The Wonderful World of Designer Germanium Quantum-Dot Transistors

P. W. Li, *Professor/IEEE DL/IEEE Senior Member, NYCU*

Abstract—Since the inception of the first transistors in the 1940s, the enormous investment and immense body of research on Group IV semiconductors, including silicon (Si) and germanium (Ge), have spearheaded spectacular and rapid advances in ULSI technology enabling a vast landscape of applications including logic, memory, computing, and sensing, etc. Although Ge was the initial semiconductor of choice for both research and industry, it was quickly superseded by Si as the active-layer material of choice for both bipolar junction transistors and MOSFETs. However, more recently, Ge-based nanoelectronics is making a comeback. In particular, Ge nanophotonics is breaking new ground as the enabling technology for Si photonics applications. Cutting-edge research on semiconductor quantum dots (QDs) has opened up access to wide-ranging applications in electronics, photonics, quantum computing, and sensing. The "holy grail" for device manufacturing is to achieve scalability through precise control and repeatable fabrication of QDs with desired shapes, sizes, and ac-curate placement for predictable electrical and optical proper-ties. A Bohr radius of 5 nm in Si dictates the fabrication of ultrasmall Si QDs, which are difficult to controllably produce using either self-assembly or lithographic techniques. In contrast, a large Bohr radius of 25 nm in Ge enables easier modification of electronic structures using Ge QDs, imposing less stringent demands on lithographic control.

Starting with our remarkable discovery of spherical Ge QD formation, we have embarked on an exciting journey of further discovery, all the while maintaining CMOS-compatible processes. We have taken advantage of the many peculiar and symbiotic interactions of Si, Ge and O interstitials to create a novel portfolio of electronic, photonic and quantum computing devices. This talk summarizes several of these completely new and counter-intuitive accomplishments. Using a coordinated combination of lithographic patterning and self-assembly, size-tunable spherical Ge QDs were controllably placed at designated spatial locations within Si-containing layers. We exploited the exquisite control available through the thermal oxidation of $Si_{1-x}Ge_x$ patterned structures in proximity to Si_3N_4/Si layers. Our so-called "designer" Ge QDs have succeeded in opening up myriad device possibilities, including paired QDs for qubits, single-hole transistors (SHTs) for charge sensing, phototransistors for Si sensing, and junctionless FETs using standard Si processing.

PEI-WEN LI (Senior Member, IEEE) received her Ph.D. degree in electrical engineering from Columbia University in New York City in 1994. Since 2015, she is a Professor in the Institute of Electronics at National Chiao Tung University (NCTU) (as National Yang Ming Chiao Tung University (NYCU) in 2021). Prior to joining NCTU in 2015, she was a Distinguished Professor, Chair of Electrical Engineering Department, and Director of Nano Science and Technology at National Central University. She was a Research Visiting Scholar at Caltech in 2011–2012. She worked with Vanguard International Semiconductor Corporation on DRAM technology integration in 1995-1996. Her research themes focus on experimental germanium nanostructures and devices, encompassing quantum-dot single-electron transistors, photodetectors, light emitters, and thermoelectric devices, making use of self-assembly nanostructures in silicon integration technology. She has published more than 300 technical journal and conference papers and holds 8 patents.
Dr. Li is an IEEE Distinguished Lecturer and has served on the VLSI Technology and Education committees of IEEE Electron Devices Society. She has been an editor of IEEE Journal of Electron Device Society since 2022 and an editorial board member of Applied Physics A, Springer since 2020. She is a senior member of the IEEE Electron Device Society and serves on various IEEE conference committees (Silicon Nanoelectronics Workshop (SNW) and Electron Devices Technology and Manufacturing (EDTM) Conference).