EDS Distinguished Lecturer Mini-Colloquium

SiC: technology, devices, modeling

organized by:	ED Poland Chapter Gdynia Maritime University Instytut Technologii Elektronowej (Warsaw)
technical support:	Lodz University of Technology, Department of Microelectronics and Computer Science
venue:	Gdynia Maritime University ul. Morska 83, 81-225 Gdynia, Poland (https://goo.gl/maps/oYALC3dPRG22)
date:	June 20, 2018

9:00-9:05 Opening

9:05-9:50

Lecturer: **Dr. Muhammad Nawaz, ABB Corporate Research, Forskargränd 7, Västerås 721 78 Sweden**

Title: **SiC technology offerings; challenges and opportunities**

Abstract: A wide bandgap SiC technology has now entered in transitional phase on various power electronics front; thanks to its superior physical properties such as wide bandgap, larger breakdown field strength, higher carrier saturation velocity, and larger thermal conductivity than that of Si counterpart. Low voltage SiC MOSFET discrete devices and power modules within voltage range of 1.2 -1.7 kV are commercially available. On the other side, medium voltage MOSFET devices of 3.3 – 6.5 kV and high voltage MOSFET devices of 10 - 15 kV are also visible in the scientific literature with excellent static and dynamic performance, illustrating the potential benefit for high power applications in energy transmission and distribution networks.

This talk will focus on the requirement and issues using SiC MOSFETs facing high power applications while addressing simultaneously the potential benefits for high power converters. Reliability concerns from the end user's perspective will be addressed as well.

10:00-10:45

Lecturer: **Prof. Simon Deleonibus, IEEE Fellow, Fellow Electrochemical Society, CEA Research Director**

Title: **On the way to the Energy and Variability Efficient (E.V.E.) Era**

Abstract: Major power consumption reduction will drive future design of technologies and architectures that will request less greedy devices and interconnect systems. The electronic market will be able to face an exponential growth thanks to the availability and feasibility of autonomous and mobile systems necessary to societal needs. The increasing complexity of high volume fabricated systems will be possible if we aim at zero intrinsic variability, and generalize 3-dimensional integration of hybrid, heterogeneous technologies at the device, functional and system levels. Weighing on the world energy saving balance will be possible and realistic by maximizing the energy efficiency of co integrated Low Power and High Performance Logic and Memory devices. The future of Nanoelectronics will face the major concerns of being Energy and Variability Efficient (E.V.E.).

10:55-11:15 Coffee break

11:15-12:00

Lecturer: **Dr. Victor Veliadis, IEEE Fellow, Deputy Executive Director and CTO, PowerAmerica**
Professor of Electrical and Computer Engineering, North Carolina State University

Title: **SiC power device fabrication and path to commercialization**

Abstract: The presentation will discuss major SiC power device application areas and touch on foundry models, cost reduction strategies, and path to commercialization. The advantages of SiC over other power electronic materials will be outlined, and SiC devices currently developed for power electronic applications will be introduced. Emphasis will be placed on SiC MOSFETs, which are currently being inserted in the majority of SiC based power electronic systems. Aspects of device fabrication will be given, with stress on processes that do not carry over from the mature Si manufacturing world and are thus specific to SiC. Finally, the presentation will highlight common SiC Edge Termination techniques, which allow devices to reach their full high-voltage potential.

12:10-12:55

Lecturer: **Henryk M. Przewłocki, Instytut Technologii Elektronowej (ITE), Warsaw**

Title: **The importance of the diffusion currents in the photoelectric investigations of the MIS system**

Abstract: The fundamental property of any nanoelectronic material or system is its energy band diagram, which allows to predict its physical properties, potential applications and/or limitations. The most effective methods of band diagram

determination are the photoelectric methods, which deserve therefore detailed theoretical analysis, as well as precisely controlled experimental procedures.

It is shown in this paper that the commonly accepted and currently applied theory (further called classical theory) of internal photoemission in the metal-insulator-semiconductor (MIS) system, which very well represents its experimental characteristics taken at high enough electric fields E, in the insulator, fails at low electric fields (usually for E<(104-105) V/cm), i.e. in the vicinity of the point where the photocurrent changes sign (I=0). This failure of the classical theory will be demonstrated by comparing the characteristics calculated using the classical theory with the experimental characteristics taken in the range of low electric fields in the insulator. It was already shown some time ago, by the present author that this discrepancy results from the neglect of the diffusion currents, which become important at low electric fields in the insulator. In this paper the origin, the magnitude and the role of diffusion current in determination of the MIS system photoelectric characteristics at low electric fields in the insulator will be quantitatively analyzed. The theory of the photocurrent vs. gate voltage characteristics, at different wavelengths of light illuminating the structure under test, with diffusion currents taken into account will be presented. It will be shown that characteristics calculated using this theory remain in good agreement with the relevant experimental characteristics. The ability to accurately predict these characteristics in the range of low electric fields opens the possibilities of developing new measurement methods of the MIS system crucial parameters. Examples of such methods will be demonstrated.

13:05-14:05 Lunch break

14:05-14:50
Lecturer: **Prof. Mike Brinson, Centre for Communications Technology, London Metropolitan University**
Title: **Verilog-A compact modelling of SiC devices with Qucs-S, QucsStudio and MAPP/Octave FOSS tools**

Abstract: The purpose of this presentation is provide an overview of the fundamentals of the Verilog-A hardware description language and its use in compact modelling of established and emerging semiconductor technology devices. With the adoption of Verilog-A as the standardised model interchange language by CMC, a knowledge of this subject is of increasing importance to the modelling community. Similarly, access to freely available Verilog-A modelling tools and circuit simulators is essential if Verilog-A modelling techniques are to be widely adopted. For this reason, in an attempt to encouraging all who attend to experiment with Verilog-A. the presentation is based on the Qucs-S, QucsStudio and the MAPP/Octave FOSS software. Throughout the talk a series of modelling case studies outline the stages in the development of Verilog-A models for established and SiC semiconductor devices. In the later stages of the presentation participants are also introduced to using the Berkeley MAPP tools with Qucs-S/Xyce.

15:00-15:45
Lecturer: **Dr. Wladek Grabinski, MOS-AK (EU)**
Title: **FOSS TCAD/EDA Tools for Advanced Compact Modeling**

Abstract: Compact/SPICE models of circuit elements (passive, active, MEMS, RF) are essential to enable advanced IC design using nanoscaled semiconductor technologies. Compact/SPICE models are also a communication means between the semiconductor foundries and the IC design teams to share and exchange all engineering and design information. To explore all related interactions, we are discussing selected FOSS CAD tools along complete technology/design tool chain from nanascaled technology processes; thru the MOSFET, FDSOI, FinFET and TFET compact modeling; to advanced IC transistor level design support. New technology and device development will be illustrated by application examples of the FOSS TCAD tools: Cogenda TCAD and DEVSIM. Compact modeling will be highlighted by review topics related to its parameter extraction and standardization of the experimental and measurement data exchange formats. Finally, we will present two FOSS CAD simulation and design tools: ngspice and Qucs. Application and use of these tools for advanced IC design (e.g. analog/RF IC applications) directly depends the quality of the compact models implementations in these tools as well as reliability of extracted models and generated libraries/PDKs. Discussing new model implementation into the FOSS CAD tools (Gnucap, Xyce, ngspice and Qucs as well as others) we will also address an open question of the compact/SPICE model Verilog-A standardization. We hope that this presentation will be useful to all the researchers and engineers actively involved in the developing compact/SPICE models as well as designing the integrated circuits in particular at the transistor level and then trigger further discussion on the compact/SPICE model Verilog-A standardization and development supporting FOSS CAD tools.

15:55 Closing