1st Region 9 EDS Application Specific Integrated Circuit Contest

In September 2020, EDS Region 9 launched the EDS ASIC Design Contest.
Thirteen proposals out 15 proposals from 6 different Region 9 countries were selected.
EDS approved US$25K to cover the fabrication with the 180 nm Europractice TSMC MPW.

1. Conditioning system and digital biomedical signal, **Mexico**.
2. Receiver for Internet of Medical Things (IoMT) and ADC Converters, **Mexico**.
3. Low Power circuits for Biomedical Applications, **Brazil**.
4. A RISC-V Based MCU With a 15000 Tuning Range Feed-Forward Ring Oscillator for Multi-Protocol Support Applications, **Colombia**.
5. Delay-based Temperature Sensor for IoT applications , **Ecuador**.
6. FEI2020 and ProjectFEI2020, **Brazil**.
7. Low Power Analog and Mixed-Signal blocks for IoT interfaces, **Brazil**.
8. Passive RFID reading range enhancement using energy harvesting techniques, **Uruguay**.
9. ELAPSE Electronics for pArticle PhysicS Experiments, **Chile**.
10. A Current Limiter Circuit with GaN Power Switch for Payloads Protection, **Brazil**.
11. Design of Ultra Low Voltage Energy Harvesting Converter for IoT applications ULV-EH, **Brazil**.
12. Design of a CMOS Circuit for a Fully Integrated Electro photonic Lab-On-A-Chip, **Mexico**.
13. Design of Ultra Low Voltage Energy Harvesting Converter for IoT applications, **Brazil**.

A total of 24 PhD, 22 MsC, 8 undergraduate students, and 22 Professors participated in the 13 projects. In February 2021, US$25K were approved by EDS for the 2nd contest, which calls for projects to be launched in the second half of 2021.

Call for R9 EDS/IEEE Student ASIC Design Fabrication

EDS approved funding of ASIC MPW fabrication run including up-to 9 designs for EDS student members in Region 9 (Latin America and Caribe), for a total of US$ 25,000.00

For this, we launch a call for proposals as follows:

- Technology TSMC 0.18um MS/RF
- Europractice MPW run of May 2021
- Maximum design area: 1660 x 1660 microns
- Delivery: free samples (dies), maximum 40
- Packaging: free up to 700 euro/proposal
- Additional details: https://europractice-ic.com/

Selection criteria:

- University located in R9
- Maximize the distribution of selected projects over the region
- Maximum of one design/university
- Advisor professor and main student being EDS member
- Number of students involved
- Available EDA tools, characterization plan and infrastructure
- Quality of the ASIC proposal: originality, innovation, complexity (not too simple or too complex)
- Experience in ASIC design of the advisor professor
- Commitment to tape-out on pre-defined date
- Commitment to report results after 3 months after receiving the chips.
- Commitment to participate at a virtual program workshop to share results

Deadline dates:

- Proposal submission: Nov 3st, 2020
- Selection outcome: Nov 23rd, 2020
- GDS II tape-out: May 1st, 2021.
- Shipment of the chips: around Mid Sep, 2021
- Report submission: Jan 11, 2022
- Workshop report presentation – special session at LAEDC2022.

Proposal Submission address:

- edmundo@inaoep.mx

Management & Selection Committee:

- Edmundo Gutiérrez, INAOE, Mexico
- Elkim Roa, UIS, Colombia
- Jacobus Swart, UNICAMP, Brazil