Introduction to the 2006 International Integrated Reliability Workshop (IIRW) Special Issue

I. Introduction

The papers in this special issue of IEEE TDMR were selected from the International Integrated Reliability Workshop (IIRW), which was held October 16th to 19th, 2006 at the Stanford Sierra Camp on the shores of Fallen Leaf Lake near South Lake Tahoe, CA. This annual workshop, sponsored by the IEEE Reliability Society and the IEEE Electron Devices Society, provides a unique forum for open and in-depth discussions of all areas of semiconductor reliability research and technology.

Unlike typical technical presentation focused conference, the setting of IIRW encourages the interaction among all attendees. Attendees stay in cabins without TVs or phones, dress is casual, and meals are provided at the family-style lodge dining room. Attendees are expected to participate actively and are drawn into technical discussions from the start. Days are packed with oral presentations, and short courses, while evenings are spent in reliability discussion groups, poster sessions, and special interest groups (SIGs). The fresh mountain air can stimulate discussions late into the night.

The collection of articles presented here is intended to provide a flavor of the results presented and discussions held at the workshop and should be of great interest to anyone working on all aspects of advanced MOS device, circuit, and material reliability. In addition to this special proceeding issue, the workshop also publishes a Final Report.

II. Editorial Preview

There are 14 invited papers in the special IIRW 2006 Proceedings Issue. The first two papers focus on device reliability, followed by four papers on back-end reliability, two paper on wafer level reliability, three papers on memory reliability and e-fuse reliability, along with two papers on high-k, and the final paper on ESD.

J. M. Roux, D. Roy and P. Abramowitz from STMicroelectronics and X. Federspiel from Philips investigate the impact of self-heating on the Hot Carrier Injection (HCI) lifetime prediction for SOI technology. Based on their study, a method is proposed to correct the HCI dataset from self-heating contributions, and thus obtain an accurate estimate of HCI lifetime prediction.

C. Guerin, A. Bravaix and M. Denais from STMicroelectronics and V. Haurd from Maisondes Technology focus on the Channel Hot Carrier (CHC) degradation mechanisms in nFETs at the 45 nm and 65 nm nodes. This study applies both the charge pumping (CP) and DCIV measurement methods to determine the density and spatial extent of the interface traps, and thereby shows that there are two different CHC degradation regimes which depend on the gate voltage (V_g). The study also highlights the need for relevant model that would take into account the high V_g regime.

The next four papers focus on reliability problems in back-end including capacitors and resistor in mixed signal applications.

X. Federspiel, L. Doyen from Philips, and D. Ney, and V. Girault from STMicroelectronics combine physical analysis of failed parts with in-depth analysis of resistance evolution in dual damascene Cu lines subjected to electromigration stress. From this analysis they extract activation energy from single samples as well as information about liner properties and fabrication process.

A. Bajolet, S. Bruyere and M. Proust of STMicroelectronics and L. Montes and G. Ghibaudo of IMEP examine the impact of TiN post-treatment on charge trapping in alumina layers in a three-dimensional metal-insulator-metal (MIM) capacitor. Comparison of CVD and PVD TiN deposition process effects on the alumina layer are discussed.

Y Li, G Groeseneken, K. Maex and Z. Tokei from IMEC analyzed conduction mechanisms in advanced low k by means of intermittent capacitance measurement during voltage stress. They evidenced changes of the donor/acceptor densities from I-V curve slope evolution aside from dominant bulk conduction.

R Bryndsvold from Analog Devices investigates wear out mechanisms in SiCr resistive devices under constant current stress. An accurate analysis of resistivity and TCR was performed to obtain a fair comparisons of devices issued from different production sites and to establish robust design rules. Additionally, a physical origin to the resistance changes detected during wear out is proposed.

The two wafer level reliability papers focus on electromigration and TDDB.

O. Aubel from AMD and T.D. Sullivan, D. Massey, T.C. Lee, T. Merrill, P. Polchlopek, A. Strong from IBM presents various normalization procedures applicable to wafer level electromigration tests, including, cross section and TCR corrections. Using theses procedures, the authors analyzed the evolution of electromigration activation energy as function of line width.

The second paper is from Andreas Aal from Elmos Semiconductor AG. The authors present a method to generate TDDB data with high accuracy from linear ramped voltage test. Such a method is very useful for performing fast lifetime projection for gate oxides. Compared to conventional Constant voltage stress (CVS) based TDDB tests, the new method offers a much faster test, resulting in reduced costs for process qualification and WLR-monitoring.

The following three papers review reliability issues associated with NiSi Polycide eFuses and embedded Flash Memory reliability.

B. Ang, S. Tumakha, J. Im and S. Paak from Xilinx describe eFuses in the 65nm node. Optimal programming stimulus and mechanisms are described, and a study on the limitations of reliability for un-programmed eFuses versus read current limits is discussed.

H. Suto, S. Mori, M. Kanno, N. Nagashima from Sony investigate dopant dependant eFuse properties. A discussion of the current flow and it's effect within the silicide layer and the polysilicon layer is analyzed.

G. Tao, H. Chauveau, S. Nath from NXP Semiconductors study the endurance of a 2T-FNFN NOR flash memory cell that is embedded in a 0.13µm technology node. An empirical model describing the degradation in the program window as a function of temperature is described.

In the final papers of the special issue, focus is shifted to high-k reliability.

S. Jakschik, M. Kerber from Infineon, T.h. Kauerauf, R. Degreave from IMEC, Y.N. Hwang from Samsung, R. Duschl, A. Avellan, S. Kudelka from Qimonda discuss the influence of stress-induced leakage current in HfSiO devices under substrate injection conditions. Most of the degradation was attributed to damage in the high-k layer and not at the interface with silicon.

J.-P. Manceau, S. Bruyere, S. Jeannot from STMicroelectronics, A. Sylvestre from LEMD, P. Gonon from LTM investigate the current instability and permittivity variation with frequency for Ta_2O_5 capacitors where three types of phenomena are observed: polarization current, Poole-Frenkel conduction, and a resistance degradation phenomenon. A model for oxygen vacancy migration is also proposed.

The last paper of the special issue is by Wei-Jen Chang and Ming-Dou Ker from National Chiao-Tung University who investigate the dependences of device structures and layout parameters on ESD robustness in a 40-V CMOS chips, and conclude that the high-voltage (HV) MOSFETs without drift implant in the drain region have better TLP-measured It2 and ESD robustness.

The cross section of the work presented at IIRW that appears in this issue should allow the reader to come away with a deeper understanding of the latest reliability challenges.

III. Acknowledgements

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