Introduction to the Special Issue on Failure Analysis of Integrated Circuit Devices and Packages

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I. INTRODUCTION

As the demand for better device performance continues to shrink devices, package size and features are also shrinking. There is a trend for both horizontal and vertical stacking of the devices to meet the demands of the higher performance devices for microprocessors, Flash memory, micro-controllers, etc.

TECHNICAL TRENDS

Moore's Law, a doubling of transistors every 18-24 months, has driven profound changes in packaging technology to accommodate the resultant performance gains. Some of the key technology trends contributing to this revolution in packaging have been increasing die size (7% annually since 1970), increasing transistor count (5k to 42M) and increasing power density (W/cm^2) by 30X.[1] The impact of this trend on packaging has driven package interconnects more than 6-fold in the last 5 years, increased via counts, and decreased metal line widths and spaces.[1] This in turn has driven bump fatigue (due to reduced compliance of smaller bumps), metal migration, and electromigration concerns. The power dissipation requirements have driven the need for compliant, adherent thermal interface materials that endure temperature cycling without loss of thermal conductivity. Another significant challenge is the integration of mechanically weak Cu/low-k dielectrics at the $\leq$ 90nm node with organic packages that induce thermal mechanical and mechanical stress. Packaging plays bigger role beyond interconnection; provides peripheral performance enhancements; VRM, embedded components.

In addition to the high performance packaging challenges, there is an explosion of package technologies to satisfy the needs of the communications and other emerging market segments. Some of these products are cell phones, PDAs, routers, hubs, switches, memory devices, flash cards, network processing units, optical devices (switches, amplifiers, diodes), and MEMs (accelerometers for air bags, ink jet printers, digital mirror devices for in focus projectors, in-situ pumps). This rapid development of applications has led to a bewildering array of packages such as chip scale packages (CSP), molded matrix array packages (MMAP), system on a chip (SOC), system in a package (SIP), stacked chip scale packages (SCSP) to service this divergent marketplace. Low cost driving new pkg alternatives (eg. Flex) which my have rel implications or not depending on market segment Some of the key challenges associated with this diverse population are reliability in harsh environments, stiction, corrosion, thermal management, and mechanical stability of optical paths.

On the integrated circuit device site the Gate oxide thickness has been reduced to a few nm in thickness. Gate width is under 20nm. As features get smaller the non-visible defects will be increasingly significant and will require electrical characterization at the die level to be resolved properly. Copper has replaced Aluminum for interconnect, and the number of interconnect layers has increased to more than 9. This has the effect of blocking light from escaping from the front of the die, which precludes many frontside optical based diagnostic tools like PEM (Photo Emission Microscopy). The growing thickness of the metal stack makes it increasingly difficult for laser heating methods like OBIRCH (Optical Beam Induced Resistance Change) to penetrate into the metal stack and therefore it limits its ability to resolve defects.

For the above reasons backside diagnostic tools are increasingly used to localize defects – and die thinning is required for the technique to be effective. Backside sample preparation significantly increases the complexity of preparing samples for analysis – particularly for dynamic diagnostic tools that require the part to be operated at maximum frequency docked to an ATE system.

New materials complicate analysis tasks. Copper metallization requires a modified approach to FIB based circuit editing, including editing done to facilitate failure analysis probe access. Low-k dielectrics present both mechanical and deprocessing issues. The dielectric is weak which causes problems for parallel and cross sectioning. Low-k is porous which causes challenges for chemical and plasma etching for deprocessing. It also causes charging issues for SEM imaging.

On the environmental side -- The industry trend to centralizing analysis capability has the implication that companies may buy fewer of the increasingly expensive diagnostic tools, reducing the TAM (Total Available Market) for these new diagnostic tools. This tends to reduce the motivation for vendors to spend the millions of dollars necessary to bring a tool into reality.

The increased pace of markets drives the need for getting a product to market soon. Customers want analysis results and corrective action on a rapid schedule – This requirement and the increased complexity of the parts required to be analyzed raise significant challenges. Additionally, the global nature of manufacturing makes the task of effective information sharing challenging. Problems can originate at any stage of design, development, and manufacturing and can affect one or many products that share similar design elements, components or processes. The diagnostic focus is often customer based. The challenge is to have a knowledge base that propagates information critical to problem solving and corrective action to the various locations within the organization tasked to resolve the problem.

II. EDITORIAL PREVIEW

There are four invited papers in this special Failure Analysis of Integrated Circuit Devices and Packages issue.

The special issue begins with an overview of the challenges in the failure analysis. The first paper by David Vallet illustrates how the need for improved analytical capability is rapidly outpacing the development of instrumentation and methods, and to recommend steps that must be taken before failure analysis becomes cost and/or time-prohibitive, or altogether obsolete. This paper has briefly summarized the challenges facing the semiconductor FA community, and by extension the entire industry. It has then discussed the lack of R&D and especially the acute need for development and commercialization of revolutionary analytical instruments needed to maintain viability. Two major barriers to such innovation exist – finding sources of new technology, and creating a fertile business infrastructure to support development. The authors have also proposed a solution as well.

Balu Pathangey el al. has discussed the effect of package level contamination on the product reliability and the techniques and challenges of identifying these contaminants. They have described the surface analytical techniques that are primarily used as problem solving tools as part of the framework of failure analysis. This includes such things as materials selection or comparison, assembly process excursions and reliability failures. However, we make extensive use of optical imaging, SEM/EDX (Scanning Electron Microscopy /Energy Dispersive X-ray spectroscopy), FTIR (Fourier Transform Infra Red spectroscopy) and occasionally use AES (Auger Electron Spectroscopy). The multi-technique approach is a well-established methodology for analytical problem solving. From the reliability perspective, it is essential to achieve integrity at all internal interfaces in the flip-chip, wire-bond and novel mixed technology packages. In many instances, both organic and low level ionic contaminants have resulted in interface delamination, metal migration, micro-cracking, etc., leading to premature failure of products either in reliability tests or in the field. This paper will present several examples of failure analysis relating to package contamination in the assembly world and the effectiveness of Time Of Flight Secondary Ion Mass Spectroscopy (TOFSIMS) in isolating and understanding failures are highlighted in this paper.

The paper by Ulrike Kindereit, et al. presents a systematic investigation of LVP signals on isolated CMOS transistors across a wide range of parameters. They show that the LVP effects of interest are based on free-carrier effects. Their measurements agree qualitatively in magnitude and behavior with a simple physical model. This paper presents a thorough understanding of LVP physics that allows extraction of detailed voltage information, knowledge about such practical issues as probe placement, and prediction of the scaling of LVP signals on future process technologies.

Finally, in the review article by Glowacki, et al. they first start with the laser stimulation (LS) basics and the description of various localization techniques based on LS. After that, they present the application of scanning laser beam to stimulation of various devices present in modern integrated circuits (ICs) from both front and back sides of the silicon chip. They begin from simple metallic and polysilicon interconnects, then describe the interaction of the laser with thermoelectric device and end with the laser stimulation of active devices like diodes and MOSFETs. Models aimed at understanding of laser stimulation effects in such devices have been discussed as well.

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