Introduction to the Special Issue on Smart Power Device Reliability.

Introduction

Smart power devices and technologies try to combine high density CMOS logic with power handling capabilities on one single chip, with voltages and currents in the range of 20-150V and 1-10A respectively. Such technologies are used in various application areas such as automotive, industrial, telecom and consumer electronics. The required robustness in a harsh environment (e.g. high-energetic pulses, high ambient temperatures, local hot spots, etc..) pushes the devices and the technologies to their limits in terms of reliability. Hence, a detailed reliability study and an in-depth understanding of the physical mechanisms in smart power devices, is mandatory.

This special topic issue of IEEE Transactions on Device and Materials Reliability documents on the recent progress in the area of reliability of smart power devices. These high voltage/power devices such as LDMOS and DeMOS are increasingly integrated into advanced process technologies for mixed signal IC applications e.g. smart low-side and high-side drivers, motor and relay driver/controllers, printer and display drivers/controllers, audio amplifiers, xDSL line drivers, high efficiency power management circuits for AC/DC conversion and DC/DC conversion (programmable buck, boost and linear regulators). Reliability challenges in these devices are gaining more attention in the industry. This issue contains one review paper and several contributed papers covering a range of topics on reliability physics, characterization and failure mechanisms of smart power devices. This collection of articles will be of great interest to anyone working in the field of smart power reliability.

Editorial Preview.

There is one review and eight contributed paper in this special issue on smart power reliability. The first four papers focus on the study of the location of the degradation induced in lateral DMOS transistors under hot carrier stress, and the relation to the impact on the shift in transistor characteristics. The five other papers are focusing on the transistor behavior under adverse pulse conditions, and the modeling of the parasitic transistor effects thereof.

The special issue begins with an overview paper on how to characterize the total Safe Operating Area on integrated power transistor for short and medium time pulses (ns – ms) and under hot carrier conditions. Different measurement and characterization techniques, as well as the modeling, are highlighted. A methodology to build the total SOA is highlighted and experimentally verified.

The second paper by C. Cheng et al. presents a novel three-level charge pumping technique to characterize hot carrier induced degradation in different regions in a n-type LDMOS. The trap location and the properties of various stress modes and their impact on the device characteristics has been analyzed. A nice correlation between the device degradation and the charge pumping results is achieved. A physical explanation is provided, supported by device simulations.

Continuing on this theme, D. Brisbin et al. focuses on the understanding of anomalous hot carrier results obtained on a LDMOS with varying drift implant dose. Increasing the drift doping concentration yields an –expected— increase in substrate current, but resulted in a lower hot carrier degradation. Charge pumping, hot carrier and device simulation results suggest that the drift dose impacts the location of maximum impact ionization, hence device degradation. In addition, at low gate voltage, hole trapping in the device birds beak area results in an improved device performance.

K.M. Wu et al. correlated hot carrier degradation phenomena in 0.5 µm 12V drain extended MOS transistors with the nldd dose and identified two different degradation mechanisms to be responsible for the observed effect i.e. channel and drift region hot electron injection and hot hole trapping in the accumulation region of the device.

The next five papers are on parasitic transistor effects in smart power devices, occurring when the devices are subjected to adverse pulse conditions. S. Schwantes et al. discuss in much detail the back gate bias dependency of the on-state breakdown voltage of lateral DMOS transistors on SOI. It is shown that the back gate bias significantly affects the breakdown voltage and therefore the safe operating area of the device. Important circuit design implications are highlighted. Furthermore the paper presents a detailed analytical model for the back gate bias dependency. The model is verified on silicon.

Next, R. Zhu et al. indicate that substrate majority conduction can become a severe issue for advanced smart power technologies in terms of parasitic latch-up and excess power dissipation. A multi-isolated device approach is proposed and experimentally verified. The device safe operating area, however, is degraded with the new approach. By drain drift engineering the safe operating area can be recovered.

P. Moens et al. report on the high ruggedness of a vertical integrated nDMOS under TLP pulsed conditions, being attributed to the simultaneous activation of both a lateral and a vertical parasitic bipolar transistor. As such, current capabilities in excess of 90 mA/µm can be achieved for small devices. A model to predict the thermal failure current out of the device width, is provided.

On the same topic, C. Salamero et al. present a new method to predict the ESD protection robustness of a device with TCAD simulations. Tested on different devices and two Smart Power technologies, the results are validated through electrical measurement and failure analysis. The methodology provides a significant simulation time speedup compared to classical methods based on a temperature criterion.

In a final paper, J. Oehmen et al. present a comprehensive model for parasitic transistors in junction isolated smart power ICs. The model accounts for inhomogeneous current flows and high electrons densities and can predict substrate currents at high injection levels. The model allows to indicate inadmissible substrate currents already in the design phase.

The reader of this issue will have a deeper understanding of the reliability aspects of smart power transistors, and will appreciate the many challenges in terms of robustness and reliability of smart power technologies. It is hoped that this issue can serve to guide work in this challenging area.

Acknowledgment

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Peter Moens,
AMI Semiconductor Belgium BVBA
Oudenaarde, Belgium
e-mail: peter_moens@amis.com

Prasad Chaparala
National Semiconductor Corp.
Santa Clara, CA, USA
e-mail: prasad.chaparala@nsc.com