Guest Editorial Introduction to the Special Issue: High-k Reliability—Status 2009

I. Introduction

THE gate dielectric made of SiO_2 has been scaled to the point where it can no longer satisfy future transistor-scaling requirements. This has prompted many researchers and companies to investigate suitable SiO_2 replacement for their logic applications. For these applications, Hf-based materials have been demonstrated as suitable, meeting all the requirements set forward for logic applications. Such requirements include, but are not limited to, gate-stack capacitance (or equivalent oxide thickness), mobility, I_{ON}/I_{OFF} performance, V_T control, and scalability.

Throughout this transition, high-k materials have grown in importance outside the logic-device development arena. New applications for these dielectrics are foreseen into the field of nonvolatile-memory applications, resistive RAM, microelectromechanical switches, and so forth. With such a large variety of applications, large variations in the processing conditions, as well as testing conditions, are found in literature.

In review of such findings, one may wonder whether the experimental techniques and the fundamental learning cumulated during the past years provide enough confidence in the high-k materials in meeting the reliability requirements for such widespread applications. In other words, one may wonder whether some conclusions are generally applicable to all gate stacks. As a matter of fact, the high-k quality and properties critically depend on the material composition and temperature considered. Therefore, studies on reliability methodology and nature of defects are extremely valuable and timely.

The aim of this Special Issue on high-k reliability is twofold: first of all, to provide a general overview on the key learning from the past and present on reliability. Second, to present the state of the art on reliability and characterization of these advanced gate stack.

II. Editorial Preview

There are five invited papers in this Special Issue on high-k dielectric—status 2009, each addressing important topics surrounding the use and implementation of high-k dielectrics. Topics include high-k dielectric reliability, characterization methodology, defect generation and their impact on gate-stack quality, noise generation and its effect on device performance, and new applications with respect to microelectromechanical-system (MEMS) devices.

In the first paper, Kerber and Cartier investigate in detail the reliability challenges for HfO_2/TiN. Details of the gate stack including high-k composition, thickness, quality, and interfacial-layer integration are extremely important, since they affect the electrical parameters one can measure. Using several experimental techniques—transient VT instability, charge pumping, and noise during CVS—the authors discuss defect locations and behavior in the gate stack. Furthermore, charge trapping and detrapping has important consequences both for the reliability extrapolation as well as the asymmetric-polarity behavior. For example, the time-to-failure under alternate stress is $10\times$ lower as compared to the conventional constant-voltage test.

The issue in which traps are responsible for breakdown is also addressed in the second paper from Hirano *et al.* In their paper, the authors extensively investigate the impact of fluorine incorporation in the HfSiON as a way to effectively passivate electrically active defects in these layers. F incorporation also reduced the defect-generation rate as measured using stress-induced leakage current. As a result, the overall reliability was improved, and the authors therefore concluded that the nature of generated traps corresponds to that of preexisting traps.

The third paper from Kang *et al.* investigates an alternative (important) technique in modifying the gate-stack properties by capping the high-k with rare-earth materials. Kang *et al.* has thoroughly investigated the impact of capping layers on reliability and defect transient charging effects. Rare-earth materials incorporation provided a dramatic change in electrical properties, and these effects were generally understood in terms of charged defects.

While most of these studies mainly focused on reliability methodology and improvements, Magnone *et al.* focused on the impact of high-k and associated defects in the low-frequency noise. This is an important topic, particularly toward the use of these materials for digital and analog circuits (i.e., analog amplifiers, mixers, etc.). Magnone *et al.* investigated the gate-stack impact (i.e., high-k defects) on the 1/f noise, both from the drain current as well as the gate current. The authors concluded that the interfaces between the SiO_2 and the high-k as well as the high-k and the top electrode are both important to reduce the noise in the system.

The last paper of this Special Issue deals with high-k applications for MEMS. MEMS is a booming field and deals with the integration of mechanical elements, sensors, actuators, and electronics on a common silicon substrate through microfabrication technology. Dielectrics in MEMS can fill the role of sacrificial, structural, optical, masking, passivation, a

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thermalization, etch stop, insulator, and (for integrated packaging) encapsulation layer. Therefore, the high-k requirements are very different from the ones for logic and memory in terms of thickness quality and composition. De Groot *et al.* provides an extensive review of the prevalent failure mechanisms resulting from the use of dielectrics in electrostatically driven MEMS devices and methods to characterize both their material properties and impact on reliability performance.

The reader will come away with a deeper understanding of the reliability and characterization issues associated with the high-k materials. An important challenge for reliability assessment is "which defects are important when considering long-term degradation and reliability degradation" and how to link them to the engineered gate-stack quality.

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