# Introduction to the Special Issue on the 2009 International Reliability Physics Symposium

## I. Introduction

ON APRIL 26–30, 2009, the 47th Annual IEEE International Reliability Physics Symposium (www.irps.org) was held in Montreal, Quebec, Canada. For nearly 50 years, IRPS has been the leading conference in the area of microelectronics reliability. This was the first year that the symposium was held outside of the U.S., and it received a record number of paper submissions. The technical program included 18 invited talks in addition to 96 contributed talks and 78 posters. The papers document a strong interest in the fundamental reliability of transistors, interconnects, and back-end dielectrics, as well as memory devices, circuits, product qualification, failure analysis, process and integration impact on reliability, ESD and latchup, compound semiconductors, soft errors, packaging, extreme environments, high voltage, and thin-film devices. From this strong technical field, this Special Issue features three selected papers on topics of ongoing and lasting interest. These papers are extensions of presentations given at the conference.

## II. Editorial Review

The paper by S. Ramaswami *et al.* from Applied Materials, Inc., describes the methods for integration of through-silicon vias. This technology is emerging as a means for dense versatile 3-D integration, yet, as the authors remind us, much remains to be done in aspects such as defect management, testing, and reliability in order for this technology to become mainstream.

T. S. Kim and R. H. Dauskardt of Stanford University review the reliability issues for nanoporous low-$k$ materials for back-end dielectrics. The mechanical properties of such films make them prone to cracking and delamination, and Kim and Dauskardt describe ways to improve these properties by depth-dependent UV curing.

P. Moens and coworkers of ON Semiconductor discuss trench-based power devices for integrated smart power technologies. Hot carrier effects and trench gate oxide quality are studied in detail, and the authors demonstrate that these devices can achieve much higher power density at snapback, compared to competitive technologies.

The Guest Editors would like to thank T. Oates, Editor-in-Chief, for the opportunity to make these papers available to the T-DMR readership, and J. A. Marsh, T-DMR Administrative Support, for her constant and patient guidance through this process. We particularly thank the anonymous reviewers, who worked under a tight deadline and who, without exception, provided thoughtful and constructive comments which led to improvements in these already outstanding papers.

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