Introduction to the Special Issue on Negative Bias Temperature Instability

I. Introduction

NEGATIVE bias temperature instability (NBTI) is a significant reliability concern for submicrometer CMOS technologies. NBTI in PMOSFET devices is not a recently discovered wearout mechanism. It was originally observed in the early phases of CMOS development almost 40 years ago but was not considered of great importance because of the low electric fields in operation. However, technology scaling has resulted in the convergence of several factors, which have together made NBTI the most critical reliability concern for deep submicrometer transistors. These trends include the introduction of nitrided oxides (required to reduce boron penetration in p^+ poly PMOSFETs) as well as the increase in gate oxide fields and operating temperature with technology scaling.

Tremendous amount of research has been carried out by both the industry and academia over the last few years, resulting in significant advances in our understanding of NBTI. However, some key aspects of the physics of NBTI remain controversial. In particular, questions related to gate oxide nitridation and its relation to hole trapping and interface states generation, and the appropriate choice of stress/test methodologies to characterize NBTI remain unresolved. Additionally, the impact of the NBTI in new materials like HfO_2 gate stacks is beginning to attract attention, given the possible use of these high-K films in 45-nm technologies and beyond.

II. Editorial Preview

This Special Issue on NBTI of the IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY (TDMR) focuses on the recent progress in the aforementioned areas. The seven invited papers in this Special Issue are intended to reflect the current thinking among different researchers on the controversial aspects of the NBTI mechanism. The next issue of TDMR will include several papers that provide viewpoints of other researchers on some of the same topics.

We start by treating a key aspect of the NBTI mechanism: What is the correct way to characterize NBTI? Reisinger *et al.* give an overview of the currently adopted three fast measuring methods, namely "on the fly," fast direct threshold voltage Vt, and fast drain–current switching method. The possible problems with the different methods are discussed, and the systematic and statistical errors involved are analyzed.

The other group of three papers addresses particular aspects of the NBTI physics. Tsetseris *et al*. highlight the role of hydrogen in contributing to the NBTI through first principles calculations. In particular, they propose an alternative picture where depassivation of the Si–H bonds is assisted by extra H^+ species that are released in the substrate and reach the interface under the influence of the applied stress bias.

Campbell *et al.* use a combination of dc gate-diode measurements, spin-dependent recombination, and tunneling magnetic resonance techniques to identify the nature of the defect responsible for NBTI. They confirm that the NBTI mechanism in SiO_2 gate oxides is dominated by the generation of Pb_0 and Pb_1 interface defects. They also suggest that in plasma-nitrided oxide, a new type of Si–N defects is generated. Different defects are involved in the NBTI damage generated in the HfO_2-based oxides as well.

Rauch gives a review of the understanding and modeling of the statistical nature of the NBTI-induced interface damage. The author critically examines the NBTI-induced threshold voltage shift distributions and the accuracy of the normal approximations that are commonly used today.

The last two papers of this Special Issue focus on circuit level simulation of NBTI. Huard *et al.* introduce a design-in-reliability methodology to quantify the degradation due to hot carriers and NBTI in 90-nm as well as 65-nm technologies. This simulation tool is built on top of an existing analog simulator ELDO. The impact of these two degradation modes on circuit level aging is analyzed in several typical circuits.

Wang *et al.* propose a unified approach that directly predicts the change in transistor parameters under various process and design conditions for both NBTI and channel hot carrier effects. Models are verified in a 65-nm technology where it is observed that NBTI is the dominant reliability concern for circuit performance.

The last invited paper of this issue investigates the NBTI damage in a PMOSFET with a HfSiON–SiO2 gate stack. By using a fast transient measurement technique, Tang *et al*. observe that in certain stress conditions, the NBTI induced instability evolves from enhancement mode to degradation mode, giving rise to an anomalous turn-around evolution with stress time and stress gate voltage. A bipolar charge trapping model along with trap generation in a HfSiON gate dielectric is proposed to account for the observed phenomena. These observations are further confirmed by charge pumping and carrier separation measurements and a model describing the drain–current instability due to the NBTI voltage, temperature, and time dependence is developed.

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