Title: Memristive Dynamics Based Hardware Primitives for Efficient Computing

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Non-von Neumann architectures based on emerging memristive devices, such as ReRAM, PCM, etc., hold great prospect in constructing AI devices with extremely high energy efficiency that could bloom applications in edge computing. The introduction of analog nonvolatile memories allows both inference with high energy efficiency, and training as well. Throughput and energy efficiency of inference are strongly dependent on exercised neural network topologies, computational precision and network sparsity, and the chip design requires optimized mixed-signal circuit design, chip architecture and data flow, etc. On-chip local training is highly desirable for the application of deep neural networks in environment-adaptive edge platforms, which however is hindered by the high time and energy costs of training. Direct feedback alignment provides a viable choice for local learning when combined with transfer learning in convolutional layers, which can be achieved by exploiting the inherent stochasticity in the conductance states of phase change memory chip. Besides, a hardware spiking neural network circuit is constructed based on hybrid weight elements combing different memristive dynamics, which demonstrates temporal correlation detection after online unsupervised learning. We also developed a memristive optimizer hardware based on Hopfield network, which introduces transient chaos to simulate annealing in aid of jumping out of the local optima while ensuring convergence. A continuous function optimization problem as well as a NP-hard combinatorial optimization problem are experimentally demonstrated, therefore indicating great potential of the memristive optimizer as future computing platform for solving optimization problems in general.