

Manufacturing Challenges of High-k Materials – an Industry Perspective
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In the early days of the search to find a replacement for SiO₂-based gate oxides the goal was to find a material with a very high k value which could be incorporated into CMOS production for multiple technology nodes. A retrospective of the many promising high k materials considered for SiO₂ replacement, leading to the selection of Atomic Layer Deposition of Hafnium Oxide (ALD HfO₂) as “the winner” will be presented. ALD HfO₂ has successfully been implemented in CMOS production for 15 years, starting at the 45nm node. There are two general integration approaches for implementing ALD High-k/Metal Gate stacks (HKMG) in production: gate first and gate last. Manufacturing challenges with each integration approach, leading to the wider adoption of gate last will be discussed. Furthermore, as the dielectric constant of HfO₂ is only ~20 and a thin SiO₂- base interface was still required to maintain mobility and reliability, HfO₂ provided essentially a one-time scaling benefit. Further thinning of HfO₂ resulted in unacceptable leakage and thus, to continue transistor scaling, fully depleted devices such as FINFET and Ultra-Thin Planar SOI (FDSOI) were pursued. High volume manufacturing flows for FINFET (with gate last integration) and FDSOI (with gate first integration) come with their own unique challenges. For example, with FINFET maintaining gate height uniformity is crucial for V_t targeting and control. With FDSOI, maintaining gatestack stability at high temperature is key. To continue future scaling, new device architectures (e.g. GAA, CFET.) will pose further challenges for gate stack integration. Recent and historical progress in HfO₂ growth, interface control, selective deposition, morphology, and etching will be discussed about the possibility for future gate stack engineering.