

Past, Present, and Future of CMOS Scaling – An Academic Perspective

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For decades, CMOS scaling has been the key driving force in digital electronics. While scaling has always been demanding, recently more and more people in the electronics community express concerns about a slowing down and an approaching end of CMOS scaling. On the other hand, chipmakers still proceed with scaling and a lot of processing innovations and novel new transistor architectures are explored. In the present webinar, we walk through the evolution of CMOS scaling, starting with Dennard's scaling rules elaborated in the early 1970s at IBM and ending with two major achievements from the past months – the demonstration of stacked nMOSFET-on-pMOSFETs reported by Intel engineers at IEDM 2020 and the announcement of IBM's 2-nm technology in May 2021. We discuss the four stages of scaling, i.e., (i) traditional scaling and (ii) equivalent scaling of conventional single-gate MOSFETs, (iii) FinFET scaling, and (iv) scaling of gate-all-around stacked nanosheet channel FETs. Moreover, important trends in digital CMOS are analyzed and beyond-CMOS solutions for information processing are highlighted.

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