Title: Compact Modeling of Emerging Ferroelectric devices

Abstract:
Conventional non-volatile memories, such as flash memories, are now reaching their performance and scaling limits. At the same time, the scaling of logic devices conventionally governed by Moore's law is also slowing down due to the inability to remove the generated heat by reducing the power supply voltage. Emerging ferroelectric-based memory and logic devices promise to mitigate these issues and have gained traction in the last decade, primarily due to the discovery of ferroelectricity in CMOS manufacturing process-compatible oxides. There is a growing need for computationally efficient SPICE-compatible compact models for circuit design and co-optimization of these ferroelectric technologies. In this talk, I will discuss the physics and recent compact models developed by our group for ferroelectric random-access memory (FERAM), ferroelectric tunnel junction (FTJ), ferroelectric field-effect transistor (FEFET), and ferroelectric Negative Capacitance FET.