Negative Bias Temperature Instability (NBTI) modeling from devices to circuits

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The PMOS Negative Bias Temperature Instability (NBTI) phenomenon continues to impact the reliability of advanced logic devices and circuits. In this talk, a physical modeling framework (BTI Analysis Tool, or BAT) will be discussed that can explain the NBTI stress and recovery time kinetics under random stress (bias / time) conditions. The framework can also explain different technological aspects such as incorporation of Nitrogen in the gate stack, Germanium in the channel, and changes in mechanical strain in the channel due to changes in device dimensions, in FinFETs and GAA NSFETs. A circuit simulation framework (CARAT, or Circuit Aging Reliability Analysis Tool) will be discussed, that includes the BAT framework, and can model activity-aware circuit aging under different operating workloads. Comparison will be made between activity aware circuit aging and blanket worst-case condition, and the pessimism in standard guardbanding practices will be highlighted.