Electrostatic Discharge (ESD) Issues and Challenges for Ultra-High-Speed Components and Systems

Abstract: ESD has been a pervasive issue for semiconductor IC technologies for the last four decades. However, CMOS technology scaling and demand for ultra-high-speed IOs are placing a severe restriction on achieving adequate reliability from the ESD threat. Adding to this 3D IC integration is increasing the level of attention needed to make them feasible. Aside from the IC components to be protected from ESD during fabrication and assembly, electronic systems with high-speed applications also face higher ESD threat from external events. This webinar will give an overview of these different focus areas for ESD. The talk will first describe the Charged Device Model (CDM) as the main ESD threat and the implications for ultra-high-speed interfaces. It will conclude by addressing the impact on system level ESD design and the simulation methods to optimize system efficient ESD designs.