Graphene on cubic silicon carbide: a platform on silicon for More-Than-Moore integrated technologies

Prof. Francesca Iacopi
School of Data and Electrical Engineering, Faculty of Engineering and IT,
University of Technology Sydney,
Ultimo 2007 New South Wales, Australia
francesca.iacopi@uts.edu.au

The continued progress of semiconductor technologies strongly relies on the continued innovation in electronic (nano)materials and their successful integration into novel and reliable devices on silicon, which can be fabricated consistently at the wafer –scale. Graphene was the first material discovered within the now large 2D family, and holds vast promise for integrated technologies. In particular, graphene possesses a variety of exceptional functionalities ranging from electronics, optics/photonics, electrochemical and biocompatibility properties, which could complement well silicon technologies. However, despite the interest, its introduction in semiconductor technologies is still lagging behind. We will review some of the specific challenges that graphene has encountered in terms of semiconductor applications, with particular focus on the need for direct, consistent and up-scalable synthesis and some of the reliability aspects. We will then share our unique approach to obtain graphene on silicon substrates over large areas and in a site – selective fashion, based on a solid-state source approach using silicon carbide on silicon, combined with a liquid-phase-epitaxy growth of graphene enabled by a catalytic alloy of nickel and copper. This technology has allowed us to reveal for the first time the electronic transport properties of epitaxial graphene on 3C-SiC on silicon over large scales, and to learn that, more so than defects, the control of the graphene interfaces as an area that deserves key focus for a successful integration of graphene. We also show how, depending on the chosen application, well-engineered defects in graphene are key to achieving the wanted performance. We will review our progress and current understanding of this new technology, and illustrate how it could augment current silicon technologies for More than Moore applications from electronics to photonics and energy storage.

Prof.Francesca Iacopi, MSc Physics (Rome, 1996), PhD EE (KULeuven, 2004) has over 20 years' international industrial and academic expertise in the miniaturisation of semiconductor technologies. She has led large R&D projects for IMEC (Belgium) and Globalfoundries Inc (USA) across electronic devices, interconnects, and packaging. She is known for her influential work in porous dielectrics for interconnects, and, more recently, graphene for on-chip applications. Recipient of an MRS Gold Graduate Student Award (2003), an ARC Future Fellowship (2012), and a Global Innovation Award in Washington DC (2014), she was listed among the most innovative engineers by Engineers Australia (2018). Francesca is a Fellow of the Institution of Engineers Australia and serves in several international technical committees for MRS and IEEE, including the Emerging Research Materials Chapter of the International Roadmap for Systems and Devices (irds.ieee.org). She leads the Integrated Nanosystems Lab at the University of Technology Sydney. She is a Core Member of the Centre for Clean Energy Technology at UTS, an Associate Investigator of the ARC Centre of Excellence in Low-Energy Electronics Technologies (FLEET) and a Chief Investigator of the Centre of Excellence in Transformative Meta-Optical Systems (TMOS). She is also founder and inaugural Chair of the IEEE NSW EDS Chapter.