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Table of Contents

Technical Briefs

2023 IEEE International Electron Devices Meeting Highlighted Advances in Critical Semiconductor Technologies with the Theme "Devices for a Smart World Built Upon 60 Years of CMOS"

by Jungwoo Joh, IEDM 2023 Publicity Chair and Kang-ill Seo, IEDM 2023 Publicity Vice Chair

edited by Daniel Tomaszewski, EDS Newsletter Editor-in-Chief

Since it began in 1955, the IEEE International Electron Devices Meeting (IEDM) has been where the world's best and brightest electronics technologists go to learn about the latest breakthroughs in semiconductor and related technologies. That tradition continued last year, when the 69th annual IEEE IEDM conference took place in-person on 9-13 December 2023 at the Hilton San Francisco Union Square hotel, with online access to recorded content available afterward.

The 2023 IEDM technical program, supporting the theme, "*Devices for a Smart World Built Upon 60 Years of CMOS*," consisted of more than 225 presentations plus a full slate of panels, Focus Sessions, Tutorials, Short Courses, a career luncheon, supplier exhibit, and IEEE/EDS award presentations.

(continued on page 3)

Your Comments Solicited

Your comments are most welcome. Please write directly to the Editor-in-Chief of the Newsletter at daniel.tomaszewski@imif.lukasiewicz.gov.pl

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(continued from page 1)

"*The IEDM offers valuable insights into where the industry is headed because the leading-edge work presented at the conference showcases major trends and paradigm shifts in key semiconductor technologies*," said Jungwoo Joh, IEDM 2023 Publicity Chair and Process Development Manager at Texas Instruments. He continued: "*For example, this year many papers discuss ways to stack devices in 3D configurations. This is of course not new, but two things are especially noteworthy about this work. One is that it isn't just happening with conventional logic and memory devices but with sensors, power, neuromorphic, and other devices as well. Also, many papers don't describe futuristic laboratory studies, but rather specific hardware demonstrations that have generated solid results, opening pathways to commercial feasibility*." "*Finding the right materials and device configurations to develop transistors that will perform well with acceptable levels of reliability remains a key challenge*," said Kang-ill Seo, IEDM 2023 Publicity Vice Chair and Vice President, Semiconductor R&D, Samsung Semiconductor. He added: "*This year's program shows that electrothermal considerations remain a key focus, particularly with attempts to add functionality to a chip's interconnect, or wiring, which is fabricated using low-temperature processes*."

Here are details of the 2023 IEEE International Electron Devices Meeting:

Tutorial Sessions

On Saturday, 9 December, six **Tutorial sessions** on emerging technologies were presented by experts in the field to bridge the gap between textbook-level knowledge and leading-edge current research, and to introduce attendees to new fields of interest. The tutorials are listed below together with a brief description of their content:

- *Innovative Technology for Beyond 2 nm*, by Matthew Metz, Intel;
  The tutorial was focused on two topics that are the subject of intense research and development at Intel: Transition Metal Dichalcogenides (TMDs) for continued CMOS scaling and new materials and Magneto-Electric Spin-Orbital (MESO) devices for ultra-low power computation. The use of 2D TMDs leads to the monolayer channel thickness, thus to better gate control, to better mobility than in silicon at scaled channel thickness, thus better performance, and to high effective mass and larger band gap, thus low SD tunneling and lower power consumption. The use of MESO devices enables switching at lower voltage (~0.1V), transfer of lower energy, and a non-volatility of logic, thus drastically decreasing power consumption.
- *CMOS+X: Functional Augmentation of CMOS for Next-Generation Electronics*, by Sayeef Salahuddin, UC-Berkeley;
  The tutorial concerned CMOS+X, i.e. integration of CMOS with different non-silicon material systems and devices operated based on new physical phenomena. CMOS+X devices allow for the development of circuits demonstrating new functionalities. Integration of CMOS with magnetic tunnel junctions (MTJs) has allowed the manufacturing of MRAM and the development of circuits for neuromorphic computing. Integration of CMOS with ferroelectric capacitors demonstrating a negative differential capacitance has led not only to the development of FE-FETs having a smaller subthreshold slope that allows for the design of circuits with lower supply bias than CMOS, thus consuming less power but also to the development of FE-RAM concept. Those and other aspects of CMOS+X were discussed in the tutorial.
- *Reliability Challenges of Emerging FET Devices*, by Jacopo Franco, Imec;
  Fundamentals of charge trapping in gate dielectrics in terms of phenomenology, characterization techniques, and physical models were reviewed in the tutorial. Several MOS systems, e.g.: SiGe channels, III-V, and Ge channels for logic were used as case studies. Challenges posed by the specific gate stacks in Nanosheet and Forksheet device architectures, in stacked Complementary FET (CFET) and 2D-channel transistors were presented. The role of trapping in wide-bandgap semiconductor (GaN, SiC) MOS-based devices as well as in transistors based on oxide semiconductor channels (e.g. IGZO) was highlighted. The interplay between their gate dielectric and channel instabilities was also discussed. It makes the reliability assessment and optimization complex and requires combining electrical and optical characterization techniques.
- *Advanced Packaging and Heterogeneous Integration-Past, Present & Future*, by Madhavan Swaminathan, Penn State;
  The tutorial concerned fundamentals of advanced packaging (AP) covering the past and present state-of-the-art. Chips (ICs) connected on a Multi-Chip Module (MCM) or stacked on top of each other on an interposer (3D) are examples of the AP which is necessary for system scaling at present and is a step towards the heterogenous integration (HI) that will be decisive for scaling in the future. The speaker stated, "Heterogenous integration uses packaging technology to integrate dissimilar chips, photonic devices, or components … with different materials and functions, and from different

design houses, foundries, wafer sizes, feature sizes, and companies into a system or subsystem." Different approaches to the HI were discussed in the tutorial using the metrics: size, performance, and functionality.

- *Synapses, Circuits, and Architectures for Analog In-Memory Computing-Based Deep Neural Network Inference Hardware Acceleration*, by Irem Boybat, IBM;
  The tutorial was focused on the emerging field of analog in-memory computing (AIMC). More specifically, the talk delved into devices, synapses, circuits, and architectures for building energy-efficient yet accurate AIMC-based inference accelerators for deep neural networks (DNNs). It was shown how the AIMC paradigm can overcome the limitations of traditional digital computing approaches and offer better energy efficiency by blurring the distinction between memory and computing. The speaker investigated the impact of device characteristics and their organization into synapses on DNN inference accuracies. Furthermore, he discussed the role of peripheral circuits and accelerator architectures on energy efficiency and performance.
- *Tools for Device Modeling: From SPICE to Scientific Machine Learning*, by Keno Fischer, JuliaHub;
  In the tutorial, a hierarchy of modeling modalities available for semiconductor devices, from compact MOSFET models, through TCAD, down to direct Density Functional Theory calculations was reviewed. The speaker discussed how these models can be leveraged beyond simple simulation for device optimization, characterization, and more. Then, more recent techniques, exploring how Scientific Machine Learning allows the creation of multi-scale surrogate models at tunable fidelity and performance, were explored. Finally, the talk presented the real-world experiences developing CedarEDA, and vision for the future of device modeling, and how we can bring advanced modeling closer to engineering practice to reduce the costly iterations, build better devices, and improve productivity.

Short Courses

On the next day of the IEDM, Sunday, 10 December, two full-day **Short Courses** were held in parallel. In contrast to the Tutorials, they were focused on a single technical topic. They offered the opportunity to learn about important areas and developments, and to network with global experts. The Short Courses and their content are presented below:

- **Transistor, Interconnect, and Chiplets for Next-Generation Low-Power & High-Performance Computing**, organized by Yuri Y. Masuoka, Samsung.
  The next generations of low-power and high-performance computing systems will demand a large progress in the device, SOC, and SOP architectures. Efficiencies of the architectures used at present approach their limits and establish serious challenges for semiconductor and packaging technologies. The Short Course aimed at the presentation of technologies used nowadays, at the identification of their limitations, related challenges, and means to mitigate them, and at possible directions of development of devices, interconnects, and integration techniques.
  The first three talks of the Course were:
  - *Advanced Technology Requirement for Edge Computing*, by Jie Deng, Qualcomm;
  - *Process Technology toward 1nm and Beyond*, by Tomonari Yamamoto, Tokyo Electron;
  - *Empowering Platform Technology with Future Semiconductor Device Innovation*, by Jaehun Jeong, Samsung;

  They concerned technologies that enable the evolution of logic transistors and interconnects towards the 1nm node and beyond. With the FinFET scaling approaching limits, novel device architectures emerge, including Gate-All-Around (GAA)/Multi-Bridge Channel FET (MBCFET™), Forksheet FET, Complementary FET (CFET), 2D-material FET. Scaling of the logic cell area requires decreasing the cell width and height. The gate pitch decrease is crucial for the cell width scaling. This requires scaling of gate length (e.g. by use of the GAA FETs), gate spacer width, and contact feature size. Advancements in layout and transistor structure (e.g. by use of the CFETs), as well as interconnect metal pitch scaling, contribute to the cell height scaling. For the metal pitch scaling, RC reduction techniques have to be implemented for copper interconnect extension. Alternative metals that outperform copper at a CD size of 10nm and below need to be considered, too. To mitigate challenges following the layout and performance advancements, a Backside Power Delivery is attractive. Material advancements are necessary to mitigate parasitic capacitance and resistance increase while securing yield and reliability. To enable progress, continuous process, and tool advancements are necessary for the film, etch, lithography, and wet processing, as well as in wafer bonding and thinning technologies. They have a great, economic impact on the whole semiconductor ecosystem. This aspect of the technology was discussed too.
  The next three talks were:
  - *Future Power Delivery Process Architectures and Their Capability and Impact on Interconnect Scaling*, by Kevin Fischer, Intel;
  - *DTCO/STCO in the Era of Vertical Integration*, by YK Chong, ARM;
  - *Low Power SOC Design Trends/3D Integration/ Packaging for Mobile Applications*, by Milind Shah, Google;

  They concerned different aspects of integration. Coordinated innovations across system, circuit, and

technology abstraction levels are needed to continue the trajectory of power, performance, area, and cost (PPAC) metrics within compressed product development timelines. New architectures for power delivery, e.g. buried power rails, can reduce the impact of scaling interconnect pitches and feeding through pitches, and of adding ever more interconnect layers. One step beyond that is moving power to the backside of the wafer. This eliminates the need to spend interconnect resources on power. Next, the industry perspective on the technological and product development challenges of advanced process nodes was presented. The Design-Technology Co-Optimization (DTCO) and System-Technology Co-Optimization (STCO) strategies explored at ARM, encompassing techniques for logic, SRAM, interconnects, power delivery, system partitioning, and packaging were discussed. Finally, the course made a review of the current industry landscape of 3D packaging integration solutions which enable higher off-chip interconnect density resulting in higher data bandwidth, power efficiency, lower data communication latency, and future trends. A trend of 3D interconnect packaging strategy and optimization was also highlighted.

- **The Future of Memory Technologies for High-Performance Memory and Computing**, organized by Ki Il Moon, SK Hynix.

  The Short Course concerning perspectives of memory technologies consisted of six talks covering the physics of memory operation, memory architectures, integration/packaging of memories, in-memory computing, AI architectures, and challenges of memory technology.

  The first two talks of the Course were:

  - *High-Density and High-Performance Technologies for Future Memory*, by Koji Sakui, Unisantis Electronics Singapore/Tokyo Institute of Technology;
  - *Advanced Packaging Solutions for High-Performance Memory and Compute*, by Jaesik Lee, SK Hynix;

  They introduced memory technology issues. Four technologies: Dynamic Flash Memory (DFM), Key shape Floating Body Memory (KFBM), Surrounding Gate Transistor (SGT), and Bumpless Build Cube (BBCube) 3D, their advantages and fields of application were discussed, e.g. possibility of realizing a high-density DFM using the Si technology, compatibility of the KFBM with CMOS, improved density and reduced power leakage in SGT. The presentation of the heterogeneous integration aspects in BBCube 3D was a link with the next talk on the high bandwidth memory (HBM) stacking innovations and challenges associated with advanced packaging technologies. In that talk, HBM challenges associated with the system-level cooling integration were also presented.

  The next three talks were:

  - *Analog In-Memory Computing for Deep Learning Inference*, by Abu Sebastian, IBM;
  - *The Next Generation of AI Architectures: The Role of Advanced Packaging Technologies in Enabling Heterogeneous Chiplets*, by Raja Swaminathan, AMD;
  - *Key Challenges and Directional Path of Memory Technology for AI and High-Performance Computing*, by Keith Kim, NVIDIA;

  They concerned memory concepts for Deep Learning, Artificial Intelligence, and High-Performance Computing. First, analog in-memory computing (AIMC) based on non-volatile memory technology was introduced. A multi-tile mixed-signal AIMC chip for deep learning inference was presented. The chip fabricated in 14 nm CMOS technology comprises 64 AIMC cores/tiles based on phase-change memory technology and will serve as the basis to delve into the device, circuits, architectural, and algorithmic aspects of AIMC. Next, some possible ways forward to address the challenges of the advanced packaging were discussed, e.g.: How do we bring the Universal Chiplet Interconnect Express (UCIe) standard together with advanced packaging? What standard form factors should we define? What kind of power delivery and thermal controls will we need? New 2.5D fanout and 3D hybrid bonded architectures driving AMD's industry-leading advanced technology roadmap, as well as challenges and solutions for large chiplet modules were shown. Next, a directional path of memory technology requested by AI/HPC applications, and technical challenges for bandwidth, power, density, RAS, and security were discussed. Barriers and potential technology solutions were reviewed.

  The 6th talk of the Course

  - *Charge-Trapping Memories: From the Fundamental Device Physics to 3D Memory Architectures (3D NAND, 3D NOR, 3D DRAM) and Computing in Memory (CIM)*, by Hang-Ting (Oliver) Lue, Macronix;

  reviewed the physics behind bandgap engineered SONOS, encompassing *Ab Initio* modeling of commercially adopted SiON tunnel dielectrics and SiN traps. Next, the discussion was extended to 3D NAND architectures. The potential of 3D NOR structures to offer superior product performances with low latency and byte-addressable 3D memory was explored. Finally, 3D DRAM architectures and the concept of computing in memory utilizing 3D memory technology were presented to address the escalating demands of big-data AI computing.

Welcome and Awards

The main part of the 2023 IEDM started on Monday, 11 December with the **Welcome** by Dina Triyoso, General Chair of the Conference. Afterwards, recipients of the following awards were announced:

- **2023 IEEE Andrew S. Grove Award** was given to Hon-Sum Philip Wong "For contributions to novel and advanced semiconductor device concepts and their implementation";
- **2022 Roger A. Haken Best Student Paper Award** was given to Ruben Asanovski for the paper "New insights on the excess 1/f noise at cryogenic temperatures in 28 nm CMOS and Ge MOSFETs for quantum computing applications";
- **2022 EDS Paul Rappaport Award** was given to Akshay Arabhavi, Filippo Ciabattini, Sara Hamzeloui, Ralf Flückiger, Tamara Saranovac, Daxin Han, Diego Marti, Giorgio Bonomo, Rimjhim Chaudhary, Olivier Ostinelli, and Colombo R. Bolognesi For the paper "InP/GaAsSb Double Heterojunction Bipolar Transistor Emitter-Fin Technology With f_{MAX} = 1.2 THz";
- **2022 EDS George Smith Award** was given to Sourav De, Franz Müller, Nellie Laleni, Maximilian Lederer, Yannick Raffel, Shaown Mojumder, Alptekin Vardar, Sukhrob Abdulazhanov, Tarek Ali, Stefan Dünkel, Sven Beyer, Konrad Seidel, and Thomas Kämpfe for the paper entitled "Demonstration of Multiply-Accumulate Operation With 28 nm FeFET Crossbar Array";
- **2022 EDS Leo Esaki Award** was given to Fei Mo, Jiawen Xiang, Xiaoran Mei, Yoshiki Sawabe, Takuya Saraya, Toshiro Hiramoto, Chun-Jung Su, Vita Pi-Ho Hu, and Masaharu Kobayashi for the paper "Efficient Erase Operation by GIDL Current for 3D Structure FeFETs With Gate Stack Engineering and Compact Long-Term Retention Mode";
- **2023 EDS Distinguished Service Award** was given to Fernando Guarin, Retired, NY, USA "For Outstanding and Dedicated Service for the Benefit and Advancement of the Electron Devices Society";
- **2023 EDS Education Award** was given to Gary S. May, University of California, Davis, CA, USA "For dedicated leadership and mentorship that has diversified academic leaders in education";
- **2023 EDS Lester F. Eastman Award** was given to James C. Hwang, Cornell University, Ithaca, NY, USA "For outstanding achievement in high-performance semiconductor devices";
- **2023 EDS J.J. Ebers Award** was given to Mukta Farooq, IBM, Hopewell Junction, NY, USA "For development of emerging heterogeneous integration architectures for 3D ICs".

Next, the 2023 IEEE/EDS Fellows were announced.

Technical Program

The technical program of 2023 IEDM consisted of 41 technical sessions including one Plenary Session held on Monday immediately after the Welcome and Awards ceremonies and four Focus Sessions.

During the Plenary Session, three **Plenary Presentations** were given:

- *Redefining Innovation: A Journey forward in the New Dimension Era* by Siyoung Choi, President & GM, Samsung Foundry Business, Device Solutions Division;
- *The Next Big Thing: Making Memory Magic and the Economics Beyond Moore's Law* by Thy Tran, Vice President of Global Frontend Procurement, Micron;
- *Semiconductor Challenges in the 5G and 6G Technology Platforms* byBjörn Ekelund, Corporate Research Director, Ericsson.

Below, we briefly report four **Focus Sessions** devoted to key emerging technologies. We describe their leading themes and content.

Neuromorphic Computing for Smart Sensors (Session #7)—Interest is growing in neuromorphic computing, where electronic devices and systems are designed to emulate how the brain works. The hope is that this will make possible new and better solutions to difficult computing challenges. This Focus Session contained invited papers describing recent advances in neuromorphic computing and smart sensors:

- *The Case for Hybrid Analog Neuromorphic Chips Based on Silicon and 2D Materials*, G. Iannaccone, et al, Università di Pisa/Quantavis s.r.l.;
- *Case Study of Tactile Sensors: System-Level Approach to Analog In-Sensor Computing*, M-Y Mun, et al, Samsung Advanced Institute of Technology;
- *Intelligent Vision Sensor and Edge Computing Envisage the Future*, R. Eki, et al, Sony Semiconductor Solutions Corporation;
- *Live-Cell Imaging with Integrated Capacitive Sensor Arrays*, J. Rosenstein, et al, Brown Univ./Northeastern Univ./Raytheon/Boston Univ.;
- *Towards CMOS Capacitance Sensors for DNA Origami Characterization*, M. Dandin, et al, Carnegie Mellon Univ.;
- *Scalable Biosensors Using Standard CMOS Process*, U. Noyan, et al, Univ. of Maryland/Arizona State Univ.

Logic, Memory, Package and System Technologies for Future Generative AI (Session #15)—Generative artificial intelligence (AI) has been all the buzz lately, with its potential to increase productivity and efficiency in many spheres of human endeavor. However, creating the logic, memory and other devices needed for future generative AI systems is a formidable technical challenge. This Focus Session covered system requirements, technical barriers, and solutions for AI computing and included the papers:

- *Generative AI on a Budget: Processing Transformer-based Neural Networks at the Edge*, Y. Tanurhan, et al, Synopsys Inc.;
- *Design of Analog-AI Hardware Accelerators for Transformer-based Language Models*, G. Burr, et al, IBM;

- *The Era of Generative Artificial Intelligence: In-Memory Computing Perspective*, K. Sohn, et al, Samsung Electronics;
- *Innovations For Energy-Efficient Generative AI*, S. Naffziger, AMD;
- *Beyond Exascale: A Paradigm Shift for AI and HPC*, W. Gomes, Intel;
- *Advanced Packaging Technologies in Memory Applications for the Future Generative AI Era*, K-I. Moon, et al, SK Hynix Inc.;
- *NVDRAM: A 32Gb Dual-Layer 3D Stacked Non-Volatile Ferroelectric Memory with Near-DRAM Performance for Demanding AI Workloads*, N. Ramaswamy, et al, Micron Technology Inc; this paper is briefly summarized in the "Memories" section below.

3D Stacking for Next-Generation Logic & Memory by Wafer Bonding and Related Technologies (Session #19)—As the feature sizes in leading-edge CMOS devices approach atomic dimensions, traditional scaling has become much more difficult and expensive. One way to meet the demands of ever-growing computing and AI workloads, while still achieving the traditional PPAC benefits of scaling (performance, power, area, and cost), is to stack integrated circuits vertically, in 3D configurations. The following works were presented during this Focus Session:

- *Process Innovations for Future Technology Nodes with Backside Power Delivery and 3D Device Stacking*, M. Kobrinsky, et al, Intel;
- *Backside Power Delivery: Game Changer and Key Enabler of Advanced Logic Scaling and New STCO Opportunities*, A. Veloso, et al, Imec;
- *Thermal Dissipation in Stacked Devices*, W-Y. Woon, et al, TSMC/Stanford Univ.;
- *Ultimate Layer Stacking Technology for High-Density Sequential 3D Integration*, I. Radu, et al, Soitec/CEA Leti/Imec;
- *CMOS Directly Bonded to Array (CBA) Technology for Future 3D Flash Memory*, M. Tagami, Kioxia;
- *Wafer Bonding as Next-Generation Scaling Booster*, T. Wernicke, P. Lindner, et al, EV Group E. Thallner GmbH.

Sustainability in Semiconductor Device Technology and Manufacturing (Session #28)—This Focus Session was about sustainability in device technology and manufacturing because it has never been more important to use Earth's finite resources more efficiently and to reduce associated environmental impacts. Six papers were presented at this Focus Session:

- *Cradle-to-Gate Life Cycle Assessment of CMOS Logic Technologies*, L. Boakes, Imec;
- *Sustainability-Aware Technology Development at Applied Materials*, B. J. Gross, et al, Applied Materials;
- *EUV Energy Efficiency*, T. Thijssen, et al, ASML;
- *Sustainable Environmental Technologies for Advanced Semiconductor Manufacturing Intelligent FAB,* H-C. Lee, et al, Samsung/Seoul National Univ.;
- *Modeling 300 mm Wafer Fab Carbon Emissions*, S. W. Jones, TechInsights;
- *Developing Sustainable Technologies for a More Sustainable Future*, S. Nicoleau, et al, STMicroelectronics.

The following sections present summaries of the most noteworthy, in our opinion, papers presented during the technical sessions of the 2023 IEDM. Several papers can be assigned to common thematic groups. We present these groups first. Then, we present other noteworthy papers on diverse topics.

CMOS Scaling: CFETs and 2D Channel FETs

Nanosheet-based transistors, and 3D complementary FETs (CFETs) built from nanosheets, are key to continuing Moore's Law scaling. Nanosheets are gate-all-around (GAA) transistor architectures where stacks of silicon channels are completely surrounded by the gate. They offer better electrostatic control than FinFETs, relatively high drive currents, and variable widths. CFET architectures are highly integrated 3D designs where n-FET and p-FET nanosheets are stacked on top of one other. These stacked devices may be built monolithically (on one wafer), or sequentially (built on separate wafers and then transferred and integrated). At the IEDM, a number of papers advanced the state-of-the-art in these areas. Among them, there were papers from TSMC and Intel that discussed ways to scale silicon (Si) CMOS technology in the nearer term.

A Practical, Monolithic CFET Architecture: In the late-news **paper #29.6**, ***"Complementary Field-Effect Transistor (CFET) Demonstration at 48nm Gate Pitch for Future Logic Technology Scaling"***, TSMC researchers unveiled what they call *a practical, monolithic CFET architectural approach* for logic technology scaling. It features 48nm-gate-pitch stacked n-FET-on-p-FET silicon nanosheet transistors (Fig.1). These demonstrated high on-state current/low subthreshold leakage, leading to an impressive on/off current ratio (six orders of magnitude). They also exhibited a relatively high yield, with a FET survival rate of >90%. Although previous work has shown that functional CFET devices can be built on 300mm wafers, the gate pitches of those devices have been too large for future scaling. In this work, a more relevant 48nm gate pitch was achieved with a vertically stacked n/p source-drain (SD) epitaxy, comprising middle dielectric isolation, an inner spacer, and n/p SD isolation. While other essential features still must be integrated to unleash CFET technology's potential, this work paves the way for that to happen.

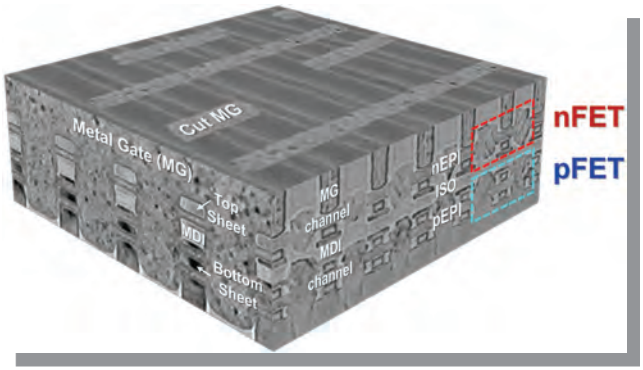

Figure 1. Inline cross-section TEM demonstration of a monolithic CFET with a gate pitch of 48nm and with nFETs placed above pFETs, and both types of transistors surrounded by a single metal Gate (Paper #29.6, "Complementary Field-Effect Transistor (CFET) Demonstration at 48nm Gate Pitch for Future Logic Technology Scaling," *S. Liao, et al, TSMC).*

A CFET-Based CMOS Inverter: Intel researchers presented in the paper #29.2, "***Demonstration of a Stacked CMOS Inverter at 60nm Gate Pitch with Power Via and Direct Backside Device Contacts***," a 3D monolithic CFET device they built, consisting of 3 n-FET nanoribbons on top of 3 p-FET nanoribbons, with 30 nm of vertical separation between them (Fig. 2). In an industry first, they used this device to build fully functional inverters (test circuits) at a 60nm gate pitch. The devices also featured vertically stacked dual-S/D epitaxy; dual metal work function gate stacks connecting the n- and p- transistors; and integration with backside power delivery and direct backside device contacts. The researchers also described a nanoribbon "depopulation" process, for which unequal numbers of n-MOS/p-MOS devices are needed. The work helps to increase understanding of the potential to scale CFETs for logic and SRAM applications and to understand key process enablers.

Record Results from Stacked NMOS Nanosheets with TMD Channels: Research on scaling of devices in the beyond-CMOS domain was presented in **paper #2.1** ***"Monolayer-MoS_2 Stacked Nanosheet Channel with C-type Metal Contact".*** Currently, nanosheet scaling is accomplished by thinning the Si channels, but work is ongoing to find practical ways to use ultra-thin transition metal dichalcogenides (TMDs) as the channel material instead. TMDs such as MoS_2 are called monolayer/2D materials because they're just an atomic layer thick. A TSMC-led team discussed the unprecedented performance of two stacked NMOS nanosheets with MoS_2 channels (Fig.3). The 40nm gate-length NMOS devices exhibited positive threshold voltage (V_{TH} ~1.0 V); high on-current (I_{ON} ~370 μA/μm at V_{DS} = 1 V); a large on/off ratio (10^8); and low contact resistance (R_C ~0.37-0.58 kΩ-μm). Key to these results was a novel C-shaped wrap-around contact offering greater contact area and gate stack optimization. The devices exhibited acceptable mechanical stability but the researchers said more research is needed to mitigate defect creation in the MoS_2 channels.

First True 2D CMOS Demonstration: Another interesting work on scaling of beyond-CMOS devices was presented in **paper #10.1** ***"Status and Performance of Integration Modules Toward Scaled CMOS with Transition Metal Dichalcogenide Channel."*** FET devices of each polarity (n-FETs and p-FETs) must offer matched performance for proper operation for CMOS logic. But while MoS_2 is a suitable TMD material for n-type devices, it doesn't work well for p-type devices, where the TMD material WSe_2 is better suited. Also, both extremely thin materials must be robust enough to withstand typical fabrication processes. In the industry first, a TSMC-led team described the well-matched n- and p-MOS transistors made using

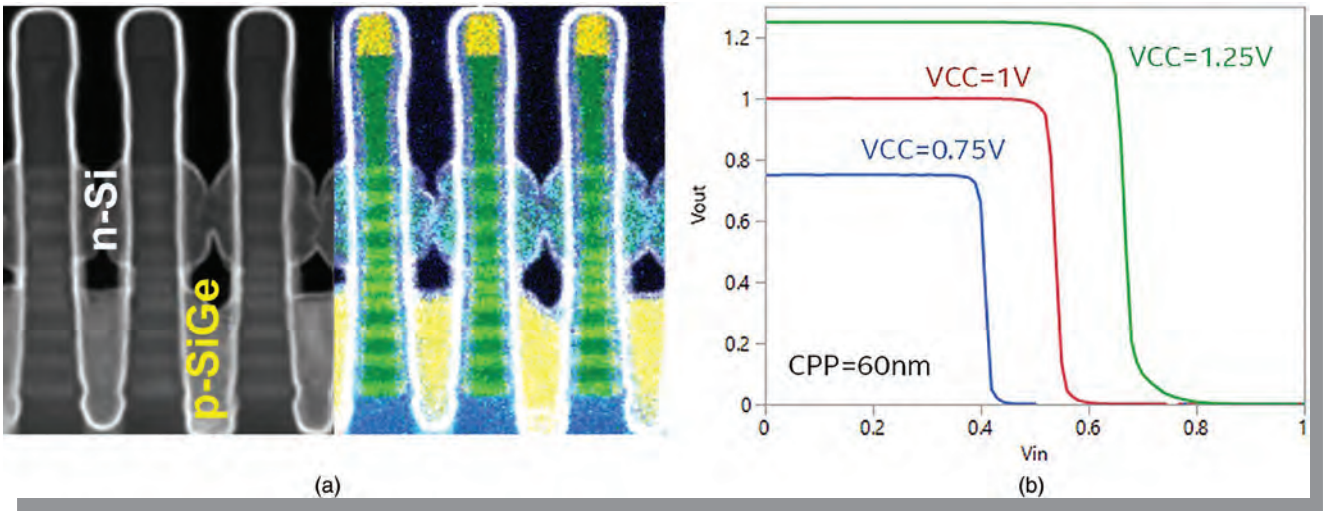

Figure 2. a) TEM micrograph of the CFET device following vertically stacked dual source-drain (SD) epitaxy at contacted poly pitch (CPP) = 60 nm, b) the inverter voltage transfer curve, which verifies that all components make a well-balanced inverter (Paper #29.2, "Demonstration of a Stacked CMOS Inverter at 60nm Gate Pitch with Power Via and Direct Backside Device Contacts," *M. Radosavljević, et al, Intel).*

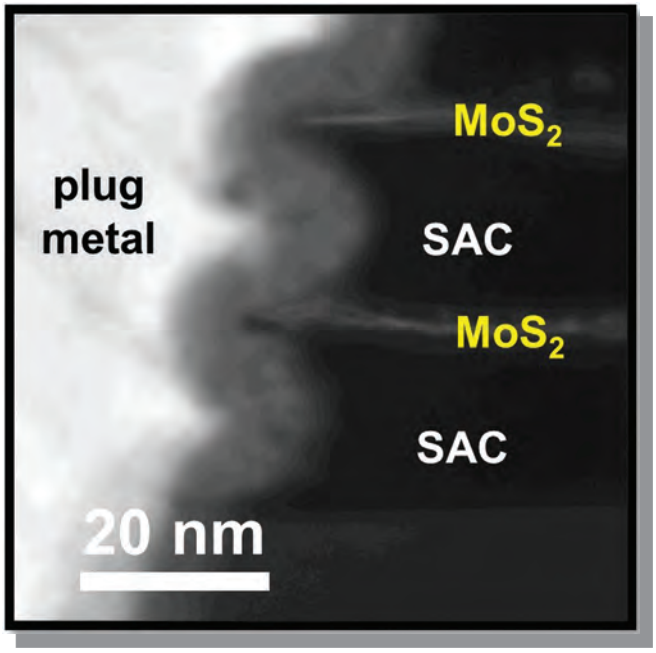

*Figure 3. Dark-field TEM image of the stacked 1L-MoS_2 channel structure with a C-type metal contact (Paper #2.1, "*Monolayer-MoS_2 Stacked Nanosheet Channel with C-type Metal Contact,*" Y-Y Chung, et al, TSMC/Nat'l Yang Ming Chiao Tung Univ./National Applied Research Laboratories).*

these two TMD channel materials, respectively (Fig.4). The robustness of these highly scaled (~50nm channel lengths) and high current-density materials was demonstrated by growing them separately on sapphire and then transferring them die-by-die to a 300 mm silicon wafer to integrate them. The devices showed nearly unaltered performance after this transfer process, with a high output current (~410 μA/μm) at the same gate overdrive for both n- and p-FETs (V_{DS} = 1 V). In addition, p-FET mobility reached a record high level (~30 cm^2 /V·s).

Memories

Dense, Fast, Low-Voltage, High-Endurance STT-MRAM: Non-volatile memories retain data when power is shut off, making them useful in embedded applications such as automotive. Flash memory has been the go-to choice for embedded, but is falling short at advanced nodes. Non-volatile magnetic memory (Magnetoresistive RAM, or MRAM) stores data as a magnetic state, not as an electrical charge, and has made inroads into embedded applications. A type called Spin-Transfer Torque MRAM (STT-MRAM) offers fast write speeds, the potential for very high density, low-power operation, and long endurance. In **paper #21.5**, "***Low Voltage (<1.8V) and High Endurance (>1 M) 1-Selector/1-STT-MRAM with Ultra-Low (1 ppb) Read Disturb for High Density Embedded Memory Arrays***", a TSMC-led team described the STT-MRAM with a 1S1R (1 selector/1 resistor) crosspoint array architecture, having more than twice the density (>2.2x) of conventional 1T1R (1 transistor/1 resistor) designs at a 16 nm technology node (Fig. 5). What makes this possible is the use of a specially engineered selector material, SiNGeCTe. The STT-MRAM demonstrated low-voltage operation (<1.8 V); high-speed switching (off-on/on-off transitions of 2.5 ns/3 ns, respectively); and outstanding read/write endurance (>1e9/>1e6 cycles, respectively). The architecture is said to be suitable for stackable 3D memory arrays.

A New Way to Scale DRAMs: DRAM is the workhorse memory of electronic systems, but scaling it to 10 nm and below brings difficult challenges. At advanced nodes, patterning the extremely small features of conventional 6F^2 buried cell array transistors is extremely difficult, as is suppressing "row hammer" electrical interference from nearby cells. However, Samsung researchers saw an opportunity to scale DRAM further with vertical-channel transistors (VCTs) using IGZO (indium gallium zinc oxide) as the channel material. IGZO offers high electron mobility, low leakage, and a high on/off ratio that leads to low power consumption and is suitable for low-temperature processing. In **paper #6.3**, "***Highly Manufacturable, Cost-Effective, and Monolithically Stackable 4F²***

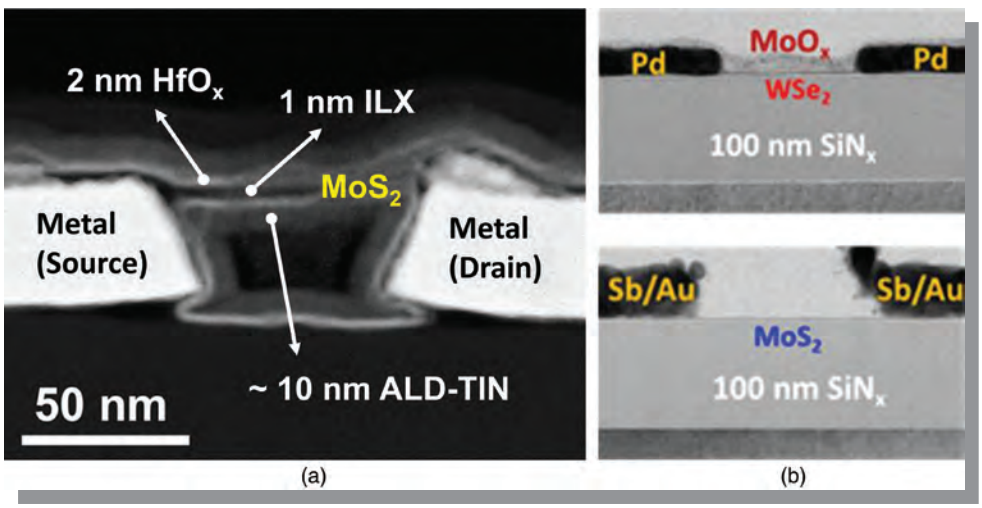

*Figure 4. A cross-sectional TEM of the suspended MoS_2 nanosheet structure with conformal gate stack comprising 10nm TiN, 2nm HfO_x, and 1 nm ILX (interfacial dielectric); b) cross-sectional TEM images of integrated n/p FETs (Paper #10.1, "*Status and Performance of Integration Modules Toward Scaled CMOS with Transition Metal Dichalcogenide Channel,*" A-S Chou, et al, TSMC/Nat'l Taiwan Univ/Nat'l Yang Ming Chiao Tung Univ.)*

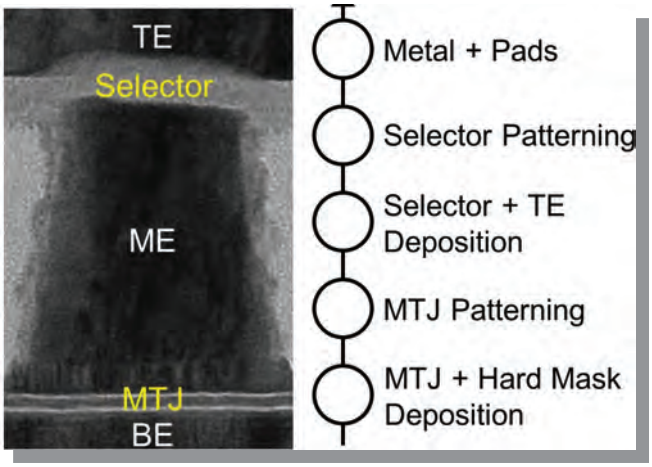

*Figure 5. A TEM image of the integrated 1S1R STT-MRAM memory (Paper #21.5, "*Low Voltage (<1.8 V) and High Endurance (>1 M) 1-Selector/1-STT-MRAM with Ultra-Low (1 ppb) Read Disturb for High Density Embedded Memory Arrays*," E. Ambrosi, et al, TSMC/Taiwan Semiconductor Research Institute).*

Single-Gated IGZO Vertical Channel Transistor (VCT) for sub-10 nm DRAM," they detailed the first successful integration of a $4F^2$ single-gated IGZO-VCT, monolithically stacked on top of core/peripheral transistors with no need for wafer bonding (Fig. 6). They said the devices are suitable for sub-10 nm DRAMs. They demonstrate low leakage current (I_{OFF} <1 fA/cell); subthreshold swing (SS) of 164 mV/dec, and adequate threshold voltage (V_T = -1.73 V at 85 ˚C). The vertical architecture also can fully suppress "row hammer" interference, because the active region isn't shared with adjacent cells.

Non-Volatile Ferroelectric w/DRAM-Like Performance, for AI & Machine Learning: Rapid growth in the size of the data models used in artificial intelligence (AI) and machine-learning (ML) applications is creating an urgent need for higher-bandwidth memory solutions. While new compute paradigms like near-memory-compute and processing-in-memory are being investigated, the best near-term opportunity is to outfit existing, traditional computing architectures with more efficient memory for faster data movement and to accommodate larger models. In **paper #15.7**, ***"NVDRAM: A 32Gb Dual Layer 3D Stacked Non-Volatile Ferroelectric Memory with Near-DRAM Performance for Demanding AI Workloads,"*** presented during the **Focus Session "Logic, Memory, Package and System Technologies for Future Generative AI"** (see above), Micron researchers unveiled a memory technology for these uses which they call NVDRAM (Fig. 7). It is the world's first dual-layer, high-performance, high-density (32Gb), stackable and nonvolatile ferroelectric memory technology. It combines the non-volatile, high-endurance nature of ferroelectric memory cells with DRAM-like read/write speeds and endurance, and also surpasses the retention performance of NAND memory. NVDRAM uses an ultra-scaled (5.7 nm) ferroelectric capacitor as the memory cell, and a dual-gated, stackable, polycrystalline silicon transistor as the access device. To achieve high memory density, two memory layers are fabricated above CMOS circuitry in a 48 nm pitch, $4F^2$ architecture. Full package yield is demonstrated from –40 °C to 95 °C, along with reliability of 10 years (for both endurance and retention).

A Larger Memory Window for 3D NAND: Non-volatile 3D NAND flash memory is widely used for data storage in enterprise, mobile, and edge computing applications, as well as emerging AI use cases. 3D NAND typically uses a gate stack with a charge-trap nitride (CTN) layer. Aggressive vertical scaling of these devices has led to a massive increase in the bit-cell density, but at the expense of higher write voltage because a gate control becomes more difficult. This leads to reduced speed, increased cell size, and higher power consumption at the system level. A larger memory window (the voltage difference between the device's "on" and "off" states) is needed to increase the gate control. Ferroelectric (FE) gate stacks have gained attention as a possible replacement for the CTN layer in order to implement a larger memory window, but much work needs to be done to make the technology viable. In the **paper #24.1**, ***"Experimental Demonstration and Modeling of a Ferroelectric Gate Stack with a Tunnel Dielectric Insert for NAND Applications,"***

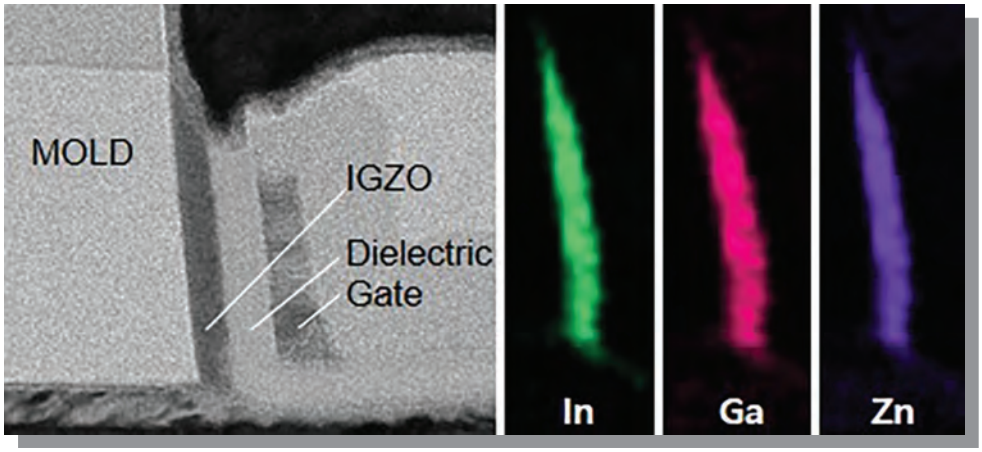

*Figure 6. X-TEM image (left) and EDS analyses (right) of the single-gated IGZO vertical channel transistor after gate stack formation.(Paper #6.3, "*Highly Manufacturable, Cost-Effective, and Monolithically Stackable 4F2 Single-Gated IGZO Vertical Channel Transistor (VCT) for sub-10nm DRAM*," D. Ha, et al, Samsung).*

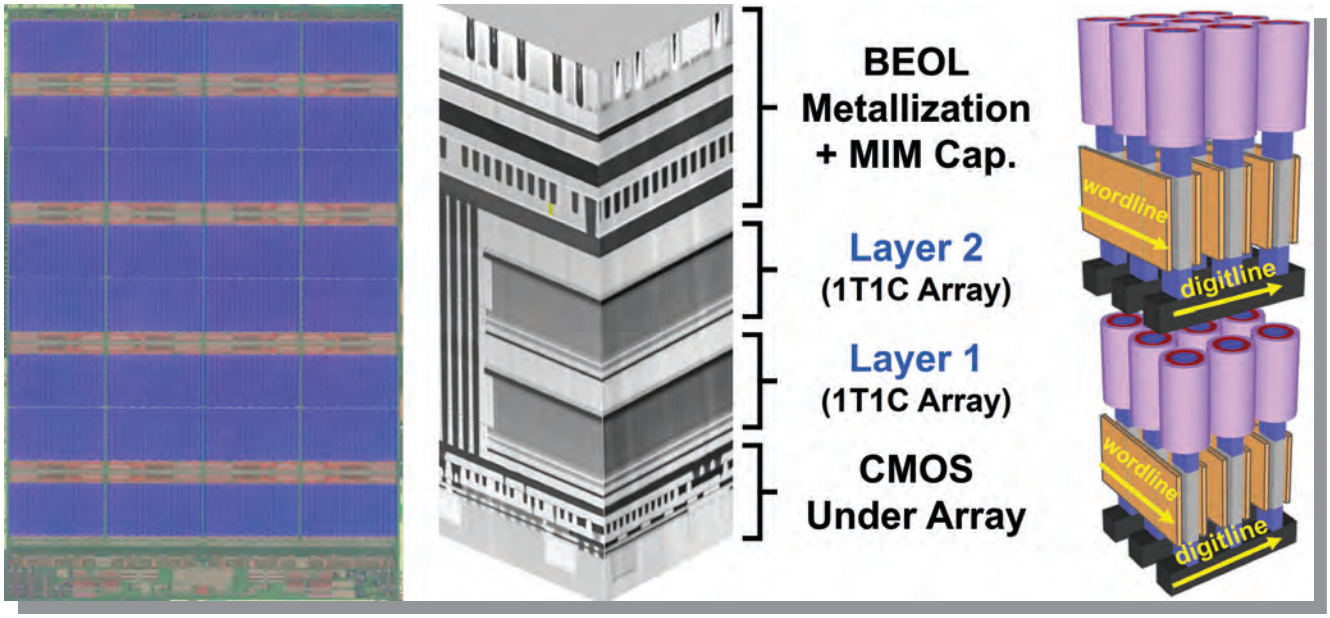

*Figure 7. Final die layout (left) and SEM cross-section (center) of a 32Gb NVDRAM with 1T1C memory layers, fabricated on a CMOS array; a schematic diagram of NVDRAM memory arrays (right) shows polysilicon access device with orthogonal word line (WL) and digit line (DL), and ferroelectric memory cells (Paper #15.7, "*NVDRAM: A 32Gb Dual Layer 3D Stacked Non-Volatile Ferroelectric Memory with Near-DRAM Performance for Demanding AI Workloads*," N. Ramaswamy, et al, Micron Technology).*

a Georgia Tech-led team presented modeling and experimentally demonstrated for the first time an Al_2O_3 layer in the middle of a FE HZO stack (Fig. 8). It significantly enhanced the device's memory window, from 3 V in a reference HZO gate stack without the Al_2O_3 insert, to as high as 7.3 V. The researchers said that further modeling suggested a pathway to achieving a 12 V memory window for the vertical NAND flash technology.

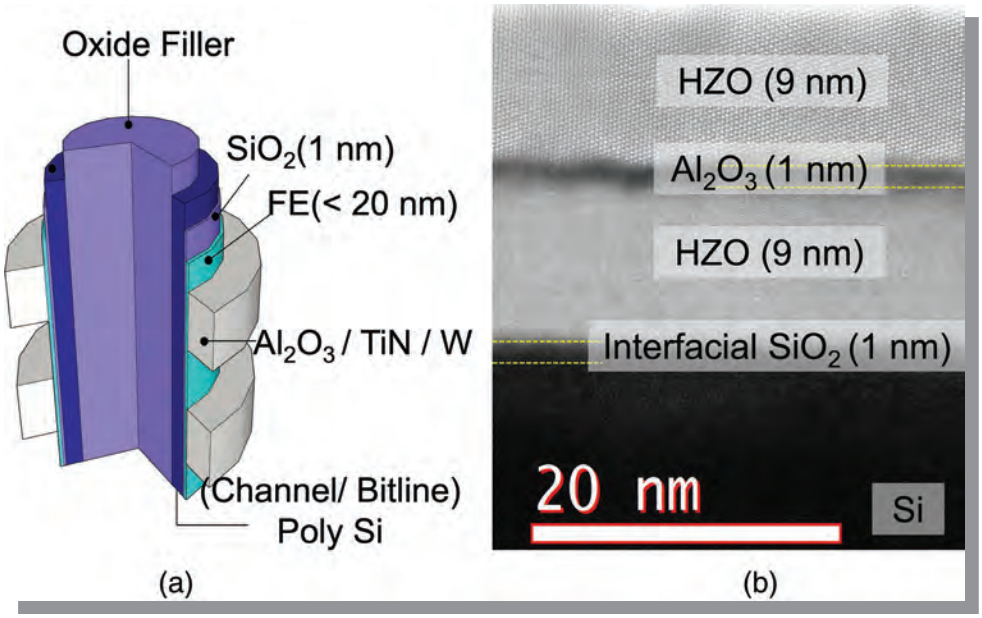

*Figure 8. a) An overview of the FE vertical NAND structure. b) A TEM image of the gate stack. A homogeneous 1nm Al_2O_3 interlayer is clearly visible, suggesting that the formation of the Al_2O_3 interlayer with uniform thickness and full coverage was achieved (Paper #24.1, "*Experimental Demonstration and Modeling of a Ferroelectric Gate Stack with a Tunnel Dielectric Insert for NAND Applications*," D. Das, et al, Georgia Tech/Samsung).*

Devices for Neuromorphic Computing

This year for the first time, the IEDM conference has established an entire technical subcommittee devoted to neuromorphic computing, given the strongly growing interest in the field.

GPU-Like Accuracy But With Far Less Energy Use & Inference Time: Large-scale AI models impose ever-increasing demands for computing power and speed in hardware. However, typical 2D compute-in-memory (CIM) architectures suffer from data transfer bottlenecks across the different CIM arrays layers used as processing elements. That's because each layer's computation results must use a limited-bandwidth on-chip bus to move between the CIM array and buffers, significantly increasing overall computing time for deep neural networks. In the **paper #23.2, "*3D Stackable***

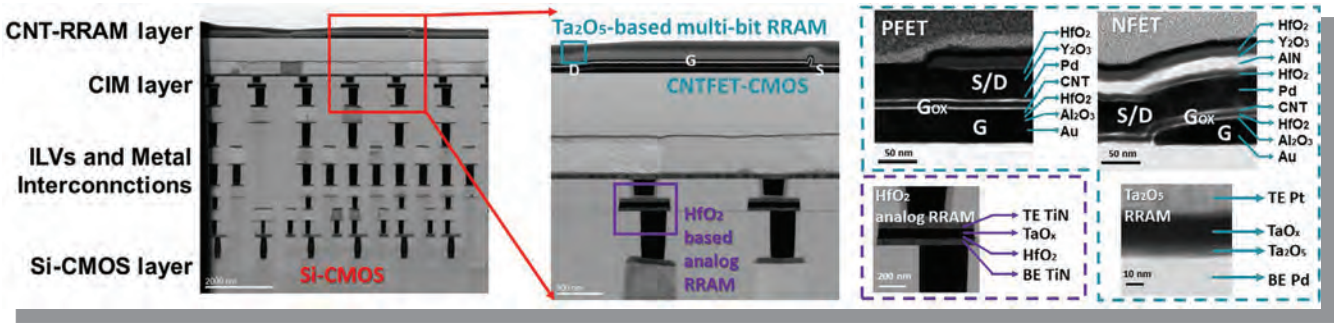

*Figure 9. Cross-sectional TEM images of the device (Paper #23.2, "*3D Stackable CNTFET/RRAM 1T1R Array with CNT CMOS Peripheral Circuits as BEOL Buffer Macro for Monolithic 3D Integration with Analog RRAM-based Computing-In-Memory*," Y. Zhang, et al, Tsinghua Univ./Peking Univ.)*

CNTFET/RRAM 1T1R Array with CNT CMOS Peripheral Circuits as BEOL Buffer Macro for Monolithic 3D Integration with Analog RRAM-based Computing-In-Memory," a Tsinghua University-led team described a monolithic 3D device architecture which integrated buffer arrays right on top of CIM arrays, and dense, fine-grain inter-layer vias (Fig. 9). The 1kb array consists of three functional layers: a 128kb HfO_2-based analog RRAM array for the CIM layer; a stackable carbon-nanotube CNT-FET/Ta_2O_5-based RRAM 1T1R buffer macro layer for data cache; and a Si CMOS logic layer. All devices and circuits were characterized to confirm that each layer worked as designed, and image classification on MLP and ResNET32 networks showed GPU-equivalent accuracy of ~96.5%, with 39x lower energy consumption and 49.6x less inference time.

Hardware Demonstration of Probabilistic Inference: A feed forward neural network is one where information only moves forward from one layer to the next and does not loop around, with the goal of having an input produce an output that contributes to some sort of prediction. Feed forward neural networks are the backbone of deep learning inference systems, but they impose heavy computational burdens on traditional computing hardware. In the **paper #12.1**, ***"Hardware Demonstration of Feedforward Stochastic Neural Networks with Fast MTJ-based p-bits,"*** a UC-Santa Barbara-led team discussed an inference system

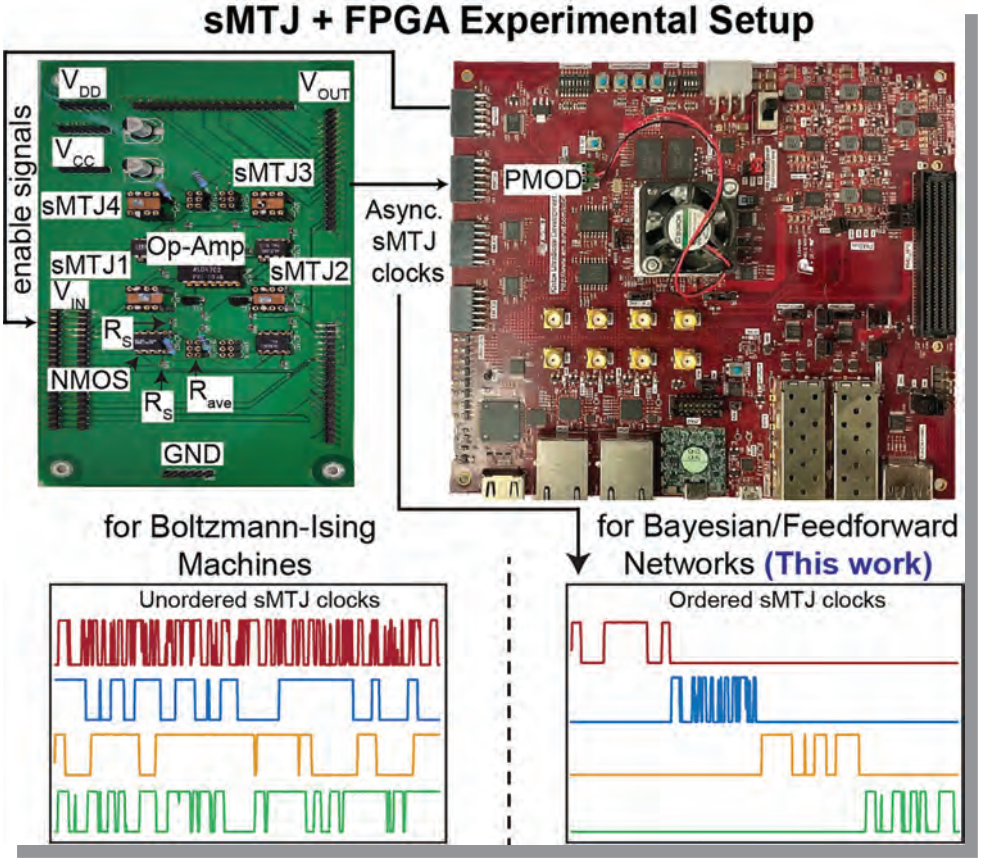

Figure 10. The experimental setup of a printed circuit board (PCB) with 4 sMTJ circuits along with an FPGA. The FPGA sends "enable" signals to the sMTJ circuit inputs (VIN), and asynchronous sMTJ circuit outputs from the PCB are then used to clock pseudo-random number generators (PRNGs). The bottom left of the image shows unordered sMTJ clocks that would be used in traditional Boltzmann machines which are update-order agnostic. The bottom right of the image shows the ordered sMTJ circuit clocks enforced by the enable signals sent from the FPGA. This ordering ensures the ancestral update order for convergence of feed forward networks to the distribution dictated by the Bayes Theorem. (Paper #12.1, "Hardware Demonstration of Feedforward Stochastic Neural Networks with Fast MTJ-based p-bits," *N. Sanjay Singh, et al, UC Santa Barbara/Tohoku Univ.)*

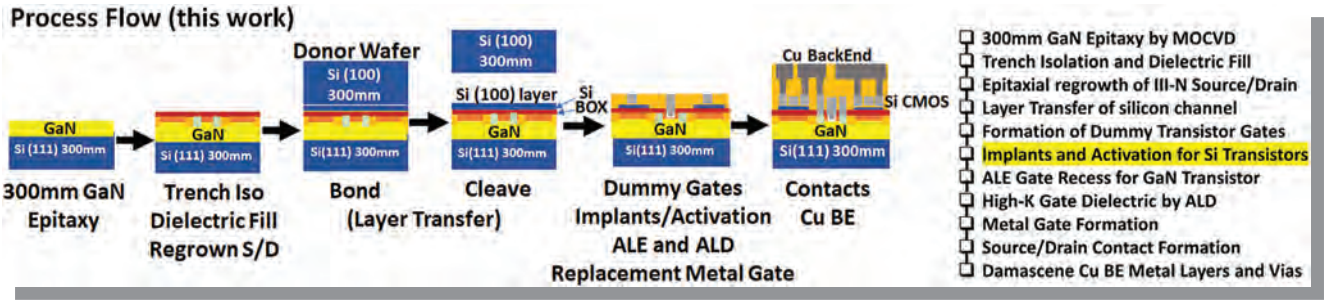

Figure 11. The new process flow for the 3D monolithic integration of GaN and Si CMOS by layer transfer, where the high-temperature activation steps for the Si CMOS transistors are completed before the gate dielectric of the GaN transistors is deposited. (Paper #9.7, "DrGaN: an Integrated CMOS Driver-GaN Power Switch Technology on 300mm GaN-on-Si with E-mode GaN MOSHEMT and 3D Monolithic Si PMOS," *H.W. Then, et al, Intel).*

for deep feed forward stochastic networks, which led to the fastest probabilistic bits (p-bits) demonstrated to date (three orders of magnitude faster than previous demonstrations). In their system, low-barrier stochastic magnetic tunnel junctions (sMTJ) are used to create probabilistic p-bits, which are then routed to a field programmable gate array (FPGA) circuit to build a hybrid CMOS+sMTJ computer (Fig. 10). The researchers say that scaled versions of the prototype circuit can be used to accelerate a broad range of applications, from deep learning to combinatorial optimization.

Power Devices

Power Device with CMOS and GaN Channels: Gallium nitride (GaN) devices are attracting great interest for their potential to address the power density/efficiency requirements of data centers and networking platforms. Intel researchers, building on their earlier work to integrate GaN technology with traditional Si CMOS technology, described in the **paper #9.7**, "***DrGaN: an Integrated CMOS Driver-GaN Power Switch Technology on 300 mm GaN-on-Si with E-mode GaN MOSHEMT and 3D Monolithic Si PMOS***," the first integrated CMOS Driver-GaN, or "DrGaN", power switch, in 300 mm GaN-on-Si technology (Fig. 11). It incorporates an e-mode HEMT and integrated 3D monolithic Si PMOS and potentially enables power delivery solutions to keep pace with the power density/efficiency demands of future CPUs and GPUs. The 180nm DrGaN devices exhibited excellent RDS_{ON} (0.8 mΩ-mm^2) and leakage (well below 0.1 mA). The researchers will detail a new gate-last process flow for the 3D monolithic integration of GaN and Si CMOS by layer transfer, where high-temperature activation steps for the Si CMOS transistors are completed before the gate dielectric of the GaN MOSHEMT is deposited. This resolves a major hurdle in the 3D monolithic integration of GaN and Si CMOS transistors. This flow also enables the GaN and Si CMOS transistors to share the same backend interconnect stack, eliminating intra-connect resistance and reducing the number of masks. The devices achieved a FOM = $1/(R_{ON}Q_{GG})$ of 0.59 (mΩ-nC)$^{-1}$ for a 30 nm gate-length GaN MOSHEMT, demonstrating the potential for future scaling of this architecture.

High-Speed Devices

World Record RF Performance & Cryogenic Possibilities: High-speed, power-efficient devices are needed for future terahertz (THz) applications, and for use in cryogenic environments such as quantum computing systems and outer space. But the faster they operate, the harder it is to measure and characterize their performance. At IEDM in 2021, ETH Zurich unveiled an InP/GaAsSb double heterojunction bipolar transistor (DHBT) with a novel emitter fin architecture, which showed record high-frequency performance. At IEDM in 2023, in the **paper #34.6**, ***"THz InP/GaAsSb DHBTs with Record f_{AVG} = 800 GHz: Characterization to 330 GHz,"*** they described significant advancements in THz transistor

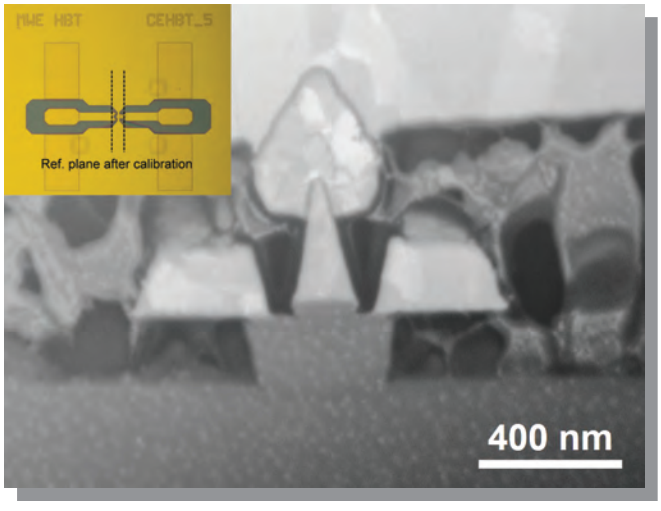

Figure 12. A cross-sectional SEM image of a 175 nm-wide emitter-fin DHBT featuring a 40 nm base access distance. The inset: a top-down microscopic image of a fabricated emitter-fin DHBT with the new shielded co-planar waveguide probe pads for high-frequency measurements. The dashed lines indicate the position of reference planes (Paper #34.6, "THz InP/GaAsSb DHBTs with Record f_{AVG}=800 GHz: Characterization to 330 GHz," *A.M. Arabhavi, et al, ETH-Zurich/Univ. of Bordeaux).*

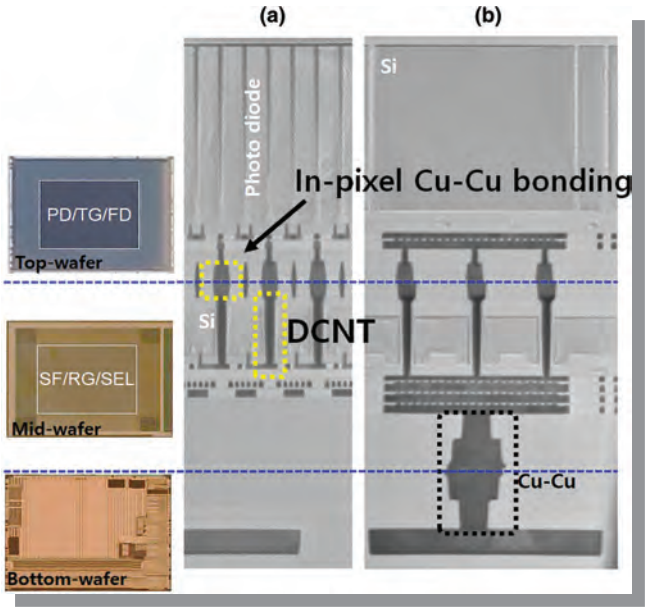

Figure 13. SEM images of the 3-stack structure (longitudinal view): a) the pixel array and (b) the peripheral region (Paper #40.1, "A 0.5 µm Pixel 3-layer Stacked CMOS Image Sensor with Deep Contact and In-Pixel Cu-Cu Bonding Technology," *G-D Ryan Lee, et al, Samsung).*

characterization and metrology methods up to 330 GHz, which enabled them to determine that their DHBT had an 800 GHz average frequency, a world record for DHBT devices (Fig. 12). They also presented the first cryogenic data for a THz transistor, showing f_T/f_{MAX} of 0.57/1.46 THz at 50 K, a world record for any HBT device, opening up new THz applications.

Advances in Imaging

Smallest Pixel Ever for CMOS Imagers: A conventional way to get higher resolution from CMOS image sensors (CIS) is to decrease the size of the individual pixels. But smaller pixels are more easily affected by electrical noise, in particular an effect known as random telegraph signals (RTS), and also by parasitic capacitance, which reduces their efficiency in converting light to electrical signals. In the **paper #40.1**, ***"A 0.5 µm Pixel 3-layer Stacked CMOS Image Sensor with Deep Contact and In-Pixel Cu-Cu Bonding Technology,"*** Samsung researchers described a stacked three-layer 64-megapixel CIS architecture with 0.5µm pixels, the smallest ever reported (Fig. 13). A key feature of the device is that it uses copper-to-copper bonding to interconnect pixels from layer-to-layer, which aligns them precisely and thereby reduces the size of the CIS, and also reduces parasitic capacitance. The pixels demonstrated an 85% reduction in RTS noise and a 67% higher gain in light conversion efficiency versus earlier work.

A New Way to Render Colors at Submicron Pixel Sizes: Next-generation CMOS imagers require smaller pixels with higher resolutions. However, smaller pixels capture less light, so increasing their resolution is difficult. A way to capture more light is to split incident light into different wavelengths corresponding to different colors, and

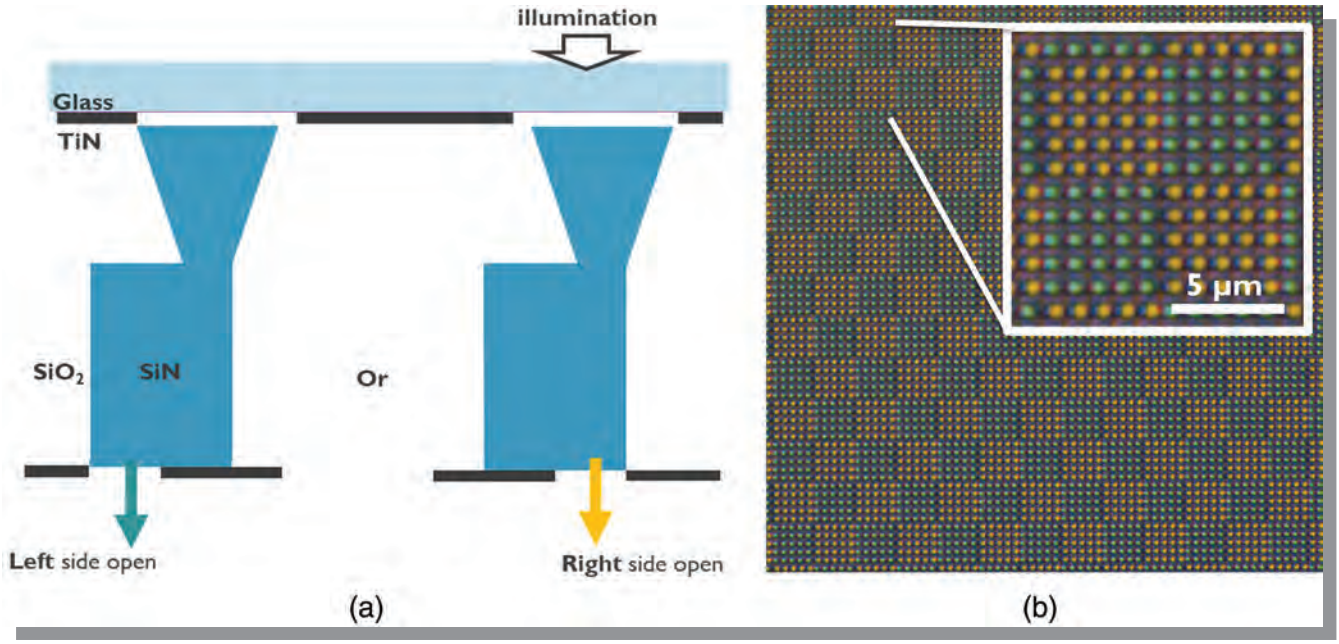

Figure 14. The wafer illuminated with a plane wave of white light; a) visualization of measurement, yellow light exits at the right part of the waveguide, blue light exits on the left; b) RGB camera measurement (100×magn.) of a structure with 620 nm × 250 nm waveguides (pitch = 1 µm) with alternating 5 left-side-open-aperture and 5 right-side-open-aperture waveguides (Paper #8.1, "Wafer-Level-Integrated Vertical-Waveguide sub-Diffraction-Limited Color Splitters," *S. Kang, et al, IMEC/KU Leuven/Ghent Univ.)*

then tune those wavelengths to match the color sensitivity of the human eye. In the **paper #8.1**, "***Wafer-Level-Integrated Vertical-Waveguide sub-Diffraction-Limited Color Splitters,***" an IMEC-led team described a fundamentally new way to do this at sub-micron pixel sizes (i.e., beyond the fundamental Abbe diffraction limit) using standard backend processing on 300 mm wafers. They built an array of Si_3N_4 multimode waveguides in a SiO_2 matrix. Each waveguide splits a different frequency of light into both symmetric and asymmetric modes, which propagate through the waveguide differently, leading to a unique "beating" pattern between the two modes for a given frequency. This beating pattern is used to represent a certain color (Fig. 14). The researchers said this technique enables further scaling of high-resolution imagers, with the ultimate goal being to detect every incident photon.

A Smart Image Sensor: A Macronix-led team described in the **paper #33.2, "*3D Monolithically Integrated Device of Si CMOS Logic, IGZO DRAM-like, and 2D MoS2 Phototransistor for Smart Image Sensing***" a sequentially stacked device for smart image sensing applications. They built on an 8-inch Si wafer a three-tier monolithically integrated device that included 20nm Si FinFETs, IGZO-based DRAM-like devices, and MoS_2 TMD phototransistors with ultra-high responsivity (Fig. 15). With it, they successfully demonstrated a Si FinFET-based logic inverter and NAND and NOR gates; long data retention (>1000s) and low-power working memory for computing-in-memory functions; and a 5x5 array of MoS_2 TMD phototransistors with responsivity of >1 A/mW and large tunable photo-gain. This novel platform shows the advantages of BEOL fine-pitch vertical interconnects and can enable small form-factor and ultra-thin smart image sensing systems.

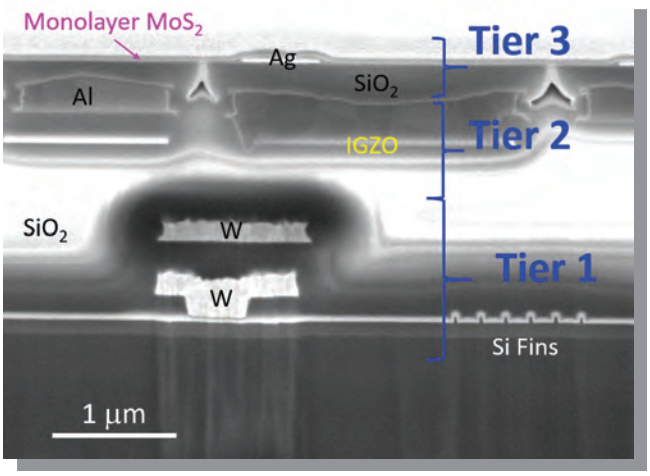

*Figure 15. Ccross-sectional SEM view of the 3-tier monolithic 3D image sensor fabricated using a low-thermal budget process; it includes Si FinFETs (Tier 1), 2T0C IGZO devices for DRAM-like operations (Tier 2), and MoS2 phototransistors (Tier 3) (Paper #33.2, "*3D Monolithically Integrated Device of Si CMOS Logic, IGZO DRAM-like, and 2D MoS_2 Phototransistor for Smart Image Sensing," *F.M. Lee, et al, Macronix/Taiwan Semiconductor Research Institute/National Tsing Hua Univ.)*

Noteworthy Papers on Diverse Topics

A Flashlight into the Brain: In the **paper #25.6**, "***Dual-Wavelength Neural Probe for Simultaneous Opto-Stimulation and Recording, Fabricated in a Monolithically Integrated CMOS/Photonics Technology Platform***," IMEC researchers detailed a monolithically integrated CMOS/photonics platform, capable of supporting passive and active visible photonics with thermo-optic switches. It incorporates PECVD SiN waveguides built in a 130-nm SOI CMOS process with six layers of aluminum BEOL. They used this platform to demonstrate an implantable CMOS-based neural probe that simultaneously stimulates the brain optically and reads electrical signals from it. It integrates a high-density array of 960 selectable electrodes/384 recording channels with 14 programmable optical emission sites for two visible wavelengths (450 nm and 638 nm) (Fig. 16). Compared to existing multifunctional neural probes having optical transmission and electrical recording capabilities, these probes achieved the largest number of emitters with dual-wavelength operation (a 14x improvement), an order of magnitude higher number of electrodes per shank (>10x improvement), and for the first time,

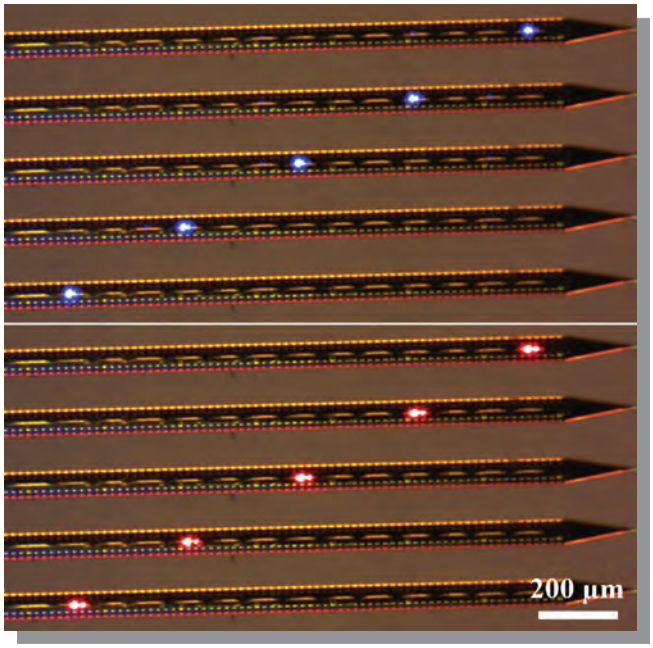

*Figure 16. Microscope images of the shank taken during switching between emission sites 1, 4, 7, 10, and 13, at light wavelength 450nm (top), and 638nm (bottom) (Paper #25.6, "*Dual-Wavelength Neural Probe for Simultaneous Opto-Stimulation and Recording, Fabricated in a Monolithically Integrated CMOS/Photonics Technology Platform, *" P. Neutens, et al, IMEC).*

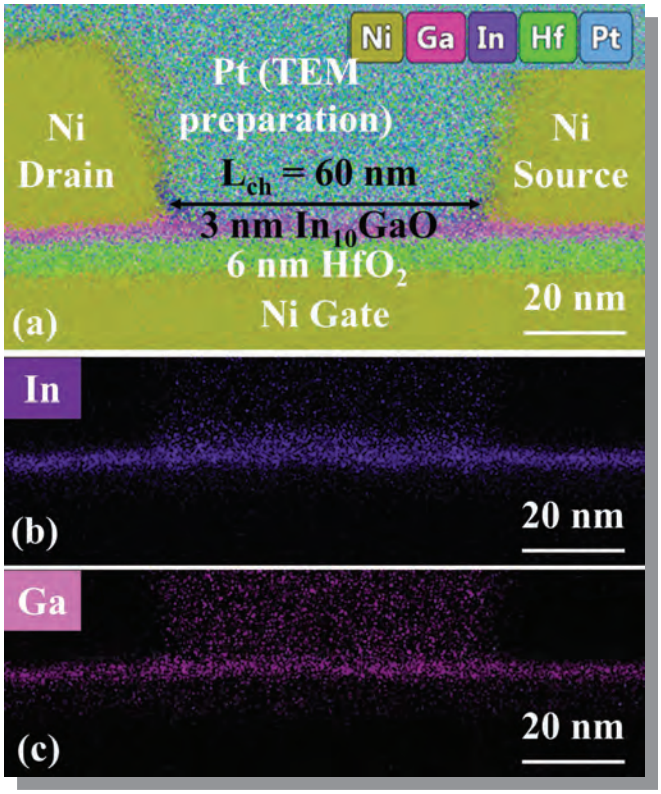

*Figure 17. A STEM image of 60nm-channel length InGaO TFTs (a), EDX mapping of indium (b) and gallium (c) (Paper #41.1, "*Fluorine Anion-Doped Ultra-Thin InGaO Transistors Overcoming Mobility-Stability Trade-Off, *" J. Zhang, et al, Purdue Univ./Xiamen Univ.)*

a monolithically integrated readout IC. This technology gives the neuroscience community a powerful tool to use in studies of cell/circuit-specific activity and neural modulation monitoring through optogenetics-based optical tagging. It also can open up opportunities in other applications such as biosensors and super-resolution microscopy.

Boosting the Reliability of BEOL-Based Thin-Film Transistors: Building and incorporating ultra-thin CMOS transistors into a chip wiring, or interconnect, as it is fabricated during back-end-of-line (BEOL) processing is a compelling way to build the monolithic, highly integrated 3D devices needed for future neuromorphic, AI, and other computing applications. But while thin-film transistors (TFTs) made from In_2O_3 are compatible with the low-temperature techniques used in BEOL processing, they suffer from defects such as oxygen vacancies which lead to poor performance and/or temperature/bias instability, impacting their reliability. In **paper #41.1**, "***Fluorine Anion-Doped Ultra-Thin InGaO Transistors Overcoming Mobility-Stability Trade-Off***," a Purdue-led team discussed the use of an alternate channel material (InGaO), doped with fluorine to neutralize defects. They built BEOL-compatible InGaO TFTs with ultra-thin (~3 nm) 60 nm-long channels (Fig. 17), demonstrating enhancement-mode operation and the highest on/off current performance ever seen in such devices (I_{ON}/I_{OFF} ~10^{11}). They featured a high I_{ON} of 418 μA/μm, along with what the researchers call "a remarkably high degree" of temperature/bias stability. The work shows the critical importance of dopants to achieve higher reliability in oxide-based TFTs, and in particular the benefit of using anions (negatively charged) like fluorine in these devices vs. more typically used cation (positively charged) dopants.

Co-Design of Materials & Devices for 2D-Based Logic Circuits: A Spin-FET is a transistor that controls current flow using electron spin states instead of using a charged layer. Although various 2D materials with a wide range of spin-orbit coupling and exotic structural/electrical properties are attractive for designing spin-based transistors and interconnects, the lack of a thorough understanding of spin dynamics has prevented the practical realization of 2D spin logic. In the **paper #3.4**, "***A Materials-Device Co-Design Framework for Realizing Ultra Energy-Efficient All-2D-Spin-Logic Circuits with 2D-Materials***," a UC-Santa Barbara-led team detailed a novel materials–device co-design framework that models many different relevant spin relaxation/dephasing mechanisms, in order to provide realistic design guidelines to both materials and device engineers to advance the state-of-the-art. In particular, the authors revealed that the 2D material graphene has spin diffusion lengths >25 μm, and they showed that circuits based on optimized 2D Spin-FETs outperform their MOSFET counterparts by an order of magnitude in energy delay, and by two orders of magnitude in energy efficiency (Fig. 18).

Other Events in the Time-Frame of 2023 IEDM

In addition to the technical program, several other events took place during 2023 IEDM. On Tuesday, 12 December, there was **a career-focused luncheon** featuring industry and scientific leaders talking about their personal experiences in the context of career growth. The discussion was moderated by Jennifer Zhao, President/CEO, asm OSRAM USA Inc. The speakers were Ilesanmi Adesida, University Provost and Acting President, Nazarbayev University, Kazakhstan, and Isabelle Ferain, Vice-President of Technology Development, GlobalFoundries. On the same day, the **Evening Panel Session** was held. It is an interactive forum where experts give their views on important industry topics, and audience participation is encouraged to foster an open exchange of ideas. The panel was moderated by Dan Hutcheson, Vice Chair at Tech Insights. John Chen, NVIDIA was the panel co-organizer. The topic was *AI: Semiconductor Catalyst? Or Disrupter?* Artificial Intelligence (AI) has long been a hot topic. In 2023 it became super-heated when large

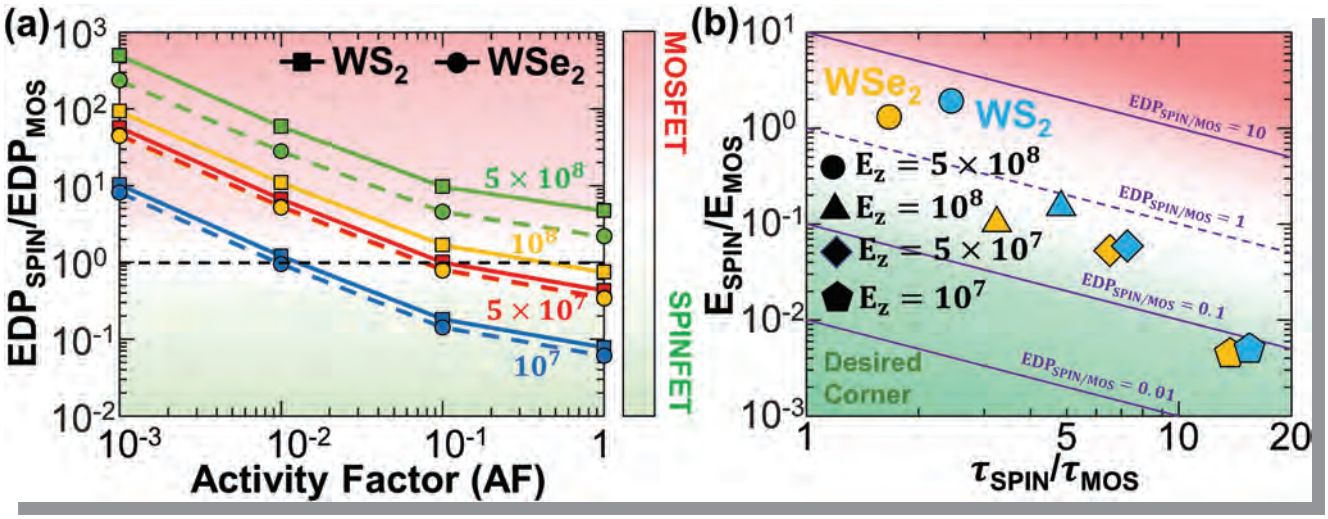

*Figure 18. Energy-delay-product (EDP) ratio of Spin-FET-to-MOSFET with p-type WS_2 and WSe_2 channels, as a function of circuit activity factor (AF) for out-of-plane electric fields (E_Z) of 10^7, 5×10^7, 10^8, and 5×10^8 V/m at 100K. The black dashed line (ratio = 1) demarcates the regions where Spin-FETs (green) and MOSFETs (red) show more EDP benefit (Paper #3.4, "*A Materials-Device Co-Design Framework for Realizing Ultra Energy-Efficient All-2D-Spin-Logic Circuits with 2D-Materials," *S. Zhang, et al, UC-Santa Barbara/Zhejiang Univ.)*

language models became readily available to the public. The 2023 IEDM brought together industry experts to have a conversation about how AI is changing the semiconductor industry and to ask them how they are using AI to transform their efforts. The panelists were Pierre Paulin, Synopsys; Ira Leventhal, Advantest; Chris Lin, TSMC; Nicole Saulnier, IBM; and Anantha Sethuraman, Applied Materials. The topics were wide-ranging, from how AI will drive demand for semiconductors, to how it's changing design and manufacturing, and even to how it will change the jobs and careers of those working in it.

Three other events are also worth mentioning, namely:

- A vendor exhibition;
- A special poster session dedicated to MRAM (magnetoresistive RAM memory) was held on Tuesday, 12 December from 2:20 p.m. to 5:30 p.m. Various topics were covered including MRAM materials, phenomena, technology, testing, hybrid CMOS/MTJ technology and circuits, and spin-logic. The session was technically organized by the IEEE Magnetics Society.
- Also sponsored by the IEEE Magnetics Society, the 15th MRAM Global Innovation Forum was held in the same venue after the IEDM conference concluded, on Thursday, 14 December. The Forum consisted of 10 invited talks from leading experts and a panel discussion. Various MRAM-related topics were covered including STT-MRAM technology deployment for embedded and standalone memories, trends, and the needs, challenges, and potential of future MRAM.

We hope that this overview will be useful to you and that it will encourage you to seek information on topics of interest to you in the 2023 IEDM materials, which will be available through IEEE Xplore. We are looking forward to meeting you at IEDM 2024!

For registration and other information, visit www.ieee-iedm.org. Follow also IEDM via social media:

- Twitter: https://twitter.com/ieee_iedm
- LinkedIn: https://www.linkedin.com/groups/7475096/
- Facebook: https://www.facebook.com/IEEE.IEDM

A Review of the 2023 IEEE International Integrated Reliability Workshop (IIRW): the Flagship Workshop on recent advances in Integrated Electronics Reliability

The aim of IIRW is to provide an annual international forum for the presentation and discussion of recent advances in all aspects related to electronics reliability. As the demand for higher computational efficiency increases and diversifies, the level of reliability required for modern devices, circuits, and systems is rapidly increasing, fostered by economic drivers such as the automotive industry, the advent of artificial intelligence, edge computing, high-performance computing, and aerospace. Therefore, more than ever before, a deeper interaction among reliability engineers, technologists and device experts, circuit designers, and system developers is necessary. In this scenario, IIRW provides the ideal setting in which the attendees can meet at the beautiful Fallen Leaf Lake, CA, USA, to exchange ideas over four days in a friendly and informal environment. The event was held in person, October 8–12 2023. Notwithstanding the echoes of the global pandemic, the widespread economic instabilities, the semiconductor business stagnation, and the critical war scenarios in Eastern Europe, the event was joined by participants from all over the world, achieving the second-highest attendance in the last ten years (excluding 2020 and 2021 in which IIRW went fully virtual), confirming the attractiveness of the workshop for the semiconductor reliability community. The IIRW conference was financially sponsored by the IEEE Electron Devices Society and Reliability Society. In addition, world-class companies in the field of micro- and nano-electronics co-sponsored the conference:

- *Major Patrons*: GlobalFoundries, Siemens, QualiTau
- *Supporting Patron*: Celadon Systems

Given the unique and secluded location of the conference, many attendees had to face a long journey to the Stanford Sierra Conference Center in Fallen Leaf Lake. Thus, the first day of the conference was dedicated to welcoming the attendees. A dinner provided ground for the attendees to start getting to know each other, before the traditional Sunday Night Tutorial, a "techlite" lecture delivered after dinner—this year the topic was the role of analog electronics in music.

The conference was then officially opened by the General Chair of the conference, Prof. Francesco Maria Puglisi (University of Modena and Reggio Emilia, IT), and by the Technical Program Chair, Dr. Charles LaRow (Intel Corporation, US) who welcomed the attendees and delivered the commemorative plaques to the awardee of the 2022 IEEE IIRW Best Student Paper Award (Tommaso Rizzi, IHP Microelectronics GmbH, DE) and to the General Chair of the 2022 IEEE IIRW, Dr. Matthew Hogan (Siemens Digital Industry Software, US). After the introduction and conference opening, the Keynote presentation by Dr. Elisa Vianello (CEA-Leti, FR) followed. Dr. Vianello's talk was entitled "Harnessing the potential of imperfect resistive memory technologies for efficient computing" and gave the attendees a vision of how it is possible to actually leverage on the intrinsic reliability issues of emerging devices such as resistive memories to realize dependable and reliable neuromorphic and in-memory computing systems, which are pivotal for the much awaited pervasive introduction of ubiquitous artificial intelligence on energy-constrained devices. Dr. Vianello showed how resistive random access memory (RRAM) holds tremendous promise for the development of innovative neuromorphic and in-memory computing platforms by enabling highly parallel, low-power, and low-latency computations, offering significant advantages in terms of energy efficiency and computing power for AI workloads compared to traditional systems. She then showed how implementing such computations using RRAM devices presents challenges due to practical device limitations, including variability, quantization error, and limited endurance, to then focus on various strategies for effectively integrating unreliable devices into neuromorphic and in-memory computing paradigms, capitalizing on the unique

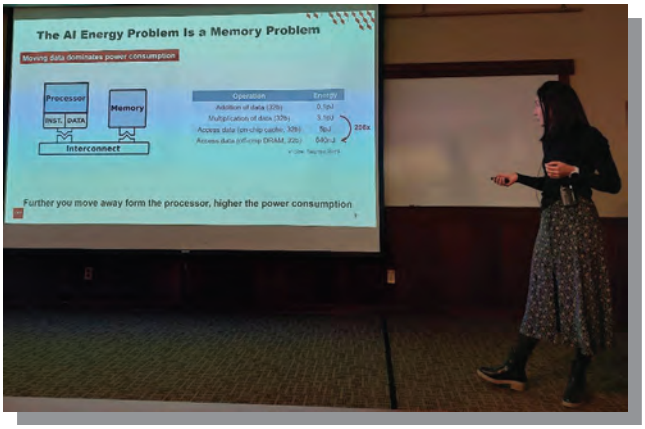

Figure 1. A picture from the keynote presentation by Dr. Elisa Vianello (CEA-LETI) entitled "Harnessing the potential of imperfect resistive memory technologies for efficient computing".

Figure 2. A group picture of the panelists who contributed to the Reliability Experts Forum, together with, on the right, the REF moderator (Dr. Zakariae Chbili, Intel Corporation) and the two REF Co-Chairs (Michael Waltl, TU Wien—Suresh Uppal, Rivos Inc.).

imperfections of RRAM devices leading to new neuromorphic circuits and Bayesian nanoelectronics.

On top of that, 20 contributed papers with deep insights and high-level technical content were presented during the conference in 7 sessions focused on specific reliability topics (Transistors, Power and RF, Device and Circuit, BEOL, Metrology and Characterization, and Memory). The sessions also included 8 invited talks by prestigious speakers on different topics, ranging from 2D materials reliability to new challenges in packaging. Additional 13 contributed papers were presented in the Poster Session, hosted after dinner on the third day of the conference, in which lively discussions between the poster presenters and the attendees took place, providing the ideal ground for ideas exchange and networking. All contributed papers can be found in the proceedings published on *IEEEXplore*.

A peculiar feature of IIRW is that tutorials are not offered in parallel sessions on a dedicated day, but are rather disseminated during the whole conference, each placed in a strategic time slot according to the subject in order to give the audience, especially students, the necessary tools to fully engage in ensuing highly technical discussions on a given topic. In 2023, tutorials were given by Cristian Zambelli (University of Ferrara, IT—"Emerging Memory Reliability"), Stephen Moxim (NIST, US—"Connecting the Dots between Analytical Magnetic Resonance Results and Semiconductor Device Reliability"), and Gennadi Bersuker (M2D Solutions, US—"From Chaos to Order: Evaluating Memristor Technologies for neural network implementations").

IIRW has evolved over the last years to include a unique event called the "*Reliability Experts Forum*" (REF), where a pool of world-class reliability experts from both industry and academia contributes to two themed panels on hot topics in reliability, involving the audience in a wide and lively discussion. Attendees registered for the conference had the chance to attend all of the scheduled activities, including the REF, the tutorials, the discussion groups, all the invited and contributed oral presentations, and the poster session. In 2023, IIRW hosted the sixth edition of the REF on the third day of the conference, to which eleven experts gathered in a day-long discussion articulated in two panels to debate about *i*) Aging in Advanced Nodes and Hot Carrier Degradation; and *ii*) V_{MAX} and technology scaling. The event was moderated by Dr. Zakariae Chbili (Intel Corporation, US). The first panel was honored by the presence of Dr. Miaomiao Wang (IBM, US), Dr. Erik Bury (imec, BE), Prof. Souvik Mahapatra (IIT Bombay, IN), Dr. Minjung Jin (Samsung, KR), and Dr. Andreas Kerber (Intel, US) as panelists, sharing their expertise with the audience. After a short presentation by each of the panelists, the audience engaged in an energetic discussion that involved the other panelists as well. Different aspects related to the main topic were discussed, including a general introduction to the topic, advanced modeling strategies, consequences at the device and circuit level, and industry-level strategies to deal with the unpredictability of the aging response in the most advanced nodes. The second panel, held in the afternoon, has seen panel contributions from Dr. Jeffrey Hicks (Intel Corporation, US), Dr. John Faricelli (AMD, US), Dr. Bonnie Weir (Broadcom, US), Dr. Jen-Hao Lee (TSMC, TW), and Dr. Patrick Justison (GlobalFoundries, US). Notwithstanding the long and vivid discussions held in the

Figure 3. Introducing the "Aging in Advanced Nodes and Hot Carrier Degradation" panel of the Reliability Experts Forum.

Figure 4. The Technical Program Chair (left, Dr. Charles LaRow, Intel Corporation) and the General Chair (right, Prof. Francesco Maria Puglisi, Università di Modena e Reggio Emilia).

morning, stimulating questions and discussions came from the audience as a result of the short presentations from the panelists. Perspectives on the factors truly limiting the supply voltage reduction in scaled technologies and on strategies to circumvent them were given by both fab leaders and design experts, offering a diversified but clear and comprehensive picture.

In addition, the conference hosted four discussion groups. After the dinner on the second day of the conference, two parallel discussion groups took place. The first was entitled "Talent Pipeline from Academia to Industry", was moderated by Dr. Zakariae Chbili (Intel Corporation, US) and focused on the current worldwide crisis of education in semiconductors and the so-called talent shortage, at the center of structural initiatives such as the US and EU Chips Acts. The second was instead focused on "Challenges in Electromigration with New Materials and Constructs" and was led by Prof. Lado Filipovic (TU Wien, AT). The presence of renowned experts in the field of electromigration made the discussion group a success. Two additional parallel discussion groups took place after the dinner on the fourth day of the conference. The first was entitled "Aging in Advanced Nodes" and was moderated by Dr. Theresia Knobloch (TU Wien, AT). Echoing the lessons learned during the first REF panel, the discussion pinpointed the expectation of the reliability community on the next generation of devices for ultimate scaling in terms of aging mechanisms, reliability margins, and possible new phenomena to carefully consider to guarantee a smooth transition toward both the beyond CMOS and the angstrom era. The second was entitled "TDDB: Is the Power-law the end of the road?", and was moderated by Dr. Bonnie Weir (Broadcom, US). Both the academic and the industrial perspectives were discussed, proposing ideas and methodologies to appropriately assess the TDDB margin. New insights derived from recent studies on AC breakdown and on the microscopic modeling of oxide integrity together with remarks from the second REF panel were brought into the discussion, bringing the community one step closer to potentially answering the long-standing question that gave the title to the discussion group.

The conference also included a social program. At the end of each day, characterized by an intense technical program, the attendees were welcomed in the "Old Lodge", a cozy cabin in which a friendly reception took place, promoting networking among the attendees. In addition, the whole afternoon of the fourth day of the conference was free of technical activities for the attendees to enjoy the unique location in which the event took place. Many returning attendees escorted first-time IIRW participants in hiking on amazing routes around the lake and up to Mount Tallac to enjoy a breathtaking view. The conference was then officially closed before lunch on the last day, with the announcement of the IIRW 2024 conference, which will take place in Fallen Leaf Lake, October 6 through 10, 2024. The deadline for a two-page abstract submission is June 16, 2024, and the preliminary Call for Papers is available at www.iirw.org.

In summary, IIRW 2023 was an inspiring event with ample participation and a rich and stimulating program. The IIRW community is looking forward to another exciting edition in Fallen Leaf Lake, CA, USA, October 6 -10, 2024.

Francesco Maria Puglisi
2023 IEEE IIRW General Chair

The 5th IEEE International Flexible Electronics Technology Conference 2023

The 5th IEEE International Flexible Electronics Technology Conference (IFETC) 2023, hereafter referred to as the "conference," was held during 14–16 August 2023 at the DoubleTree by Hilton hotel, San Jose, California, USA. This in-person conference featured outstanding presentations of contributed and invited papers and contributed posters by researchers from industry and academia as well as students from 17 countries worldwide along with *five* Plenary talks by prominent multi-disciplinary experts from the industry and academia over three scheduled days of the conference.

The conference was inaugurated on Sunday, 13 August with pre-conference tutorials in the morning and short courses in the afternoon aimed at students, practitioners, and individuals transitioning to the broad technical area of flexible/printable electronics. The tutorials and short courses were presented by internationally recognized researchers and technologists from industry and academia. The topics and instructors have been carefully chosen to have broad appeal to IFETC 2023 participants including students as well as experts in the field.

The topics of the *three tutorials* included:

- "Printed and Flexible Electronics and Devices: An Overview," by Dr. Meyya Meyyappan, Indian Institute of Technology, Guwahati, India (formerly, NASA Ames Research Center, Mountain View, California, USA);
- "Nanocarbon-Based Flexible and Stretchable Electronics," by Professor Min Zhang, Peking University, Shenzhen Graduate School, China; and
- "Flexible RFID-Tags for Smart Label Applications in Retail and Logistics," by Professor Neils Benson University of Duisburg—Essen, Germany.

The topics for *three short courses* were:

- "Inkjet-Printing Technology: From a Droplet to Flexible Electronics and 3D Artificial Tissues," by Professor Sungjune Jung, POSTECH, Korea;
- "Distributed Printed Electronics for Sustainable Environmental Practices," by Professor Gregory Whiting, University of Colorado, Boulder, Colorado, USA; and
- "Flexible and Hybrid Electronics," Professor Mark D. Poliks, State University of New York, Binghamton, USA.

The main conference opened on Monday, 14 August morning with the Plenary Session presenting *three* featured talks:

- the first, "Soft, Wireless Skin-Interfaced Devices for Health Monitoring and Haptic Interactions," by Professor John Rogers of Querrey-Simpson Institute for Bioelectronics, Northwestern University, Evanston, Illinois, USA;
- the second, "Flexible Substrates for Fabrication of Electronic Devices," by Dr. Jeffrey King of Corning West Technology Center, Palo Alto, California, USA; and
- the third, "Plasma Jet Printing for Printed Electronics," by Dr. Dennis Nordlund of Space Foundry, San Jose, California, USA.

On Day 2, Tuesday, 15 August, the conference sessions began with a Plenary talk,

- "Electronic Skins for Robotics and Healthcare Applications," by Professor Takao Someya of the University of Tokyo, Japan;

and, on Wednesday, 16 August, the conference opened with the Plenary talk,

- "Skin-Inspired Sensors, Integrated Circuits and Bioelectronics," by Professor Zhenan Bao of Stanford University, CA, USA.

The conference technical program was organized into a total of 17 sessions with multiple parallel sessions featuring papers on a broad range of flexible/printable electronics device/manufacturing-related topics including sensors, displays, and in general large area flexible electronics systems within *eight* technical areas:

1) Materials, Devices, and Processing,
2) Energy Harvesting and Storage,
3) Sensors, Actuators, and Bioelectronics,
4) Circuits and Systems Integration,
5) Functionalities, Performance, and Reliability,
6) Packaging, Heterogeneous Integration, and Manufacturing,
7) Emerging Applications and Products,
8) Flexible and Printable Solutions for RFID Identifications.

Each session included contributed and invited papers on cutting-edge flexible/printable electronics device/manufacturing-related topics within the scope of the above-selected *eight* technical areas. In this brief review, no attempt is made to summarize these papers that are available on IEEE*Xplore*: https://ieeexplore.ieee.org/xpl/conhome/10254736/proceeding. The following basic trends are observed from the presented papers at the IFETC 2023.

A large number of presentations were on *Materials, Devices, and Processing* showing a huge R&D effort leading to the manufacturing of transistors and sensors on flexible substrates. The papers include metal-halide perovskites flexible transistors, microscale photodetectors, and sensors; In-Ga-Zn-O source-gated thin-film transistors on a

flexible polyimide film substrate; sol-gel-based *p*-type copper-oxide high-performance thin-film transistor by doping the precursor solution with an alkali metal for flexible electronics; and one-dimensional and bidimensional materials technology to achieve devices and circuits on flexible substrates for large scale integration.

The papers on *Energy Harvesting and Storage* included presentations on high-efficiency ultrathin transition metal dichalcogenides (TMDs) flexible (WSe^2) solar cells using novel approaches in semiconductor device design, TMD materials growth, and photonic engineering; high-efficiency III-V flexible photovoltaic (PV) devices grown by multi-chamber hydride vapor phase epitaxy (HVPE); triboelectric nanogenerators (TENGs) for harvesting ambient mechanical energy to produce electrical power and operate self-powered sensors and wearable electronics using advanced 3D printing techniques; and materials and techniques to fabricate flexible supercapacitors and batteries.

There were, also, a large number of presentations on *Sensors, Actuators, and Bioelectronics*. The presentations included skin-interfaced wearable biosensors; wearable sensors for non-invasive sport monitoring; multilevel fabric mold textures film-based flexible pressure sensors; high-density, superior-performance and large-scale TFT-based optical/pressure/biosensors; thin-film temperature sensor on flexible polyether ether ketone (PEEK) fabric substrate with possible applications in automotive, fuel, and gas filtering monitoring; polymer-based sensors for gastrointestinal temperature and gas monitoring; battery-free wearable electrochemical sweat sensors using energy harvesting modules such as TENGs, biofuel cells (BFCs), and solar cells; biomimetic polymer electronics for intimate bio-interfaces; flexible hybrid electronics wearable sensors for mental health monitoring; inkjet-printed flexible sensors, for diabetic foot ulcer monitoring; flexible Tactile Sensors; and so on.

In continuation, there were a good number of excellent presentations on the practical implementation of flexible/printable electronics in manufacturing and productization with concentrated efforts on circuits and systems integration; functionalities, performance, and reliability engineering as well as emerging applications, specifically in the healthcare industry.

Along with the IFETC 2023, the 14th *International Conference on Computer-Aided Design for Thin-Film Transistor Technologies* (CAD-TFT) was co-located in San Jose on 16 August 2023. And, there were excellent presentations in CAD-TFT 2023 from industry and academia including numerical process and device simulation of TFT as well as compact TFT modeling for circuit analysis.

In addition to excellent contributed and invited paper sessions on the above briefed diverse topical areas of flexible/printable electronics, on *Monday, 14 August* morning, EDS president, Ravi Todi formally introduced the *75th Anniversary of the Transistor*, a commemorative book published by Wiley-IEEE Press in July, 2023. And, the evening featured the *Women in Electron Devices Society and Young Professionals* session to delve the power and influence of women and young professionals into. The session "Diversity in the Next 75 Years of the Transistor: Off to a Good Start;" on *Tuesday, 15 August* featured a luncheon talk, "Marketing the Unknown," by Sri Peruvemba of Marketer International, Inc., San Ramon, California, USA, and an evening interactive panel session, "Why and How Investment Would Accelerate Growth in Flexible/Printable Electronics Industry?," offering a forum for deep-dive discussions on the potential growth of flexible/printable electronics industry around the globe.

Samar Saha
Prospicient Devices, USA
IFETC 2023 General Chair

IRDS–Factory Integration Roadmap

Supika Mashiro
Tokyo Electron Limited, Co-chair of Factory Integration
James Moyne
University of Michigan, Applied Materials, Co-chair of Factory Integration

1. Introduction

The Factory Integration (FI) chapter of the IRDS is dedicated to ensuring that the manufacturing infrastructure of the microelectronics represented by Si-based semiconductor devices contains the necessary components to produce items at affordable cost and high volume in a sustainable manner. Realizing the potential of Moore's Law and novel device structures beyond traditional CMOS-based devices requires taking full advantage of device feature size reductions, new materials, yield improvement to near 100%, wafer size increases, and other manufacturing productivity improvements. This in turn requires a factory system that can fully integrate additional factory components and utilize these components

collectively to deliver items that meet specifications determined by other IRDS international focus teams (IFTs) as well as cost, volume, and yield targets. Preserving the decades-long trend of a 30% per year reduction in cost per function [1] also requires capturing all possible cost reduction opportunities. These include opportunities in front-end as well as back-end production, facilities, yield management and improvement, increased system integration such as up and down the supply chain, improving environmental health and safety performances, and supporting sustainable microelectronics production. FI challenges play a key role in microelectronics realizing its full potential for society and many FI technology challenges are becoming limiters to achieving major technology milestones for microelectronics.

In particular, the FI chapter addresses several challenges/issues that threaten to slow the industry's growth, including:

- *Complex business models with complex factories*—Rapid changes in microelectronics technologies as well as business requirements, such as the need for faster product delivery, high-mix production, and volatile market conditions, make effective and timely factory integration to meet accelerated ramp and yield targets more difficult over time. The factory now must integrate an even larger number of new and different equipment types, software applications, and data to meet complex market objectives and customer requirements. High mix and low-volume product runs are making mask cost, fabrication, and FI extremely difficult in a market where average selling prices are declining.
- *Ramp-up of new technologies*—Closer integration of the industry is required for successful ramp-up of new technology nodes and device architectures. There is a need for improved hardware and software capabilities as well as more rapid reliable deployment of these capabilities. Examples include process characterization involving nascent device materials, chemicals, gasses, and consumables, where the wafer process environments are far better protected to prevent yield losses and productivity degradation, and environmental impacts are assessed in advance and better controlled.
- *Control system evolution*—Control systems will continue to become more granular (e.g., lot-to-lot, to wafer-to-wafer, to within wafer), and higher speed (e.g., run-to-run to real-time quality parameter control). Centralized versus various levels of distributed control is also being evaluated, both in a horizontal (e.g., distributed applications and control optimized across the supply chain) and vertical (e.g., internal tool fault detection tied to higher level maintenance activities) sense. Big Data characteristics must improve to support the evolution of control systems. Smart Manufacturing (SM) leverages the tremendous advances in volume, velocity, variety, veracity (i.e., data quality), and value (analytics) of data, often referred to as "Big Data," by applying Big Data analytics to improve existing analysis capabilities and provide new capabilities such as predictive analytics.
- *Supply chain integration and management* — FI connectivity up and down the supply chain leveraging the accelerated information technology (IT) trends will be necessary to support tightening of production methods (e.g., associated with lean manufacturing) and addressing business requirements (e.g., for yield correlation, warranty traceability, cost reduction, and ESG (Environment, Social, and Governance) related data communication).
- *Security*—Information security will be associated with significant issues in addressing almost all difficult challenges in the near term and to a certain extent in the long term. For example, in addressing one of the near-term challenges of responding to rapidly changing, complex business requirements, security gaps (e.g., data ownership, access authentication, and authorization systems) are considered the main reason that is preventing the microelectronics industry's migration to Cloud-based Big Data Analytics. Given the increase of data shared across the factory integration space, it will become more challenging to ensure the protection of the fab instrumentation and control systems as well as equipment operation control systems from unauthorized access, operation, or alteration from both inside as well as outside the fab. For example, the concept of the "connected fab," which is one of the central concepts of Industry 4.0/ Smart Manufacturing, indicates potential direct data exchanges beyond the factory integration space within a Fab or enterprise owning Fabs. While data must be made available to promote fault detection and classification (FDC), predictive maintenance (PdM), advanced process control (APC), etc. at more granular levels (e.g., lot-based to single wafer-oriented for maximizing productivity), protection of data and intellectual property (IP) within data will become more complicated and sometimes contradictory to needs of data availability.
- *The move to Smart Manufacturing (SM)*—Smart manufacturing (SM) is a term "generally applied to a movement in manufacturing practices towards integration up and down the supply chain, integration of physical and cyber capabilities, and taking advantage of advanced information for increased flexibility and adaptability". It is often equated with "Industry 4.0" (I4.0), a term that originated from a project in the German government that promotes a 4th generation of manufacturing that uses concepts such as cyber-physical systems, virtual copies of real equipment

and processes, and decentralized decision making to create a smarter factory [2,3]. The industry needs to embrace the movement to SM that incorporates advances in Big Data, augmenting Reactive with Predictive and Prescriptive, advanced analytics and applications, digital twin, Industrial Internet of Things and the Cloud, integrated supply chain, and reliance on a knowledge network. While the literature base for SM and I4.0 is wide and varied, common themes or tenets of SM are present that help provide an understanding of the whole SM and I4.0 space, as well as the structure for the organization of SM roadmap elements [4]. Although the tenets of SM and I4.0 are industry-agnostic, the unique challenges and opportunities facing the microelectronics industry require migration strategies unique to the industry, which will be detailed in Section 5 of this article.

- *Increased integration of FI with YE and ESH/S solutions*—As noted above, FI challenges and solutions directly impact aspects of Yield Enhancement (YE) and Environmental, Safety, Health, and Sustainability (ESH/S) roadmaps, and these roadmaps in turn place requirements and provide direction for FI. This is exemplified in areas such as yield prediction and energy and resource use efficiency improvement.

2. FI Drivers and Technology Targets

Societal driving forces and trends such as mobile devices and the Internet of Things (IoT) are impacting all areas of the IRDS, however, as shown in Fig. 1, these factors impact the evolution of FI from two perspectives, namely:

- Requirements those societal driving forces place on product technologies that are delineated in roadmaps associated with other focus areas of IRDS; these technology requirements indirectly influence FI in terms of tighter process requirements with acceptable yields, throughput, and costs.
- Requirements they place on FI technologies that directly impact FI in terms of aligning with these trends and effectively leveraging these capabilities.

An analysis of the first perspective can be found by studying the roadmaps developed by other IRDS focus groups as illustrated in Fig. 1. The same analysis can be applied to determine how the FI roadmap addresses the related tighter process requirements. With respect to the second perspective, the following is an example of how some of these drivers directly impact FI:

- The Cloud: The advent of the cloud and cloud-based technologies provides tremendous opportunities in terms of analytics, by addressing data volumes, coordination, and enterprise-wide sharing. It also provides commonality and leveraging capabilities across industries. However, the Cloud also presents challenges in terms of security from attack, security for IP protection, and performance.
- Mobility: Mobile devices have and will continue to enhance the capabilities of FI systems in terms of accessibility, ergonomics, human-machine interaction, flexibility, portability, etc., but also can present many security challenges as well as performance challenges.
- Big Data: The data explosion in manufacturing provides both challenges and opportunities for FI; a section of the FI chapter was created in the ITRS 2013 Edition and enhanced in the ITRS 2.0 2015 Edition, as well as in the IRDS 2016 whitepaper that describes these in detail [5,6].

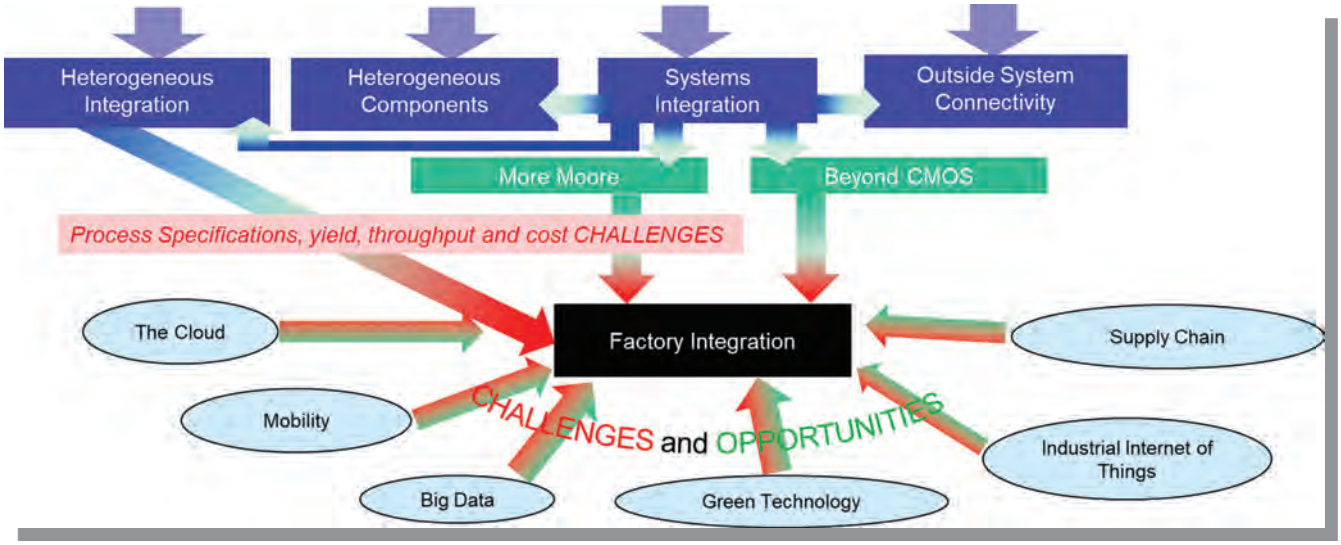

Figure 1. Societal Forces Impacting Challenges and Opportunities in FI [6].

- Green Technology: The movement towards greener technologies and subsequent requirements for reduction in energy costs and "carbon footprint" significantly impact FI. First and foremost, they require that facilities objectives such as energy consumption and ESH/S objectives such as contamination waste reduction be an integral part of FI factory operation objectives.
- Industrial Internet of Things (IIoT): IIoT technologies provide opportunities in terms of flexible connectivity and interoperability strategies for dissimilar systems across the FI infrastructure. This connectivity could be used for non-time-critical and human-in-the-loop activities when the communication is the internet, however, issues of security and response time variability must be considered and improved. The connectivity could be used for more time-critical applications such as control with intranet connectivity.
- Supply Chain: An important trend in FI is tighter integration up and down the supply chain for improved quality, traceability, efficiency, etc.

3. Vision of Future Technology

The future of microelectronics manufacturing FI is imbued in large part in the tenets of "Smart manufacturing" (SM) and Industry 4.0 (I4.0). Key tenets of this migration include leveraging Big Data infrastructures, integrating with the supply chain network, leveraging advanced analytics, improving the use of cyber-physical systems (CPS), improving the use of real-time simulation through realizing the "digital twin," and relying on a knowledge network for using subject matter expertise (SME) in an increasingly collaborative environment [7]. These terms are expounded upon in the Smart Manufacturing subchapter of the FI roadmap. This migration is associated with a number of challenges ranging from moving from reactive to a predictive/prognostic mode of operation to addressing security associated with data sharing.

4. Evolution and Extension of Factory Integration Scope

Microelectronics manufacturing extends across several manufacturing domains. FI's scope is microelectronic manufacturing including fabrication in front-end and back-end. The FI Focus Team has addressed the evolution of FI by providing an extensible roadmap that 1) focuses on the commonality of certain functional areas, 2) supports roadmaps for specific functional and physical areas, 3) addresses societal drives identified above, and 4) provides for improved synergy with Environmental, Safety, Health, and Sustainability (ESH/S) as well as Yield Enhancement (YE) objectives, requirements, and solutions. The evolution of the Factory Integration roadmap scope is depicted in Fig. 2.

The following are key factors contributing to and demanding the extension and evolution of FI scope.

- Economy of scale

The technologies addressed by the FI roadmap need to provide solutions that can be used to leverage economy of scale and resource pooling. Scaling of production

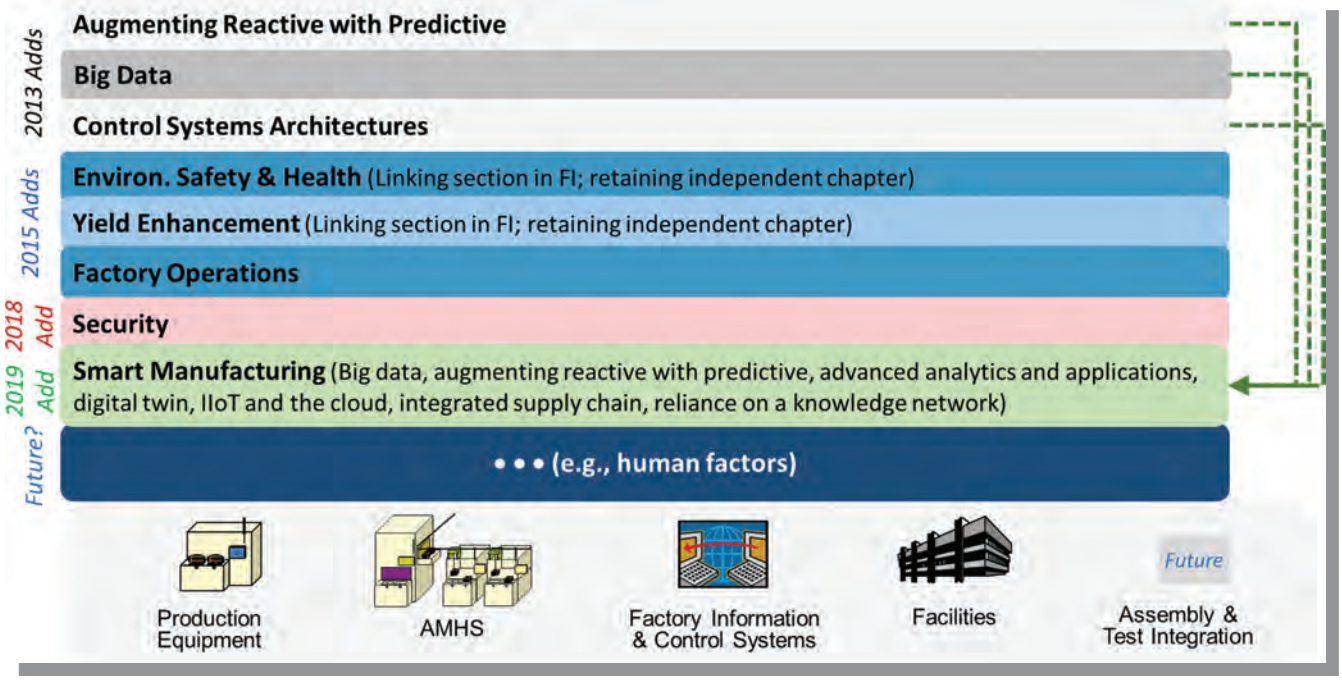

Figure 2. Factory Integration scope extension and evolution.

volumes tends to ease the typical FI issues that have an impact on cost such as 1) "design to volume production" lead time improvement, 2) yield improvement, 3) productivity waste reduction, 4) higher process controllability, and 5) reduction in utilities, power consumption and emission with even more progressive targets. Wafer size increase had also been one of the major contributing factors for the cost scaling of the semiconductor device, but this process stalled in 2015 when increasing challenges related to device functional scaling made it too difficult to continue scaling across two fronts. While it is possible that Si wafer size increase from 300mm to 450mm returns to become a high-priority FI topic again in the future, it is not deemed as a priority at least in the near or medium term, or even as far as functional performance scaling of devices continues.

- ESH/S needs data solutions in addition to traditional ESH-related demands on production equipment and Fab's facility systems.

FI scope traditionally includes some consideration on design and materials used for production equipment and the facility systems to ensure the level of ESH performance as required by regulations or Fab owners' operation policies. Implementation of Sleep mode functions for production equipment augmented with upgrades of the host-equipment message communication to support host-controlled sleep mode is an example of this type of ESH/S and FI crosscut technology requirement.

There are increasing demands from ESH/S to FI to provide better data integration and sharing not only within Fab components but also across the supply chain. For example, in order to meet near future environmental targets such as science-based targets (SBTs) in line with the goals of the Paris Agreement, collecting all the required data from every piece of production equipment and the overall facility systems operations will become paramount. This will almost certainly result in a need for more sensors and sensing methods, which can be translated into FI requirements in its production equipment as well as facility sections. Along with more sensors, networking, and data integration among sensors, equipment, and every level of control system up to the entire Fab or even a site level are to be required for better optimization of utilization efficiency of utilities (e.g., electricity or cooling water) and production materials (e.g., process chemicals/gasses) evaluated against normalized environmental impact indexes (e.g., GHG emission from Fab operation or net amount of equivalent CO2 emission). These impact indexes are called Scope 1, 2, and 3 and address the entire supply and value chain. Another ESH/S challenge example is the need to verify that semiconductor device manufacturing is compliant with ESH-related regulatory requirements, such as GHG reporting rule by the US EPA, which also is driving dedicated sensors and sensor methodologies as well as data and control integration solutions.

- Yield Enhancement (YE) needs of closer monitoring and controlling solutions as well as further integration of data in the supply and value chain.

The yield of semiconductor manufacturing has been a critical factor in determining the viability of each chip production technology, which is also the key objective of the Factory Integration (FI) chapter of the IRDS, namely producing semiconductor devices at affordable cost. Yield enhancement has been traditionally enabled by continuous improvement of the manufacturing equipment and process on one hand and by improvement of the cleanliness of the process environment and materials used on the other. There is a common understanding that systematic defect control is being addressed by IC Device Manufacturers (IDMs) working directly with the technology providers, which leaves unaddressed challenges in the space of random defect (contamination control), which is covered by the Yield Enhancement (YE) chapter of the IRDS, and the ability to respond to Yield excursion which is addressed in the Factory Integration (FI) chapter. Additionally, the need to understand and control systematic defects by the IDMs poses data availability and quality requirements to FI.

- Supply chain issues

Ongoing evolution of consumer products such as voice-activated home assistant devices and autonomous driving vehicles is heavily relying on various types of sensors, the IoT, and artificial intelligence enabled by wide varieties of semiconductor and other microelectronics devices (e.g., MEMS) This evolution has introduced the semiconductor-industry outlook of exponential growth possibility with more volatility. Today's semiconductor firms need to be more flexible, with a greater focus on research and development; increased functionality; and shorter, more efficient production times. Such changes have led to significant challenges to the traditional semiconductor supply chain, which has been accustomed to predictable demand for qualities and quantities. In order to meet the challenge posed by the evolution, all levels of production, including semiconductor device manufacturers themselves, foundries, assembly and testing firms, material providers, component, and processing equipment supplier companies will need to form an interactive, organic supply chain to meet new demands for greater capacity, performance, quality, and manufacturing costs. FI roadmap should support the application of technologies in the supply chain integration space and its challenges.

In addition to the issues stated above, the need for data transfer protocol across the supply chain for traceability of quality issues to solve productivity losses (i.e., yield losses and production equipment overall operational efficiency reduction) while maintaining data security also poses significant challenges to FI.

Furthermore, as an important part of the supply chain for the users of microelectronics devices, (e.g., automotives or medical equipment) field yield or latent yield,

which is often identified by the occurrence of a failure of the microelectronic devices in the field, can be considered as a supply chain issue within FI scope.

5. Smart Manufacturing in the Microelectronics Industry

As noted earlier, Smart Manufacturing (SM) or Industry 4.0 concepts such as cyber-physical systems, virtual copies of real equipment and processes, and decentralized decision-making are expected to create a smarter factory [2,3]. While the literature base for SM and I4.0 is wide and varied, common themes or tenets of SM are present that help provide an understanding of the whole SM and I4.0 space, as well as the structure for the organization of SM roadmap elements [7]. An SM vision for the microelectronics industry is shown in Fig. 3 [4,5]. Note that, while the tenets of SM and I4.0 are not industry-specific, each industry has its unique challenges and opportunities. IRDS FI Chapter envisions microelectronics industry-specific variations of the SM.

The microelectronics manufacturing is a unique industry characterized by high process precision requirements and a highly dynamic production environment, process and equipment complexity, high degrees of intellectual property (IP) encapsulated in production equipment, manufacturing processes, and analytical solutions, and a business model that focuses on development and maintenance of fab-wide solutions [4]. These characteristics result in unique requirements (or at least reprioritization of requirements) and challenges in realizing smart microelectronics manufacturing.

Based on an understanding of the general focus areas of SM combined with the unique needs of the microelectronics manufacturing ecosystem, the IRDS FI chapter is maintaining a roadmap for each of the following SM tenets:

- *Big Data:* Data management infrastructures are being enhanced to support improvement in capabilities associated with the "5 'Vs'", namely volume, velocity (data collection and analysis rates), veracity (data quality), variety (data merging and consolidation), and value (data analytics) [4-6]. This enhancement is punctuated by the movement to Big Data architectures that support (1) storage of data in a serial or sequential fashion, which is much more "analysis friendly" than traditional relational architectures; (2) parallel and scalable approaches for higher speed analysis of larger quantities of data; and (3) an open-architecture style environment for the development of data management and analysis tools. A key challenge is a migration from existing data management infrastructures and understanding how the data infrastructures co-exist in a collaborative environment to support capabilities ranging from real-time on-line decision-making to off-line high-fidelity model building [4].
- *Augmenting reactive operations and analysis with predictive and prescriptive*: A key aspect of the SM movement is moving from a more reactive mode of operations, where techniques (e.g., fault detection) focus on detecting and responding to an event *after* it has occurred, to moving towards a mode where events can be predicted *before* they occur (e.g., predictive maintenance) thereby avoiding any costs associated with the event. This trend also incorporates the concepts of prognostics which can be thought of

Figure 3. A Smart Manufacturing vision for the microelectronics industry [4].

as the discipline around the prediction capability, as well as prescriptive analytics which focuses on determining why an event has or will occur and how to mitigate issues in the future. While the SM focus is moving from reactive to predictive and prescriptive solutions, not all events are predictable or avoidable, thus prediction and prescription will *augment* reactive capabilities.

- *Advanced analytics and applications:* The primary benefit of the implementation of Big Data infrastructures and practices will be the enhancement of analytics to support not only improvement in the quality of existing capabilities such as fault detection and classification (FDC) but also a realization of advanced predictive capabilities such as virtual metrology (VMet) and predictive maintenance (PdM). These improved and new capabilities, summarized in Table 1, are considered part of the extended advanced process control (APC) family. The extended APC families will leverage increased data "volume" and "veracity" for more robust and maintainable models; "velocity" for more granular models; and "variety" for more causal and predictive models. From the "value" perspective, traditional analytics will become much more effective, leveraging the higher data volumes and data quality to build more robust models. New Big Data analytics such as deep learning will also emerge to complement more traditional analytics.[1] Additionally, the better integration of data systems will enable these analytics to span much larger domains, such as up and down the supply chain, and incorporate techniques such as "digital thread" for linking analyses to data chains to solve factory-wide or even supply-chain-wide problems. While there is a strong literature base in the industry of specific analytics being applied successfully to point solutions, it often is not clear how and when specific analytic types should be employed. This often results in a focus on the neatness and/or preciseness of the *analytic* (e.g., deep learning or purely statistical techniques) over the practicality, extensibility, and robustness of the *solution*, and a lack of emphasis on incorporating subject matter expertise (SME).

As a first step to address this issue, SM literature efforts have tried to define the analytics capabilities in terms of dimensions and apply these dimensions to the needs of particular applications, as shown in Fig. 4 [4]. It is expected that this definition will help guide the analytics roadmap in future FI chapters.

- *Digital Twin:* "A digital twin refers to a digital replica of physical assets, processes, and systems that can be used for various purposes" [9]. The digital twin vision is further refined as "a state of fab operations where … real-time simulation of all fab operations occurs as an extension of an existing system with dynamic updating of simulation models." Digital twins can be used to support and improve operations, controls, and forecasting throughout the manufacturing ecosystem. Many of the predictive applications being developed in the industry today will likely continue to evolve to more directly support this vision.
- *Industrial Internet of Things (IIoT) and the Cloud*: The Industrial Internet of Things (IIoT) and Cloud refers to the technical challenges and solutions associated with providing localized individual analysis and solution capabilities closer to the problem source, often referred to as an "edge" device, and providing a wide range of capabilities in a centralized, internet accessible data management and analysis location usually referred to a "cloud". Oftentimes edge and cloud solutions work together to provide more comprehensive solutions.
- *Integrated supply chain*: Tighter vertical and horizontal integration of systems is a common tenet of SM and leverages the "variety" data merging and consolidation enhancement in data architectures. From the horizontal integration perspective, the factory of microelectronics devices will become an integral part of the upstream and downstream supply chain network with factory optimization a component of overall supply chain optimization. The tighter connectivity will allow not only the microelectronics device manufacturers but also every level of the supply chain for leaner operation, better inventory management, higher flexibility of operation, improved response to demand, and better traceability to address issues such as warranty recall investigation (e.g., to address latent yield problems). An obvious requirement is the development of standards for supply chain data integration that are not specific to the microelectronics industry but applicable to its entire supply chain.
- *Reliance on a knowledge network*: The movement in technology associated with SM and I4.0 requires a corresponding change in the business operation paradigm. As solutions become more complex and consolidate larger domains of data systems and applications, realizing and maintaining these solutions requires a higher degree of cooperation between users, OEMs, and analytics solution providers in a structured knowledge network. This cooperation enables the required incorporation of subject matter expertise (SME), e.g., process, equipment, and product knowledge) into data-driven (statistical) models for improved model quality

[1] Deep Learning is a technique that is very similar to structured artificial neural networks and leverages hierarchical abstraction for improved quality and speed of high-volume data analysis [13].

Technology		Definition	NOTE
Advanced Process Control (APC)		The manufacturing discipline for applying control strategies and/or employing analysis and computation mechanisms to recommend optimized machine settings and detect faults and determine their cause [8]	1) APC includes advanced equipment control in this article. 2) Terms, APC and process control systems (PCS) are often used interchangeably
Basic APC Technologies	Fault Classification	The technique of determining the cause of a fault once it has been detected [8]	
	Fault Detection (FD)	The technique of monitoring and analyzing variations in tool and/or process data to detect anomalies. FD includes both univariate (UVA) and multivariate (MVA) statistical analysis techniques. [8]	
	Fault Detection and Classification (FDC)	Combination of FD and FC [8]	
	Fault Prediction (FP)	The technique of monitoring and analyzing variations in process data to predict anomalies [8].	
	Run-to-Run (R2R) control	The technique of modifying recipe parameters or the selection of control parameters between runs to improve processing performance. A 'run' can be a batch, lot, or an individual wafer. [8]	
	Statistical process control (SPC)	The technique of using statistical methods to analyze process or product metrics to take appropriate actions to achieve and maintain a state of statistical control and continuously improve the process capability [8]	
Technologies Extended upon APC	Equipment Health Monitoring (EHM)	The technology of monitoring processing tool (equipment) parameters to assess tool health as a function of deviation from its normal (baseline) behavior. EHM itself is not basically predictive in nature but is often a component of predictive and/or controlling systems [5]	
	Predictive Maintenance (PdM)	The technology of utilizing process and equipment state information to predict when a tool or a particular component in a tool might need maintenance, and then utilizing this prediction as information to improve maintenance procedures. This could mean predicting and avoiding unplanned downtimes and/or relaxing planned downtime schedules by replacing predetermined schedules with predictions. PdM solutions as defined herein address the entire maintenance cycle, from predicting maintenance through addressing recovery from maintenance events towards returning to production [5].	PdM for equipment or a particular equipment component can be managed at the equipment level or fab level as fab-level coordination of individual tool maintenance can contribute to fab-level productivity improvement.
	Predictive scheduling	The technology of utilizing current and projected future information on tool and factory state, capabilities, wafer/work in process (WIP), schedule, dispatch, and orders to predict and improve scheduling of a system (tool, group of tools, floor, fabs, etc.).	
	Virtual Metrology (VM)	The technology of monitoring information across the fab (e.g., tool and metrology) to predict process or end-of-line yield [8]	While E133 uses 'VM' as the acronym of Virtual Metrology, FI roadmap refers it by (VMet)
	Yield Prediction (YP)	The technology of monitoring information across the fab (e.g., tool and metrology) to predict process or end of line yield.	

Table 1. Definitions of APC and APC-extended capabilities.

and robustness. Issues such as data sharing and partitioning, intellectual property security, and managing solutions in the cloud have all come to the forefront as part of the move to enhance support for this cooperative knowledge network [5,7]. The heightened importance of incorporating subject matter expertise in microelectronics SM solutions comes from the complexity, precision, and dynamics associated with processes and equipment as noted above, but also because the production environment is associated with a large number of context changes (e.g., product change, maintenance event, or different upstream product route). In a purely statistical analysis world, these complexities would result in a need for partitioning data streams in order to understand the impact of each context change, process drift, etc. This, in turn, would result in changing the "Big Data" source into a large number of "small data" sets with insufficient precise data in each set to support good models. Incorporation of elements of process, equipment, and product SME allows quality models to be developed, verified, and especially, maintained with less data. It also allows for the intelligent merging of these small data sets when the relationships between the different contexts and dynamic situations are understood. For the above reasons, SME will continue to play an important role in analytics applications in our industry. Applications will vary, but equipment- and process expertise will remain critical components of analytical solutions for microelectronics manufacturing.

- *Security*: Although security is not a tenet specific to SM, the challenge of maintaining data and IP security has an overarching importance and relevance in realizing microelectronics SM vision. While the opportunities in SM are significant, this new paradigm of operation brings with it a risk of maintaining security in the face of higher levels of integration, data production and management, and information sharing for collaboration. While this is a challenge for SM in any industry, it is especially acute in microelectronics manufacturing where there is significant IP in process, equipment, and analysis solutions. As noted earlier in this article, information security is one of the primary challenges hindering the advancement of microelectronics industry smart manufacturing and I4.0 concepts [5,10]. Aspects of this issue vary widely ranging from concerns such as the protection of IP in collaborative activities to the introduction of malware through a USB hookup for updating a firmware that is used to collect selected data from a component of production equipment. One specific area where security is severely limiting SM evolution is data-sharing environments such as "the cloud." These environments allow data from multiple sources (including potentially multiple companies) to be centrally located so that analytics can be applied in a scalable fashion. However, as risks and solutions for cloud-based data and IP partitioning are not well-defined, many

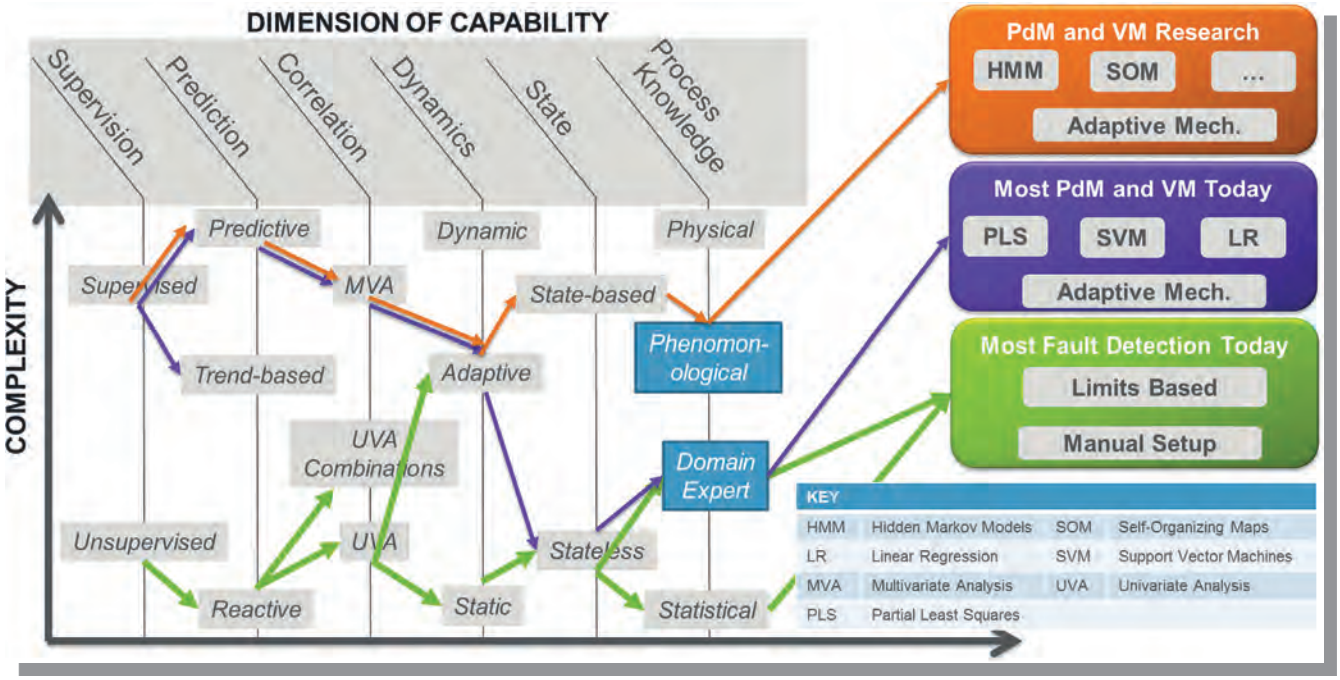

Figure 4. Example of Defining the Dimensions of Analytics Capabilities [4].

manufacturers are forced to completely avoid these solution tools, instead choosing to execute SM activities completely and exclusively within the fab. With the help of the IRDS, a roadmap to address the data and IP security issue will eventually be charted that first identifies the issues, a solution baseline, and standards needed for moving forward [4,10]. Until that time, security will likely be the main issue governing or hindering the progress of SM in the microelectronics industry.

6. Future of Analytics: AI and Further Exploitation of Big Data

Emergence or re-emergence of AI and other new Big Data-friendly analytics are expected to play an important role in realizing many of the FI objectives. Before diving into the recent and continuing evolution in this topical area, let's define a few keywords in this topical area;

- *AI*—The term AI can be used to describe any device or analytic that perceives its environment and takes action to achieve a goal. An AI system is defined as a machine-based system that, for explicit or implicit objectives, infers, from the input it receives, how to generate outputs such as predictions, content, recommendations, or decisions that can influence physical or virtual environments. AI leverages computers and machines to mimic the problem-solving and decision-making capabilities of the human mind [11]. Future manufacturing systems will increasingly leverage AI, moving from bounded learning to exploratory learning while continually improving human-artificial intelligence integration [12].
- *Deep Learning (DL)*—Deep learning (DL) is actually a sub-field of machine learning (ML) while AI and ML tend to be used interchangeably. DL differs from ML in how each algorithm learns. Deep learning automates much of the feature extraction piece of the process, reducing the manual human intervention required and enabling the use of larger data sets, hence more Big Data friendly [13].

Artificial neural networks (ANN), an example of an AI type of analytics, have been around for decades and such AI analytics have seen a resurgence as part of the Big Data evolution. DL, which is a technique very similar to structured ANN, leverages hierarchical abstraction for improved quality and speed when applied to high-volume data analysis required, for example, to optimize production equipment conditions for the process performance level necessary to achieve desirable yield. The main drawback of DL-based techniques is their relative inability to incorporate SME in model development and maintenance as well as their requirements for large amounts of data to develop models.[13,14] The models developed by the DL technique are often not explicitly available and difficult to assess, while the context richness and dynamics involved in semiconductor manufacturing analysis hinder DL-based techniques from fully leveraging large and consistent data volumes provided by the advancement of Big Data capabilities in the industry. Some research efforts have focused on combining SME with AI techniques, an approach that holds promise for future application on the manufacturing floor [12–14].

Another Big Data-friendly analytical technique is background analysis by solutions often termed "crawlers." In a similar manner to "Web crawlers", these applications mine data in the background, looking for patterns of interest in sensor trace data, such as a part nearing the threshold of its normal operation range to abnormal. They inform a relevant control system such as a PdM manager or equipment engineering system (EES) so that appropriate action can be taken to reduce unpredicted downtime.

As the microelectronics manufacturing industry migrates towards the full realization of SM, it is clear that the role of analytics empowered by Big Data advancements, in achieving yield goals while maximizing throughput and lowering cost, becomes larger.

7. The Need of Addressing the Data Sharing Conundrum

If the microelectronics industry is to fully realize the benefits of SM and especially AI analytics within the industry, it must recognize that there is a need to address a broad commercial problem. The benefits offered by SM depend upon accurate and reliable ML-based models that require large volumes of data for training and timely availability of appropriate data for inferencing. For example, DL-based models often need the use of larger and/or raw data sets to enable capabilities such as feature profiling. Within the microelectronics manufacturing Fab and across its supply chain, the data needed by AI analytics is owned by many stakeholders and may contain details that reveal proprietary IP or commercial liability. As a result, there is an inherent bias against data sharing at a level that can support the necessary modeling. In one example of many occurrences of anti-data-sharing tendencies, optimizing the complex, end-to-end process requires AI to manage the volume and rate of data flowing, but that in turn requires data from every process step to train effective models. If that data is coming from sensors integral to the operation of a process step, it may leak equipment vendor IP, so sharing with the equipment user (i.e., device manufacturer or foundry) could be seen as problematic. Meanwhile, data about the overarching process is proprietary to the user, so can't easily be shared with the equipment vendors.

The IRDS FI focus team believes, however, that this is an opportunity for exactly the type of pre-competitive collaboration that the industry has excelled at previously.

In this respect, unlocking data for AI applications will necessitate technology requirements being established in

the FI roadmap for a trusted mechanism for consuming data that is owned by multiple stakeholders, which can both ensure that stakeholder rights are protected and realize appropriate data analysis that can be of value.

8. Conclusion

The Factory Integration focus area in the IRDS is in a rather unique position in the entire set of IRDS roadmap reports in that it does not address directly any device features (e.g., structure and material) or performance requirements for devices or systems composed of devices as the core enabler of realizing each system's functions and performances. Further, it does not address technologies that directly enable device features that are required for a device technology to fulfill its functional targets such as processing speed, latency, or retention of value. Instead, the FI roadmap addresses necessary components across the manufacturing ecosystem such as facility system performance and equipment control architecture criteria allowing newer modes of operation such as energy-saving operation of production equipment. As part of this charter, the FI roadmap is increasingly addressing the incorporation of Smart Manufacturing (SM) tenets for microelectronic device production and its supply chain. While the potential of "smarter" semiconductor manufacturing realized through the adoption and optimization of the common SM tenets in microelectronics manufacturing and its supply chain has at least partially been realized, there are certain obstacles, namely security and data sharing concerns, that have prevented this industry from becoming the leading adopter and beneficially of the technologies offered by SM.

It is and continues to be the IRDS FI focus team's core mission to evaluate those SM-related challenges and come up with technology requirements needed for addressing the challenges as well as potential pathways to satisfy the technology requirements.

9. Acknowledgments

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Hybrid 2D/CMOS microchips becoming a reality

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It's accurate to say that silicon electronics are ubiquitous nowadays. From toasters to fans, electric brushes, fridges, and of course cameras, TV sets, phones, and computers have some microchip within them to deliver power, control engines or carry out computations that were unachievable, and almost unthinkable, merely a few decades ago. The importance of these microchips is being manifested in the current efforts by many countries in the semiconductor ecosystem to retain or gain some sovereignty in this geopolitical element of ever-increasing importance; the digitalization of society is one characteristic element of the XXI century.

Even though there are better-suited materials for electronics, with better carrier mobility or direct bandgaps, silicon still dominates thanks to its maturity, versatility, and cheapness. The transistor is the cornerstone on which all this progress rests. Moore's law, Dennard scaling, and ultimately Scale Length Theory, propelled the silicon technology forward as the backbone of modern electronics, pushing it to its very limits. All these developments expanded its application ranges from its early analog origins as an amplifier, with bipolar transistors, to modern logic powering data centers and AI applications with CMOS technology, which is probably the apex of silicon technology. Physically, from a manufacturing point of view, this has been achieved through miniaturization, with many different and very inventive solutions: channel strain engineering, high-K dielectrics, and channel body thinning, to name a few. There were many important advancements introduced in planar architectures, before jumping into alternative architectures such as fins, nanosheets, and nanoribbons. We are however reaching the fundamental physical limits of this approach, manifested in the so-called short channel effects, where it is clear that a paradigm change is needed if we want to keep boosting performance at the transistor level.

Now, 2D materials are entering the scene. The advent of graphene and other atomically thin materials was a lucky strike when electronics needed it the most. This new class of materials presents ultrathin bodies, with excellent electrostatic control, without showing any mobility degradation when aggressive channel scaling is introduced; furthermore, ultrapure graphene devices show mobilities exceeding that of Si and III-V materials by many orders of magnitude. Graphene was precisely the first one to be isolated, sparking interest in the field. Later, a myriad of different materials were established through extensive research, such as hexagonal boron nitride (h-BN) and transition metal dichalcogenides (TMDs). Moreover, these new materials have complementary properties such as insulating, semiconducting, and metallic behaviors, which allow them to mimic conventional electronic design. However, the two-dimensional nature of these materials enables exploiting many different exotic effects, such as multiexciton states, valley polarizations, and superconductivity (among others) which could give rise to potential new devices in the future, expanding the range of capabilities of electronics.

The first studies on 2D-layered materials for electronics produced the material by mechanical exfoliation of bulk crystals using scotch tape. The flakes produced by this method have uncontrollable lengths of a few to hundreds of micrometers, and variable thicknesses of a few nanometers [1]. However, the ease and cheapness of this method allowed 2D materials research to be somehow democratized. Then, the 2D-layered flakes were stuck onto a small substrate made of SiO_2/Si or Al_2O_3/Si, and electrodes were patterned using electron beam lithography to form the devices. Using this method, transistors, capacitors, barristers, and memristors (among others) were created, and breaking performance were reported. That includes, for example, transistors with 2D semiconducting channels that exhibit current on/off ratios order of 10^8, high charge carrier mobility of 700 cm^2/Vs, and low subthreshold swing of 74 mV/decade [2]. However, mechanical exfoliation cannot be used to produce 2D layered materials at the wafer level, and hence all those studies lack relevancy for the industry. Nevertheless, they produced valuable knowledge that allows an understanding of the potential and limitations of the 2D materials.

In the following years, different methods to produce synthetic 2D layered materials were developed. Among them, liquid phase exfoliation (LPE) and chemical vapor deposition (CVD) attracted a lot of attention due to their high throughput, as they were able to coat 300 mm wafers. The first method (LPE) produces a solution containing a high density of 2D layered flakes, which can be deposited on any wafer easily using different methods like spin coating (among others) [3]. This results in thin films with thicknesses from tens to hundreds of nanometers formed by a mesh of 2D layered flakes. Although the junctions between the different 2D-layered flakes contain defective bonds and impurities that degrade performance, the LPE method can be used to fabricate large devices on arbitrary substrates, and it is ideally suited for the production of large-area circuits and sensors for all kinds of objects in the Internet of Things. Some studies reported the construction of transistors and logic gates [4], but their size was too large (hundreds of micrometers). No study has

ever reported the fabrication of multiple nanosized electronic devices via LPE, and it is expected that the large inhomogeneities within the 2D materials film would lead to a low yield, large variability, and poor reliability (because the atoms in such film are easy to move when an electrical field is applied).

More interestingly, the scientific community and more importantly, the industry have been able to synthesize continuous 2D layered materials at wafer-scale using chemical vapor deposition (CVD). Using this approach, the thickness of the 2D material can be controlled much more accurately, and the density of native defects (such as lattice distortions, missing bonds, strained bonds, impurities, thickness fluctuations, surface roughness, wrinkles, and cracks) is also much lower [5]. The main drawback of this method is that it requires high temperatures above 800 °C, which impedes direct growth on pre-processed silicon microchips. For this reason, some efforts are focused on synthesizing 2D semiconducting materials on empty or blank wafers and employing them as a channel in transistors, building the entire chip on them—in a standard silicon microchip technology, deposition of the semiconducting Si is also the first step. IBM used this approach in 2011 to fabricate a sheet of monolayer graphene on a SiC wafer (at 1400 °C) and then built a radiofrequency mixer containing one graphene transistor and two inductors [6]. However, the capabilities of such types of small circuits are very limited, and the topography of the SiC makes it difficult to obtain low device performance variations.

There is however a second approach, in which the graphene films are grown in a substrate material and then transferred onto a different, target wafer. This transfer approach is much more versatile due to the decoupling of the growth substrate and the target wafer, which enables the integration of these materials at the back-end-of-line (BEOL) and its monolithic integration with silicon circuitry. In 2014, IBM (again) proposed the integration of 2D materials in silicon samples containing pre-patterned circuitry [7]. Using this approach, the 2D material is used only for the required operation, and the rest of the operations can be carried out according to the well-optimized traditional silicon technology. The circuit presented contained four inductors, two resistors, two capacitors, and three transistors (with a monolayer graphene channel). All the elements were patterned but the transistors were left with source and drain contacts exposed at the last metallization layer and without channel. Then, the graphene was synthesized by CVD method on a Cu substrate at 1000 °C and transferred on the pre-patterned silicon wafer using a room temperature process. Finally, the graphene film was patterned, filling only the required channel area between the source and drain. The resulting circuit exhibited a high cutoff frequency of ~16 GHz, but far from ideal estimations for standalone graphene transistors (~100 nm at 240 nm gate length), which indicates that further optimization of processing parameters was needed, and the size of the transistors was large (channel size of 10.8 μm^2), which still requires miniaturization efforts.

The very relevant work by Goosens et al. [8] at Instituto Ciencias Fotónicas de Cataluña (ICFO) used a similar approach when monolayer graphene was transferred on silicon samples containing CMOS read-out circuits and constructed an array of 388 × 288 image sensors sensitive to light wavelengths between 300 and 2,000 nm. The graphene played the role of the conductive path and covered an area of ~105 μm^2 in each pixel. The authors estimated that the yield was 99.8% by measuring if the resistance was low (correct) or high (failure). The reason for such success was that in such large areas, the presence of local defects in the graphene does not produce an open circuit, which opens up the way for certain applications in which the structures don't need to be aggressively scaled down.

The 2D Experimental Pilot line [9], a project consortium from the European Commission that involves several top European institutions, is trying to automatize the production of wafers containing 2D materials. They offer multi-project wafer tape-outs which the customers can fabricate at least once per year at prices affordable to academics and start-ups. While the consortium is strongly working on the integration of other 2D materials such as TMDs, with semiconducting properties that enable logic applications, the project currently offers only circuits containing monolayer graphene, which limits the types of circuits that can be fabricated, and almost impedes the use of 2D materials for data management.

In 2023, a breaking study published in *Nature* presented the fabrication of the first hybrid 2D/CMOS microchips for high-integration-density data storage and computation [10]. The group led by Prof. Mario Lanza at the King Abdullah University of Science and Technology (KAUST) integrated h-BN at the BEOL of a silicon microchip containing CMOS transistors of the 180 nm node. The h-BN had a thickness of ~18 layers, each of them made of B and N atoms with in-plane covalent bonding and separated from each other by a 0.33 nm van der Waals gap, leading to a total thickness of ~6 nm. The CMOS circuit was designed using Cadence software and fabricated on a 200 mm wafer in an industrial foundry. However, the wafer was terminated after the 4th metallization step and left without passivation. Hence, the vias coming from the CMOS transistors were exposed to the atmosphere. The wafer arrived at KAUST laboratories with a native oxide, which was removed via wet etching to expose the metallic vias before transferring the ~18-layer-thick h-BN on top. Finally, top Au/Ti electrodes and interconnections were created using photolithography, electron beam evaporation, and lift-off.

The h-BN stack was therefore sandwiched between two metals, the W via coming from the transistors and the top Au/Ti electrodes, forming arrays of one-transistor-one-memristor (1T1M) cells (see Figure 1). The size of the

Au/Ti/h-BN/W memristor was only 0.053 μm², which was determined by the diameter of the vertical W via (~260 nm). In terms of performance, the authors demonstrated nonvolatile bipolar resistive switching for millions of cycles, and the yield was above 80%. The size and endurance of these devices were like that of memristors integrated with commercial products, such as nonvolatile memories [11–13], with the added advantage of a higher controllability of the on/off resistance window and the possibility of inducing threshold-type resistive switching (useful for the implementation of selectors and electronic neurons). One of the clues of this study was the use of multilayer 2D material, which is much stronger than monolayer from a mechanical point of view and does not

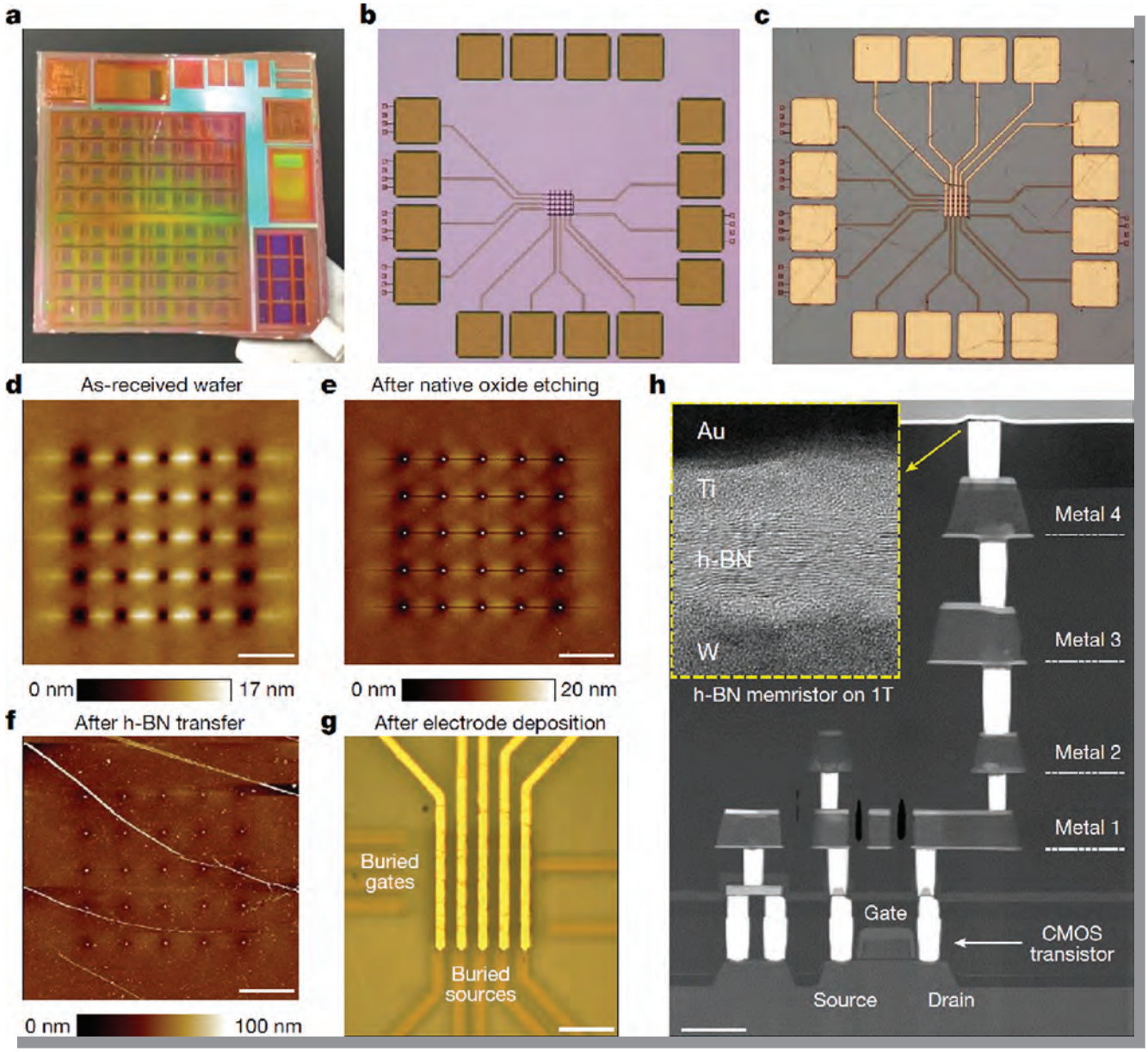

***Figure 1. Fabrication of hybrid 2D/CMOS memristive microchips. a**, Photograph of the 2 cm × 2 cm microchips containing the CMOS circuitry. **b-c**, Optical microscope images of a part of the microchip containing a 5 × 5 crossbar array of 1T1M cells, as received and after fabrication (respectively). The size of the squared pads is 50 μm × 50 μm. **d-f**, Topographic maps collected with atomic force microscopy of the vias in the 5 × 5 crossbar arrays on the wafers as-received, after native oxide etching, and after the transfer of the h-BN sheet (respectively). **g**, Optical microscope image of a finished 5 × 5 crossbar array of 1T1M, i.e., after h-BN transfer and top electrodes deposition. **h**, High-angle annular dark-field cross-sectional scanning transmission electron microscope image of a 1T1M cell in the crossbar array. The inset, which is 20 nm × 16 nm, shows a cross-sectional transmission electron microscopy image of the Au/Ti/h-BN/W memristor on the via; the correct layered structure of h-BN can be seen. Reproduced with permission from reference [10], copyright Springer-Nature 2023.*

crack so easily during transfer [5]. The 1T1M structure is the basic cell for data storage and computation in memristive circuits, and it can be used as nonvolatile memory, for in-memory computation, or as electronic synapse in crossbar arrays for vector-matrix multiplication (which is a key operation in artificial neural networks).

It is worth noting that transistors with channels made of 2D materials have been fabricated in the past and that, while large devices tend to work relatively well [14], channel lengths below 100 nm result in a prohibitive degradation of performance, variability, and yield [15]. On the contrary, memristors are devices in which the current flows across the device's weakest location, making it almost insensitive to process imperfections creating point defects [5, 10]. The size of these 2D-materials-based devices (0.053 μm^2) [10] is several orders of magnitude smaller than those previously reported on-chip using monolayer graphene (>10 μm^2) [6-8], and the technology readiness level is relatively high for this kind of materials.

Another breakthrough in hybrid 2D/CMOS integration is exemplified in the recent paper, also published in 2023, by Soikkeli et al. [17], in which monolayer graphene was also integrated at the BEOL of a CMOS wafer with read-out circuitry to create monolithic graphene biosensors, where the active element was a graphene resistor which was driven and read by the silicon circuitry sitting underneath it. This was the first example of monolithic integration of graphene for biosensing applications. In this case, the 200 mm analog CMOS wafers were sourced from a commercial foundry, fabricated with a 350 nm node. The read-out circuit consisted of 64 tiles, each with 64 individual devices, thus totaling over 4000 readouts. Each device could be operated with a two-probe or four-probe configuration, which allowed for Kelvin-type resistance measurements.

Graphene was then transferred on top of the CMOS wafers, which included up to 4 layers of metallization. Standard semiconductor techniques such as lithography, etching, and deposition were used to pattern, contact, and metalize the graphene devices. In each chip, there were 512 graphene transistors, which showed excellent resistance uniformity, with standard deviations being in the 10–15% interval concerning the average resistance values. 5 full microchips, with 2560 devices, underwent testing, from which 2558 showed consistent resistance values. Despite the large area of the graphene channels (in the micron range) this high yield (99,9%) demonstrated the maturity of the growth, transfer, and processing techniques when it comes to graphene monolayers, and should encourage the development of similar techniques for other materials such as 2D semiconductors.

Future studies in this direction should try to synthesize the 2D material in large areas with high homogeneity using wafer-compatible setups with shower-head gas delivery technology [16] and get it transferred on the pre-processed silicon wafers using advanced setups such as wafer de-bonding [18].

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Upcoming Technical Meetings

The 2024 IEEE Symposium on VLSI Technology & Circuits to Showcase Leading Edge Papers Around the Theme: "Bridging the Digital & Physical Worlds with Efficiency & Intelligence"

HONOLULU, HI (13 December 2023) —For the last 44 years, the IEEE Symposium on VLSI Technology & Circuits has delivered a unique convergence of technology and circuits for the microelectronics industry. Merged into one Symposium since 2022 to maximize the synergy across both domains, the 2024 IEEE Symposium on VLSI Technology & Circuits will be organized around the theme: "Bridging the Digital & Physical Words with Efficiency & Intelligence." The five-day event will be fully in-person with live sessions at the Hilton Hawaiian Village, Honolulu, HI, on 16 – 20 June 2024, as well as on-demand access to technical sessions starting the following week. The Symposium will feature the latest VLSI technology developments, innovative circuit design, and the applications they enable, such as artificial intelligence, machine learning, IoT, wearable/implantable biomedical applications, big data, cloud/edge computing, virtual reality (VR)/augmented reality (AR), robotics, and autonomous vehicles.

The **IEEE Symposium on VLSI Technology & Circuits** papers will focus on technical innovation and advances in the following areas:

- Advanced CMOS Platforms, Interconnect & Backside Power Delivery Network (BSPDN) Technologies
- Advanced Packaging, Chiplet & Heterogeneous Integration Technologies Including 2.5D & 3D
- Analog and Mixed-Signal Circuits
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- Frequency Generation & Clocking Circuits
- Memory Technologies, Devices, Circuits & Architectures
- Power Management Devices & Circuits
- Processes & Materials for CMOS Scaling & New Devices
- Processors & SoCs
- Sensors, Imagers, IoT, MEMS, Display Circuits
- Wireless and RF Devices, Circuits & Systems

The Symposium will continue its reputation as the microelectronics industry's premier international conference integrating technology, circuits, and systems with a range and scope unlike any other conference. In addition to the technical presentations, the Symposium program will feature a demonstration session for outstanding papers, an evening panel discussion, joint focus sessions, and Short Courses on specific topics relevant to the Symposium theme.

Plenary Speakers

Four plenary presentations are scheduled for the Symposium program:

- "Sensing at the Edge" by Dr. Ahmad Bahai, CTO, Texas Instruments

- "Future of 5G/6G Technologies" by Dr. Maryam Rofougaran, CEO & Founder, Movandi Corporation
- "Photonics-Electronics Convergence Devices to Accelerate IOWN" by Hidehiro Tsukano, Senior VP of R&D, NTT Corporation
- "Mobility Evolution: Electrification & Automation" by Dr. Kazuoki Matsugatani, Senior Director, R&D Center, DENSO Corporation

Short Courses

Two Short Courses are scheduled for Monday, 17 June.

- Technology focused—"Advanced VLSI Technologies for Next Generation Computing" will cover topics that include transistor scaling, memory technology evolution, backside power delivery network (BSDPN), and advanced packaging.
- Circuits focused Short Course on "Heterogeneous Integration", will include topics on Heterogenous Integration for automotive ICs / Edge, power delivery solutions for heterogeneous integration, memory co-integration, EDA for heterogeneous integration, 3D Packaging, and Wafer-scale integration.

Evening Panel

A joint panel discussion for Technology & Circuits is scheduled for Tuesday, 18 June on the topic "Impact of Generative AI on the Semiconductor Industry—Technology, Circuits, & EDA".

Focus Sessions

A series of special focus sessions will be part of the Symposium technical program:

- Technology Focus Session—"Backside of Silicon: from Power Delivery to Signaling"
- Circuits Focus Session—"Oxide Semiconductor's Applications in BEOL"
- Four Joint Focus Sessions
  - "Memory-centric Computing for LLM"
  - "Thermal Management & Power Delivery in 3D Integration"
  - "Processors & Compute"
  - "Sensors"

Workshop Sessions

A full day of workshop sessions will focus on merging research with applications in areas that have not been covered in detail in the Symposium technical program and could serve as topics for future Symposium sessions. The workshop sessions will be held in person during the Symposium on Sunday, 16 June, and available as on-demand recorded content following the Symposium.

Workshop topics could include:

- Open-source design
- Chiplet ecosystem: Challenges & opportunities
- Generative AI design
- Interfacing chips with biology
- Novel Metals for Advanced Interconnects
- RF and Analog 3Di: Challenges
- Silicon Photonics
- Universal Chiplet Interconnect (UCIE)

Special events at the Symposium include career mentoring events for Women in Engineering and Young Professionals sponsored by the IEEE Electron Devices Society and the Solid-State Circuits Society, and a traditional Hawaiian Luau celebration.

Best Student Paper Awards for each track of the Symposium are chosen based on the quality of the papers and presentations. The recipients will receive a monetary award, travel cost support, and a certificate. For a paper to be reviewed for this award, the lead author and presenter of the paper must be enrolled as a full-time student at the time of submission and must indicate on the web submission form that the paper is a student paper.

Further Information and Official Call for Papers

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8th IEEE Electron Devices Technology and Manufacturing (EDTM) Conference

3–6 March 2024
Bengaluru, India

IEEE EDTM is one of the premier conferences presented and sponsored by the IEEE Electron Devices Society (EDS). It is a platform for researchers to share scientific breakthroughs and enrich insights on various topics in semiconductor technology. Traditionally, it has been hosted in places that are considered major Asian semiconductor hubs. Moving forward, the 8th edition of IEEE EDTM will be hosted for the very first time in India, another major player in semiconductor research and technology. Bengaluru promises to host an exciting and overwhelming edition of the conference on 3–6 March 2024 by having leaders in the field, from around the world, delivering talks on their scientific breakthroughs. Besides, for efficient conveyance of advanced research outcomes/concepts, the conference offers a comprehensive program with tutorials/short courses on fundamental topics on semiconductor processes, technologies, devices, and circuits.

Technical Program

IEEE EDTM presents a wide range of topics from materials, device technologies & modeling to reliability, manufacturing & packaging encompassed into a progressive technical program. Broadly, the following technical areas align with the conference agenda, seeking high-quality papers:

- Logic Devices (LD)
- Power and Energy Devices (PED)
- RF Devices and Circuits (RFDC)
- Device Technology Co-optimization (DTCO)
- Emerging Materials and Devices (EMD)
- Advanced Memory Technologies (AMT)
- Process, Tools, Yield, and Manufacturing (PTYM)
- Packaging and Heterogeneous Integration (PHI)
- Modeling and Simulation (MS)
- Device and Circuit Reliability (DCR)
- Photonics, Optoelectronics, Imaging, and Displays (POID)
- Sensors, Flexible and Bio-electronics (SFBE)
- MEMS/NEMS and Heterogeneously Integrated Devices (NEMS)
- Disruptive Technologies (DT)

Please, follow the conference website https://ewh.ieee.org/conf/edtm/2024 for the updates of the Conference technical program.

Publications

All submitted papers will be subject to IEEE guidelines and review process. Accepted and presented papers will appear in IEEE EDTM 2024 proceedings published in IEEE Xplore. EDTM 2024 offers an opportunity to publish with the prestigious IEEE Journal of Electron Devices Society (J-EDS). Authors of high-quality papers will be invited to publish in a special issue of the journal. Please follow the link to learn more about paper submission/presentation guidelines and process: https://ewh.ieee.org/conf/edtm/2024/paper-submission.php.

On behalf of the Steering, Executive, and Advisory Committees, we cordially invite you to take part in the 8th IEEE EDTM Conference.

Yogesh Singh Chauhan (General Chair)
Mayank Shrivastava (General Co-Chair)
Nihar Mohapatra (TPC Co-Chair)
Ansh (Publicity Co-Chair)

2024 IEEE International Memory Workshop (IMW)

The 16th International Memory Workshop (IMW) will be held at the Grand Walkerhill hotel in Seoul, South Korea, on 12–16 May 2024. The history of the IMW dates back to the NVSMW (Nonvolatile Semiconductor Memory Workshop) which began in 1976 and which merged with the ICMTD (International Conference on Memory Technology

and Design) in 2009 to become the IMW. The IMW is sponsored by the IEEE Electron Devices Society and meets annually in May. The workshop covers all types of memory technology, is focused on advancing innovation in memory technology, and is organized in a way that provides excellent professional development and networking opportunities for attendees.

The IMW is the premier international forum for both new and seasoned technologists having diverse technical backgrounds to share and learn about the latest developments in memory technology with the global community. The scope of the workshop content ranges from new memory concepts in early research to the technology drivers currently in volume production as well as emerging technologies in development. Topics include new device concepts, technology advancements, scaling and integration, circuit design and reliability, as well as emerging applications. Consistent with the increased importance of memory system architecture and integration, the workshop also includes increasing coverage of the systems in which memories are deployed and the co-evolution of memory technology along with memory systems and applications.

The IMW is the preeminent forum covering the latest developments, innovations, and evolving trends in the memory industry. Typical workshop attendance exceeds 200 attendees, and the technical program begins with a full day short course given by distinguished experts that provides an excellent professional development opportunity for both new and experienced technologists. The single-track technical program spans three days and also includes an evening poster session for informal technical discussion with authors as well as a panel discussion where experts discuss and debate a current hot topic. The workshop includes invited talks from industry and research leaders. Keynotes in the recent workshops were presented by Infineon, TechInsights, Samsung, Micron, GLOBALFOUNDRIES, Intel, Kioxia, ASML, Western Digital, IMEC, ST Micro and NXP. Tutorial and highlights in the recent workshops included TCAD and Modeling, DNA Memory, Ferroelectric Memories, Security Aspects of Memories, 3D Memories beyond Flash, New computing paradigms, 3D NAND, DRAM, Embedded memories, Emerging memories and innovation (PCM, RRAM, MRAM, FeRAM…) for storage-class memories, data centric architectures, tremendous growth of connected objects, and neuromorphic memory, quantum computing and in-memory computing. The technical program is organized to maximize networking opportunities and facilitate open information exchange among workshop contributors, committee members, and attendees. The program schedule includes ample time dedicated to social events including provided refreshment breaks, lunch breaks, and an evening banquet, and since 2022 event, IMW has introduced a new policy of casual clothing to further promote informal discussions between participants.

On behalf of the organizing committee, I cordially invite you to participate in the IMW 2024 to continue to participate in the advancement of innovation in the rapidly evolving memory industry. For additional information, including the call for papers, key dates, abstract submission instructions, registration information, and technical program details, please visit the IMW website for the latest updates: http://www.ewh.ieee.org/soc/eds/imw/. I look forward to seeing you in Seoul next May.

Thomas Mikolajick
2024 IMW Publicity Chair

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In Memory of Prof. Simon Min Sze

By Hiroshi Iwai, NYCU

Prof. Simon Min Sze, the author of a globally renowned textbook "Physics of Semiconductor Devices" and the inventor of floating gate non-volatile semiconductor memory, peacefully passed away, on November 6, 2023, in the United States. He was 87 years old, survived by his wife, one son, one daughter, and four grandchildren. Dr. Sze was a literal giant in the field of semiconductor devices, serving as both an esteemed educator and inventor.

Prof. Simon Min Sze

His Parents and Childhood

He was born on March 21, 1936, in Nanjing, China, with his ancestral home in Wujiang, Suzhou. His father, a mining expert who had studied in Paris, France, and worked in the metallurgical industry in Mainland China, moved his family to Taiwan in December 1948. This relocation occurred when he was appointed as the director of the Taiwan Gold and Copper Mining Bureau, as detailed in the Chinese language book "Min Sze and the Story of the Digital Era" authored by Li-Chuan Wang. Later, he taught in the Department of Mining and Metallurgical Engineering at the Provincial Taipei Institute of Technology (now National Taipei University of Technology) and continued to contribute to the development of Taiwan's metallurgical industry and the establishment of a Taiwanese steel enterprise.

Simon's mother was born in Jilin Province (Northeastern part of China) during the late Qing Dynasty. Her father served as the mayor of Tianjin, and her uncles held positions as governors of Zhejiang and Jiangsu provinces. She graduated from the Foreign Languages Department of Tsinghua University in 1933, a time when it was uncommon for girls to attend college. Simon's father's busy schedule often kept him away from home, but Simon's mother always accompanied him during his childhood studies. After completing his assignments, he would present them to his mother, who would help correct any mistakes or misunderstandings. During the war period between China and Japan, his family moved from Chongqing, Kunming, Tianjin, Beijing, and Shenyang, to Shanghai. The most important thing in Simon's mother's heart was the academic success of her two sons.

During his school years in Taiwan, Simon could be considered almost a genius. His exam scores were outstanding, consistently ranking among the top in the class. There seemed to be no test that could stump him. He frequently asked questions, especially those that teachers couldn't answer, and this penchant for questioning led some of his teachers to view him unfavorably. However, this was due to his excessive curiosity, and some teachers understood this and defended him.

University Period

In 1953, he graduated from Taiwan Jianguo High School. He initially considered following his father's path in metallurgy. However, his father recommended choosing another field of engineering due to the limited mineral deposits in Taiwan. Simon entered National Taiwan University and opted for a telecommunications course in electrical engineering because he excelled in mathematics and enjoyed it. His younger brother chose chemical engineering. Simon graduated from the university in 1957 with a bachelor's thesis titled "Oscillators with Capacitance and Inductance," supervised by Professor Ju-Xian Li.

Upon graduation, he applied for admission and scholarships to a couple of universities in the United States but was unsuccessful. However, he eventually obtained admission to the University of Washington in Seattle, where some of his friends and classmates were already enrolled. After completing his mandatory military service in Gangzhi and Hsinchu for 18 months, he left Taiwan for the United States to enroll at the University of Washington in 1959. There, he secured a research assistant position with Professor Wen-Ling Wu, a Chinese professor specializing in solid-state electronics, marking the beginning of his career as a semiconductor engineer. He obtained his MS degree in 1960 with a thesis entitled "Diffusion of Zinc and Tin in Indium Antimonide."

He applied to the Ph.D. programs at Harvard and Stanford Universities and received scholarships from both institutions. He ultimately chose Stanford University for his Ph.D. studies because the electrical engineering program was at Stanford and not at Harvard. In 1963, he earned his degree with a thesis titled "Hot Electrons in Thin Gold Films," supervised by Prof. John Louis Moll, who proposed silicon as the most important material for

semiconductors. Although Simon's thesis focused on hot electrons in metal, his experience with Prof. Moll significantly influenced his career as a silicon engineer.

Early Days at Bell Labs

According to "Oral History of Simon Sze," recorded on February 11, 2014, by the Computer History Museum, he received seven job offers at the Stanford graduation, including those from Bell Labs, IBM, HP, General Electric, Westinghouse, and others. Although Bell Labs proposed the lowest annual pay, i.e., twelve thousand US dollars, he chose Bell Labs because Prof. Moll recommended it as having the best research environment, and Simon was inclined towards research.

Simon's initial supervisor at Bell Labs in Murray Hill was Robert M. Ryder, later succeeded by George Smith. The group was tasked with studying high-speed transistors and developing new device concepts. When entering Bell Labs, Simon inquired about his responsibilities, to which his boss responded, "Anything to do with silicon. Anything." There were no specific assignments, allowing members to pursue projects of their choosing. He initially picked up the hot electron transistor for the research and then shifted his attention to Schottky barrier phenomena and devices. The members at Bell Labs were highly collaborative, and he successfully completed 20 research projects with his colleagues from 1963 to 1967.

The Invention of Floating Gate Non-Volatile Memory

The 20th project was accomplished with Dawon Kahng. Simon was having lunch with him talking about the possibility of replacing non-volatile magnetic core memories, with semiconductor devices. This was not part of their research assignment, and even some colleagues believed that charge-stored semiconductor non-volatile memory was impossible due to the recombination time of electrons and holes, which was only on the order of milliseconds. One day, during lunch at the Murray Hill Cafeteria, feeling hungry, Dawon ordered a four-layered cheesecake or chocolate cake for dessert. While looking at the cake, they conceived the idea of incorporating a metal layer (later referred to as the "floating gate") in the gate oxide situated between the top aluminum metal gate (referred to as the "control gate") electrode and the channel of a conventional silicon MOS field-effect transistor (MOSFET). Later, Simon frequently recounted this tale to us. They conducted a theoretical analysis and devised the structure, initially contemplating the use of tungsten for the floating gate electrode. Marty Lepselter, an expert in metallurgy, recommended the utilization of zirconium due to its ease in forming ZrO_2 as the gate oxide between the Zr floating gate electrode and the top aluminum gate electrode. The devices were then fabricated and subjected to measurements by Simon's technicians, confirming successful charge storage at the first fabrication. However, the longest retention time among the ten to twenty samples was only one hour. This marked the advent of the first semiconductor non-volatile memory, which later evolved into the globally popular flash memory.

Dawon and Simon wrote a paper and Simon showed it to his boss who unfortunately deemed it "absolutely useless" asking Simon not to submit it to IEEE Transactions on Electron Devices. Consequently, they had no choice but to submit it to the Bell System Technical Journal on May 16, 1967, and the paper was published on July 1, 1967. The boss passed away around 1990, unaware of the rise of the floating gate nonvolatile memories for various applications. Simon acknowledged in the oral record that even he had not fully recognized the significant importance of floating gate nonvolatile memory until its widespread use in the early 1990s, because the work in the group had been focused on basic research rather than practical application. Nonetheless, the boss was a valuable mentor for Simon, as recounted in Simon's oral history. He offered kind guidance and strong support for his research as well as the choice of freedom. Additionally, he provided significant assistance in writing the book.

Writing the Textbook, "Physics of Semiconductor Devices"

Simon also revealed the story of how he came to write the world-famous textbook "Physics of Semiconductor Devices." The research at Bell Labs was too easy for him, thanks to the support of excellent facilities, highly cooperative research partners, outstanding technical assistants, typists for writing assistance, and more. This environment enabled him to complete numerous papers in a short period. Seeking more challenging endeavors, he requested his boss to assign him something highly difficult. In response, his boss drafted him to teach an in-house course in 1967. He prepared class notes covering almost all types of important semiconductor devices, a task unprecedented among other authors. He immersed himself in reading thousands of technical papers, investing a total of 3,000 hours (approximately 10 hours a day). In this exhaustive process, he meticulously synthesized and explained the structures and operations of semiconductor devices in a textbook that was not only easily understandable for beginners but also detailed and accurate. This accomplishment attests to his exceptional intellect and can be described as nothing short of a genius-level feat. The book titled "Physics of Semiconductor Devices" was published by John Wiley & Sons, Inc. in four editions (1969, 1981, 2007, and 2021), translated into six languages, and distributed worldwide, with over three million copies. As of November 2023, it has garnered over 68,000 citations, making it one of the most cited works in contemporary engineering and applied science publications. The book

is referred to as a bible among semiconductor device engineers for consultation.

As a result of his quest for papers related to the textbook, he curated and published a collection of 141 historically significant archival papers on semiconductor device technology spanning over 100 years. This compilation, titled "Semiconductor Devices: Pioneering Papers," was released in 1991 by World Scientific Publishing Co. The value of this collection extends beyond providing insight into the concise history of semiconductor device technology development. It also allows access to some old papers, including the technical memorandum documenting the initial operation of the MOSFET by D. Kahng, which are otherwise not easy to obtain.

Research Activities as a Supervisor at Bell Labs in the 1970s and 80s

Simon was promoted to the position of a group supervisor, overseeing up to 10 members, in 1969 after returning from a one-year sabbatical in Taiwan, as later described. According to him, his role was facilitating members to pursue their preferences by securing funds and equipment from Simon's superior. From the late 1960s to the mid-1980s, numerous papers, coauthored by several members including him, were published. These papers covered topics such as the microwave oscillation of IMPATT and BARITT diodes, MOSFET miniaturization, and some review papers. In 1979, they released a comprehensive guide for MOSFET miniaturization, and in 1981, they published a paper on MOSFETs with a channel length of 0.15 μm, fabricated using E-beam lithography. These MOSFETs were the smallest at that time.

During this period, he served as an associate editor for Solid State Electronics (1980 to 1984). Subsequently, he served as an associate editor (1986 to 1990) and the editor-in-chief of IEEE Electron Device Letters (1986 to 1990).

Teaching and Consulting on the Establishment of the LSI Industry in Taiwan During his Bell Labs Period

While Simon was working at Bell Labs, he took leave five times to spend time in Taiwan for teaching. Through these visits, he cultivated a substantial pool of talent essential for the development of Taiwan's semiconductor industries. His students have actively contributed to the promotion of Taiwan's industrial development, serving as great leaders in both corporate and academic spheres.

Among the five visits, the second visit took place at National Chiao Tung University (NCTU, now National Yang Ming Chiao Tung University (NYCU)) as Chao-Yung Tung chair professor from 1968 to 1969, after he finished writing the book and submitted the manuscript. During this time, he served as the chief advisor to the first-ever engineering Ph.D. program in Taiwan. The first Ph.D. graduate was Chun-Yen Chang, who later became the president of NCTU in 1998. Additionally, Simon established Taiwan's pioneer semiconductor company, "Huanyu Electronics," during this timeframe.

From 1974 to 1977, Simon returned to Taiwan for the third time to teach at National Taiwan University as a special chair professor for 3 years. During that period, he provided valuable advice to Yun-Suan Sun, Minister of Economic Affairs at that time, in deciding to introduce RCA CMOS technology to Taiwan. Simon served as a member of the Electronic Technology Advisory Committee at the Industrial Technology Research Institute (ITRI) from 1974 to 1977. Additionally, he worked as a consultant to the National Science Council (NSC) from 1974 to 1978 and was a member of the Liaison Working Group on the Development of the Integrated Circuit Program at the Ministry of Economic Affairs in 1976. The working group suggested to Minister Yun-Suan Sun, "Taiwan lacks underground resources, minerals are scarce, and the primary resource with significant development potential is human intellect. Semiconductors represent the forefront of high technology, with promising prospects. Therefore, it is strongly recommended that Taiwan concentrate on cultivating the IC industry."

Early Retirement from Bell Labs in 1989 to Join NCTU

Since the mid-1980s, Bell Labs gradually shifted its direction towards an outcome-driven strategy aligned with the company's objectives, leading to Simon's dissatisfaction. Additionally, with the implementation of an early retirement program at Bell Labs, he contemplated being the program's inaugural participant, retiring before the age of 55. He then spoke with his first Ph.D. student, Chun-Yen Chang, who served as the director of R&D at NCTU, expressing his willingness to come over and teach, and Chang extended an invitation. Simon retired from Bell Labs in 1989 and joined NCTU as a distinguished chair professor in 1990.

In the beginning, he taught two courses and served as the director of the Microelectronics and Information Systems Research Center at NCTU from 1990 to 1996. Additionally, he served as the director of the National Nano Device Laboratories (NDL) at NSC located on the NCTU campus from 1998 to 2004, contributing to the advancement of semiconductor device research not only for NCTU but also for the entire Taiwan. During his managing the center and laboratories, he collaborated with fellow professors to co-supervise students in research dedicated to resistive random-access memories (RRAMs), thin-film transistors (TFTs), and low-dielectric constant insulator (low-k) materials in the 1990s and the early 2000s.

In 2006, he was awarded the honorary chair professorship at NCTU, and in 2010, he was appointed as a life chair professor there.

Passion for Teaching Students Worldwide and Writing Textbooks

Simon enjoyed traveling to foreign countries to deliver lectures to students. He served as a visiting professor at various institutions, including Cambridge University (King's College), Delft University, Stanford University (as a consultant professor), the Swiss Federal Institute of Technology, and the Tokyo Institute of Technology (from 2009 to 2014), as well as Taiwan's institutions such as National Taiwan University, Sun Yat-sen University, National Taiwan University of Science and Technology.

He was instrumental in establishing the engineering Ph.D. course in Mainland China as well as in Taiwan. He promoted semiconductor device education in Mainland China by frequently visiting for 3-week courses. He served as an honorary or a visiting professor in many Mainland Chinese universities. such as Peking University, Tsinghua University, Shanghai Jiao Tong University, Fudan University, Shandong University, Soochow University, Anhui University, Xi'an Jiaotong University, Jilin University, Harbin Institute of Technology, Beijing Jiao Tong University and also Hong Kong University of Science and Technology. After stepping down as the director of the NDL in 2004, he entered a sort of semi-retire phase, gaining the freedom to do whatever he liked to do. According to his oral history (and based on his daily conversations with us during that period), he used to pick out a place he and his wife liked to go, find the university nearby, write a letter to the president of that university, and say, "I am coming over with free of charge with the condition of being provided with a business-class air ticket and accommodation." Following that, he conducted a three-week lecture course at the university.

He also launched the "Semiconductor Physics and Components for the Internet" course (Massive Open Online Course: MOOC) to nurture more engineering and technology talents for the future "smart society."

He maintained a passion for writing books on semiconductor education and authored, coauthored, or edited a total of 16 books. In 2021, he published the fourth edition of "Physics of Semiconductor Devices." Almost all semiconductor device engineers can be considered his students, having learned about devices from his books.

A Gentleman Who Enjoyed His Life

Simon was truly a gentleman—kind to everyone, calm, and modest. We never saw him become emotional. Simon possessed a profound understanding of history and culture, enjoying the exploration of historical and cultural landmarks worldwide and reading books to examine ancient culture and history. He was also a person with excellent self-control, understanding contentment, and paying particular attention to his health. He did not stay up late and adhered to the habit of going to bed and waking up early. During the late afternoon, he used to put on sportswear and go for a walk. According to him, his family members lived long lives, with both his parents and uncles reaching beyond 90 years. Consequently, he mentioned that he expects to live until around 100 years old.

He enjoyed listening to the radio and watching movies in his youth. Later on, he relished cable TV during his 'semi-retiring' period when he visited NCTU for a few months every spring and autumn. Additionally, he was a highly skilled harmonica player. During an invited talk at a conference, he treated the audience to a melody of "Mary Had a Little Lamb" played on his harmonica, which was recorded in a small-sized non-volatile semiconductor memory. This marked the audience's first experience of listening to music stored in semiconductor memory for most of them. Notably, "Mary Had a Little Lamb" was the first audio recorded by Thomas Edison on his newly invented phonograph in 1877. He mentioned that, at that time, only several minutes of music could be stored in semiconductor memory, but he anticipated that in the future, an entire symphony or even entire newspapers published in a year could be stored in such memory.

Honors and Awards He Received

He received many honors such as fellow of academic societies, honorable professor titles, and prizes and awards. He is a recipient of the IEEE EDS J. J. Ebers Award (1991) and the Future Science Prize China (2021), a Life Fellow of IEEE (2002), a Fellow of JSAP Japan (2014), an IEEE EDS Celebrated member (2017), an ITRI Laureate Taiwan (2014), an Academician of the Academia Sinica Taiwan (1994), a member of National Academy of Engineering United States (1995), foreign Member of Chinese Academy of Engineering China (1998), a keynote speaker at IEDM United States (1994), and so on.

He took great pride in the development of the world's first floating gate-type semiconductor non-volatile memory. He was regarded as a prominent candidate for the Nobel Prize, and he was aware of this himself. Unfortunately, he passed away without receiving the Nobel Prize, which is a great loss. Nevertheless, we believe that he led a fulfilling and satisfying life, marked by significant contributions to the world through important inventions and educational efforts. He also enjoyed culture, history, music, and world travel in his daily life.

In Memory of Judy Hoyt (1958–2023)

Judy Hoyt, a pioneer in semiconductor research, passed away on August 6, 2023.

Judy Hoyt (1958–2023)

Professor Judy Hoyt is known well for her groundbreaking work with strained silicon semiconductor materials, work which has contributed greatly to the scaling of integrated circuits. Her most recognized contribution was the first demonstration of the incorporation of lattice strain as a means to enhance performance in scaled silicon devices, a key concept behind the continuation of Moore's Law roadmap for the last twenty years. This contribution has impacted virtually every high-performance chip manufactured today, leading to the growth of both the $500-billion-dollar semiconductor industry and the multi-trillion-dollar electronics market.

Judy's contributions earned her the 2011 IEEE Andrew S. Grove Award (together with Eugene Fitzgerald) and the 2018 University Research Award by the Semiconductor Industry Association in collaboration with the Semiconductor Research Corporation.

Born on Jan. 5, 1958, Judy was a native of Garden City in Long Island, NY. She was not only a talented musician (simultaneously leading her high school band and a swing jazz band) but also a distinguished student, who earned the rank of valedictorian before going on to earn her undergraduate degree in Physics and Applied Mathematics at UC Berkeley in 1980, and her MS and PhD degrees in Applied Physics at Stanford University in 1983 and 1987, respectively.

After graduation, she stayed at Stanford first as Research Associate in Prof. James Gibbons's group and then as Senior Research Associate before joining the faculty of the MIT Department of Electrical Engineering and Computer Science (EEES) as Professor in 2000. Additionally, she served as an Associate Director within the Microsystems Technology Laboratories (MTL) at MIT from 2005–2018. In addition to her many contributions to MTL and its community, Judy was an early proponent of the new nanotechnology facility at MIT, MIT.nano. A facility that benefited tremendously from Judy's vision for state-of-the-art university cleanrooms. Throughout her academic career, Judy was a dedicated teacher and mentor to her students at both Stanford and MIT, many of whom went on to distinguished careers in the semiconductor industry.

Throughout her career, Judy has served the EDS and IEEE society greatly. After several years of service in the International Electron Device Meeting (IEDM) committees, she rose to become the first woman Chair of the conference in 2001. Many in the organization of the IEDM that year credit Judy's leadership for "saving" the 2001 IEDM during the tumultuous post-9/11 months.

Outside of her professional activities, Judy was an avid cyclist who loved the outdoors and animals; her lifelong love of music sustained her as well. Those of us who knew Judy will remember her as a gentle soul and a caring friend whose puckish humor and unassuming demeanor hid a stern wisdom, unimpeachable sense of responsibility, and passionate loyalty to her students and her family.

Dimitri Antoniadis
Massachusetts Institute of Technology

Board of Governors Meeting—December 2023

MK Radhakrishnan
IEEE EDS Secretary

EDS Board of Governors meeting in December 2023 was organized at Hilton San Francisco Union Square hotel on December 10, 2023. EDS President, Ravi Todi welcomed the attendees and presented the major highlights including the overall summary of the activities in 2023 and the successful culmination of the year with the technical activities. 75th anniversary of Invention of Transistor was celebrated by Chapters in all Regions. A commemorative anniversary book with special articles by experts on various developments and stages of device development has been prepared and being released. Highlights of EDS publications include the initiation of number of new journals. All the EDS journals are successful.

Bin Zhao, President-Elect presented the ExCom meetings summary. Strategy to strengthen the Society by various initiatives. As the semiconductor device landscape changes EDS has certain challenges, especially in the technical activities and maintaining the revenue from publications. Eventhough the rankings of EDS publications remain among IEEE publications and the downloads

increase, the overall revenue reduces. As the scope of EDS technical activities widen three groups are planned for technical activities management. An EDS speciality conference is being planned.

EDS Secretary, MK Radhakrishnan presented the Secretary's report and Newsletter report. Minutes of 2023 mid-year BoG meeting was submitted for approval. EDS Newsletter report was presented on behalf of the EiC Daniel Tomaszewski. The Regional Editor appointments are being rearranged based on regional needs. Associate EiC, Manoj Saxena is stepping down with effect from Jan 1, 2024. The articles such as Tech Briefs, YP, WIE articles for on-coming issues are planned.

EDS Treasurer, Roger Booth presented the financial status reporting a very healthy finance in 2023. The expense reduction in the previous year due to pandemic helped to attain this state where as the revenue from conferences have also reduced, but not at the same level. 50% of the operating margin can be utilized for new initiatives. The budget for 2024 has been presented.

Navakanta Bhat, VP of Education informed the successful organization of summer schools in Kenya, Jaffna, Nepal and Publa. Very successful webinars were organized every two weeks in the whole year, especially thematic webinars partnering with different education institutions and EDS TCs. Outreach program Education achievement and Certification program are progressing as planned.

Arokia Nathan, VP Publications &Products informed that all EDS journals (TED, EDL and JEDS) have an overall improvement in the Impact Factor. Sayeef Salahuddin, EiC of EDL presented the EDL status as well as strategy for progress. Patrick Fay, EiC of TED presented the journals publication details as well as editorial turn around time details. For JEDS, a new EiC takes charge in place of Enrico Sangiorgi. The acceptance rate for all three journals remains more or less the same as in the previous year.

Kazunari Izhimaru, VP of Meetings informed that most of the conferences were in person mode this year where as only a few were in hybrid format. All the EDS financially sponsored conferences, IEDM, EDTM and PVSC are now held as a full event with a good participation. Yogesh Chauhan and Mayank Srivastava presented the EDTM 2024 status, which shows higher number of paper submissions. Yang Chai presented the preparations for EDTM 2025.

Murty Polavarapu, VP Regions and Chapters, reported that EDS Chapters, especially student chapters are growing in Regions 9 and 10. Meetings organized by most of the Chapters in 2023 have been reported through L31. Regional Chapters meetings were held in Region 8, Region 9 and Regions 1–7. The DL programs are more in person activity, where as virtual DLs are also continuing. Chapter subsidy requests as well as MQ requests are being processed.

Membership development report was presented by VP for Membership, Merylne de Souza. Currently EDS has more than 13000 members worldwide with an increase in student membership and the growth mostly focused in Regions 10 and 9. Undergraduate student member strength is mostly concentrated in Region10. The programs such as WiE events, activities related to 75th year of transistor invention, online webinars and MQs contributed to. the member growth.

Doug Verret, VP Strategic Directions, presented the EDS strategy outline and reviewed the KPI status. KPIs for various activities for the next year and 2025 were highlighted. Strategic plan fanout was reviewed and a report outlining the potential steps for the Strategic directions committee was presented.

John Dallessase, VP for Technical Committees reported that there are 16 TCs with about 170 TC members. Most of the Committees are healthy. TC members provide healthy support for Webinars and special issues. As the scope of EDS technical activities widen three groups for TA—traditional, Inter-disciplinary and New initiatives—are planned. A nomination process for the TC members/Chair recruitment is being established.

Camilo Velez reported the activities of Communications Committee. EDS social media followers are now more than the total member strength. Communicating strategy plan for coming years was presented. EDS visibility in Social Media platforms are very good. Especially in LinkedIn. YP Committee Chair, Mario Aleman, presented Young Professionals committee report. A number of activities were reported. WiEDS report was presented by its Chair Susthitha Menon. A number activities have been reported for this new Committee. Various WiEDS activities have promoted the growth of women members in the society.

Dina Troyoso, 2023 IEDM General Chair presented the latest status of the IEDM 2023. The Tutorials and Short courses had good participation. The conference registration is near to 1900 and it is expected to reach 2000.

Fernando Guarin presented the details of newly elected Fellows from EDS. 27 EDS members are elevated to Fellow grade out of which 10 were evaluated by the Society. The success rate is comparable to that previous years. Cor Clayes presented the Humanitarian activities report. EDS office and Staff report was presented by Patrick McCarren.

Ravi Todi thanked all the attendees of the meeting for their participation and support throughout the year, as well as EDS Staff for their dedicated effort to make the Society one of the vibrant among IEEE Societies. The meeting was adjourned at 5.00 pm.

MK Radhakrishnan
IEEE EDS Secretary

Message from EDS Newsletter Editor-in-Chief

Daniel Tomaszewski
EDS Newsletter
Editor-in-Chief

Dear Readers, Members of the IEEE Electron Devices Society,

Welcome to the IEEE EDS Newsletter issue of January 2024. Let me briefly introduce to you the contents of the issue.

We share with you an extensive obituary of Prof. Simon Min Sze who passed away on 6 November 2023. It is a great loss for the semiconductor engineering community. Prof. Sze's works had a huge impact on different areas of electron device physics, technology, and education. I am very grateful to Prof. Hiroshi Iwai for the article. We also would like to commemorate Prof. Judy Hoyt who passed away on 6 August 2023. Her contribution to the technology of strained silicon was invaluable. Prof. Dimitri Antoniadis wrote the text. Thanks a lot.

Prof. James Hwang has been selected as the 2023 EDS Lester Eastman Award winner. Congratulations! Prof. Hwang kindly agreed to write an article about the life and work of Lester Eastman. I strongly recommend reading this article which is included in the Awards Section. Thanks a lot, Prof. Hwang.

Also in the Awards Section, please find information about a podcast with Prof. Mukta Farooq, IEEE EDS J.J. Ebers Award Winner. Congratulations, Prof. Farooq. We also would like to congratulate all the Awardees mentioned in the concise note "2024 IEEE Technical Field Awards Winners".

The Technical Briefs Section summarizes three conferences held in 2023: the 69th IEEE International Electron Devices Meeting, the 2023 IEEE International Integrated Reliability Workshop, and the 5th IEEE International Flexible Electronics Technology Conference. I hope that you will find the texts informative and they will be an inspiration for your works.

In addition, this Section contains the next installment of the series of articles reporting the works of International Focus Teams (IFTs) of the International Roadmap for Devices and Systems (IRDS). The article concerns the Factory Integration Roadmap. We are looking forward to the next parts of the IRDS-related series. The Section contains also the article about Hybrid 2D/CMOS microchips technology. Presenting the article was an initiative of Prof. Mario Lanza. I think that this article corresponds to some degree with the 2023 IEDM report because the integration issues were intensively explored there.

The Upcoming Technical Meetings Section announces and invites you to participate in three important EDS-sponsored conferences: the 2024 IEEE Symposium on VLSI Technology & Circuits, the 8th IEEE Electron Devices Technology and Manufacturing Conference, and the 2024 IEEE International Memory Workshop.

Coming back to the Society News, I strongly recommend reading a report by M K Radhakrishnan, the EDS BoG Secretary, about the Board of Governors Meeting that was held in the time-frame of 2023 IEDM.

This Newsletter issue also brings, as usual, Regional News. I believe that this part is underrepresented. It is visible in this issue where a majority of the content belongs to other sections, despite the Women in EDS, and Young Professional Sections being empty. We also finished issuing a series of articles celebrating the 75th Anniversary of Transistor. Works on the missing three sections were coordinated in the last three years by Manoj Saxena. However, Manoj decided to step down from the position of Associate EiC due to his professional duties. I deeply appreciate his excellent work and great contribution to the Newsletter. Thanks a lot and I wish you a lot of success, Manoj.

Dear Readers, if you have any suggestions or comments regarding the Newsletter contents, please do not hesitate to contact us. We will be very glad to receive your feedback. Interesting views will be presented with the authors' consent, along with our replies in the Letters to Editors section. Finally, I would like to wish you a prosperous and healthy New Year 2024.

Sincerely,

Daniel Tomaszewski

Lester Eastman and the MMIC Technology

James C. M. Hwang

The late Prof. Lester (Les) F. Eastman of Cornell University retired in 2011 but remained in Ithaca, New York until he passed away a decade ago. His career accomplishments are well known. For example, in six decades of his academic career, he graduated 125 Ph.D. students. There are good articles about him on Wikipedia and the Memorial Tributes of the National Academy of Engineering, although they miss some key points. For example, they cite his APS Fellow Award in 2001 but fail to mention his IEEE Fellow Award in 1969, at the age of around 40, shortly after being awarded tenure at Cornell. Before that and later, when he was an assistant professor at Cornell, he started a conference series on high-speed semiconductor devices and circuits and presented himself as a leader in the field. (The conference was renamed in his honor decades later.) Few people would have the guts to pull such a stunt in their careers so early.

Late in Les' life, he shared with his children the research accomplishments that meant the most to him during his long career. His son Daniel recalls speaking with Les at length about what reflected his deep patriotism and love for his country. "In the late 1960s, Dad was asked to assist the government in developing a jamming technology for fighter planes to avoid enemy radar detection. His research team not only solved this strategic challenge but also came up with a device as small as a pen that pilots could carry in the event they were shot down to enable search and rescue teams to accurately and covertly locate them. He was proud that his work helped save the lives of key military personnel."

Les was a life-long friend, mentor, and collaborator. As I earned my Ph.D. at Cornell and spent most of my career working on compound semiconductors, I was often mistaken as one of Les' students. I remember fondly that Les was especially nice to me and I thought I knew him fairly well. It was only through a recent conversation with his daughter Laurie that I learned he was a devoted family man who kept his personal life private. Les seemed to have had an excellent balance of work and life.

Les was a big guy difficult to ignore. As an undergraduate student at Cornell, he was a football lineman. He was obviously talented. He graduated from high school at the top of his class and earned the highest score in the New York State Physics Exam given that year. Growing up in a household of limited means, he was inspired by his high-school physics teacher to apply to college. He was admitted by Cornell but could not afford the tuition. He solved the problem by enlisting in the U.S. Navy for a couple of years before entering Cornell on the GI Bill. Thus, he came to Cornell in 1948 and then never left! He did not change jobs here and there to advance his career. He did not put his career before his family. When he was an undergraduate student, he got married and had three children. Career advancement seemed to come naturally to him. However, according to Laurie, he struggled like many of us. Les was actually rather shy and introverted. Though he was the valedictorian of his high school class, public speaking did not come naturally to him. When he spoke in public, he always made sure he thoroughly rehearsed beforehand what he was going to say. Les spent many evenings writing proposals for research funding. And he traveled frequently while missing the family.

Les Eastman with wife Anne, daughter Laurie, and sons David and Daniel in 1957.

Serving as a Navy radar specialist piqued Les' interest not only in microwave electronics but also in sailing. As an avid sailor, he owned two sailboats and often entertained visitors by sailing on the Cayuga Lake, one of the largest Finger Lakes next to Cornell. After his 1960-61

sabbatical at Chalmers Institute of Technology, Gothenburg, Sweden, and inspired by his experience there sailing with a friendly neighbor, Les and a colleague bought a beautiful vintage Nordic wooden Folk Boat from Sweden. Shortly before Les died, he sold it to a former student who kept it in good condition until he too was too old to sail. He offered to return it to Laurie but she hesitated. I was tempted but, although I like sailing, I never owned any boat. I heard that owning a boat, especially a wooden one, was worse than having a mistress. Somehow Les managed everything well.

Les was a real operator in a good way. In the 1980s, Raytheon pioneered monolithic microwave integrated circuits (MMICs). Like digital integrated circuits invented a couple of decades earlier, MMICs were smaller, lighter, and more reliable and manufacturable than microwave circuits made of individual transistors. Being a competitor with Raytheon in the radar business, GE was threatened by the development of the MMIC technology. Les convinced the GE management to start a major MMIC effort to catch up with Raytheon and told them that "Jim Hwang of Bell Labs would be ideal to lead this effort." Les then visited me at Bell Labs and told me "There is this great opportunity for you and I will support you …" Following Les's advice, I started the MMIC effort from scratch in Syracuse, New York, which was only an hour's drive from Cornell. Les encouraged many of his PhD graduates such as Umesh Mishra (now Dean of the College of Engineering, UC Santa Barbara) to join me even though they had job offers from better-established places. It helped that Les was the most "productive" in the 1980s and was graduating a half dozen Ph.D. students every year. With the help of the Cornell graduates, we quickly produced the world's smallest transistor with a critical dimension of 250 nm, which unleashed a new wave of investments by GE. However, the truth of the matter was that the transistor was produced not only by Cornell graduates but also in Cornell's clean rooms and on materials grown by Les's group. Like today, even though I had ample funding, building clean rooms and buying semiconductor equipment took a long time. Collaborating with those having existing expertise and facility bought us time while waiting for our own facility to be completed and equipment to be delivered.

Les was instrumental in starting the half-billion-dollar, decade-long MMIC project of the US Defense Advanced Research Projects Agency, which was one of their most successful projects. In the 1980s, Japan appeared to be conquering the world in manufacturing. The saying then was "Everything is made in Japan," especially electronic gadgets. Les led a study team of academic, industrial, and governmental experts who recommended accelerating the MMIC development and pilot production in the US to trump the Japanese, who were still riding on the coattails of their success in individual microwave transistors. Through the MMIC program, the US came to dominate the microwave components business. To this date, most mobile phones contain MMICs that are made in the US.

Les was a visionary. MMICs were made possible only after solid-state microwave transistors were developed to replace bulky vacuum tubes. His doctoral thesis had been on vacuum electronics, as were those of his first two Ph.D. students. However, starting from 1968, all of his Ph.D. students studied solid-state transistors.

I was happy to see MMIC technology flourishing. Before joining GE and while still at Bell Labs, I contributed to the development of microwave transistors to replace vacuum tubes in the terrestrial microwave network, which then carried all long-distance telephone calls. The development was not only a technical success but also a commercial success. As a young component engineer, I learned that big companies make money in systems instead of components. They will love you if you improve the system capacity several times by replacing a few key components in an existing system. Replacing components takes months and costs millions of dollars; fielding a new system takes years and costs billions of dollars.

Another lesson I learned at Bell Labs is that big companies support component development because it helps differentiate their systems. However, once a system is developed into a volume business, they often turn to bids outside. After developing microwave transistors at Murray Hill, New Jersey, I traveled often to Reading, Pennsylvania to transfer the technology into production. (The highway literally cut across the campus of Lehigh University and I flew by it many times without knowing that later I would start my academic career there.) As usual, technology transfer, even within the same company, was delayed while system delivery was committed. We then mounted a heroic effort to not only accelerate the transfer to Reading but also to ramp up the research facility in Murray Hill for production. Still, after meeting the initial delivery deadlines, Ma Bell decided to buy microwave transistors from Japanese suppliers such as Fujitsu. Thus, all our efforts in technology transfer to Reading had been in vain.

By contrast, Fujitsu was very effective in transferring microwave transistors from R&D to production. Later, while a consultant for the US Defense Satellite Communications System, I visited Fujitsu in Japan and learned their tricks in technology transfer. Literally, the same day a decision was made to transfer technology into production, everyone switched hat from R&D to production with the same team and in the same facility. Had the approach been adopted in the US, many R&D engineers would have bailed out.

However, the Japanese were not perfect in technology transfer. As the demand for microwave transistors continued to escalate in the 1990s, Fujitsu decided to transfer their production out of metropolitan Tokyo to a newer and bigger facility and not everyone was willing to move. Unbeknownst to anyone, It caused a temporary setback in

transistor reliability, which in turn, caused many US defense and communications systems to prematurely fail. The so-called "power-slump" problem of gallium-arsenide transistors prompted my visit to Fujitsu and my becoming an expert on power slump. I found the failure was caused by differences in surface passivation and field distribution, like the more recent and severe "current-collapse" problem of gallium-nitride transistors. However, having been labeled as a slump expert, I decided not to become a collapse expert.

Les's memory was legendary, especially concerning technical matters. Once I asked him "Who invented silicon-nitride passivation of gallium arsenide?" He said, "You did. I first heard it from you twenty years ago in your Bell Labs office." It was my most impactful invention, but few knew about it because it was never published except buried in the US Patent No. 4,493,142 "GaAs FETs having long-term stability." At Bell Labs, I was free to publish anything except this invention which enabled Ma Bell to use gallium-arsenide transistors in satellites. Nevertheless, back then I knew telling Les was almost as good as publishing because he was consulting with many companies and government labs. When Umesh joined GE, I gave him a copy of the patent and tasked him to develop the passivation process for gallium-arsenide transistors. He said he was totally baffled by the patent. I told him that Bell Labs had many talented patent attorneys who knew exactly how much to disclose. Back during the good old days of Bell Labs, Ma Bell had a deal with the government to continue their telecommunications monopoly while licensing all their patents without fees to anyone except their non-existent direct competitors. Eventually, mounting political pressure prompted the breakup of Ma Bell in 1983. I owe Les for getting me out of Bell Labs just before the chaotic divestiture.

The above is what I know and remember about Les, especially the tidbits not well known. It represents a tiny facet of this giant in our field, because, unlike Les, my memory is fading.

Author Biography

James C. M. Hwang (Life Fellow, IEEE) received the B.S. degree in physics from National Taiwan University, Taipei, Taiwan, and the M.S. and Ph.D. degrees in materials science and engineering from Cornell University, Ithaca, NY, USA. He is currently a Professor at the Department of Materials Science and Engineering, at Cornell University. Prior to that, he spent most of his academic career at Lehigh University, Bethlehem, PA, USA, after years of industrial experience at IBM, Yorktown Heights, NY, USA; Bell Labs, Murray Hill, NJ, USA; GE, Syracuse, NY, USA; and GAIN, Somerville, NJ, USA. He cofounded GAIN and QED, Bethlehem, PA, USA; the latter became the public company IQE and remains the world's largest supplier of compound-semiconductor epitaxial material. He was a consultant for the Air Force Research Laboratory, Dayton, OH, USA, and a Program Officer for GHz-THz Electronics at the Air Force Office of Scientific Research, Arlington, VA, USA. He was an IEEE Distinguished Microwave Lecturer. He is an Editor of IEEE Transactions on Microwave Theory and Techniques. He has worked on electronic, optoelectronic, and micro-electromechanical materials, devices, and circuits for decades. He has received many honors and awards, including the IEEE Lester F. Eastman Award for outstanding achievement in high-performance semiconductor devices. His current research focuses on sub-terahertz materials, devices, and circuits for 6G wireless communications and next-generation automobile radars.

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Regional News

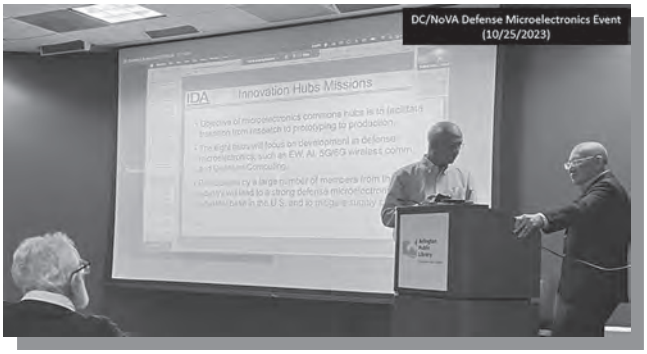
USA, Canada (Regions 1–6, 7)

Northern Virginia/Washington DC Chapter Hosts Two Events: CHIPS—An Unprecedented Opportunity What This Program Means by Dr. Michael Fritze, and Defense Microelectronics Industrial Base by Dr. Clifford Lau

—by Xiangyi "Tony" Guo

The EDS Northern Virginia/Washington DC Chapter hosted two events on CHIPS (Creating Helpful Incentives to Produce Semiconductors) related topics. The first topic, "CHIPS—An Unprecedented Opportunity What This Program Means" was presented on 20 September 2023 by Dr. Michael Fritze, Consultant at Trusted Strategic Solutions and former Vice President at the Potomac Institute for Policy Studies. The event was co-sponsored by a few other EDS Chapters. Dr. Fritze began the talk with CHIPS legislation background and timeline and the motivations behind this historic semiconductor investment. Later, he covered the CHIPS appropriations period what we will focus on, and execution plans. This included the Department of Commerce Incentives and R&D efforts and the Department of Defense Microelectronics Commons. The event ended up with hot discussions on some of the key challenges of this major US Government investment (see the event image). The lecture presentation slides can be accessed through the vTools event (ID: 371348) Media section. The event was attended by 109 participants. This event hit the highest attendee count in the last year. The other topic, "Defense Microelectronics Industrial Base", was presented on 27 October 2023 by Dr. Clifford Lau, a research staff member at the Institute for Defense Analyses and former program director of the Office of Naval Research (ONR). The event was also co-sponsored by a few other EDS Chapters. Dr. Lau reviewed the microelectronics background in defense C4ISR and weapon systems. He stated the importance of CHIPS and the Science Act to reshore semiconductor manufacturing back to the U.S. He reviewed DoD's Microelectronics Commons selected eight regional innovation hubs that include a large number of members in the industrial base, and their focus on strengthening the defense microelectronics industrial base. At the end of the event, there were a few excellent Q&As on the 8 hub members, TSMC/IMEC differences, spending and timeline, and university and talented international student roles. This event was attended by 56 participants.

"CHIPS—An Unprecedented Opportunity What This Program Means" by Dr. Michael Fritzeheld event held on 20 Sept. 2023.



"Defense Microelectronics Industrial Base" by Dr. Clifford Lau event held on 25 Oct. 2023.

Future Semiconductor Workshop at the University at Buffalo

—by Vasili Perebeinos

On 17 June 2023, a Workshop on Future Semiconductors: Chiral Photonics and 2D Materials for Future Semiconductors took place at the University at Buffalo, sponsored by the National Science Foundation, IEEE EDS Buffalo Section, and the University at Buffalo. Eminent speakers from industry, academia, and US National and Department of Defense laboratories, including Scott Gatzemeier (Micron Technology), Weilu Gao (University of Utah), Joshua Hendrickson (AFRL, Dayton), James Hone (Columbia University), Shengxi Huang (Rice University), Tsung-Wei Huang (University of Utah), Junichiro Kono (Rice University), Paras N. Prasad (University at Buffalo), Angela Rasmussen (University of Utah), Sergei Tretiak (Los Alamos National Laboratory) were invited to join the event and deliver a lecture on the exploration of the co-design of chiral quantum photonic devices and circuits integrated with 2D material heterostructures to enable future high-performance integrated quantum photonic systems. This inaugurating workshop had a primary subject, Quantum Materials Informatics, for materials development and application at the intersection of first-principles calculations, machine learning, and experimental characterization of chiral materials, and

2023 Workshop on Future Semiconductors: Chiral Photonics and 2D Materials for Future Semiconductors at the University at Buffalo.

their heterostructures for applications in photonics. The event saw a significant participation of young PhD students, post-docs, and early-stage researchers.

Meet Your Heroes Event

—by Paul R. Berger

Role models are an important reflection of our EDS Society and serve to elevate the community, lifting all boats with the tide. On 4 October 2023, a "Meet Your Heroes" event was held to create an open, inclusive conversation on career development and career aspirations, by revealing the obstacles and challenges overcome by some of our EDS role models. We hoped to motivate the next workforce wave by illustrating how their tribulations may not be very dissimilar to your own personal hardships. Two panelists were invited to speak to the semiconductor industry from various perspectives as academicians, industrialists, and innovators. Although speakers centered on the semiconductor industry, all visitors were welcome.

Tsu-Jae King Liu, Dean, UC Berkeley College of Engineering

Tsu-Jae King Liu, faculty from the University of California, Berkeley in the Department of Electrical Engineering and Computer Sciences, and Dean of the College of Engineering since 2018 represented a more academic side, but with her work on the Board of Directors for Intel and Maxlinear, she transcended into the industrial world too.

Carolyn Duran, Senior Director, Product Integrity, Apple

Balancing the panel was **Carolyn Duran**, now at Apple, who spent 25 years at Intel Corporation, most recently as Vice President within the Components Research organization. Carolyn is also an Adjunct Professor of Materials Science and Engineering at Northwestern University and is the immediate past President of the Materials Research Society.

They both spoke about their early careers, overcoming career obstacles and even perceived career detours that actually provided a depth of complementary experience that empowered their careers later. Tsu-Jae King Liu vocalized her aspirations for "embracing challenges and seizing opportunities," and always saying "yes" to new opportunities. Carolyn Duran expressed a rhyming voice for everyone to "raise your hand!"

The sharing of their own very personal challenges was extremely comforting to the audience, who all endure their own personal challenges and hardships. By overly idolizing the seemingly idyllic worlds of our role models, we promote the anxiety of FOMO (fear of missing out) within our community. But this very personal event shattered those barriers and promoted a can-do message to all the attendees.

Paul R. Berger of Ohio State University and Tampere University created the event and acted as master of ceremonies, polling the attendees along the way as to their career stage, if they are underrepresented, their

Paul Berger, Professor, Ohio State University

areas of interest (i.e., academic, industry, etc.) and if they find the EDS field rewarding. Polling showed a broad and diverse audience from students to early-career and senior professionals. The audience also reflected a very positive tone for EDS being rewarding with replies centered upon agree and strongly agree and a dearth of negative responses.

About 40% of the attendees were from the USA, balanced with attendees from Germany, the United Kingdom, Switzerland, Bangladesh, India, Indonesia, Malaysia, the Philippines, and Saudi Arabia.

Europe, Middle East & Africa (Region 8)

7th Symposium on Schottky Barrier MOS (SB-MOS) devices—The Schottky barrier transistor in emerging electronic devices

—by Mike Schwarz and Laurie Calvet

The 7th Symposium on Schottky Barrier MOS (SB-MOS) devices was held on 28–29 September 2023 at the Ecole Polytechnique in Palaiseau, France. It was a joint chapter event organized by the EDS France and Germany Chapter and co-sponsored by Ecole Polytechnique and CNRS. It was attended by approx. 30 participants in both presence and hybrid formats.

After a short welcome of Dr. Laurie Calvet from CNRS-Ecole Polytechnique (FR) with a detailed schedule, the presentations were started by the chair Kham Niang with an inspiring talk of Dr. Calvet on the topic of "The Schottky barrier transistor in emerging electronic devices". She reviewed a variety of applications and material systems for over 60 years and introduced the SB transistor. She started with an overview of the device modeling and presented the two large classes of SB devices: 1) those that aim to reduce the Schottky barrier and 2) those that aim to take advantage of it. The talk concluded with a series of questions meant to serve as the starting point for the panel discussion later in the afternoon.

The next talk entitled "Silicon-Germanium Nanosheet Schottky FETs, from Contact Properties to Runtime Reconfigurable Circuit Demonstrators" was given by Prof. Walter Weber, TU Vienna (AT). Prof. Weber offered new insights into the silicon germanium compound (Si_xGe_{1-x}). While the silicon germanium active regions have been intensively investigated for the realization of both bipolar and field effect devices over the past decades, the realization of ultrathin-body Si_xGe_{1-x} transistors, in particular Schottky contact transistors, with high germanium content in the channel has been hampered by instabilities of interfaces between semiconductors and metals and insulators. Prof. Weber discussed the combination of advances in ultra-low-temperature epitaxy, contact- and interface-solid state Al diffusion processes as well as reliable surface passivation measures that allow for the realization of ultrathin Si_xGe_{1-x} nanosheet Schottky contact FETs being integrated on commercially available silicon-on-insulator substrates. He offered high-resolution images of the obtained Schottky Si_xGe_{1-x} devices with abrupt Al contacts which profit from the abrupt Schottky junctions and high germanium content and form a base technology for the realization of future contenders of electronic devices beyond the scope of the industrial roadmaps. Finally, Prof. Weber showed the possibilities of runtime reconfigurable transistors, neuromorphic devices, and cryogenic quantum devices which can be realized using the same technological platform.

The symposium continued with "DC Compact Modeling of Schottky Barrier Field-Effect Transistors at Deep Cryogenic Temperatures". The PhD candidate Christian Römer from the University of Applied Sciences Mittelhessen (Technische Hochschule Mittelhessen (THM)) (DE) discussed Schottky barrier field-effect transistors as candidates for applications at cryogenic temperatures since their characteristics improve with decreasing temperatures. He presented a physics-based DC compact model to calculate the injection tunneling current through a device's Schottky barrier. Verification of the compact model was performed by measurements at temperatures around 5 K.

The final part of the first workshop day was the panel discussion on the question "What is the future of Schottky barrier devices?". At the panel, Dr. Calvet, Prof. Weber, and PhD candidate Römer offered their opinions, and various questions were discussed from different aspects.

The second workshop day was chaired by Prof. Weber and started with the talk entitled "Ferroelectric Schottky barrier transistor for neuromorphic computing" by

Participants of the 7th Symposium on Schottky Barrier MOS (SB-MOS) devices.

Prof. Qing-Tai Zhao from the Forschungszentrum Jülich (DE). Prof. Zhao offered the challenges of the slow and ambipolar switching behavior of Schottky barrier MOSFETs which poses certain challenges for logic applications. Nevertheless, during his presentation, he explored potential applications of the SB MOSFETs in neuromorphic computing when combined with a ferroelectric gate oxide. Prof. Zhao discussed the implementation of artificial synapses and capacitorless neurons using ferroelectric Schottky barrier transistors. By this novel approach, he offered advantages for advancing the field of neuromorphic computing.

The next talk was given by Prof. Radu Sporea from the University of Surrey (UK). Before Prof. Sporea started the talk on "Recent implementations of source-gated transistors and circuits with high gain", he shortly introduced the campus of Surrey where the next Symposium of Schottky Barrier MOS devices will take place. Then he continued with the source-gated transistor (SGT), which is celebrating 20 years since its invention, and presented the way how some of the more fundamental limitations of these devices have been explored and gradually overcome. The latest advances in exploiting the SGT's high intrinsic gain, along with a roundup of essential design rules of thumb were offered.

Afterward, Prof. Alexander Kloes from THM presented "Evaluation of approaches for analytical calculation of tunneling currents in Schottky barrier transistors". He explained the different methods to calculate the transmission coefficient in the tunneling equation, explaining why compact modeling of tunneling currents is so challenging. Prof. Kloes reviewed the analytical calculations of a quantum wave-based current transport through Schottky barriers that are suitable for compact modeling. He focused on a new promising approach based on the wavelet transform.

"Indium Gallium Zinc Oxide Source-Gated Transistors" by Kham Niang, a PhD candidate at the University of Cambridge (UK), was the next talk. Ms. Niang discussed the use of amorphous oxide semiconductor (AOS) thin film transistors (TFTs) as SGTs. She presented also the fabrication and performance of recent IGZO SGTs, discussed in particular the challenges in realizing a Schottky contact between AOS and high-work function metal, and presented various methods adopted to mitigate this problem.

The presentations continued with "TCAD simulation studies of source-gated p-type CuO TFTs" by Qi Chen, a PhD candidate from the Université Catholique de Louvain (UCLouvain) (BE). Source-gated p-type CuO TFTs with HfO_2 gate dielectric were studied using TCAD tools. Based on parameters extracted from experiments, the gate modulation of the source barrier was investigated varying the thicknesses of CuO and HfO_2 and the Schottky barrier height at the source contact. The optimal structure design was further explored to obtain good transconductance and output conductance parameters for circuit design.

Afterward, Prof. Benjamin Iniguez from Universitat Rovira i Virgili (URV) (ES) gave a talk entitled "Compact modeling of the nonlinear contact effects in Organic Thin Film Transistors". He presented the nonlinear contact effects due to the presence of Schottky barrier at the source-channel interface which may significantly affect the I-V characteristics in Organic Thin Film Transistors. He reviewed four different models that can be used for compact modeling.

The final talk "A Source-Gated Transistor Compact Model Designed Using TCAD Simulations" was given by Patryk Golec, a PhD candidate at the University of Surrey. a compact model developed for a source-gated transistor (SGT) using the data obtained from TCAD simulation. He reported some fundamental simulations that he made to explain the fundamental different current injection mechanisms occurring at the source region. This causes the contact effects to be dominant in the SGTs, as opposed to the TFTs. With this, the resulting compact model of a-Si SGTs describes the changes in device parameters within the source region.

Dr. Laurie Calvet closed the Symposium with some final remarks that Schottky barrier junctions offer a wide spectrum of applications and thanked all the participants and organizers for realizing the 7th edition of SSBMOS.

Events in Spain in 2023

—by Lluis F. Marsal

Mini-Colloquium on the 75th Anniversary of the Transistor

A Mini-Colloquium commemorating the 75th Anniversary of the Transistor Invention was held at the University Rovira i Virgili (Tarragona, Spain) on January 26. It consisted of three talks by EDS Distinguished Lecturers. Two talks were virtual and the other one was online. Prof. Manoj Saxena (University of Delhi, India) gave an online presentation entitled "Journey through Three

Professors Lluís F. Marsal (Chair of the ED Spain Chapter), Sorin Cristoloveanu, and Benjamin Iñiguez (Vice-Chair of the ED Spain Chapter) at the MQ in Tarragona (Spain).

Magical Months 75 years ago: Transistor Invention." Dr. Wladek Grabinski (GMC, Switzerland) addressed in a virtual talk the "History and Evolution of TCAD/EDA Tools Towards FOSS Applications," Finally, Prof. Sorin Cristoloveanu (Grenoble. INP, France) targeted, "The SOI Transistor" in a hybrid presentation. The Chair of this Mini-Colloquium was Prof. Benjamin Iñiguez, Vice-Chair of the ED Spain Chapter.

EUROSOI-ULIS 2023

The 9th Joint International Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS 2023) took place between May 10 and 12 2023 in Tarragona (Spain). The Chair of this workshop was Prof. Benjamin Iñiguez (University Rovira i Virgili, Tarragona, Spain). EUROSOI-ULIS is one of the mainstream conferences about semiconductor devices in Europe.

There were five invited speakers at EUROSOI-ULIS 2023. Ehrenfried Seebacher, ams-OSRAM (Austria) talked about "Semiconductor Devices for Integrated Optical Solutions". Luciana Capello, SOITEC (France), addressed "Piezoelectric on Insulator structures". Stefan Lischke, Leibniz-Institute for High-Performance Microelectronics (Germany), targeted "Photonic BiCMOS technology—an enabler of high-speed monolithic EPIC". Finally, Muhammad Nawaz, Hitachi Energy (Sweden), gave a presentation about"SiC devices for power electronics; performance, issues and challenges"

On May 9 2023 a Workshop on Advanced Materials for Disruptive Devices and Applications was also held in Tarragona. It was organized by the SINANO Institute and ASCENT+, an EU-funded project aimed at offering the infrastructure of the biggest European semiconductor device laboratories to other researchers and technicians in Europe and Elsewhere. This workshop included 18 invited talks, most of them targeting advanced materials, device integration, disruptive devices, and future computing.

Distinguished Lectures

On 18 May 2023, two EDS Distinguished Lecturers gave talks at the University Rovira i Virgili (Tarragona, Spain). Prof. Magali Estrada (CINVESTAV, Mexico) targeted "Hybrid solar cells: An overview of their main characteristics, state of the art and applications," Prof. Antonio Cerdeira (CINVESTAV, Mexico) addressed the "Modeling of nanowires and nanosheets at high temperature."

Mini-Colloquium

An EDS Mini-Colloquium (MQ) o was held on June 5 2023 in Valencia (Spain), organized by the ED Spain Chapter, prior to the Spanish Conference on Electron Devices (CDE). The Chair of this MQ was Prof. Lluís F. Marsal (University Rovira i Virgili, Tarragona, Spain), Chair of the Chapter.

Several topics related to semiconductor devices were addressed by five speakers, all of them EDS Distinguished Lecturers. Four presentations were in person and one was virtual.

The Graduate Student Meeting on Electronic Engineering was held also in Tarragona on 29–20 June and included the Joint Session with the MQ mentioned above, two sessions with Ph.D. student presentations (June 29 afternoon and June 30 morning), a poster session, and two more invited talks. The Chair was Josep Ferré-Borrull, a Professor at the University Rovira i Virgili. It is an annual event created and organized by the Department of Electronic, Electrical, and Automatic Control Engineering of the Universitat Rovira i Virgili (URV) in 2003. It consists of two days of plenary talks given by invited prestigious researchers about selected topics related to electronic engineering, short talks given by last year's Doctoral students presenting their last research results, and a poster session where master and Ph.D. students in this field present their work.

This MQ was one of the EDS events commemorating the 75th Anniversary of the Transistor. Actually, two lectures were directly related to that anniversary. The first speaker, Dr. Fernando Guarín (Senior Past President of the EDS), gave a talk entitled "75th Anniversary of the Transistor: Semiconductor Industry Perspective." The title

Professors Benjamin Iñiguez (Vice-Chair of the ED Spain Chapter), Antonio Cerdeira, Magali Estrada, and Lluís F. Marsal (Chair of the ED Spain Chapter), at the DL in Tarragona (Spain).

(Left) Fernando Guarín, Senior Past President of the EDS, and (Right) Benjamin Iñiguez, Fernando Guarín, Samar Saha, Mario Lanza, Arokia Nathan, and Lluis F. Marsal at the Mini-Colloquium in Valencia (Spain).

of the presentation by the last speaker, Dr. Samar Saha (Prospicient Devices/Santa Clara University, CA, USA) was "Invention that made Profound Changes to Humanity: Transistor and its Evolution Enabling Digital Ecosystem."

On the other hand, Prof Arokia Nathan (Darwin College, University of Cambridge) addressed the "Ultra-low power sensor interfaces for IoT." Prof. Nazek El-Atab (King Abdullah University of Science and Technology, Saudi Arabia) gave a virtual presentation about "Smart multifunctional electronic devices with atypical architecture for IoT applications." Finally, Dr. Mario Lanza (King Abdullah University of Science and Technology, Saudi Arabia) targeted the "Advanced nanoelectronics metrology."

CDE 2023

The 14th Spanish Conference on Electron Devices (CDE) was held in Valencia from June 6 to 8 2023. It is a usually bi-annual event. This year its 25th Anniversary was celebrated. The Chair of CDE 2023 was Càndid Reig (University of Valencia).

CDE is the main forum where most Spanish researchers working on electron devices can meet, but the conference is open to researchers from outside Spain. There were four talks, two of them related to the 75th Anniversary of the Transistor Invention. Dr. Samar Saha (Prospicient Decices, and Santa Clara University, CA, USA) addressed "An overview of FinFET devices and non-planar CMOS device technology," Prof. Ignacio Mártil (Universidad Complutense, Madrid) gave a presentation entitled "The History of the Transistor." Prof. Arokia Nathan (Darwin College, University of Cambridge, UK) targeted "Low-power flexible electronics." Prof. Ronald Tetzlaff (TU-Dresden, Germany) gave a talk entitled "Memristors." In addition, there was a roundtable about Microelectronics in Spain.

Graduate Student Meeting on Electronic Engineering

The Graduate Student Meeting on Electronic Engineering was held at the University Rovira i Virgili (URV) in Tarragona (Spain) on June 29–30 2023.

It is an annual event combining plenary talks by prestigious researchers and student presentations in both oral and poster forms. This year it included presentations by postdoctoral researchers at URV.

One of the plenary speakers, Dr. Fernando Ávila (GlobalFoundries, Dresden, Germany) addressed the "High Voltage MOSFET Compact Models Challenges." Another keynote speaker, Stefania-Alexandra Iakab (Center for Mass Spectrometry and Optical Spectroscopy, Mannheim, Germany) targeted the "Monitoring small molecules from 3D cell culture models using MALDI MSI."

On the other hand, one of the invited speakers, Prof. Claudio Paoloni (Lancaster University, UK), gave, as an EDS Distinguished Lecturer, a talk entitled "Renaissance of Travelling Wave Tube Technology for sub-THz Applications,"

Professors Benjamin Iñiguez, Vice-Chair of the ED Spain Chapter, and Claudio Paoloni, at the Graduate Student Meeting of Electronic Engineering in Tarragona (Spain).

that was somewhat related to the 75th Anniversary of the Transistor Invention, which replaced vacuum tubes in most applications.

The Basics and Evolution of Organic Devices by Prof. Benjamin Iniguez

—by Mike Schwarz

On December 14, 2023, a distinguished lecture titled "**The Basics and Evolution of Organic Devices**" was delivered by Prof. Benjamin Iniguez, an IEEE Fellow from URV. The event, organized by Prof. Alexander Kloes and Prof. Mike Schwarz of the Competence Center for Nanotechnology and Photonics (NanoP) at THM - University of Applied Sciences, Germany, drew the participation of 25 attendees.

During the lecture, Prof. Iniguez provided an overview of the historical development of the first Thin-Film Transistor (TFT) devices leading up to the present day. He delved into the details of their properties, benefits, and applications. Subsequently, Prof. Iniguez shifted the focus to Organic Light-Emitting Diode (OLED) devices, offering a

Prof. Benjamin Iniguez celebrating the 75 Anniversary of the Transistor in front of the audience.

historical perspective and discussing the applications and future trends of these devices. The lecture concluded with an overview of Organic Photovoltaic (OPV) devices, covering their current efficiencies in laboratory settings and industrial applications.

This distinguished lecture was part of the celebration of the 75th anniversary of the transistor and showcased one of the many use cases that have emerged over the last few decades. Participants were intrigued by the revelation that the invention of the transistor ultimately paved the way for the development of technologies found in today's applications.

Latin America (Region 9)

2nd Edition of the IEEE EDS R9 Summer School

—by Wendy Pantoja

The 2023 IEEE EDS Summer School, entitled "Design, Characterization, and Fabrication of Sensors and Integrated Circuits" was organized by the Latin American Electron Devices Congress LAEDC and hosted by the National Institute for Astrophysics, Optics, and Electronics (INAOE). The event took place from 29 June to 1 July 2023, in Puebla, Mexico. The three-day summer school featured lectures, guided laboratory tours, experiments, hands-on training, and research experience in the design, characterization, and fabrication of integrated circuits (ICs) produced in Latin America.

The event hosted more than 220 students (80 in-person, and 140 virtually) from Colombia, Ecuador, Peru, Costa Rica, Guatemala, Honduras, Panama, Chile, and Mexico. Scholarships for 80 attendees were awarded to selected students to cover accommodation and meals. The participants attended a three-day course with nine lectures from both industry (Synopsis) and academic institutions (INAOE/Georgia Tech/Universidad de los Andes). The tools provided included licensed and open-source software tools. Furthermore, a guided tour of the laboratories was arranged to visit INAOE's facilities including Microelectronics, LiMEMS, Microscopy, Electro-photonics, Optical Communications, and MEMS laboratories.

Students from EDS Chapters at the Puebla City Hall, Mexico for the special session with the community.

Additionally, the Summer School aimed to raise awareness within the community about the impact of technology and to inspire children to pursue careers in science, technology, engineering, arts, and mathematics (STEAM). To achieve this goal, a special session was organized at the Puebla City Hall, where 300 students from the municipality of Puebla actively participated. This activity was a collaborative effort between INAOE, the City of Puebla, IEEE Puebla Section, and the student branches of various institutions, including BUAP, UDLAP, UPP, UPAEP, ITNM Huachinango, Atlixco, and Puebla IEEE of Mexico, and the Universidad de los Andes as a special guest for presenting the result of a humanitarian engineering project that focuses on helping the community understand two of the parameters that determine water quality: pH and conductivity.

This version of the summer school was also the venue for the launching of the project "Latin Practice", a new EDS/Synopsys initiative to expand microelectronic design in Latin America.

More information can be obtained at https://attend.ieee.org/laedc-2023/special-sessions/summer-school/#1681591120141-9fe64bf4-4bfe

~Paula Agopian, Editor

Asia & Pacific (Region 10)

ED Indonesia Chapter

Mini Colloquium on 75th Anniversary of Transistor Invention

—by Basuki Rachmatul Alam

On 28 August 2023, the IEEE Electron Devices (ED) Indonesia Chapter successfully organized a Mini Colloquium (MQ) to commemorate the 75th Anniversary of the invention of the Transistor. This event was a joint initiative between IEEE EDS and SCCS. The MQ was co-hosted with the Microelectronic Center and Electronic Research group of the Institute of Technology Bandung (ITB). The theme of the Mini-Colloquium was "75-Year Transistor Evolution: A Journey from Point Contact to 3D Integration of Multi-Technology Transistors". A total of 151 participants took part in the meeting, both offline and online (via Zoom).

Undergraduate and graduate students from the Institute of Technology Bandung and nearby universities, as well as

A group of participants of the Mini-Colloquium "75-Year Transistor Evolution: A Journey from Point Contact to 3D Integration of Multi-Technology Transistors."

students from Batam State Polytechnic, participated in the MQ. Senior researchers from the National Research and Innovation Council (BRIN) also attended in person. The event began with an opening speech by Dr. Basuki Rachmatul Alam, the Chair of the ED Indonesia Chapter, who shared insights from his past work on the fabrication of heterojunction transistors, including his thesis work on InGaAsP Double Heterojunction Bipolar Transistor.

Following the opening speech, Prof. Susthitha Menon delivered a speech online as a member of the EDS Board of Governors. As the chair of WiEDS (Women in Electron Device Society), she introduced WiEDS' vision, mission, and activities. The MQ commenced with a lecture by Prof. Pei Wen Li on Germanium Quantum Dots (QD), titled "The Wonderful World of Designer Germanium Quantum-Dot Transistors." Prof. Li discussed spherical Ge QD for pairing as a qubit cell, which is compatible with CMOS processes.

The second lecture, presented virtually on behalf of SCCS by Dr. Vita Pi-Ho Hu of National Taiwan University, covered "Advanced SRAM Design and Technologies." Dr. Vita provided insights into SRAM cache memory design and technology, including cryo-CMOS SRAM, monolithic 3D SRAM, and non-volatile ferroelectric-based SRAM cells.

The third distinguished lecture by Prof. Cor Claeys, the former director of IMEC Leuven, was titled "Trends and Challenges in Micro- and Nanoelectronics for the Next Decade." He discussed the exponential evolution of the field, necessitating the implementation of novel materials and transistor structures, along with advanced design concepts. He highlighted various device architectures, such as FinFETs, TFETs, negative capacitance, Gate-All-Around, nanowires (NWs), nanosheets (NSs), CFET, and Forksheet structures, not only for logic gates but also for analog/RF building blocks in System-on-Chip (SoC) applications.

After a lunch break, the MQ continued with a fourth lecture by Prof. Carlo Samori, who discussed "How Transistor Scaling Reshaped the PLL." The speaker explored recent implementations of digitally-intensive PLLs that leverage technology scaling, highlighting both their advantages and limitations.

The fifth distinguished lecture, delivered by Prof. Albert Chin, Chair Professor of National Yang Ming Chiao Tung University, was titled "Outstanding High Transistor Mobility Toward Three-Dimensional Brain-Mimicking IC Architecture." Prof. Chin discussed nanosheet transistors with significantly higher electron mobility compared to other high-speed transistors and their potential as an enabling technology for logic cells in brain-mimicking ICs and 3D ICs.

The MQ, celebrating the 75-year evolution of the transistor, concluded with closing remarks from the Chair of the ED Indonesia Chapter, who expressed gratitude to the distinguished lecturers from EDS and SCCS and encouraged the young student audience to maintain their passion for semiconductor device technology for the future progress in microelectronics.

~ Sharma Rao Balakrishnan, Editor

EDS Japan Joint Chapter

—by Nobuyuki Sugii and Naoki Watanabe

EDS Distinguished Lectures

On 6 September, the EDS Japan Joint Chapter in collaboration with TeraTech 2023 (https://www.teratechconf.org/) organized in a hybrid-mode the EDS Distinguished Lecture event at Aizu University, Japan. Prof. Michael Shur from Rensselaer Polytechnic Institute presented "Sensing using terahertz radiation," exploring after a comprehensive review, the new frontiers of terahertz (THz) sensing. Subsequently, Prof. Taiichi Otsuji of Tohoku University discussed "Terahertz plasmonic devices using graphene-based 2D materials," offering insights into recent progress in THz devices employing graphene-based

Prof. Michael Shur and attendees of the IEEE EDS Distinguished Lectures held at Aizu University, Japan and online on 6 September 2023 (left). Prof. Taiichi Otsuji lecturing on THz devices utilizing graphene-based 2D materials (right).

materials. The lecture notably emphasized THz sources and detectors for future wireless communication systems beyond 5G. After the lecture, the attendees engaged in discussions about the nuances and prospects of these technologies

EDTM-2023 (IEEE Electron Devices Technology and Manufacturing) Report Session

On 22 August 2023, the report session for the 7th IEEE Electron Devices Technology and Manufacturing (EDTM) Conference 2023 was held at the Ookayama Campus of Tokyo Institute of Technology and conducted in a hybrid format. Prof. Hitoshi Wakabayashi, a member of the Steering Committee for EDTM-2023, delivered a comprehensive report on the activities of EDTM-2023 and outlined the plans for EDTM-2024. During the session, subcommittee members presented the trends discussed in their respective technical sessions, including:

- Subcommittee on Power and Energy Devices: Prof. Wataru Saito (Kyushu University),
- Subcommittee on Process, Tools, Yield, and Manufacturing: Dr. Makoto Miura (Hitachi High-Technologies) and Dr. Yoshiki Yamamoto (Renesas),
- Subcommittee on Nanotechnologies: Ms. Kim Myeongok (University of Tokyo),
- Subcommittee on Semiconductor Devices: Prof. Kuniyuki Kakushima (Tokyo Institute of Technology).

Attendees (in-person and online) of the report session of EDTM-2023 on 22 August 2023, Tokyo.

For detailed information on the program and announcements of the report session, please refer to the EDS Japan Joint Chapter's website (https://www.ieee-jp.org/section/tokyo/chapter/ED-15/). The next edition of the conference, IEEE EDTM-2024, is scheduled to be an in-person event held in Bangalore, India, from 3–6 March 2024. Please refer to the conference website for detailed information. (https://ewh.ieee.org/conf/edtm/2024/)

EDS Kansai Chapter

—by Tokiyoshi Matsuda

Committee Meeting

The Committee meeting of the EDS Kansai Chapter (EDSK) took place on 27 July 2023. 26 committee members took part in the event. They discussed on the arrangement of the then-upcoming technical meeting, colloquium, and the annual IMFEDK 2023 meeting.

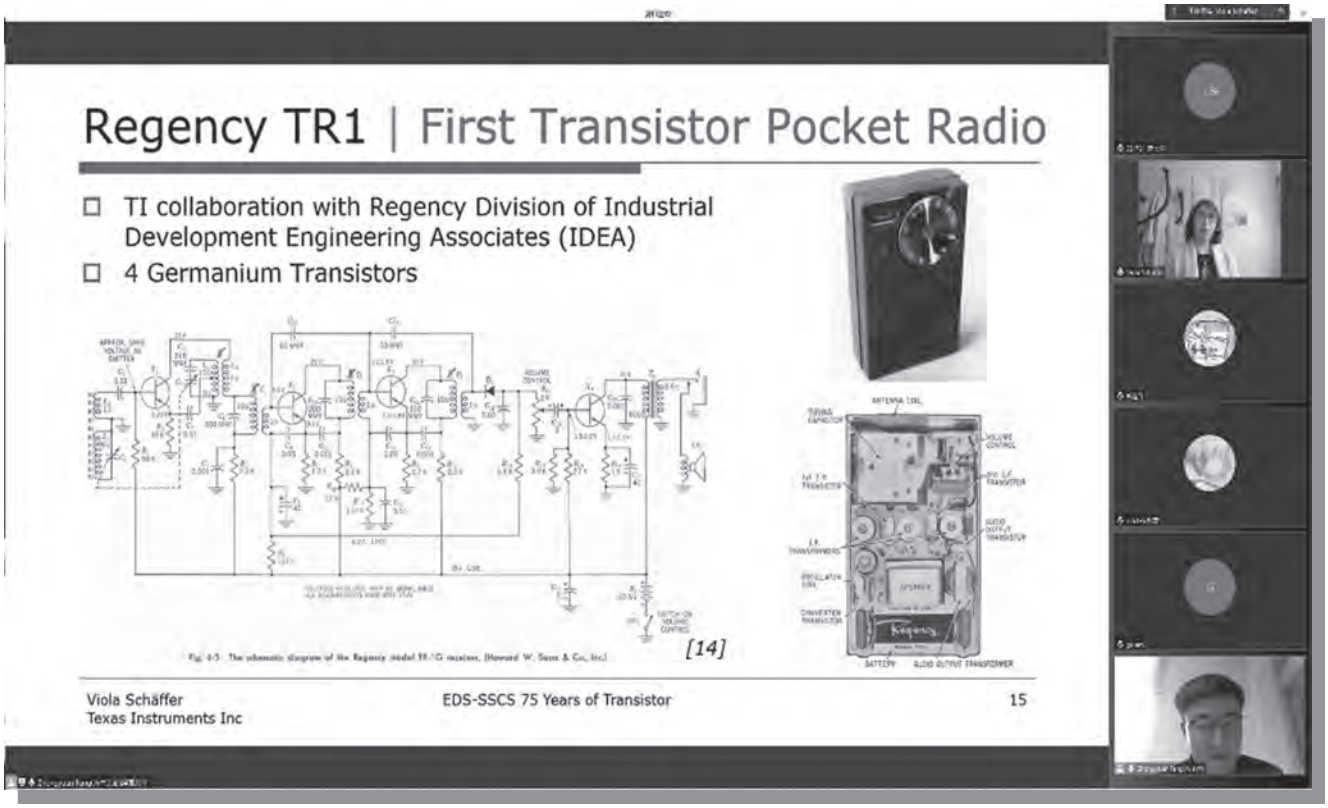
Then-Upcoming Events:

First, the Colloquium and Workshop on Electron Devices 2023 scheduled by EDSK on 6 October, was held. The colloquium consisted of four sessions covering topics such as CMOS Process, Device, and Circuit, Optoelectronics, Displays and Imagers, and Power and Compound Semiconductor Devices. Nine papers selected from the Kansai region were presented, and two awards were given. Second, IMFEDK 2023 (The 2023 International Meeting on the Future of Electron Devices, Kansai) was held as scheduled, on 16–17 November 2023. The refereeing process was underway during the Committee meeting with about 30 submitted papers. More information about IMFEDK 2023 is available at (https://www.ieee-jp.org/section/kansai/chapter/eds/imfedk/).

ED/SSC Nanjing Chapter

—by Weifeng Sun

The Nanjing EDS/SSCS Joint Chapter and the School of Integrated Circuits, Southeast University held on



ED-SSC Nanjing, Invited Transistor 75th Anniversary Webinar on 28 March 2023, the lecture by Ms. Viola Schaffer and the attending faculties and students in Southeast University.

28 March 2023 a special invited talk to celebrate the Transistor 75th Anniversary. The event in the form of a webinar was hosted by Prof. Zhongyuan Fang, who represented Prof. Weifeng Sun, the Chair of the Nanjing ED/SSC Chapter and the dean of the School of Integrated Circuits, Southeast University. The invited expert, Ms. Viola Schaffer, is a Distinguished Member of the Technical Staff at Texas Instruments. Ms. Viola received her M.S. degree in electrical engineering from the University of Arizona, Tucson in 1999. She joined Texas Instruments in 1998 and has been working as an analog IC design engineer and manager at various locations including Tucson, Arizona, as well as Germany. She was elected Distinguished Member of Technical Staff in 2018. Her work focuses on precision signal conditioning, including instrumentation and programmable gain amplifiers, power amplifiers, industrial drivers, magnetic-based current sensors, and precision magnetic sensors. She has design experience in CMOS, HV-CMOS, precision bipolar, and BCD processes. She has led multiple technology-circuit co-developments and designed key-enabling IPs on these new process nodes. At this time, her lecture topic is "Transistor diversity: looking beyond CMOS to improve analog performance".

In the lecture, Ms. Viola indicated that although CMOS transistors came to dominate integrated circuits, some other transistor types such as the bipolar junction transistor (BJT); its variant, the super-beta BJT; the junction gate field-effect transistor (JFET) and laterally diffused metal-oxide-semiconductor field-effect transistor (LDMOS) continued to thrive in specific applications. The talk revisited the discovery of these transistors, their operating principles, and key characteristics, as well as circuit examples that benefit from these characteristics. Ms. Viola also envisioned how these transistors have eluded extinction despite their larger feature sizes and process complexities and how they have evolved in modern technologies. Some interesting games and interactions with audiences were organized by Ms. Viola during the lecture.

This event attracted many attendances with more than 70 PhD and master students, six faculties, and post-doctors.

IEEE Uttar Pradesh Section, ED15 Nepal Chapter

—by Bhadra Pokharel

The ED Nepal Chapter organized a Distinguished Lecture program in Kathmandu on 5 September 2023. The distinguished lecturer was Prof. Chandan Kumar Sarkar, Jadavpur University, Kolkata, India. The title of his presentation was "75 Anniversary of Invention of Transistor". Prior to the program, the Chapter Chair Prof. Bhadra Pokharel

presented the EDS overview slides. Dr. Sanju Shrestha read the short resume of Prof. Sarkar and the abstract of his presentation. The talk was impressive, containing both the historical development and research parts of advanced nano-transistors from micro-level transistors. Prof. Sarkar presented the history of the invention of vacuum devices such as vacuum diodes and multi-electrode devices such as vacuum triodes etc. A journey through the inventions of semiconductor devices from p-n junction diodes to modern transistors was presented with colorful pictures and important data. In total, 19 persons took part in the program. Among them, 14 participants were IEEE members and 5 were non-IEEE students and faculty. Prof. Sarkar was asked many questions. He answered all questions, satisfying the participants' curiosity.

IEEE Kolkata Section, Meghnad Saha Institute of Technology, ED15 Student Branch Chapter

—by Manash Chanda

On 6 January 2023, the Chapter hosted a Technical Talk, delivered by Dr. Saptarshi Das from Penn State University, USA. The event was organized in collaboration with Meghnad Saha Institute of Technology (MSIT) IEEE Signal Processing Society Student Branch Chapter (SBC), IEEE MSIT EDS SBC, and Center of Advanced Research in Renewable Energy and Sensor Technology (CARREST)—MSIT. A total of 39 students attended the program, out of which 15 were IEEE student members. The Chapter also organized on 26 July 2023 an industrial visit at Central Mechanical Engineering Research Institute, Durgapur. The visit was attended by students of the Department of Electronics and Communication Engineering, MSIT, and of Sister Nivedita University, New Town, Kolkata.

A Technical Talk on "Recent trends on optical devices" was organized by the Chapter on 8 February 2023. Mr. Niloy Ghosh, a Ph.D. scholar at IIT Kharagpur delivered the talk. A total of 45 students attended the talk, out of which 12 were IEEE student members. Next, Mr. Debadi Prasanna Gangopadhyay, Design and Verification Engineer, Tech Mahindra Cerium Pvt. Ltd. delivered on 24 March 2023 a Technical Talk titled "Verification techniques in VLSI engineering". This talk was jointly organized by the SSCS Kolkata chapter and EDS MSIT SBC in association with the Department of Electronics and Communication Engineering, MSIT. A total of 76 students attended the program, out of which 13 were IEEE student members.

Dr. Angsuman Sarkar, Professor, ECE Department, Kalyani Government Engineering College delivered on 11 May 2023 an IEEE Technical Talk on "TFET based Biosensors". On 22 May 2023, the Chapter, together with the Department of Electronics and Communication Engineering, MSIT, organized a competition for the presentation of the projects. A total of 63 students attended the project competitions. Mainly VLSI devices, circuits, and system-based projects were presented. Prof. Debasish De, Professor, Maulana Abul Kalam University of Technology, and Prof. Angsuman Sarkar, Professor, Kalyani Government Engineering College judged them and selected the best projects: "AI/ML assisted variability analysis of the JLFET", "Design and implementation of the bulk MOSFET based neuron", and "Junctionless MOSFET based adiabatic logic circuit for ultra-low power applications". The Chapter organized another technical talk on 14 September 2023 on "Posit number system and its application" delivered by Mr. Hemanga Banerjee, a Ph.D. scholar at the University of Strathclyde, Glasgow, UK. A total of 76 students attended the program. A total of 46 students attended the program, out of which 13 were IEEE student members.

IEEE Kolkata Section, University of Calcutta, ED15 Student Branch Chapter

—By Koyel Mukherjee and Soham Banerjee

The Chapter, in collaboration with the IEEE Kolkata Section, Institute of Engineering & Management (IEM),

Participants and the speaker during the outreach program 11 August 2023.

One of the speakers in the "Career Fair" program held on 11–12 October 2023.

and IEEE CASS Student Branch Chapter organized an outreach program on 11 August 2023. The speaker was Dr. Soumya Pandit of the Institute of Radio Physics and Electronics, University of Calcutta. The title of the talk was "Challenges and Prospects of VLSI Devices and Systems." Dr. Pandit elaborately discussed the various issues related to the VLSI deep sub-micron devices and outlined the solutions to mitigate them. The applications of modern devices in Artificial Intelligence and Machine Learning based systems have also been discussed with illustrations. The program was attended by 90 students from graduate and undergraduate levels.

On 11–12 October 2023, a two-day "Career Fair" was organized by the Chapter. The program was jointly organized with chapters of the IEEE Kolkata Section: University of Calcutta, PH036 Student Branch Chapter; University of Calcutta, APS Student Branch Chapter; PH036 Chapter; University of Calcutta, MTT17 Student Branch Chapter, and with the Astronova Club, and AI and Robotics Club. The event aimed to create a platform that brings together esteemed professionals and experts from various industries like GlobalFoundries, HCL Technologies, Ericsson, TCG Crest, C-DAC Kolkata, and ITOrizin Technology Solutions Pvt. Ltd., to share their invaluable experiences, insights, and knowledge regarding the latest trends, opportunities, and challenges within their respective fields.

IEEE Madras Section, IIITDM - Kancheepuram, ED15 Student Branch Chapter

—by Kumar Prasannajit Pradhan

The Chapter in association with the Department of Electronics and Communication Engineering, Indian Institute of Information Technology, Design, and Manufacturing (IIITDM) Kancheepuram organized a school event under the banner of "Engineers Demonstrating Science—an Engineer Teacher Connection (IEEE EDS-ETC)" program. The event was held on 14 August 2023 at Kandigai Government High School, Chennai, Tamil Nadu, and included hands-on sessions during which children utilized snap circuit kits under the supervision of the Chapter members. The students, including their teachers, enjoyed the session by performing the experiments with the motto of "learning by doing". This was really a fun event explaining the fundamentals of electronics while performing live experiments of day-to-day life things.

The Chapter also organized on 12 September 2023 a virtual Distinguished Lecture on "Agrivoltaics: Where Engineers Meet Farmers" by Prof. Santosh Kurinec, Rochester Institute of Technology, USA.

~Soumya Pandit, Editor

Post-event photo with school kids and their teachers on 14 August 2023 in the presence of Prof. K. P. Pradhan, Faculty Advisor of the Chapter, and Chapter Chair Mr. Rameez Raja Shaik.

EDS MEETINGS CALENDAR

The complete EDS Calendar can be found at our web site: http://eds.ieee.org. Please visit.

2024 8th IEEE Electron Devices Technology & Manufacturing Conference (EDTM)	03 Mar - 06 Mar 2024	Bangalore, India
2024 Conference of Science and Technology for Integrated Circuits (CSTIC)	17 Mar – 18 Mar 2024	Shanghai, China
2024 25th International Symposium on Quality Electronic Design (ISQED)	03 Apr – 05 Apr 2024	San Francisco, CA
2024 IEEE International Reliability Physics Symposium (IRPS)	14 Apr – 18 Apr 2024	Grapevine, TX
2024 IEEE 36th International Conference on Microelectronic Test Structures (ICMTS)	15 Apr – 18 Apr 2024	Edinburgh, United Kingdom
2024 International VLSI Symposium on Technology, Systems and Applications (VLSI TSA)	22 Apr – 25 Apr 2024	Hsinchu, Taiwan
2024 Joint International Vacuum Electronics Conference and International Vacuum Electron Sources Conference (IVEC + IVESC)	23 Apr – 25 Apr 2024	Monterey, CA
2024 IEEE Latin American Electron Devices Conference (LAEDC)	02 May – 04 May 2024	Guatemala City, Guatemala
2024 International EOS/ESD Symposium on Design and System (IEDS)	08 May – 10 May 2024	Hangzhou, China
2024 IEEE International Memory Workshop (IMW)	12 May - 15 May 2024	Seoul, Korea (South)

2024 35th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC)	13 May – 16 May 2024	Albany, NY
2024 36th International Symposium on Power Semiconductor Devices and ICs (ISPSD)	02 Jun – 06 Jun 2024	Bremen, Germany
2024 IEEE International Interconnect Technology Conference (IITC)	03 Jun – 06 Jun 2024	San Jose, CA
2024 IEEE 52nd Photovoltaic Specialist Conference (PVSC)	09 Jun – 14 Jun 2024	Seattle, WA
2024 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)	16 Jun – 18 Jun 2024	Washington, DC
2024 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)	16 Jun – 23 Jun 2024	Honolulu, HI
2024 Device Research Conference (DRC)	24 Jun – 26 Jun 2024	College Park, MD
2024 25th International Microwave and Radar Conference (MIKON)	01 Jul – 04 Jul 2024	Wroclaw, Poland
2024 31st International Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD)	02 Jul – 05 Jul 2024	Kyoto, Japan
2024 IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)	15 Jul – 18 Jul 2024	Singapore, Singapore
2024 IEEE International Flexible Electronics Technology Conference (IFETC)	15 Sept – 18 Sept 2024	Bologna, Italy
2024 19th European Microwave Integrated Circuits Conference (EuMIC)	23 Sept – 24 Sept 2024	Paris, France
2024 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)	13 Oct – 16 Oct 2024	Fort Lauderdale, FL

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EDS Vision, Mission and Field of Interest Statements

Vision Statement
Promoting excellence in the field of electron devices for the benefit of humanity.

Mission Statement
To foster professional growth of its members by satisfying their needs for easy access to and exchange of technical information, publishing, education, and technical recognition and enhancing public visibility in the field of Electron Devices.

EDS Field of Interest
The EDS field-of-interest includes all electron and ion based devices, in their classical or quantum states, using environments and materials in their lowest to highest conducting phase, in simple or engineered assembly, interacting with and delivering photo-electronic, electro-magnetic, electromechanical, electro-thermal, and bio-electronic signals. The Society sponsors and reports on education, research, development and manufacturing aspects and is involved in science, theory, engineering, experimentation, simulation, modeling, design, fabrication, interconnection, reliability of such devices and their applications.