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75th Anniversary of the Transistor

History of Naming Non-planar FET Devices

By Digh Hisamoto

Today, with the advent of FinFET, the mainstream of advanced devices has evolved from conventional planar to non-planar structures. Historically, fin devices have paved the way for the development of practical double-gate FET (field-effect transistor) by combining two separate approaches: the study of double-gate mechanisms and non-planar channel structures. The name FinFET is the current industry-standard terminology, but many other names were proposed in the past. I would like to take a bird's-eye view of the history of developing non-planar devices by tracing their names. The narrative is based partly on my own involvement and partly on my understanding of device evolution gathered from numerous patents and papers that I have collected. In some cases, the exact time frames of various inventions might not be precise, but the overall sequence of events should be fairly accurate. First, let us look back on the history of double-gate mechanisms research before the birth of the fin structure.

The first description of a double-gate structure appeared in a patent by Oskar Heil [1]. He is known as the inventor of the FET after Julius Edgar Lilienfeld developed the field effect concept in an earlier patent [2]. A structure in which a thin semiconductor layer is sandwiched between upper and lower gate electrodes is depicted in Heil's patent. It is remarkable that this patent, which was derived from the image of capacitor elements, described the effect of reducing the thicknesses of the gate-insulating film and the semiconductor layer. At that time, the word "transistor" did not even exist, and there is no evidence that the device was given a name.

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History of Naming Non-planar FET Devices

(continued from page 1)

In the 1960s and 1970s, after the invention of various transistors including metal-oxide-semiconductor FETs (MOSFETs), double-gate structures were actively analyzed, and most of the basic ideas still in use today were explored. The term 4-terminal also seems to have been used after the Junction Field Effect Transistor (JFET) along with the double-gate FET [3], [4]. Experimentally, the device structure was realized by depositing multiple thin films on the substrate. Therefore, it seems that it was generally recognized as a thin-film transistor (TFT) [5]. Various semiconductor materials such as amorphous silicon, Cadmium Sulfide, Cadmium Selenide, and Tellurium were studied as semiconductors for the channel. This situation changed significantly around 1980 when the technology for manufacturing Silicon on Insulator (SOI) substrates using ion implantation technology (separation by implanted oxygen: SIMOX) was developed, and SOI devices with silicon single-crystal channels were produced [6]. Although the ideal channel sandwiched by the gates that have been analyzed could not be fabricated, the supporting substrate could be used as a pseudo-gate electrode. Using this approach, the characteristics of double-gate devices with single-crystal semiconductor channels have been experimentally demonstrated [7]. At that time, the term "thin-film SOI" was often used. In the early stages of research using SOI, the name X-MOS was proposed by Toshihiro Sekigawa and Yutaka Hayashi because the shape sandwiched between the gates resembled the Greek capital letter Ξ, corresponding to the letter "X" [8]. Although the name was mentioned in many references, there is no evidence of its widespread use because the structure itself has been widely known for a long time.

Next, looking at research on non-planar channel structures, this field made great progress with the establishment of silicon-substrate etching technology in the second half of the 1960s. It seems that power devices have driven the evolution of non-planar devices rather than large-scale integration (LSI) devices, which have improved the degree of integration through device scaling. It was first formed using the crystal orientation dependence of wet etching, and later dry etching by reactive ion etching was used. Devices fabricated by wet etching are called V-MOS or V-groove MOS due to the characteristic channel shape [9]. To increase the trench density and avoid electric-field concentration at the tip of the V-groove, rectangular trenches were first formed by skillfully using the crystal orientation dependence of wet etching [10]. After that, due to advances in etching technology and interfacial treatment technology, the grooves were formed by dry etching [11]. These are commonly called U-MOS due to their rounded trench-bottom shape [12]. Since UMOS demonstrated that the sides of trenches made perpendicular to the substrate surface can be used as channels, many structures using the sides as channels were proposed in the 1970s and 1980s. The name trench MOS or trench-gate was often used. Power devices require high current-driving capability per unit area, so trench structures were attracting attention as a way to expand the channel width. Initially, there was only one trench, but in order to increase the number of sides, it was considered better to form multiple trenches side by side [13]. By thinning the walls between the trenches, the structure evolved into one consisting of gates from both sides [14], [15]. These structures were also considered as trench MOS and there is no evidence of a different name. However, this idea led to laterally diffused MOS (LDMOS), also known as lateral trench-gate or folded-gate LDMOS [16].

Looking at LSI devices, device scaling progressed in the 1970s, and the short-channel effect became increasingly important. To increase the effective channel length or increase the channel width even if the channel length is the same, the use of trenches was considered as an extension of the planar structure. Those with longer channel lengths are often called grooved-gates, and those with wider channel widths are often referred to as trench gates or folded channels. It has become clear that the trench structure poses serious problems considering LSI devices rather than power devices. Regarding LSI devices supported by planar processing technology, topologically speaking, a trench gate basically has a channel outside the gate. Therefore, when integrating devices, so-called isolation problems such as interference with adjacent devices arise. For example, even if several trenches are arranged in parallel, there will inevitably be a structure that cannot be covered with gates at the outermost periphery or at the bottom of the device. It was clear that integrating multiple devices would cause interference between devices. For this reason, though trench gates were first proposed in the LSI field, pillar gates, in which the gate covers the channel, were later considered. I surmise that this is one of the reasons why Hitoshi Takato and his colleagues named the first pillar-shaped device in LSI the surround gate transistor (SGT) [17]. There was still work to be done to knock down the pillars as with the lateral groove structure, but these studies have set the stage for the emergence of the fin structure.

In the latter half of the 1980s, my collaborators at Hitachi and I developed the first fin-type device on the basis of the idea of making fins by knocking down pillars or thin walls and name it a fully depleted lean-channel transistor or DELTA, imagining the δ-function [18]. I decided on this name because I thought that in addition to the similarity in shape, it would also highlight the fact that it can be isolated from adjacent devices for LSI. I also used the word

"lean" to describe the feature, borrowed from the field of chemistry, where it is a common term that means low concentrations in gases and liquids and used, for example, in lean combustion. Therefore, I decided to adopt the term for the solid phase, although it might have been misused. At that time, the necessity of lowering the channel concentration for device scaling was not widely recognized, so the device name DELTA was adopted to emphasize the necessity of reducing the impurity concentration of the substrate (channel). However, the word DELTA has a stronger image of a triangle than the δ-function, and was not associated with the shape of the device. As a result, the name DELTA did not become very popular.

In the late 1990s, I collaborated with Device Group at UC Berkeley, directed by Professors Jeffrey Bokor, Tsu-Jae King, and Chenming Hu, to demonstrate further miniaturization using fin structures. At that time, we decided to use the name folded-channel for the device from discussions at the group meetings. I have noticed that the thickness of the gate-stack structure becomes a challenge when applying device scaling to the fin structure.

As shown in Fig. 1, the gate is arranged to cover the channel in the fin-type device. Even in DELTA, the first fin-type to use the quarter-micron technology, we can see the gate occupying a large part of the device. Considering the generation with a channel length of 20 nm or less, the fin thickness, gate insulating film thickness, and gate electrode thickness can be expected to be $t_f \simeq 10$ nm, $t_{ox} \simeq 5$ nm, and $t_g \simeq 20$ nm, respectively. In this case, the total width will be 60 nm, which is the sum of the width of the fin and twice the thickness of the gate stack on either side of the fin. This is, of course, much larger than the channel length, and I expected the time would come when device scalability would be dominated by the gate-stack thickness. Therefore, the word "fold", which means bending the gate electrode, carries an important message, so I thought it was not a bad name.

I presented this folded-channel structure at the 1998 IEDM (International Electron Devices Meeting) held in San Francisco [19]. The following year, when we were preparing to submit a manuscript to the IEDM, I was asked by Professor Hu about the name. According to him, at a conference he attended, he heard someone calling the channel of our device a fin and thought about calling it FinFET. I remember agreeing immediately. This is because the moment I heard the word fin, the word Fin that appears in the end roll of French movies that I often watched as a child under the influence of my mother came to my mind, and I thought that this would signify the last FET. Before this, the source-channel-drain structure was sometimes called fin in the Japanese semiconductor community, as it resembles the fins of a fish. However, since it was not alphabetic, it had never occurred to me that fin could be connected to the meaning of "the last". Thus, I told the editor who was in charge of the paper I had already submitted that I wanted to change the device name and the title used in the manuscript, and was able to obtain the editor's approval [20]. At the 1999 IEDM held in Washington, D.C. in December, we reported the device structure for the first time under the name FinFET [21].

These presentations prompted many universities, research institutes, and companies to publish research on FinFET in conferences and journals. Most used the name FinFET, but some used names such as π-gate or Ω-gate [22], [23]. I think the use of Greek letters for these names was a tribute to the name DELTA used in the initial announcement, and I am grateful to them.

At the 2002 SSDM (International Conference on Solid State Devices and Materials), Robert Chau and colleagues of Intel made the first conference presentation using the tri-gate name [24]. I presumed that the reason for using tri-gate instead of FinFET was to show that it was an improvement over the double gate. This naming led to the movement to classify non-planar devices by the number of gates surrounding the channel. They are classified into single gates, double gates, triple (tri) gates, and quadruple gates, and are collectively called multi-gates or MUGFETs. However, I felt a little uncomfortable with this classification and naming. The reason is that the principle of operation is the same even if there are multiple gate electrodes, so I thought it would be more appropriate to use the same terminology. As FinFET evolution proceeded by scaling the fins taller and narrower, resulting in a more fin-like shape, these names fell out of use and converged on FinFET. It became widely accepted because the shape can be easily visualized, thus appropriate. I believe that this naming has had a great effect in revitalizing and advancing device research.

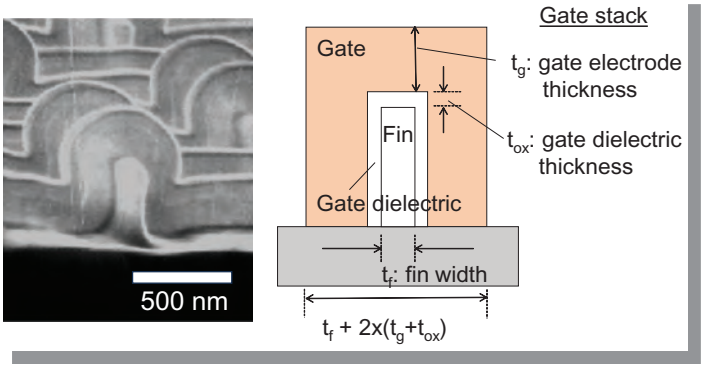

Figure 1. SEM image of the first fin device DELTA (left) and the size of the fin device configuration (right). In the scaled fin-type device, it can be seen that the gate stack structure occupies most of the device.

Gate-all-around (GAA) has been mentioned as the next-generation non-planar structure after the current FinFET. GAA is a long-time name proposed by Jean-Pierre Colinge and his colleagues the year after DELTA was announced [25]. For some time, the name nanowire was more popular than GAA, but it

faded due to problems with the driving current. After that, names such as multi-bridge, nano-sheet, and nano-ribbon have appeared. Currently, GAA seems to be the most commonly used, though the layered structure of the channel is not well described by this name. It is my fervent hope that a more descriptive name will emerge in the near future for the next non-planar FET structure.

At the end of the article, the author would like to thank Dr. Eiji Takeda, Prof. Chenming Hu, Dr. Samar Saha, Prof. Manoj Saxena, and Dr. Daniel Tomaszewski for their valuable support and suggestions regarding the writing of this article.

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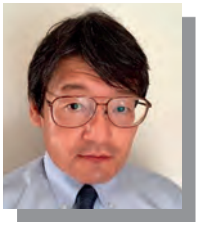
Biography



Digh Hisamoto received the B.S., M.S., and Ph.D. degrees from the University of Tokyo in 1984, 1986, and 2003, respectively. In 1986, he joined Central Research Laboratory, Hitachi, Ltd., Tokyo, where he has been working on ULSI device physics and process technologies. He developed scaled CMOS and memory devices including DELTA, the original model of FinFET. From 1997 to 1998, he was a Visiting Industrial Fellow at the University of California, Berkeley, where he developed the first FinFET. For his achievements, he received the IEEE Andrew S. Grove Award in 2019. He has expanded his research interests into RF devices, tunnel FETs, Non-volatile memory devices, and Power devices using wide bandgap semiconductors. From 2015 to 2019, he was invited as a visiting professor at Tokyo Institute of Technology, where he started the research of quantum devices including quantum sensors with color centers of wide bandgap materials and Si quantum computing devices. He served as a member of the Committee of International Electron Devices Meeting, VLSI Symposium, and International Conference on Solid State Devices and Materials, and an Associate Editor of IEEE Electron Device Letters. He also served as Executive Director of the Japan Society of Applied Physics (JSAP). Dr. Hisamoto is a Fellow of IEEE and JSAP.

The SOI MOSFET

Sorin Cristoloveanu[1], Life Fellow, IEEE

SOI materials and transistors have been developed in parallel with the CMOS technology on bulk silicon. This article reviews, from inside, 60 years of SOI MOSFETs, highlighting the milestones and some of the key actors.

I. The Beginnings

SOI chips have already invaded all our smart-phones and will conquer our Internet things, cars and homes. But the reason why SOI has been invented is elsewhere. The first MOS circuits were badly hurt by the radiation effects. Energetic particles from cosmic rays or human-manufactured rays generate undesirable electron–hole pairs along the transistor thickness which are responsible for leakage currents, charge collection and logic upsets. The only way to alleviate the transient radiation effects was to reduce the thickness of the device to half-micron or less.

60 years ago, while we were listening to The Beatles, the terrifying music of the cold war was orchestrated by Brezhnev. SOS distress signals alerted on the vulnerability of integrated circuits to radiations, and the military ordered: *'Integrate CMOS in a thin silicon layer on top of an insulator.'* Ironically, the first member of the SOI club preserved the acronym SOS: Silicon On Sapphire. Being an expensive technology, SOS was developed with the financial benediction of the defense and aerospace industry. The work by Cullen's group at RCA was most influential.

The heteroepitaxial growth of silicon layers on sapphire substrate is adversely affected by the mismatch of their thermal and crystallographic parameters. Over 50 nm near the Si-Al_2O_3 interface, the crystalline quality was miserable (Fig. 1a). A breakthrough came from the *Solid-phase epitaxial regrowth* (SPER) process. Silicon ions were implanted to render amorphous the Si film, except for a thin surface layer that acted as a seed during subsequent epitaxial regrowth. Additional innovations could achieve 100-nm-thick films with improved carrier mobility and lifetime but made the SOS wafers even more expensive.

In the meantime, the SOS transistor (Fig. 1) revealed promising assets: simple processing, perfect dielectric isolation for latch-up elimination, drastically reduced leakage and parasitic capacitance, enhanced radiation hardness. However, it was long admitted that SOS was not the best option. In the late 70's, its decline was precipitated by the rise of SIMOX (Separation by Implantation of Oxygen) technology.

II. The Renaissance

The synthesis of SIMOX wafers is brutal: deep implantation of enormous amounts of oxygen (≈ $2x10^{18}$ cm^{-2}) to achieve a continuous buried oxide (BOX, Fig. 2a). Despite the astronomic number of dislocations and traps, Katsu Izumi and his team at NTT Labs succeeded in 1978 to fabricate improbable CMOS circuits.

It was the presence of relatively thin Si film (200 nm) and BOX (400 nm) that opened the *back gate*: biasing the substrate enabled the tuning of the threshold voltage, a unique asset of fully-depleted SOI (FD-SOI) transistors. Any SOI device comprises an upside-down MOS structure where the BOX plays the role of gate dielectric. We showed that two probes acting as source and drain are sufficient to operate the pseudo-MOSFET (Ψ-MOSFET), the undisputable method for electrical characterization of SOI materials. This kind of embryonic transistor is what the Three Tenors at the Bell Labs attempted to prove 75 years ago. Since SOI was not imagined yet, they ended up with the bipolar transistor.

The performance of test CMOS circuits on SIMOX was incentive to pursue material developments and design dedicated ion implanters and furnaces. Peter Hemment

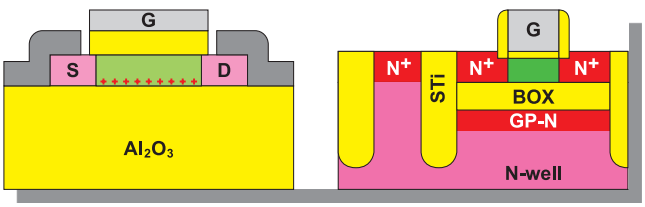


Figure 1. The venerable SOS MOSFET next to its FD-SOI offspring.

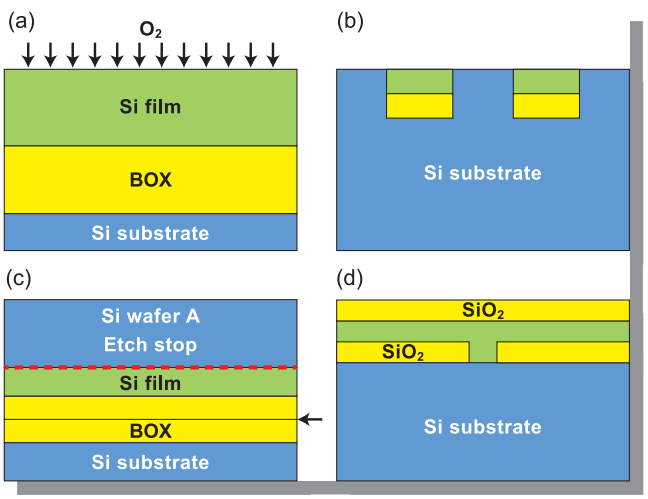


Figure 2. A few SOI variants: (a) SIMOX, (b) localized SOI (via SIMOX and SON), (c) wafer bonding, (d) CELO.

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organized a dynamic European Consortium in competition with American and Japanese organizations. IBIS Corporation brought SIMOX on the marketplace.

During his sabbatical at LETI, Yannis Stoemenos had the *hot* idea of annealing at extremely high temperature (>1300 °C). This cleared the silicon film of crystal defects leaving a sharp Si-SiO_2 interface and a leakage-free BOX. SOITEC Company was founded by A-J. Auberton-Hervé and J-M. Lamure with the initial goal of commercializing this top-quality SIMOX.

SIMOX was handicapped by its long and costly processing, low throughput and rather rigid thickness of film and BOX. The ITOX variant was conceived by Izumi-san's group to lower the implant dose and reduce the layer thickness below 100 nm.

Material magicians uncovered astonishing SOI structures to compete with SIMOX.

Wafer Bonding (WB or BESOI) consists in mating two wafers, at least one of which is oxidized (Fig. 2c). The bonded structure is thinned down by etching and grinding to reach the target thickness of the film. Etch-stop layers (SiGe, porous Si, junctions) are helpful but insufficient for achieving ultrathin layers. WB technology is dedicated to thick power devices and sensors.

Zone Melting Recrystallization (ZMR) starts with the deposition of a polycrystalline Si layer on an oxidized wafer. A heat source (lamps, lasers, beams) is scanned across the surface to erase the grain boundaries and associated defects. The limited extension of the monocrystalline islands is a frustrating issue.

Epitaxial Lateral Overgrowth (ELO) favors the epitaxy of single-crystal silicon through seed windows opened on the oxidized bulk-Si wafer. The growth proceeds laterally and vertically, which implies a thinning step. This inconvenience is eliminated with the ***CELO*** variant of tunnel epitaxy through a confined cavity (Fig. 2d). ELO is fit for 3D integration as it does not require post-growth recrystallization at high temperature.

Full Isolation by Porous Oxidized Silicon (FIPOS) makes use of selected P-doped regions in a N-type wafer which are converted into porous silicon by anodic reaction. Thanks to their huge surface-to-volume ratio, the porous regions are preferentially oxidized to form the BOX.

The 80's was a glorious decade for material science and device physics. The annual IEEE International SOI Conference was not only the grand scene for creativity but also the arena of memorable fights between the gladiators of competing camps. Jerome Lasky, Witek Maszara, Ulrich Gösele and their colleagues pushed the progress in wafer bonding technology. Gerry Neudeck advanced ELO process and demonstrated double-layer SOI devices stacked on top of each other. Atsushi Ogura invented the CELO variant used nowadays to combine Ge, III-V and silicon heterointegration. Jean-Pierre Colinge at CNET and George Celler at Bell Labs were fanatics about ZMR before thinking better.

While bulk-Si CMOS continued its triumphal (and boring) march from node to node, SOI was around to entertain imagination and boost novel concepts, smart characterization techniques and beautiful or lousy devices.

The theory of gate coupling and threshold voltage modulation was elaborated by Jerry Fossum and Hyung-Kyu Lim 40 years ago. After completing his PhD, Lim returned home and could not stop before becoming the boss of Samsung.

An ultrathin SOI film behaves as a quantum well where carrier confinement and subband splitting takes place; Yasuhisa Omura alerted on the inevitable rise in threshold voltage. Dimitris Ioannou was busy with the transient floating-body effects. We revealed the principle of *volume inversion* which stipulates that in a thin body the mobile carriers are no longer confined at the interface. Jean-Pierre Colinge invented the gate-all-around (GAA) MOSFET omnipresent today in nanowire and nanosheet devices. A fascinating three-tier image processor was fabricated at Mitsubishi by Akasaka's team via monolithic integration in 1987, too early for volume production. All these bright guys are very old or worse.

III. The Smart-Cut Reign

In early 90's, too many SOI materials kept competing, which means that none was really convincing. The dilemma was fixed by Michel Bruel from LETI and his genius idea of Smart-Cut. The processing sequence (Fig. 3) consists in transferring a premium-quality silicon layer from wafer *A* to a passive wafer *P*. The magic of Smart-Cut is the ability to detach a nanometer-thick film from wafer *A* using hydrogen implantation as an atomic scalpel (ion cut). Hydrogen ions implanted in wafer *A* generate fine microcavities which result in a mechanically fragile planar zone. Annealing or a mechanical force is used to split the wafers along the hydrogen-weakened zone rather than at the original bonding interface. The microcracks act as a zipper, leaving a well-controlled Si film on wafer *P*. The SOI wafer undergoes surface polishing and annealing to strengthen the bonded interface. The silicon film retains the excellent crystal quality of the high-grade

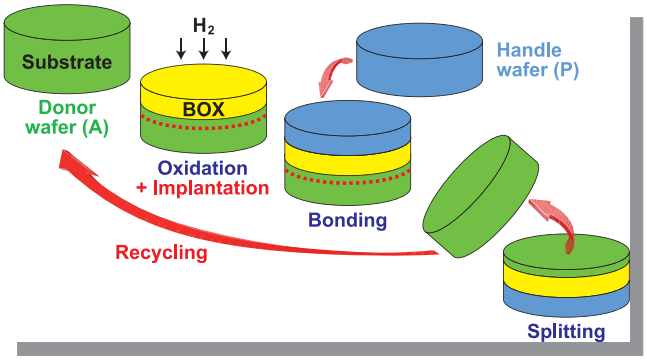

Figure 3. Synthesis of SOI wafer by Smart-Cut.

wafer *A* which is recycled repeatedly; according to the sausage theorem, a slice is cheaper than the whole sausage. The handle wafer serves as mechanical support and is less costly.

Smart-Cut technology provides a full range of thicknesses: Si film from 5 nm to 2 µm and BOX from 5 nm to 5 µm. 5 nm means 200,000 thinner than the initial thickness of the wafer. The film uniformity is amazing: ±4 Å across a 30-cm wafer is like travelling the world without seeing mountains taller than 4 cm. Low defectivity, sharp interfaces and high carrier mobility are other unrivalled assets.

The success of Smart-Cut can be inferred from collateral damage. First, the competition was killed, all other SOI materials left the arena. As of 2023, SOITEC and licensed companies provide the quasi-totality of FD-SOI wafers on the market. Second, in 30 years of sovereignty no new candidate could challenge Smart-Cut:

- Also based on wafer bonding, the *Epitaxial Layer Transfer* (ELTRAN) used a thin porous-Si buffer to define the splitting region. The Si film was grown directly on the porous template. Uniformity and throughput were fatal.

- *Silicon-On-Nothing* is Thomas Skotnicki's SON. Sacrificial SiGe regions are grown on silicon wafer and receive a thin epitaxial Si layer. Selective etching of SiGe leaves cavities (the 'nothing' part of the SON) subsequently filled with oxide (localized SOI, Fig. 2b). SON could not comply with the variability criteria of billion-transistor chips but serves as a building brick for GAA nanowire and nanosheet MOSFETs.

- *Silicon-On-Diamond* for high-temperature circuits had a brief and innocent life.

Smart-Cut is a generic technology able to expand SOI to SOA (Something On Anything) where the mating materials defy the chemistry laws. Silicon can give way to more suitable semiconductors for speed (Ge, SiGe, InGaAs, strained layers), power (SiC by SmartSiC, GaN) or photonic devices. The faithful SiO_2 BOX is replaceable by Al_2O_3, AlN and diamond for mitigating self-heating. Ferroelectrics or silicon nitride promote the BOX from a passive to an active role, enabling nonvolatile buried memory and universal memory.

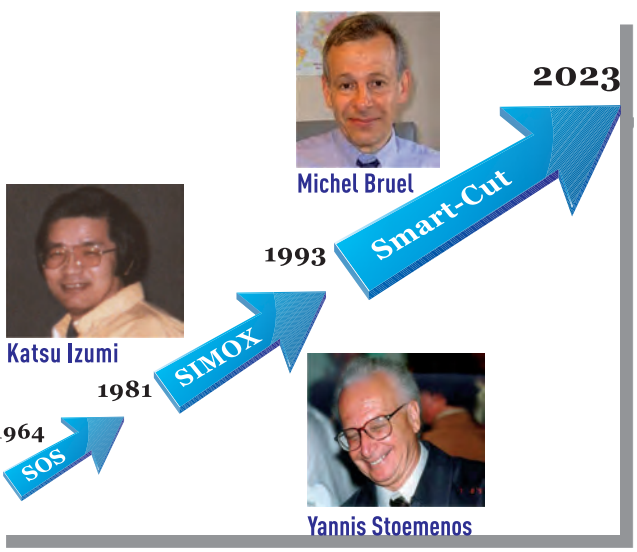

Figure 4. 60 years of SOI.

RF-SOI is a success story originated from a seemingly insane idea of demolishing the quality of the BOX-substrate interface. The trap-rich SOI promoted by Jean-Pierre Raskin is actually a brilliant concept that conquered the RF market. Adding interface traps prevents the activation of a parasitic channel by BOX charges, and preserves the high resistivity of the substrate.

Two recent applications of Smart-Cut attract attention: (i) Piezoelectric-On-Insulator (POI) comprising a $LiTaO_3$ film on high-resistivity substrate and (ii) transfer of layers containing pre-processed circuits from a silicon wafer to another substrate (3D integration, RF devices). Albeit Smart-Cut encouraged new materials to bond together, the divorce of the old couple, silicon and silicon-oxide, is seemingly impossible. Figure 4 summarizes the SOI story over the past 60 years.

IV. SOI Transistors

Partially-depleted (PD) MOSFETs won the first set but finally lost the game against their fully-depleted (FD) cousins. Ghavan Shahidi pushed at IBM the adoption of PD-SOI for performance/power/area advantages over bulk-Si CMOS. Lower power for equivalent performance, or higher speed at same biasing were solid arguments. PD-SOI processors became available on the marketplace in 1995. AMD and Global Foundries followed in 2001 with high-end power-PC micro-processors. This route could not continue indefinitely for the limits of downscaling are similar in PD-SOI and bulk-Si MOSFETs whereas fully-depleted devices are well] equipped. Electrostatic considerations led Konrad Young define an *intrinsic* length, function of film thickness. A thumb-rule stipulates that a Si layer of thickness t_{si} can accommodate FD-SOI MOSFETs with a minimum length of $L = 4t_{si}$. Smart-Cut enabled thinner and shorter transistors. Imagine a cargo crossing an ocean just a few meters deep. Without waves or tsunamis, the cargo moves faster with reduced consumption. This is exactly what happens in ultrathin SOI transistors where the electrons are more mobile and most parasitic effects are suppressed.

A peculiar short-channel effect in FD-SOI transistor is the penetration of the electric field from source and drain into the body via the BOX. The fringing field reduces the threshold voltage and contributes to DIBL (drain-induced barrier lowering). This is why a thin BOX (< 20 nm) is unavoidable for further downscaling.

A state-of-the-art FD-SOI transistor (Fig. 1b) features 6 nm film and 20 nm BOX. The body is undoped and there is no need of halos, pockets or LDD regions. A highly-doped

ground-plane underneath the BOX serves as back gate. The source and drain are raised by epitaxial regrowth with *in-situ* doping to minimize the series resistance. Each transistor is isolated from the next one by STI. 90% of the process modules, including the gate stack, are imported from bulk-Si CMOS. The duplication of such a transistor by sort of copy-and-paste process is the foundation of the monolithic integration of 3D circuits.

Around the turn of the millennium, many research groups joined the SOI family. Francisco Gamiz developed Monte-Carlo-in-Granada simulations, in competition with his dear friends from Udine (Luca Selmi and David Esseni). Ron Schrimpf and colleagues in Vanderbilt focused on the permanent effects of cumulated radiation dose. Gérard Ghibaudo (Grenoble), Babis Dimitriadis (Thessaloniki) and Cor Claeys (IMEC) enriched knowledge in noise and specialized characterization methods. Joao-Antonio Martino built an enthusiastic team at the University of São Paulo. Outstanding contributions came from the groups led by Shinichi Takagi and Toshiro Hiramoto at the University of Tokyo, by Jong-Ho Lee at Seoul National University, and by Tamara Rudenko at the Academy of Science in Ukraine. How can I list all who would deserve it?

Stunning device concepts fueled by FD-SOI came out since 2010. Colinge invented the junctionless MOSFET with mandatory ultrathin body. We demonstrated the four-gate MOS transistor, where each gate can independently turn on and off the current. A number of capacitorless DRAM variants use the MOSFET to store and read information. Band-modulation devices, electrostatic doping and tunneling FETs all take advantage of ultrathin SOI films.

Inspired from several SOI workshops organized in Grenoble, the annual EuroSOI conference has formally been initiated 20 years ago in Granada. It is sponsored by IEEE and travels around Europe, attracting specialists from all continents. Alexei Nazarov organized sister SOI workshops in Ukraine. Carlos Mazuré, aided by Bich-Yen Nguyen and Ionut Radu, put together the SOI Industry Consortium where designers and technologists have started to talk to each other.

Global Foundries, IBM, STMicroelectronics and some Japanese sumos acquired expertise and ambitions in FD-SOI circuits. Technology modules, models and design libraries were elaborated to conquer the market. Everyone expected FD-SOI to replace the dying bulk-Si CMOS before 2010. Conservative management delayed the switch, letting Intel to make a big surprise by introducing their FinFETs, soon adopted by major companies. This is how FD-SOI missed the chance to be a premier technology.

However, SOI did not give up and today the market is booming. It is the technology for low-power, IOT and AI circuits, RF and reconfigurable devices. Many emerging devices wouldn't have been discovered had SOI not been around. Band-modulation and electrostatic doping are powerful concepts unknown 20 years ago.

V. Special Mechanisms in FD-SOI MOSFET

An FD-SOI transistor is a perfectly isolated nano-box which accommodates unusual effects our dear 75-year-old MOS patriarch never heard of. The following is a homeopathic introduction.

Interface Coupling–The properties of one channel depend on the quality and biasing of the opposite interface. The primary application is the tuning of the threshold voltage V_T via the back gate. For 200 mV shift in V_T the OFF current and standby power are reduced by three orders of magnitude. Only FD-SOI transistors can enjoy this capability which is instrumental in low-voltage, low-power circuits.

Supercoupling–The coexistence of electron and hole channels facing each other is denied in films thinner than 10 nm. Supercoupling inhibits the floating-body effects but causes bilayer devices (single-transistor DRAM and TFET) to fail.

Electrostatic Doping–Volume inversion and accumulation enable the carrier spreading in the whole body. Such gate-induced doping behaves in many respects as a chemical doping with the additional merit of reconfigurability. The possibility to emulate P-N junctions in a fully-depleted body just by adding gates has fascinating applications (virtual diode, undoped Esaki diode, band-modulation devices).

Thickness Effects–The carrier mobility is hardly affected by film thinning. Only below 3 nm does the mobility drop due to surface roughness. The energy quantization induces interesting transport and electrostatic properties.

VI. Next

Nanoelectronic devices have more impact on our society than politics and religions. Whether this is wonderful or devastating does not really matter; progress is ineluctable to satisfy the exponential demand. However, challenges are tough at several levels: technological, financial, societal and even geopolitical.

Nobody could predict, 60 years ago, the adventurous story of SOI technology. I believed in SOI for almost 50 years, a few more will not hurt. There is no doubt that SOI will be there for the celebration of the 150th anniversary of the transistor.

Acknowledgements. An enriched version of this article will appear on the commemorative volume, 75th Anniversary of the Transistor, IEEE Press-Wiley, 2023. Details and references are also available in recent books:

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Evolution of Surface-Potential-Based Compact Modeling

M. Miura-Mattausch, T. Iizuka, H. Kikuchihara, H. J. Mattausch, and S. Saha

Conventionally, a compact model of an electronic device is developed for utilization in circuit simulation. This means that the main task of the compact model is to accurately describe the characteristics of a device as a function of the applied voltages by simple equations in order to predict the performance of circuits using this device with sufficient precision. This overview article focuses on the compact modeling of the metal-oxide-semiconductor field-effect transistor (MOSFET)-device structure, which has the largest variety of applications. However, the modeling methodology is valid for any type of transistor or electronic device.

Shortly after the transistor invention, Shockley developed the well-known *pn* junction current-voltage equation [1]. The underlying physics and assumptions can be found in most semiconductor textbooks (e.g. [2]), describing the control of the current by an applied bias. The electrostatics of the *pn* junction is characterized by the Poisson equation, which describes the relationship between the potential distribution and the charges within the *pn* junction (see Fig. 1). Based on the Poisson and continuity equations for electrons and holes, with appropriate boundary conditions, the current-voltage relationship can be obtained.

Shockley's modeling concept has been extended to MOSFET devices by Pao and Sah in 1966 [3]. Aside from using a gate voltage (V_{gs}) induced electric field to control the current in a direction perpendicular to the field, known as the field effect [4], the main difference is that the carriers in the MOSFET are confined within a potential well at and near the semiconductor surface. The drain voltage (V_{ds}) is applied to enable the carrier flow into the drain from the source according to the potential gradient (see Fig. 2). Pao & Sah solved the Poisson equation in two dimensions, the well depth direction *x* and the channel direction *y*. Consequently, the solution of the Poisson equation is reduced into a two-dimensional (2D) potential distribution. Previously, Sah has focused only on the strong-inversion condition, where the potential distribution along the channel can be drastically simplified, and derived a simple analytical equation for the drain current I_{ds} as [5]

$$I_{ds} = \mu \frac{W}{L} C_{ox} \left[(V_{gs} - V_{th}) V_{ds} - \frac{1}{2} V_{ds}^2 \right] \quad (1)$$

Here, μ is the carrier mobility and the threshold voltage V_{th} is the V_{gs} value needed to form the channel at the onset of strong inversion. This equation was commonly used in compact analytical modeling of MOSFETs for circuit simulation.

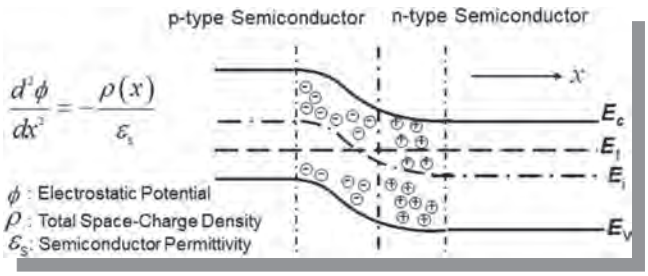

Figure 1. Potential distribution along the p/n *junction as the solution of the Poisson equation.*

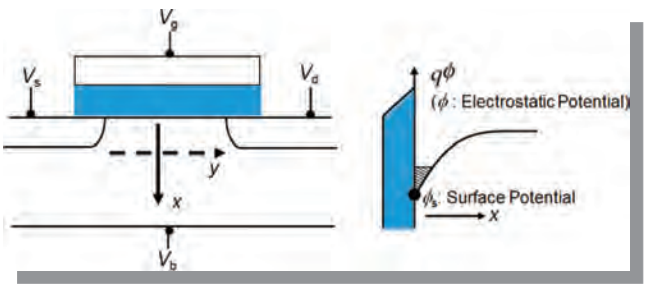

Figure 2. MOSFET structure schematic together with the potential φ distribution in the x direction.

1. Circuit-Simulation Model

The equivalent-circuit model for the MOSFET, developed by Meyer, is shown in Fig. 3 in a simple way [6]. A compact model provides equations for all elements in the equivalent circuit model. The current is an integration of the carrier density multiplied by velocity from source to drain. The capacitances are the derivatives of charges induced on the transistor nodes (V_s, V_g, V_d, and V_b). As the current equation, the Sah equation is taken and the analytical charge equations are derived in the same manner as I_{ds}. Equations for subthreshold and saturation conditions are written phenomenologically to enable the completion of the switching-performance simulation.

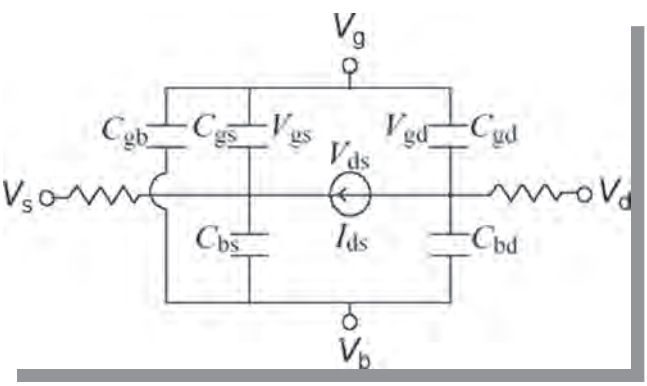

Figure 3. Equivalent MOSFET circuit proposed by Meyer.

The basic transistor equations are derived on the basis of the Maxwell equations, where the potential φ is a function of position within the transistor. Instead of solving the Poisson equation, the potential values at the source and drain side are fixed to $\varphi=2\Phi_B$ and $\varphi=2\Phi_B+V_{ds}$, respectively, where $\Phi_B=kT/q\ \ln(N_{sub}/n_i)$ [5]. Since the SPICE (Simulation Program with Integrated Circuit Emphasis) circuit simulator was developed at UC Berkeley in an early stage during the 1970s and provided for public usage [7], circuit simulation has become a powerful method for circuit development.

2. V_{th}-Based Compact Model

The V_{th}-based model development was completed as BSIM4 [8] at the beginning of this millennium under the support of the CMC (Compact Model Council) [9], and has been widely used for circuit design. Singularities in modeled derivatives of device characteristics, caused by the piece-wise modeling approach, have been removed by smoothing functions. Thereafter, the V_{th}-based modeling method became the mainstream in the compact-modeling community. However, shortcomings of the applied simplifications, considering the strong-inversion condition, became obvious as technology advanced further. Subthreshold characteristics give rise to important technological features that must be considered. Thus, to have a physics-based analytical model for the subthreshold region, as well as a smooth continuous transition to the strong-inversion region, became essential. Due to the parameters introduced through smoothing functions, the connection between the model parameters and the measured device parameters became more tenuous, necessitating further improvements in the modeling approach.

3. Surface-Potential-Based Compact Model

In the 1970s, since CMOS technology became ready for circuit applications with low power [10], the development of large-scale integrated circuits became the mainstream. Further, the transistor-size reduction was accompanied by a bias reduction, requiring good V_{th} control. Here, the importance of the Poisson equation-based modeling has been raised again due to its validity for all bias conditions and its physical correctness. Three investigations have been published nearly at the same time [11], [12], [13]. The main improvement was the introduction of the charge-sheet approximation [11], which reduces the Pao-Sah's double integrals into one, only in the channel direction, while neglecting the carrier density variation in the channel-depth direction, since the space-charge density variation in that direction is negligible in comparison to that along the channel length. Thus, only the surface-potential distribution along the channel is considered. The short-channel effect, accompanying the size reduction, was the next phenomenon to be modeled. This has been done by considering the lateral electric field in the Poisson equation analytically [14]. The first complete model for advanced technologies was developed at Siemens in the early 1990s, which then has been further developed and named HiSIM [15]. This model solves the Poisson equation iteratively to avoid any approximations with a good initial guess and preserves the smoothness of the higher-order derivatives of physical quantities. The Poisson equation is solved only two (2) times (at the source side and at the drain side) for describing potential distribution within the transistor. The calculated potential values are used to determine all charges and currents induced within the semiconductor. It has been demonstrated that the circuit simulation time could be even reduced with a simplified source code due to the simple model description. A big advantage of potential-based modeling is that the meaning of most model parameters coincides with corresponding technological device parameters. The predictability of the HiSIM compact model is demonstrated in Fig. 4 [16].

A major challenge was to develop a thin-layer MOSFET model for devices composed of different layers, where not only the surface potential but the entire potential distribution within different layers must be solved (see Fig. 5 [17]). It has been demonstrated that compact modeling by solving the Poisson equation iteratively is suitable even for such cases as MG-MOSFETs and GAA-MOSFETs, e. g. [18]. Due to the CMC leadership, the movement of compact models from V_{th}-based to potential-based modeling has been accelerated, though the mainstream of potential-based modeling is still using analytical solutions of the Poisson equation [19]. However, it has been slowly accepted, that deriving an analytical description for calculating

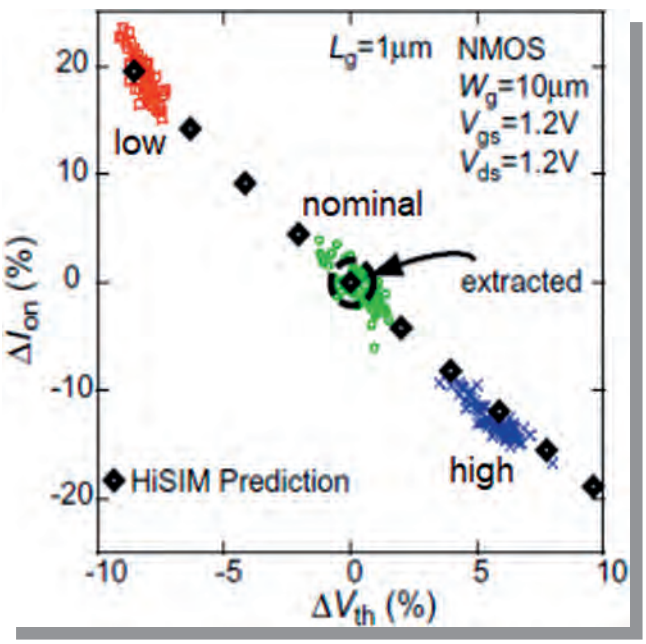

Figure 4. Reliability test of the developed model for three different wafers with different impurity concentrations, where only the nominal-device data has been used for the model, and only the impurity concentration was changed for low and high cases. Black diamonds are the model predictions.

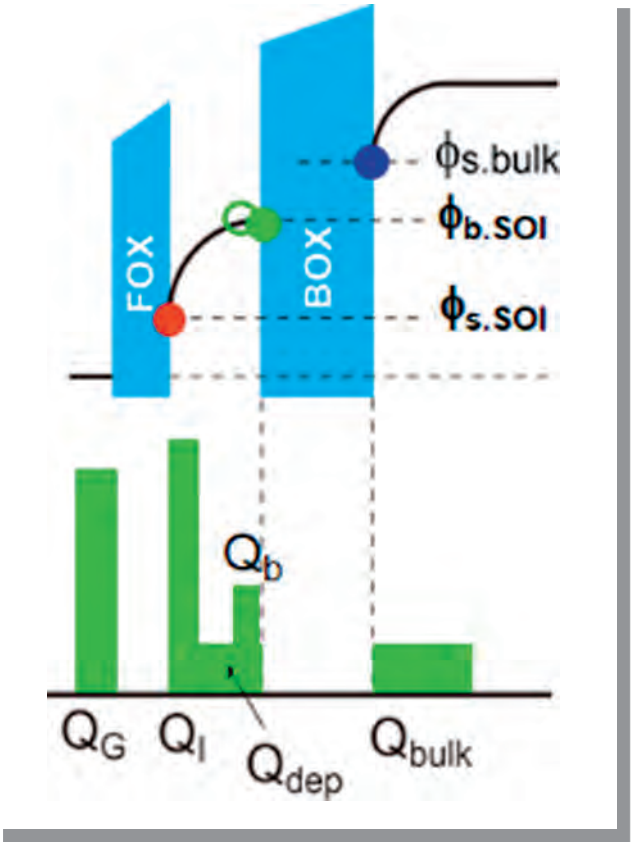

Figure 5. Schematic of thin-layer MOSFET and its potential distribution vertical to the surface.

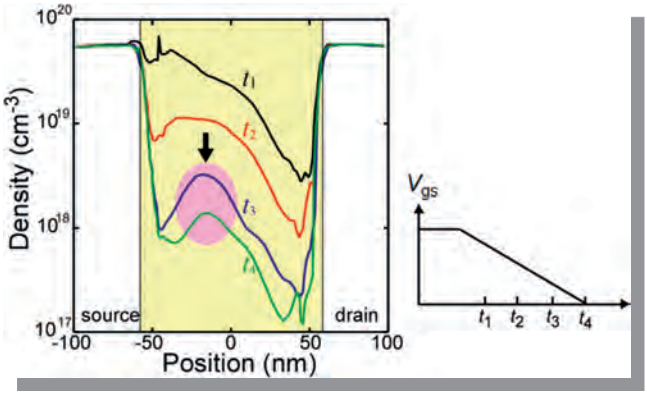

Figure 6. 2D numerical device simulation of the carrier-density distribution within the MOSFET channel. The transit delay is obvious in the middle of the channel.

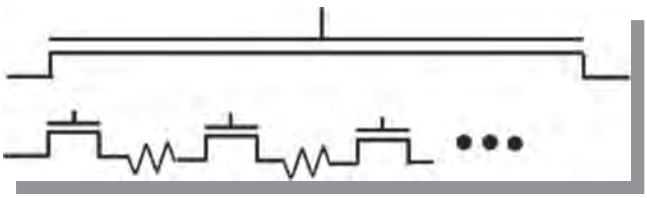

Figure 7. Elmore channel-segmentation model for the carrier-transit delay.

the potential values requires several simplifications, which may bring problems for accurate modeling of advanced technologies.

3.1. NQS Effect

In the beginning of the 1990s, internet technology (IT) development emerged throughout the world, requiring high-speed MOSFETs to realize monolithic integration of different circuit functions. The carrier transit delay with respect to bias changes limits the transistor's cut-off frequency (f_T) improvement [20]. Therefore, a new task was to model the carrier-transit-delay effect, which is basically determined by the carrier mobility. During switching on and -off, carriers don't appear and disappear immediately along with the switching waveform. This phenomenon is called the Non-Quasi-Static (NQS) effect caused by the carrier-transit delay (see Fig. 6 [21]). Resistances and capacitances induced within a transistor influence this delay too. Therefore, the delay has been modeled originally by dividing the channel into several segments and by stacking resistances between these segments, as shown in Fig. 7 [22]. However, such a modeling approach increases circuit simulation time drastically. A more reasonable approach considers the carrier-transit time, which is required to complete the movement within the transistor, explicitly. If the transit time is longer than the switching time, only a part of the carriers can complete this action [23]. Thus, a reduced amount of charge is considered in the Poisson equation, resulting in a reduction of the potential values at the same bias condition. The resulting NQS model for RF performances has been verified with measurements, as shown in Fig. 8 [24].

3.2. High-voltage (HV) Modeling with an Internal Node

The MOSFET has been extended for high-voltage (HV) applications by introducing long resistive drift regions to sustain the applied high voltage (see Fig. 9) [25]. In the early stage of the compact model development, HV-MOSFET models consisted of a conventional MOSFET and a resistance, called a macro-model. The disadvantage of this modeling approach is the complication of the model parameter extraction. And, instability in circuit simulation has also been reported. Thus, a new modeling approach has been proposed by introducing an internal node explicitly between the intrinsic MOSFET and the resistive drift region [26]. The potential distribution is solved from the source to the internal node and from the internal node to the drain contact by a circuit simulator. The calculated results of the potential characteristics are depicted together in Fig. 9.

HV-MOSFETs have been realized not only by introducing a long resistive region but also by structural modifications such as planar or trench structures. By combining a MOSFET with a bipolar transistor, the IGBT has been invented [27], which has realized bias ranges up to a thousand volts even

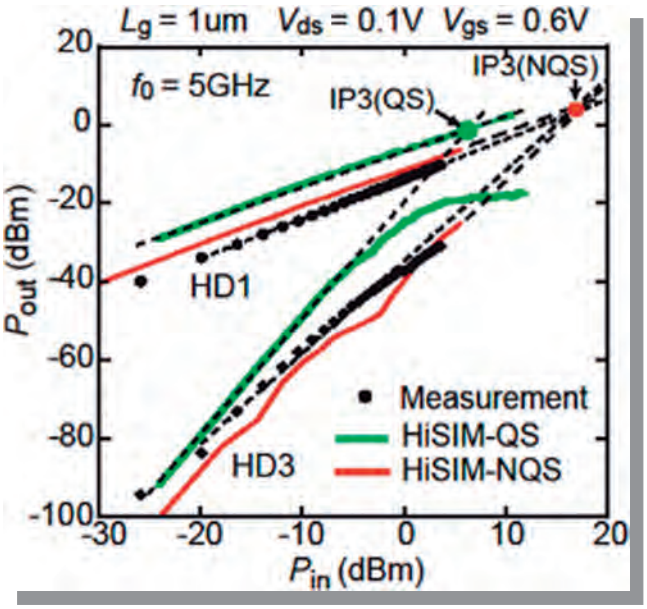

Figure 8. HiSIM-model-calculation results for harmonic distortions with/without the NQS effect in comparison to measurements.

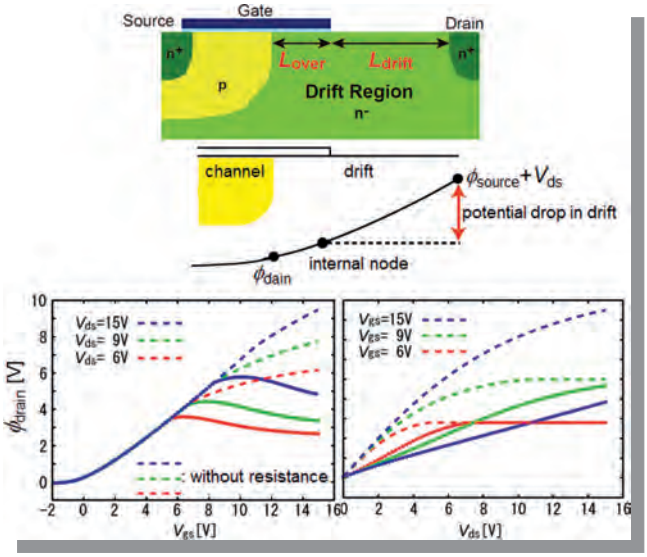

Figure 9. Schematic of a high-voltage MOSFET (LDMOS) (top) and its potential distribution (middle) together with potential values with (bottom left) / without (bottom right) the drift-resistance contribution.

with Si-based technologies. The main modeling difficulty is that the potential drop, induced within the overlapping region of the MOSFETs drift region and the bipolar base, is strongly influenced by the IGBT structure and the bias conditions. It has been demonstrated that consistent and accurate compact modeling is possible by introducing an additional internal node, which is solved iteratively again by the circuit simulator [28]. Thus, compact modeling is entering into a new era, getting more freedom with the use of internal nodes, solved by a circuit simulator. Self-heating-effect models are also a mandatory requirement for power devices.

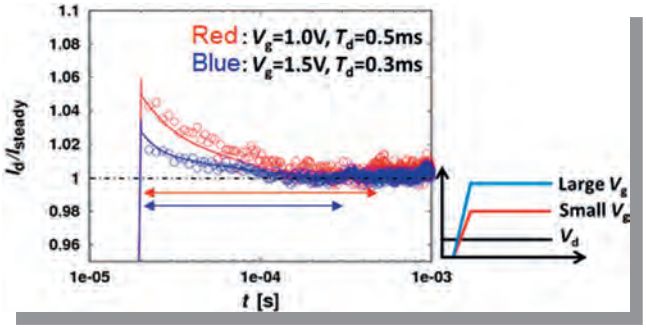

Figure 10. Measured trapping-time constant T_d from switching-on characteristics under two different bias conditions.

3.3. Trap Model

The Poisson equation includes all charges induced within the semiconductor, and thus the entire potential distribution along the transistor depth direction is required to calculate charges. Trap charges can be induced during circuit operation as well as device fabrication. Carriers are trapped/detrapped by crystal defects mostly at the insulator/semiconductor interface. A trap increase is known as the origin of circuit degradation [29]. The physical quantity, determining the easiness of carriers to be trapped, is the capture cross section σ. In compact modeling, σ is macroscopically modeled by the time constant T_d, which is written with σ as follows [30]

$$T_d[s] = \frac{A}{n[\mathrm{cm}^{-3}] \cdot v_{\mathrm{th},n}[\mathrm{cm}/s] \cdot \sigma[\mathrm{cm}^2]} \quad (2)$$

n: Carrier Density — σ: Capture Cross Section
$v_{\mathrm{th},n}$: Thermal Velocity — A: Trapping Coefficient

4. Compact Model vs. TCAD

The first technology CAD program (called TCAD by Dutton [31]) was developed by Scharfetter and Gummel [32] in 1969. The breakthrough invention was the discretization within the device to solve the potential distribution numerically. The concept has been further developed to solve the basic equations numerically in two dimensions (x and y) or even in three dimensions (x, y, and z). Instead of solving numerically, a compact model derives simplified equations by integrating the distribution from source to drain, to obtain quantities suitable for compact models at transistor nodes. Macroscopic quantities, mainly obtained from measurements, reflect the node potential conditions. Predicting the switching performance accurately is not an easy task, because characteristics of a real transistor demonstrate many discrepancies compared with the compact model of the ideal device. By investigating the target circuit, however, model deficits, which prevent from an accurate circuit-performance prediction, become often clear. For such a deficit case, a TCAD investigation is carried out to find the underlying reason. Since the basic equations are the same for the two methods of TCAD and compact modeling, the model parameter dependencies of the device characteristics must preserve those of the TCAD results.

5. Verilog-A Language

The compact-model equations must be implemented in the circuit simulator, which should provide an interface for this purpose. At an early stage of the model development, nevertheless, this implementation was a tough task for the model developers. The Verilog-A language has been originally developed for analog circuit designers to verify or design their own analog model equations to achieve their specific modeling tasks. In parallel, the Verilog-A language has been extended for compact-model developers as an alternative language to C-Code [33]. A big advantage of the Verilog-A code is that derivatives are numerically solved within the simulators. The Verilog-A description has been further extended for compact-model developers to support the easy implementation of quite complicated model constructions into commercial circuit simulators, providing model developers with more freedom in their development framework. Additionally, new solution-algorithm developments of circuit simulators have improved drastically the simulation time as well as the model calculation stability.

6. Circuit Design Perspectives

On the circuit level, the compact models have mainly two application areas. The first is the design of analog and RF circuits. The second is the development of elementary digital circuit cells and macro-circuit blocks for industrial design libraries, which are then used by higher-level design and verification software, to compose the complete circuits for different application tasks [34]. The preserved physical relationships between the actual device parameters and the parameters of potential-based models allow the circuit designers to better understand the effects of technology changes on the performance characteristics of the designed circuits. It further facilitates the simulation of statistical technology variations and aging effects on their designed circuits. Even though the simulation speed remains a major consideration for the characterization of the design-library cells, it is the model accuracy, which has become the most important for both analog and digital circuit design. In particular for advanced technologies, with device-structure sizes reaching below 10 nm, simple digital cells such as inverters or 2-input logical cells start to show strong analog features, requiring accurate compact models for more accurate characterization. The surface-potential compact models now have run-time speeds comparable to V_{th}-based models [35], so that they have become the mainstream in compact-model development and practical applications [9].

7. Summary

The development of the compact modeling approach, based on the potential distribution induced within a transistor, is reviewed. The purpose of a compact model is to describe the transistor characteristics in a simple but accurate way, to enable correct circuit-performance prediction. Therefore, the basic physics of observed phenomena must be modeled by simplified and yet physically correct equations. To meet such requirements, potential-based modeling is a natural fit. A compact model and TCAD are both based on the same transistor equations. The difference is that TCAD considers the distribution of all physical quantities within a device, and a compact model integrates these distributions to calculate transistor characteristics at its nodes. The shortcomings of resulting simplifications, introduced for analytical integration, can be examined using TCAD, to identify observed phenomena still missing in the compact modeling. In this way, compact modeling is performed by learning from measurements macroscopically and from TCAD microscopically.

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2023 VLSI Symposium

The Symposium on VLSI Technology & Circuits was held at Rihga Royal Hotel Kyoto from June 11–16, 2023 in Kyoto, Japan around the theme: "Technology & Circuits for the Critical Infrastructure of the Future." The Symposium featured advanced VLSI technology developments, innovative circuit design, and the applications they enable, such as artificial intelligence (AI), machine learning, internet of things (IoT), wearable/implantable biomedical applications, big data, cloud/edge computing, virtual reality (VR)/augmented reality (AR), robotics, and autonomous vehicles. More than 1600 people attended the Symposium with a record number of attendees.

The weeklong Symposium continued its reputation as the microelectronics industry's premiere international conference integrating technology, circuits, and systems with a range and scope unlike any other conference. In addition to the technical presentations, the Symposium program featured a demonstration session, evening panel discussions, joint focus sessions, short courses, workshops, and a special forum session that provided a focused discussion on a specific topic relevant to the Symposium theme.

Plenary Sessions:

- **"Multi-Chiplet Heterogeneous Integration Packaging for Semiconductor System Scaling" by Suraya Bhattacharya, Director, System-in-Package, A*STAR, IME**–Over the past decade, the diverse system requirements from wide ranging markets have driven the industry to use heterogeneous integration of multiple chiplets enabled by advanced packaging as a key new toolbox for System-in-Package scaling. The director of A*STARI, IME provided an overview of multi-chiplet heterogeneous integration (MCHI) packaging platforms to address system scaling needs in coming decades.
- **"Searching for Nonlinearity: Scaling Limits in NAND Flash" by Siva Sivaram, President, Western Digital**–In this talk, the WD President showed that as NAND Flash moves into a mature era of 3D scaling using only increasing layer count results in a sub-linear cost reduction while producing higher bit growth. Wafer bonding technology allows for decoupling the memory array from complex logic circuits, allowing new high speed logic integration with the memory layers, and simplifying manufacturing cycle times. This technology also allows the industry to move away from a one-size-fits-all NAND die to customized solutions for various applications and system level savings.
- **"Quantum Computing from Hype to Game Changer" by Hiroyuki Mizuno, Distinguished Researcher, Hitachi, Ltd.**–Quantum computing is increasingly considered hype as its benefit to the consumer remains unrealized despite widespread investment and investigation. CMOS annealing technology attempts to provide a stop gap solution. In this talk, Dr. Mizuno introduced the top-down approach that takes full advantage of existing semiconductor technologies and notable developments including the "shuttling qubit" to reach the next milestone to develop silicon quantum computers–qubit operation in a scalable qubit array structure.
- **"A New Era of Hardware: AI-driven, Software-defined, and Uncomfortably Exciting" by Partha Ranganathan, Vice President, Technical Fellow, Google** – The AI revolution, cloud, and smart edge are all accelerating the demand for computing, yet Moore's Law is slowing down. This is constantly challenging traditional assumptions around cheaper and more energy-efficient systems and resulting in a significant and growing supply-demand gap for future computing systems. In this talk, Dr. Ranganathan discussed how to rethink and design future hardware and presented two broad themes–efficient hardware design through custom silicon accelerators and efficient hardware utilization through software-defined systems design.

Focus Sessions

Two technology focus sessions were held on "BEOL Interconnects and BPD/BSPDN" and "More novel memory devices to continue scaling". In addition, there were four joint focus sessions on "New Computing", "AR/VR/MR/Metaverse and its Integration", "Aerospace and Automotive Applications", and "3D packaging technology and system integration", where papers with both circuits and technology novelty & interest were presented.

Short Courses on Key VLSI topics

Two full-day short courses were featured:

- The Short Course 1 "Advanced CMOS technologies for 1 nm & beyond" focused on novel logic technologies with coverage of FEOL/BEOL processes including EUV lithography, device evolution from Si to novel 2D materials, 3D integration from backside

power delivery network (PDN) and heterogeneous integration, and future metrology for production.
- In the Short Course 2 "*Future Directions in High-Speed Wireline and Optical IO,*" industry experts delved into the latest advancements in SerDes circuit system design, coherent ASICs, and silicon photonics. State-of-the-art chiplet technology, innovative packaging, high-speed receivers and transmitters, and memory interfaces were covered as well.

Forum Session

The Symposium program also featured a multi-speaker full day Forum Session on "Compute Paradigms for Secured Microelectronics and Combinatorial Optimization".

The VLSI Forum is devoted to topics that extend the scope of the Symposia by suggesting the future direction of VLSI Symposium, or by showing the emerging cutting-edge applications of VLSI. Top expert speakers are invited from all over the world to contribute to this forum. This year we focused on secured microelectronics and combinatorial optimization, covering hardware security, cryptographic circuit technology, cyber security, as well as combinatorial optimization accelerators based on processor, FPGA, and superconducting quantum annealer.

In addition, two **Evening Panel Sessions** were held:

- *"What is scalable & sustainable in the next 25 years?"*

  Technology node scaling has been successful for many decades with the evolutions in lithography, materials, and device structure, but how about in the next 25 years? How can we overcome the limits of scaling in Physics, Manufacturability, Economy, Energy in chip operation, Energy in manufacturing, Greenhouse gas emissions in manufacturing, and Engineering resources. Can our industry continue to be attractive to grow further? Dr. Tomonari Yamamoto from TEL moderated a panel of distinguished guests from across industry and R&D organizations to offer their valuable insights and thoughts, and share their experience with attendees.
- *"Can Universities Help to Revitalize the IC Design Industry? If so, how?"*

  Chips are becoming commodities, and the semiconductor industry is now reinventing itself. In this climate, can universities contribute to the revitalization of chip companies? Is it possible to form mutually beneficial relationships? Or will university researchers continue to focus only on what they want to do and companies will continue to look to universities only as a source of educated employees? Prof. Asad Abidi from University of California, Los Angeles moderated a panel of distinguished guests from across the industry and academia to offer their valuable insights and explore this important topic.

Demonstration Session

From this year, the demonstration session was fully operated in-person, providing participants an opportunity for in-depth interaction with authors of selected papers from both Technology and Circuits sessions. These demonstrations through table-top presentations showed device characterization, chip operational results, and potential applications for circuit-level innovations.

Workshops

A series of workshop sessions were held during the Symposium program to provide additional learning opportunities for participants. This year, we were pleased to announce six exciting workshops:

Technology Workshops

- EUV lithography & path to high NA EUV patterning solutions
- Towards Functional Backside: What's next after Backside Power Delivery?
- The Deployment of Materials to System Co-Optimization Methodology (MSCO™) to Enable Rapid PPACt Assessment for Advanced Node Technology Development

Circuit Workshops

- Uniform and Rigorous Benchmarking of Machine Learning ICs and Systems
- 3D image sensor
- Open Source PDKs and EDAs, community experiences toward democratization of chip design

Special events at the Symposium were held including mentoring events for Women in Engineering and Young Professionals, sponsored by the IEEE Electron Devices Society and the Solid State Circuits Society.

Best Student Paper Awards for each track Symposium were chosen based on the quality of the papers and presentations. The recipients received a monetary award, travel cost support, and a certificate. For a paper to be reviewed for this award, the lead author and presenter of the paper must be enrolled as a full-time student at the time of submission, and must indicate on the web submission form that the paper is a student paper.

Sponsoring Organizations

The IEEE VLSI Symposium on Technology & Circuits is sponsored by Japan Society of Applied Physics, the IEEE Electron Devices Society, the IEEE Solid State Circuits Society, and in cooperation with the Institute of Electronics, Information and Communication Engineers.

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Publicity Chair of the 2023 VLSI Symposium

2023 IEEE International Memory Workshop (IMW)

By Dirk Wouters

The 15th International Memory Workshop (IMW) took place at the Hyatt Regency Hotel in Monterey, CA, on 21–24 May 2023. After the entirely virtual 2020 and 2021 editions, and the hybrid 2022 edition held in Dresden, this year's IMW was the first on-site only after the COVID-19 pandemic, returning to the true interactive Workshop format.

The IMW is sponsored by the IEEE Electron Devices Society and meets annually in May. The workshop is a unique forum for specialists in all aspects of semiconductor memories (non-volatile & volatile). The scope of workshop content ranges from new memory concepts in early research to the technology drivers currently in volume production as well as emerging technologies in development. The technical sessions are organized in a manner that provides ample time for informal exchanges among presenters and attendees. More than 150 people took part in our meeting this year.

This year's program included a one-day short course, with tutorials on TCAD and Modeling and on DNA memory, delivered by experts on the topics from both the industry and academia. The technical program for the single-track conference spanned three days and opened with keynote talks by Alessandro Grosso (Infineon) on RRAM technology for automotive, Jeongdong Choe (TechInsights) on the status of STT-MRAM technology, and Sunil Sim (Samsung) on 3D NAND Flash.

The program included invited talks given by experts in the memory field– Wei-Chen Chen (Macronix), Konrad Seidel (Fraunhofer), Biswajit Ray (Univ. Alabama), Antonio Conte (ST Microelectronics), Bhagwati Prasad (Indian Institute of Science Bangalore), Sebastian Couet (imec), and Bala Haran (Applied Materials)-providing an exciting overview of the main trends for memory technologies and applications.

The IMW is also an excellent forum to present new and original technical works and this year's technical program comprised 31 excellent papers, which included 17 oral presentations and 14 posters. The papers were selected by the technical committee among more than 59 papers submitted and covered the major categories of memory technologies (3D NAND, 3D DRAM, Ferroelectric, STT, RRAM, PCM, and selectors) and NVM applications (Automotive, In-memory and Neuromorphic Computing).

Among the exciting news presented at the conference, the paper titled "Process improvements for the 7th generation 1Tb Quad-Level Cell 3D NAND Flash Memory in Mass Production" presented by Soochan Kyle Chung (Samsung) won the Best Paper Award, and the paper "Proposal of P-channel FE NAND with High Drain Current and Feasible Disturbance for Next Generation 3D NAND" presented by Song-Hyeon Kuk (Korean Advanced Institute of Science and Technology) received the Best Student Paper Award.

Different activities were organized to promote social contacts between the participants. The conference included lunch meals, a welcome reception with the poster presentation, and a conference dinner.

Another highlight of the conference was the panel discussion on the topic "Can 3D structuring be a technology driver for memory like it was for NAND?", hosted by Tomoya Sanuki (Kioxia).

The next IMW edition will be held in May 2024 in Seoul, South Korea. For more details on the IMW conference please visit the IMW website: https://www.ewh.ieee.org/soc/eds/imw/. IMW technical proceedings are available on the IEEE Xplore database: https://ieeexplore.ieee.org/xpl/conhome/1002800/all-proceedings.

Thomas Mikolajick, General Chair 2023, opening the conference

2023 Technical Chair Antonio Arreghini presenting the 2023 Best Paper and Student Best Paper Award winners

2023 IEEE International Electron Devices Meeting to Highlight Advances in Critical Semiconductor Technologies with the Theme "Devices for a Smart World Built Upon 60 Years of CMOS"

- *A practical, monolithic 3D CFET technology for logic scaling, from TSMC*
- *Fully functional monolithic 3D stacked CMOS inverters, from Intel*
- *A new way to scale DRAM memories, from Samsung*
- *A device offering GPU-like accuracy but with far less energy use, from Tsinghua Univ./Peking Univ.*
- *World-record RF performance, from ETH-Zurich/Univ. Bordeaux*
- *The smallest pixel ever for CMOS imagers, from Samsung*
- *Four Focus Sessions on topics of intense research interest:*
  - *3D Stacking for Next-Generation Logic & Memory by Wafer Bonding and Related Technologies*
  - *Logic, Package and System Technologies for Future Generative AI*
  - *Neuromorphic Computing for Smart Sensors*
  - *Sustainability in Semiconductor Device Technology and Manufacturing*

Since it began in 1955, the IEEE International Electron Devices Meeting (IEDM) has been where the world's best and brightest electronics technologists go to learn about the latest breakthroughs in semiconductor and related technologies. That tradition continues this year, when the 69th annual IEEE IEDM conference takes place in-person December 9-13, 2023 at the Hilton San Francisco Union Square hotel, with online access to recorded content available afterward.

The 2023 IEDM technical program, supporting the theme, "*Devices for a Smart World Built Upon 60 Years of CMOS*," will consist of more than 225 presentations plus a full slate of panels, Focus Sessions, Tutorials, Short Courses, a career luncheon, supplier exhibit and IEEE/EDS award presentations.

"The IEDM offers valuable insights into where the industry is headed, because the leading-edge work presented at the conference showcases major trends and paradigm shifts in key semiconductor technologies," said Jungwoo Joh, IEDM 2023 Publicity Chair and Process Development Manager at Texas Instruments. "For example, this year many papers discuss ways to stack devices in 3D configurations. This is of course not new, but two things are especially noteworthy about this work. One is that it isn't just happening with conventional logic and memory devices, but with sensors, power, neuromorphic and other devices as well. Also, many papers don't describe futuristic laboratory studies, but rather specific hardware demonstrations that have generated solid results, opening pathways to commercial feasibility."

"Finding the right materials and device configurations to develop transistors that will perform well with acceptable levels of reliability remains a key challenge," said Kang-ill Seo, IEDM 2023 Publicity Vice Chair and Vice President, Semiconductor R&D, Samsung Semiconductor. "This year's program shows that electrothermal considerations remain a key focus, particularly with attempts to add functionality to a chip's interconnect, or wiring, which is fabricated using low-temperature processes."

Here are details of the 2023 IEEE International Electron Devices Meeting:

Tutorial Sessions–Saturday, Dec. 9

The Saturday tutorial sessions on emerging technologies are presented by experts in the field to bridge the gap between textbook-level knowledge and leading-edge current research, and to introduce attendees to new fields of interest. There are three time slots, each with two tutorials running in parallel:

1:30 p.m.–2:50 p.m.

- *Innovative Technology for Beyond 2 nm*, Matthew Metz, Intel
- *CMOS+X: Functional Augmentation of CMOS for Next-Generation Electronics*, Sayeef Salahuddin, UC-Berkeley

3:05 p.m.–4:25 p.m.

- *Reliability Challenges of Emerging FET Devices*, Jacopo Franco, Imec

- *Advanced Packaging and Heterogeneous Integration - Past, Present & Future*, Madhavan Swaminathan, Penn State

4:40 p.m.–6:00 p.m.

- *Synapses, Circuits, and Architectures for Analog In-Memory Computing-Based Deep Neural Network Inference Hardware Acceleration*, Irem Boybat, IBM
- *Tools for Device Modeling: From SPICE to Scientific Machine Learning*, Keno Fischer, Julia Hub

Short Courses–Sunday, Dec. 10

In contrast to the Tutorials, the full-day Short Courses are focused on a single technical topic. They offer the opportunity to learn about important areas and developments, and to network with global experts.

- **Transistor, Interconnect, and Chiplets for Next-Generation Low-Power & High-Performance Computing**, organized by Yuri Y. Masuoka, Samsung
  - *Advanced Technology Requirement for Edge Computing*, Jie Deng, Qualcomm
  - *Process Technology toward 1nm and Beyond*, Tomonari Yamamoto, Tokyo Electron
  - *Empowering Platform Technology with Future Semiconductor Device Innovation*, Jaehun Jeong, Samsung
  - *Future Power Delivery Process Architectures and Their Capability and Impact on Interconnect Scaling*, Kevin Fischer, Intel
  - *DTCO/STCO in the Era of Vertical Integration*, YK Chong, ARM
  - *Low Power SOC Design Trends/3D Integration/ Packaging for Mobile Applications*, Milind Shah, Google
- **The Future of Memory Technologies for High-Performance Memory and Computing**, organized by Ki Il Moon, SK Hynix
  - *High-Density and High-Performance Technologies for Future Memory*, Koji Sakui, Unisantis Electronics Singapore/Tokyo Institute of Technology
  - *Advanced Packaging Solutions for High Performance Memory and Compute*, Jaesik Lee, SK Hynix
  - *Analog In-Memory Computing for Deep Learning Inference*, Abu Sebastian, IBM
  - *The Next Generation of AI Architectures: The Role of Advanced Packaging Technologies in Enabling Heterogeneous Chiplets*, Raja Swaminathan, AMD
  - *Key Challenges and Directional Path of Memory Technology for AI and High-Performance Computing*, Keith Kim, NVIDIA
  - *Charge-Trapping Memories: From the Fundamental Device Physics to 3D Memory Architectures (3D NAND, 3D NOR, 3D DRAM) and Computing in Memory (CIM)*, Hang-Ting (Oliver) Lue, Macronix

- **Plenary Presentations–Monday, Dec. 11**
  - *Redefining Innovation: A Journey forward in the New Dimension Era*, Siyoung Choi, President & GM, Samsung Foundry Business, Device Solutions Division
  - T*he Next Big Thing: Making Memory Magic and the Economics Beyond Moore's Law*, Thy Tran, Vice President of Global Frontend Procurement, Micron
  - *Semiconductor Challenges in the 5G and 6G Technology Platforms*, Björn Ekelund, Corporate Research Director, Ericsson

Evening Panel Session–Tuesday evening, Dec. 12

The IEDM evening panel session is an interactive forum where experts give their views on important industry topics, and audience participation is encouraged to foster an open exchange of ideas. This year's panel will be moderated by Dan Hutcheson, Vice Chair at Tech Insights.

- *AI: Semiconductor Catalyst? Or Disrupter?* Artificial Intelligence (AI) has long been a hot topic. In 2023 it became super-heated when large language models became readily available to the public. This year's IEDM will not rehash what's been dragged through the media. Instead, it will bring together industry experts to have a conversation about how AI is changing the semiconductor industry and to ask them how they are using AI to transform their efforts. The topics will be wide-ranging, from how AI will drive demand for semiconductors, to how it's changing design and manufacturing, and even to how it will change the jobs and careers of those working in it.

Luncheon–Tuesday, Dec. 12

There will be a career-focused luncheon featuring industry and scientific leaders talking about their personal experiences in the context of career growth. The discussion will be moderated by Jennifer Zhao, President/CEO, asm OSRAM USA Inc. The speakers will be:

- **Ilesanmi Adesida, University Provost and Acting President, Nazarbayev University, Kazakhstan**. Professor Ilesanmi Adesida is a scientist/engineer and an experienced administrator in both scientific and educational circles, with more than 350 peer-reviewed articles/250 presentations at international conferences.
- **Isabelle Ferain, Vice President of Technology Development, GlobalFoundries**. Dr. Ferain oversees GF's technology development mission in its 300mm fabs in the US and Europe.

Vendor Exhibition/MRAM Poster Session/MRAM Global Innovation Forum

- A vendor exhibition will be held once again.
- A special poster session dedicated to MRAM (magnetoresistive RAM memory) will take place during the IEDM on Tuesday, Dec. 12 from 2:20 pm to 5:30 p.m., sponsored by the IEEE Magnetics Society.

- Also sponsored by the IEEE Magnetics Society, the 15th MRAM Global Innovation Forum will be held in the same venue after the IEDM conference concludes, on Thursday, Dec. 14.

Further Information About IEDM

For registration and other information, visit www.ieee-iedm.org.

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About IEEE & EDS

IEEE is the world's largest technical professional organization dedicated to advancing technology for the benefit of humanity. Through its highly cited publications, conferences, technology standards, and professional and educational activities, IEEE is the trusted voice on a wide variety of areas ranging from aerospace systems, computers, and telecommunications to biomedical engineering, electric power, and consumer electronics. The IEEE Electron Devices Society is dedicated to promoting excellence in the field of electron devices, and sponsors the IEEE IEDM.

2024 IEEE International Reliability Physics Symposium (IRPS)

The IEEE International Reliability Physics Symposium (IRPS) is the world's premier forum for leading-edge research addressing developments in the Reliability Physics of devices, materials, circuits, and products used in the electronics industry. IRPS is the conference where emerging reliability physics challenges and practical solutions to achieve realistic end-of-life projections and mitigation are first discussed.

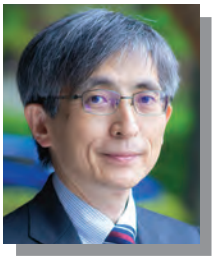
In 2024, the IRPS will be held on 14–18 April at the Hilton DFW Lake, Dallas, Texas. Over the course of the conference, IRPS will offer a blended mix of keynote talks, tutorials, year-in-reviews, workshops, vendor exhibits, and technical presentations. Abstracts are due by 22 October 2023. Late breaking news submissions are welcome by 8 January 2024.

For over 60 years, IRPS has been the premier reliability conference, drawing presentations and attendees from industry, academia, and governmental agencies worldwide. No other meeting presents as much leading work in so many different areas of reliability as IRPS. These areas comprise electronic devices, including silicon and non-silicon devices, process technology, nanotechnology, optoelectronics, photovoltaics, MEMS technology, circuits, and systems reliability, including packaging. IRPS 2024 is now soliciting increased participation in the following areas: GAA, nanosheets, ribbonFETs, Forksheets, SiGe channels, 3D packaging, heterogeneous integration, and reliability-aware EDA.

IRPS 2024 will be kicked off by keynote presentations from reliability experts covering the latest reliability trends, and mitigation approaches from various industry perspectives.

Further opportunities at the Symposium include:

- **Tutorial Program.** The IRPS tutorial program is a comprehensive event designed to help new engineers and experienced researchers. The program contains both beginner and expert tracks and is broken down into topic areas that allow the attendees to participate in tutorials relevant to their work with minimal conflicts between subject areas.
- **Year-in-Review Session.** These seminars provide a summary of the most significant developments in the reliability community over the past year. This serves as a convenient, single source of information for attendees to stay up to date with the recent reliability



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Dr. Yu Gyun Shin Samsung Electronics

literature. Industry and academic experts serve as the "tour guides" and save your time by collecting and summarizing this information as efficiently as possible.

- **Poster Reception.** The poster session provides an additional opportunity for authors to present their original research. The setting is informal and allows for easy discussion between authors and other attendees.
- **Workshops.** The workshops enhance the Symposium by providing the attendees an opportunity to meet in informal groups to discuss key reliability physics topics with the guidance of experienced moderators. Some of the workshop topics are directly coupled with the technical program to provide a venue for more discussion on the topic.
- **Vendor Exhibits.** Held in parallel with the technical sessions, the equipment demonstrations provide a forum for manufacturers of state-of-the-art laboratory equipment to present their products. Attendees are encouraged to visit the manufacturers' booths for information and demonstrations.
- **IRPS Paper Awards.** IRPS awards: Best Paper, Best Student Paper, Best Posters, and People's Choice.
- **IEW Co-Location.** In 2024, the IRPS will be co-located with the International ESD Workshop (IEW). Now in its 17th year, the IEW provides a relaxed, invigorating atmosphere to present new work and engage in discussions about the latest issues confronting the Electrostatic discharge (ESD) and electrostatic over-stress (EOS) communities.

For the call for papers and other information, visit the IRPS webpage (www.irps.org) or join the IRPS LinkedIn group (https://www.linkedin.com/company/89865382/admin/feed/posts/).

The IRPS committee members look forward to seeing you in Dallas, Texas!

Koji Eriguchi 2024 IRPS General Chair, Kyoto University Taiki Uemura 2024 IRPS Publicity Chair, Samsung Electronics

Be Wary of Email SCAMS Targeting IEEE Members

IEEE reminds all members to remain alert to the risk of fraudulent emails and to maintain continued vigilance online. For more information visit this IEEE webpage,, https://mga.ieee.org/news/21-action-items-deadlines/245-cyber-alert-be-aware-and-protect-ieee-from-business-emails-scams

Your IEEE Technical Profile

All IEEE members are encouraged to update their technical interest profiles in their accounts whenever they join a new society or make career changes. Log in to your IEEE account today and check if all information is current and complete so you don't miss important notices.
https://www.ieee.org/membership/benefits/index.html

Message from EDS President-Elect

Bin Zhao
EDS President-Elect

Dear EDS Colleagues and Friends,

First, I want to extend warm greetings to each of you, hoping that everyone is faring well. This year, we are excited to celebrate a remarkable milestone–the 75th anniversary of the transistor. This invention stands as the cornerstone of modern electronics, propelling us into an era defined by high-performance computing and data storage, Internet connectivity, mobile communications, artificial intelligence (AI), machine learning (ML), and the captivating realm of the Metaverse. Reflecting on the past 75 years, we marvel at the journey we embarked upon, driven by the power of the transistor and the subsequent technologies. The impact has been profound, revolutionizing industries and shaping the world we inhabit today.

As we commemorate these achievements, it's essential that we direct our focus towards the future. Over the past decade, the landscape of the semiconductor industry has undergone significant changes. Today, only a select few IC manufacturers carry the torch of cutting-edge technology development, a testament to the escalating costs of technology scaling and advancement. Electron devices have laid the foundation for modern electronics, supporting every facet of our digital lives. As technology's frontiers continue to advance, encompassing areas like Super Computing, Future Networks, AI, ML, the Metaverse, Health Wellbeing, Renewable Energy Generation, and Efficient Energy Storage, the domain of electron devices and technologies grows increasingly diverse. These dynamic advancements are propelled by a multitude of innovative applications that challenge the limits of what's achievable in human history.

To remain attuned to these changes and cultivate stronger engagement within our global technical communities, EDS is committed to enhancing our activities and fostering greater volunteer involvement. Earlier this year, EDS President Ravi Todi established the EDS Organization Enhancement Ad Hoc Committee, comprising five dedicated volunteers–John Dallesasse, M.K. Radhakrishnan, Ravi Todi, Cary Yang, and Bin Zhao (Chair). Working in close collaboration with EDS ExCom, BoG, and Forum, this committee has been earnestly exploring pathways to elevate our Society and enhance our activities, all in pursuit of mitigating the challenges and seizing the opportunities that lie ahead.

The ongoing effort encompasses revisions to the EDS Constitution and Bylaws, enabling volunteers to resume certain roles after a brief break, thus amplifying the reservoir of expertise, experience, and contributions. We are devoted to invigorating EDS technical activities, creating fertile ground for volunteers to contribute and lead. Central to the tapestry of EDS are its Technical Committees (TCs) and their vibrant activities. We have recently updated the position description of TC Chairs to better reflect the evolving landscape and ambitions of the TCs. This update is intended to synchronize the roles of our esteemed TC Chairs with the dynamic pursuits of their respective committees. We're thrilled to introduce an open nomination process for TC Chairs–a pathway that will help us more effectively identify individuals who will lead the TCs in producing lasting, influential, and impactful outcomes for our technical communities.

As we stand on the verge of this transformative journey, I wholeheartedly invite you to consider volunteering or nominating individuals as TC Chairs or TC Members. Your knowledge, expertise, and enthusiasm serve as the driving forces behind our collective achievements. Let's collaborate to maintain the momentum of pioneering, exploration, collaboration, and accomplishments. For deeper insights and heightened engagement, please take a moment to review the accompanying documents "Call for Nominations of EDS TC Chairs" and "Position Description of EDS TC Chairs" included in this Newsletter issue. These documents provide a comprehensive background that will enrich your understanding of this exciting new endeavor.

Thank you for being an invaluable part of EDS–a community that continues to define the frontiers of possibility in electronics.

Bin Zhao
EDS President-Elect

Call for Nominations

Technical Committee Chairs, IEEE Electron Devices Society

The IEEE Electron Devices Society (EDS) is actively seeking visionary and dynamic individuals to assume the Chair positions for its Technical Committees (TCs) with a two-year term starting in January 2024. The following TCs are currently open for nominations:

- Device Reliability Physics
- Electronic Materials
- Flexible Electronics and Displays
- Nanotechnology
- Neuromorphics
- Optoelectronic Devices
- Microelectromechanical Systems
- VLSI Technology and Circuits

The TC Chair will lead the committee's efforts in fostering technology innovation, identifying future technology directions, promoting the growth of emerging technical domains, and facilitating pioneering work within the committee's focus area of electron devices and technologies. The TC Chair will provide leadership by initiating tasks and setting the priorities of the committee. This includes selecting focus areas, organizing workshops, special conference sessions, journal special issues, conference sponsorship, technical or student competitions, etc. The TC will contribute to the development of technical communities and generate technical content. This may involve creating review articles, white papers, roadmaps, books, award recognition programs, tutorials, webinars, short courses, and others in advanced and emerging technical areas. This position presents a unique opportunity to shape the future of EDS and its corresponding technical field. The TC Chair will have the chance to collaborate with technical leaders from around the world and contribute to cutting-edge advancements in electron devices and technologies with full support from EDS. As a voting member of the EDS Forum, the TC Chair will work closely with other EDS leaders, EDS journals, EDS conferences, and other EDS organizations to achieve identified goals. Efficient allocation and management of limited funding to support the committee's activities will be an important responsibility of the TC Chair as well.

Criteria for the Nominees:

- In-depth knowledge of the technical areas related to the TC, including emerging technologies and future trends.
- Strong leadership skills, with the ability to inspire and motivate team members.
- Excellent communication and networking abilities.
- Willingness and dedication to invest sufficient time in serving the leadership role.
- Should be a member of EDS.

Requirement for Nominations:

Self-nominations are permitted and strongly encouraged. Nomination materials should include:

- A concise CV of the nominee (two pages).
- A list of previous volunteering experience within EDS, IEEE, and other professional organizations, and relevant achievements (one page).
- The nominee's statement on his/her vision and plan for the Technical Committee (one page).

If you are interested in participating in this nomination, please complete the online EDS Technical Committee Chair Nomination Form (https://ieeeforms.wufoo.com/forms/wt0u4em095cn60/). The nomination will remain open until the position is filled. EDS encourages diversity and inclusion in all dimensions including gender, geographic, technical, and professional affiliation and they will be considered in the selection process. Please email any questions to: eds_tcc_nominations@ieee.org.

Position Description–EDS Technical Committee Chair

An EDS Technical Committee (TC) Chair plays a pivotal role in promoting technological advancements, fostering innovation, and shaping the future of electron devices and technologies. As a visionary leader and expert in the field, the EDS TC Chair spearheads initiatives to identify future technology directions, nurture emerging technical domains, and facilitate groundbreaking work within the committee's focus areas.

Responsibilities and Activities:

- Provide proactive leadership by setting **strategic focus and priorities** and **generating annual progress report** for the committee's work.
- Initiate and guide the **selection of work areas** that help push technological boundaries and drive innovation.
- Organize impactful **workshops, special conference sessions, and journal special issues** to disseminate cutting-edge research and development results.
- Facilitate **conference sponsorship, technical competitions, award programs, and other initiatives** to foster technical growth and recognition.
- Contribute to the development of dynamic technical communities by **generating influential and relevant technical content**.
- Proactively create **review articles, white papers, roadmaps, books, and other materials** to establish **thought leadership** and provide guidance in advanced and emerging technical areas.
- Drive the establishment of **tutorials, webinars, and short courses** to disseminate knowledge and promote skill development in advanced technologies.
- Serve as a voting member of the EDS Forum, **collaborating actively** with other EDS leaders, journals, conferences, and organizations to achieve committee goals.
- Leverage EDS support and **collaborate with external organizations** to make **a lasting impact** and drive **cutting-edge advancements** in the field.
- Efficiently **budget, allocate and manage limited funding** to ensure maximum **impact and sustainability** for committee activities.
- Work with the EDS VP of Technical Activities to **recruit and retain committee members** who are willing and able to commit their time and effort to advancing the committee's objectives.
- Promote and embody principles of **inclusion, equity, and diversity** in all committee activities and assist in facilitating a seamless **committee leadership transition** when necessary.

This position presents a unique and influential opportunity to shape the trajectory of EDS and its technical field. An EDS TC Chair will be at the forefront of technological advancements, collaborating with global technical leaders, and contributing to the cutting-edge progress of electron devices and technologies. This role carries the responsibility to make strategic decisions, promote innovation, and create a lasting impact on the future of EDS and the broader scientific and engineering community.

Message from EDS Newsletter Editor-in-Chief

Daniel Tomaszewski
EDS Newsletter
Editor-in-Chief

Dear Readers, Members of the IEEE Electron Devices Society,

Welcome to the IEEE EDS Newsletter issue of October 2023. I do hope that it brings you interesting articles concerning different topics.

Please find included the next three articles celebrating the 75th Anniversary of Transistor and devoted to the history of the non-planar FETs, SOI technology and MOSFET compact modeling. The Anniversary celebration goes down slowly in history. The related articles have shown continuous efforts of the researchers and engineers in electron device technology over the past 75 years. In each stage, they were possible thanks to the achievements of the predecessors. For sure, it will be so in the future and the next anniversaries of Transistor will be great opportunities to celebrate them in the Society journals and conferences.

The Technical Briefs section presents highlights of two important EDS-sponsored conferences: 2023 VLSI Symposium, and 2023 International Memory Workshop. In the Upcoming Technical Meeting section, we announce the next two principal conferences: 2023 IEEE International Electron Devices Meeting, and 2024 International Reliability Physics Symposium.

We are happy to present in this issue a Message from the EDS President-Elect, Bin Zhao. I would like to draw your attention to his words on the role of the Technical Committee Chairs and inviting you "to consider volunteering or nominating individuals as TC Chairs or TC Members." In relation to that, the Call for Nominations for Technical Committee Chairs and the Position Description are presented in the issue. Bin will take his responsibilities very soon. Let's not only cross fingers for his initiatives and decisions but support him and all the EDS Executive Committee in their work. I would be very glad if Bin could share his thoughts and requests with the EDS community using the EDS Newsletter platform as well.

This issue brings the third part of "A Brief History of the IEEE Electron Devices Society" by Samar Saha. It is devoted to Conferences and Awards & Recognition. We are very grateful to Samar for that huge and fascinating work based on numerous sources.

In the Women in Engineering section, two outstanding researchers present their careers, achievements, and thoughts: Prof. Sarah Kurtz working, among others, on multijunction GaInP/GaAs solar cells, and Prof. Mina Rais-Zadeh working on MEMS and Micro-Instrumentation.

We are happy to present a rich material on humanitarian activities undertaken by EDS entities in various communities. We are open to such news. I believe that they can be inspiring to us. Any, even small voluntary services can help others.

As usual, the Chapter and Regional News contain articles on daily activities of the EDS chapters, both societal and technical. I am very glad that most of the IEEE regions are represented in this Newsletter issue. Personally, I regret and understand that Ukrainian chapters have not been represented in the Newsletter since 2021. I am aware of their difficult situation, and wish for our colleagues from Lviv, Kyiv, Kharkiv a better future, and a return to normal, safe life.

At the end, the updated calendar of the EDS-supported conferences is presented. I would like to draw your attention also to the announcement of the inaugural IEEE Life Member Conference which will be held in the next year. This handout is included on the inside back cover.

The EDS Newsletter editorial team work was coordinated for several years by Joyce Lombardini. In August, she stepped down from her position. Her diligent and silent way of handling the tasks towards fruitful culmination of EDS programs was much impressive during the past many years of working in the EDS team. We wish her a healthy and happy life ahead and all the very best in future endeavours.

Dear Readers, if you have any suggestions, or comments regarding the Newsletter contents, please do not hesitate to contact us. We will be very glad to receive your feedback. Interesting views will be presented with the consent of the authors together with our replies, in the Letters to Editors section.

Sincerely,

Daniel Tomaszewski

A Brief History of the IEEE Electron Devices Society—Part III Conferences and Awards & Recognition

Samar K Saha
Prospicient Devices, Milpitas, CA 95035, USA

This article presents a comprehensive history of sponsored and co-sponsored technical meetings and conferences of the *Electron Devices Society* (EDS) of the *Institute of Electrical and Electronics Engineers* (IEEE) over the past seven decades. The growth of the IEEE EDS over the past seven decades is inherently related to the invention of the *Transistor* [1]–[4] and its post-invention evolution enabling the digital revolution [5]. In an effort to present a comprehensive history of the IEEE EDS, the story of the *origins* and *growth* [6], and *publications* [7] of the Society has been told in Part I and Part II of the article, "A Brief History of the IEEE Electron Devices Society," *IEEE Electron Devices Society Newsletter*, vol. 30, no. 2 and no. 3, respectively. In continuation, this final Part III of EDS history describes the Society's relentless pursuit to sponsor and co-sponsor technical meetings and conferences within the technical areas of importance to its global community as well as establishing a series of special awards to recognize major accomplishments of individuals within the *field of interest (FoI) of the Society.*

I. Conferences

As described in part I [6], the IEEE was formed after the amalgamation of the *Institute of Radio Engineers* (IRE) and

the *American Institute of Electrical Engineers* (AIEE) in 1963 [8], [9]. Prior to the formation of IEEE, the IRE *Professional Group on Electron Devices* (PGED) was established on March 5, 1952, to interact directly with the *electron devices community*. After the formation of IEEE, the IRE PGED became on January 1, 1963 the *IEEE Professional Technical Group on Electron Devices* (PTGED) which on May 20, 1964 was renamed the *IEEE Electron Devices Group* (EDG), and on February 17, 1976 became the IEEE EDS.

Over the past seven decades, the electron devices leadership under the IRE and IEEE has been actively continuing to sponsor and cosponsor repeat and new conferences and meetings on the topical interest of the global electron devices community.

A. IRE Sponsored Meetings and Conferences

During the formative years, the IRE PGED actively *sponsored* and *cosponsored* meetings and conferences on areas of interest to the group's technical community[10]. A few of the major events are described below.

1) *East Coast–West Coast Conferences:* In the 1950s, the IRE PGED sponsored parallel sessions at the annual IRE meeting in New York and the *Pacific Coast Council* conference, known as WESCCON on the West Coast [10]. Typical sessions were on *electron tubes*, *microwave tubes*, and *transistors*. All sessions were well attended, especially the newly invented transistor sessions at which very often the demand exceeded the seating capacity [10]. In addition, the IRE PGED often *cosponsored* more specialized meetings of interest to its members with other IRE professional groups including a *Symposium on Microwave Radio Relay Systems* held in November 1953 [11], and a *Symposium on Fluctuation Phenomena in Microwave Sources* in 1954 [12].
2) *Device Research Conference:* In the early 1950s, the sponsorship of the annual *Electron Device Research* conference was controlled by the IRE entity called the *IRE Committee on Electron Tubes and Solid-State Devices* [6]. In 1952, this gathering became two separate annual meetings: (i) the *Conference on Electron Device Research* (CEDR) and (ii) the *Solid-State Device Research Conference* (SSDRC) [10]. The major features of CEDR and SSDR were *by-invitation-only* and off-the-record without proceedings, facilitating open discussions of advanced cutting-edge research without violating the proprietary concerns of employers. However, authors interested in print copies of their papers could always send them to PGED publication successive chairmen *Herbert J. Reich* of Yale University, Connecticut and *John Saby* of General Electric (GE), New York (1952-1954), or the editor *Earl L. Steele* (1955-1961) for publication in the *PGED Transactions* [7], [10], [13]–[15].

   Although the IRE PGED actively participated in cosponsoring meetings, membership strongly supported the idea of sponsoring a technical meeting of their own which led to the origins of the annual IRE Fall Electron Devices Meeting in Washington, D.C. [10], [16].
3) *IRE Fall Electron Devices Meeting:* The overwhelming support for the idea of holding a technical meeting every fall in an eastern city (of the United States of America) led PGED *Administrative Committee* (AdCom) to approve such a meeting at the January 1955 meeting. IRE PGED AdCom's first Chairman, *George O'Neill* of Sylvania agreed to serve as the Chairman of the *first annual meeting* in Washington, D.C.. George made the necessary arrangements with support from the local *PGED chapter* holding the first *IRE Fall Electron Devices Meeting* in Washington, D.C. in the Fall of 1955 [10], [16], [17]. The *Call for Papers* emphasized that the meeting was primarily intended *to provide an outlet for presentation of material covering areas between research and process engineering*. The gathering was to be a "Conference on Electron Devices, as distinguished from their circuit applications." It occurred during October 24-25, 1955, at the *Shoreham Hotel* near *Rock Creek Park*, with over 600 in attendance, the first of many annual meetings held at this hotel [17]. In the following year, October 25-26, 1956 meeting attracted more than 1,000 attendees, *William Shockley* delivered the luncheon speech [18]. The major topical areas at the annual meetings included *quantum devices*, *semiconductor lasers*, *and light-emitting diodes*.

   In the mid-1960s, as the IEEE EDG began expanding its activities beyond the United States (US) of America borders, the annual Fall Washington Meeting was renamed the International Electron Devices Meeting (IEDM) in 1965 [19].

B. IEEE Sponsored Meetings and Conferences

The relentless efforts of the IEEE EDG/EDS AdCom, which later became the Board of Governors (BoG) in 2013 [6], to launch some of the major conferences are briefly described below.

1) *International Electron Devices Meeting*: The first IEDM was held at the Sheraton-Park Hotel and Motor Inn, Washington D.C. during October 20–22, 1965 under the leadership of the General Chairman *Clarence G. Thornton* of Philco Corporation, Lansdale, Pennsylvania [19]. In the mid-1960s, typical sessions of this annual meeting were *electron tubes*, *solid-state devices*, *energy-conversion devices*, *integrated circuits*, and *quantum devices*. The new emerging areas such as *imaging displays* and *sensors* were of major attraction in the late 1960s as evidenced by three sessions devoted

to these topics in the 1967 Washington D.C. meeting [19].

In the year 1982, the IEDM was first held outside the Washington D.C. in *San Francisco Hilton, San Francisco*, *California* during December 13–15 with *Al F. Tasch, Jr.* of Motorola, Austin, Texas as the Conference Chairman. In IEDM, sessions on *complementary metal-oxide-semiconductor* (CMOS) technology for very large scale integrated (VLSI) circuits attracted large crowds. For example, at the 1982 IEDM, a paper by several Toshiba researchers that demonstrated how to achieve 1.2-micron n-p spacing between elements was a major attraction. And the very next year, scientists at the Nippon Telegraph and Telephone (NTT) Corporation revealed new CMOS technologies to obtain submicron features in Dynamic Random Access Memory (DRAM) chips, the first memory chips to offer megabit storage capacities [19].

The success of IEDM in San Francisco in terms of both attendance and finances, convinced AdCom to hold the IEDM on the West Coast every other year. This decision benefited not merely the large concentrations of California members, especially in Silicon Valley, but also the growing membership in Japan and in the Asia-Pacific. Such members were much more inclined to attend meetings in California than in Washington, D.C. Remarkably, in 1984, when IEDM again occurred in San Francisco, a record 2,900 attended, and the Society received a $70,000 surplus, a major part of the total EDS surplus of $175,000 that year. Except for 1986, when it was held in *Los Angeles*, the IEDM has ever since returned to San Francisco in the even years. And, since 2016, the IEDM is held annually in San Francisco only [16], [19].

2) *Reliability Physics Symposium:* From 1962 to 1966, a series of *Symposium on Physics of Failure* (PoF) concept was organized by the Rome Air Development Center (RADC) of the US Air Force [20]. Since 1967, the I*EEE PGED* and *Reliability* jointly cosponsored the *Annual Reliability Physics Symposium* presenting a wide range of device and systems reliability issues on fundamental physical and chemical processes that contribute to the degradation, aging, and failure of electronic components and materials. In 1994, the conference was renamed the *IEEE International Reliability Physics Symposium* (IRPS), jointly co-sponsored by the IEEE EDS and Reliability Society which is held annually in March/April [21].
3) *Device Research Conference:* In the year 1969, under the leadership of *Herbert Kroemer* of the University of Colorado at Boulder (later at the University of California, Santa Barbara, California) and *Calvin F. Quate* of Stanford University, the CEDR and SSDR merged back into a single *Device Research Conference* (DRC), which continues to be held annually around June [22]. The merged annual DRC managed the unique characteristics of CEDR and SSDR by their own special committees coordinating their plans and activities with the IEEE EDG. The 1970 DRC was held at the *University of Washington in Seattle, Washington*. The major revelation of the meeting was new applications of CMOS technology such as DRAM and charge-coupled devices (CCD) by participants from Bell Labs, Fairchild, and other companies [10] as well as an announcement of the development of semiconductor room temperature lasers by Bell Labs researchers [10], [22]. In 1972, the annual DRC was held for the first time beyond US borders at the *University of Alberta in Edmonton, Canada*.

In the mid-1970s, the attendance at DRC continued to decline, reaching close to 200 in 1975. This fall-off, also, may have reflected a decline in the electron devices field in the mid-1970s. In part to raise attendance, the 1976 DRC in Salt Lake City was held in tandem with the *Electronic Materials Conference* sponsored by the *American Institute of Metallurgical Engineers* (also called *The Metallurgical Society*). As a result, the attendance revived to typical levels of about 500 by the end of the 1970s [10].

From the 1990s to the present day, DRC has been the world's premier forum to present innovative and exploratory semiconductor device research including thin film transistors, graphene and carbon nanotube transistors, and two-dimensional (2D) materials. In 2017, the 75th anniversary of DRC was celebrated with special sessions and an article in the *IEEE Journal of the Electron Device Society* [22].

As the metal-oxide-semiconductor (MOS) devices became the pervasive technology for VLSI circuits in the 1980s, a concentrated effort started to support the emerging area with a new Symposium on VLSI Technology.

4) *Symposium on VLSI Technology:* In the early 1980s, semiconductor industry leaders championed the goal of very large-scale integration by scaling down MOS geometry enabling microchip features as small as a micron, or a millionth of a meter [5]. By the mid-1980s, VLSI pioneers approached the submicron scale. The IEEE EDS strongly supported these efforts, often working in tandem with the Solid-State Circuits Council and Japanese counterparts. In 1979, a special VLSI issue was published jointly by the *IEEE Transactions on Electron Devices* (T-ED) and *Journal of Solid-State Circuits*, edited by AdCom member *Walter Kosonocky* of RCA along with *Takuo Sugano* of the University of Tokyo and *Hans Friedrich* of Siemens [23]. And, the Society cosponsored a

VLSI Workshop in 1980, and the first *Symposium on VLSI Technology* in Maui with the *Japan Society of Applied Physics* in 1981. Moreover, the T–ED published special issues on VLSI technology and simulations in 1980, 1982, and 1983 [15].

Historically, the Electron Devices Group/Society strategically positioned itself in the frontiers of providing forums for its global community on emerging technology through collaboration in organizing meetings and conferences within its technical FoI as in the case of a conference on photovoltaic devices.

5) *Photovoltaic Specialists Conference:* The discussions to organizing a technical meeting in the topical area of photovoltaic devices started in the early 1960s at the regular group meetings of the *Interservice Group for Flight Vehicle Power* (IGFVP) of the US government's *Department of Defense* and *National Aeronautics and Space Administration* (NASA) carrying out and *supporting* Research and Development (R&D) *on energy conversion devices and systems*. On March 7, 1961 meeting in Philadelphia, Pennsylvania, the *Solar Working Group* (SWG) of the IGFVP decided that a broader meeting was needed to include personnel from the industry and academia who are active in the area of photovoltaic devices, and reported the decision in the meeting minutes published on March 16, 1961. Subsequently, on April 14, 1961, the first meeting of *photovoltaic device specialists* was organized by the *Institute for Defense Analysis* (IDA) at NASA Headquarters (HQ) in Washington D.C. [24].

   In 1962 February 27 and 28, the *Interagency Advanced Power Group* (IAPG) held the second *Solar Working Group Conference* at NASA HQ in Washington, D.C. [24]. On April 10-11, 1963, the third *Photovoltaic Specialists Working Group* meeting was held at the Statler Hilton, Washington D.C., and sponsored jointly by the *IEEE, AIAA* (*American Institute of Aeronautics and Astronautics*), and NASA. In 1964, the conference began using a *numbering system* along with the title *Photovoltaic Specialists Conference* (PVSC) [24]. For example, the 1964 annual meeting was formally called the 4th PVSC. The 4th and 5th PVSC on June 2-3, 1964 and October 18-20, 1965, respectively were, also, *jointly* sponsored by the IEEE, AIAA, and NASA. Since the 6th PVSC on March 28-30, 1967 at Cocoa Beach, Florida, the conference has been sponsored solely by the *IEEE, and the then EDG became the sole financial sponsor of the PVSC and to this date, the EDS remains the sole financial sponsor of the PVSC* [16], [24].

   In the ensuing decades, the list of professional meetings supported by the EDS continued to grow and diversify. Where the EDS had supported 39 meetings at the beginning of the 1990s, the total number of conferences grew to 68 by the end of the second millennium and continued to climb in the third millennium with the rapid changes in the VLSI manufacturing landscape.

6) *Electron Devices Technology and Manufacturing Conference:* In the mid-2010s, the EDS Senior leadership including *Paul Yu,* (2012-2013 President) of the University of California, San Diego, *Albert Wong* (2014-2015 President) of the University of California, Riverside, *Bin Zhao* of Fairchild/ON Semiconductor, Irvine, California, and *Ravi Todi* of Globalfoundries along with *EDS VLSI Technology & Circuits Committee* started discussions to organize an EDS Flagship conference in the hotbeds of semiconductor manufacturing, Asia-Pacific countries. Based on strong manufacturing technologies, Asia has an excellent potential to take an initiative for system integration through collaboration among materials, process, and device communities to accelerate manufacturing innovations. Thus, an IEEE initiative is crucial to provide a timely forum for the electron devices community to come together to collaborate on topics from devices-to-materials-to-tools thus facilitating the creation of new and innovative technologies for system integration. In this context, through the effort of VLSI Technology & Circuits Committee chairman, *Shuji Ikeda* of Tei Solutions Co. Ltd. Tsukuba, Japan, along with EDS *VP* of Conferences and Technical Activities, Ravi Todi, and 2016-2017 President *Samar Saha* of Prospicient Devices, the EDTM was launched and the 1st *IEEE Electron Devices Technology and Manufacturing* (EDTM) Conference was held in Toyama, Japan during March 12-16, 2017 with Shuji as the General chairman [25].

   Within a short span of time, the EDTM conference has become one of the top-tiered forums among the electron devices community. The 2nd and 3rd EDTM were held during March 13–16, 2019 in Kobe, Japan, and March 13–16, 2019 in Singapore, respectively. The 4th EDTM 2020 was held virtually from Penang, Malaysia (the 1st IEEE virtual conference) due to the COVID-19 pandemic; the 5th in 2021 was held as a hybrid (in-person & virtual) in Chengdu, China; 6th, virtually in Oita, Japan in 2022; and 7th in-person in Seoul, Korea in 2023 [25]. The 8th EDTM is scheduled in Bangalore, India [26].

   *In the mid-2010s, the Society's Senior leadership perceived that it was crucial to execute new initiatives to support EDS membership and its growth in the IEEE Region 7, Canada that led to discussions among the EDS President Samar, Ta-Ya Chu of the National Research Council Canada, Canada, and Jamal Deen of McMaster University, Canada during the 7*th *International Conference on Computer-Aided Design for Thin-Film Transistor Technologies,*

CAD-TFT 2016 in Beijing, China. This finds the origins of the IEEE International Flexible Electronics Technology Conference (IFETC).

7) *International Flexible Electronics Technology Conference:* In the late 2017, through the effort of *Gaozhi* (*George*) *Xiao*, Ta-Ya Chu, and 2016-2017 EDS President Samar, the IEEE *International Flexible Electronics Technology Conference* (IFETC) was established. The first IEEE IFETC was held on August 7–9, 2018 at the Delta Hotel City Centre in Ottawa, Ontario, Canada with George and Samar as the General Co-Chairs and Ta-Ya along with *Ye Tao* of Advance Electronics and Photonics, Canada as the Technical Program Co-Chairs [27]. Due to the short time to plan for the EDS budget, the IFETC 2018 was financially sponsored by the IEEE *Council of Radiofrequency Identification* (CRFID) with EDS providing funding in the amount of US$ 5K. Following the year with the approved budget, the EDS assumed 100% financial sponsorship from the 2nd IFETC 2019. The IFETC provides a unique forum for discussions on a broad range of flexible/printable electronics device/manufacturing-related topics including sensors, displays, and in general large area flexible electronics systems.

   The 2nd IEEE IFETC was held on August 11-14, 2019 in Vancouver, Canada with *Woo So Kim* of Simon Fraser University as the General Chair; the 3rd IFETC on August 8-11, 2021 Virtually with *Paul Berger* of the Ohio State University as the General Chair; and the 4th IFETC was held as a Hybrid conference during August 21-24, 2022 in Qingdao, China with *Arokia Nathan* as the General Chair. The 5th IEEE IFETC 2023 was held during August 14-16 in *San Jose, California, USA* with Samar as the General Chair. In the year 2022, the IFETC steering committee approved the rotation of the IFETC conference location between North America, Asia, and Europe.

   In order to support the growth of EDS membership in the IEEE Region 9 (South America), a dedicated EDS flagship conference, the Latin American Electron Devices Conference was established in 2019.

8) *Latin American Electron Devices Conference:* In the late 2010s, the *Latin American Electron Devices Conference* (LADEC) was established through the efforts of 2018-2019 President *Fernando Guarin* of Globalfoundries [16]. The inaugural LADEC was held on February 24-27, 2019 in Armenia, Colombia with General Chairs, *Johan Sebastián Eslava* of the National University of Columbia (UNAL), Colombia, and *Andrei Vladimirescu* of Paris Institute of Digital Technology (ISEP), France and the University of California, Berkeley, USA. In the following year, the LADEC was held on February 25-28, 2020 in San Jose, Costa Rica with *Mario Alemán* of IEEE Nicaragua as the General Chair. LADEC 2021 was held virtually online during April 19-21, 2021 with *Mario* as the General Chair. In the year 2022, LADEC was held in person on July 4-6, 2022 in Puebla, Mexico with *Edmundo A. Gutiérrez* of the Instituto Nacional de Astrofísica Óptica y Electrónica (INAOE), Mexico as the General Chair. The LADEC has become an attractive forum for microelectronics researchers of IEEE Region 9 and going strong. The 2023 LADEC was held on July 3-5, 2023 in Puebla, Mexico with *Esteban Arias* of Instituto Tecnológico de Costa Rica Cartago, Costa Rica, and *Cor Claeys* of KU Leuven, Belgium as the Co-General Chairs [28].

   Along with the growth in membership, supporting members' needs for publications, meetings, and conferences, the Society established awards to recognize technical and professional achievements of members as well as individuals within the EDS FoI as described below.

II. Awards and Recognition

Since the 1970s, the then AdCom and renamed BoG leadership has been actively implementing new initiatives to establish a series of special awards to recognize major accomplishments of individuals in the *field of electron devices* as briefed in the following Section.

A. J.J. Ebers Award

In March 1971, the *IEEE Awards Board* approved an award *for outstanding technical contributions to electron devices* to be presented annually at the Washington D.C. meeting. It was named the *J. J. Ebers Award* to honor the exemplary life and work of *Jewel James Ebers*, who had met an untimely death in 1959 after making important contributions to *electron-tube technology* and *semiconductor device art*. The *first* recipient of the *J. J. Ebers Award* was *John Moll* of Fairchild Semiconductor, Mountain View, California in the fall of 1971 [16]. Since 2016, the award has been presented annually at the IEDM San Francisco

B. Jack A. Morton Award

In order to commemorate the lifelong achievement of *Jack A. Morton* on the development *of electron tubes and solid-state devices*, the IEEE established in the year 1974 an Institute-level technical field award named, *Jack A. Morton Award* for contributions to electron-devices. This award was presented annually to an individual or group *for outstanding contributions to the field of solid-state devices*. In 1976, *Robert Hall* of GE received the first Morton Award "for outstanding achievement in solid-state physics and chemistry and the invention and development of semiconductor devices" [16]. The following year, it went to *Morgan Sparks* "for contributions to solid-state devices technology and the management of research and development." In 2000, the *Jack A. Morton Award* was replaced by the *Andrew S. Grove Award* [16].

C. William R. Cherry Award

The *William R. Cherry* Award was established in the year 1980 to recognize the outstanding contributions of *William R. Cherry to the advancement of photovoltaic science and technology*. Shortly after the passing of William R. Cherry, the *IEEE PVSC Committee* at one of the planning meetings for the 14th PVSC, January 7-10, 1980, decided to establish the award. *Paul Rappaport,* the Chairperson of the 5th PVSC was the recipient of 1980 *William. R. Cherry* Award. And, the 1981 winner was *Joseph L. Loferski*, Chairperson of 8th PVSC [16].

D. Paul Rappaport Award

In 1983, AdCom approved a new award named after Paul Rappaport, who had served on the committee during the early 1970s and as EDS President in 1975. Paul's research work had been on photovoltaics at Radio Corporation of America (RCA) before joining as the Director of the *National Renewable Energy Center*, Golden, Colorado in the *late* 1970s. The award is given annually at the IEDM to the author or authors of the best paper that appeared in IEEE T-ED during the previous year [16]. At the 1984 San Francisco IEDM, *Jaroslav Hynecek* of *Texas Instruments* received the first *Paul Rappaport Award* for his article on "Electron-hole recombination antiblooming for virtual-phase CCD Imager," which was published in the August 1983 issue of the IEEE T- ED [15].

E. Distinguished Service Award

In the year 1993, AdCom approved the establishment of the *EDS Distinguished Service Award*, to be presented every year to an individual member *to recognize and honor outstanding service to the Electron Devices Society and its sponsored activities*. In 1994, the first award was presented to *Friedolf M. Smits*, who served as EDS Treasurer during 1980-1987 and moved forward the Society toward financial stability by the end of the decade [6], [16].

F. Chapter of the Year Award

AdCom established the *Chapter of the Year Award* in 1997. This is awarded annually to a chapter based on the quantity and quality of the activities and programs implemented by the chapters during the prior July 1st to June 30th of the year of the award. The recipients of the first award were IEEE ED/MTT ((Electron Devices)/(Microwave Theory and Techniques)), India, and ED/CPMT/RS ((Electron Devices)/(Components, Packaging, and Manufacturing Technology/Reliability)), Singapore joint-chapters in the year 1998 [16].

G. Millennium Medals

At the beginning of the third millennium, the EDS looked back at the impact of electron devices have had on humanity over the past century and the contributions of the individuals and institutions that made it happen. In order to honor some of the Society's leading members, especially those whose selfless dedication of their time and efforts contributed to its success over the past five decades, the *Society awarded 45 Millennium Medals at the* 2000 *IEDM in San Francisco*. The EDS members and former officers came to San Francisco from around the world to accept their medals. They were honored for their *outstanding contributions to the Electron Devices Society and to the field of electron devices* [10], [16].

H. Andrew S. Grove Award

The *Andrew S. Grove Award* replaced the Jack A. Morton Award and its financial responsibility was approved by AdCom in the year 1999. The award is given to an individual or group (of not more than three persons) *for outstanding contributions in the field of solid-state devices and technology*. In 2000, the award was presented for the first time at IEDM to *Wolfgang Fichtner* of the Swiss Federal Institute of Technology in Zurich, "for outstanding contributions to semiconductor device simulations." The following year, *Al F. Tasch* of the University of Texas, Austin, won the award "for contributions to MOS technology, ion implantation, and device modeling" [16].

I. George E. Smith Award

The *George E. Smith Award* was established in 2002 to recognize the best paper appearing in the fast turnaround archival publication, the *IEEE Electron Device Letters* (EDL). The award is given annually at the IEDM to the author(s) of the best paper that appeared in the IEEE EDL during the previous year [16]. At the 2002 San Francisco IEDM, *B. Jagannathan et al.,* of *IBM, NY* received the first *George Smith Award* for their article entitled, "Self-aligned SiGe npn transistors with 285 GHz f_{MAX} and 207 GHz f_T in a manufacturable technology," which was published in the May 2002 *issue of* the IEEE EDL [16], [29].

J. Region 9 Biennial Outstanding Student Paper Award

In 2002, the IEEE Region 9 *Outstanding Student Paper Award* was established to promote, recognize, and support meritorious research achievement of the IEEE Region 9 (Latin America and the Caribbean) students and their advisors through the public recognition of their published work within the EDS FoI. The winners also receive up to three years of complimentary IEEE and EDS student membership depending on their eligibility [16].

K. Education Award

The *Education Award* was established in 2005 to recognize the distinguished contributions of individuals to education within the EDS FoI. The first recipient was *Mark S. Lundstrom* of Purdue University, West Lafayette, Indiana in the year 2006 [16].

L. Early Career Award

The EDS *Early Career Award* was established in 2009 to promote, recognize, and support early career technical development within the EDS FoI. It is presented annually to honor an IEEE EDS member who has received his/her first professional degree (Bachelor) within the 10th year defined by the August 15th nomination deadline, making contributions within the EDS FoI. The first recipient was *Chi On Chui* of the University of California, Los Angeles, California, USA in the year 2009 [16].

M. Robert Bosch Micro and Nano Electro Mechanical Systems Award

The *Robert Bosch Micro and Nano Electro Mechanical Systems Award* was established in 2014 to *recognize and honor advances in the invention, design, and/or fabrication of micro- or nano-electromechanical systems and/or devices.* Individual contributions should be innovative and useful for practical applications. The first recipient of the award was *Yu-Chong Tai* of Caltech, Pasadena, California, USA, "for pioneering contributions in materials, technologies, and design of MEMS/NEMS and groundbreaking achievements in the realization of biomedical parylene MEMS" [16].

N. Lester F. Eastman Award

The *Lester F. Eastman Award* was established in 2019 to recognize individuals *for outstanding achievement in high-performance electronic and optoelectronic devices*. It is named after the late Professor *Lester F. Eastman* of Cornell University, Ithaka, NY, USA, a world leader in the physics and technology of compound semiconductor materials and devices. The first recipient of the award was *Asif Khan*, University of South Carolina, Columbia, South Carolina, USA in the year 2020.

O. Leo Esaki Award

The *Leo Esaki Award* was established in 2019 to recognize the best paper appearing in open access archival publication, the *IEEE Journal of Electron Devices* (J-EDS) during the previous year [16]. It is presented annually at the IEDM. The first recipients were *Masaharu Kobayashi et al*. for their paper, "Ferroelectric HfO_2 Tunnel Junction Memory with High TER and Multi-level Operation Featuring Metal Replacement Process," published in the December 2018 issue of the IEEE J-EDS [16], [30].

P. Student Fellowships

The Society has instituted a number of student fellowships to promote, recognize, and support different levels of studies and research within the EDS FoI [16] as described below:

- The *PhD Student Fellowship*s were established in the year 2001 to promote, recognize, and support PhD level study and research within the EDS FoI. Three one-year fellowships are awarded annually to eligible students, one each from each of the following IEEE Regions: (1) IEEE Region 1-7 (Americas), (2) IEEE Region 8 (Africa, Europe, and Middle East), and (3) IEEE Region 10 (Asia and Pacific). Only one candidate can win per academic institution.
- The *Masters' Student Fellowships were established* in 2007 to promote, recognize, and support Masters level graduate study and research within the EDS FoI. Again, three one-year fellowships are awarded annually to eligible students, one each from each of the following IEEE Regions: (1) IEEE Region 1-7 (Americas), (2) IEEE Region 8 (Africa, Europe, and Middle East), and (3) IEEE Region 10 (Asia and Pacific). Only one candidate can win per academic institution.
- The *Undergraduate Student Scholarships* were established to promote, recognize, and support undergraduate-level study and hands-on experience within the EDS FoI in 2020. Five fellowships are awarded annually with the selection of only one fellowship to eligible students in each of the IEEE geographical Regions 8, 9, and 10 and *two* fellowships in Regions 1-7 not exceeding one from Region 7.

III. Conclusion

The *Electron Devices Society*, EDS is a true volunteer-led volunteer-driven global association of electron devices community under the *Institute of Electrical and Electronics Engineers, IEEE*. The Society has established itself in an enviable intellectual and financial position due to the selfless dedication and relentless efforts of its AdCom/BoG and volunteers over the past seven decades. Since the 1950s, the EDS governing body has engaged with dedicated efforts to successfully expand its activities within the US–coast-to-coast, beyond US borders, and internationally. The Society welcomed international AdCom/BoG members with financial support to travel; formed new chapters around the globe including self and joint chapters with other IEEE entities of common interest; implemented educational programs; established student fellowships; funded awards to recognize its members and luminaries of electron devices community; launched humanitarian programs; and so on to support EDS members worldwide. Furthermore, the Society's worldwide growth is culminated by a portfolio of diverse top-tiered professional journals as well as sponsored meetings and conferences on topics of growing interest *to foster the professional growth of its members by satisfying their needs for easy access to and exchange of technical information, publishing, education, and technical recognition and enhancing public visibility in the field of electron devices*. Surely, a new horizon is coming into view of the electron and ion devices related to technology, however, the long glorious history of EDS over seven decades tells us that the Society is strategically

well-positioned to navigate through the technological changes by timely strategic planning for *Future Directions*. Since the formative years, the EDS leadership implemented new initiatives and diversified its day-to-day operations accordingly with electron and ion device technology transitioning from electron tubes to solid-state devices, transistors, and throughout its evolution from point-contact to bipolar junction transistor (BJT) to metal-oxide-semiconductor transistor (MOSFET) to Fin Field-effect transistor (FinFET). Thus, through the relentless efforts of BoG, the Society is on the right path to continue to *build EDS on the past to meet the challenges of the future* and continue to enjoy an enviable intellectual and financial position.

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2022 EDS Paul Rappaport Award

A high priority of the Electron Devices Society (EDS) is to recognize and enhance the quality of papers published in EDS archival literature. Every year, the Society confers its prestigious Paul Rappaport Award to the best paper published in the *IEEE Transactions on Electron Devices*. Among other criteria including technical excellence, an important metric for selection for the award is comprehensive and impartial referencing of prior art.

The winning paper was selected from over 1,084 articles that were published in 2022. The winning paper is entitled "*InP/GaAsSb Double Heterojunction Bipolar Transistor Emitter-Fin Technology With f_{MAX} = 1.2 THz*". This paper was published in the April 2022 issue of the *IEEE Transactions on Electron Devices*, and was authored by Akshay M. Arabhavi, Filippo Ciabattini, Sara Hamzeloui, Ralf Flückiger, Tamara Saranovac, Daxin Han, Diego Marti, Giorgio Bonomo, Rimjhim Chaudhary, Olivier Ostinelli, and Colombo R. Bolognesi.

The award will be presented during the IEEE EDS International Electron Devices Meeting to be held in December 2023. In addition to the award certificate, the authors will receive a check for $2,500 to be shared equally among all authors. On behalf of the Electron Devices Society, I would like to congratulate the authors for this achievement. Brief biographies of some of the authors follow.

Arokia Nathan
EDS Vice-President of Publications and Products

2022 EDS Leo Esaki Award

The Leo Esaki Award was established in 2019 to recognize the best paper appearing in a fast turn around archival publication of the IEEE Electron Devices Society, targeted to the IEEE Journal of Electron Devices Society. Among other criteria including technical excellence

The paper winning the 2022 Leo Esaki Award was selected from over 144 articles that were published in 2022. The paper is entitled, *"Efficient Erase Operation by GIDL Current for 3D Structure FeFETs With Gate Stack Engineering and Compact Long-Term Retention Model".* This paper appeared in the November 2021 issue of the *IEEE Journal of the Electron Devices Society* and authored by Fei Mo, Jiawen Xiang, Xiaoran Mei, Yoshiki Sawabe, Takuya Saraya, Toshiro Hiramoto, Chun-Jung Su, Vita Pi-Ho Hu, and Masaharu Kobayashi.

The award will be presented during the IEEE EDS International Electron Devices Meeting to be held in December 2023. In addition to the award certificate, the authors will receive a check for $2,500 to be shared equally among all authors. On behalf of the Electron Devices Society, I would like to congratulate the authors for this achievement.

Arokia Nathan
EDS Vice-President of Publications and Products

2022 EDS George E. Smith Award

A high priority of the Electron Devices Society (EDS) is to recognize and enhance the quality of papers published in EDS archival literature. The George E. Smith Award was established in 2002 to recognize the best paper appearing in a fast turn-around archival publication of EDS, targeted to the *IEEE Electron Device Letters*. Among other criteria including technical excellence, an important metric for selection for the award is comprehensive and impartial referencing of prior art.

The paper winning the 2022 George E. Smith Award was selected from over 506 articles that were published in 2022. The paper is entitled, *"Demonstration of Multiply-Accumulate Operation With 28 nm FeFET Crossbar Array."* This paper appeared in the December 2022 issue of the *IEEE Electron Device Letters* and authored by Sourav De, Franz Müller, Nellie Laleni, Maximilian Lederer, Yannick Raffel, Shaown Mojumder, Alptekin Vardar, Sukhrob Abdulazhanov, Tarek Ali, Stefan Dünkel, Sven Beyer, Konrad Seidel, and Thomas Kämpfe.

The award will be presented during the IEEE EDS International Electron Devices Meeting to be held in December 2023. In addition to the award certificate, the authors will receive a check for $2,500 to be shared equally among all authors. On behalf of the Electron Devices Society, I would like to congratulate the authors for this achievement.

Arokia Nathan
EDS Vice-President of Publications and Products

Members Named Recipients Of 2023 Ieee Medals

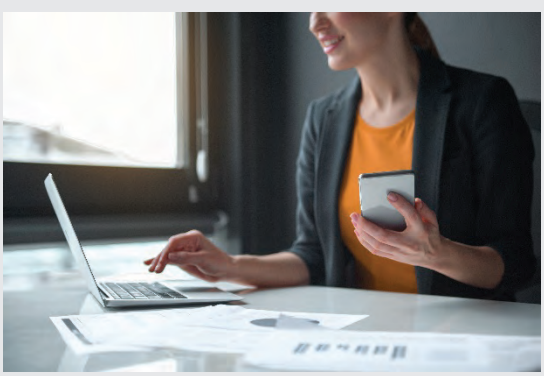
Three EDS members were named 2023 IEEE Medal recipients. Please be sure to visit the IEEE website at https://corporate-awards.ieee.org/recipients/current-recipients/ to view all the award recipients.

IEEE Medal for Environmental and Safety Technologies

Tatsuhiko Fujihira, David James Coe, and Gerald Deboy

"For contributions to the concept and realization of superjunction power devices that significantly improve power efficiency."





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https://www.ieee.org/membership/benefits/index.html

Call for Nominations
2022-2023 IEEE EDS Region 9 Biennial Outstanding Student Paper Award

Description: Awarded to promote, recognize, and support meritorious research achievement on the part of Region 9 (Latin America and the Caribbean) students, and their advisors, through the public recognition of their published work, within the Electron Devices Society's field of interest: All aspects of the physics, engineering, theory and phenomena of electron and ion devices such as elemental and compound semiconductor devices, organic and other emerging materials based devices, quantum effect devices, optical devices, displays and imaging devices, photovoltaics, solid-state sensors and actuators, solid-state power devices, high frequency devices, micromechanics, tubes and other vacuum devices. The society is concerned with research, development, design, and manufacture related to the materials, processing, technology, and applications of such devices, and the scientific, technical and other activities that contribute to the advancement of this field.

Prize: A distinction will be conferred in the form of an Award certificate bestowed upon the most outstanding Student Paper nominated for the two-year period. The prize will be presented at either the Latin American Electron Devices Conference (LAEDC) or the Symposium on Microelectronics Technology and Devices (SBMicro). In addition to the recognition certificate, the recipient will receive a subsidy of up to $1,500 to attend the conference, where the award is to be presented. There will be a formal announcement of the winner in a future issue of the EDS Newsletter. The winner will also receive up to three years of complimentary IEEE and EDS student membership, as long as winner remains eligible for student membership.

Eligibility: Nominee must be enrolled at a higher education institution located in Region 9. In the case of a co-authored paper, only eligible co-authors may be nominated. Papers should be written in English on an electron devices related topic. Papers should have been published, in full-feature form, during 2022-2023 in an internationally recognized IEEE sponsored journal or conference in the field of electron devices related topics. Statements by the student and by the faculty advisor should accompany the nomination. Nominator must be an IEEE EDS member. Previous winners of this award are ineligible. There must be a minimum of five nominations submitted in order for the award to be administered for that year.

- **Basis for Judging:** Demonstration of Nominee's significant ability to perform outstanding research and report its results in the field of electron devices. Papers will be judged on: technical content merit, originality, structure, clarity of composition, writing skills, overall presentation. These criteria will be weighted by the assessment of the nominee's personal contribution and the linkage of the nominated work to the nominee's career plans.
- **Nomination Package:**
  - Nominating letter by an EDS member (it may be the faculty advisor)
  - A brief one-page (maximum) biographical sketch of the student
  - 1000 words (maximum) statement by the nominated student describing the significance and repercussion of the nominated work within the wider scope of the nominee's career plans
  - 400 words (maximum) statement by the faculty advisor under whose guidance the nominated work was carried out. It should unmistakably state the faculty advisor's support of the nomination, and clearly explain the extent of the nominated student's contribution, as well as its relevance for the overall success of the reported work.
  - A copy of the published paper

Timetable:
- Submit your nomination online: https://ieeeforms.wufoo.com/forms/zvywrvw03cy9rx/
- Nominations are due no later than **15 February 2024**
- Winners will be notified by April 2024
- Recipients may choose to have the formal presentation of the award at either one of the conferences: LAEDC or SBMicro

For more information contact: Laura Riello, EDS Executive Office
l.riello@ieee.org or 732-562-3927

Lessons from a life's journey

Sarah Kurtz
University of California, Merced

When I was a girl, I assumed I would grow up to be a piano teacher, with kids to take care of, but giving piano lessons after school each day. Of the women I met, that seemed to be the most interesting career–otherwise, I could just take care of the kids… I was fortunate that my parents set the expectation that I would go to college, though I didn't know what I should study–maybe music so I could be a piano teacher? But, I was good at math, so maybe I could apply that to chemistry. Then, when I was a junior in college, a fellow student suggested that I apply to a summer research program at Yale University. I didn't know what research was, but I enjoyed it and decided to go to graduate school. I ended up with a Ph.D. in Chemical Physics from Harvard University. I've been fortunate to have been guided by many people over the years. Here I recall my research journey, highlighting lessons I learned along the way.

As a graduate student at Harvard, I studied with Roy Gordon. It was just after the OPEC oil embargo. He had a vision of making solar cells at low cost by depositing the layers of a solar cell on the glass as it cooled from the float line, providing a solution to the energy crisis. The deposition system I built deposited aluminum oxide as a diffusion barrier (to block sodium moving out of the glass), tin oxide as a transparent conductor, p-i-n layers of amorphous silicon (the active layers), and metal to make the final contact. The cells were not very efficient, but I learned a lot about materials deposition and characterization. Perhaps more importantly, I learned about identifying new research directions: Roy Gordon was known as a theorist, but when the world had a problem to be solved, he undertook to solve it, even though that meant developing experimental skills. Researchers may need to change direction when the world confronts a new problem. I might not have been brave enough to change research directions later in my career if I had not seen Roy Gordon tackle that new, important problem.

After graduating, I joined Jerry Olson at the Solar Energy Research Institute (SERI) studying III-V multijunction cells. He had just patented the GaInP/GaAs solar cell and we undertook to implement the concept. At the time he applied for the patent, it was well known that GaInP is an alloy that phase separates into GaP and InP, so it was "known" that his idea would not be successful, and SERI chose not to retain rights to the patent. However, our studies showed that if the fluxes of the Ga and In precursors are appropriately controlled, it is possible to grow a high-quality single-crystal $Ga_xIn_{1-x}P$ lattice matched to GaAs. Today, GaInP is used in multijunction solar cells on satellites and some Mars rovers, as well as in red LEDs. I learned from Jerry Olson to be open-minded. It is a real breakthrough when someone shows that conventional wisdom is wrong. In this case, it enabled a new technology. When the technology was transferred into production, SERI (now the National Renewable Energy Laboratory-NREL) had to ask the U.S. Department of Energy to return the title of the patent so the technology could be licensed. More generally, being open minded (*e.g.* looking at both sides of things or considering the other person's perspective) leads to innovations and solutions that might otherwise be ruled out because they are "known" to not work or because they are somehow flawed.

Our solar cells achieved 40% efficiency, but the industry had difficulty integrating them into working systems. I made a major career change to study the reliability of solar panels and systems. Although my efforts didn't enable the 40%-efficient cells to succeed, I was able to contribute to reducing and quantifying the risk associated with wide-scale deployment of solar panels. These are useful to the world if they last 20–30 years, but a problem for the world if they fail after a couple of years. I learned many lessons from the 10 years I spent studying photovoltaic reliability, but a key one is that to be successful, good devices must be delivered consistently. If a company made the perfect module, but then manufactured a million of them without adequate concern for quality control, not only would the company go out of business, but the world would conclude that that product won't work. The lesson on consistency may feel at odds with a lesson I learned from John Benner (one of my supervisors at NREL): he called it the 80–20 rule, but it has lots of other names. It's essential that 80% of the benefit is achieved with 20% of the effort. So, I can choose between "doing a job right" and putting in the full 100% effort to reach the 100% point for one task, or doing 20% of the effort to complete 80% of five times as many tasks. In the case of photovoltaic reliability, though consistency is important, it is also essential to cut some corners, so the 80-20 rule is essential. Doing the full testing to

quantify the lifetime of a module takes years. By the time the full testing is completed, the results are irrelevant as the industry has moved on to a new product. So, doing 80% in 20% of the time enables the launch of a product in a timely way with the confidence that it will last many years, but without quantifying how many years that will be.

About five years ago, I moved to the University of California Merced, and, again following Roy Gordon's lead, I undertook a new direction: to understand how solar electricity can be coupled with storage to drive our electrical grid through the night and year-round. We find that there are many energy technologies and that, together, they can solve the world's energy problems, but none of them is perfect. A key lesson I've learned is "we need to stop being against the things we aren't 100% for." No energy solution is perfect, so we should choose a mix with small imperfections to assemble an energy system that will be better than today's even though it won't be perfect.

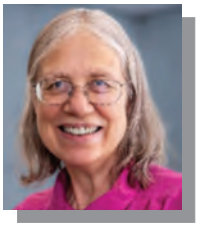
I've had many wonderful role models over the years. Nancy Haegel is a very special one–she has shown me many things, including how to chip away at difficult tasks by taking a step at a time–an essential approach when crossing a minefield, which is often what today's world feels like. My first role models were my parents (and, later, my entire family) who taught me to treat everyone with respect and to embrace and value individuals' strengths while minimizing any need to expose their weaknesses.

With my research I strive to help develop low-cost, effective technical solutions to the world's problems, a career I have found exciting and gratifying and that I highly recommend to anyone interested in engineering. At the same time, I find I can often have the biggest impact by caring for and improving the lives of those around me. Treating everyone with respect and supporting every person is essential to solving the world's technical problems as well as social problems.

For successful research in today's rapidly moving world, lessons I've learned include:

- As research problems are solved and new problems arise, some researchers should tackle those new problems even if they aren't experts in that area.
- We should recognize when it's not necessary (or advantageous) to do 100% of the job. The 80-20 rule suggests that we may choose to complete 80% of five tasks with the same effort it takes to complete 100% of one task. Even then I still have items on my "to-do" list that are at 0% completion.
- We should be open-minded–being open to ideas that are different from what we believe opens the door to innovation and advancements
- A corollary: We should accept imperfect solutions. Solar and wind energy are challenged when the sun sets or the wind stops blowing, but could storage coupled with flexible loads enable them to meet our energy needs? Fossil fuels are causing global warming and other pollution, but could research enable them to be used cleanly? Nuclear projects are blocked because of public safety concerns, but could they be made safe? Might the Allam cycle, small modular reactors, and enhanced geothermal improve our lives as we pursue my vision: "The beautiful thing about renewable energy is that the more you use it, the cheaper it gets, which paves a pathway to prosperity for the whole world."

I hope these thoughts will be useful to electrical engineers and others who undertake to solve today's problems–the world needs you!



Sarah Kurtz obtained her Ph.D. in 1985 from Harvard University and now works at the University of California Merced after more than 30 years working at the National Renewable Energy Laboratory, in Golden, CO. She is known for her contributions to developing multijunction, GaInP/GaAs solar cells, supporting the Concentrator Photovoltaic (PV) industry, and leading efforts on PV performance and reliability. Her work has been recognized with a jointly received Dan David Prize in 2007, the Cherry Award in 2012, the C3E Lifetime Achievement Award in 2016, and induction into the National Academy of Engineering in 2020. At the University of California Merced she is working both to help the university grow and to support the Energy Transition through a variety of studies, including a current study on long-duration energy storage.

The Journey of an Iranian-American Pioneer in MEMS and Micro-Instrumentation

Mina Rais-Zadeh
Group Supervisor, Advanced Microsensors and Microsystems,
NASA Jet Propulsion Laboratory, California Institute of Technology

I am an Iranian-American electrical engineer and professor who has made significant contributions to the field of microelectromechanical systems (MEMS) and micro-instrumentation. I began my academic journey in Iran, where I attended Farzanegan Middle and High School which is a part of the National Organization for Development of Exceptional Talents (NODET) educational system. I excelled academically and was ranked 9th in the national entrance exam (Konkour) in the area of mathematics in 1998. This was a significant achievement, as around 400,000 students participate annually in Konkour, considered one of the most rigorous and challenging academic examinations in the world.

After completing high school, I went on to study electrical engineering at the Sharif University of Technology in Iran. Sharif University is one of the top engineering schools in Iran and the Middle East, and I excelled in my studies there. I completed my undergraduate degree in electrical engineering and then moved to the United States to pursue my graduate studies in electrical and computer engineering at the Georgia Institute of Technology.

My research at Georgia Tech focused on MEMS and RF (radio frequency) devices, which led to breakthroughs in the design and fabrication of high-Q inductors and tunable passive components for use in wireless communication systems. Following my Ph.D., I continued my research as a Postdoctoral Research Fellow at Georgia Tech, where I developed phonon-phonon scattering models to predict the limit of quality factors in micromechanical resonators. This work, published in Transducers 2009, was cited more than 200 times and has important applications in the field of resonant devices and microsystems.

In 2009, I joined the faculty at the University of Michigan, Ann Arbor, as an Assistant Professor of Electrical Engineering and Computer Science. At the University of Michigan, my research focused on gallium nitride (GaN) MEMS, resonant sensors, and phase-change electrical and optical devices. One of my significant contributions was the demonstration of the first GaN bulk acoustic wave (BAW) resonator, which has important applications in wireless communication systems. My team also developed the highest-Q GaN micromechanical resonator, which is crucial for achieving low phase noise and high sensitivity in oscillators and filters. I was promoted to the rank of Associate Professor with tenure in 2014 and received several prestigious awards and honors, including the NSF CAREER Award, ONR Young Faculty Award, NASA Early CAREER Faculty Award, and the IEEE Sensors Council Technical Achievement Award. In addition to my research, I supervised numerous graduate students and postdoctoral researchers and have inspired many young people to pursue careers in engineering and science.

In 2016, I joined the Jet Propulsion Laboratory (JPL) (on sabbatical leave from U. of Michigan) as a group supervisor for the Advanced Optical and Electromechanical Microsystems Group. In this role, I lead a team of researchers and engineers in the development of advanced MEMS and micro-instrumentation for use in space exploration and other applications. One of my major accomplishments at JPL has been the work on developing more reliable microvalves for the International Space Station (ISS) spacecraft atmospheric monitoring instrument (S.A.M.).

I also delved into the development of high-temperature tolerant GaN resonators for harsh environment applications, including surface missions to Venus. The resonators are able to withstand extreme temperatures and harsh environments, making them an ideal choice for space applications where traditional resonators may not function properly. I also continued my work on resonant IR detectors by developing random sparse arrays of resonant IR detectors. Such arrays of detectors have important applications in focal plane array (FPA) for harsh environments, where there are significant challenges in interfacing the sensor head with the readout electronics by routing the signal in the 3rd dimension.

My contributions to NASA and JPL have earned me several awards and accolades, including several Team Awards, the designation of Senior Research Scientist (SRS), and Principal at JPL. The SRS designation, equivalent to the full professor level, is a testament to the recognition of the significance and impact of my work by both JPL and the external community. Similarly, the Principal designation is awarded to acknowledge sustained outstanding individual contributions in advancing scientific or technical knowledge or advancing the implementation of technical and engineering practices for projects, programs, or the JPL Institution as a whole.

My contributions in the field of MEMS and micro-instrumentation have paved the way for advancements that will lead to a better understanding of our world and beyond. As a leading figure in the field of space microsystems, I continue to shape the future of MEMS and micro-instrumentation, specifically for planetary, Earth, and Astrophysics applications.

My journey in science and engineering has been filled with challenges, but also with moments of great joy and satisfaction. From my early days as a student in Iran to my

current position as a group supervisor at JPL, I have been fortunate to work with great students, peers, and technologists on cutting-edge research and make contributions that have a real impact.

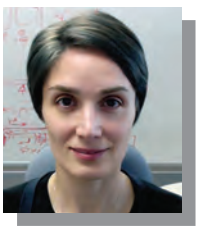
As women in engineering, we possess the potential to make remarkable contributions, shape the future, and transcend the boundaries of imagination. We should embrace our unique perspectives, unyielding determination, and untapped potential. The realms of science and engineering hold no limits to what we can achieve. In our pursuit, we shall embrace each challenge as a lesson learned, guiding us towards greatness. With each opportunity, we learn, grow, and expand our horizons.

The IEEE Electron Device Society community stands as a collective of like-minded individuals, ready to support and uplift one another. Our curiosity, perseverance, and unwavering dedication are paramount to achieving our goals. I believe that staying curious, persevering, and never giving up on our dreams are key to achieving our goals. Being surrounded by supportive mentors and allies, and seeking out opportunities to learn and grow are also important for success. It is important to remember that one's gender does not define their abilities. Anyone can make a significant impact in science and engineering if they stay committed and work hard. It is important to take risks, be bold, and not be afraid to fail. It is not the number of failures that matter, it is the impact of the good work that matters at the end.

As women in science and engineering, we hold a powerful position in breaking barriers and shattering stereotypes. In this remarkable journey, we find strength in the Women in EDS—an essential community that supports and empowers women in science and engineering. Let us use this platform to amplify our voices, celebrate our achievements, and uplift each other as we strive for excellence.

My research is now more focused on space applications of MEMS and micro-instrument and microsystems with emphasis on extreme cold and hot environments. MEMS is known for having a low Size, Weight, and Power (SWaP), which is critical for space missions, as the size and mass of the payload directly impacts the cost of the mission. However, qualifying and characterizing MEMS for space is a less explored area. The space environment is known for its harsh conditions, including extreme temperatures, radiation exposure, extreme pressures, and sometimes existence of corrosive gases. When developing space instruments, several factors must be considered to ensure their survivability in this environment. These factors include the selection of materials that can withstand the harsh conditions, designing for radiation hardness and fault tolerance, developing effective thermal control systems, and ensuring the proper packaging of components. Often times, even if the lifetime of the mission is short, the required shelf time is long and the instruments must be tested thoroughly to ensure they can function reliably in space for extended periods. My future research will focus on developing and qualifying MEMS instruments that meet the challenging requirements of space. These are some of the interesting future research directions in MEMS and microsystems in my opinion:

1) Material Selection and Harsh Environment Survivability:
   One exciting fundamental research area is the careful selection of materials that demonstrate exceptional resistance to the rigors of space. Enduring the extreme temperatures and enduring corrosive agents will be vital for the longevity and reliability of MEMS instruments.
2) Radiation Hardness and Fault Tolerance:
   Radiation poses a formidable threat to electronics in space. Our quest will involve developing radiation-hardened MEMS devices and exploring fault-tolerant architectures that can withstand radiation-induced challenges.
3) Effective Thermal Control Systems:
   Thermal management is a pivotal aspect in space missions. Designing efficient micro-instruments to self-regulate their temperature, or endure and function in extreme temperatures, ensuring their optimal performance and prolonged operation is a fascinating area of research.
4) Robust Packaging and Long Shelf Time Testing:
   The packaging of components plays a pivotal role in ensuring the integrity of MEMS instruments during launch and deployment.
5) Mission-Specific Customization:
   Each space mission comes with unique challenges. Future research need to embrace the concept of mission-specific customization, crafting MEMS instruments tailored to the demands of each space exploration endeavor.



Mina Rais-Zadeh (S'03-M'08-SM'12) received the B.S. degree in electrical engineering from Sharif University of Technology and M.S. and Ph.D. degrees in Electrical and Computer Engineering from Georgia Institute of Technology in 2005 and 2008, respectively. From 2008 to 2009, she was a Postdoctoral Research Fellow at Georgia Institute of Technology. In 2009, she joined the University of Michigan, Ann Arbor, as an Assistant Professor of Electrical Engineering and Computer Science (EECS). From 2014-2018 she had been a tenured Associate Professor in EECS with courtesy appointment in the Department of Mechanical Engineering. She is currently leading the MEMS and micro-instrument development activity at JPL as a group supervisor for the Advanced Microsensors and Microsystems Group.

IEEE EDS SHE in ECE Event—2023

By Durga Misra

With the support from the IEEE Electron Devices Society (EDS) and in collaboration with the IEEE Circuits and Systems Society (CASS) and Electrical and Computer Engineering Department at NJIT, a "One-Day Summer Camp for Female High School and Middle School Students" was hosted on NJIT campus on 27 June 2023. The focus of the event was to encourage female students to join engineering, especially in electrical engineering and/or computer engineering. The program was organized from 8:30 AM to 3:30 PM. The theme was **S**oaring **H**igh-powered **E**xcellence (SHE) i.e., SHE in IEEE and SHE in Electrical and Computer Engineering (ECE).

Snapshots of the IEEE EDS SHE in ECE Event–2023

Students were recruited by sending emails and mailing postcards to the NY-NJ area school counselors. The program was listed in IEEE's vtools. A dedicated website (https://she.njit.edu/) was created to inform the community members and registration. The program was regularly updated on the website. All university guidelines were followed and to ensure the safe dismissal of students, an organized exit plan was created.

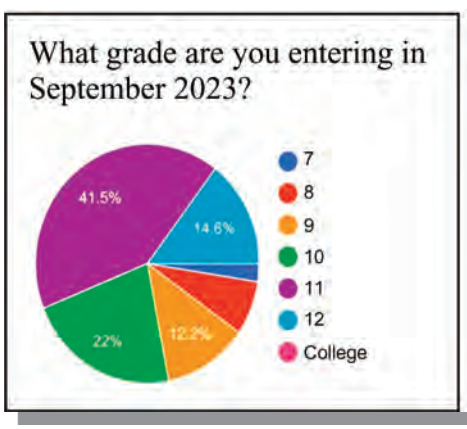
More than 80 girls entering 7th to 12th grades from the local schools attended the event. The student group included many minority students. Students were welcomed by Prof. Durga Misra, EDS Chapter Chair. He encouraged the students to develop new technologies in the high-tech industry and in space research and encouraged the young female students to be the leaders of technology and innovation. He emphasized the role of IEEE such as Try Engineering programs and appreciated the financial support from the IEEE EDS and IEEE CASS.

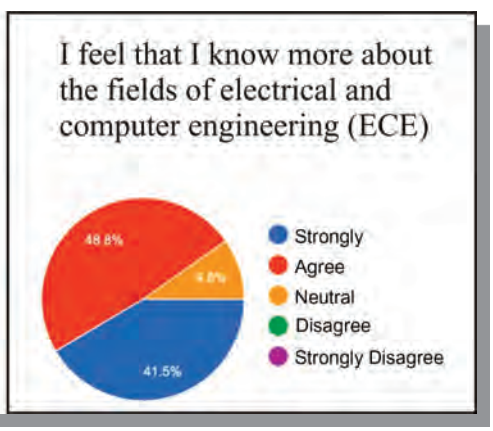
The opening remark was given by Ms. Marjorie Perry, CEO, and sole principal of MZM Construction. Ms. Perry inspired the girls to be engineers and mentioned how electrical engineers and computer engineers are leading the way from self-driving cars to communication using their mobile phones. She encouraged them to do well in science and mathematics in school.

Following the opening keynote, a panel discussion was held. The panel consisted of women faculty members and industry leaders in the engineering field. The faculty panelists were Prof. Ratna Raj of the Elect & Comp Eng Department and Prof. Kerri-lee Chintersingh of Chem & Materials Engineering. The industry panelists were, Ms. Chitra Venkatraman, retired Telecommunication Engineer from Nokia; Dr. Anisha Apte, Sr. Design Engineer at Synergy Microwave Corporation; and Dr. Charlotte Blair, Technical Manager, ANSYS and Women in Engineering (WiE) Chair of IEEE Region 1; Ms. Carol Benitez, Vice President of Operations at Greener by Design and Ms. Amira Feknous, Strategic Teleport Partners at SES Satellites. The panel was moderated by Ms. Susan Gross, Vice Provost for Enrollment Management at NJIT. Most of the panel members talked about their high school days and explained how they selected their career as an engineer, especially an electrical engineer. They advised the students how they can think about selecting their career. The panelists told the students to be strong and brave as female electrical engineers because female engineers make a highly positive impact on new technology development and innovation. They also suggested exploring more about the IEEE TRY Engineering programs and the WiE initiatives to select their engineering career.

After the panel discussion the students were divided into four groups: (i) a visit to Makerspace; (ii) the university campus tours; (iii) Hands-on-Activity; and (iv) the current electrical and computer engineering female undergraduate students' panel. The groups were rotated. In the Makerspace the students were experienced with 3D Printing and other machines that the students use to make new things. As part of the campus tour the students experienced the conditions and atmosphere of a college campus. The hands-on activity was guided by Dr. Byron Chen, Director of Labs of the ECE Department. The students were given the *Snap Circuits Green Energy* from Elenco Electronics and a multimeter to work on several circuits using solar energy and wind energy. They were excited to build their projects and wanted more time. The fourth group was with current female ECE students to "ask anything" in an informal environment.

During lunch time, Mr. Steven Eck, Director of NJIT's admission office guided the high school seniors through the application process and declared that the application fee would be waived if they applied to ECE Department or any engineering program for their undergraduate program. An excellent breakfast and a hot lunch were provided to the students. Ms. Teri Bass and Ms. Ryoko Mathes of the ECE Department of NJIT worked tirelessly from January 2023 to make the project a success. Around 15 ECE students worked as volunteers to help the students to have an excellent time.





Following the program, we had a survey to receive feedback from female high school and middle school students. More than 50% of the students who attended the program responded. Out of the responders, we had 41.3% Asians, 43.9% African Americans and Latinos, 9.8% Whites, and 5.0% others including American Indians. The results of the survey are shown in the left.

The 5th IEEE-IFETC 2023 Women in EDS and Young Professional Session

By Bonnie Gray, Laura Marcela Sabogal, Arokia Nathan, Samar Saha, Abhishek Raol, and P. Susthitha Menon

IEEE Electron Devices Society (EDS) sponsored the Women in EDS (WiEDS) and IEEE Young Professionals (YP) joint session that closed the first day of the 5th IEEE International Flexible Electronics Technology Conference (IFETC) held at the Silicon Valley Doubletree Hilton Hotel in San Jose, California. The session was held on 14 August 2023 and featured the theme: *Diversity in the Next 75 Years of the Transistor: Off to a Good Start*. The session was organized by Dr. Susthitha Menon (Universiti Kebangsaan, Malaysia), Marcela Sabogal (University of Los Andes, Colombia), and Dr. Bonnie Gray (Simon Fraser University, Canada). Dr. Gray also moderated the event, which featured 4 panelists in varying fields relevant to WiEDS and YP: Dr. Alba Avila (University of Los Andes, Colombia), Dr. Tse Nga Ng (University of California San Diego), Dr. Nazek El Atab (King Abdullah University of Science and Technology, Saudi Arabia), and Dr. Martina Aurora Costa Angeli (Free University of Bozen-Bolzano, Italy). This event was supported by the IEEE-IFETC Organizational and Steering Committee, IEEE EDS, IEEE WiEDS, and IEEE YP.

Attended by 25 people, the audience was first presented with opening remarks by Dr. Gray, followed by video presentations on WiEDS by Dr. Menon and YP by Ms. Sabogal. Next, Dr. Avila set the stage for the discussion that followed through her video presentation highlighting her extensive work on making science and technology more widely accessible and inclusive. Next, Dr. Gray posed questions to the three in-person panelists (Drs. Ng, Angeli, and El Atab) on topics that included: increasing diversity and inclusivity in EDS; the importance of mentorship; overcoming imposter syndrome; and keeping passion for engineering. The audience was highly enthusiastic and continued with their own questions that filled the remainder of the two-hour session. Afterwards, the panelists and Dr. Samar Saha, the General Chair of IFETC 2023 and with whom the event would not have proceeded, received small thank-you gifts from EDS.

Thank you to IFETC, WiEDS, YP, the organizers, panelists, and especially the audience, for making this event a huge success!

5th IEEE IFETC 2023 Women in EDS (WiEDS) & Young Professionals Panel (from L to R facing the audience: Drs. Gray, Ng, Angeli, and El Atab) and Audience.

Humanitarian News

ED Malaysia Chapter-ED Cares For The Environment

By Maizatul Zolkapli

On 10 June 2023, a community service event took place at Pantai Morib Selangor, organized by the IEEE Electron Devices Society Malaysia Chapter and co-organized by the Institute of Electrical and Electronics Engineering UiTM Student Branch (IEEE UiTM SB) and IEEE Power & Energy Society Malaysia Chapter. The main goal for the members was to actively participate in environmental conservation efforts by effectively removing litter and fostering a culture of cleanliness at our local beach.

A group of 38 individuals, including students and faculty members from the School of Electrical Engineering, College of Engineering UiTM Shah Alam, actively engaged in the beach clean-up. Their collective passion demonstrated their commitment to making a positive environmental impact.

Upon reaching the beach, the participants were organized into smaller groups to ensure optimal efficiency of work. Each group was assigned a specific area to focus on during the clean-up process. The activities carried out during the beach clean-up encompassed:

- Litter gathering: participants collected with meticulous care a diverse range of litter, such as plastic waste, cigarette butts, and food wrappers;
- Education and raising awareness: Throughout the event, participants actively interacted with beachgoers and nearby visitors, imparting knowledge about the significance of environmental preservation and the upkeep of cleanliness.

The participants cleaning up the beach.

Thanks to the dedicated involvement of 38 individuals who exemplified their dedication to environmental conservation, the beach clean-up event organized by the members achieved its objectives. Through our collective efforts, we made a significant and positive difference to the local beach, while simultaneously raising awareness about the importance of upholding cleanliness within our community.

We express our heartfelt appreciation to all the participants for their unwavering commitment and diligent efforts in ensuring the success of this event.

The chapter maintains its steadfast dedication to arranging forthcoming community service endeavors aimed at enhancing society's well-being.

STEM4FUN: STEM For All

By Maizatul Zolkapli, Ahmad Sabirin Zoolfakar, Rozina Abdul Rani, and Azrif Manut

On 13 June 2023, the chapter collaborated with the IEEE UiTM Student Branch (IEEE UiTM SB) to organize a community event at Sekolah Kebangsaan Pendidikan Khas Selangor. The primary objective of the program was to promote an interest in STEM among special needs students. A team of 22 enthusiastic individuals from IEEE UiTM SB, led by Ir. Dr. Maizatul Zolkapli, actively participated in assisting 111 special needs elementary school students, including those with hearing impairments and learning disabilities of both low and high functional levels. Their dedication and commitment showcased their determination to make a positive educational impact.

The special needs students actively participate in STEM activities.

During the event, each team member was assigned to smaller groups of students to ensure an efficient and effective learning experience. The activities carried out during the event included electronics block experiments for hearing-impaired students, solar car assembly for all groups, and engaging magnetic building block play for students with learning disabilities. Additionally, the students with learning disabilities had the opportunity to construct a DIY wooden reptile robot, providing them with both knowledge and hands-on experience in STEM fields.

Thanks to the hard work and dedication of the IEEE EDS and IEEE UiTM SB members, the community event was a resounding success. The special needs students were given equal opportunities to explore STEM education, and their interest in the field was nurtured through these inclusive and supportive activities. The program aimed to create an inclusive and accessible learning environment for individuals with diverse abilities, particularly in the younger generation. The organizers expressed their gratitude to all participants, Jabatan Pendidikan Negeri Selangor, and Sekolah Pendidikan Khas Selangor for their cooperation and warm welcome. Through collective efforts, this event made a significant positive impact on the younger generation's interest in STEM and raised awareness about the importance of supporting special needs students in pursuing STEM education.

~ Sharma Rao Balakrishnan, Editor

EDS-Centre of Excellence, Heritage Institute of Technology

By Mousiki Kar

The center, in collaboration of IEEE SIGHT (Special Interest Group on Humanitarian Technology) Kolkata Section organized a special "Pre-University STEM Training Workshop" for teachers of Vivekananda Adarsha Vidyalaya located in Sankijahan, a remote village in West Bengal, India. The workshop was held on 29 April 2023. The school aims at bringing children of fishermen and agricultural workers to education at a high quality school and providing them basic academic resources, quality mentoring & one meal a day. The school is run by an NGO and currently provides primary education to 182 children. The workshop was attended

Speakers and participants of the seminar "Humanitarian Technology for Sustainable Development".

Outreach activity by the IEEE EDS CoE: Workshop using EDS-ETC kit at Shishu Tirtha.

by 11 primary school teachers who participated enthusiastically and wholeheartedly.

The centre, in collaboration with IEEE Kolkata Section SIGHT Group organized a seminar on the topic "Humanitarian Technology for Sustainable Development" which was held on 31 May 2023, at Heritage Institute of Technology, Kolkata. The event was attended by 196 academicians, professionals and students from across the state of West Bengal, India. The event began with Prof. Iti Saha Misra, Chair, IEEE Kolkata Section and Prof. Jawad Siddiqui, Chair, IEEE AP-S SIGHT presenting their past SIGHT projects. They encouraged the participants to think of simple technology-based solutions for society. Ms. Sudeshna Choudhury from TCS, India and Dr. Susanta Ray from Jadavpur University discussed various interesting scalable technology-based humanitarian projects. Dr. Mousiki Kar, Chair, coordinator of the center concluded the event.

The centre, in collaboration with IEEE SIGHT Kolkata Section organized at Shishu Tirtha, a primary school for the underprivileged, a workshop "**Empowering Young minds through STEM education**". It was run by the NGO **Society 5.0** on 12 July 2023. The workshop was designed to introduce young students from underprivileged backgrounds to the exciting world of science, technology, engineering, and mathematics (STEM) through hands-on learning experiences using EDS-ETC kits. The workshop conducted by Dr. Mousiki Kar, coordinator of the IEEE EDS Center of Excellence, aimed at inspiringing curiosity. Dr. Kar started off the workshop with a brief introduction to robotics, explaining what robots are, how they work, and their significance in today's world using age-appropriate language and visual aids to make the concepts easily understandable. The children were shown examples of robots used in everyday life, such as automated machines, robotic toys, and robotic vehicles. This segment aimed to connect the workshop subject matter with real-world applications. The children were also introduced to basic electronic circuits through interactive presentations and simple demonstrations. Each participant was subsequently provided with a pre-designed circuit building kit containing various components, such as motors, integrated circuits, LEDs, batteries, and switches. Dr. Kar, along with two undergraduate engineering student volunteers, demonstrated how to build basic circuits step-by-step, and the children followed along. The workshop was successful in sparking curiosity and interest in STEM among the 6 young participants of class IV through the hands-on exercises with electronics.

~Soumya Pandit, Editor

A Specialized High School Course for STEM Education: A Case Study of FEE-UNI

By Sandra Veljković, Miloš Marjanović, Emilija Živanović, and Danijel Danković

Years of experience and work with students have contributed to the publication of a paper, entitled "The Importance of Students' Practical Work in High Schools for Higher Education in Electronic Engineering" [1], that concerns the advancement of students' knowledge and their skills in practical implementations. STEM education has become increasingly important in today's world, as it provides students with practical skills and knowledge in science, technology, engineering, and math. This article presents a case study of a specialized high school course for STEM education and its impact on university students, as well as the benefits of collaboration between universities and high schools.

The case study was conducted at the Faculty of Electrical Engineering (FEE-UNI), where the specialized high school courses were organized for more than 500 high school students from different high schools and cities in Serbia, as described in [1]. In high schools, deductive learning with a teacher-centered approach is the norm, even for subjects like Physics and Informatics, which mainly consist of lectures, problem solving, and computational tasks. The courses focused on hands-on activities in STEM, and the students were later divided into groups and attended specific workshops under the supervision of FEE-UNI teaching staff.

The first of many realized courses was "Let's Put the Knowledge into Practical Work" aimed to provide practical knowledge of electronic components using an inductive "learning by doing" approach. The course objectives included interpreting electronic components' datasheets, identifying basic applications of electronic devices, employing principles of digital electronics, performing simulations of simple circuits, and assembling and testing electronic circuits on a protoboard. Over the course of 15 weeks, the course was organized for third and fourth-year high school students, assuming prior theoretical knowledge from Physics, Mathematics, and Informatics, as shown in Fig. 1.

Handouts, presentations, and computer simulations were used to accommodate different learning styles. The chosen tools for simulations of the protoboard layout, analog, and digital circuits were Fritzing, LTspice, and Logisim, respectively, as illustrated in Fig. 2.

Assessment methods include performance tasks/projects, homework, tests, academic prompts, and informal observations. A digital counter with a 7-segment display was selected for the project-based learning. Students are

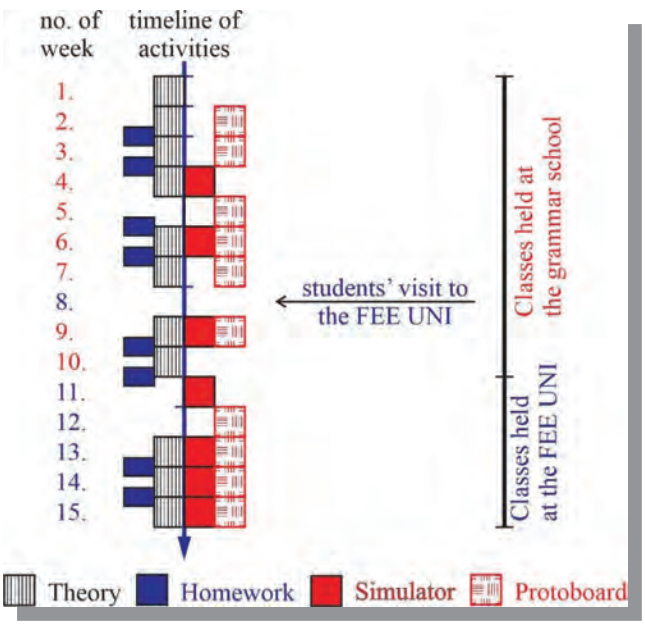


Figure 1. Course timeline with corresponding activities.

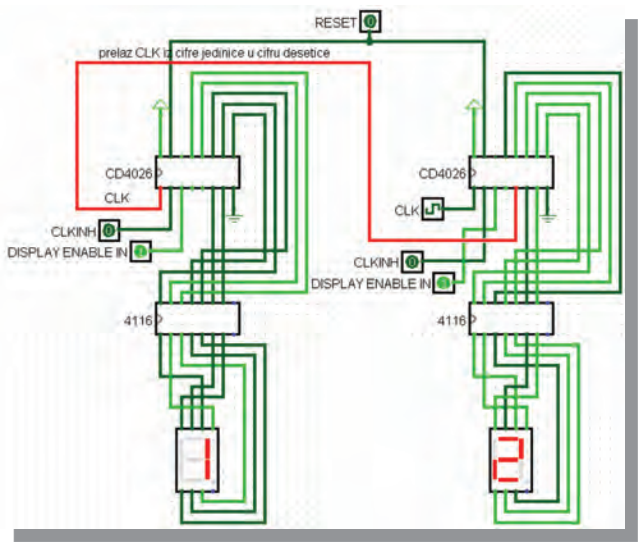


Figure 2. Student exercise–Decade counter, realized in Logisim.

expected to complete all activities individually or through three-member teamwork, with educators from the FEE-UNI teaching staff members. Each group proposed and implemented a project idea inspired by the STEM sessions, and as a result, 30 high school students wrote ten papers for the IEEESTEC conference.

The success of this initiative was acknowledged by IEEE, and grants were approved for the years 2021 and 2022 through the projects called "STEM visits IEEESTEC" and "Let STEM visit again IEEESTEC", respectively. The research showed that students having practical experience in high school achieved better results at university than those who had none. They studied not only to pass the exams but also to deepen their knowledge, gained self-confidence, and presented their ideas, as explained in [1]. The importance of IEEE support to FEE-UNI teaching staff in educational activities cannot be overstated. In return, students become acquainted with IEEE, implying early involvement in its activities. Participation in the IEEE supported conference motivates high school and university students to apply their knowledge through projects. Coordination between the state and universities is beneficial to improving the quality of higher education. However, universities need to take a step forward in initiatives and maintain connections with high schools. In this way, FEE-UNI was able to contribute to the content of the relevant national frameworks, and establishing this type of feedback makes access to funds for educational projects easier. Building positive professional and personal relationships between high school teachers and university professors is crucial to overcome bureaucratic barriers. Organizing workshops has proven to be an effective way to establish such relationships. Additionally, courses, either vocational for teachers or educational for high school and FEE-UNI students, have contributed to a favorable environment for further activities. The inclusion of STEM learning approach subjects in the high school curriculum can contribute to a better understanding of theory, provided it does not overburden students. Preliminary data indicate an expected positive impact on students enrolling in FEE-UNI, but this has yet to be confirmed.

In conclusion, the specialized high school course for STEM education presented in this case study demonstrates the benefits of hands-on activities in STEM and the importance of collaboration between universities and high schools. The success of this initiative shows that students with practical experience in high school achieve better results at university, deepen their knowledge, and gain self-confidence. It also highlights the importance of IEEE support to FEE-UNI teaching staff in educational activities and early involvement of students in its activities. Finally, this case study underscores the need for coordination between the state and universities and the establishment of feedback mechanisms to facilitate access to funds for educational projects. The IEEESTEC Conference [2], is a place where all these previously mentioned actions could be achieved, so our pleasure is to invite all interested students to write manuscripts for the IEEESTEC.

References

[1] Danijel Danković, Miloš Marjanović, Nikola Mitrović, Emilija Živanović, Milan Danković, Aneta Prijić, and Zoran Prijić, "The Importance of Students' Practical Work in High Schools for Higher Education in Electronic Engineering", IEEE Transactions on Education, vol. 66, no. 2, pp. 146-155, April 2023, doi: 10.1109/TE.2022.3202629.

[2] IEEESTEC Conference, Available on: https://ieee.elfak.ni.ac.rs/

Region 1 Mid-Hudson Annual Banquet

By Mukta Farooq

The IEEE Region 1 along with the EDS Mid-Hudson Valley Chapter hosted a Region 1 Mid-Hudson Annual Banquet on 2 May 2023 at the Villa Borghese in Wappingers Falls, New York. The event was open and free to all IEEE Region 1 current members. Each member could add a guest for a small fee. The total number of registrations was approximately 50. Rasit O. Topaloglu, Chair of the IEEE Mid-Hudson Section, gave the opening remarks and welcomed the attendees. Rasit shared that Region 1 comprises over 100 municipalities, with most of the members representing four IEEE societies: Electron Devices, Computer, Power and Energy, and Electronic Packaging. In addition, 4 IEEE student branches were also named: SUNY New Paltz, West Point Academy, Marist College, Vassar College. Rasit also named all candidates who achieved Senior and Fellow promotions in 2023 within IEEE Region 1. Mukta Farooq, IEEE Fellow and Chair of the Mid-Hudson EDS Chapter, then gave a short talk on Celebrating Electron Devices. This talk showcased the evolution of devices over time, and highlighted the groundbreaking contributions made by IBM in semiconductor technology.

L-R: Rasit Topaloglu, Ron Geiger, Mukta Farooq, Mukesh Khare

Mukesh Khare's talk

The featured presentation of the evening was by Mukesh Khare, General Manager, IBM Semiconductors, and VP, Hybrid Cloud Research who gave an inspiring talk on "Securing the Future of Semiconductors in the US". This presentation showed the path forward for the US to have a strong presence in semiconductor and packaging manufacturing. Dr. Khare shared details on what was being done to enable a secure future not only in the US, but also along the Hudson Valley. This talk was very timely and well-received, given that we were celebrating the 75th anniversary of the transistor! Listening to this talk, the newer professionals in the audience were encouraged about their prospects in semiconductors. Many thanks to Dr. Khare for carving out the time to give this presentation and thus enlightening the audience about what is happening in this field. The event was also a great opportunity for all attendees to network over dinner, and meet familiar faces as well as new professionals in the IEEE Region 1 area.

~ Michael Adachi, Editor

IEEE EDS Malaysia Annual General Meeting 2023

By Nurul Ezaila Alias and Hazian Mamat

The 33rd Annual General Meeting (AGM) of the ED Malaysia Chapter took place on 4 February 2023, at the prestigious Hotel Royale Chulan Damansara, located in Mutiara Damansara, Petaling Jaya, Selangor. The event was attended by 28 enthusiastic EDS members from various parts of Malaysia, representing the diverse and vibrant community of professionals in the field.

The AGM was conducted under the expert guidance of Assoc. Prof. Ir. Dr Sabirin who had previously served as the Past Chair from 2021 to 2022. Dr. Sabirin, with the assistance of Dr. Maizatul and Dr. Azrif, presented a comprehensive overview of the EDS events, activities, and financial status throughout the year 2022. This review highlighted the chapter's numerous accomplishments and underscored the dedication and hard work of all members involved.

One of the significant highlights of the AGM was the election of the new Executive Committee (Excomm) members for a two-year term. The election process was carried out meticulously, ensuring transparency and fairness. Members had the opportunity to cast their votes, and the results were eagerly awaited by all in attendance.

The newly elected Excomm members, who emerged victorious through the voting process, are as follows:

Chair	Ir. Dr. Hazian Mamat (no voting)
Vice Chair	Ir. Dr. Azrif Manut
Secretary	Ts. Dr. Nurul Ezaila Alias
Treasurer	Dr. Haslina Jaafar
Auditor	Prof. Dr. Zahirul Alam and Dr. Sharma Rao A/L Balakrishnan
Excomm	Dr. Aliza Aini Md Ralib, Dr. Iskandar Yahya, Ts. Dr. Suhana Mohamed Sultan, and Assoc. Prof. Dr. Rosminazuin Ab. Rahim

These individuals, with their diverse backgrounds and expertise, bring a wealth of knowledge and passion to

Attendees of the 33rd AGM of IEEE ED Malaysia Chapter members during the meeting.

their respective positions. The ED Malaysia Chapter is excited to have such dedicated individuals leading the way for the next two years, steering the chapter towards further growth and success.

During the AGM, the Excomm members of 2022 received special recognition. In acknowledgment of their outstanding contributions, all members of the previous Excomm were presented with well-deserved appreciation certificates, expressing gratitude for their hard work and commitment. The following volunteers received their awards from the IEEE ED Malaysia Chapter.

2022 Outstanding Volunteer Award	Ts. Dr. Nurul Ezaila Alias
2022 Outstanding Volunteer Award	Ir. Dr. Hazian Mamat
2022 Outstanding Student Volunteer Award	Mr. Lee Xiao Xian
2022 Outstanding Portfolio Award-Student	Dr. Iskandar Yahya
2022 Outstanding Portfolio Award-Student	Assoc. Prof. Dr. Badariah Bais
2022 Outstanding Portfolio Award-Student	Assoc. Prof. Dr. P Susthitha Menon

To foster a sense of companionship and create an opportunity for members to know each other better, ED family members were also invited to the evening event. The night was filled with laughter and joy as fun games were organized, creating a warm and welcoming atmosphere. Through these activities, the ED community deepened its bonds and forged new connections, strengthening the overall sense of belonging to the chapter.

The 33rd AGM of the chapter was an overwhelming success, celebrating the achievements of the past year while setting the stage for an even brighter future.

As the Chapter embarks on this new chapter of its journey, it is with great anticipation and enthusiasm that we look ahead to the exciting opportunities and accomplishments that lie ahead. With the support and active participation of its members, the Chapter will undoubtedly continue to thrive and make significant contributions to the field of engineering and related disciplines.

Stay tuned for more updates and upcoming events as we embark on an extraordinary year ahead with the ED Malaysia Chapter. Together, let us create a thriving community of engineering professionals, united by our shared passion and commitment to excellence.

ED Malaysia Chapter-2023 IEEE EDS Women In Engineering (WiEDS) Virtual Forum

By Nurul Ezaila Alias, Rosminazuin Ab. Rahim, Aliza Aini Md Ralib, and Hazian Mamat

In a ground-breaking initiative, the Chapter organized on 8 March 2023 its first-ever Virtual Live Forum in commemoration of International Women's Day. This exceptional program aimed to celebrate and empower women in the engineering field, providing a platform for them to share their experiences, motivations, and thoughts on this momentous occasion.

The Women in Engineering Forum featured insightful interviews with three esteemed and accomplished ladies, each recognized for their exceptional contributions to the field. The honored guests were as follows:

1) Ana Maria Bura Kufner - Talent Acquisition Project Manager, AT&S Malaysia, Kulim Hi-Tech Park.
2) Zalhan Md Yusof - Principal Researcher and Head of Photonics Technology Laboratory, MIMOS Berhad.
3) Dr. Anis Suhaili Bakri - Senior Engineer, Semiconductor Technology Development, MIMOS Berhad.

These remarkable women, through their dedication and expertise, have become trailblazers in the engineering domain, inspiring countless others with their achievements. The interviews provided an opportunity for them to reflect on their journey, share their insights, and offer advice to aspiring professionals.

The forum was skilfully moderated by Assoc. Prof. Dr. P. Shusthita Menon, a renowned academic from Universiti

Poster of 2023 IEEE EDS Women In Engineering (WiEDS) Virtual Forum.

Kebangsaan Malaysia. Dr. P. Shusthita Menon, who also serves as a Member of the IEEE ED Board of Governors, EDS Educational Activities, and Vice-Chair of EDS R10 SRC, as well as the Past Chair of the IEEE ED Malaysia Chapter, brought her vast expertise and experience to facilitate engaging discussions.

Themed "Women in Engineering Leads The Way," the forum encapsulated the essence of empowering women in the field. With an attendance of 25 participants, the event covered a range of topics, delving into each woman's unique journey and experiences. Some of the key discussion points included their decision to pursue a career in electronic engineering academia, their educational path, the specific challenges and successes they encountered, achieving work-life balance, and the invaluable advice they had for others in the field.

The Chapter takes pride in organizing such impactful events that not only celebrate the achievements of women but also promote inclusivity and gender diversity within the engineering field. Through initiatives like the Women in Engineering Forum, the Chapter continues to foster an environment that nurtures and empowers women professionals, creating a more equitable and vibrant community.

As the Chapter looks to the future, it remains committed to organizing engaging programs and events that foster knowledge sharing, professional development, and networking opportunities. Stay tuned for more updates on upcoming events and initiatives as we work together to shape a more inclusive and diverse engineering landscape.

2023 IEEE EDS Malaysia Raya Gathering

By Nurul Ezaila Alias, Rosminazuin Ab Rahim, Aliza Aini Md Ralib, and Hazian Mamat

In conjunction with the monthly meeting held in May, the Chapter organized a celebratory gathering for the committee members. The event aimed to foster a sense of camaraderie and celebrate Eid among the members. In the spirit of Eid celebrations, the gathering took place on 17 May 2023 at the Kulliyyah of Engineering, International Islamic University Malaysia (IIUM). The event was attended by EDS ExCom members and Chapter members both in person and through video conferencing. This social event was organized with the hope of promoting positive engagement among EDS members.

Raya celebration gathering at IIUM.

ED Malaysia Chapter-DroBotics @ Putrajaya

By Zurita Zulkifli

The Chapter organized the DroBotics program on 21 and 22 February 2023 at Putrajaya Open Innovation Center (POINT), Kompleks Kejiranan Precinct 16. In total, 40 school children from the Putrajaya Precinct 16 community were provided with the basics of block programming through line-follower robots and drone operation. The 2-day program was designed for the school children to learn simple programming and simultaneously understand the robot and drone operation. The program was partially sponsored by CelcomDigi and Putrajaya Corporation, with the Chapter as the technical content provider and trainer. The participants responded positively at the end of the program after spending two days immersing themselves in the world of robotics and drones. It is hoped that the program has sparked their interest in STEM, especially in programming.

Participants tested their coding for drones using DroneBlock programming and competed with each other to overcome the drone obstacles.

ED Malaysia Chapter-STEM4FUN: Start Them Young

By Maizatul Zolkapli, Ahmad Sabirin Zoolfakar, Rozina Abdul Rani, and Azrif Manut

Fostering children's interest in science, technology, engineering, and mathematics (STEM) can be done easily and can even be cultivated from a young age. For example, one can start by taking them to science and technology exhibitions to expose them to these fields. Additionally, introducing them to STEM-based workshops, such as basic modeling and robotics, can be beneficial. On 19 May 2023, the Chapter in collaboration with the final-year students of the Bachelor's Degree in Electronic Engineering with Honors from Universiti Teknologi MARA (UiTM) conducted the STEM4FUN: Start Them Young program for preschool children from Sekolah Kebangsaan Seksyen 7 Shah Alam, Selangor. The program commenced at 8:00 a.m. and concluded at 12:00 p.m. It was led by Anis Suaida binti Mohd Annuary, who served as the leader of the program and was supported by Ir. Dr. Maizatul Zolkapli, the advisor for the program. The program involved a total of 100 preschool children who were divided into 4 groups. Each group was assisted by UiTM students in conducting the activities.

The first activity involved coloring and assembling paper and LED lanterns. The assistance provided by the final-year students must have been beneficial in guiding them through the assembly process. It is impressive to note that many students were able to assemble the lantern without help, and some even discovered new colors by mixing different ones. This shows how hands-on activities can spark curiosity and problem-solving skills in young minds.

In the second activity, using soft blocks, the students were given the freedom to assemble the blocks as they liked, encouraging them to be even more creative and innovative. Throughout the program, the students gained new knowledge and had the opportunity to sharpen their thinking and hands-on skills.

The participants during an activity in the STEM4FUN: Start Them Young program.

Overall, it's clear that the program which gained support from the Ministry of Education Malaysia was successful in providing the children with new knowledge and enhancing their thinking and hands-on skills. Such programs are essential in nurturing a generation of creative and innovative individuals, and they play a significant role in inspiring interest in STEM fields from an early age. It is hoped that the program can help in addressing the issue of declining interest in the Science stream among students. When children are engaged and interested in STEM from a young age, they are more likely to be better prepared for future academic pursuits and potential STEM-based careers. This, in turn, can lead to an increase in the number of students pursuing STEM-based careers in the future, and having a skilled workforce in these areas can significantly contribute to the country's progress and development.

~ Sharma Rao Balakrishnan, Editor

Regional News

USA, Canada (Regions 1-6)

Antique Wireless Association Museum Celebrates 75 Years of Bipolar Junction Transistor (BJT)

—by Steven Ziblut, Robert Hobday, and Santosh Kurinec

Santosh Kurinec, Professor of Electrical & Microelectronic Engineering, Rochester Institute of Technology, Fellow IEEE, coordinated with Antique Wireless Association (AWA) museum located at Bloomfield, NY to celebrate 75 years of Bipolar Junction Transistor (BJT). The IEEE banner is displayed over the first radio that was built using BJTs. Just after the invention of the BJT at Bell Laboratories, several radio receivers were constructed to demonstrate the feasibility of replacing vacuum tubes with solid-state transistors. The radio receiver in the picture under the banner is one of those first transistor radios.

Museums collect artifacts and knowledge of scientific, artistic, or historical significance. Museums share or provide access to the artifacts and knowledge by means of displays, publications, and education. To that end, the over 1,400 members of the Antique Wireless Association, Bloomfield, NY have been committed to preserving, understanding, and sharing in areas related to the technology used for wireless communication. As society is changing, the focus of museums, including the AWA museum, is evolving with a greater emphasis on education. The museum might soon be better known as the AWA Educational Institute.

The AWA has existed for over 70 years and the early telegraph systems might describe a starting point for the physical collections that extend all the way up to current electronics technology. Early telegraph equipment was as much a mechanical accomplishment as electrical or electronic. The vacuum tube or valve along with countless other technologies enabled wireless communication where we saw the explosive growth that included broadcasting of radio and television. The roots of our laptop computers and smartphones can be traced back to those same electronic technologies. It was about

Antique Wireless Association museum display of the world's first transistor radio.

K-12 students learning about LEDs, transistors, radio transmitters, and electromagnetic waves, building and testing circuits at the AWA museum.

75 years ago that the transistor was developed and enabled communication equipment with greater capability at a lower cost. Since then, the microelectronics industry has grown so that devices with billions of transistors are available in a single package.

The IEEE Region 1 Western Area and the Antique Wireless Association museum host IEEE member day each year. IEEE members and their families are invited to visit and tour the museum. The members and contributors to the AWA are from all over the world. Some are highly skilled practitioners in the area of electronics. Many are or have been IEEE members. Their passion and enthusiasm motivate them to collect, repair, and restore relevant artifacts and bodies of knowledge. They provide access to knowledge by means of publications, video presentations, and classes. Recently the AWA had over 80 young people attend Radio Fab-Lab hands-on courses. More than 50 adults attended its Learn-it, Build-it, and Fix-it programs where participants often build their own equipment. The AWA museum website (https://www.antiquewireless.org/homepage/museum/) provides details on events and educational initiatives.

Photos: Courtesy Elizabeth Lamark

Berger Earns 8-state Region IEEE Outstanding Engineering Educator Award

Ohio State Electrical & Computer Engineering Professor Paul Berger won the Outstanding Engineering Educator Award for his ongoing services to the eight-state IEEE Region 2.

IEEE, Institute for Electrical and Electronics Engineers, is the world's largest technical professional organization dedicated to advancing technology for the benefit of humanity. Its members inspire a global community through its highly cited publications, conferences, technology standards, and professional and educational activities.

Berger is being recognized for his service to IEEE Region 2, which extends from Eastern Indiana to Southern New Jersey, including Pennsylvania, West Virginia, Delaware, Maryland, the National Capital Region of D.C. and Northern Virginia.

Berger is a Professor in ECE and Physics at Ohio State and serves as a Distinguished Visiting Professor at Tampere University in Finland. He is actively working on quantum tunneling devices, printable semiconductor devices & circuits for IoT, bioelectronics, novel devices, novel semiconductors and applied physics. The professor was also elevated to IEEE Fellow in 2011 for his work on quantum tunneling devices.

The Columbus Section, with 934 members, boasts 30 IEEE Fellows, 24 Life Fellows, 102 graduate students and 38 student members.

Berger has also remained active in the IEEE Columbus Section, where he is serving his second term as elected vice chair. IEEE Columbus previously earned the 2022 Member and Geographic Activities Outstanding Section

Award worldwide for medium-sized sections through vital activities, including forming the new Women in Engineering Chapter, conducting several community service projects in Columbus. Berger also served in South America helping to construct solar-powered desalinization for indigenous people, and brought the 2021 IEEE International Flexible Electronics Conference (IFECTC) to Columbus in a virtual setting during COVID-19.

Elected IEEE Columbus Chair Helen Winfrey said there are 21 sections in Region 2 and their section swept the Five 2023 Region 2 Individuals Awards.

"This is an amazing accomplishment to get all five awards by one section," Winfrey said.

Columbus IEEE winners include:

- Helen Winfrey, Professional Leadership Award
- Paul Berger, Outstanding Engineering Educator Award
- Daniel Chionuma, Outstanding Service Award
- Dan Recker, Outstanding Engineer Award

Learn more about the Columbus IEEE Section.

~ Michael Adachi, Editor

Electron Devices Society (EDS) - Santa Clara Valley and San Francisco Joint Chapter (SCV/SF) Q2 2023 Events

—by Imran Bashir

The IEEE Electron Devices Society (EDS) San Francisco / Santa Clara Valley joint Chapter hosted on 19 May an EDS Distinguished Lecturer Webinar Event with Dr. Adam Skorek who is currently a Full Professor at University of Quebec at Trois-Rivières (UQTR, Canada) and the Director of the UQTR's Electro-Thermal Management Laboratory. The title of the lecture was 'Artificial Intelligence and Brain Biofields Quantum Computing.' Dr. Skorek started the discussion with brain inspired AI applications such as biofields that are defined as electromagnetics and thermal fields in living matter. The modeling of biofields with its environment is a computationally expensive task which can only be tackled through high performance computing (HPC) that is aided and assisted by a Quantum Computing infrastructure. Dr. Skorek presented a worldwide survey on the nature and complexity of the aforementioned problem and stressed on the need for greater collaboration between intellectuals and researchers in the field of high-performance quantum computing. The discussion was very lively and the scope of the discussion extended to quantum computing startups and education in Canada. Dr. Skorek also introduced nanoHUB as a valuable resource tool for researchers.

We were also excited to host on 28 July Dr. Eric Pop who is a Professor of Electrical and Materials Science Engineering at Stanford University. His lecture was titled 'What Are 2D Materials Good For?' Please visit our website @ https://site.ieee.org/scv-eds/ and join the email list to receive notification of current and future events and instructions on joining remotely through Zoom.

AP/MTT/ED-S Chapter of IEEE Finland Section– Distinguished Lecture by Prof. Albert Wang

—by Haneda Katsuyuki

Prof. Albert Wang gave a distinguished lecture on ESD protection designs for RFICs. The lecture took place on Monday, 5 June at the Aalto University, Finland. It was very well received by the audience thanks to the interesting and timely topic and the lecturer's approachable attitude. Our chapter would like to thank Prof. Wang for visiting us, and the EDS for giving us this valuable opportunity to listen to the DL's talk.

ESD failure is one of the most devastating IC reliability problems. Recent developments in IC technologies and designs make on-chip ESD protection design extremely challenging. These advancements include: sub-14 nm CMOS, FinFET, GAA, 3D heterogeneous integration, chiplet-based SoW, 5G wireless, U/WBG power electronics and biomedical electronics, This talk discussed different aspects of ESD

The distinguished lecture by Prof. Albert Wang at the Aalto University.

protection in the RF ICs. Starting with the ESD protection fundamentals, challenges and design methods for RF ESD protection designs were discussed in detail, using practical design examples. Future on-chip ESD protection perspectives were highlighted.

~ Larry Larson, Editor

Europe, Middle East & Africa (Region 8)

—by Mike Schwarz

A three-day event **"Sustainable Electronics and International Cooperation On Semiconductors"** supported by IEEE-IRDS-EDS and jointly organised by the SiNANO Institute and the newly launched "International Cooperation On Semiconductors" (ICOS) project, took place on 26-28 April 2023 in Grenoble, France. The goal of the Horizon Europe ICOS project coordinated by Francis Balestra Grenoble INP-UGA/CNRS, Chair of EDS France Chapter, and SiNANO Institute Director Emeritus is in line not only with the objectives of the EU ChipsAct, the EU Critical Raw Material Act, but also with the objectives set out by the European Green Deal and Digital Agenda strategies.

ICOS starts with an exhaustive analysis of the value chains of semiconductors for electronics and photonics, the strengths and gaps of European and international industries and research communities in this area, as well as emerging technologies. The findings regarding the most promising research subjects and international partners will be translated into proposals for future bilateral or multilateral research initiatives and practical cooperation modalities.

This workshop was organised to gather an overview of the strategies of different leading countries in the field of semiconductors, of European and International roadmaps, and conduct an initial analysis of the gaps between EU activities and the most promising technologies highlighted in Roadmaps for possible future international collaborations (collaborations to be strengthened or to be proposed on topics of mutual interests). It covered three main thematic, the European Innovation Council, Sustainable Electronics and Technology scanning and foresight.

The first session was devoted to the presentation of the European Innovation Council programme by Dr. Eric-Olivier Palu, Senior Policy Officer and Isabel Obieta, Programme Manager for Responsible Electronics from the EISMEA and other testimonials.

The second session was dedicated to the **Chips Acts**, with a first talk on the EU Chips Act by Marco Ceccarelli, Programme Officer, European Commission's Directorate-General for Communications Networks, Content and Technology, followed by the presentation of US Chips Acts and IRDS building pillars and bridges over valleys of death by Paolo Gargini, IRDS chairman & US Chips Act.

The third session devoted to **Sustainable Electronics** featured 9 speakers: Leo Kenny, the Chair of the *Environment, Safety, Health, and Sustaiability* (ESH/S) IRDS International Focus Team (IFT); Stéphane Monfray, ST; Mathilde Billaud, Fraunhofer IZM; Cedric Rolin, imec; Thomas Ernst, CEA - Leti; Thibault Pirson, UCLouvain; Patrick-Pype, NXP; Attila Geczy, BME-VIK; Dmitri Petrovykh, INL who covered the different domains from life cycle, environmental impact of ICs chip manufacturing and possible path to greener Electronics in order to find sustainable solutions and reduce environmental footprints of electronics as quickly as possible.

A panel session **Challenges and Solutions for Sustainable Electronics** concluded this first day of the workshop, with the participation of industrials, researchers

Panel session–Challenges and Solutions for Sustainable Electronics.

and policy makers, Leo Kenny, Chair of the ESH/S IRDS IFT; Isabel Obieta, EISMEA; Patrick Pype, NXP; Markus Pfeffer, Fraunhofer IISB; Mustafa Badaroglu, *More Moore* IRDS IFT leader; Dominique Thomas, ST Microelectronics; Thomas Ernst, CEA-Leti; Cédric Rolin, imec.

The third part on **Technology scanning and foresight** was divided in several sessions, starting with **Advanced Functionalities** covering the **Smart Sensors** Session where Matthias Illing Bosch presented the Innovation in MEMS for IoT and digital life, in particular for Automotive Applications but also for Consumer Electronics and other applications, as for example the Self-learning AI sensors. Then, Cosmin Roman, ETH Zürich gave a talk on Low power transducers for the IoT and Ultra low power sensors and emerging Self-powered sensors. Finally, together with Alan O'Riordan, Tyndall National Institute we discussed Sensors for Sustainable Agrifood and the Environment, in line with the EU Green Deal. The next Session devoted to **Smart Energy**, started with a presentation by Markus Pfeffer, Fraunhofer IISB on Si CVDMOS Technology evolution as an example for sustainable and efficient energy conversion, and Mikael Östling, KTH Royal Institute of Technology told us more about the Wide Bandgap Power Devices for a Sustainable Future with a specific focus on SiC and GaN technologies.

On the next **Beyond CMOS** session, Konrad Seidel, Fraunhofer IPMS presented Ferroelectric memories–Enabler for novel computing architectures, explaining the role of these emerging memories. To cover even more the topic, Jouni Ahopelto, VTT spoke about On and Beyond CMOS integration, which requires material and process compatibility and suitable back-end processing for these innovative concepts at a very low TRL. Qing-Tai Zhao, Forschungszentrum Jülich then talked about Nanowire operation from RT to Cryogenic temperatures and about the interest in Electronics working in the very Low Temperature range. Andreas Hemmeter, AMO GmbH, presented the interest in Flexible Electronics with 2D Materials. An Chen, leader of the *Beyond CMOS* IRDS IFT, gave us an overview of the Beyond CMOS roadmap which surveys, assesses, and catalogs viable emerging devices and novel architectures for their long-range potential and technological maturity, and identifies the challenges to be overcome for their acceptance by the semiconductor industry.

Panel session–Strategy for International Cooperation Chips-Act

During the **Quantum Information processing session,** D. Scott Holmes, chair of the *Cryogenic Electronics and Quantum Information Processing* IRDS IFT, gave an overview of the 2023 report and highlighted emerging memory and logic devices, their applications in novel computing paradigms, and the co-optimization of beyond-CMOS devices and architectures. Maud Vinet, Siquance explained the path to large scale quantum computing using semiconductor technologies. The ecosystem and methods are now in place to turn the scientific first into reliable quantum processor units. This session ended with The European Quantum Strategic Industry Roadmap by QUIC presentation by Johanna Sepúlveda, Airbus.

A panel session on **Strategy for International Cooperation–Chips Act** was then chaired by Patrick Cogez, AENEAS, with Paolo Gargini, IRDS Chair & US Chips Act; Enrico Sangiorgi, Director Emeritus SiNANO Institute & *More than Moore* IRDS IFT leader; Matthias Illing, Bosch; Markus Pfeffer, Fraunhofer IISB; Abdul Rahim, EpiXFab; Giorgos Fagas, Tyndall; Holger Schmidt, Infineon; and Carlo Reita, CEA-Leti.

The 3rd day started with Mr. Hisashi Kanazashi, Director of IT Industry Division, Commerce and Information Policy Bureau, Ministry of Economy, Trade and Industry, who presented the Japanese government strategy in the field of semiconductors, and Colette Maloney, Head of unit, European Commission's Directorate-General for Communications Networks, Content and Technology, who presented the Japan-European digital partnership, the EU Chips Act, and the EU efforts to develop the semiconductor value chain and academic partnerships to improve research at an international level and face the talents shortage. Mr. Makoto Ikeda, Professor at the University of Tokyo then introduced us to the AI Chip Design Center (AIDC), SoC design platform for small industries and startups in Japan, whereas Carlo Reita, Director of Strategic Partnerships and Planning, CEA-Leti presented the #PREVAIL project which, through European partnerships, aims at providing an open access pilot line for fast Edge AI chip prototyping. Mr. Takashi Yasumasu, vice president at Renesas Electronics focused on the automotive industry covering Megatrends such as CASE, software and semiconductor market growth. Matthias Illing, Bosch presented the global trends for software-define vehicle, electrification and autonomous driving. Some of the most important ongoing cooperations between Japanese and European institutions were highlighted by Francis Balestra, ICOS Coordinator.

The 8th session on **AdvancedComputing** started with the talk by Mustafa Badaroglu, leader of the *More Moore* IRDS IFT, who presented cloud and edge computing with intelligent connectivity as drivers for More Moore. The mission of this IRDS chapter is to explore scaling trends in terms of Performance, Power, Area, Cost, Temperature,

Schedule (PPACTS) for logic and memory application technologies. Then Roberto Gonella, R&D Executive Director at STMicroelectronics delivered a talk on the sustainable FDSOI platform for Smart Mobility, Power & Energy, IoT and Connectivity. Anabela Veloso, imec talked on Nanosheet-based Device Architectures for Enabling Advanced CMOS Logic Scaling, and in particular on advantages of the Nanosheet FET Devices over Nanowires. This session ended with Sébastien Loubriat, SOITEC who focused on FDSOI engineered substrates for advanced computing with state-of-the-art SOI wafers, enabled by the SmartCut process, and on FDSOI key applications as ultra low voltage and mmWave RF-CMOS.

The very last session, on **Semiconductor-based photonics**, had three enthralling presentations. Abdul Rahim, ePIXfab-the European Silicon Photonics Alliance, gave a very instructive introduction on Silicon Photonics: Current state, trends, and future evolution. Then Stephan Suckow, AMO GmbH talked about Neuromorphic Computing-At the intersection between Electronics and Photonics. The last talk of the workshop, on Silicon photonics and applications was given by Frédéric Boeuf, STMicroelectronics. He discussed the similarity between density, performance, and cost trends followed by electronics and photonics and presented the development of their silicon photonics technology platform and the future evolution towards non-telecom applications.

Please, consult the presentations on the ICOS website: https://icos-semiconductors.eu/workshop-sustainable-electronics-international-cooperation-on-semiconductors/

—by Mike Schwarz

In mid-May 2023, the next group of colleagues and researchers gathered for one of the most interesting events of the Spanish Spring landscape: the **Community Workshop on "Advanced Materials and Nanostructures for Disruptive Devices & Applications"** organized by ASCENT+ and the SiNANO Institute, and sponsored by IEEE-IRDS-EDS as a satellite event of the EUROSOI-ULIS 2023 conference.

The aim of this event was to discuss emerging research challenges in nanoelectronics. The one-day workshop included three sessions: Advanced Materials and Device Integration, Disruptive Devices, and Future Computing followed by a Networking Cocktail to allow discussions and exchange after this full intense day.

The workshop started with a session dedicated to **Advanced Materials and Devices Integration**, discussing first

Mikael Östling explaining parts of the IRDS roadmap.

GaN IC development for power electronics application (Urmimala Chatterjee, imec), then **Chip Scale Package Solution for GaN Bridge Devices** (Michael Schiffer, Fraunhofer IZM), next **Power Devices in Wide Bandgap materials and the recommendations by IRDS More than Moore roadmaps** (a captivating talk by Mikael Östling, KTH Royal Institute of Technology), and finally **Thermal, acoustic and optical properties of Si-based nanostructures** (Emigdio Chavez Angel, ICN2-Catalan Institute of Nanoscience and Nanotechnology). The session ended with a series of precise questions from the audience.

The second session on **Disruptive Devices** featured a talk on **Pulsed laser annealing of Transition Metal dichalcogenides** (Enrico Di Russo, University of Padova), then some insights on the **Electrical characterization of 2D-channel MOSFETs** (Christoforos Theodorou, CNRS). It was also the opportunity to discuss **Quantum wave-based modeling of nanoscale transistors for circuit simulation** (Alexander Kloes, Technische Hochschule Mittelhessen) and **More than Moore applications of 2D materials** (Francisco Gamiz, University of Granada).

The workshop concluded with the session dedicated to **Future Computing**, during which two talks focused on quantum dots: **Integration of site-controlled quantum dots"** (Emanuele Pelucchi, Tyndall) and **Scaling up quantum computers with silicon quantum dots through rapid characterization** (Mark Johnson, Quantum Motion Technologies). Afterwards, Sergio Nicoletti from CEA-Leti presented the project **PREVAIL: the Test and Experimentation Facility for the realization and validation of prototype chips dedicated to Edge AI**. The last talk of the workshop covered **Topological Insulator Josephson Junctions integrated in superconducting Qubit circuits** (Anna Schmidt, Forschungszentrum Jülich).

After the event, the participants had the possibility to exchange further opinions on these topics and discuss new collaborations.

All the presentations are available on the SiNANO website: https://www.sinano.eu/advanced-materials-and-nanostructures-for-disruptive-devices-and-applications-may-9th-2023/

Double Event-Two IEEE Distinguished Lectures at TU Dresden

—by André Heinzig

The EDS Germany Chapter hosted on 22 June 2023 a double event with two high-level lectures at Dresden University of Technology (TU Dresden - TUD).

Prof. Francesca Iacopi, IEEE DL, from the University of Technology Sydney, and Prof. Paul Berger, IEEE DL, from Ohio State University, presented their research with the lectures "Graphene on cubic silicon carbide: integrated functionalities on silicon" and "Si-based Resonant Interband Tunnel Diodes for Quantum Functional and Multilevel Circuitry (Mixed-Signal, Logic, and Low Power Embedded Memory) to Extend CMOS". The audience was very interested in the presented topics.

From the beginning, it became clear that the EDS vision, 'Providing excellence in the field of electron devices for the benefit of humanity' connects the researchers with the same motivation for their application-oriented research on novel electronic devices.

Starting the event with a tour at the Institute for Semiconductor and Microsystems Technology, Dr. André Heinzig and Prof. Thomas Mikolajick presented the research on reconfigurable devices and 2D devices at the TUD Chair for Nanoelectronics. The research on organic electronic devices was presented in a tour by Dr. Hans Kleemann and Prof. Karl Leo at the Institute of Applied Physics (IAP). The event organization was supported by Sandra Bley from the Center for Advancing Electronics Dresden (cfaed).

Professor Iacopi introduced her distinguished lecture with a look at the fascinating properties of graphene. She pointed out that the considerations must be carried out in different ways depending on the application in electronics, chemistry, or physics and that in almost all cases, graphene is combined with other materials, which significantly influence its properties. As one of the essential steps for the industrial implementation of graphene, providing uniform wafer-scale growth methods is challenging. Francesca Iacopi's achievements in epitaxial graphene growth on SiC demonstrated an impressive result of uniform wafer-scale processing. She continued the topic by presenting charge transfer doping and the characterization of fabricated devices. The formation of buffer layers depending on the crystallization of the SiC led to different electrical properties. Impressive achievements in providing patterning techniques with solid sources and catalytic alloys demonstrated additional device design flexibility. The lecture was finalized with a video on applying brain-computer interfaces, e.g., to control robots using the biocompatibility and robustness of epitaxially fabricated Si/SiC/graphene sensors.

Professor Berger began his presentation by introducing Ohio State University and the outstanding individuals and historical developments in electronic devices at this place. After presentation of the theoretical background on interband tunnel diodes, he demonstrated ways to reduce circuit complexity, e.g., for oscillators and multivalued logic, using negative differential resistance (NDR) devices instead of conventional transistors. His group's developments in the field showed impressive results with record peak-to-valley ratios using both epitaxially grown and CVD-grown devices. In particular, the developed delta doping techniques in Si/SiGe structures allow for high band bending, enabling efficient band-to-band tunneling of charge carriers resulting in high tunnel currents.

In the subsequent discussion sessions, the interest of the audience in the device topics as well as the expanding potential for the IEEE community became apparent. The guests' and host groups' complementary research fields allow us to expect an intensive exchange of expertise and close cooperation in the development of future electronic devices.

After the lectures, Prof. Berger and Prof. Iacopi were hosted by Dr. Kleemann and Prof. Leo at Dresden Integrated Center for Applied Physics and Photonic Materials (IAPP), where they saw recent developments on flexible organic solar cells, printed human-machine interfaces, and polymer-based neuromorphic circuits. Unfortunately, Prof. Iacopi had to head back to the airport in the late afternoon. However, Prof. Berger and Dr. Kleemann used the occasion to continue the discussion and shared anecdotes with a glass of beer in front of the famous Frauenkirche in the scenic heart of Dresden.

Fundamentals of Security Practical Case: Secure Boot of processors by Mr. Rodrigue Simonneau, NXP

—by Mike Schwarz

On 3 July 2023, Prof. Mike Schwarz from the EDS Germany Chapter and Prof. Ulrich Birkel organized a lecture entitled "**Fundamentals of Security Practical Case: Secure Boot of processors**". 33 participants attended the lecture which was given by Rodrigue Simonneau, FAE i.MX Processors at NXP Semiconductor.

In introduction, Mr. Simonneau explained the **pillars of security**. Afterwards, he went through "**Building blocks for HW backed security**" and offered boundaries with focus on how to compare all hardware enabling depth security components. This led him to the topic of "**Security Architecture across i.MX Processors Family**". Here he gave insight in the i.MX series 6, 7, and 8, the device architecture, and how security is enabled at different levels. Afterwards, he moved forward to the latest i.MX 93 architecture including RISC-V topology and referred to the security aspects.

Mr. Rodrigue Simonneau explaining the pillars of security.

The secure boot example enabled the students to acquire some processor security fundamentals, illustrated at the end by a live demo. The i.MX93 could first boot a simple signed image, which was in a second step manipulated at the binary level by Mr. Simonneau. The device protected here by means of ECC signing was able to detect that the image has been tampered and thus declined to boot.

Afterwards, the students had the opportunity to ask detailed questions and there were many of them, caused by the great demo. The lecture ended after approximately 90 minutes with some conclusions and thanks to Mr. Simonneau for the chance to have an experienced engineer of NXP at THM.

Prof. Ram Achar Distinguished Lecture in Lisbon, Portugal

—by António L. Topa

The Portuguese MTT/AP/EDS Joint Chapter invited Prof. Ram Achar, Distinguished Lecturer for IEEE Electron Devices Society (EDS), to emphasize on "Signal Integrity and the Emerging Challenges of High-Speed Nanoscale Interconnects." With the increasing demands for higher signal speeds coupled with the need for decreasing feature sizes, signal integrity effects such as delay, distortion, reflections, crosstalk, ground bounce and electromagnetic interference have become the dominant factors limiting the performance of high-speed systems.

This distinguished lecture was delivered on 12 May 2023, at Instituto Superior Técnico, University of Lisbon, Portugal.

The host was Prof. António Topa who introduced Prof. Ram Achar and made a short revision on IEEE mission, vision and organizational ethics. Prof. Ram Achar on his side, introduced Carleton University, Ottawa, Ontario and gave a very interesting talk for any member of three societies of the joint chapter, raising a number of questions and observations from the audience.

~ Mike Schwarz, Editor

30th International Conference "Mixed Design of Integrated Circuits and Systems" - MIXDES 2023

—by Mariusz Orlikowski

On 29–30 June 2023, the 30th Jubilee International Conference MIXDES took place. This year the MIXDES Conference participants had an opportunity to meet in the beautiful city of Kraków, Poland. The event was organized by the Lodz University of Technology together with the AGH University of Science and Technology and Warsaw University of Technology. The conference was co-sponsored by the Poland Section IEEE ED & CAS Societies, the Polish Academy of Sciences (Section of Microelectronics and Electron Technology), and the Commission of Electronics and Photonics of Polish National Committee of International Union of Radio Science-URSI.

The conference program included 65 presentations by speakers coming from 21 countries. The following general

Participants of the IEEE DL given by Prof. Achar (holding the IEEE logo).

MIXDES 2023 participants in front of the conference site.

invited talks were given during the conference plenary sessions:

- *1 Selector - 1 Resistor (1S1R) Crossbar Arrays for Neural Networks Hardware Implementation* - Joel Minguet Lopez (CEA, LETI, MINATEC Campus, Grenoble, France),
- *Design, Analysis, Fabrication and Dynamic Testing of Insect-inspired Nano Air Vehicles* - Sébastien Grondel (Univ. Polytechnique Hauts-de-France, CNRS, Univ. Lille, France),
- *From Embedded to Cyber-physical Systems, AI and Beyond* - Nikolaos Voros (University of Peloponnese, Greece),
- *Noise-Based Simulation Approach for Statistical Analysis of Parameter Fluctuations in Circuits* - Alexander Kloes (THM University of Applied Sciences, Germany).

The conference program also included presentations in the frame of three special sessions:

- *Compact Modeling of Micro- and Nanoelectronic Devices and Systems with Support for Free Open Source PDK Initiative* organized by Dr. Daniel Tomaszewski, Łukasiewicz - IMiF, Poland, and Dr. Władysław Grabiński, Switzerland,
- *GaN-based Devices* organized by Dr. Anna Szerling, Łukasiewicz - IMiF, Poland,
- *Offshore Wind Farm Energy & Power Cables* organized by Prof. Edward Gulski, Switzerland, and Prof. George Anders, Canada.

The Conference organizers hope to meet next year in Gdansk (27-29 June 2024), Poland's principal seaport and the cradle of the "Solidarity" movement. The MIXDES 2024 Call for Papers is available at http://www.mixdes.org/downloads/call2024.pdf. More information about the past and next MIXDES Conferences can be found at http://www.mixdes.org.

~ Marcin Janicki, Editor

Asia & Pacific (Region 10)

ED Malaysia Chapter-Distinguished Lecture Talk with Prof. Simon Deleonibus

—by Hazian Mamat and Nurul Ezaila Alias

The Chapter organized on 8th June 2023 a Distinguished Lecturer Talk with the prominent speaker Prof. Simon Deleonibus. The event, held at MIMOS Berhad, successfully gathered more than 40 attendees, including students, academicians, and industry professionals. Prof. Deleonibus presented on one of the most anticipated topics: "New Routes and Paradigm for Device Engineering in the Nanoelectronics and Nanosystems Era."

Prof Simon Deleonibus' DL at MIMOS Auditorium; Prof. Simon with MIMOS CEO and IEEE Malaysia Section Chair, and IEEE Malaysia ED Chapter Chair.

Following the Distinguished Lecture presentation, an industry forum was held to discuss semiconductor technology and its future direction. The panelists were Prof. Simon, Prof. Azrul Azlan Hamzah from Universiti Kebangsaan Malaysia (UKM), Ir. Dr. Nordin Ramli (IEEE Malaysia Section), and Dr. Lee Hing Wah (Head of Dept. MIMOS Semiconductor).

The event received support from MIMOS CEO Dr. Iskandar, who engaged in a fruitful discussion with Prof. Simon regarding semiconductor industry technology and the way forward for MIMOS Semiconductor Technology Centre (STC).

This event was organized by the ED Malaysia Chapter and co-organized by MIMOS Berhad. During the event, the Chapter chair also delivered a brief presentation to introduce IEEE to the audience. Additionally, the event included a tour of the MIMOS Semiconductor Technology Centre, showcasing the Semiconductor Fabrication Lab, R&D Fabrication Lab, and Failure Analysis Lab.

ED Malaysia Chapter-Professional Talk on The Art of Transmission Electrons Microscopy (TEM) by Dr. Anis Suhaili Bakri

—by Zurita Zulkifli

The Chapter organized on 18 July 2023 a Professional Talk by an expert through the Webex platform. The speaker, Dr. Anis Suhaili Bakri is a Senior Failure Analysis Engineer at MIMOS Berhad. Based on her experiences and skills in the operation of laboratory equipment, the sharing session managed to gather more than 40 attendees from students, academicians and industry practitioners. Dr. Anis shared the concept and properties of Transmission Electrons Microscopy (TEM) with examples of results from various types of samples. TEM is the most expensive method of characterization

Poster of talk and sharing by Dr. Anis Suhaili Bakri.

in the nanotechnology which can identify the growth of layers, material composition and defects in the semiconductor materials. Almost half of the audience were students from universities in Malaysia. The participants were actively engaged with the speaker to know more about TEM capabilities.

~ Sharma Rao Balakrishnan, Editor

EDS Kansai Chapter

—by Tokiyoshi Matsuda

Round Table Meeting

The EDS Kansai Chapter (EDSK) round table meeting was held on 7 April 2023. At the meeting, the participants had extensive discussions on technical, industrial, educational, and business interests and concerns. The two guest speakers, Dr. Hayashi, who presented the IEEE senior grade application and its social impact, and Dr. Umezawa, who recently joined EDSK, presented the recent research about diamond devices and the current issues of the research. The meeting was attended by 25 participants who actively joined the discussions.

Committee Meeting

The committee meeting of EDSK with 21 committee members took place on 26 April 2023. The members focused on the management of the upcoming technical meeting, colloquium, and the annual International Meeting for Future of Electron Devices, Kansai (IMFEDK 2023).

Technical Meeting

A technical meeting was held on 5 June 2023. We hosted two speakers: Dr. Takeshi Fukuda from Sekisui Chemical Co. Ltd., who spoke about "Creating business solutions for social issues", in which he discussed the development of products to solve social issues such as SDGs in the company. The other one was by Dr. Hidenori Kawanishi from the former Sharp Co. Ltd., who presented on "R&D within a company", in which he discussed the GaN LED products from his R&D experience. All 44 attendees enjoyed the insightful presentations.

On-coming events

First, the reports of the VLSI Technology meeting 2023 will be co-organized by the EDS Kansai Chapter (EDSK) on 5 July. Second, the 2023 International Meeting for Future of Electron Devices, Kansai (IMFEDK 2023) will be held on 16-17 November 2023. For detailed information, please refer to the conference website (https://www.ieee-jp.org/section/kansai/chapter/eds/imfedk/).

EDS Taipei Chapter

—by Steve Chung

The EDS Taipei Chapter invited Prof. Pramod Kumar Tiwari from the Indian Institute of Technology Patna, to give a talk on 25 April 2023. The Lecture title was "Unified modeling of Multi-gate MOSFETs". As the transistor technology moved from planar FET to 3D FinFET, nanosheet

EDS Taipei, Invited Talk, 25 April 2023.
First row from left: Y. C. Wu (2nd), P. K. Tiwari (3rd, speaker), K. S. Chang-Liao (4th, seminar chair).

etc., the gate-all-around (GAA) structure becomes a popular way to further boost the IC performance. As a consequence, the modeling of gate-all-around transistors becomes important to the further development of these technologies. In this talk, he presented a unified model of GAA device well-suited for the circuit simulation. First, a unified model of core drain current and gate capacitance for GAA MOSFETs was formulated, which is applicable to different shapes of GAA devices, including square, circular, trapezoidal, round-cornered trapezoidal, rectangular, elliptical, triangular, and round-cornered triangular cross-sections. The model is based on a unified charge control model for long-channel undoped circular gate MOSFET, using effective radius, effective width, and a unified model for gate capacitance. Moreover, the model has infinite continuity in weak, moderate, and strong inversion regimes, making it suitable for circuit simulations. This talk was attended by more than 35 graduate students and professors.

~Tuo-Hung Hou, Editor

ED Delhi Section Chapter

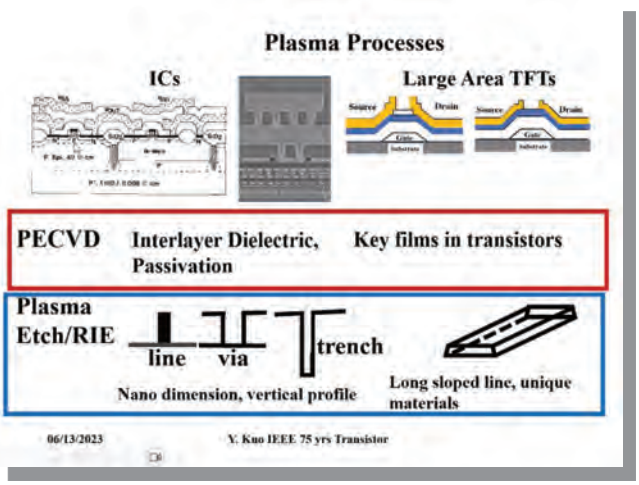
—by Harsupreet Kaur and Manoj Saxena

In April 2023, the EDS Delhi Chapter organized Virtual Mini Colloquia (MQ) on "Reliability issues in CMOS Devices" as part of the commemoration of "75th Anniversary of Transistor Invention". On 3 April 2023, the Distinguished Lecture (DL) "Transistor technologies beyond Si CMOS" was delivered by Professor Mikael Östling, Fellow IEEE, KTH Royal Institute of Technology. He addressed several new power device solutions based on silicon carbide (SiC) and gallium nitride (GaN) semiconductors. The next DL "Reliability of Metal Gate / High-K CMOS devices" was delivered by Andreas Kerber, IEEE Senior Member and Distinguished Lecturer. He discussed how to obtain stochastic BTI data for discrete SRAM and logic devices. On 8 April 2023, the DL "Anomalous mechanical impact on reliability of physically conformal CMOS electronics" was delivered by Professor Muhammad Hussain, Fellow IEEE, Purdue University's Elmore Family School of Electrical and Computer Engineering. He enlightened the delegates about physically conformal (flexible, stretchable, reconfigurable) electronics that will open up new application areas for healthcare technology and human-machine interfacing. 135 delegates from Australia, Brazil, Greece, Hong Kong SAR, India, Indonesia, Ireland, Israel, Italy, Japan, Kazakhstan, Nepal, Nigeria, Russia, Saudi Arabia, Serbia, Sudan, Switzerland, Taiwan and United States attended the MQ.

EDS SSCS 75 Years of the Transistor - Commemorative Lecture was organized on 23 May 2023 on the topic "Transistor diversity: looking beyond CMOS to improve analog performance" which was delivered by Viola Schäffer, Texas Instruments–Precision Amplifiers. 69 delegates from India, Taiwan, United States, Nigeria, Switzerland attended the talk.

The EDS Delhi Chapter initiated "Webinar Series by Leading IEEE Electron Device Luminaries" as a part of the Celebration of 75 Years of Invention of Transistor which was jointly organized with Deen Dayal Upadhyaya College (University of Delhi), DBT Star College Status Program, and The National Academy of Sciences India–Delhi Chapter. 220+ delegates from Bangladesh, Canada, Germany, Greece, India, Indonesia, Ireland, Israel, Italy, Japan, Kazakhstan, Republic of Korea, Malaysia, Nepal, Nigeria, Russia, Saudi Arabia, Serbia, Switzerland, Taiwan, United States and Venezuela attended the series.

On 19 April 2023, the technical talk "Bandgap Engineering and Device Applications of Dilute Nitrides" was delivered by Charles W. Tu, Department of Electrical Engineering, National Chung Hsing University, Taichung, Taiwan. He apprised that with the introduction of iPhone X in 2017, which incorporates several vertical-cavity surface-emitting lasers (VCSELs) for face recognition, long-wavelength (1550 nm) VCSELs have aroused a new interest in dilute nitride GaInNAsSb sandwiched between top and bottom GaAs/AlAs Distributed Bragg Reflectors (DBRs) for eye-safety and cost reasons. On 27 April 2023, a technical lecture "The Future of Transistor Integration" was delivered by Prof. H.-S. Philip Wong, Department of Electrical Engineering and Stanford SystemX Alliance, Stanford University. On 8 May 2023, Sung-Mo "Steve" Kang, Distinguished Professor Emeritus and Distinguished Research Professor, University of California, Santa Cruz delivered a technical talk "Evolution of Semiconductor Technology". He addressed emerging technologies, including memristor technology along with their applications for ultra-dense intelligent VLSI systems, future neuromorphic computing, generative AI, and scientific hardware acceleration.



A slide from the talk of Prof. Philip Wong.

Participants of the program for STEM Awareness of School Teachers of Uttarakhand, 20-23 June 2023.

On 13 June 2023, a technical lecture on "Plasma-Based Thin Film Technology in Fabrication of Nano- to Giga-Sized Electronics" was delivered by Yue Kuo, Joe M. Nesbitt Professor, Texas A&M University College of Engineering. Prof. Kuo presented examples of manipulating the bulk film and interface properties to obtain the optimized device characteristics using the PECVD process. On 19 June 2023, Stephen Pearton, Professor Emeritus, Department of Materials Science and Engineering, University of Florida delivered a technical talk "The Rise of Compound Semiconductors". On 21 June 2023, a technical lecture "Transistor technologies for RF power amplifiers" was delivered by Peter Asbeck, Professor Emeritus, Center for Wireless Communications, University of California San Diego. This talk reviewed strengths and shortcomings of the technologies, recent directions of progress, and problems remaining to be solved.

On 20-23 June 2023, an Institutional Teacher Training Program for STEM Awareness of School Teachers of Uttarakhand was held at Deen Dayal Upadhyaya College (DDUC). It was jointly organized by DDUC; Uttarakhand Science Education & Research Centre (USERC), Department of Information & Science Technology, Govt. of Uttarakhand; Scientific Social Responsibility Cell & Science Foundation (Under the aegis of DBT Star College Program, DDUC); IEEE EDS Delhi Chapter; and The National Academy of Sciences, India (NASI), Delhi Chapter. Representations of 35 Government Schools from 12 Districts of Uttarakhand (Almora, Almora, Bageshwar, Chamoli, Champawat, Dehradun, Pauri Garhwal, Pithoragarh, Rudraprayag, Tehri Garhwal, Udham Singh Nagar and Uttarkashi) participated in the training program.

IIITDM-Kancheepuram, ED Student Branch Chapter

—by Kumar Prasannajit Pradhan

The chapter in association with the Department of Electronics and Communication Engineering, Indian Institute of Information Technology Design and Manufacturing (IIITDM) Kancheepuram organized a Technical Talk on "ReRAM for In-Memory Computing: Prospects and Challenges" by Mr. Shubham Pande, IIT Madras. The lecture was held in a virtual mode on 17 April 2023. In addition, the chapter successfully organized on 21 April 2023 a Distinguished Lecture on "Challenges of Reliability in Advanced Electronics" by Prof. Cher-Ming Tan, Chang-Gung University. The DL was held in-person at IIITDM Kancheepuram.

Photo session with Prof. Cher-Ming Tan on 21 April 2023 in the presence of Prof. K. P. Pradhan, Faculty Advisor of the chapter and chapter chair Mr. Rameez Raja Shaik.

Speech delivered by Dr. Anindita Ganguly, DTE, Govt. of WB during inauguration of DevIC 2023.

IEEE EDS Kalyani Government Engineering College Student Branch Chapter

—by Angsuman Sarkar

The 5th International Conference on "Devices for Integrated Circuits (DevIC 2023)" was held in-person on 7-8 April 2023. The conference was organized by the EDS Kalyani Government Engineering College (KGEC) Student Branch Chapter in association with the Department of Electrical and Computer Engineering, KGEC, and with technical partnership from IETE Kolkata Chapter and IEEE EDS Kolkata Chapter.

This year the conference saw a dramatic increase in participation and involvement of students, professionals and researchers. More than five hundred papers were submitted to this conference. The papers came from different countries around the globe, from academia, industry and professionals. A total of 116 regular contributions were presented. The high-level technical sessions were highlighted by plenary talks and invited talks by international research pioneers and leaders of device technology. The conference has been successfully completed with twenty Technical Tracks, Four Plenary and six Keynote Talk sessions with focused areas on: Device Physics and Characterization, Device Technology and Characterization, Circuit and Device Integration, Emerging Device and Circuits, Nanostructure-based devices/systems & Biosensor Design, and Nanostructures & Quantum Devices. The conference proceedings (550 pages) were published through the IEEE Conference Publication Program and are available on IEEE Xplore.

ED Kanpur Chapter-Uttar Pradesh Section

—by Shubham Sahay and Avinash Lahgere

The chapter organized three distinguished lectures. The first one, on "Protonic Non-Volatile Programmable Resistors for Analog Deep Learning", was delivered by Prof. Jesús A. del Alamo, Donner Professor and Professor of Electrical Engineering at Massachusetts Institute of Technology. The second one was delivered by Dr. Andreas Kerber, Intel, Senior Member IEEE, on the topic "Reliability of Metal Gate/High-K CMOS devices". The third one was delivered by Dr. Charvaka Duvvury, Fellow Texas Instruments, Fellow IEEE, on "Advanced Electrostatic Discharge Technology Issues".

~Soumya Pandit, Editor

EDS MEETINGS CALENDAR

THE COMPLETE EDS CALENDAR CAN BE FOUND AT OUR WEB SITE: HTTP://EDS.IEEE.ORG. PLEASE VISIT.

2023 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)	14 Oct – 18 Oct 2023	Monterey, CA
2023 IEEE 33rd International Conference on Microelectronics (MIEL)	16 Oct – 18 Oct 2023	Nis, Serbia
2023 20th International Conference on Electrical Engineering, Computing Science and Automatic Control (CCE)	25 Oct - 27 Oct 2023	Ciudad de México, Mexico
2023 Symposium on Internet of Things (SIoT)	25 Oct - 27 Oct 2023	São Paulo, Brazil
2023 IEEE/ACM International Conference on Computer Aided Design (ICCAD)	28 Oct – 02 Nov 2023	San Francisco, CA
2023 Middle East and North Africa Solar Conference (MENA-SC)	15 Nov – 18 Nov 2023	Dubai, United Arab Emirates
2023 IEEE 10th Workshop on Wide Bandgap Power Devices & Applications (WiPDA)	04 Dec – 06 Dec 2023	Charlotte, NC
2023 International Electron Devices Meeting (IEDM)	09 Dec – 13 Dec 2023	San Francisco, CA
2023 IEEE 54th Semiconductor Interface Specialists Conference (SISC)	13 Dec – 16 Dec 2023	San Diego, CA
2024 8th IEEE Electron Devices Technology & Manufacturing Conference (EDTM)	03 Mar - 06 Mar 2024	Bangalore, India
2024 25th International Symposium on Quality Electronic Design (ISQED)	03 Apr – 05 Apr 2024	San Francisco, CA

2024 IEEE International Reliability Physics Symposium (IRPS)	14 Apr – 18 Apr 2024	Grapevine, TX
2024 IEEE 36th International Conference on Microelectronic Test Structures (ICMTS)	15 Apr – 18 Apr 2024	Edinburgh, United Kingdom
2024 Joint International Vacuum Electronics Conference and International Vacuum Electron Sources Conference (IVEC + IVESC)	23 Apr – 25 Apr 2024	Monterey, CA
2024 IEEE Latin American Electron Devices Conference (LAEDC)	02 May – 04 May 2024	Guatemala City, Guatemala
2024 IEEE International Memory Workshop (IMW)	12 May - 15 May 2024	Seoul, Korea (South)
2024 36th International Symposium on Power Semiconductor Devices and ICs (ISPSD)	02 Jun – 06 Jun 2024	Bremen, Germany
2024 IEEE 52nd Photovoltaic Specialist Conference (PVSC)	09 Jun – 14 Jun 2024	Seattle, WA
2024 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)	16 Jun – 23 Jun 2024	Honolulu, HI
2024 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)	16 Jun – 18 Jun 2024	Washington, DC
2024 25th International Microwave and Radar Conference (MIKON)	01 Jul – 04 Jul 2024	Wroclaw, Poland

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"Device innovation has never been more dependent on novel materials. This Journal brings academics and industrial scientists together to truly validate if, how and which novel materials could become a solution for current and future challenges in electron devices."

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Scope

The IEEE Transactions on Materials for Electron Devices (T-MAT) publishes contributed and invited articles of different formats in the field of materials for electron devices and their interconnects.
The focus of T-Mat is on the applied aspects of electronic materials, as well as fundamentals directly relevant to individual and integrated device engineering and fabrication.

Topics

Materials will include advanced thin-films and their interfaces, as well as nanomaterials (nanowires, nanotubes, 2D materials and their combination). Manufacturing platforms will include wafer-level, roll-to-roll as well as direct-write and additive technologies. Processing techniques will also be incorporated that can hone materials' properties to an optimal performance for designated applications. Aspects of interest also include advances in scalability, large-scale structuring and patterning, robustness and control of interfaces, integrated performance and reliability, and related novel metrics, while keeping an eye out for long-term sustainability of large-scale deployment in semiconductor manufacturing.

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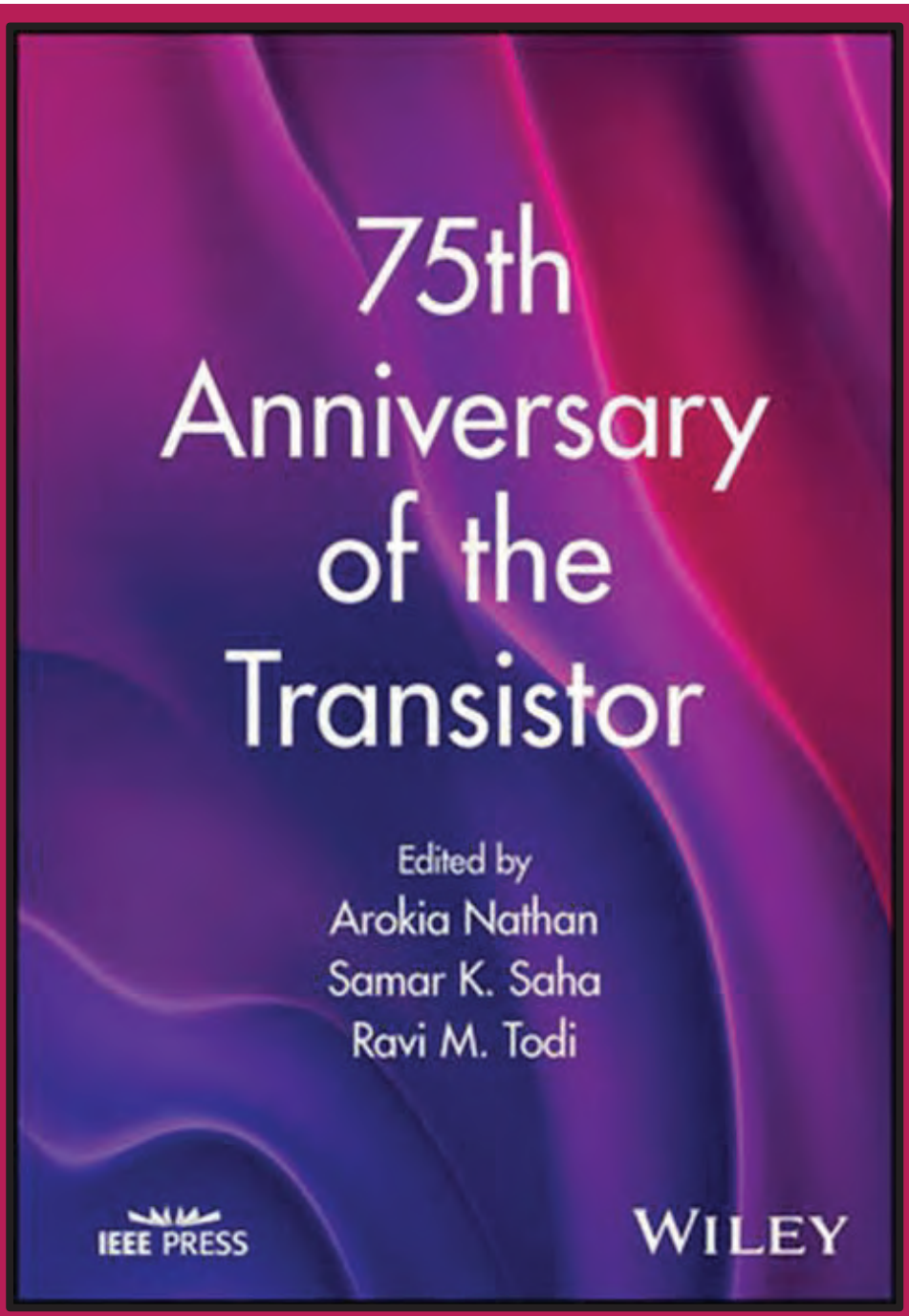


The **75th Anniversary of the Transistor** commemorative book will be released at the IFETC 2023 in San Jose, CA on August 14, 2023. A limited number of books will be available to purchase onsite. All editors will be available for Book signing on August 14, 2023.

For more information, please visit: Wiley

Evolution

Life Member Conference

April 14-16, 2024

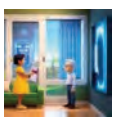
Hyatt Regency, Austin, TX

We are excited to announce the **inaugural Life Member Conference**, designed to strengthen the engagement of IEEE's 38,000 Life Members in shaping our collective future. Life Members represent all disciplines across the IEEE's fields of interest. We are also dedicated to giving back and sharing our expertise with the next generation.

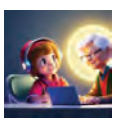
The conference has **three tracks**:

1. **Emerging Technologies – that impact seniors**
   - ❖ Technologies of the Future and the Next Chapter
   - ❖ Aging Society and Technology Progress
   - ❖ Renewable Energy and Sustainability

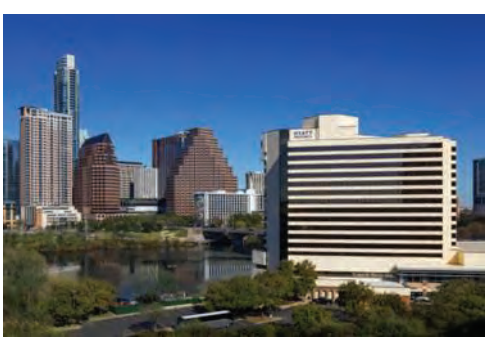
2. **Applications – technologies used by aging populations**
   - ❖ Financial and Investment Strategies
   - ❖ Smart Systems, Infrastructure, Equipment and Living



3. **Contributions – members sharing resources with future leaders**
   - ❖ Mentors and Influencers in the Modern Society
   - ❖ Professional Development, Sharing and STEM Education



Our growing list of speakers include Rodney Brooks (iRobot), John McDonald (GE), Whurley (Strangeworks), Manuela Veloso (JP Morgan), Bernie Sander (AMD), Julie Shah (MIT) (and more!). Speaker commitments are ongoing and over the summer and fall, we'll have a large list of exciting and engaging speakers, keynotes and topics to share.



Join other Life Members, Senior Members, influencers, innovators, technical professionals, and members of the STEM community in Austin for this inaugural event. Registration will be limited, so be sure to secure your spot early.

Stay tuned for further details about the conference at https://life.ieee.org/news-events/ieee-life-members-conference and our social media channels.

EDS Vision, Mission and Field of Interest Statements

Vision Statement
Promoting excellence in the field of electron devices for the benefit of humanity.

Mission Statement
To foster professional growth of its members by satisfying their needs for easy access to and exchange of technical information, publishing, education, and technical recognition and enhancing public visibility in the field of Electron Devices.

EDS Field of Interest
The EDS field-of-interest includes all electron and ion based devices, in their classical or quantum states, using environments and materials in their lowest to highest conducting phase, in simple or engineered assembly, interacting with and delivering photo-electronic, electro-magnetic, electromechanical, electro-thermal, and bio-electronic signals. The Society sponsors and reports on education, research, development and manufacturing aspects and is involved in science, theory, engineering, experimentation, simulation, modeling, design, fabrication, interconnection, reliability of such devices and their applications.