1. Introduction
The purpose of the Outside System Connectivity (OSC) roadmap is to identify communication requirements for systems in different applications, identify gaps in capabilities, identify critical component and device development needs and monitor developments of capabilities to fill these future gaps.

The Internet of Everything (IoE) is continuing to expand in applications that demand higher volumes of higher performance communication. The IoE was initially defined as a wide range of Internet of Things (IoT) devices communicating with cloud computing that store data and which was analyzed with applications and actions communicated. As IoE was used for a broader range of applications, some applications added acceptably slow performance due to the latency of communicating with the cloud. To overcome this latency limitation, some applications added local storage and processing close to the IoT devices and network, which is referred to as fog computing.

Most applications will employ RF/microwave wireless communication to connect to the internet which will then connect through high-performance backhaul or fiber optical interconnects to a cloud data center. In the future, millimeter waves (mmWaves), massive multiple-input multiple-output (MIMO) or other 5G media will be implemented for high-speed connection to terminal devices, while low-power wide-area network (LoWAN) communications, such as LoRaWAN, SIGFOX, LTE Cat 0 and NB-IoT, will be utilized to connect and provide enormous data to the cloud and/or fog computing system from IoT-edge sensor devices. Within the data center, communication to servers is through fiber optical interconnects with signals being routed through multiple routers. Upon arrival at a router, the optical signals are converted to electrical, routed and then converted back to optical signals, which adds to energy consumption and latency. The requested data is then routed out of the data center and returned to the requesting IoT devices through a path similar to the request path.

Applications that require fast communication and decision making, such as autonomous vehicles and traffic control, are adopting edge computing. In this model fast communications are made between the edge and vehicles and traffic flow controls and filtered data is communicated between edge computing and the supporting cloud computing capabilities. Fast communication with low latency is required between the IoT devices and the fog, while fast communication will be required also between elements of the Edge. Computing in the Edge can be performed in a micro data center, which is connected to the network and the internet.

With the rapid growth of high data rate internet applications and IoT, communication rates in data centers need to grow to support high-speed access and provide high-speed low latency communication between servers and memory or other servers. With increased use of high-resolution video, virtual reality, and augmented reality applications, ever higher data rate communication with lower latency is required in data centers. Communication between racks and switches is carried by optical interconnects; however, the capacity of switches is increasing faster than the capacity of fiber interconnects. Also, the power consumed by the switches in data centers is approximately 30% of the power consumed in the data center. To reduce switching power and overcome the fiber capacity gap, companies are working to integrate silicon photonics into the switch. There are also efforts to extend fiber into the server, into packages and thus reduce power. There are significant technical challenges with developing and implementing single mode fiber with low loss for these applications. These challenges will be highlighted in this article.

Applications that will first drive the development of high-volume component and device development are communication in data centers and mobile handheld devices. Over time new applications, such as quantum computing, may arise that require the development of new component and device capabilities and these are monitored in the roadmap.

2. Application/System Requirements & Challenges
While a broad range of applications are assessed in the OSC roadmap, data centers and mobile smartphones are driving development of higher performance circuits and devices and are described in this article.

Data Center Communication
For data centers, the drivers for communication are the data rate per server unit, which is currently 400 Gbps, as shown in Table 1, and

outside system connectivity roadmap
C. Michael Garner
GARNER NANOtechnology SOLUTIONs, Chair OUTside SyStems ConnectivitY

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power consumption. Data centers typically upgrade servers approximately every three years and would like to have the data rates increase when they upgrade the servers; however, this would require upgrading the optical interconnect cables with every server upgrade. Power consumed in communication and switching is becoming significant, 30% of data center power in 2013, and signal integrity is being compromised at higher data rates due to RF loss in the metal trace between the switch chip to the faceplate, so Data Centers are requesting that optical I/O be integrated into the switch package by the 51.2 Tbps switch. The Consortium for On-Board Optics (COBO) or Co-packaged Optics (CPO) is driving to have the photonic transmitter and receiver on the board and connecting this to single-mode fiber in the data center. This would enable upgrading the data center communication rate when the servers are upgraded. At the same time, the routers in data centers are adding communication capacity and ports that consume considerable power, so the industry is seeking ways to reduce router thermal density and improve energy efficiency.

**Mobile Handheld**

As smart phones incorporate more functionality, they will need to communicate at higher data rates, as shown in table 2, with the internet, but also detect signals from GPS satellites, cell towers, health monitors, watches, and other RF sources. Thus, they will need to have compact antennas that can receive and transmit to multiple ranges of frequencies with multiple protocols. The RF and AMS (Analog/Mixed-Signal) components will need to support all of the communication with high energy efficiency for multiple applications simultaneously.

A significant challenge for mobile smartphones is to integrate additional antennas into thin smartphones without causing interference in other communications or integrated circuits.

### 3. Critical Components

**Data Centers**

To achieve higher data rates, more wavelengths than 4 in current CWDM4 format and higher order modulation, will be needed in addition to higher data rates per lane. To support pulse amplitude modulation, DAC/ADCs are needed.

**Mobile Phones**

In the longer term, high frequency mmWave may be used in high population density areas to support high

---

**Table 1: Wavelength Division Multiplexing Module Performance Requirements**

<table>
<thead>
<tr>
<th></th>
<th>2019</th>
<th>2021</th>
<th>2023</th>
<th>2025</th>
<th>2027</th>
<th>2029</th>
<th>2031</th>
<th>2033</th>
<th>2035</th>
<th>2037</th>
</tr>
</thead>
<tbody>
<tr>
<td>System structure</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Data Rate/ Lane [1] (Gbit/s)</td>
<td>100</td>
<td>100</td>
<td>100/200</td>
<td>200</td>
<td>200/400</td>
<td>200/400</td>
<td>400</td>
<td>400</td>
<td>400</td>
<td>400/800</td>
</tr>
<tr>
<td>Data Rate/fiber (Gbit/s)</td>
<td>400</td>
<td>400</td>
<td>800</td>
<td>800</td>
<td>1600</td>
<td>1600</td>
<td>3200</td>
<td>3200</td>
<td>3200</td>
<td>3200</td>
</tr>
<tr>
<td>Distance (km)</td>
<td>&lt; 10</td>
<td>&lt; 80</td>
<td>&lt; 80</td>
<td>&lt; 80</td>
<td>&lt; 80</td>
<td>&lt; 80</td>
<td>&lt; 80</td>
<td>&lt; 80</td>
<td>&lt; 80</td>
<td>&lt; 80</td>
</tr>
<tr>
<td># Wavelengths [2]</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>Number of Bits per symbol (HOM) [3]</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>Additional link penalty due to HOM (dB)</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>9</td>
<td>9</td>
<td>9</td>
<td>9</td>
</tr>
</tbody>
</table>

[1] a lane is for a single data stream with only amplitude modulation in a fiber (per wavelength)
[2] assuming HOM on fully integrated Si Photonics: QPSK/DQPSK demonstrated with Si-photonics, 16-PSK, 32-PSK not demonstrated
[3] assuming integrated laser on Si after 2019, 40 mW on WDM laser at high temperature not demonstrated yet
HOM: Higher Order Modulation (i.e. PAM4, QPSK, etc.)
PAM: Phase Amplitude Modulation
QPSK: Quadrature Phase-Shift Keying
WDM: Wavelength-Division Multiplexing
data rate applications with a large number of users. A significant challenge is that 28 GHz to 78 GHz signals do not penetrate buildings, so buildings would need to have repeaters in the building or employ massive MIMO or ultra-high data rate Wi-Fi.

If 5G is implemented with mmWave and MIMO, cell phones would need to have multiple antennas to receive and transmit information and each antenna would need to have power amplifier (PA) and an ADC and DAC [1], which would consume considerable power operating with high precision at high frequencies. A critical challenge is to increase the energy efficiency of the PA at mmWave frequencies while maintaining linearity, since the efficiency of the PA decreases with operating frequency. Thus, higher performance of incumbent process technologies or even new materials may be required to improve energy efficiency. In the transmit mode, the antenna array would operate as an active phased array to focus transmission toward the base station. To overcome the high operating power of the high precision DAC/ADCs, use of hybrid analog/digital preprocessing [2, 3] or lower precision DAC/ADCs (1bit) [1, 2, 4] has been proposed. To compensate for potential blockages [5], multiple antennas would need to be integrated into the cell phone to be connected with multiple base stations.[6]

For >10 Gb/s communication rates, proposals have been made for a single bit zero crossing modulation protocol; however, energy efficiency of all required components need to be investigated.

4. Integrated Circuits
To increase data rates of communication with lower power and lower power, DACs and ADCs need to operate with higher sampling rates and lower power consumption. Also, serializer-deserializer (SERDES) circuits need to operate at higher frequencies with higher efficiency. To achieve higher data rates with improved energy efficiency in these circuits, devices need to operate with lower power at higher frequencies. This may require introduction of new device, gate, contact, or interconnect materials while decreasing circuit cost.

Recently, a 5 nm integrated circuit technology was announced that demonstrated a transmitter test circuit that operated at 130 Gb/s data rates with PAM4 modulation and 0.97 pJ/bit energy consumption [7].

Table 2: Mobile Device Wireless Cellular Performance Requirements

<table>
<thead>
<tr>
<th>Year</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
<th>2024</th>
<th>2025</th>
<th>2026</th>
<th>2027</th>
<th>2028</th>
<th>2029</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cellular Data Rate Gbps (Max.)</td>
<td>5</td>
<td>5</td>
<td>7</td>
<td>7</td>
<td>7</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>20</td>
</tr>
<tr>
<td>Max. Cell Range(^a) (km) [unobstructed]</td>
<td>35/0.2-1</td>
<td>35/0.2-1</td>
<td>35/0.2-1</td>
<td>35/0.2-1</td>
<td>35/0.2-1</td>
<td>35/0.2-1</td>
<td>35/0.2-1</td>
<td>35/0.2-1</td>
<td>35/0.2-1</td>
</tr>
<tr>
<td>3G Frequency</td>
<td>&lt;4 GHz</td>
<td>&lt;4 GHz</td>
<td>&lt;4 GHz</td>
<td>&lt;4 GHz</td>
<td>&lt;4 GHz</td>
<td>&lt;4 GHz</td>
<td>&lt;4 GHz</td>
<td>&lt;4 GHz</td>
<td>&lt;4 GHz</td>
</tr>
<tr>
<td>4G Frequency</td>
<td>&lt;4 GHz</td>
<td>&lt;4 GHz</td>
<td>&lt;4 GHz</td>
<td>&lt;4 GHz</td>
<td>&lt;4 GHz</td>
<td>&lt;4 GHz</td>
<td>&lt;4 GHz</td>
<td>&lt;4 GHz</td>
<td>&lt;4 GHz</td>
</tr>
<tr>
<td>5G Maximum Data Rate (Gbps)</td>
<td>5</td>
<td>5</td>
<td>7</td>
<td>7</td>
<td>7</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>20</td>
</tr>
<tr>
<td>6G Maximum Data Rate (Gbps)</td>
<td>20</td>
<td>20</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>70</td>
<td>70</td>
<td>70</td>
<td>70</td>
</tr>
</tbody>
</table>

\(^a\) Assumes that Massive MIMO will be implemented in 2019 and full 5G performance in 2025.

\(^b\) Assumes 4G LTE through 2017, Massive MIMO <6 GHz through 2023 and both Massive MIMO <6 GHz and mmWave beyond 2025.
5. Device Requirements, Challenges & Potential Solutions

**CMOS Devices**
The 2022 roadmap technology plots reflect the RF and analog performance metrics needed to support the technology roadmap developed by the IRDS More Moore IFT in 2017. The RF-AMS performance metrics for CMOS devices have been restricted to peak \( f_T \) (Figure 1) and peak \( g_m \) (Figure 2) and have been calibrated on recent averaged measured data in the 28 nm, 22 nm, and 16 nm nodes. The 2020 roadmap gives the above performance FoMs for n-channel FDSOI and double-gate FinFET high-performance devices obtained from technology computer aided design (TCAD)-based device modeling methods(a) [8]. These include hydrodynamic transport with thin silicon mobility physics, as well as the estimated resistive and capacitive device parasitics up to the first metal layer, which defines the terminals of a transistor in high-frequency analog circuit design. They indicate the degradation in \( f_T \) and \( g_m \) at gate lengths below 10 nm as a result of mobility degradation caused by surface scattering at the gate oxide interface, and due to the ever-thinner silicon body. As can be observed, the double gate of the FinFET results in higher transconductance but also higher capacitive parasitics compared to the single-gate FDSOI MOSFETs. Note that the displayed \( f_T \) (Figure 1) does not include the capacitive parasitics resulting from connecting the transistor cell to the passive devices in the upper metal layers of the back-end. The introduction of new materials, and transistor and gate structures may change the \( f_T \) trend of sub 10 nm CMOS devices. Reduction of gate and contact resistance has been demonstrated to improve \( f_{max} \) [9, 10], but not impact \( f_T \).

Many of the materials-oriented and structural changes being invoked in the digital roadmap degrade or alter RF and analog device behavior. Complex tradeoffs in optimization for RF, HF, and AMS performance occur as different mechanisms emerge as limiting factors. Examples include series resistances at gate, source and drain, as well as parasitics from interconnecting the transistors to other devices in a circuit that greatly affect the device impedances and the “loaded” figures of merit as measured at the upper metal levels. Fundamental changes of device structures, e.g., multiple-gates and silicon-on-insulator (SOI), to sustain continued digital performance and density improvements greatly alter RF and AMS characteristics. Such differences, along with the steady reduction in supply voltages, pose significant circuit design challenges and may drive the need to make dramatic changes to existing design structures.

**Group IV Bipolar**
The roadmap for SiGe heterojunction bipolar transistors (HBTs) and associated benchmark circuits at mm-wave frequencies has been based since 2013 on a seamless set of TCAD device simulation tools in order to obtain consistent compact model parameters for the complete transistor structure used in the respective circuit simulations. All known transport, structural parasitics up to metal 1 (i.e. transistor cell terminals) and temperature effects have been included in the results [11] and calibrated based on experimental data. Furthermore, the TCAD tools and those parameters that cannot be obtained by TCAD have been calibrated on existing prototyping process technologies. Performance

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*Figure 1. CMOS Roadmap for Peak \( f_T \) vs. Physical Gate Length for FDSOI and Double-gate (FinFET) MOSFETs Based on Technology CAD.*

*Figure 2. CMOS Roadmap for Transconductance per Unit Gate Width, \( g_m \) vs. Physical Gate Length for FDSOI and Double-gate (FinFET) MOSFETs Based on Technology CAD.*

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\(^1\)TCAD simulations performed by Sorin Voinigescu at the University of Toronto.
plateaus have been assumed to last four years and are linked to applications and the foregoing system drivers. It has been assumed that at least two foundries offering the technology of the respective node for product prototyping are presented. The benchmark circuits for LNA, PA, VCO, and current-mode-logic-based (CML) ring-oscillator (RO) have been manually optimized for each technology node and a variety of commercially relevant frequencies. The most recent result for a prototyping process [12] corresponds closely to the performance predicted for node N3 (Figures 3, 4).

Even though it is a challenge for the HS-NPN to increase the unity current gain cut-off frequency $f_T$ by more aggressive vertical profiles, it is less of a challenge to achieve $f_{MAX} > f_T$. What is unclear today is, how large the ratio $f_{MAX}/f_T$ needs to be for future circuit applications. That is, the challenge is to determine what this ratio should be by using the "plateau technologies" for the next roadmap and appropriate benchmark circuits. Since lateral scaling requirements for HBTs are significantly relaxed compared with those for MOSFETs, vertical profile fabrication under the constraints of overall process integration appears to be the bigger challenge. The reduction of imperfections and the increase of current carrying capability of the emitter and collector contact metallization are further challenges that need to be met by process engineers on the way to achieving the physical limits of this and any other technology [12].

**III-V FET and Bipolar**

The FoMs depend on technology and include: $f_T$, $f_{MAX}$, $g_m$, and $V_{BD}$; power, gain, and efficiency at 10, 24, 60, 94, 140, and 220 GHz; $NF_{MIN}$ and $G_s$ at 10, 24, 60, and 94 GHz; LNA NF and $G_s$ at 140 and 220 GHz. $f_T$ and associated gain are as shown in Figures 5–6. As mentioned previously, RF and AMS front-end components are a growing part of the semiconductor industry. However, this has divided the III-V technology landscape into two groups, one dominated by the large volume consumer market and the other dominated by low volume specialty markets. Within the III-V technology landscape, the large volume consumer driven market is best represented by GaAs HBT power amplifiers for cellular communications.

The unique challenges for III-V devices are yield (manufacturability), substrate size, thermal management, integration density, dielectric loading, and reliability under high fields. Challenges common with Si-based circuits include improving efficiency and linearity/dynamic range, particularly for power amplifiers. A major challenge is increasing the functionality of power amplifiers in terms of operating frequency and modulation schemes while simultaneously meeting increasingly stringent linearity and efficiency requirements at the same or lower cost.

**Photonic Integrated Circuits and Devices**

Near-term challenges are to 1) increase the data rate per wavelength and total throughput per fiber, density of optical transceivers while reducing their power and cost, and 2) develop a router/switch package integrated photonic interconnects for data centers. Long-term challenges include 1) processing information in the optical domain, and 2) developing methods for communication between systems with different wavelengths, polarizations, and modulations.

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**Figure 3. High Speed SiGe HBT $f_T$ and $f_{MAX}$ Roadmap vs. Year of Production.**

**Figure 4. High Speed SiGe HBT Maximum Available Gain Roadmap vs. Year of Production.**
Photonic Integrated Circuits (PIC)

Recently, photonic integrated circuits on silicon, using either hybrid or heterogeneous integration methods, have been introduced into the market by multiple transceiver manufacturers. Currently, some of these products have separate transmitter and receiver chips.

Some of these transmitter circuits have the lasers integrated with the modulators, while some of these have the laser packaged separately from the modulators. In most cases, the modulators and waveguides are fabricated on single-crystal silicon on insulator wafers. Most suppliers are employing Mach Zehnder modulators, while more compact ring modulators are being evaluated in research and moving to product phase in a few years. Since ring modulator operating wavelength is sensitive to temperature, they have been integrated with tuning elements to control the optimal wavelength, which increases power consumption and cross-talk, which must be managed. Many of these transmitter circuits employ multiple wavelengths that either are transmitted over individual fibers or multiplexed into a single fiber. Mach Zehnder modulators and the (de)multiplexers currently use silicon waveguides and the weak electro-optic effect from free carriers means the foot-print of the PIC is relatively large. Future energy-savings from these circuits, will depend upon improvements to laser wall-plug efficiency and reduction in size and power consumption of electro-optic modulators, thereby having a cascading effect of reduced power consumption and cost for the photonic chip, and supporting integrated circuits.

Low Power High Output Lasers

To reduce the power consumed in communication, there is a need to increase the efficiency of lasers in converting electrical energy to photons. VCSELs and edge-emitting lasers are used for different applications and may be competing in some applications as silicon photonics strives to reduce cost while increasing data rates.

Although VCSELs are more energy efficient than edge emitting lasers, the power to modulate at higher data rates will increase, which can cause reliability issues. So more efficient top emitting lasers are needed in the future. To support high volume manufacturing, III-V quantum dot VCSELs epitaxially grown and fabricated on (001) silicon [13] with p-doping [14] have been demonstrated with high stability over a wide temperature range.

An emerging technique to increase photonic light source energy dissipation is to introduce nanostructures that increase energy density. This has been used to demonstrate electrically pumped lasers with lasing thresholds of 287 nA at 150 K [15] that is 1000x less than earlier electrically pumped nanocavity lasers.

Some short-distance communication links may also be powered by high-efficiency LEDs (no threshold). However, higher throughput relies on efficient packaging of several thousand spatially multiplexed optical channels.

High-Density Low Power Modulators

For optical interconnects to meet future requirements, all supporting devices must operate with higher performance, lower energy consumption, higher optical efficiency, and have a lower cost. Essential for long-distance communication, Electro-Optic Modulators (EOM) can modulate the amplitude, phase, frequency, or polarization...
of the light; however, these devices must become more compact, and operate with lower power consumption. Compact modulator options in the future will likely use the following physical effects: electro-absorption modulation, bulk semiconductor Franz-Keldysh effect (III-V, Ge), plasmonics, Stark Effect, or Wannier-Stark localization.

**High Speed, High-Density Photodetectors**

A significant challenge for optical detectors is to increase operating frequency to support higher data rates. A limiting factor is the RC time constant of the photodetector. The most logical solution is to reduce the detector size which reduces junction capacitance, but this may not be able to absorb most of the light, i.e., poor responsivity. Ongoing efforts are focused on reducing the junction and contact resistance for the smaller photodetectors, and achieve a good speed-responsivity tradeoff. The most recent research breakthrough has yielded a bandwidth in excess of 250 GHz [16]. If the detector intercepts less light from the waveguide, the amplifier will need to have higher gain that will potentially reduce the signal-to-noise ratio. The best solution to this is to develop techniques to effectively couple light from the waveguide into the detector. Possible solutions include using plasmonic structures above the photodetectors to focus light into the detector. Another option is to include passive periodic or apodized nanophotonic structures to focus light onto the photodetector. The temperature dependence of the potential solutions needs to be understood, to design the optimal solution.

**Optically Based Switching and Routing**

Currently, optical signals are redirected by electrical routers where the light must be converted to electrical signals that are routed to different fiber channels. This significant latency can be added to the transmission of optical signals that go through multiple routers. New technologies are needed to enable optically based switching and routing that do not require the optical-electrical-optical conversion. Hybrid electrical/optical (E/O) routing capabilities have been demonstrated using both MEMS [17–20] and E/O switches including Mach-Zehnder interferometers [21] and ring resonators [22].

If all-optical networks are to be viable, optically based logic will be needed to identify signal stream routing conflicts and determine the correct routing alternative. A number of optical logic devices and functions have been proposed that require local nonlinearity of optical properties [23]. It is proposed that branched waveguides with local nonlinear optical materials could function as AND or OR functions [24].

**6. Summary**

Future system communication requirements are driving development of new communication architectures, circuits, and devices. The OSC promises high speed and low power. The OSC industry needs to make major contributions of the IEEE IRDS within the next 3 years. The OSC will need to have higher gain than today’s photodetectors, and achieve a good speed-responsivity tradeoff.

**7. Acknowledgments**

The author acknowledges the valuable contributions of the IEEE IRDS members and former ITRS members to the IEEE IRDS Outside System Connectivity Roadmap. Furthermore, valuable improvements were made to this paper by Carlos Augusto, Di Liang, and Sudharsanan Srinivasan.

**References**


