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Newsletter

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TECHNICAL BRIEFS

SILICON SOLAR CELL TURNS 70

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On 25 April 1954, Bell Labs in Murray Hill, New Jersey announced the invention of a silicon solar cell. They demonstrated their solar panel by using it to power a small toy Ferris wheel and a solar-powered radio transmitter. *The New York Times* on 26 April 1954 wrote that the silicon solar cell "may mark the beginning of a new era, leading eventually to the realization of one of mankind's most cherished dreams–the harnessing of the almost limitless energy of the sun for the uses of civilization."

Vast Power of the Sun Is Tapped By Battery Using Sand Ingredient

Special to The New York Times.

MURRAY HILL, N. J., April 25—A solar battery, the first of its kind, which converts useful amounts of the sun's radiation directly and efficiently into electricity, has been constructed here by the Bell Telephone Laboratories.

The new device is a simple-looking apparatus made of strips of silicon, a principal ingredient of common sand. It may mark the beginning of a new era, leading eventually to the realization of one of mankind's most cherished dreams—the harnessing of the almost limitless energy of the sun for the uses of civilization.

The sun pours out daily more than a quadrillion (1,000,000,000,000,000) kilowatt hours of energy, greater than the energy content of all the reserves of coal, oil, natural gas and uranium in the earth's crust.

With this modern version of Apollo's chariot, the Bell scientists have harnessed enough of the sun's rays to power the transmission of voices over telephone wires. Beams of sunlight have also provided electricity for a transistor in a radio transmitter, which carried both speech and music.

The Bell scientists reported they had achieved an efficiency of 6 per cent in converting sunlight directly into electricity. This, they asserted, compares favorably with the efficiency of steam and gasoline engines, in contrast with other photoelectric devices, which have a rating of no more than 1 per cent.

With improved techniques the efficiency may be expected to be increased substantially they added. They observed that nothing is consumed or destroyed in the energy conversion process and there are no moving parts, so the solar battery "should theoretically last indefinitely."

The experimental solar battery uses strips of wafer-thin silicon about the size of common razor blades. These strips are extremely sensitive to light. They can be linked together electrically and can deliver power from the sun at the rate of 55 watts a square yard of surface.

The atomic battery recently announced by the Radio Corporation of America delivers one-millionth of a watt. The new Bell solar battery thus delivers 50,000,000 times the power of the R.C.A. atomic battery.

Silicon is a semiconductor,

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The New York Times: April 26, 1954
"Vast Power is Tapped by Battery Using Sand Ingredient"

…may mark the beginning of a new era, leading eventually to the realization of one of mankind's more cherished dream —the harnessing of the almost limitless energy of the sun for the uses of civilisation".

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Your comments are most welcome. Please write directly to the Editor-in-Chief of the Newsletter at daniel.tomaszewski@imif.lukasiewicz.gov.pl

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NEWSLETTER DEADLINES

ISSUE	DUE DATE
October	July 1st
January	October 1st
April	January 1st
July	April 1st

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Silicon Solar Cell Turns 70

(continued from page 1)

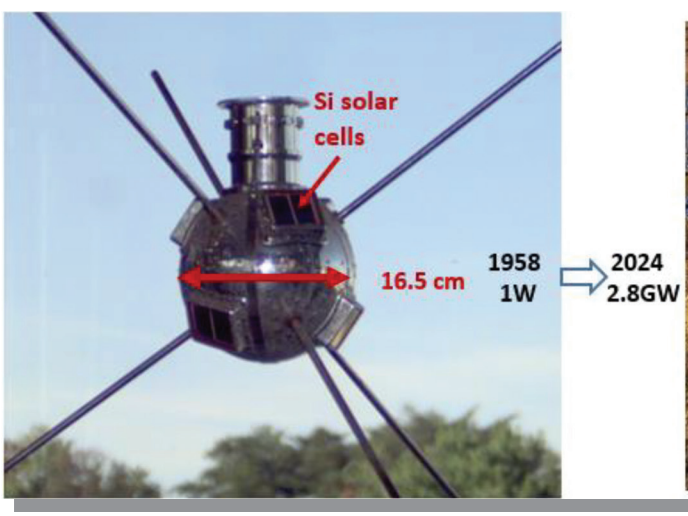
The inventors Daryl Chapin, Calvin Fuller, and Gerald Pearson were simply trying to solve problems within the Bell telephone system to explore alternative sources of freestanding power. Selenium solar cells, the only type on the market, produced too little power—a mere 5 watts per square meter—converting less than 0.5% of the incoming sunlight into electricity. Calvin Fuller, a chemist, and Gerald Pearson, a physicist, were studying the properties of semiconductors by introducing impurities. They observed that when gallium-doped silicon was dipped in lithium, it resulted in a light-generated current, to their surprise. Observing the instability of lithium, they replaced it with arsenic to get a stable p-n junction. It yielded ~ 6% conversion efficiency. That was the beginning of switching from selenium to silicon [1].

The inventors of the Si p-n junction Bell Solar Battery, from left, Gerald Pearson, Daryl Chapin, and Calvin Fuller, Credit: AT&T Archives.

In 1958, the American satellite *Vanguard 1* entered orbit with six square silicon solar cells, (roughly 5 cm on a side) which generated about 1-watt power in total. Most PV interests in the US were for space applications. The IEEE started the first Photovoltaic Specialists Conference (also called PVSC) in 1961 at the NASA headquarters in Washington DC. It is the longest-running technical conference dedicated to photovoltaics, solar cells, and solar power.

Growing interest in re-evaluating terrestrial applications emerged with the release of small commercial modules by Sharp, Philips, and Solar Power in the early 1970s. The energy crisis and subsequent oil embargoes stimulated the rapid development of PV technology in the mid-1970s, with the first modern modules fabricated in 1976. In 1978, President Carter founded the Solar Energy Research Institute (SERI) in Golden, Colorado and later in 1991, President George H. W. Bush elevated SERI to a national member of the Department of Energy (DOE) - National Renewable Energy Laboratory (NREL). Martin Green, PV pioneer and world-leading specialist in both monocrystalline and polycrystalline silicon solar cells, founded in *University of New South Wales* (UNSW) Australia, Engineering, the largest and best-known university-based photovoltaic research group in the world in 1974 [2].

The US DOE SunShot initiative was launched in 2011 with the goal of cost reduction of utility-scale solar to approximately $1 per watt- or $0.06 per kilowatt-hour that



Vanguard 1 *with its six solar cells attached*
(Source: Wikipedia)

2.8 GW Golmud Solar Park in China
(https://www.theecoexperts.co.uk/solar-panels/biggest-solar-farms)

was met three years earlier in 2017. The program recently expanded its target to $0.03 per kilowatt-hour by 2030.

Crystalline silicon with a bandgap of 1.12 eV has the theoretical Shockley and Queisser efficiency limit of ~ 29.4% [3]. Over the last seven decades, academics, scientific laboratories, and niche industries worldwide have remained diligently committed in achieving higher efficiencies across cell, module, and system levels. A series of high-efficiency crystalline silicon solar cell structures have emerged, that include passivated emitter rear cell (PERC), passivated emitter, rear locally diffused cell (PERL), interdigitated back contact cell (IBC), heterojunction with intrinsic thin-layer cell (HIT), heterojunction solar cells with interdigitated back contacts (HBC), bifacial cells and TOPCon solar cells. At the substrate level, monocrystalline silicon grown by the Czochralski method has dominated in efficiency and cost reduction by increasing the wafer size (210 mm × 210 mm) and decreasing the wafer thickness (~170 µm). Cells have reached ~ 27.5% in efficiency today. Detailed information on these innovations, co-authoring with Martin Green will be presented in IEEE Electron Devices Magazine. The efficiency has increased ~ 0.3% per year since 1954 and worldwide silicon PV installations have exceeded terawatts. The Golmud Solar Park in China is the world's largest solar farm at present with an installed solar capacity of 2.8 GW, with nearly seven million solar panels. Happy Birthday, Si Solar Cell!

Rochester IEEE EDS local chapter will celebrate the 70th birthday of Si Solar Cell at the Imagine RIT Festival dedicated to sharing scientific and technical achievements with the public on 27 April 2024.

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8th IEEE Electron Devices Technology and Manufacturing (EDTM) Conference

Theme: "Strengthening Globalisation in Semiconductors"

3–6 March 2024 Bengaluru, India

Introduction

Since its inception in 2017 in Toyama, Japan, IEEE Electron Devices Technology and Manufacturing (EDTM) Conference has been hosted by all the major Asian countries with semiconductor manufacturing hubs. The 8th edition of this conference was held in India for the first time at Bengaluru; the Silicon Valley of India and hub of semiconductor companies; preserving the tradition. **IEEE EDTM 2024** was an in-person full four-day conference held between 3–6 March 2024 at the Hilton hotel Bengaluru Embassy Manyata Business Park. Promoting the theme of "***Strengthening Globalisation in Semiconductors***", this conference was loaded with 6 plenary talks, more than 145 keynote/invited talks, 140 accepted oral papers, over 107 accepted poster presentations with proceedings, and 60 accepted poster presentations without proceedings. In addition to the technical sessions, EDTM began with tutorials and short courses specifically designed to provide participants with in-depth knowledge and hands-on experience on advanced topics related to electron device technology and manufacturing. The conference was attended by over 600 participants from around 20 countries from all over the world, including US, UK, Spain, India, Belgium, Netherlands, Bangladesh, Austria, Australia, Russia, France, Saudi Arabia, Japan, and Taiwan. 26 national and international sponsors including 11 exhibition stalls embraced the event with their presence.

Day-wise details of the 2024 IEEE EDTM conference are presented below.

Day 0 (3 March)—Tutorials and Short-courses

The day prior to the technical sessions i.e. 3 March was dedicated to Tutorials and Short-courses which were conducted by the leading experts in the field from both industry and academia. EDTM 2024 offered 4 tutorials and 3 short-course sessions designed to provide in-depth insights and hands-on experience on specific topics of interest. These sessions allowed attendees to gain practical knowledge and skills in areas such as device fabrication techniques, simulation tools, and emerging technologies. Topics of the tutorials and their details are given below:

Tutorial 1: Wide Bandgap Devices for RF and Power Applications

GaN Power Transistors: Technology and Applications by **Ken Shono**; *Transphorm Japan.*

In this tutorial, structure, benefit, quality & reliability, and application of GaN were presented. There are two types of GaN in the market. One is Cascode GaN, another is p-GaN E- mode. A comparison of the two types was given. SiC is already in the market as high high-efficiency power switch. Pros and Cons of GaN and SiC were also discussed.

GaN Microwave/RF Transistors: From Fundamentals to Emerging Trends by **Digbijoy Nath**, *Indian Institute of Science Bangalore, India.*

This tutorial was dedicated to the basics of GaN RF HEMT keeping the focus on practical issues that are relevant for technology such as the effect of substrate, dislocations, compensation doping, device dimensions, passivation, etc. It was also discussed how various device dimensions and material/device properties affect device parameters, and how those, in turn, affect the performance of a power amplifier. How the device design and various aspects of it evolve with the need for power at higher frequencies, was also touched upon. Next, the lecturer discussed the transition to multi-finger HEMTs with high absolute output power because these are the devices that go into real-world systems. Since most research publications and reports on GaN HEMTs concern two-finger devices only, a large part of the know-how on how to realize multi-finger GaN RF HEMTs is often strategic in nature and also proprietary, and hence, not published. Finally, emerging trends in GaN RF devices were discussed in relation to the literature. These include GaN on silicon for low-power applications - especially E-mode devices, N-polar GaN for W-band, ultrathin barrier and buffer-free HEMTs, and approaches to realizing GaN HEMTs with better linearity. Future challenges and opportunities for GaN HEMT were also discussed.

Tutorial 2. Reliability in Advanced Semiconductor Devices

A Device to Circuit Framework for Aging (BTI, HCD) in Advanced Technology Nodes by **Souvik Mahapatra**, *IIT Bombay, India.*

In this tutorial, the following topics were discussed;

- Characterization of BTI and HCD, recovery, impact of measurement delay
- BTI Analysis Tool (BAT) framework-related analysis of measured BTI data - estimation of end of life (EOL), process impact of BTI
- Hot Carrier Analysis Tool (HCAT) framework-related analysis of measured HCD data - decoupling of BTI and HCD, the impact of Self Heating
- TCAD for reliability - BTI and HCD simulation
- Circuit analysis for aging due to BTI and HCD, using Circuit Aging Reliability Analysis Tool (CARAT), demonstration of a seamless TCAD to SPICE framework

Insulators for Devices based on 2D Materials by **Tibor Grasser**, *Institute of Microelectronics, TU Wien, Austria.*

The selection of suitable insulators for 2D nanoelectronics has always been a challenge. this tutorial addressed the current state of the art and summarized the main problems together with potential solutions. This problem is of key importance since scaling of 2D semiconductors towards sub-10 nm channel lengths is only possible with gate insulators scalable down to sub-1 nm equivalent oxide thicknesses (EOT). To achieve competitive device performance, these insulators need to meet stringent requirements regarding (i) low gate leakage currents, (ii) low density of interface traps, (iii) low density of border insulator traps, and (iv) high dielectric strength.

The insulators typically used for 2D electronic devices are amorphous 3D oxides known from Si technologies (SiO_2, HfO_2, Al_2O_3), while native 2D oxides (MO_3, WO_3, and Bi_2SeO_5), layered 2D crystals (hBN, mica) and ionic 3D crystals (CaF_2 and other fluorides like SrF_2, MgF_2) have received increasing attention. 3D oxides often form poor-quality interfaces with 2D semiconductors and contain border traps which severely perturb stable device operation. Native oxides, on the other hand, are often non-stoichiometric due to the lack of well-adjusted oxidation methods and thus have limited dielectric stability and inherently narrow bandgaps. As the most popular candidate, the layered 2D insulator hBN forms excellent van der Waals interfaces with 2D semiconductors but has mediocre dielectric properties resulting in excessive leakage currents for sub-1 nm EOT. The potential of other 2D insulators (e.g. mica) is currently unclear, in part due to the absence of scalable growth techniques. Finally, very promising insulators for 2D electronics are 3D ionic crystals like CaF_2 which form well-defined interfaces to 2D channel materials. In contrast to hBN, fluorides have good dielectric properties and thus exhibit low gate leakage currents.

Tutorial 3. Artificial Neural Networks

In-Memory Computing for Artificial Neural Networks by **Abu Sebastien**, *IBM Research Zurich, Switzerland.*

This tutorial introduced Analog In-Memory Computing (AIMC) using non-volatile memory technology, emphasizing key concepts and related terminology. Following that, it presented a multi-tile mixed-signal AIMC chip designed for deep learning inference. Fabricated using 14nm CMOS technology, this chip features 64 AIMC cores/tiles built on phase-change memory technology. This presentation served as a foundation to explore the device, circuitry, architectural, and algorithmic aspects of AIMC in more detail. A key focus was on achieving classification accuracy equivalent to floating point precision while conducting the majority of computations in the analog domain with relatively lower precision. At the end, the tutorial discussed ongoing research efforts aimed at the next generation of AIMC chips and offered insights into the future outlook of this technology.

Biologically Realistic Artificial Neural Networks by **Veeresh Deshpande**, *IIT Bombay, India.*

The tutorial introduced the basics of piking neural networks (SNNs) highlighting the bio-realistic elements in their implementation and some of the learning/training mechanisms employed. The speaker briefly touched upon SNN hardware implementation examples, implementation of quantum tunneling-based neurons, and SNN implementation in 45 nm CMOS technology. Thereafter, various approaches and examples of the implementation of neurons, synapses, and SNNs with unique properties of nanoscale non-volatile memory (NVM) devices in hybrid CMOS-NVM technology were discussed. The talk was concluded by discussing challenges and opportunities for NVM-based implementation of SNNs.

Tutorial 4. TCAD and Compact Modeling

Compact Modeling: General Introduction and Modeling of Statistical Variability by **Gert-Jan Smit**, *NXP Semiconductors, The Netherlands.*

This tutorial started with a general introduction to compact modeling which included the role of compact models in the design flow, challenges related to their development, and a quick overview of the main compact models that are used in the industry today. Then, the presentation elaborated on the variability that inherently comes with semiconductor manufacturing. Accounting for this variability during circuit design is critical for the development of products with good fabrication yield. Consequently, it is critical that SPICE libraries not only accurately reflect the nominal behavior of the electrical components, but also capture the stochastic variations. It also reviewed, the most used methods to model variability in industrial SPICE libraries: fixed corners and Monte Carlo models. What are they based on, how are these models created, what modeling techniques are used, what do they represent, and - very importantly - what do they not represent? Special attention was devoted to the intrinsic limitations of corner models. Finally, the speaker discussed some lesser-known domains where variability modeling is very important: 1/f noise and (passive) backend devices.

MOSFET Characterisation and Modeling for Cryogenic Applications by **Thomas Bedecarrats**, *CEA-Leti, Grenoble, France.*

This tutorial provided an overview of today's measurement methods, the latest reported cryogenic electrical behaviours, and corresponding compact modeling strategies. Finally, it discussed what is missing to get an operational PDK for IC design.

TCAD-based Compact Model Parameter Extraction of Si and SiC High-Power Devices by **Vinay Kumar**, *Synopsys, India.*

In this tutorial, the steps w.r.t. Process and Device simulation of power devices using Sentaurus TCAD – simulation of device characteristics required for extracting the model parameters of a given compact model were discussed in detail. The compact model could be a standard model approved by CMC for high-voltage power devices or a user-defined model based on a sub-circuit modeling approach. In the end, the speaker elaborated on the validation aspects of the compact model before using it for the circuit design tasks.

Short courses

Along with the tutorial sessions, short courses were conducted on the same day by experts in the field.

Short Course 1. Advances in Logic Devices

Logic Technology Roadmap by **Gaurav Thareja**, *Applied Materials, USA.*

This short course focused on the logic technology roadmap. The current state of transistors and interconnects, materials/process/equipment challenges, and emerging technologies for next-generation low-power, high-performance computing were explored. With FinFET scaling approaching its limits, innovative device architectures emerge as promising candidates for next-generation transistor technology, including **G**ate-**A**ll-**A**round (**GAA**) and complementary **FET** (**CFET**). To address large wire delay and the high IR drop issue resulting from continuous area scaling, novel interconnect material and innovative integration schemes like **B**ackside **P**ower **D**elivery **N**etwork (**BSPDN**) have been developed. It was also discussed why the technology roadmap follows a 'perseverant tortoise' approach and how we can expedite this.

Nanosheet-based Transistor Architectures for Advanced CMOS Scaling by **Hans Mertens**, *IMEC Leuven, Belgium.*

This short course covered various aspects of nanosheet-based transistor fabrication. The basic building blocks of GAA nanosheet fabrication were visualized by 3D animations. Subsequently, potential solutions to either place nanosheet-based transistors closer to each other

Short course "Advances in Logic Devices/Logic Technology Roadmap" by Hans Mertens.

(Forksheet) or stack them on top of each other (CFET) were described. Recent progress in the fabrication of these types of transistors was discussed, covering front-end-of-line and middle-of-line innovations.

Short Course 2. Advances in Memory Technologies

DRAM and NAND Memories: Technology and Design Perspectives by **C. R. Parthasarathy**, *Micron Technology, India.*

This short course covered the fundamentals of the NAND and DRAM memories. The basics of technology and the devices associated with these memories were examined. The issues of scaling and design that provide exciting opportunities to create next-generation memory systems were also addressed.

DRAM Scaling: History and Innovation by **Sungho Jang**, *Samsung Electronics, South Korea.*

This course introduced the evolution and challenges of DRAM cell technology for DRAM scaling to increase its capacity. The future directions of scaling technology and topics such as overcoming data sensing margin challenges and the DRAM peripheral transistor technology challenges for achieving high performance of graphic DRAM (GDDR), and high-bandwidth memories (HBM) for AI servers in the era of sub-15 nm deep scaling were also discussed during this course.

Short Course 3. Semiconductor Packaging Technology

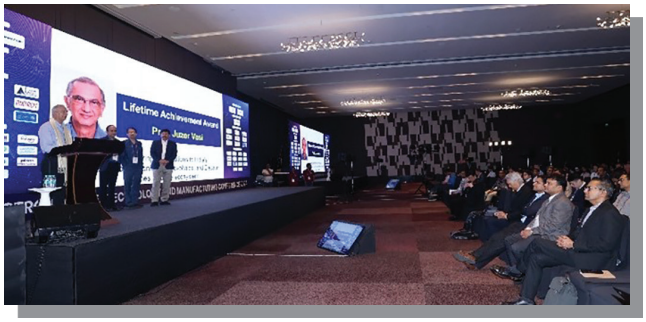
Recent Advancements in Interconnect Materials and Technologies in Semiconductor Packaging by **Nilesh Badwe**, *Indian Institute of Technology Kanpur, India.*

This course covered the advancement in both the first-level interconnects (FLI) and second-level interconnects (SLI) in semiconductor packaging. The FLIs have evolved from older generation techniques like wire bonding or flip chip using soldering to solderless direct copper-to-copper hybrid bonding enabling sub-10 µm pitch with significant improvement in performance. The course also highlighted the progress in the SLI connections with a case study on low-temperature solders for board-level assembly.

Day 1 (4 March): Inauguration Day

The inauguration started with welcoming all the participants including Plenary, Keynote, and Invited speakers by Prof. Yogesh Singh Chauhan (General Chair, EDTM 2024) and Prof. Mayank Shrivastava (General Co-chair, EDTM 2024). This was followed by the presentation of the Technical Program Committee report by Prof. Nihar Ranjan Mohapatra (TPC Co-Chair, EDTM 2024).

The crowning moment of the Inauguration session was conferring the Life-time Achievement Award to **Prof. Juzer Vasi** for his immense contribution to Indian micro/nano-electronics research, known for sowing the seeds of microelectronics education in India. The IEEE EDS Early Career award was also given to Prof. Shubham Sahay from IIT Kanpur.



Conferring the Life-time Achievement Award to Prof. Juzer Vasi.

Following the inauguration session, the first plenary talk *Semiconductor – the Next 75 Years?* was given by **Prof. Chenming Hu** (*TSMC Distinguished Professor Emeritus, University of California Berkeley, USA*). He summarized the past 50 year history of semiconductor research and how it has contributed to the digital age lifting up the technology, industry, and even science. The second plenary talk *GaN Technology enabling Power Electronics* was given by **Sameer Pendharkar** (Vice President Technology Development and TI Senior Fellow, *Texas Instruments, USA*). 25 parallel sessions including 15 keynote, 47 invited and 38 oral presentations were witnessed by the participants on the first day of the conference covering the topics of CMOS Technology Scaling, RF, Millimetre and Terahertz Technologies, Circuits and Systems, TCAD and Manufacturing, Emerging Memory Technologies, Ferroelectric Materials and Devices I, WBG Device Applications, Packaging Materials, 2D Sensors, Design Technology Co-Optimization I, Neuromorphic Computing I, TCAD Simulation, Ferroelectric Memories, 2D Materials and Devices I, High Power Device Reliability, Packaging—Mechanical Properties and Reliability, Microfluidics and MEMS Sensors, Technology for Future Chips, Semiconductor Device Characterization, Neuromorphic Computing II, TCAD and Device Modeling, Ferroelectric FETs, Neuromorphic Devices, SiC-based Power Devices, Memory and Metallization Reliability, Yield, and Manufacturing.

The first Evening Panel Discussion titled: *Is there no scope for deep tech semiconductor start-ups in India?* was moderated by Prof. Ramgopal Rao (*BITS Pilani, India*). It gathered the panelists Chandrasekhar Nair (*Bigtec Private Ltd.*), Suryaprakash Konnanuru (*CTO, Ideaspring Capital*), Shantanu Chaturvedi (*VP, Transition VC*), Dipanjan Gope (*CEO, Simyog Technology Private Limited*) who delved into challenges faced by semiconductor start-ups in India and measures to be adopted to overcome them.

Panel Discussion titled: Is there no scope for deep tech semiconductor start-ups in India?

The latter half of the evening was devoted to the poster session I and IEEE Young Professionals Event. 167 posters were displayed for the viewers on day 1 and 2 of the conference, giving the opportunity for the students and researchers to showcase their work and share recent developments.

The IEEE Young Professionals event was attended by over 30 persons. The panel session gathered the speakers: Prof. Francesca Iacopi (FIEEE, Editor-in-Chief, IEEE Trans. Materials for Electron Devices), Early Career awardee, Prof. Shubham Sahay (*IIT Kanpur*), Prof. Avirup Dasgupta (*IIT Rorkee*), Prof. Manan Suri (*IIT Delhi*), Prof. Harshit Agarwal (*IIT Jodhpur*), Prof. Abhronil Sengupta (*Penn State University*) who generously shared their insights and suggestions with young researchers. That will help them advance their research towards real-world applications.

A view at the poster session

Participants of IEEE Young Professionals event with Bin Zhao, EDS President.

Day 2 (5 March)

The second day of the conference commenced with the third plenary talk by **Dr. Balajee Sowrirajan** (*Samsung Electronics, India*) titled: *Semiconductor Systems Driving AI.* It was dedicated to strengthening the globalization of semiconductors and advancing technology for the benefit of humanity. Highlighting the rapid progress of Generative AI in the semiconductor industry, the speaker emphasized its transformative impact and discussed its applications in areas like *TextToText*, *TextToImage*, *ImageToText*, and beyond. He also delved into the rapidly changing landscape of coding, where various tools are gaining momentum.

The fourth plenary talk *From Ferroelectric Materials to Enhanced Semiconductor Devices* was delivered by **Prof. Thomas Mikolajick** (*NaMLab GmbH, Germany*). As a leading figure in the field of ferroelectric memory and devices, he enriched the audience with the 100-year history of ferroelectric memories to its future opportunities and related challenges.

25 parallel sessions consisting of 38 invited talks, 12 keynote, and 62 oral presentations were devoted to the following topics: Gate-All-Around (GAA) Devices, In-Memory Computing I, Cryogenic CMOS Compact Modeling, 2D Materials and Devices II, AI/ML in Process Control, Package Manufacturing, Logic, Memory and 2D Material Reliability, Si; SiGe, III-V Technologies for RF Applications, Alternate Devices and Computing Options, Flash Memories, Ab-initio Simulation and Modeling, Thin Film Devices, Sensors and Biosensors I, Integrated Photonics I, Ga_2O_3-based Power Devices, SOI Devices for RF Applications, Ferroelectric Materials and Devices II, Unconventional Computing I, Design Technology Co-Optimization II, Optoelectronic Devices, Sensors and Biosensors II, Integrated Photonics II, Solar Cells, and GaN HEMTs for RF Applications.

Apart from the poster session, the evening of the second day was reserved for the IEEE WiED event. That interesting session is broadly reported in the EDS Women in Engineering section of this Newsletter issue.

The Evening panel discussion titled: *Is Quantum the new Nano?* had panelists: Manish Chhowala (*University*

From the left: Prof. Nihar Ranjan Mohapatra, Prof. Thomas Mikolajick, Prof. Navakanta Bhat, Dr. Balajee Sowrirajan, and Prof. Yogesh S. Chauhan before the plenary session on the 2nd day of the conference.

The Evening panel discussion: Is Quantum the new Nano?

Participants of the Student Research Forum

of Cambridge, UK), Ritesh Agarwal (*University of Pennsylvania, USA*), Hitoshi Wakabayashi (*Tokyo Institute of Technology, Japan*), Samit Ray (*IIT Kharagpur, India*) and was moderated by Saptarshi Das (*Pennsylvania State University, USA*).

Day 3 (6 March)

Two eminent experts gave plenary talks on the 3rd day of the conference Firstly, **Anand Murthy** (*Intel, USA*) presented the topic *Transistor Scaling for the Future*. As transistor sizes shrink, power density rises, leading to issues such as increased heat generation and power inefficiency. Overcoming the Power Wall is crucial for sustaining advancements in technology and preventing devices from becoming impractical due to excessive energy consumption. Intel Corporation as a leading technology enabler is coming up with a series of innovations to address this challenge for the future. The last plenary talk of the conference was given by **Srinivas Raghvendra** (*Synopsys, USA*) and was titled *Simulation and Analytics in the Angstrom Era*. The speaker emphasized the transition from the nanometer scale to the angstrom one in semiconductors, and how the electronics industry can make the best of it.

15 parallel sessions with 27 invited talks, 5 keynote talks, and 46 oral presentations were held on the 3rd day. They covered the following topics: Design Technology Co-Optimization III, In-Memory Computing II, ML-based Device Modeling, RRAM and OTS Selected Crossbar Arrays, 2D Materials and Devices III, Process and Metrology, Package Design, Printed Devices, GaN-based Power Devices, In-Memory Computing III, Ferroelectric/Memory Modeling, Unconventional Computing II, Magnetic, Straintronic and Quantum Computing Devices, and MEMS Devices.

Student Research Forum (SRF)—To promote and encourage young researchers in the domain of semiconductor devices and circuits, a Student Research Forum (SRF) was also organized during the last day of the conference. This forum helped students interact with the pioneers in their research area and get valuable feedback on their work, where 12 students presented their work through posters.

The conference concluded with the closing remarks and awards ceremony. A vote of thanks was given by Yogesh Singh Chauhan (General Chair, EDTM 2024) and Mayank Shrivastava (General Co-chair, EDTM 2024).

Awards

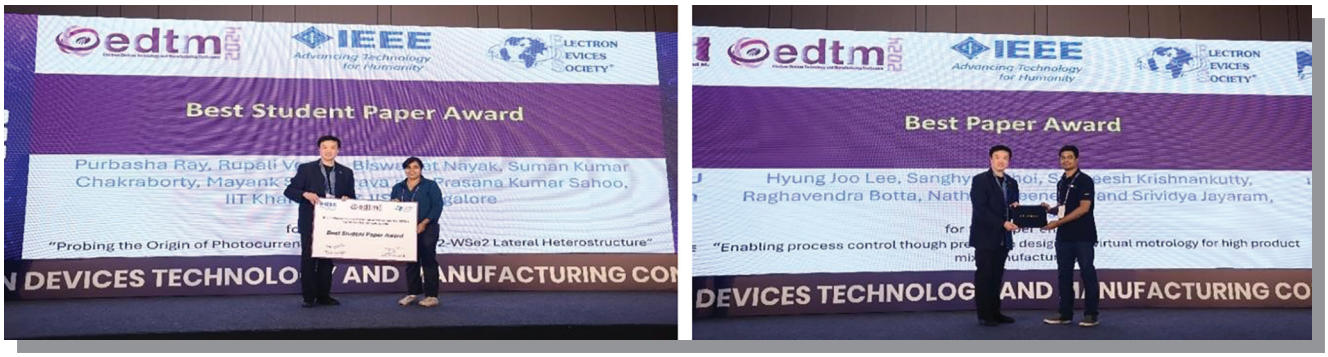
EDTM 2024 recognized outstanding contributions with Best Paper Awards. The awards honoured researchers whose work demonstrated exceptional quality, significance, and impact in the field of electron devices technology and manufacturing. The awards were presented by Bin Zhao, EDS President. Congratulations to the recipients of this prestigious recognitions. Details of the awards are given below:

Best Student Research Forum (SRF) Poster Award:

- Shubham Patil (*IIT Bombay*) for the poster "*Silicon/Germanium-on-Insulator Transistor - Variability, Reliability Characterization, Modelling and Fabrication*"
- Ankita Nandi (*IISc Bangalore*) for the poster "*Advancing Analog Computing through Bias & Process Technology Scalable Analog Standard Cells*"

Best Poster Awards:

- Nitupon Dihingia and Sandip Mondal (*IIT Bombay*) for the poster "*Solution-processed Forming-free ALPO - RRAM based Artificial Synaptic Device with 3 orders of Conductance – Modulation*"
- Aishwarya Singh, Mohit Ganeriwala, and Nihar Mohapatra (*IIT Gandhinagar*) for the poster "*Physics-based Scalable Compact Model for Terminal Charge, Intrinsic Capacitance and Drain Current in Nanosheet FETs*"
- Paromita Bhattacharjee, Parameswar Krishna Iyer, and Harshal Bhalchandra Nemade (*IIT Guwahati*) for the poster "*Real time acoustic convolution of RF signals using organic semiconductor*"
- Linet Thomas C, Nithin B, Bhat K N, Nayak M M, and Navakanta Bhat (*IISc Bangalore*) for the poster "*Fabrication of Miniaturized Pressure Sensors for Invasive Pressure Measurements*"
- Ankan Gayen, Nagarajan Nallusamy, Goutham Ezhilarasu, Shamsul Hasan, Vinoth Subramanian, Kumar Piyush, Arnab Goswami, and Bijoy Krishna Das



Bin Zhao, EDS President presenting the Best Student Paper Award (left) and the Best Paper Award (right).

The EDTM 2024 conference is over; we are looking forward to meeting you at EDTM 2025.

(*IIT Madras*) for the poster "*A Robust and Low-cost Fiber-optic Array Attachment Solution for Silicon Photonics Chips with Large Number of Input/output Channels*"

Best Student Paper Awards:

- Anil Kumar and Sumit Kale (*Delhi Technological University*) for the paper "*Dual-k Reconfigurable Silicon Nanowire Schottky Barrier Transistor for Biosensing Application*"
- Purbasha Ray, Rupali Verma, Biswajeet Nayak, Suman Kumar Chakraborty, Mayank Shrivastava, and Prasana Kumar Sahoo (*IIT Kharagpur & IISc Bangalore*) for the paper "*Probing the Origin of Photocurrent in 2D Bilayer MoSe2-WSe2 Lateral Heterostructure*"
- Shiv Kumar, Arnab Mondal, Anand Pandey, Subhashis Das, and Ankush Bag (*IIT Guwahati*) for the paper "*Exploring Phase and Bandgap Variations in Gallium Oxide Using Mist-based Chemical Vapor Deposition System*"

Best Paper Award:

- Hyung Joo Lee, Sanghyun Choi, Sudheesh Krishnankutty, Raghavendra Botta, Nathan Greeneltch, and Srividya Jayaram (*Siemens*) for the paper "Enabling process control though predictive design and virtual metrology for high product mix manufacturing"

Conclusion: Overall, the IEEE Electron Devices Technology and Manufacturing Conference (EDTM) 2024 was a resounding success, providing a platform for advancing the frontiers of electron devices technology and manufacturing. The conference fostered collaboration, knowledge exchange, and innovation, contributing to the continued growth and evolution of the field. We look forward to future editions of EDTM and the exciting developments they will bring.

The 9th IEEE Electron Devices Technology and Manufacturing (EDTM) Conference, 2025 is scheduled on 9–12 March 2025 at Hong Kong Science and Technology Parks (*HKSTP*) as announced by Shuji Ikeda (*TEI Solutions*).

Yogesh Singh Chauhan (General Chair)
Mayank Shrivastava (General Co-Chair)
Nihar Ranjan Mohapatra (TPC Co-Chair)
Shubham Sahay (Treasurer)

Upcoming Technical Meetings

The 70th annual IEEE International Electron Devices Meeting will be held at the Hilton San Francisco Union Square hotel in San Francisco, CA, December 7–11, 2024.

The paper submission deadline is Thursday, July 11, 23:59 PDT. The late news submission deadline is August 19, 23:59 PDT. Accepted papers will be published as-is in the proceedings.

For more information, see https://www.ieee-iedm.org/ and the EDS Newsletter issue of July 2024.

IEDM 70th International Electron Devices Meeting

36th International Symposium on Power Semiconductor Devices and ICs (ISPSD) 2024 in Bremen

The 36th International Symposium on Power Semiconductor Devices and ICs is scheduled to be held in Bremen, Germany, on 2–6 June 2024.

ISPSD is the premier forum for technical discussion in all areas of power semiconductor devices, power integrated circuits, their hybrid technologies, and applications. With an attendance of more than 500 engineers, scientists, and students last year in Hong Kong, it is firmly established as the must-attend conference for the power semiconductor industry reflecting the growing importance of power electronics in modern society.

ISPSD 2024 will be held in the historical city center of the Free Hanseatic City of Bremen, which includes St. Peter's cathedral, the origin of the city, and the UNESCO World Heritage Site, consisting of the historic city hall and the statue of knight Roland. Bremen is the vibrant heart

of north-western Germany and a major cultural and economic hub. Its charm, traditions, historical treasures, and arts will give this conference a unique atmosphere.

The ISPSD captures all areas of power semiconductor devices and power integrated circuits, such as low and high-voltage devices and circuits, all semiconductor materials including Si, SiC, GaN, Ga_2O_3, diamond, and power semiconductor packaging. The conference offers an attractive short course program on Sunday covering important topics like advanced SiC devices and materials, their robustness and reliability, driver concepts and system topologies, wide band-gap (WBG) devices, power IC design in GaN, and multi-dimensional architectures for WBG devices.

The main conference will be held Monday through Thursday starting with plenary talks on trends and challenges for the power semiconductor industry followed by talks and poster sessions organised along the following tracks:

- **High Voltage Power Devices:** High voltage silicon-based discrete devices (>200 V) such as super junction MOSFETs, IGBTs, thyristors, GTOs, and pn-diodes
- **Low Voltage Power Devices and Power IC Technology:** Low voltage silicon-based discrete power devices (≤ 200 V) and power devices for power ICs of all voltage ranges
- **Power IC Design:** Circuit design and demonstration using power IC technology platform
- **GaN and III/V Compound Materials:** GaN and other III/V compound material (e.g. AlN, GaAs) based power devices, technology and integration, materials, and processing
- **SiC and Other Materials:** SiC and other material (e.g. Ga_2O_3, diamond) based power devices, technology and integration, materials, and processing
- **Module and Package Technologies:** Package technology for modules, discrete power devices, and power ICs

Session topics include Ruggedness & Advanced Drive of SiC, Novel GaN Power Devices and Technologies, and Low Voltage Power Devices and Power ICs, to name a few. The conference is organised in non-paralleled sessions allowing the attendees to listen to all fields of power semiconductors enabling new views beyond their own field of research.

A regular registration is possible until the last day of the conference. Further information can be found on the conference homepage www.ispsd2024.com

The ISPSD is organized by Prof. Nando Kaminski (General Chair, University of Bremen, Germany), and Prof. Ulrike Grossner (Technical Program Chair, ETH Zurich, Switzerland). Prof. Florin Udrea (Short Course Chair, University of Cambridge, United Kingdom) and Pavla Hlinková (Local Arrangements Chair, Guarant International, Czech Republic). The conference is technically co-sponsored by IEEE and its societies EDS and PELS, as well as by ECPE, VDE-ETG, and IEEJ.

Nando Kaminski
General Chair of ISPSD 2024

INTERNATIONAL INTERCONNECT TECHNOLOGY CONFERENCE

IEEE IITC 2024 Electron Devices Society

JUNE 3-6 | SAN JOSE, CALIFORNIA

The 27th edition of the International Interconnect Technology Conference (IITC) will be held on 3–6 June 2024 in San Jose, California. IITC is sponsored by the IEEE Electron Devices Society as the premier conference for interconnect technology devoted to leading-edge research in the field of advanced metallization and 3D integration for ULSI IC applications. The conference promotes presentations and discussions on all aspects of BEOL/MOL interconnects and metallization, including design, unit process, integration, and reliability.

Applications of Interest

- Advanced interconnects: low-k interconnects, optical, wireless, and carbon-based interconnects, Airgap, 1D/2D interconnects, beyond Cu…
- Emerging BEOL Integration flows such as semi-damascene
- 3D integration & packaging concerns: Wafer-to-Wafer/Chip-to-Wafer bonding, RDL's and Interposers, Through Si Via, Non-destructive, high throughput methods to identify defects, backside power distribution network (BSPDN), thermal management

- Contacts on MOS devices: Silicide, III-V, 2D materials…
- Memory architecture: CBRAM, PCRAM, ReRAM, MRAM, FeRAM, DRAM, 3DNAND…
- Novel System and Emerging Technology: Energy harvesting, brain-inspired computing…
- Novel Form Factors: flexible electronics, wearables…

Topics of Interest

- Process integration, advanced patterning for MOL/BEOL
- Materials and Unit Processes (Dielectrics, metals, barriers, Wet, CMP, PVD, CVD, ALD, selective deposition/SAMs, patterning, advanced cleaning and surface treatment)
- Reliability and Failure analysis, characterization, techniques, and methods
- Advanced material/process characterization, system-technology & design-technology co-optimization, and modeling techniques

Keynote Speakers

Dr. James A. O'Neill Senior VP and CTO of Entegris
"Materials Challenges for the Semiconductor Industry"

Dr. Huiming Bu Vice President, Global Semiconductor R&D and Albany Operations, IBM Research
"Technology Innovations to Fuel 1T Transistors"

Dr. Nirmal Ramaswamy Vice President, Advanced DRAM and Emerging Memory Technology, Micron Technology Inc.
"Memory Technology: Status and Scaling Perspective"

The conference will include a workshop titled **"New dimensions to harness, upside & backside; What to consider and how to control?"** This workshop will discuss the key challenges in the 3D integration of devices, as described in the synopsis below.

As the conventional planar scaling of CMOS devices reaches its limits, new directions are being pursued in the vertical dimension to achieve better power, performance, and area (PPA). This shift began with the development of device architectures such as FinFETs, Nanosheets, VTFETs, and StackFETs, which extend or stack up the transistor channels in vertical direction. The trend is now expanding to the interconnect/BEOL domain, where the backside of the wafer (BSPDN) and the vertical stacking of semiconductor dies (HBM) are being explored. These vertical integration techniques enable new possibilities for chip design and packaging that can improve PPA. However, they also pose new difficulties in various aspects such as wafer distortion, metrology, defect control, heat management, and reliability. These difficulties must be addressed to ensure the quality and functionality of the devices with novel structures. One of the critical areas that requires more attention is the wafer bonding and thinning process, which affects the lithography process on the wafer backside. Another significant challenge is the heat removal of the bonded wafers that lack the Si substrate. In this workshop, experts from both industry and academia will present and discuss in detail the key technical challenges associated with the 3-dimensional integration of devices, so that the audience can gain more knowledge and insights on this new and important industry trend. The workshop will include the following talks:

Welcome and Introduction
By Kisik Choi, IBM Research

BSPDN design considerations for advanced logic device
By Stanely S.C. Song, Google

Delivering Power and Removing Heat; Two challenges that could become the Achilles heel for AI Applications
By Madhavan Swaminathan, Penn State University

Advanced packaging solutions for high performance memory
By Kunal Parekh, Micron

Wafer bonding hybrid/fusion bonding
By Ilseok Son, TEL

Backside patterning from lithography perspective: alignment, metrology, and overlay control
By Michael Kubis, ASML

Wafer warpage control by film deposition
By Fayaz Shaikh, LAM Research

We are looking forward to meeting you at the 27th IITC.

Zhihong Chen—General Chair
Mansour Moinpour—Program Chair
Nick Lanzillo—Program Co-Chair

The European Flagship Conference ESSERC 2024
The Next Circuits for a Better Life

The first European Solid-State Device Research Conference (ESSDERC) conference was organized in 1971 in Munich, Germany, aiming to present the latest developments in physics, technology, and characterization of solid-state devices and bringing together both the academic world and the industry active on silicon and compound semiconductor integrated circuits. The sister conference, the European Solid-State Circuits Conference (ESSCIRC) started in 1975 and focused on recent advances in design concepts, design methodologies, circuit simulation, and solid-state circuits.

Since 2002 both conferences have been organised at the same time and in the same location. However, since the last decade, there has been a worldwide trend towards education, academic research, and industrial development while strengthening the link between device technology and circuit design. This is due to the world becoming more and more application-driven, with a need to start from the system level and to work down to circuit design and device technology. The level of integration for system-on-chip design is rapidly increasing. This is made available by advances in semiconductor technology. Designers and technologists must closely collaborate, and both disciplines and skills have to go hand in hand to achieve optimal results. Therefore, the Steering Committee decided to reorganize the conferences into a single conference format under a new name, i.e., "European Solid State Electronic Research Conference – ESSERC". The aim is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits. The first ESSERC conference will take place on 9–11 September 2024, in Bruges Belgium. The conference is organized by KU Leuven, Belgium and sponsored by IEEE Electron Devices Society (EDS), IEEE Solid-State Circuits Society (SSCS), and IEEE Circuits and Systems Society (CAS).

The following tracks will be covered:

- **Advanced Technology, Process, and Materials**: Process and material developments for logic, memory, and non-CMOS, including electrical and physico-chemical characterization, process integration, and manufacturing: 2D TMDs and related insulators (e.g., hBN), graphene, TFTs, gate oxide, gate material, silicide, MOL and BEOL materials, 3D monolithic as well as conventional and novel memory cells including charge-based memories, ReRAM, MRAM, PCRAM, ferroelectrics, crosspoint and selectors, organic memories.
- **Analog, Power, and RF Devices**: From material growth to device, components, and systems (process, design, device fabrication, applications); Device design and electrical/ physical/electro-thermal/reliability characterization of devices based on Si RF CMOS, RF SOI, SiGe HBTs, SiC, InP/InGaAs/GaAs, AlGaN/InGaN/GaN, CNT, diamond, and related material systems; Power systems integration issues including thermal management, packaging technologies, system-level electro-thermal characterization, product quality, and system reliability aspects; Device production processes and design for manufacturability.
- **Compact Modeling and Process/Device Simulation**: TCAD and advanced simulation techniques and studies; Compact/SPICE modeling of electronic, optical, organic, emerging, and hybrid devices and their

IC implementation and interconnection; Verilog-A models of semiconductor devices (including bio/med sensors, MEMS, microwave, RF, high voltage and power, emerging technologies, and novel devices); Parameter extraction, reliability and variability, performance evaluation, and open-source benchmarking/implementation methodologies; Modeling of interactions between process, device, and circuit design, design/technology co-optimization, and foundry/fabless interface strategies; Numerical, analytical, statistical modeling and simulation of electronic, optical, and hybrid devices, interconnects, isolation, and 2D/3D integration; Simulations of material properties and fabrication processes; Advanced physical phenomena (quantum mechanical and non-stationary transport phenomena, ballistic transport); Mechanical and/or electro-thermal modeling and simulation; Simulations of reliability aspects of materials and devices.

- **Analog Circuits**: Building blocks, systems, and techniques operating in the analog or mixed-signal domain, such as amplifiers, drivers, comparators, filters, references, analog systems, analog interfaces, and analog techniques.
- **Data Converters**: Nyquist-rate and oversampling A/D and D/A converters. Capacitance-to-digital, time-to-digital, frequency-to-digital converters. Embedded and application-specific A/D and D/A converters; Analog-to-information conversion; A/D and D/A converter building blocks (sample-and-hold circuits, calibration circuits); Enabling new techniques, architectures, or technologies.
- **RF and mm-Wave Circuits**: Building blocks, and front-ends operating at RF, mm-Wave and THz frequencies for wireless communication, radar, sensing, and imaging.
- **Frequency Generation Circuits**: Oscillators and controlled oscillators, PLL, DLL, injection-locked oscillators, frequency dividers, any kind of frequency generation, or time base circuits and systems.
- **Digital Circuits and Systems**: Digital circuits and memory subsystems for microprocessors, micro-controllers, application processors, and graphics processors; Digital systems for communications, video, multimedia, security, and cryptography applications; Digital design techniques for power reduction, intra-chip communication, clock distribution, soft-error, and variation-tolerant design, and system-level integration; Devices and circuits for IoT and IoE security (e.g., PUFs, TRNGs).
- **Power Management**: Power management and control circuits: Regulators; Switched mode power converter ICs using inductive, capacitive, and hybrid techniques; Energy harvesting circuits and systems; Wide-bandgap topologies and gate-drivers; Power and signal isolators; Robust power management circuits for automotive and other harsh environments; Circuits for lighting, wireless power, and envelope modulators; Design for manufacturability.
- **Wireless Systems**: Radio transceivers, highly integrated front-ends, SoCs, and SiPs, including heterogeneous packaging solutions, at RF, mm-Wave or THz frequencies, for established or future standards, as well as novel applications such as radar, sensing, and imaging.
- **Wireline and Optical Circuits and Systems**: 2.5/3D interconnect, copper-cable links and equalizing on-chip links, exploratory I/O circuits for advancing data rates, chip-to-chip system communications, high-speed serial interfaces, optical interfaces, laser drivers, optical receivers, clock and data recovery.
- **Emerging Computing Devices and Circuits**: Novel devices and circuits to improve existing and enable new computing paradigms; In-memory computing and logic-in-memory using emerging devices; Qubit devices and cryogenic circuits for quantum computing; Non-charge-based logic devices and circuits (magnetic logic, spintronics, and plasmonics), beyond CMOS transistors (tunnel FETs, Dirac-source FETs); Devices and circuits based on low-dimensional systems (2D materials, nanowires etc.), topological insulators, and phase transitions.
- **Architectures and Circuits for AI and ML**: Silicon implementations of AI, ML, neuromorphic accelerators, and processors, together with their applications; Edge and cloud AI computing platforms; In- and near-memory computing at the array/processor-level using commercially available technologies.
- **Devices & Circuits for Sensors, Imagers, and Displays**: Devices and circuits based on MEMS and bio-electronics, devices for biomedical and imaging applications; Image sensors and related circuits and systems, SoCs; Automotive, LIDAR, and ultrasonic sensors for ADAS, autonomous driving, smart mobility; MEMS sensor systems; Wearable, implantable, ingestible electronics, biomedical SoCs, neural interfaces and closed-loop systems; Biosensors, microarrays, and lab-on-a-chip; Display electronics, displays with sensing functionality; Devices, circuits, and systems for AR/VR and related sensing/actuation; Product quality and reliability aspects; Device and circuits production processes and design for manufacturability.

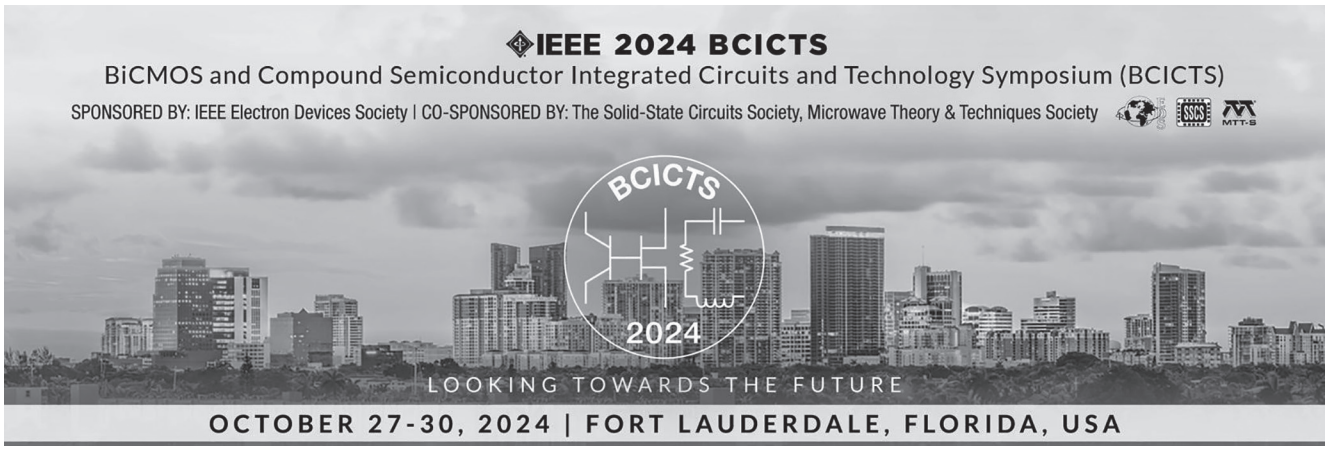
The deadline for paper submission is **5 April 2024**.

Bruges is a place that lives and breathes history. Visiting this historic city means traveling back in time to the Middle Ages. It is both magical and authentic. Brugge in medieval times was known as a commercial metropolis in the heart of Europe. Bruges is one of Europe's best-preserved cities, evidenced by the fact that its historic city centre has been designated a UNESCO world heritage site. The iconic spires of its cathedral and bell tower, its cobbled streets, winding canals, and whitewashed façades are almost painfully picturesque.

In the 15th century, Brugge was the cradle of the Flemish Primitives and a centre of patronage and painting development for artists such as Jan van Eyck and Hans Memling. Many of their works were exported and influenced painting styles all over Europe. Exceptionally important collections have remained in the city until today. Travelers from all over the world are coming to Belgium to visit Bruges.

The conference will be held in the Bruges Meeting & Convention Centre (BMCC). Full details can be found on the website www.esserc2024.org.

Patrick Reynaert, General Chair Technical Program Committee
Cor Claeys, Chair Local Arrangements and Executive Secretary Steering Committee



The 2024 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS) will be taking place in Fort Lauderdale, Florida on 27–30 October, and is the 7th edition of the successful merger between the original Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) and the Compound Semiconductor Integrated Circuit Symposium (CSICS). BCICTS is the premier forum for the presentation and discussion of the latest developments in bipolar, BiCMOS, and compound semiconductor circuits, devices, and technologies. Coverage includes all aspects of these technologies, including materials, device fabrication, device phenomena, TCAD modeling, compact modeling, integrated circuit design, testing, and system applications. A wide range of integrated circuit technologies are covered, including bipolar and field-effect transistors manufactured using materials such as Si, SiGe, GaAs, GaN, InP, and SiC. The latest results in wireless, analog, RF, microwave, high-speed digital, mixed signal, optoelectronic, millimeter wave, and THz integrated circuits are embraced.

The conference itself will take place at W Fort Lauderdale hotel, Fort Lauderdale, Florida. Fort Lauderdale, known for its beautiful beaches and vibrant culture, offers a variety of interesting sites including Fort Lauderdale Beaches for plenteous water activities, Las Olas Boulevard for popular shopping and dining, and Bonnet House Museum and Gardens for exploring historic estate with beautiful gardens.

The Technical Program Committee for BCICTS cordially invites you to submit papers. **The submission deadline is May 10, 2024**. Submissions are encouraged in all areas of advanced circuits, devices, and modeling, with particular emphasis on:

- Bipolar/BiCMOS devices, circuits, and technologies
- 5G/6G, satellite communication ICs
- GaN HPAs/LNAs, InP THz PAs
- High-performance RF switch technologies
- GaN HEMT and other wide bandgap power devices
- Analog, RF, and microwave ICs
- mmW and THz ICs
- Process and device technology
- Modeling/simulation
- Optical CMOS/SiGe transceivers
- High-speed digital, mixed signal, and electro-optic ICs
- Cryogenic devices and circuits

Extended versions of selected papers from the Symposium will be invited for publication in the September 2025 issue of the IEEE Journal of Solid-State Circuits. The BCICTS will be also offering short course, primer course, vendor exhibition, and plenary/invited talks given by internationally renowned experts in their field. For more details, please visit the BCICTS website at www.bcicts.org.

The BCICTS Committee members look forward to seeing you at 2024 IEEE BCICTS in Fort Lauderdale!

2024 IEEE BCICTS Organizing Committee
Munehiko Nagatani, BCICTS Publicity Chair

Society News

Message from the IEEE EDS President

Bin Zhao
EDS President
2024–2025

Dear EDS Colleagues and Friends,

As we stride into 2024, I extend my warmest greetings to each of you, hoping this message finds you in good health and spirits. This year brings a wave of new energy as we welcome fresh faces into our EDS teams, eager to contribute to our shared vision.

Looking back, we find ourselves standing on the shoulders of giants, marveling at the brilliant history that EDS has carved out in the evolution of modern electronics. From groundbreaking semiconductor devices and technologies to transformative advancements in high-performance computing, artificial intelligence, and the boundless potential of the Metaverse, the technical fields of EDS have been the foundation of them all.

As we cast our gaze towards the horizon, we are confronted with a landscape characterized by both boundless opportunities and formidable challenges. Amid the continued digital transformation era, it is incumbent upon us to fortify our ranks, engage a diverse array of volunteers, and strengthen our activities in critical areas to ensure the sustained success of EDS.

Technical activities serve as the lifeblood of EDS, driving our growth and enabling us to achieve our goals and mission. To enhance inclusivity and coverage, we have renamed the position of Vice President of Technical Committees to Vice President of Technical Activities, reflecting the broader responsibility encompassing all technical endeavors in EDS. Furthermore, we have revised EDS governance to permit the appointment of up to three Vice Presidents of Technical Activities. This year, we restructured our Technical Committees (TCs) into three groups (Mainstream, Interdisciplinary, and New Initiatives) and appointed and assigned one Vice President of Technical Activities to work with each group. This restructuring aims to foster improved leadership, initiation, execution, and coordination in EDS Technical Activities.

We charge our technical activities with a renewed focus on leading, advancing, pathfinding, and pioneering work, supported by a clearly defined mission and vision. We are committed to fostering a culture of collaboration, innovation, and excellence in EDS TCs. Through strategic initiatives, collaborative projects, and knowledge-sharing in leading-edge technologies, we aim to harness the collective expertise and passion of our volunteers and members to address pressing challenges and explore new frontiers in electron devices and technologies.

As part of our commitment to fostering leadership and providing equitable opportunities, we have implemented an open nomination process for the appointment of Technical Committee Chairs. This inclusive approach helps us to tap into the diverse expertise and perspectives in EDS, ensuring that our technical activities are driven by the best and brightest minds in the field. Additionally, we are allocating dedicated funding to support EDS technical activities, enabling our TCs to pursue ambitious goals, build communities and forums for leading-edge R&D, and make impactful contributions to the advancement of electron devices and technologies.

All these strategic moves aim to bolster our capacity to navigate the ever-changing technological landscape with agility and foresight and to ensure that EDS remains at the forefront of technological advancement.

In our pursuit of a more inclusive, capable, and dynamic organization, we conducted a thorough review and finalized revisions to the term limits for volunteer positions. Recognizing the challenges posed by rigid term constraints, such as the previous imposition of two terms in a lifetime for all volunteer positions, we acknowledge the need to strike a delicate balance between continuity and rejuvenation within our volunteer and leadership ranks.

By considering the candidate pool and the typical number of candidates for each position, as detailed in the revised EDS Constitution and Bylaws, we have classified volunteer positions into three distinct categories. Each category is tailored with a term limit to suit the diverse needs and aspirations of our society, as outlined below. Additionally, in some cases, term limits are determined by IEEE policies and/or agreements with other non-EDS organizations.

Category 1: two-term limit in a lifetime.

- 2 years per term: Vice Presidents, Committee Chairs
- 3 years per term: Editor-in-Chief of EDS Publications, Members of EDS Board of Governors

Category 2: two-term limit with a reset by rotating out for at least one year, 2 years per term.

- Committee Members, SRC Chairs and Vice Chairs
- EDS Representatives to Joint Publications, EDS Representatives to Other Organizations
- Treasurer, Secretary
- Chairs and Members of Technical Committees

Category 3: special cases.

- Editors of EDS Journals: 3 years per term, three-term limit in a lifetime

- Editors of EDS Newsletter or ED Magazine: 3 years per term, three-term limit with a reset by rotating out for at least one year

These revisions in EDS volunteer position term limits broaden opportunities, allowing many willing, capable, and influential volunteers to participate and contribute throughout their professional careers. They ensure continuity while also making space for new volunteers, aligning our policies with the evolving needs of EDS. Overall, this initiative fosters inclusivity, dynamism, and representation within the organization, paving the way for a more vibrant and engaged EDS.

As EDS continues to expand its footprint and influence in the global technical community, the demand for resources and support is rapidly growing. In addition to the term limit revisions, we are also exploring avenues to create more volunteer positions to address the evolving needs and priorities of our society. From membership engagement and social media management to conference organization and fundraising initiatives, these volunteer roles are pivotal in ensuring the scalability and sustainability of EDS's operations. By fostering a culture of collaboration, innovation, efficiency, and effectiveness, we aim to optimize our collective efforts and drive impactful progress in the field of electron devices and technologies.

The future of EDS shines brightly, filled with innovation, collaboration, and boundless opportunities. As we navigate challenges and seize opportunities ahead, I invite each of you to join us on this exciting journey of growth and discovery.

Thank you for your unwavering dedication and support to the IEEE Electron Devices Society.

Bin Zhao
IEEE EDS President

Announcement of Newly Elected Officers & BoG Members

Cary Y. Yang
2023 EDS Nominations and Elections Chair

The Electron Devices Society (EDS) Officers and Board of Governors (BoG) members-at-large election was held in December 2023. I am pleased to present the results of this election and short biographical information of the incoming team that will lead EDS in the years to come.

Officers

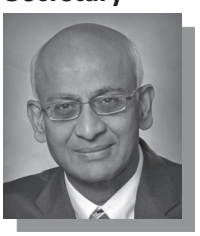
The following volunteers were elected as Officers beginning 1/1/2024:

President-Elect

Arokia Nathan

Arokia Nathan is a leading pioneer in the development and application of thin film transistor technologies to flexible electronics, display and sensor systems, and mm-Wave radios on glass. Following his PhD in Electrical Engineering, University of Alberta, Canada in 1988, he joined LSI Logic USA and subsequently the Institute of Quantum Electronics, ETH Zürich, Switzerland, before joining the Electrical and Computer Engineering Department, University of Waterloo, Canada. In 2006, he joined the London Centre for Nanotechnology, University College London as the Sumitomo Chair of Nanotechnology. He moved to Cambridge University in 2011 as the Chair of Photonic Systems and Displays, and he is currently a Bye-Fellow and Tutor at Darwin College. He has over 600 publications including 6 books, more than 150 patents, and four spin-off companies. He is a Fellow of IEEE, a Distinguished Lecturer of the IEEE Electron Devices Society and Sensor Council, a Chartered Engineer (UK), Fellow of the Institution of Engineering and Technology (UK), Fellow of the Royal Academy of Engineering, Fellow of the Canadian Academy of Engineering, Fellow of the Society for Information Displays, and winner of the 2020 IEEE EDS JJ Ebers Award.

Secretary



Murty Polavarapu

Murty Polavarapu is engaged in developing advanced semiconductor memory and logic products for defense and aerospace markets, especially for space applications. He also serves as the Managing Director of Virginia Microelectronics Consortium. His career includes management and technical leadership roles at various companies including BAE Systems, IBM, Lockheed Martin, Micron, and Toshiba. Murty Polavarapu has served the EDS community in many capacities including Chapter Chair, Regional Editor for the Newsletter, SRC Chair, Member of Board of Governors, and most recently Vice President for Regions and Chapters. He is also currently the MGA Vice Chair for Geographic Activities. He is based in the Washington, DC area.

Treasurer

Roger Booth

Roger Booth received a PhD in Electrical Engineering from Michigan State University and is a Senior Member of IEEE. He works for Qualcomm, and his career has included time at IBM, TowerJazz, and Booz Allen Hamilton (at DARPA). He has spent most of his career working on RF/Analog CMOS processes but has experience with SOI, SiGe, and high-power RF processes.

BOG Members-at-Large

A total of eight members were elected for a three-year term (2024–2026). Four of the eight electees whose names are followed by * are serving a second term, while the other four have joined the board for the first time. The backgrounds of the electees span a wide range of professional and technical interests. The following are the results of this election and brief biographies of the individuals elected.

Harshit Agarwal

Harshit Agarwal is working as Associate Professor, Dept. of Electrical Engineering, Indian Institute of Technology (IIT) Jodhpur, India. Before moving to academia, he served as BSIM program manager cum Center Manager, Berkeley Device Modeling Center (BDMC) at UC Berkeley (2016–2020). He has more than 10 years of experience in industry-standard compact model research and development, model quality assurance, circuit simulations, and device-circuit co-design. His research interest is on emerging devices for logic, analog, RF, memories, high power and voltage devices and circuits. He is a recipient of 2020 IEEE EDS Early Career Award and 2022 Young Researcher Award, IIT Jodhpur. He served as a member of IEEE EDS Technical Committee on Compact Modeling, a founding member of IEEE EDS student branch chapter, and guest editor of IEEE TED special issue on compact modeling. He has published more than 50 research articles in journals and conferences of international repute (IEDM, IEEE-EDL, IEEE TED etc.) and has delivered talks on compact modeling in reputed modeling workshops and meetings.

Luisa Petti

Luisa Petti received her BSc. and M.Sc. in Electronic Engineering from Politecnico di Milano (Italy) in 2009 and 2011, respectively. She obtained her Ph.D. in Electrical Engineering from ETH Zurich (Switzerland) in 2016 with a thesis entitled "Metal oxide semiconductor thin-film transistors for flexible electronics", for which she won the ETH medal. After a short post-doc at ETH Zurich, she joined first Cambridge Display Technology Ltd in October 2016 and then FlexEnable Ltd in December 2017 in Cambridge, UK as a Scientist. In 2018 she joined the Free University of Bozen-Bolzano, where she has been Associate Professor in Electronics since March 2021. Luisa's current research includes the design, fabrication, and characterization of flexible and printable sensors, energy harvesters, and thin-film devices and circuits. At the Free University of Bolzano, Luisa is heading the Sensor System Technology Lab at NOI Techpark, while also being member of the competence center for plant health and directing the B.Sc. in Electronics and Cyber-Physical Systems Engineering.

She is IEEE senior member, member of EDS Flexible Electronics and Display TC, EDS Women in EDS committee, EDS Meetings committee, CRFID Additively Manufactured Electronics Systems TC, IES MEMS and Nanotechnologies TC, CAS special interest group on Electronics for Agri-food. Luisa is co-chair of IEEE IFETC 2024, technical co-chair of IEEE CAFE 2024, IFETC 2023 and IFETC 2021, TPC member of IEEE conferences CAFE 2023, FLEPS 2023, EDTM 2021, 2022, 2024. She is also associate editor-in-chief of IEEE J-FLEX, and associate editor of IEEE TAFE. She is author of 2 patent applications (1 granted) and >150 scientific peer-reviewed publications. Luisa is recipient of the 2019 IEEE EDS Early Career Award.

Xiaojun Guo

Xiaojun Guo* is currently a Professor with Department of Electronic Engineering, Shanghai Jiao Tong University, Shanghai, China. He leads the Printed Electronics and Flexible Integration (pEFi) research lab, working on core device technologies (transistors, sensors, displays), hybrid transistor circuit design, heterogeneous integration architectures, and disruptive manufacturing approaches towards making friendly "human-machine-environment" interface electronics, as the base for future sustainable and intelligent society of "internet of everything". Dr. Guo has authored more than 70 technical papers in international journals, and given more than 20 invited talks in international conferences organized by IEEE/SID/ECS/SPIE societies. He serves as Senior Editor of Flexible and Printed Electronics, Associate Editor of IEEE J-EDS and TED, Member of Active Matrix Devices Sub-committee of the SID, Expert of IEC Technical Committee No. 119: Printed Electronics, and Chair of IEEE Electron Device Society Flexible Electronics and Displays Technical Committee (2016 – 2019). He is actively organizing IEEE IFETC and CAD-TFT conferences.

Francesca Iacopi

Francesca Iacopi* (MSc La Sapienza University, Rome, Italy; PhD KULeuven, Belgium) is an IEEE Fellow with over 20 years' industrial and academic research expertise in semiconductor technologies, with 170 peer-reviewed publications and 10 granted US patents, spanning interconnects, CMOS devices and packaging. Research Scientist at IMEC (Belgium) over 1999–2009, she then took up a year's Guest Professorship at the University of Tokyo (Japan). In 2010–2011 she directed the Chip-Package Interaction strategy for GLOBALFOUNDRIES (CA, USA). Having worked on 4 continents, she currently leads the Integrated Nanosystems Lab, in the Faculty of Engineering and IT, University of Technology Sydney, Australia. Her research focuses on the translation of basic scientific advances in nanomaterials and novel device concepts into implementable integrated technologies. She is known for her seminal work on the integration of porous dielectrics in on-chip interconnects, and for the invention of a direct and selective process for the wafer-scale synthesis of graphene on silicon, with applications in integrated microtechnologies, including nanophotonics, neural electrodes, and energy storage. She was recipient of an MRS Gold Graduate Student Award (2003), an Australian Research Council Future Fellowship (2012), a Global Innovation Award in Washington DC (2014), and was listed among the most innovative engineers by Engineers Australia (2018). Francesca is an IEEE EDS Distinguished Lecturer and serves regularly on technical and strategic committees for IEEE and the Materials Research Society. She serves on the Editorial Advisory Board for the IEEE The Institute magazine, and she is the inaugural Editor-in-Chief of the IEEE Trans. on Materials for Electron Devices (IEEE T-MAT), to launch in 2024.

Meikei Ieong

Meikei Ieong* is currently chair of the IEEE EDS Special Projects Oversight Committee and member of the EDS BoG. He has been an active member of the IEEE EDS, serving on the committee of publications and conferences, including General chair of IEDM. Meikei is also founding chairman of Semiconductor Nanotechnology Alliance (SNA). He held various leadership positions in Taiwan Semiconductor Manufacturing Company and IBM Research. Meikei holds a PhD degree in Electrical and Computer Engineering from the University of Massachusetts, Amherst and a MBA degree from the MIT Sloan Fellows Program at the MIT School of Management. He has published more than 130 papers in journals and conference proceedings and more than 120 patents and received more than 15,000 citations (h-index:66, i10-index:142).

Andreas Kerber

Andreas Kerber received his Diploma in physics from the University of Innsbruck, Austria, in 2001, and a PhD in electrical engineering from TU-Darmstadt, Germany, with honors in 2004. From 1999 to 2000 he was an intern at Bell Labs. From 2001 to 2003, he was the Infineon Technologies assignee to International SEMATECH at IMEC in Leuven, Belgium. From 2004 to 2006, he was with the Reliability Methodology Department at Infineon Technologies in Munich, Germany. From 2006 to 2018 he was working for AMD and GLOBALFOUNDRIES in NY as a Principal Member of Technical Staff on front-end-of-line (FEOL) reliability research with focus on metal gate / high-k CMOS process technology, advanced transistor architecture and device-to-circuit reliability correlation. From 2018 to 2019 he was with Skorpios Technologies in Albuquerque, NM, working on reliability of Si-photonic devices. From 2019 to 2021, he was with ON-Semiconductor in Santa Clara, CA working on product quality management of CMOS image sensors. Since 2021 he has been with Intel in Santa Clara, CA working on CMOS reliability for Logic technologies. Dr. Kerber has contributed to more than 115 journal and conference publications. He presented his work and gave tutorials at various conferences including VLSI, IEDM and IRPS. Dr. Kerber is a Senior Member of the IEEE and a Distinguished Lecturer (DL) for the IEEE Electron Devices Society.

P. Susthitha Menon

P. Susthitha Menon* is currently an Associate Professor at the Institute of Microengineering and Nanoelectronics (IMEN), Universiti Kebangsaan Malaysia (UKM), and the IMEN-UKM Coordinator for Alumni Engagement. She received her BEng (Hons) degree from UKM in 1999. As an Intel scholar, she worked at Intel Malaysia as a Product Engineer for mobile modules systems from 1999 to 2002. She then received her MSc and PhD (Distinction) degrees in 2005 and 2008 respectively from UKM, for the development of Si- and InGaAs-based interdigitated p-i-n photodiodes. At IMEN, she specializes in the fields of plasmonics, optoelectronics, nanophotonics, and robust engineering optimization. Dr. Menon is a Senior Member of IEEE, OSA, and SPIE. She is a member of IEEE Electron Devices Society (EDS) Board of Governors (BoG) 2021–2026, the Chair of the IEEE Women in EDS committee 2022–2025, and is the Past Chair of the IEEE EDS Malaysia Chapter 2017–2018 which during her tenure as Chair, won the IEEE EDS R10 Best Chapter Award in 2018 as well as the IEEE Malaysia Section's Best Chapter Award in 2017 and 2018 respectively. Dr. Menon is also the recipient of the IEEE Malaysia Section's Outstanding Women in Engineering Award 2022.

Camilo Velez

Camilo Velez is an Assistant Professor in the Department of Mechanical and Aerospace Engineering at University of California, Irvine. He created the Laboratory called: "Magnetic Microsystems & Microrobotics". His research interests include micro/nano robotics, microfabrication of magnetic devices, MEMS, TFTs, and microfluidics. He conducted postdoctoral research at Carnegie Mellon University in the Microrobotics Lab and at the Interdisciplinary Microsystems Group at University of Florida (UF). He received his Ph.D. and M.Sc. in electrical and computer engineering at UF, a M.Eng. at Universidad de los Andes-Colombia, and his B.S. in Electronic Engineering at Pontificia Universidad Javeriana-Colombia. He was awarded an Engineering Award for Creativity at UF, honorable mention for excellence in research in his B.S., and won two best poster awards. He currently serves on the board of Governors of Electron Devices Society at IEEE. Committees EDS: Young Professionals (Chair), Microelectromechanical Systems. IEEE-RAS: Micro/Nano Robotics and Automation. His research is currently sponsored by Meta, Army Research Lab USA, and National Science Foundation USA.

Cary Yang
2023 EDS Nominations and Elections Chair

EDS Newsletter New Direction Ad Hoc Committee

M K Radhakrishnan

The EDS Newsletter, an essential publication of the Society for the past 30 years, has been the vehicle to convey the Society news to its members, to highlight members' contributions to our community, as well as to acknowledge members' accomplishments and recognitions for broader visibility. Originally a quarterly leaflet, it has evolved into a comprehensive publication on the Society, featuring conference summaries, technical briefs, Chapter activities, Women in Electron Devices, and Young Professionals. The recent introduction of Electron Devices Magazine has prompted us an opportunity to take a comprehensive review of the current Newsletter and how it could be better positioned to serve our members. With this in view, the EDS President, Bin Zhao, has formed the EDS Newsletter New Direction Ad Hoc Committee chaired by M.K. Radhakrishnan. The Committee members include Karim S Karim, Joao Antonio Martino, Murty Polavarapu, Samar Saha, Manoj Saxena, Jonathan Terry, and Daniel Tomaszewski. This Committee aims to craft a unique value proposition for the Newsletter to distinguish it within the EDS community, offering content and features that set it apart. It will also recommend actions to position the Newsletter as a valuable resource and communication tool, complementing existing publications while catering to the diverse interests and preferences of our community. The Committee will explore innovative approaches and strategies for content enhancement, design format, and media integration. In addition, development of an app for mobile platform to offer a dynamic and seamless experience will also be explored. The Ad Hoc committee invites suggestions on the EDS Newsletter enhancements from EDS members and readers. Suggestions can be submitted via email to radhakrishnan@ieee.org

M K Radhakrishnan
EDS Newsletter New Directions Ad Hoc Committee Chair

Message from Chair of IEEE EDS Compact Modeling Committee

Yogesh S. Chauhan

I am delighted to write this message to my fellow researchers in industry and academia as a Chair of the IEEE EDS Technical Committee (TC) on Compact Modeling (CM).

The TC on CM is one of the 16 TCs under IEEE EDS. Compact modeling is a key component of process design kits (PDKs) and serves as a bridge between the foundry and the circuit designers. The objective of this TC is to work with the industry, academia, and standardization bodies on various technical issues in the field of compact modeling.

In 2022, the EDS sponsored a short course on "Modeling and simulation of Nano-transistors" organized by the IIT Kanpur Chapter, spanning over 18 days with 29 expert

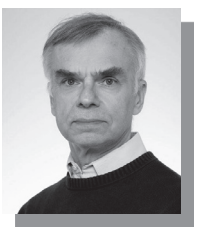
lectures on topics including physics of semiconductors and compact modeling, hands-on SPICE and TCAD simulation training, IC fabrication, atomistic simulations, RF and sub-THz measurements, neuromorphic computing, and on-wafer characterization. The recorded presentations and slides of the lectures given in the short course are available on the website https://www.youtube.com/user/yogtc/videos. EDS also sponsored three more short courses in the same year: "Machine Learning for Electron Devices" at IIT Roorkee, "Emerging Devices and Circuits to Mimic Biologically Plausible Neuronal Functionalities for Neuromorphic Computing" at IIITDM Kancheepuram, and "THz Electronics" at NIT Calicut. All these short courses were well attended by students, researchers, and engineers.

To engage the Electron Devices Community in a serious discussion with their focused scholarly contributions in the broad area of compact device modeling for circuit and system design, the TC on CM took the initiative to publish a dedicated special issue of IEEE Transactions on Electron Devices (TED) on *Semiconductor Device Modeling for Circuit and System Design*. The call for the special issue was first published in October 2022 and more than 115 submissions were received. After careful and rigorous reviews, 46 submissions were recommended for publication.

At last, I would like to highly encourage all the readers of this message to get in touch with me or any of the TC on CM members for more information and discussions on CM-related topics. If you have any suggestions, feel free to reach out to us.

Yogesh S. Chauhan
Chair of EDS Compact Modeling Committee

Message from EDS Newsletter Editor-in-Chief



Daniel Tomaszewski
EDS Newsletter
Editor-in-Chief

Dear Readers, Members of the IEEE Electron Devices Society,

Welcome to the IEEE EDS Newsletter issue of April 2024. In this short text, I would like to introduce you to some of its contents.

The Society News section brings us a Message from the EDS President. Bin Zhao who started his service in this position in January, is sharing with us a vision of the Society's future that he and the Board of Governors have been recently elaborating. Bin wrote: "*Through strategic initiatives, collaborative projects, and knowledge-sharing in leading-edge technologies, we aim to harness the collective expertise and passion of our volunteers and members to address pressing challenges and explore new frontiers in electron devices and technologies"*. Bin is presenting several steps supporting that idea that were made during the BoG meeting in December 2023. Sort of in conjunction with the EDS Presient's Message, Cary Yang presents a list of newly selected BoG officers and BoG Members-at-Large. We, the EDS Newsletter editorial team, are happy to share this vision with you and wish Bin and the Board of Governors a fruitful service for the Society. We also hope to present in the Newsletter their further activities as frequently as possible.

Please, find also in that section a list of recently nominated IEEE Fellows, members of EDS. We congratulate them on recognizing in this way their achievements in the area of Electron Devices. We present also a Message from Yogesh Chauhan, Chair of the EDS Compact Modeling Committee. We will try to continue presenting such short articles about the activities of other Technical Committees in the future. Sort of in conjunction with the Society News, please find included a broad presentation of IEEE and EDS awards given to EDS members. Congratulations to all of them!

The Technical Briefs section brings us a very interesting paper by Santosh Kurines about the 70-year-long history of Silicon Solar Cells. Santosh, thanks a lot for this contribution. Next, please find in this section a comprehensive and very "fresh" report on the EDTM 2024 conference that was held at the beginning of March in Bengaluru. The conference Team chaired by Yogesh Chauhan not only organized a great technical event but promptly prepared its review for us too. Thanks a lot! Here, I would like to draw the Reader's attention to two articles about events organized by the Women in Electron Devices Affinity Group during IEDM 2023 and EDTM 2024.

We are happy to present advertisements for five very important this year's technical conferences sponsored/co-sponsored by EDS: 70th Annual IEEE International Electron Devices Meeting IEDM), 36th International Symposium on Power Semiconductor Devices and ICs (ISPSD) 2024, 27th International Interconnect Technology Conference (IITC), 50th European Solid-State Electronics Research Conference (ESSERC) 2024, 2024 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS).

This Newsletter issue also brings, as usual, Chapter News and Regional News. They illustrate activities of the EDS chapters and joint chapters in Regions 1-7, 9, and 10. The lack of news from Region 8 results for sure from

the terrible more than two-year-long war in Ukraine that has destroyed or frozen many aspects of people's lives including IEEE and EDS chapter activities. Let us not be indifferent to the fate of our colleagues and people there. In addition, two Regional Editors for Region 8 Western Europe, and Region 8 Central Europe, and Scandinavia ended their 2nd terms. Unfortunately, despite several attempts, we have not been able to find a replacement for the latter one so far.

Dear Readers, I received recently a few questions concerning missing pages in the printed version of the Newsletter issue of January 2024. I would like to apologize to you for that mistake. If you have noticed it in your copies, let me know please. Such information can help us prevent the Newsletter production failures in future. Thanks in advance. If you have any suggestions or comments regarding the Newsletter contents, please do not hesitate to contact us. We will be very glad to receive your feedback. Interesting views will be presented with the authors' consent, along with our replies in the Letters to Editors section.

Sincerely,

Daniel Tomaszewski

IEEE EDS Fellows Elected 2024

Since 1963, IEEE has acknowledged those individuals who have contributed to the advancement of engineering science and technology. The honor of Fellow is bestowed on the recipient who has had an extraordinary record of accomplishments in any of the IEEE fields of interest. To learn more about the IEEE Fellow Program: https://www.ieee.org/membership/fellows/index.html. Congratulations to the 27 EDS members elected to IEEE Grade of Fellow in 2024.

Massood Zandi Atashbar
for contributions to flexible hybrid electronics

Joseph Bardin
for contributions to cryogenic microwave circuits

Premjeet Chahal
for contributions to additive manufacturing and materials characterization

Ke-Horng Chen
for contributions to power management integrated circuits and system design

Srabanti Chowdhury
for contributions to wide bandgap semiconductor devices and technology

Dirk Englund
for contributions to semiconductor quantum photonics and machine learning

Oliver Faynot
for leadership in CMOS technology development

Aaron Franklin
for contributions to transistor scaling and carbon nanotubes applications in electronics

Sergiu Goma
for contributions to hardware implementation of image processing for color cameras in mobile phones

Thomas Hall
for leadership in engineering technology education

Francesca Iacopi
for contributions to integration strategies of nanomaterials in silicon technologies

Debdeep Jena
for contributions to distributed polarization doping in the III-V semiconductor family

Mario Lanza
for contributions to nanoelectronics metrology of ultra-scaled materials and devices

Di Liang
for contributions to photonic integration in optical communication, computing, and volume production

Marko Loncar
for contributions to thin film lithium nanophotonics

Ionut Radu
for contributions to silicon-on-insulator materials for semiconductor devices

Li Ran
for contributions to the modeling of power electronic devices

Michael Ropp
for contributions to distributed energy resources integration in power systems

Atif Shamim
for contributions in the field of antenna-on-chip and antenna-in-package

Volker Sorger
for contributions to the optoelectronic devices and photonicelectronic ASICs

Vladimir Stojanovic
for contributions to electronic-photonic design and system-onchip integration

Yukiharu Uraoka
for contributions to reliability evaluation technology for thin film devices

Alberto Valdes-Garcia
for contributions to millimeter-wave circuits and systems for communications

Barry Bing-Ruey Wu
for contributions to enhancement and commercialization of InPbased ultra-high-speed DHBT IC technology

John Yeow
for contributions to the understanding and applications of nanostructures and nanocomposites

Shimeng Yu
for contributions to non-volatile memories and in-memory computing

Jim Zheng
for contributions to energy storage technologies

Call for nominations for the 2024 Student Fellowships

Dear EDS Members:
The IEEE Electron Devices Society invites nominations for the 2024 PhD, Masters, and Undergraduate Student Fellowships. These awards are presented annually to promote, recognize, and support undergraduate, graduate and masters level study and research within the EDS field of interest. For both Masters and PhD, it is expected that at least one fellowship will be awarded to a student in each of the following geographical regions: Americas, Europe/Middle East/Africa, and Asia/Pacific. For Undergraduate, it is expected that five fellowships will be awarded, with a selection of only one fellowship to eligible students in each of the IEEE geographical Regions 8, 9, and 10 and two fellowships in Regions 1-7, not exceeding one from Region 7.

Please visit the EDS website links below to access information about these Fellowships.

EDS Masters Student Fellowship
Prize: US $2,000 and an award plaque
Submission Deadline: June 15, 2024

EDS PhD Student Fellowship
Prize: US $5,000 and travel funds to attend the IEDM for presentation of an award plaque
Submission Deadline: June, 15 2024

EDS Undergraduate Student Fellowship
Prize: US $1,000 and an award plaque
Submission Deadline: June 15, 2024

Please help to promote the EDS Student Fellowships by distributing this information to your colleagues and students. If you have any questions or need further information, please do not hesitate to contact Stacy Lehotzky by email at s.lehotzky@ieee.org.

Thank you!

Call for Nominations Editor-in-Chief
IEEE Transactions on Device and Materials Reliability

The *IEEE Transactions on Device and Materials Reliability (TDMR*) provides leading-edge/state-of-the-art information that is critically relevant to the creation of reliable microelectronic products. The Transactions is a forum for interdisciplinary studies on reliability and publishes original and significant research contributions on the reliability of Electronic and Photonic Devices, Materials, Processes, Interfaces, Integrated Microsystems (including MEMS & Sensors), Process Technology (CMOS, BiCMOS, etc.) and Integrated Circuits (IC, SSI, MSI, LSI, ULSI, etc.) and Packages. The measurement and understanding of the reliability of such entities at each phase, from the concept stage through research and development and into manufacturing scale-up, provides the overall database of the reliability of the devices, materials, processes, package, and other necessities for the successful introduction of a product to market. Reliability, in a sense, is everything that can be or has to be done to guarantee that the product successfully performs in the field under customer conditions. Our goal is to capture these advances.

Founded in 2000, TDMR publishes original papers and letters. The editor-in-chief together with the editorial team also solicits review articles and invited papers for special issues on highly topical themes. TDMR is co-sponsored by the IEEE Electron Devices and the IEEE Reliability Societies.

Nominations and applications are invited for the position of Editor-in-Chief (EiC) for TDMR for a 3-year term **beginning as soon as available, but no later than January 2025**. The EiC's ongoing duties include assigning submitted manuscripts to one of the editors who cover the range of reliability issues within TDMR's scope. The EiC makes the final decision regarding the disposition of each manuscript submitted to TDMR based on the recommendation of the editor. TDMR publishes four issues per year, each approximately 150-200 pages in length.

The EiC is helped administratively by a person from the IEEE publications staff.

Criteria for the Nominees:

- Ability and motivation to spend sufficient time assigning manuscripts and reviewing the acceptance or rejection recommendations made by the editors;
- Demonstrated technical leadership within the field of reliability evaluation and characterization;
- Formal support from the institution for which the nominee works (waived if self-employed or employed at an academic institution);
- Experience serving as an editor of TDMR or another journal whose scope includes the field of reliability of microelectronic devices;
- Commitment to guide TDMR according to this Call for Nominations and to further actively develop the journal;
- Willingness to work collaboratively with internal and external stakeholders to ensure the technical leadership and fiscal health of TDMR.

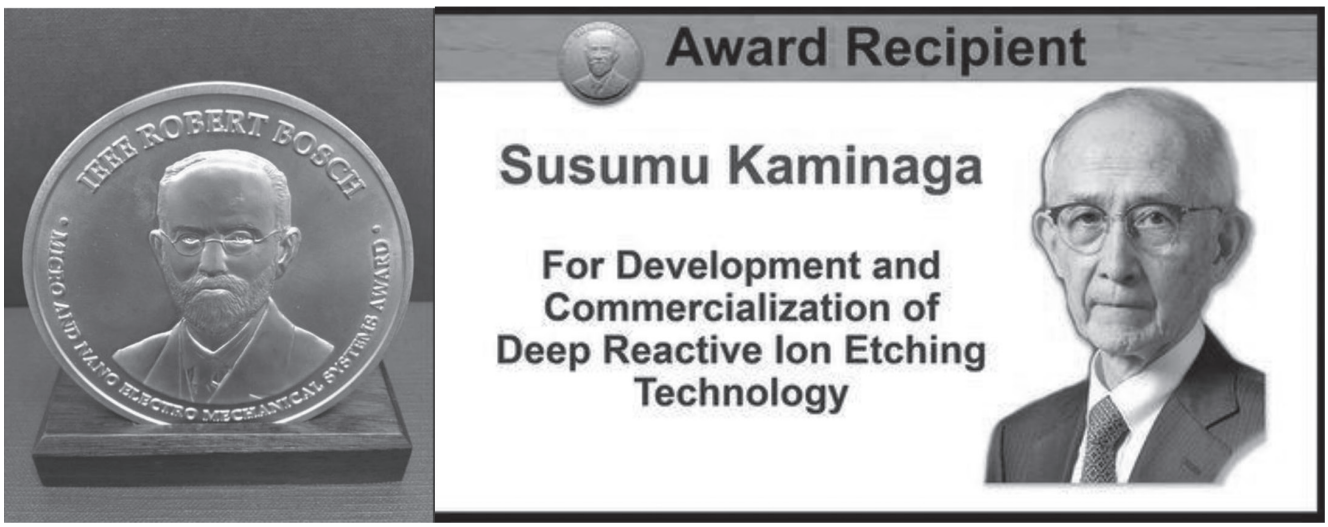
Requirements for Nominations:

- A brief IEEE-style biography (up to 250 words) of the nominee;
- A complete CV and list of publications of the nominee;
- A brief statement from the nominator on the nominee's qualification and how the nominee meets the criteria listed above;
- A letter from the nominee's employer indicating support for the EiC activity (can be waived, see above);
- Endorsement from two IEEE members on the nomination;
- A statement (up to 500 words) from the nominee on his/her vision and plan for the journal.

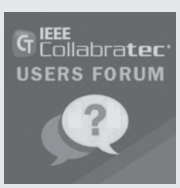
Please email the nomination materials to Laura Riello (l.riello@ieee.org), no later than **May 15, 2024**

2024 IEEE EDS Robert Bosch Micro and Nano Electro Mechanical Systems Award Winner

The 2024 IEEE EDS Robert Bosch Micro and Nano Electro Mechanical Systems Award was awarded to Susumu Kaminaga. The award was presented at the 2024 IEEE MEMS Conference, January, 2024. This prestigious award recognizes and honors advances in the invention, design, and/or fabrication of micro- or nano-electromechanical systems and/or devices.



Osamu Tabata
EDS Bosch Award Chair



IEEE Collabratec Users Forum

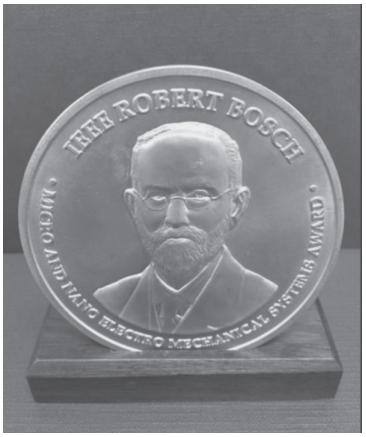
This community forum provides IEEE Collabratec users the opportunity to ask questions about the platform, report system problems, especially critical ones, and learn about new features and functionality on the platform. Users should avoid posting complex laundry lists, personal discussions, or other items that don't relate to user issues. Also, unless you are CT Staff or have gone through Ambassador training, do not provide alternate training that may confuse users. Thank you!

Communities in IEEE Collabratec® offer a forum to:

- Stay current with opportunities and insights around the community's shared interests including location, interests, or career pursuits
- Network with like-minded people
- Pose, discover, and receive answers to technical and professional questions
- Exclusive IEEE Collabratec® communities may require additional memberships

IEEE EDS ROBERT BOSCH MICRO AND NANO ELECTRO MECHANICAL SYSTEMS AWARD

CALL FOR NOMINATIONS



Robert Bosch (1861-1942)
Inventor, Entrepreneur, Founder of Robert Bosch GmbH

The Robert Bosch Micro and Nano Electro Mechanical Systems Award was established by the IEEE Electron Devices Society in 2014, to recognize and honor advances in the invention, design, and/or fabrication of micro- or nano-electromechanical systems and/or devices. The contributions to be honored by this award should be innovative and useful for practical applications.

This award is sponsored by the IEEE Electron Devices Society, with financial support from Robert Bosch LLC. It is intended that the award will be presented annually to an individual or to as many as three individuals whose achievements and contributions are judged to meet the selection criteria for the award. The award will be presented at an IEEE conference of the winner's choice. It is not necessary for the recipient(s) to be a member(s) of IEEE.

The recipient will receive a US$10,000 honorarium, travel expenses to attend the award presentation, a bronze medal, and a certificate. If more than one awardee is selected the cash honorarium will be equally divided among the recipients. Each recipient will receive a bronze medal and a certificate.

Please visit the EDS website for more information on this award:
https://eds.ieee.org/awards/robert-bosch-micro-and-nano-electro-mechanical-systems-award.

Nominations for this award should be made using our online nomination form, and submitted before midnight (EST) on October 2nd.

Congratulations to James Hwang
2023 IEEE EDS Lester F. Eastman Award Winner

Ravi Todi, 2023 EDS President presenting the 2023 Lester Eastman Award to James Hwang

James Hwang is a professor in the Department of Materials Science and Engineering at Cornell University. He graduated from the same department with a Ph.D. degree. After years of industrial experience at IBM, Bell Labs, GE, and GAIN, he spent most of his academic career at Lehigh University. He cofounded GAIN and QED; the latter became the public company IQE and remains the world's largest compound-semiconductor epitaxial wafer supplier. He has been a consultant for the US Air Force Research Laboratory. He was a Program Officer at the U.S. Air Force Office of Scientific Research for GHz-THz Electronics. He is an IEEE Life Fellow and an editor for the IEEE Transactions on Microwave Theory and Techniques. He has published over 400 refereed technical papers and been granted eight U.S. patents. He has researched the design, fabrication and characterization of electronic, opto-electronic, and micro-electromechanical materials, devices and circuits. His current research focuses on materials, devices and circuits above 110 GHz for 6G wireless communications, next-generation automobile radars, and low-orbit satellites.

As an individual contributor, Dr. Hwang invented PECVD SiN passivation and analyzed failure modes of GaAs power transistors, resulting in orders-of-magnitude improvement in device life and enabling their use in TELSTAR satellites. He designed an advanced reactor that transformed molecular beam epitaxy from research to manufacturing. Using the reactor, he demonstrated record-quality GaAs heterostructures, which allowed Drs. Laughlin, Stormer, and Tsui to systematically investigate the fractional quantized Hall effect and to win the 1998 Nobel prize in physics. As a technical leader, he led a team to demonstrate 1) the first 0.25-μm high-electron-mobility transistor (HEMT) with record high-frequency and low-noise performance, 2) the first power HEMT while others thought HEMT was good only for low-noise applications, and 3) the first cryogenic HEMT enabling NASA to detect the extremely weak signals beamed back by the deep-space explorer Voyager 2 when it outlived its life expectancy and continued its voyage to Uranus and Neptune. His team was the first to investigate the "power slump" problem of HEMTs and to propose a trap-induced mechanism. He led the efforts to solve the dielectric charging problem of RF MEMS switches and demonstrated billions of life cycles for the first time. His team continues to lead the world in broadband sensing and characterization of individual biological cells. Most recently, he invented a microwave annealing tool for efficient, abrupt and stable activation of dopants above their solubility limits in semiconductors.

IEEE Electron Devices Society

Erhard Kohn
2023 EDS Lester F. Eastman Award Chair

IEEE EDS Lester F. Eastman Award

Call For Nominations

The IEEE Electron Devices Society invites the submission of nominations for the Lester F. Eastman Award. This award is presented annually to honor an individual who has made an outstanding achievement in high-performance semiconductor devices. The recipient is awarded a certificate and a check for $5,000, presented at the IEEE International Electron Devices Meeting (IEDM).

Description: To recognize individuals with outstanding achievement in high-performance semiconductor devices

Prize: $5,000 and a plaque

Funded: Funded by the Lester F. Eastman endowment fund and the IEEE Electron Devices Society

Eligibility: Any person active in the field of semiconductor devices, whether or not they are members of the IEEE Electron Devices Society, are eligible for the award. The EDS Lester Eastman Award cannot be given to a candidate for the same work for which an IEEE Technical Field Award, IEEE Medal, or other society level award was previously received.

Basis for Judging: Criteria considered by the selection committee will include an impact on the field of semiconductor devices. Evidence should include examples of leadership and professional interaction. Tangible supporting evidence in the form of publications, patents, and/or transition(s) to practice should be provided.

Presentation: Annually, at the International Electron Devices Meeting (IEDM)

Visit: https://eds.ieee.org/awards/lester-f-eastman-award

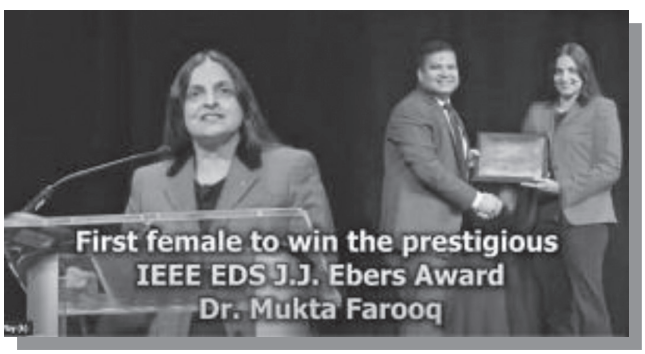
Donate: https://www.ieeefoundation.org/Eastman

Contact: If you have additional questions, contact the EDS Executive Office at eds@ieee.org

Nomination form: Visit the EDS website

Deadline to submit nominations: July 1st

2023 IEEE EDS J.J. Ebers Award Winner



Mukta Farooq, 2023 IEEE EDS J.J. Ebers Award Winner
For development of emerging heterogeneous integration architectures for 3D ICs

Dr. Mukta Farooq is an IBM Distinguished Research Scientist, and 3D/Heterogeneous Integration Leader for the IBM AI Hardware Center. She is an IEEE Fellow, IEEE EDS Distinguished Lecturer, and IIT-Bombay Distinguished Alumna.

Mukta is a materials scientist with expertise in Heterogeneous Integration for AI Architectures, 3D Copper TSV (Through-Silicon-Vias), CMOS BEOL (Back-End-Of-Line), C4 (Controlled-Collapse Chip Connection), Lead-Free Alloys, and Chip-Package Interaction. She has 233 granted US patents and 66 international patents. Mukta's wide-ranging contributions to intellectual property were recognized by her appointment as IBM Lifetime Master Inventor and member of the IBM Academy of Technology.

Mukta has been invited for keynote talks and short courses at IEDM, EDTM, VLSI, ASMC, and universities. She has written seminal papers in semiconductor technology. Mukta received the IEEE EPS Sustained Contribution and Region1 Technological Innovation Awards. She is an active mentor to Women-in-EDS. Mukta received her BS from IIT-Bombay, MS from Northwestern University, and PhD from Rensselaer Polytechnic Institute.

Paul Yu
EDS J.J. Ebers Award Chair

IEEE ELECTRON DEVICES SOCIETY
J.J. EBERS AWARD

Nominate:
https://eds.ieee.org/awards/j-j-ebers-award

Submission Deadline:
July 1, 2024

Contact:
If you have any questions regarding the EDS J.J. Ebers Award, please contact the EDS Executive Office at eds@ieee.org

CALL FOR NOMINATIONS

The IEEE Electron Devices Society (EDS) invites the submission of nominations for the 2024 J.J. Ebers Award. This award is presented annually by EDS to honor an individual(s) who has made either a single or a series of contributions of recognized scientific, economic, or social significance to the broad field of electron devices. The recipient(s) is awarded a plaque and a check for $5,000, presented at the International Electron Devices Meeting (IEDM) or any one of the EDS's flagship conferences.

2023 IEEE Electron Devices Society Education Award Winner

Chancellor Gary S. May (right) with 2023 EDS President, Ravi Todi

The EDS Education Award recognizes an IEEE/EDS Member from an academic, industrial, or government organization with distinguished contributions to education within the fields of interest of the IEEE Electron Devices Society. Chancellor Gary S. May was selected as the 2023 EDS Education Award winner. The award cites Chancellor Gary May "For dedicated leadership and mentorship that has diversified academic leaders in education".

Chancellor Gary S. May is a highly engaged leader with a passion for helping others succeed. He believes success is best judged by how we enhance the lives of others.

Throughout his career, he's championed diversity, equity and inclusion in both higher education and the workplace. He developed nationally recognized programs that attract, mentor and retain underrepresented groups in the STEM fields of science, technology, engineering and math. In 2015, President Obama honored him with the Presidential Award for Excellence in STEM Mentoring.

May earned his master's and Ph.D. degrees in electrical engineering and computer science at UC Berkeley. He was inducted to the National Academy of Engineering in 2018. In 2020, May was elected to the American Academy of Arts and Sciences under the classification of "educational and academic leadership." In 2021, May was awarded a Lifetime Mentor Award from the American Association for the Advancement of Science and an honorary doctorate from the Georgia Institute of Technology.

A prominent voice in higher education, May is a Commissioner of the Council on Competitiveness and other national committees.

His vision as UC Davis' seventh chancellor is to lead the university to new heights in academic excellence, inclusion, public service and upward mobility for students from all backgrounds.

Hiroshi Iwai
2023 EDS Education Award Chair

2024 EDS EDUCATION AWARD
CALL FOR NOMINATIONS

The IEEE Electron Devices Society invites the submission of nominations for the EDS Education Award. This award is presented annually by EDS to honor an individual who has made distinguished contributions to education within the field of interest of the Electron Devices Society. The recipient is awarded a plaque and a check for $2,500, presented at the IEEE International Electron Devices Meeting (IEDM).

The nominee must be an EDS member engaged in education in the field of electron devices, holding a present or past affiliation with an academic, industrial, or government organization. Factors for consideration include achievements and recognition in educating and mentoring students in academia or professionals in the industrial or governmental sectors. Specific accomplishments include effectiveness in the development of innovative education, continuing education programs, authorship of textbooks, presentation of short-courses at EDS sponsored conferences, participation in the EDS Distinguished Lecturer program, and teaching or mentoring awards.

Since this award is solely given for contributions to education, the nomination should exclude emphasis on technical contributions to engineering and physics of electron devices.

The nomination form can be found on the EDS website:
https://eds.ieee.org/awards/education-award

The deadline for the submission of nominations for the 2024 award is September 1, 2024.

2023 IEEE EDS Distinguished Service Award

EDS President Ravi Todi (left) presenting Distinguished Service Award to Fernando Guarin (right)

The IEEE Electron Devices Society (EDS) is extremely proud of the services that it provides to its members. EDS members generate the leading edge developments in the field of electron devices and share these results with their peers and the world-at-large by publishing their papers in EDS journals and presenting results in its meetings. This is a global activity that is effective because of the efforts of numerous volunteers. Many of these dedicated volunteers labor in relative obscurity, with their only reward being the satisfaction that they receive in being an important part of a successful organization, namely of the IEEE Electron Devices Society. One means of thanking these volunteers is to recognize their contributions through the EDS Distinguished Service Award.

The recipient of the 2023 EDS Distinguished Service Award was Dr. Fernando Guarin. Please visit the IEEE EDS website to view the award presentation video.

Dr. Fernando Guarín is an IEEE Lifetime Fellow, Senior Past President of EDS, Chair of IEEE's Smart Village (ISV) Board of Governors and Distinguished Lecturer for the IEEE Electron Device Society since 2005. He has served EDS in many capacities including Chapter Chair for Mid-Hudson Valley, member of the IEEE's EDS Board of governors, Chair of the EDS Education Committee, and Secretary for EDS. Dr. Guarin was the EDS President 2018-2019. He earned his BSEE from the "Pontificia Universidad Javeriana", in Bogotá, Colombia, the M.S.E.E. degree from the University of Arizona, and his Ph.D. in Electrical Engineering from Columbia University, NY. Over the span of his career, he made several key contributions to semiconductor reliability and physics-based aging models.

Dr. Fernando Guarin worked in the semiconductor industry as individual contributor and team leader for over 42 years. From 1980 until 1988 he worked in the Military and Aerospace Operations division of National Semiconductor Corporation. In 1988 he joined IBM's microelectronics division where he worked in the reliability physics and modeling of Advanced Bipolar, CMOS and Silicon Germanium BiCMOS technologies. In 2015 he retired from IBM's Semiconductor Division at the Senior Member of Technical Staff level. Most recently he was the leader of the team qualifying GlobalFoundries RF 5G technology offerings. He retired in July 2022 as a Distinguished Member of Technical Staff from GlobalFoundries, New York where he led the reliability teams responsible for the qualification of 5G and SiGe technologies. He has authored over 160 technical papers and semiconductor technology qualification reports, 12 patents, 6 book chapters and has delivered over 50 lectures in Europe, Asia, and the Americas as Distinguished Lecturer for EDS.

Ravi Todi
EDS Awards Chair

2023 IEEE Electron Devices Society Early Career Award Winners

2023 EDS President, Ravi Todi presenting 2023 Early Career Award winner, Abhronil Sengupta

2024 EDS President, Bin Zhao presenting 2023 Early Career Award winner, Shubham Sahay

2023 EDS President, Ravi Todi presenting 2023 Early Career Award winner, Yansong Yang

The EDS Early Career Award recognizes young IEEE/EDS members who have made outstanding contributions in an EDS field of interest during the early years of their professional career after graduation.

The 2023 EDS Early Career Award winners are Abhronil Sengupta (The Pennsylvania State University), Shubham Sahay (Indian Institute of Technology), and Yansong Yang (Hong Kong University of Science and Technology). The award presentations took place at the 2023 IEDM and 2024 EDTM.

Please visit the IEEE EDS website to view additional information about the award.

Bin Zhao
2023 EDS Early Career Award Chair

CALL FOR NOMINATIONS

2024 IEEE EDS Early Career Award

Description: Awarded annually to individuals to promote, recognize and support Early Career Technical Development within the Electron Devices Society's field of interest.

Prize: An award of US$1,000, a plaque; and if needed, travel expenses not to exceed US$1,500 for each recipient residing in the US and not to exceed US$3,000 for each recipient residing outside the US to attend the award presentation.

Eligibility: Nominees are required to be IEEE EDS members. Nominees must have their first professional degree within the 10th year defined by the August 15 nomination deadline and have made contributions in an EDS field of interest area. Nominators must be IEEE EDS members. Previous award winners are ineligible.

Selection/Basis for Judging: The nominator will be required to submit a nomination package comprised of the following:

- The nomination form that is found on the EDS website, containing such technical information as the nominee's contributions, accomplishments and impact on the profession or economy and a biographical description.
- A minimum of two and a maximum of three letters of recommendation from individuals familiar with the candidate's technical contributions and other credentials, with emphasis on specific contributions and their impact.

The basis for judging includes such factors as: demonstration of field leadership in a specific area; specific technical contribution(s); impact on the profession or economy; originality; breadth; inventive value; publications; honors; and other appropriate achievements.

Schedule: Nominations are due to the EDS Executive Office on **August 15th** each year. Candidates will be selected by the end of September, with the presentation to be made in December.

Presentation: At the EDS Awards Dinner that is held in conjunction with the International Electron Devices Meeting (IEDM) in December. The recipients will also be recognized at the December EDS BoG Meeting.

Nomination Form: Visit the EDS website: https://eds.ieee.org/awards/early-career-award

For more information contact: eds@ieee.org

Arokia Nathan
EDS Early Career Award Chair

Transactions on Semiconductor Manufacturing Best Paper Award

Best Paper Award 2023

Bayesian Nonparametric Classification for Incomplete Data With a High Missing Rate: an Application to Semiconductor Manufacturing Data

Authors: Sewon Park, Kyeongwon Lee, Da-Eun Jeong, Heung-Kook Ko, and Jaeyong Lee

Honorable Mention Award 2023

Machine Learning-Based Edge Placement Error Analysis and Optimization: A Systematic Review

Authors: Anh Tuan Ngo, Bappaditya Dey, Sandip Halder, Stefan De Gendt, and Changhai Wang

Automatic Pico Laser Trimming System for Silicon MEMS Resonant Devices based on Image Recognition

Authors: Yuxian Liu , Qiancheng Zhao, Dacheng Zhang, and Jian Cui

Best Paper Award 2023 Editorial

The IEEE Transactions on Semiconductor Manufacturing congratulates Sewon Park, Kyeongwon Lee, Da-Eun Jeong, Heung-Kook Ko, and Jaeyong Lee whose paper "Bayesian Nonparametric Classification for Incomplete Data With a High Missing Rate: an Application to Semiconductor Manufacturing Data" (Vol. 36, No. 2, May 2023) was selected as the Best Paper for 2023 by a team of Associate Editors. This paper proposes using the the Dirichlet Process - Naive Bayes model (DPNB) to simultaneously impute missing values and address classification problems in semiconductor manufacturing data. The DPNB is based on the use of infinite Gaussian mixture models to model complex data distributions and estimate missing data records and variables, which is of utmost importance in semiconductor manufacturing. The DPNB performs well for high missing rates since it uses all the information from observed components. Experiments on various real datasets including semiconductor manufacturing data show that the DPNB has better performance than state-of-the-art methods in terms of predicting missing values and target variables as percentage of missing values increases.

Two other papers were recognized with an Honorable Mention.

a) "Machine Learning-Based Edge Placement Error Analysis and Optimization: A Systematic Review" by Anh Tuan Ngo, Bappaditya Dey, Sandip Halder, Stefan De Gendt, and Changhai Wang (Vol. 36, No. 1, February 2023)

b) "Automatic Pico Laser Trimming System for Silicon MEMS Resonant Devices based on Image Recognition" by Yuxian Liu , Qiancheng Zhao, Dacheng Zhang, and Jian Cui (Vol. 36, No. 2, May 2023

The Editorial Board of IEEE Transactions on Semiconductor Manufacturing Journal continues to explore innovative all of semiconductor manufacturing with special attention to design, modeling and process control aspects. The entire editorial team for IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING welcomes authors to submit their papers for review. We also encourage all authors and readers to participate in the manuscript review process. The 2023 Best Paper selection team consisted of Dr. Jeanne P. Bickford, Dr. Dragan Djurdjanovic, and Dr. Natarajan Mahadeva Iyer.

The 5th IEEE IEDM 2023 Women in Electron Devices (WiED) and Young Professionals (YP) session

By P Susthitha Menon, Mario Aleman, Mukta Farooq, Tsu-Jae King Liu, Fernando Guarin, Merlyne de Souza, Qianqian Huang, and Laura Riello

The IEEE Women in Electron Devices (WiED) and IEEE Young Professionals (YP) joint panel session was held during the 69th International Electron Devices Meeting (IEDM) on 12 December 2023 at Hilton San Francisco Union Square, California, USA. The event was moderated by the 2023 JJ Ebers Award Winner, Mukta Farooq, an IEEE Fellow from IBM Semiconductor Research – Thomas J. Watson & Albany. The panel members were Tsu-Jae King Liu (University of California, Berkeley), Fernando Guarin (Past Chair of IEEE EDS & ex-GlobalFoundries), Merlyne de Souza (University of Sheffield), and Qianqian Huang (Peking University, China). The event was fully sponsored by IEEE EDS and was attended by 50 people. We discussed various topics related to life trajectories and the secret of the panel members' successes. About 50% of the audience were young professionals with less than 10 years of working experience.

The event kicked off with WiED Chair P Susthitha Menon (National University of Malaysia, UKM) introducing the event moderator and panel members, followed by welcoming remarks from Ravi Todi, IEEE EDS President. Next, Dr. Mukta Farooq introduced herself and invited the panel members to introduce themselves via individual infographic posters highlighting their achievements, years of experience, family, and hobbies. The session was intertwined with polling questions to make it interactive for the audience and the panel members. The session introduced many interesting questions, including how the panel members managed stress and avoided burnout when trying to balance work and personal life. The panelists also shared how cultural differences impact people's views on the balance between career and personal life. Some other issues that were discussed were societal pressures influencing people's decisions regarding career and personal life.

The audience was very active in asking various types of questions via the polling app. Some of them included whether panel members ever had to work regularly on weekends and if so, how they managed a healthy work-life balance. This topic was further discussed in view of the pandemic, and whether that event had significant implications now in the post-pandemic era. Other questions posted were how panel members balance their time between their respective departments/schools and professional societies like IEEE EDS. All questions were answered by panel members, and the audience was 100% satisfied with the answers, which surpassed their expectations of the event which lasted 2 hours!

In the closing remarks, IEEE EDS President-Elect, Bin Zhao thanked the organizers, moderator, and panelists. He then gave tokens of appreciation followed by a group photo. Thank you to IEEE EDS, IEDM, WiED, YP, the organizers, panelists, and especially the audience, for making this event a huge success!

The EDS President-Elect, Bin Zhao (left) with the panel moderator, Mukta Farooq, the panelists: Tsu-Jae King Liu, Fernando Guarin, Merlyne de Souza, Qianqian Huang, and the WiED Chair, P Susthitha Menon

Women in Electron Devices Panel Session at the 8th IEEE-EDTM 2024

By Pei-Wen Li, P Susthitha Menon, Shubhangi Bharadwaj, Francesca Iacopi, John Dallasesse, Madhu Bhaskaran, Mayank Shrivastava, Yogesh Chauhan, Durga Misra, and Bin Zhao

The IEEE Women in Electron Devices (WiED) panel session, sponsored by the IEEE Electron Devices Society (EDS) was held during the 8th IEEE Electron Devices Technology and Manufacturing (IEEE EDTM) 2024 Conference on 5 March 2024 at the Hilton Garden Inn Bengaluru Embassy Park, Bangalore, India. With the theme *Empowering Diversity in Electron Devices: Navigating Career Success, Wellness and Work-Life Balance*, the session was moderated by WiED member, Prof. Pei-Wen Li from the National Yang Ming Chiao Tung University, Taiwan. The panel members were Prof. John Dallesasse (University of Illinois at Urbana Champaign, USA), Prof. Francesca Iacopi (University of Technology Sydney, Australia), Prof Madhu Bhaskaran (RMIT University Australia), Dr Vini Gautam, and Shubhangi Bharadwaj (Indian Institute of Science, Bangalore). The event was attended by 30+ people.

The event kicked off with welcoming remarks from IEEE EDS President, Bin Zhao (ON Semiconductor) and IEEE EDS Vice President of Membership, Durga Misra (New Jersey Institute of Technology, USA). Next, WiED Chair, P Susthitha Menon (National University of Malaysia, UKM) gave a virtual introduction to the various initiatives of the WiEDS affinity group. The moderator, Pei-Wen introduced herself and invited the panel members to introduce themselves via individual infographic posters highlighting their achievements, years of experience, family, and hobbies.

The audience gained valuable insights and discussed issues with the outstanding panelists who hail from versatile backgrounds in the academic and semiconductor industry. They all unanimously agreed that work-life balance is important because it reduces stress, helps avoid burnout, increases job/personal satisfaction, and improves overall health and productivity. In order to achieve a healthy work-life balance, the audience was advised to manage their priorities and commitments. This requires an organized approach to both time and task management. Fruitful communication and sharing between the audience and panelists brought forth tips for managing stress, staying centered, and remaining calm in the midst of hectic workdays as well as in personal life. These include but are not limited to "Set boundaries between work and personal time", "Schedule time for hobbies and interests", "Delegate tasks when possible", "Say No to extra work when necessary", "Practice Relaxation techniques", and "Love to give". Another discussion point was how to make recruitment processes more equitable, taking into account career interruptions, for example, due to carer's responsibilities. At this point, the EDS President Bin Zhao also reminded that the Early Career Award now allows to declare career interruptions and still qualify within the required time window, and that EDS is on course to making adjustments at all levels to embrace more equity and diversity. There were also messages around "pay it forward" and "strategizing for success".

The session was remarkable because of the active participation of senior semiconductor professionals as well as young engineers/students who were able to interact freely and share their insights/experiences.

Thank you to IEEE EDS, EDTM, WiED, the organizers, panelists, and especially the audience, for making this event a huge success!

Group photo with IEEE EDS President, Bin Zhao with the moderator, panel members, and attendees

Chapter News

ED Indonesia Chapter

PRE-U STEM: Implementation of Virtual Reality-Based Electromagnetic Field Learning for Senior High School Students in West Java, Indonesia

—by Basuki Rachmatul Alam

The ED Indonesia, led by Prof. Budi Mulyanti and Dr. Roer Eka Pawinanto, has been organizing a series of pre-university STEM workshops in 12 Senior High Schools/Vocational High Schools across West Java, Indonesia. These workshops focus on the implementation of Virtual Reality (VR) in the learning of Electromagnetic Field (EM) and are funded by the IEEE EDS project.

The team of lecturers, comprised of educators from the Education University of Indonesia, has conducted these pre-university STEM workshops to engage thousands of Senior and Vocational high school students. The goal is to inspire creativity, critical thinking, and problem-solving skills by utilizing virtual reality technology for a better understanding of electromagnetic fields. The initiative aims to stimulate cognitive processes, including critical thinking, creativity, and problem-solving skills, among pre-university students in the subject matter of EM field learning.

A student of State Senior High School 17 in Bandung, West Java using virtual reality to study electromagnetic fields.

This project encourages collaboration among educational institutions, the university community, and relevant stakeholders. The workshops already took place in three Senior High Schools and three Vocational High Schools during daytime sessions in November 2023. The series will continue in January 2024 with workshops scheduled in six other High Schools and Vocational High Schools in different areas of West Java.

Each workshop consists of two 40-minute lectures conducted by two lecturers, followed by an 80-minute hands-on session where students practice the use of Virtual Reality in learning EM field concepts. The first lecture focuses on understanding the concept of Electromagnetic Field by exploring Virtual Reality as a learning medium, while the second lecture delves into enhancing students' critical, creative, and problem-solving skills in Electromagnetic Field learning using Virtual Reality media.

During the November 2023 sessions, 89 to 112 students from each High School or Vocational High School actively participated, resulting in a total of 601 students. The upcoming January 2024 workshops aim to involve a maximum of 720 students across six different Senior High Schools and Vocational High Schools.

Students of State High School 1 at Cilimus, West Java after practical session on the use of virtual reality in electromagnetic field learning.

The participation of all students in the learning process is crucial for acquiring knowledge about electromagnetic fields through the utilization of virtual reality media. The tutor team includes senior members and members of the ED Indonesia, along with student members actively involved in the workshop.

~ Sharma Rao Balakrishnan, Editor

ED Malaysia Chapter

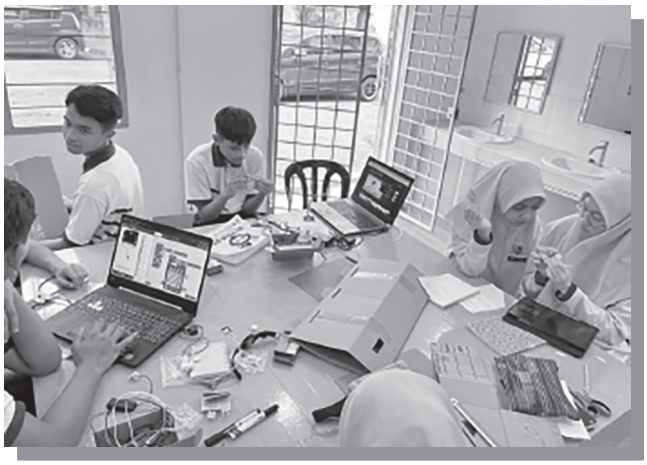
2023 IEEE EDS Malaysia Chapter Do-Your-Bit Nature Challenge 2.0

—by Rosminazuin Ab Rahim, Aliza Aini Md Ralib, and Nurul Ezaila Alias

The Do-Your-Bit Nature Challenge 2.0 builds upon the success of the previous online Microbit design competition, Do-Your-Bit Nature Challenge 1.0, which was conducted during the pandemic for Form 4 students from Sekolah Berasrama Penuh Integrasi Gombak (SBPI Gombak) in 2021 (30 August–14 September 2021). The earlier program was sponsored by IEEE R10 EA in 2021.

Do Your Bit Nature Challenge 2.0 was a 2-day workshop and 1-day competition designed to introduce the Sustainable Development Goals (SDGs) through Microbit to Form 3 students. The event hosted 40 participants, including 4 student volunteers, 6 staff volunteers, and 2 competition judges. The aim was to kindle an interest in STEM education among Form 3 students at Sekolah Berasrama Penuh Integrasi Gombak, Malaysia.

Before the competition date, participants received comprehensive online lesson plans (series of videos) guiding them on Microbit and how to develop simple systems using the microcontroller. The program spanned two days at the school and was divided into two phases: Phase 1 involved group discussions where students were given a theme, a Microbit kit with sensors and actuators, and had to discuss the problem, propose a solution with a block diagram, and present their ideas as a group. On the second day, students were provided with basic knowledge about the Microbit kit, sensors, actuators, and coding techniques. This phase aimed to support participants in utilizing Microbit to design a simple sensor system.



Picture of the participants and their activities throughout the Do Your Bit Nature Challenge 2.0 event.

The highlight of the program was the face-to-face competition held at the Kulliyyah of Engineering, IIUM, on 14 September 2023. During this competition, students were tasked with developing a simple sensor system using a Microbit microcontroller. Based on the positive feedback received, all groups successfully presented working prototypes and effectively communicated the components used in their prototypes.

Participants thoroughly enjoyed the program and expressed satisfaction with its content. Most students demonstrated an understanding of coding according to the provided kit. A feedback video is available at https://youtu.be/LCizpHBaxTQ.

2023 IEEE EDS Malaysia Chapter STEM IT RIGHT Showcase

—by Rosminazuin Ab Rahim, Aliza Aini Md Ralib, and Nurul Ezaila Alias

The STEM IT RIGHT Showcase was successfully organized at three schools in Kuala Lumpur, Malaysia, targeting the following institutions:

- September 4, 2023: STEM IT RIGHT at Sekolah Men Melawati
- September 5, 2023: STEM IT RIGHT at Sekolah Men Al Amin
- September 6, 2023: STEM IT RIGHT at Sekolah Men Setia Budi

The event engaged a total of 372 Form 3 students, with the invaluable support of 25 student volunteers and 6 staff volunteers. The decline in Form 3 students opting for STEM subjects is a concerning trend, leading to a decrease in STEM enrollment across various schools. As STEM professionals, it is our responsibility to address this issue and provide students with the right perspective on STEM education.

In collaboration with Kulliyyah of Engineering, IIUM, IEEE EDS Malaysia, ICESCO, SCITECH flagship, and IEEE Malaysia, we have initiated a project to conduct a series of half-day workshops for Form 3 students. This endeavor

Picture of the participants throughout the STEM IT RIGHT Showcase.

aims to expose students to diverse STEM-based activities, including interactive talks with professors, hands-on sessions, and group discussions under the theme "Let's Think Like Engineers." The entire program is generously sponsored by the IEEE STEM Portal Grant from the Islamic World Educational, Scientific, and Cultural Organization (ICESCO).

The "STEM IT RIGHT" workshop serves as an eye-opener for students, inspiring them to explore STEM further as they progress to Form 4. Through this collaborative initiative, the IEEE EDS Malaysia Chapter, Kulliyyah of Engineering, and IIUM aspire to be recognized globally as catalysts in empowering STEM talents and making meaningful contributions to humanity.

IEEE EDS Design Your Own PCB Circuit With Eagle

—by Zurita Zulkifli and Sukreen Hana Herman

A hands-on workshop for the school community in Sabak Bernam took place on 15–16 November 2023. The workshop engaged 6 secondary schools (with 30 students and 6 teachers) and 5 primary schools (with 30 students and 5 teachers). Over the two days, the workshop provided valuable learning opportunities for both teachers and students as they designed their own Printed Circuit Board (PCB) circuits and gained hands-on experience in soldering.

The participants were introduced to the EAGLE software for schematic circuit drawing and PCB design. The teaching commenced with the fundamentals of creating schematic diagrams, involving the selection of appropriate components, adding components to the EAGLE library, and correct circuit connections. The Electrical Rule Check was employed to ensure error-free schematics before converting them into PCB forms. Participants were tasked with arranging components on the PCB board to design their circuits. Once the PCB design was finalized, participants had the chance to place components on the completed PCB board. Circuit testing followed to confirm the proper functioning of the components.

Excitement filled the room as participants successfully activated blinking LEDs in their circuits. To add a personal touch, the PCB boards were transformed into keychains. The program, supported by funding from the IEEE Pre-U STEM program, opened up new avenues for learning materials, empowering teachers and students in the realm of electronics and PCB design.

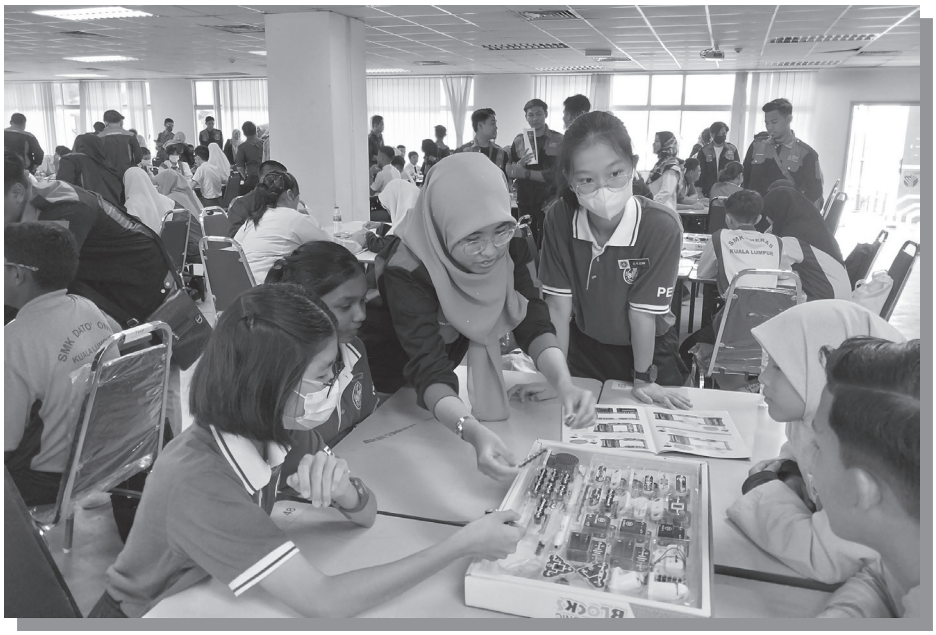
STEM4FUN: STEM FOR ALL Program Leaves A Good Impression on Mainstream and Special Integrated Education Program (PPKI) Students From 32 Schools in Kuala Lumpur

—by Maizatul Zolkapli, Ahmad Sabirin Zoolfakar, Rozina Abdul Rani, and Azrif Manut

On 25 October 2023, the STEM4FUN: STEM FOR ALL program in conjunction with the Kuala Lumpur State Education Department STEM Convention was executed in collaboration with Universiti Teknologi MARA (UiTM) final-year students pursuing a Bachelor's Degree in Electronic Engineering with Honors. Led by Assoc. Prof Ir. Dr. Ahmad Sabirin Zoolfakar and Ir. Dr. Maizatul Zolkapli, the program sought to spark interest in STEM subjects among mainstream and Special Integrated Education Program (PPKI) students from 32 schools in Kuala Lumpur. Running from 8:00 am to 1:00 pm, the program engaged a total of 102 students organized into 40 groups, each receiving guidance from UiTM students. This collaborative effort aimed to provide hands-on STEM experiences and explore fundamental concepts, fostering interaction between mainstream and PPKI students.

In the initial activity, students participated in the assembly of electronic blocks, benefiting from the guidance of final-year students. This hands-on experience enabled

Participants and teachers from the schools in Sabak Bernam, Selangor after completing the PCB training.



School students attentively listening to the facilitator's explanation on electrical circuits during Kuala Lumpur State Education Department STEM Convention.

students to comprehend electrical circuit basics and experiment with various circuit configurations, showcasing the potential of such activities to nurture curiosity and problem-solving skills.

Subsequently, students were challenged to assemble a solar-powered Autobot, promoting awareness of renewable energy and offering practical insights into the mechanics and environmental benefits of solar power. This activity not only enhanced teamwork skills but also transformed learning into an engaging experience. The assembly of solar robots served as a tangible method to instill environmental responsibility, cultivating a generation knowledgeable about sustainable practices.

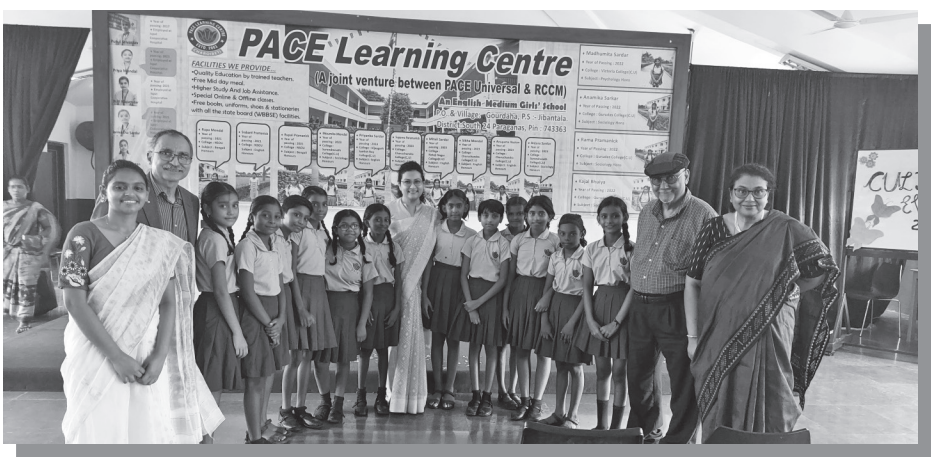
The program's effectiveness in imparting knowledge, enhancing critical thinking, and honing practical skills is evident. Such initiatives play a pivotal role in nurturing a creative and innovative generation with an early interest in STEM fields. Addressing the decline in science stream interest, the program ensures equal opportunities for all students, including those with special needs. By actively involving and inspiring students in STEM subjects from a young age, they are better prepared for future academic pursuits and potential STEM careers. Ultimately, this contributes to an increase in students pursuing STEM-based occupations, significantly advancing the country's progress and development by building a skilled workforce in these domains.

~ Sharma Rao Balakrishnan, Editor

Heritage Institute of Technology-Kolkata, ED15 Student Branch Chapter

By Ayush Kashyap and Mousiki Kar

The IEEE EDS Center of Excellence, Heritage Institute of Technology organized an outreach program on 21 September 2023, at Piyali Learning Center-PACE Universal located at Piyali Junction, a village 30 km outside Kolkata. It is an educational oasis created for underprivileged girls in order to prevent sex trafficking and child marriage which was once rampant in the area. Dr. Mousiki Kar, Coordinator of IEEE EDS Center of Excellence, Heritage Institute of Technology was joined by Dr. Deepa



Group photograph at Piyali Learning Center-PACE Universal during the outreach program on 21 September 2023.

Interactive session with staff and children at Piyali Learning Center-PACE Universal on 10 October 2023.

Willingham, Founder & CEO – PACE Universal, USA, and past president of the Rotary Club of Santa Ynez Valley, California, Prof. Mostafa Mortezaie, Educational Activities Chair in IEEE Region 6, Professor and faculty chair at DeVry University, USA, Prof. Bhaskar Biswas, Senior Professor at Keller School of Management, Sacramento, California and Prof. Iti Saha Misra, Professor at Jadavpur University. This marked the beginning of a long-term relationship of providing educational empowerment through hands-on and activity-based learning leading to engineering studies.

This was followed by a visit to the Piyali Learning Center-PACE Universal on 10 October 2023. Shri Pradip Agarwal, CEO of Heritage Group of Institutions along with Dr. Mousiki Kar, had a productive discussion regarding career counseling and collaborative educational exchanges that can be conducted by the IEEE EDS Center of Excellence, Heritage Institute of Technology for the students and faculty of the school.

~Soumya Pandit, Editor

Regional News

USA, Canada (Regions 1–6, 7)

IEEE Dayton Section STEM Events

—by Ahmad E. Islam

IEEE Dayton section is continuing to organize STEM events on "Introduction to Microfabrication – the enabler for Microelectronics". In 2023, we organized STEM events at different Dayton area high schools and at TechFest (https://www.techfestdayton.org/). The participants of these events obtain a general introduction to microelectronics and microfabrication, and an overview of the OASIS Rapid Certification Program issued by the University of Cincinnati (https://www.credly.com/org/university-of-cincinatti/badge/oasis-rapid-certification). We would like to thank Mrs. Margie Treon and Mrs. Jenny Stammen at Versailles High School, Ms. Stephanie Adams Taylor and Mr. Nick Pant at the Dayton Regional STEM School, and Mr. Adam Ciarlariello at Centerville High School for assisting us with the organization of these events. We will also like to thank the IEEE Electron Device Society for financial support and the speakers: Dr. Katherine Burzynski (AFRL), Dr. Charles Cerny (AFRL), Dr. Ahmad Islam (AFRL), Prof. Ahsan Mian (Wright State University), Prof. Guru Subramanyam (University of Dayton), Prof. Weisong Wang (Wright State University), and Mr. Alexander Grilliot (Wright State University).

—Michael Adachi, Editor

Picture taken during the STEM event at Dayton Regional STEM School.

Electron Devices Society (EDS)—Santa Clara Valley and San Francisco Joint Chapter (SCV/SF) Q3/Q4 2023 Events

—by Imran Bashir (Vice Chair) and Hiu Yung Wong (Chair)

The IEEE Electron Devices Society (EDS) San Francisco / Santa Clara Valley (SCV/SF) joint Chapter hosted a number of seminars from July till Dec 2023 including a very successful two-day workshop on Quantum Computing Devices, Cryogenic Electronics and Packaging. That workshop was organized in collaboration with the IEEE Circuits and Systems Society and Electronics and Packaging Society local chapters. The forum was designed to cover a wide range of topics on various quantum computing modalities, control and readout electronics, and IO and packaging challenges to an electrical engineering audience. Over 20 notable lecturers from academia (San Jose State University, University of Basel, University of Waterloo, UC Santa Barbara) and industry (Quantinuum, Rigetti, Quantum Motion, Equal1, Nexus Photonics, Photonic, Intermodulation Products, NVidia, Forschungszentrum Jülich, Taiwan Semiconductor Research Institute, Politecnico di Milano, MIT Lincoln Laboratory) presented at the workshop. A number of onsite attendees traveled from outside California, Europe, and Southeast Asia. The workshop started with an introduction to quantum computing lecture by Dr. Hiu Yung Wong from San Jose State University. Dr. Kathrin Spendier described the state-of-the-art trapped-ion quantum computing hardware and software solution from Quantinuum and also gave a live demonstration of "TKET" which is an open-source, architecture-agnostic quantum software development kit. Dr. Dominik Zumbühl, Dr. Fernando Zalba, and Dr. Jonathan Baugh covered recent developments in semiconductor qubits. Dr. Daniel Tennant gave an introduction to superconducting qubits and an overview of thermal and cabling challenges in scaling that technology to a large number of qubits. There were a few presentations for cryogenic electronic for quantum control and readout from Dr. René Otten, Dr. Masoud Babaie, Lea Schreckenberg, Chia-Hsin Lee, Alfonso R. Cabrera-Galicia, Michele Castriotta, and Dr. Imran Bashir. Dr. Marina Kudra gave an introduction to Quantum Error Correction and its significance in realizing fault-tolerant quantum computing. Three speakers from NVidia Inc. namely Dr. Jin-Sung Kim, Dr. Azzam Haidar, and Dr. Shinya

Chia-Hsin Lee presenting her work from Taiwan Semiconductor Research Institute during the Quantum Computing Devices, Cryogenic Electronics, and Packaging workshop.

Lea Schreckenberg (left) from Forschungszentrum Jülich receiving a plaque from Dr. Imran Bashir (right).

Morino discussed how to effectively combine future quantum processors with existing classical computing infrastructure and also gave an introduction to cuQuantum SDK. Finally, Dr. Jennifer Smith and Dr. Rabindra Das gave an overview of cabling, IO bottleneck and packaging challenges and their potential solutions for scaling large-scale quantum processors. The hybrid event was held at SEMI World Headquarters in Milpitas, CA (near San Jose) and was attended by 48 IEEE members and 72 non-IEEE members. Also, two lucky attendees walked away with a high-end Nvidia GTX graphic card given as a raffle prize. The details of the event and the lecture recordings can be found on IEEE TV and the following link: https://attend.ieee.org/qc-dcep/program. Plans are underway to host a similar workshop this year. So, stay tuned!

In addition to the aforementioned workshop, the EDS SF/SCV chapter hosted Dr. Eric Pop from Stanford University on 28 July for a lecture titled "What Are 2D Materials Good For?" Dr. Pop discussed useful applications of 2D materials including 3D heterogeneous integration of electronics for energy-efficient computing. The lecture also covered some unconventional applications such as thermal insulators to control heat in "thermal circuits" analogous to electrical circuits. The online event was attended by 16 IEEE and 15 non-IEEE members. On Friday, 20 October 2023, Dr. Meenakshi Singh gave a webinar titled "Investigating Quantum Speed Limits with Superconducting Qubits." In her lecture, Dr. Singh experimentally demonstrated the speed limit of entanglement between two superconducting transmon qubits. She also proposed how that limit can be increased by introducing additional transmon and the implications for large-scale quantum computing. Lastly, EDS SF/SCV collaborated with Dr. Wladek Grabinski to organize a multi-distinguished lecturer hybrid event titled "MOS-AK Workshop" held at the Keysight Technologies campus in Santa Clara, CA on 13 December 2023. The theme for the workshop was Compact/SPICE models of circuit elements using nano-scale semiconductor technologies. The agenda also included a discussion on applications of FOSS TCAD tools such as Cogenda TCAD and DEVSIM, model implementation, and Verilog-A standardization. Two of the talks were also the DL talks of the Chapter. They were "European Open Source PDK Initiative Technology – Devices – Applications" by Dr. Wladek Grabinski and "Some efforts toward the modeling of integrated antennas" by Dr. Roberto S. Murphy.

Please visit our website @ https://site.ieee.org/scv-eds/ and join the email list to receive notification of current and future events and instructions on joining remotely through Zoom.

~Larry Larson, Editor

Latin America (Region 9)

EDS Puebla Chapter

IEEE Latin American Electron Devices Conference 2023 (LAEDC2023)

—by Joel Molina-Reyes

On 3–5 July 2023, the fifth IEEE Latin American Electron Devices Conference 2023 (https://attend.ieee.org/laedc-2023/) was held in Puebla, Mexico where students (undergraduate and graduate levels) and professionals on electron devices from many Latin American countries, attended in-person or via virtual sessions.

LAEDC2023 offered truly interesting and diverse talks as well as activities on topics related to electron devices so that all of the attendees could see the advances and hot research topics that some of these technologies have reached up to now. Some of the covered topics were:

Keynote speakers of the IEEE Latin American Electron Devices Conference 2023.

- All electron-based devices
- Electron Devices for Quantum Computing
- RF-MMW-5G
- Semiconductor-, MEMS- and Nanotechnologies
- Packaging, 3D integration
- Sensors and actuators
- Display technology
- Modeling and simulation
- Reliability and yield
- Device characterization
- Agrivoltaics
- Flexible electronics
- Biomedical Devices
- Circuit-device interaction
- Novel materials and process modules
- Technology roadmaps
- Electron device engineering education
- Optoelectronics, photovoltaic and photonic devices and systems
- Energy harvesting
- 2D Materials and Devices

Six keynote talks were delivered during the conference:

- "Recent developments and future trends in solar photovoltaics," by Martin Green.
- "Wide band gap technology: state-of-the-art and problems to solve," by Michael Shur.
- "75th anniversary of the transistor," by Fernando Guarin.
- "Agribusiness impact on climate change," by Victor Grimblatt.
- "Pandemics, migration and climate change," by Luis Kun.
- "Hunting a supermassive black-hole in the center of the Milky Way with the EHT," by David Huges.

During this event, special sessions also took place, offering plenty of options to all the attendees:

- EDS Summer School: Design, Characterization, and Fabrication of Sensors and ICs
- Women In Engineering / Young Professional: The Role of Women in STEAM Fields
- EDS Mini Colloquium: Technical Talks delivered by EDS Distinguished Lecturers
- MOS-AK Workshop: Enabling Compact Modeling R&D Exchange
- IEEE Humanitarian Technology Session
- Special Local Session: Ingeniería Abierta para la Ciudadanía

LAEDC2024 will be held at Guatemala City by 8-10 May, where all the sessions and research topics on electron devices are expected to reach out to our vibrant Latin American community again: https://attend.ieee.org/laedc-2024/

~Joel Molina-Reyes, Editor

IngenIEEEría Costa Rica

EDS Mini Colloquium Costa Rica 2023 Special celebration: 75th anniversary of the invention of the transistor

—by Esteban Arias Méndez

Snapshot of celebration of the 75th Anniversary of Transistor by IEEE Costa Rica Section and EDS Costa Rica Chapter.

Engineering stands as a driving force in the economic development of nations, employing science and technology to elevate infrastructure and enhance quality of life. As society reaps the rewards of advancements in science and technology, the inaugural IngenIEEEría Costa Rica event aimed to shed light on the latest breakthroughs in modern electronic devices, coinciding with commemorating the transistor's 75th anniversary.

In the pivotal years of 1947-1948, scientists at Bell Labs achieved a groundbreaking feat—the creation of the first functional transistor. Walter Brattain and John Bardeen developed the point-contact transistor on 16 December 1947, while William Shockley presented the junction transistor in January 1948. Tasked with replacing vacuum tubes, this innovation stands as a monumental achievement in semiconductor technology, acknowledged with the Nobel Prize in Physics in 1956 for its transformative impact on electronic devices.

The **IEEE Costa Rica Section**, in collaboration with the **EDS Costa Rica Chapter**, celebrated the 75th anniversary of the transistor on 7 September 2023 at the Instituto Tecnológico de Costa Rica in Cartago and on 8 September at the National Council of Rectors (CONARE) Auditorium in San José.

The inclusive gatherings offered free registration and admission, facilitating participation in cutting-edge discussions presented in both Spanish and English. Thursday featured a morning coffee break with sandwiches, fruits, and lunch. The hospitality extended on Friday with a morning coffee break, lunch, afternoon coffee break, and a closing cocktail with snacks. For remote participants, the main event was broadcast live via Facebook Live on the IEEE Costa Rica Section page, broadening the celebration's reach.

The event commenced with a presentation by the EDS Costa Rica Chapter Chair, M.Sc. Esteban Arias-Méndez. Subsequently, our distinguished speakers: Dr. Fernando Guarín, Dr. Anirban Bandyopadhyay, Dr. Edmundo Gutiérrez, Dr. Mukta Farooq, and Dr. Alba Ávila, enriched the occasion with their knowledge. The celebration culminated with a symbolic 75th-anniversary cake on both days, marking a triumphant and enlightening occasion for all immersed in electronics and technology.

For more information about the sessions, visit [https://www.facebook.com/ieeecostarica]

~Joel Molina-Reyes, Editor

Centro Universitario FEI ED Student Branch Chapter

—by Marcelo Antonio Pavanello and Michelly de Souza

The 2023 EDS Brazil Mini Colloquium and 37th Symposium on Microelectronics Technology and Devices – SBMicro2023

On 28 August 2023, the Centro Universitario FEI ED Student Branch Chapter organized the 2023 EDS Brazil Mini-Colloquium, which was the first in-person event after the outbreak, held in Rio de Janeiro. It is an annual

Dr. Adam Skorek's Distinguished Lecture at the 2023 EDS Brazil MQ; Dr. Skorek's photo in the inset.

Opening Session of SBMicro2023

event that precedes the Symposium on Microelectronics Technology and Devices. This year's Mini-Colloquium consisted of four presentations given by EDS Distinguished Lecturers, covering state-of-art topics in micro/nanoelectronics:

- Dr. Frank Schwierz (DL from EDS), from the Technische Universität Ilmenau, Germany, "2D Materials and their Role in Future Electronics";
- Dr. Adam Skorek (DL from EDS), from the University of Québec, Canada, "High-Performance Quantum Computing in Nanoelectronics";
- Dr. Edmundo Gutierrez (DL from EDS), from National Institute for Astrophysics, Optics and Electronics, Mexico, "From micro-semiconductor devices to the discovery of the black hole in the Milky Way";
- Dr. Andreas Kerber (DL from EDS), from Intel, USA, "Reliability of Metal Gate / High-K CMOS devices".

Every presentation of the Mini-Colloquium received more than 60 participants, from undergraduate and graduate students as well as professors and researchers.

After the Mini-Colloquium, the 37th Symposium on Microelectronics Technology and Devices – SBMicro2023 was held from 29 August to 1 September. SBMicro is the largest conference in Latin America in the field of micro/nanoelectronics, covering topics such as fabrication technology, sensors, modeling, device characterization, and photonics. This year, 55 papers were selected by the program committee to be presented orally. The Symposium included four invited presentations: Andreas Kerber (Intel), Frank Schwierz (Technische Universität Ilmenau), and Edmundo Gutierrez (National Institute for Astrophysics, Optics and Electronics). About 250 people registered for the conference this year. The conference is technically co-sponsored by the IEEE EDS and its proceedings are available at IEEE Xplore.

~Paula Agopian, Editor

Asia & Pacific (Region 10)

EDS Peking University Chapter

—by Bingrui Song

On 25 December 2023, the Peking University Chapter organized an EDS Distinguished Lecture in Beijing, China. Professor Xing Zhou from Nanyang Technological University in Singapore was invited to deliver a presentation entitled "Compacting Models: The Art of Compact Modeling." During the lecture, Professor Zhou provided

EDS Distinguished Lecture of Prof. Xing Zhou organized by EDS Peking University Chapter.

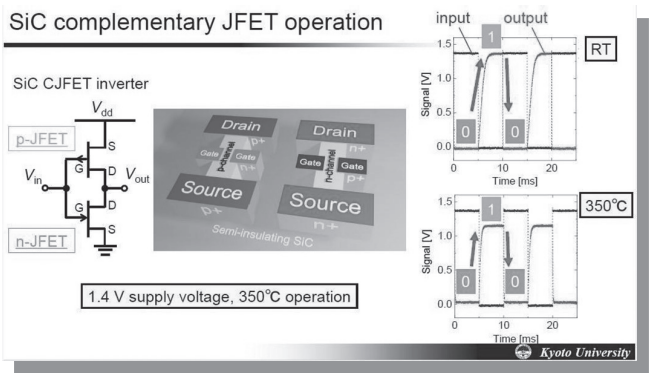
an overview of compact modeling and discussed the motivation behind MOS model unification. Additionally, he introduced various compact modeling approaches and formulations. Subsequently, he presented the Unified Regional Modeling (URM) approach for bulk/SOI and DG/NW MOSFETs modeling. Finally, Dr. Zhou extended the model to GaN HEMT devices. His lecture gathered over 20 students and faculty members.

EDS Kansai Chapter

—by Tokiyoshi Matsuda

EDS Kansai Colloquium

We successfully organized the 23rd "Kansai Colloquium on Electronic Devices Workshop," featuring papers selected by researchers in the Kansai region and neighboring areas. These papers were presented in Japanese, covering the same content as the original submissions. This year's workshop, conducted online, continued the trend from the past two years. The sessions focused on "Power and Compound Semiconductor Devices", "CMOS Process, Device, and Circuit", and "Optoelectronics, Displays, and Imagers". Out of 67 papers submitted from the Kansai region, the committee meticulously reviewed and selected 9 presentations.



SiC CMOS inverter circuit and output signal obtained at RT and 623 K.

Dr. Kaneko was honored with the Best Paper Award for his presentation on "SiC Complementary Junction Field-Effect Transistor Logic Gate Operation at 623 K, IEEE EDL, vol. 43, no. 7, pp. 997-1000 (2022)". The figure above illustrates the SiC CJFET inverter structure and output signal obtained at both room temperature (RT) and 623 K. Additionally, the Student Paper Award (MFSK Award) was presented to Dr. Matsumoto for the paper titled "Switched-Capacitor Voltage Boost Converter with Digital Maximum Power Point Tracking for Low-Voltage Energy Harvesting, Extend. Abstr. SSDM 2022, K-9-07, pp. 800-801, (2022)". We are looking forward to advancing technology with more innovations in the coming years.

EDS NCTU Student Branch Chapter

—by Ming-Chun Hong

An invited hybrid seminar, "*In search of industry-compatible deposition approaches for highly crystalline TMD materials,*" was co-organized by Taiwan Semiconductor Research Institute and EDS NCTU Student Branch Chapter on 8 November 2023. Dr. Benjamin Groven was invited to share his experience and research findings in

Dr. Benjamin Groven and the audience during the seminar "In search of industry-compatible deposition approaches for highly crystalline TMD materials".

developing deposition techniques for large-area transition metal dichalcogenides (TMD) channel materials on 200 mm and 300 mm wafers. Dr. Groven is a research scientist in the "Advanced Channels" group at the R&D hub for nano- and digital technologies, imec. In his talk, Dr. Groven emphasized the importance of aligning with industrial deposition chemistry and proposed CVD principles for large-scale TMD monolayer production. He addressed challenges such as MOCVD oversaturation during TMD growth and introduced a surface-smoothing technique. This presentation gave us a deep understanding of large-area TMD monolayer preparation methods and related optimizations. We look forward to seeing the widespread application of these research findings and their contribution to innovation and progress in semiconductor technology.

~Tuo-Hung Hou, Editor

ED Indonesia Chapter

Distinguished Lecture by Dr. MK Radhakrishnan

—by Basuki Rachmatul Alam

The ED Indonesia Chapter organized a Distinguished Lecture (DL) featuring Dr. MK Radhakrishnan, titled "Semiconductor Device Evolution in the Last 120 Years." The event took place on 6 November 2023, at the auditorium of the Technopreneur Building in the State Polytechnics of Batam campus, Batam Island, Indonesia. The DL was conducted in-person and attracted a strong attendance of 51 participants.

This lecture coincided with the 75th anniversary of the invention of the transistor, and Dr. MK Radhakrishnan

Participants of Dr. MK Radhakrishnan's Distinguished Lecture. The Lecturer is sitting behind the table (2nd from the left).

Picture of 2023 IEEE RSM conference's committee members and some of participants during the conference day.

delivered insights on the evolution of semiconductor devices over the past 120 years. He highlighted the significance of the invention and patents of the solid-state diode by JC Bose in 1901. However, the pivotal moment in semiconductor device technology occurred with the invention of the transistor in 1947 by Nobel Prize winners William Shockley, John Bardeen, and Walter Brattain.

Dr. Radhakrishnan's lecture comprehensively and thoroughly entertained the audience, providing an overview of the remarkable journey from the early inventions of semiconductor devices to the current complexities of semiconductor integrated circuits (ICs). He emphasized how advancements in IC technology have played a crucial role in the widespread applications of global social media in the present millennium. Furthermore, these advancements have paved the way for upcoming technologies such as AI, VR, Augmented Reality, Cloud Computing, Quantum Computing, and neuromorphic technology.

The talk significantly broadened the knowledge of the DL audience, primarily consisting of students enrolled in the manufacturing electronics program of the Electrical Engineering Department. Additionally, some attendees were employees of electronic industries in Batam, further emphasizing the practical relevance of the lecture in the context of contemporary technological advancements.

ED Malaysia Chapter

2023 IEEE Conference Regional Symposium on Micro and Nanoelectronics (RSM)

—by Hazian Mamat and Nurul Ezaila Alias

The 14th RSM Conference, organized by the ED Malaysia, was successfully held on 28-29 August 2023, at Holiday Villa Langkawi, Malaysia. This conference, the 14th in its series, was orchestrated by the Electron Devices Chapter of the IEEE Malaysia Section and received technical co-sponsorship from the IEEE Electron Devices Society.

Throughout the past three decades, the RSM conference series has evolved into a leading international platform for semiconductor electronics, covering all facets of semiconductor technology across four main clusters: Devices, Nanophotonic, IC Design and Manufacturing, and Material, Process, and Products. The two-day conference featured 38 oral presentations spanning various technical sessions, including insights from three keynote speakers: Dato Prof. Dr. Zaliman Sauli (UNIMAP), Prof. Dr. Azrul Azlan Hamzah (UKM), and Dr. Yik Yee Tan (YOLE Group). In commemoration of the 75th year of the Transistor, special topics about the Transistor's roadmap were delivered by the keynote speakers.

Taking place in Langkawi, Malaysia's premier tourist attraction, participants had the unique opportunity to delve into the rich culture of Langkawi during breaks. Nearby attractions such as the Skybridge and the Seven Wells Waterfall offered breathtaking views and memorable experiences. The vibrant night markets showcased local cuisine, adding a flavorful touch to the event. As organizers, we ensured a seamless integration of the conference with the island's attractions, fostering an environment where learning and leisure harmoniously coexisted. The juxtaposition of academic discussions against the backdrop of Langkawi's natural wonders made this RSM conference an unforgettable experience.

2023 IEEE EDS Malaysia Chapter Mini-Colloquium

—by Hazian Mamat and Nurul Ezaila Alias

The IEEE EDS Mini-Colloquium 2023, held on 29 August at Holiday Villa Langkawi, Malaysia, marked a successful event. Coinciding with the 75th-year celebration of the Transistor, this Mini-Colloquium, organized by ED Malaysia, proved to be a resounding success, bringing together academic minds and fostering insightful

Picture of IEEE EDS Malaysia Mini-Colloquium with the lineup of distinguished speakers (Prof. Mayank Shrivastava, attending in-person, 4th from left) with IEEE EDS Malaysia Chair and Executive Committee members. Some of the participants won lucky draw presents prepared by IEEE EDS ExCom.

discussions. Centered around the theme of 2D Materials, the colloquium featured distinguished speakers, including Prof. Francesca Lacopi from the University of Technology Sydney, Prof. Nowshad Amin from the University of Chittagong, and Prof. Mayank Shrivastava from the University of Bangalore. Their presentations elevated the colloquium to new heights.

Prof. Francesca Lacopi captivated the audience with her presentation on "Graphene on Cubic Silicon Carbide: Integrated Functionalities on Silicon." Her expertise shed light on the integration of graphene with silicon carbide, offering insights into the potential for enhanced functionalities on silicon substrates. This topic sparked engaging discussions and paved the way for a deeper understanding of advanced materials.

Prof. Nowshad Amin shared the success story of "Thin Film Photovoltaics: Success Story of Cadmium Telluride Thin Film PV." Hailing from the University of Chittagong, his presentation not only highlighted achievements in thin film photovoltaics but also underscored the importance of sustainable energy solutions. Attendees gained valuable perspectives on advancements in solar technology and its impact on the renewable energy landscape.

Prof. Mayank Shrivastava, representing the University of Bangalore, presented a roadmap for "Disruptive Applications and Heterogeneous Integration Using Two-Dimensional Materials: State-of-the-Art and Technological Challenges." His comprehensive overview navigated through the current state of two-dimensional materials, outlining a roadmap for disruptive applications and addressing technological challenges in heterogeneous integration. The presentation sparked enthusiasm among participants and opened avenues for future exploration in the field.

Beyond the academic presentations, the success of the mini-colloquium extended to fostering networking and collaboration prospects among attendees. With more than 60 participants joining the event (40 in-person and 20 online), the combination of insightful presentations and engaging discussions made this EDS Malaysia-organized event a standout success, leaving participants enriched with knowledge and inspired by the forefront of research in materials science and technology.

IEEE EDS Malaysia Distinguished Lecture Series 2023 at Universiti Putra Malaysia

—by Haslina Jaafar and Nurul Ezaila Alias

The 2023 edition of the Distinguished Lecture Series, organized by the ED Malaysia, showcased a captivating presentation titled "Multifunctional Materials for Emerging Technologies" by Prof. Dr. Federico Rosei. The event unfolded on 4 October 2023, from 10:00 am to 12:00 pm (MYT) at Thinker Space 2.0, situated within the Faculty of Engineering at University Putra Malaysia (UPM). Drawing an audience of approximately 25 participants, including lecturers, postgraduate, and undergraduate students from UPM's Faculty of Engineering, the event was conducted both physically and through an online platform to facilitate broader participation.

Prof. Federico Rosei, a distinguished expert from the Centre for Energy, Materials, and Telecommunications at Institut National de la Recherche Scientifique in Varennes, Canada, delivered an insightful talk on "Multifunctional Materials for Emerging Technologies." His presentation explored cutting-edge materials with versatile functionalities, showcasing their immense potential in advancing emerging technologies. The lecture captivated the audience, garnering positive feedback for its interesting and informative content.

In addition to the enlightening presentation, Prof. Federico Rosei took the opportunity to promote the IEEE Electron Devices Society, emphasizing the benefits of membership. He encouraged attendees to become

Distinguished Lecture by Prof. Dr. Federico Rosei

active members, emphasizing the valuable resources and networking opportunities the society provides.

The event proved to be both successful and enriching, combining a distinguished speaker, engaging content, and active audience participation. Beyond expanding the knowledge base of the attendees, the event served as a platform for networking and professional development.

Sitting (from left): Dr. A. Hossain (faculty), Dr. T. R. Lenka (Chapter Advisor), Prof. R. H. Laskar (Head of Department, ECE), Prof. Dragana Krstic, Prof. Nenad Milosevic; standing: Dr. D. S. Gurjar and faculty colleagues, and EDS Student Members.

IEEE EDS Technical Webinar

—by Zurita Zulkifli and Nafarizal Nayan

The IEEE EDS Malaysia Chapter successfully hosted a Professional Talk titled "Recent Progress of GaN Semiconductor Research for Power Electronic Applications in Malaysia" via the Google Meet platform on 28 November 2023. The webinar garnered active participation from 59 attendees, representing a diverse range of backgrounds, including students, industry practitioners, lecturers, and researchers.

The featured speaker, Ts Dr. Mohd Rofei Mat Hussin, a Staff Engineer at MIMOS Berhad, delivered a comprehensive 1-hour and 30-minute presentation, providing valuable insights into the ongoing research on GaN semiconductor applications in power electronics. The talk also delved into the research and development (R&D) infrastructure at MIMOS Berhad, with a special focus on the GaN reactor, set to be operational in Q2 of 2024. The GaN reactor is poised to bring significant advantages, including cost-effectiveness, high flexibility in process capability, and a quicker time to market.

Throughout the webinar, participants gained exposure to the advantages of GaN in the electronics industry and explored its diverse applications. The audience actively engaged in the session, posing relevant questions to the speaker. The positive feedback received from participants reflects the success of the webinar in effectively disseminating knowledge and fostering meaningful interactions within the community.

~Sharma Rao Balakrishnan, Editor

National Institute of Technology—Silchar, ED15 Student Branch Chapter

—by Trupti Lenka

IEEE ED NIT Silchar Student Branch Chapter, Assam, India in association with IEEE Nanotechnology Council Chapter, and IEEE Silchar Sub-Section organized a seminar on 8 December 2023. The event comprised two invited talks, delivered by Prof. Nenad Milosevic and Prof. Dragana Krstic, both from the Faculty of Electronic Engineering, University of Nis, Serbia. The talks were attended by more than 50 participants, including students and faculty members. On 13 December 2023, the chapter also celebrated the 75 Anniversary of Transistor.

Heritage Institute of Technology—Kolkata, ED15 Student Branch Chapter

—by Ayush Kashyap and Mousiki Kar

The Heritage Institute of Technology - Kolkata ED Student Branch Chapter (HITK SBC), in association with IEEE EDS Center of Excellence, organized a practical hands-on ***Electronic Product Design Workshop*** for undergraduate students running through August and September 2023. The Workshop consisted of eight two-hour sessions where the students were trained to build market-ready products starting from discrete circuit components. The sessions were conducted by Dr. Atanu Kundu, Advisor of the IEEE EDS HITK SBC. A total of 18 students participated in the workshop. An interactive session on "Sustainable Development through Humanitarian Technology" was organized on 3 October 2023. Prof. Mostafa Mortezaie, IEEE Region 6, Educational Activities Chair and Professor at San Jose State University and DeVry University, USA interacted with engineering undergraduate students. He discussed various IEEE global humanitarian grants that students can obtain to participate in humanitarian activities. Globally implemented projects were discussed to help the students write their project proposals. The participants got an overview of the entire lifecycle of a humanitarian project that is executed under the aegis of IEEE HTB (Humanitarian Technologies Board) or IEEE SIGHT (Special Interest Group on Humanitarian Technology). The session was attended by 23 participants. A seminar on the topic "Innovative MEMS Technology: A Designer's Perspective" was organized on 16 January 2024, at Heritage Institute of Technology - Kolkata. The speaker was Mr. Akash

Group photo of participants of the IEEE seminar on "Innovative MEMS Technology: A Designer's Perspective," Heritage Institute of Technology - Kolkata, 16 January 2024.

Roy, an alumnus of HITK who is pursuing his PhD from the University of Southern California in Los Angeles where he is a PhD scholar at the Micro Electromechanical Systems (MEMS) Lab. Mr. Roy spoke about his work in areas such as MEMS Microphones, Acoustic Tweezers, and Single Focused Acoustic Transducers (SFAT). The event was attended by 50 academicians, professionals, and students from across the state of West Bengal.

ED University of Calcutta Student Branch Chapter
—by Koyel Mukherjee and Uday Sannigrahi

The chapter and the IEEE Photonics Society Calcutta University (CU) Student Branch Chapter (SBC) organized jointly a Career Fair. The event was organized in collaboration with the IEEE APS CU SBC, the IEEE Photonics Society Kolkata Chapter, the IEEE MTT CU SBC, the Astronova Club, and the AI and Robotics Club. The Career Fair, held from 11 to 12 October 2023, aimed to create a platform that brings together esteemed professionals and experts from various industries to share their invaluable experiences, insights, and knowledge regarding the latest trends, opportunities, and challenges within their respective fields. The tagline for the event was "Future Focus: Illuminate Your Career". Each session lasted 1 hour, including an interactive Q&A part, allowing students to have direct contact with the speakers. Mrs. Koyal Mukherjee expertly anchored the event under the supervision of Dr. Shampa Guin, Assistant Professor at the Institute of Radio Physics and Electronics. Each speaker was honored with a flower bouquet and a specially designed memento as a token of gratitude for their valuable contributions. The Fair was executed with remarkable efficiency under the able leadership of Mr. Suman Dey and Mr. Sayanhodeep Banerjee, encapsulating the spirit of the Career Fair's tagline "Future Focus: Illuminate Your Career." Here are some snapshots from the event.

Mr. Debojyoti Choudhuri of HCL Pvt. Ltd. shared insights into modern antenna design techniques, delving into theoretical aspects and the role of smart antennas and radars in contemporary applications. He also shed light on the design of cellular antennas by various companies, offering guidance to students seeking to venture into this industry. Basudeb Gangopadhyay from ITOrizin Technology Solutions Pvt. Ltd. delivered a vivid and interactive session on cybersecurity. He emphasized the growing importance of cybersecurity in our technology-dependent lives and explored the various threats and security vulnerabilities in current IT and internet systems. Moreover, he highlighted the training opportunities their institute offers, acknowledging the increasing job prospects in the cybersecurity domain. Dr. Anupam Dutta, a Senior Member of the Technical Staff of GlobalFoundries, provided insights into the world of chips and circuits used in modern cell

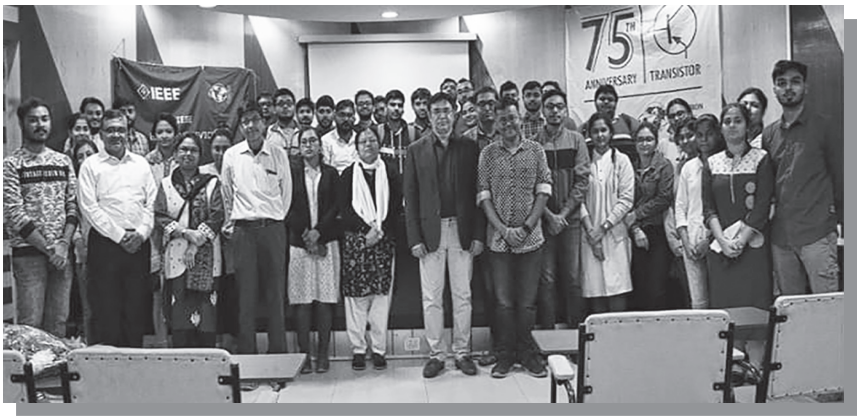
Participants of the Career Fair "Future Focus: Illuminate Your Career".

phones and AI-powered devices. Dr. Dutta elucidated how GlobalFoundries is pioneering the development of smaller chips using their proprietary technologies. Mr. Swagatam Das, a distinguished scientist associated with TCG CREST, delivered an engaging lecture on AI, focusing on contemporary trends such as generative AI and the BERT model. He provided a clear overview of AI's evolution, from perceptrons to multilayer neural networks and the research facilities at TCG Crest. Mr. Bhaskar Mukherjee, the Head of Enterprise Application Competency within the Service Delivery Unit at Ericsson, India, offered an illuminating presentation on modern telecommunication technologies. He explored ongoing research in the realm of 5G and the upcoming 6G communication, providing students with valuable insights into preparing for careers in telecommunication. Mr. Sourav Mitra, Joint Director of C-DAC, Kolkata, shared insights into various cybersecurity-related projects and initiatives undertaken by C-DAC. He underscored the critical importance of cybersecurity in the modern era, elucidating government-funded projects and outlining the challenges and AI-driven solutions within the field. As the second day of the Career Fair drew to a close, attendees were privileged to partake in a captivating 30-minute IEEE student membership-drive session

Commemorating the 75th Anniversary of the Transistor, the chapter organized an EDS Distinguished Lecture on "Wireless Connectivity for the Next Decade - Bridging the Digital Divide". The speaker was Dr. Anirban Bandyopadhyay, Senior Director and head of Strategic Applications within the Smart Mobile Devices and Wearables business unit of GlobalFoundries, USA. Dr. Bandopadhyay elaborated on the fundamentals of wireless communication as well as on the recent trends. The phenomenal implications of wireless communication for societal applications, especially in digital learning and remote health monitoring systems, were highlighted. The talk was attended by more than 50 student members and a few faculty members.

The chapter organized the A. K. Chowdhury Centenary Memorial Workshop on 13 December 2023. The reminiscences of Prof. A. K. Chowdhury were discussed by Prof. Bhabani P. Sinha, IEEE Fellow, formerly with Indian Statistical Institute, Kolkata. Dr. Angshuman Chakraborty, CDAC Kolkata, presented a talk on "Using Deep Learning and Robotic Operating System (ROS) to Tackle Challenges in Robotics". Prof. Bhargab B. Bhattacharya, IEEE Fellow, formerly with Indian Statistical Institute, Kolkata delivered a talk on "From Integrated Circuits to Lab-on-Chips: A New Revolution in the Offing". Prof. Sajal K. Das, IEEE Fellow, Missouri University of Science and Technology, USA delivered a talk on 'Machine Learning over Internet of Things". A hands-on session dedicated to COMSOL simulation software was also organized during the workshop.

The chapter financially co-sponsored the 8th International Conference on Computers and Devices for Communication (CODEC-2023) which was held on 14–16 December 2023. The conference is a flagship technical event of the Institute of Radio Physics and Electronics, University of Calcutta. The conference started with an Inaugural Session in the prestigious Vivekananda Hall of the Ramakrishna Mission Institute of Culture, Golpark which



DL talk by Dr. Anirban Bandyopadhyay.

Group photo of CODEC-2023 participants.

was addressed by Swami Suparnanada Maharaj among others. The technical session started with a plenary talk by Dr. Anirban Bandyopadhyay of GlobalFoundries, USA. It was followed by 15 invited talks and 28 contributing papers. The program of the second day started with a plenary talk by Prof. Sajal K. Das, Missouri University of Science and Technology, USA followed by 15 invited and 31 contributing papers. At the end of the day, there was a cultural program followed by the Conference Dinner. On the third day of the conference, there were 2 plenary talks delivered by Prof. Nuno B. Carvalho, University de Aveiro, Portugal, and Dr. Debabani Choudhury, Intel Corporation, USA. This was a special session organized jointly with IEEE APS/MTTS. This was followed by 6 invited and 26 contributory papers. The other important feature of the last day was a poster session with 32 papers. After a proper evaluation, the CODEC-2023 committee awarded the best track papers. The IEEE WiE, Kolkata Section evaluated the poster papers. The authors of the awarded papers received the awards during the valedictory session. The awards for the best papers were sponsored by IEEE EDS Kolkata Chapter, TechLabs, and Monorama Enterprise. The papers accepted and presented at the conference will be uploaded for possible inclusion in IEEE Xplore.

~Soumya Pandit, Editor

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2024 25th International Symposium on Quality Electronic Design (ISQED)	03 Apr – 05 Apr 2024	San Francisco, CA
2024 IEEE International Reliability Physics Symposium (IRPS)	14 Apr – 18 Apr 2024	Grapevine, TX
2024 IEEE 36th International Conference on Microelectronic Test Structures (ICMTS)	15 Apr – 18 Apr 2024	Edinburgh, United Kingdom
2024 International VLSI Symposium on Technology, Systems and Applications (VLSI TSA)	22 Apr – 25 Apr 2024	Hsinchu, Taiwan
2024 Joint International Vacuum Electronics Conference and International Vacuum Electron Sources Conference (IVEC + IVESC)	23 Apr – 25 Apr 2024	Monterey, CA
2024 IEEE Latin American Electron Devices Conference (LAEDC)	02 May – 04 May 2024	Guatemala City, Guatemala
2024 International EOS/ESD Symposium on Design and System (IEDS)	08 May – 10 May 2024	Hangzhou, China
2024 IEEE International Memory Workshop (IMW)	12 May - 15 May 2024	Seoul, Korea (South)
2024 35th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC)	13 May – 16 May 2024	Albany, NY
2024 36th International Symposium on Power Semiconductor Devices and ICs (ISPSD)	02 Jun – 06 Jun 2024	Bremen, Germany
2024 IEEE International Interconnect Technology Conference (IITC)	03 Jun – 06 Jun 2024	San Jose, CA

2024 IEEE 52nd Photovoltaic Specialist Conference (PVSC)	09 Jun – 14 Jun 2024	Seattle, WA
2024 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)	16 Jun – 18 Jun 2024	Washington, DC
2024 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)	16 Jun – 20 Jun 2024	Honolulu, HI
2024 Device Research Conference (DRC)	24 Jun – 26 Jun 2024	College Park, MD
2024 25th International Microwave and Radar Conference (MIKON)	01 Jul – 04 Jul 2024	Wroclaw, Poland
2024 31st International Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD)	02 Jul – 05 Jul 2024	Kyoto, Japan
2024 IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)	15 Jul – 18 Jul 2024	Singapore, Singapore
2024 IEEE European Solid-State Electronics Research Conference (ESSERC)	09 Sept - 12 Sept 2024	Bruges, Belgium
2024 IEEE International Flexible Electronics Technology Conference (IFETC)	15 Sept – 18 Sept 2024	Bologna, Italy
2024 19th European Microwave Integrated Circuits Conference (EuMIC)	23 Sept – 24 Sept 2024	Paris, France
2024 IEEE Region 10 Symposium (TENSYMP)	27 Sept – 29 Sept 2024	New Delhi, India
2024 International Semiconductor Conference (CAS)	09 Oct – 11 Oct 2024	Sinaia, Romania
2024 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)	27 Oct – 30 Oct 2024	Fort Lauderdale, FL
2024 IEEE 11th Workshop on Wide Bandgap Power Devices & Applications (WiPDA)	04 Nov – 06 Nov 2024	Dayton, OH
2024 IEEE International Electron Devices Meeting (IEDM)	07 Dec – 11 Dec 2024	San Francisco, CA
2024 IEEE 55th Semiconductor Interface Specialists Conference (SISC)	14 Dec – 18 Dec 2024	San Diego, CA

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- Advanced CMOS Platforms, Interconnect and Backside Power Delivery Network (BSPDN) Technologies
- Advanced Packaging, Chiplet and Heterogeneous Integration Technologies Including 2.5D and 3D
- Analog and Mixed-Signal Circuits
- Beyond CMOS Devices That Utilize New Physics Including Spin, Optical and Quantum Computing
- Biomedical Devices, Circuits, and Systems
- Data Converters
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- Devices and Accelerators For ML/DL and New Compute
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- Workshops
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Prospective authors are invited to submit two-page extended abstracts to www.vlsisymposium.org. Accepted papers will be published as submitted, with no revisions permitted. Authors must follow detailed instructions provided within the "Authors" section of the website, including the Authors' Guide and Pre-publication Policy.

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Topics

Materials will include advanced thin-films and their interfaces, as well as nanomaterials (nanowires, nanotubes, 2D materials and their combination). Manufacturing platforms will include wafer-level, roll-to-roll as well as direct-write and additive technologies. Processing techniques will also be incorporated that can hone materials' properties to an optimal performance for designated applications. Aspects of interest also include advances in scalability, large-scale structuring and patterning, robustness and control of interfaces, integrated performance and reliability, and related novel metrics, while keeping an eye out for long-term sustainability of large-scale deployment in semiconductor manufacturing.

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