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Technical Briefs

Marvels in Microelectronic Devices Structure: Actuate, Isolate and Interconnect

by Simon Deleonibus, Past Chief Scientist, CEA,LETI

Looking for the Holy Grail device having the lowest parasitics, the highest performance and the lowest leakage current has been the rule of the game for microelectronics since Large Scale Integration (LSI) offered the possibility to design complex circuits for digital and mixed signals applications. In their time, groundbreaking ideas to actuate, isolate and interconnect all devices with the smallest footprint possible have been proposed. Among these, channel/substrate engineering with Silicon on Insulator (SOI), Local Oxidation of Silicon (LOCOS) and Shallow Trench Isolation (STI), and copper interconnects have been developed worldwide, as breakthroughs in high risk/high gain projects pushed by highly talented teams and their charismatic leaders.

The attractiveness of SOI was put forward for its unbeatable isolation capabilities and low junction capacitance, especially for power, radio frequency or rad-hard applications. Initially considered as restricted to niche applications, SOI is nowadays considered a mainstream substrate, a must for RF and Low Power applications and is a candidate to replace bulk Si in the high performance market.

SOI was first mentioned in the 1960s during the search of epitaxially grown Silicon on Sapphire (SOS), which was supposed to "almost" epitaxially match perfectly with Si (100). The "almost" was actually a best case 7% crystallographic strain mismatch, thus thermal mismatches, between Si and sapphire induced a substantial number of crystallographic defects, such as threading dislocations (10^6–10^7/cm^2) [1].

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Marvels in Microelectronic Devices Structure: Actuate, Isolate and Interconnect

(continued from page 1)

The first demonstration of SOS was made in 1968 by HM Manasevit and WI.I. Simpson at North American Aviation, Inc., later on known as North American Rockwell Corp. [2], [3]. Following a decomposition of SiCl4 by H2 at 1250 °C, the substrate was reduced by Si. Further coalescence of the reacting Si atoms occurred on the surface of alpha alumina.

Jean Pierre Colinge, 2012 IEEE A. Grove Award recipient, now with CEA, LETI, reports: "In the early 1980's, the only proven SOI technology was SOS (Silicon on Sapphire), which was used in military/aerospace applications because of its resistance to radiation, and in some Hewlett-Packard computers, the 1000 Series processor in the L-Series computers introduced in 1979 [6]. SOS technology was, however, clearly unsuitable for 3D monolithic integration, and other techniques, based on laser/lamp melting and recrystallization or various epitaxial techniques, were developed." From the late 1970s to the beginning 1990s, various alternatives to SOS were developed on full sheet substrates (BESOI by IBM in the 1970s; ELTRAN by Canon in 1990) or by 3D process integration (Zone Melted Recrystallization ZMR since the 1980s). "The real breakthroughs in SOI wafer fabrication were the Separation by Oxygen Implantation (SIMOX) technique, first used in 1978 to fabricate CMOS circuits by NTT [4], and the Smart-Cut process, invented by LETI [5], [7]." SIMOX kept on improving by perfecting substrate annealing during oxygen implantation and high temperature annealing (by CEA,LETI at 1300 °C) [8], multi-implantation (by Monsanto) [9] and low energy implantation (by Spire) [10]. Defect density drastically dropped by 4 orders of magnitude (10^2–10^3/cm^2) compared to SOS.

Since the late 1960s, Michel Bruel, was involved at CEA, LETI to develop defect free heavy dose ion implantation. With his team and the collaboration of visiting Professor Stoemenos, of Thessaloniki University, he was the right person to successfully address the reduction of defect density in SIMOX, which he succeeded in, and finally he invented SMARTCUT. Michel Bruel says: "I wanted to imagine new solutions better suited than SIMOX for electronic mass market applications. I thought of a fracturing process, based upon defects generated at their projected end of range (Rp) by light ions implanted at high dose, giving rise to the formation of nano-gaseous bubbles and nano-fracturing. Hydrogen, or helium gas ions, would penetrate into silicon without introducing any damage along the major part of the Rp. By tuning the acceleration voltage on the implanter, we could choose the depth of the nano fracturation layer, i.e. the

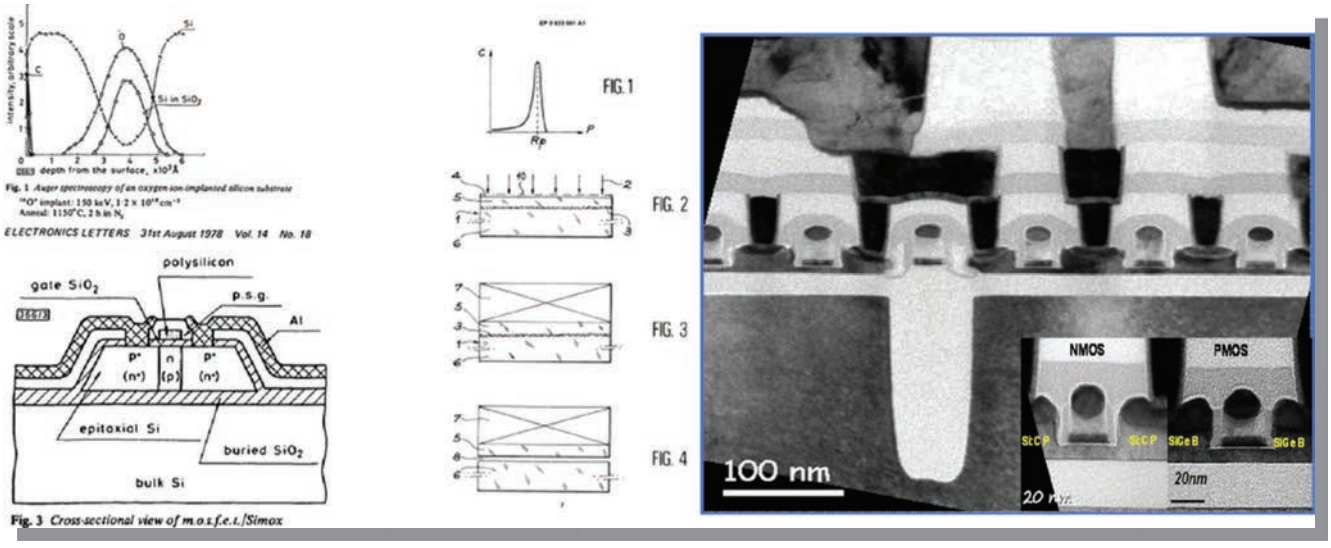


Fig. 3 *Cross-sectional view of m.o.s.f.e.t./Simox*

(left) The first SIMOX paper [4]. (middle) Smartcut principle: European patent EP/FR9111491, filed Sept. 18, 1991 by Michel Bruel (CEA, LETI)[5] showing the 3 major steps of ion implant into the substrate through a screening layer, bonding to a handle wafer and splitting of the new substrate at the fracture zone around Rp after heat treatment. (right) Ultra thin FD devices for CMOS scaled logic applications.(Tsi = 6 nm TBOx = 20 nm) Lg = 14 nm processed on 300 mm SMARTCUT wafers (middle and right figures provided by courtesy of CEA, LETI)

thickness of the layer to be created. After the implant, we bonded the substrate to a handle wafer, applied a thermal cycle that fractured the implanted substrate. We removed the initial substrate before smoothly polishing the final SOI substrate surface. The initially fractured wafer was recyclable. This process was directly applicable in a microelectronics environment. We wanted to keep some lead time: the invention was kept confidential from 1991 to 1995." Meanwhile, SIMOX was used to process radiation hardened high speed microprocessors of the 68000 family, for military and space applications, as soon as 1988. Michel Bruel received many awards for the invention of the SMARTCUT process, among which was the 2008 IEEE Cledo Brunetti Award. In 1992, in the context of the fall of Berlin wall, André-Jacques Auberton-Hervé and Jean-Michel Lamure started SOITEC, with the support of Michel Bruel in the clean rooms of CEA, LETI, and were convinced to apply the technology to future low power and high performance civilian applications. Initially a company of 4 employees, today SOITEC counts 1000 employees worldwide. SOITEC has ramped up the SMARTCUT wafer production since 1993 and is nowadays the provider of 90% of the SOI market worldwide. Auberton-Hervé, SOITEC CEO until 2015, declares: "We licensed SEH in 1997 and used the money to invest in our first factory. Nobody believed we could challenge them not only on innovation but also on production." SMARTCUT SOI wafers have a diameter range from 50 to 450 mm, with the lowest defect density, comparable to what is provided on commercial bulk silicon by volume. The SMARTCUT principle is applied to many different materials that could be bonded to an oxidized Si wafer.

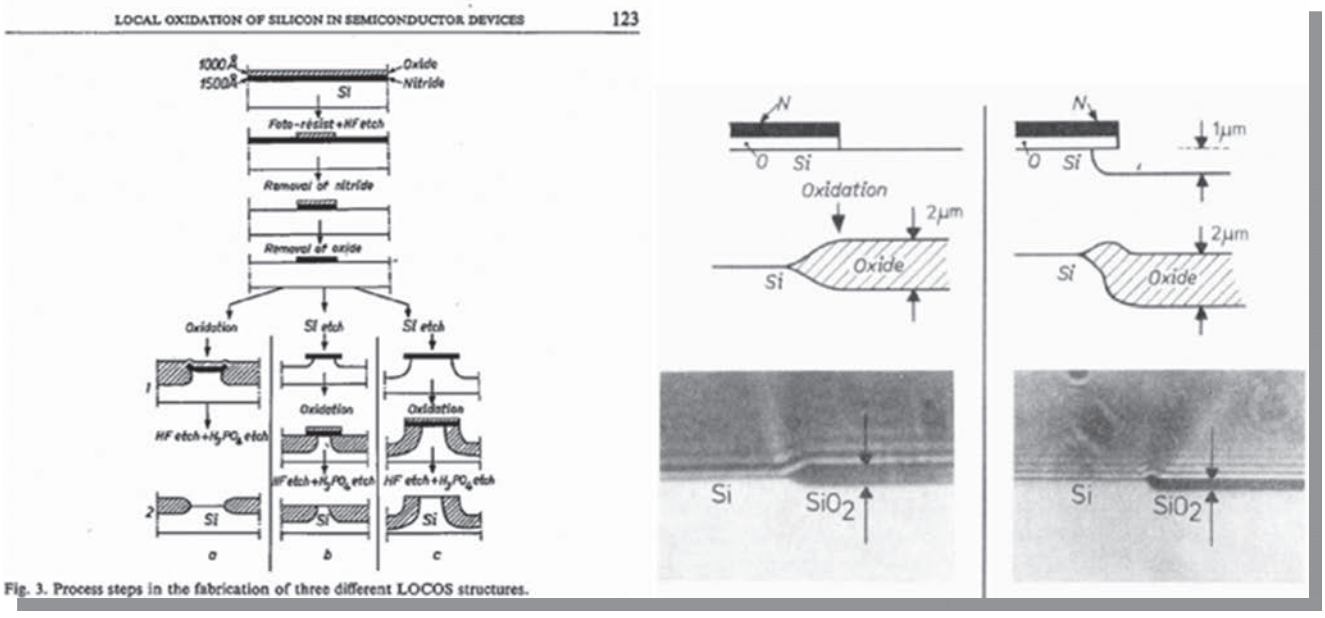
Ghavam Shahidi, the IEEE 2010 Cledo Brunetti and 2006 JJEbers Awards recipient, was among those who pioneered the realization of VLSI designs on Partially Depleted SOI as soon as 1989 at IBM. Shahidi says: "Over the first 10 years, the biggest 'non-technical' challenges were convincing the IBM management and end users to commit product to SOI technology." It took 8 years in device engineering and development to achieve the first complex circuit demonstration (the Power PC601). The "first commercial IBM's Power 4 processor in 180 nm CMOS SOI technology, came out in 2001, first IBM's giga frequency processor and largest chip at the time." Other companies adopted partially depleted SOI in the 180 down to 45 nm nodes, such as Freescale (Power PC7455 CPU), AMD (K series) or SONY (Xbox360, PS3, Wii).

Fully depleted and multigate/ Gate-All-Around architectures have been studied since the 1980s by SONY [11], CEA,LETI [12], Hewlett-Packard [13], IMEC [14] and are necessary to reach a MOSFET minimum subthreshold slope of 60 mV/dec, and thus reduce drastically leakage current. The reduction of Si (TSi) and buried oxide (BOx) thicknesses are the prime challenges to scaledown CMOS devices. It took approximately ten years to achieve sub-20 nm gate lengths devices on less than 10 nm thin SOI and 10 nm thin BOx on 300 mm wafers [15]. OKI was the first company to ship in 2000 an ultra low power circuits based on FDSOI, including an MCU, power circuits, memory and LCD driver. STMicroelectronics, IBM and Globalfoundries adopted FDSOI for their sub-28 nm nodes, moving towards 10 nm. As such, SMARTCUT is a desirable choice for monolithic 3D integration based on thin film devices [16].

Beyond digital applications, SOI is fulfilling the promise of penetrating the More-Than-Moore diversification market. SMARTCUT is providing 90% of the RF Front-End devices for mobile phones. The substrate engineering has been refined by including high resistivity and a trap rich interface at the buried oxide backside [17], [18] to enhance the final apparent substrate resistivity and, thus, reduce the cross talk to the substrate significantly. Many teams worldwide such as IBM and CEA, LETI/STMicroelectronics, have been developing the integration of RF and mixed signal technology on SOI since the early 2000s. The exceptional vertical isolation and high quality passivation brought by such a thick oxide, combined to high resistivity silicon and trap rich oxide backside interface, makes it ideal to enable co-integrated RF switches with LNA [19], [20]. Auberton-Hervé concludes: "In the past 3 decades, SOI has also been the test bench for Si based diversification for sensors, photonics systems, on-chip applications for communication and data transmission, and concentration PV system markets. It is still able to expand to other areas."

Lateral field isolation is **anyway necessary whatever the substrate**. The invention of LOCal Oxidation of Silicon (LOCOS) brings us back to the late 1960s when E. Kooi, J.A. Appels and their team at Philips Research Labs were strongly committed to advanced microelectronics research. Unfortunately, both of these highly talented individuals passed away. We had the kind contribution of Prof. Pierre H. Woerlee, at Technical Univ. of Eindhoven (Netherlands), the first non-US General Chair of the IEDM, who worked with E. Kooi and J.A. Appels in the 1980's at Philips Research Labs. The LOCOS isolation has been nurturing microelectronics business for decades and has been applied into other types of applications such as microsystems or power devices. Else Kooi was the 1990 IEEE Cledo Brunetti Award recipient.

The introduction of LOCOS needed new process alternatives. LOCOS isolation posed new constraints at the integration level: knowledge on selective oxidation, nitride selective etching, stress induced in the active area during oxidation, generation of stacking faults or dislocations depending on the oxidation conditions, nitridation of active area edge (Kooi effect), etc. The fact that the silicon nitride oxidation rate is much less than Si's (under 1 atm it is several 10x higher), is a remarkable property that was advantageously exploited by E. Kooi and his team (1966



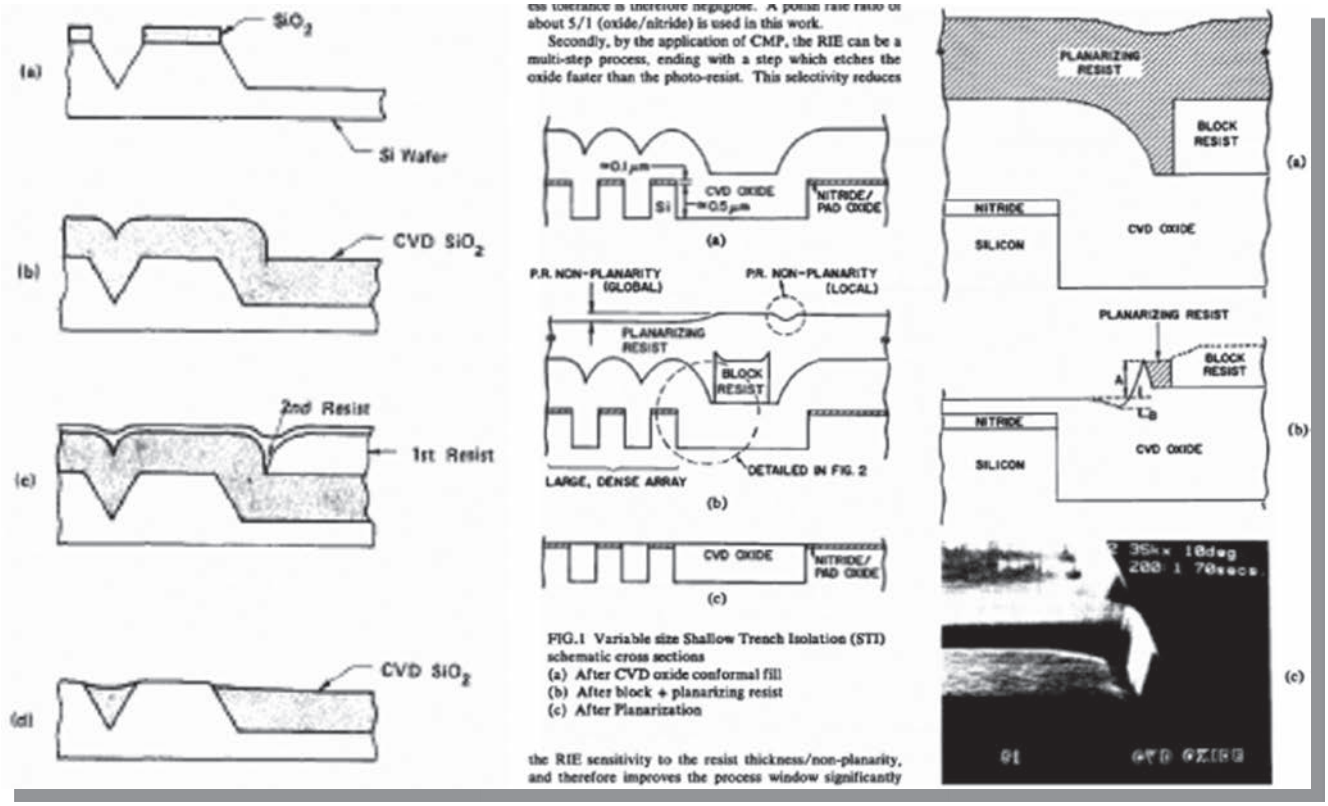
(left) LOCOS isolation invented by Appels and Kooi, first presented at 3rd Conference Solid State Devices in 1969 at Exeter(UK) [21]: three options for process flow showing the selective oxidation of silicon and increasing recess of field oxide. No pad oxide was used (right) LOCOS isolation: semi-recessed and recessed [22]. A pad oxide is used to reduce dislocations. The bird's beak and bird's head appear on the semirecessed and recessed versions respectively. (by permission of Koninklijke Phillips Electronics N.V.*)*

patent [23]) and published in 1969 and 1970 [21]. The initial motivation to introduce LOCOS isolation was to reduce the lateral diffusion of dopants that reduced the distance between active areas and increased the lateral parasitic capacitance of p-n junctions in planar technology. That, of course, had great impact on bipolar devices too and could be extended to MOSFET technology. Marc J. de Vries and Kees Boersma reported in 2005 [24]: "All this happened in connection with MOS (Metal Oxide Semiconductor) ICs…it was quite some time before the Nat. Lab. was prepared not only to work on bipolar ICs for analogue purposes, but also to work on MOS, which was considered to be more suitable for digital techniques."

A dopant free lateral recessed isolation was needed. The solution they imagined was to recess an insulator (silicon dioxide) because the direct moat isolation was degrading the step coverage problem (gate metallization and lithography), without stopping the diffusion of dopants. LOCOS isolation, in spite of the bird's beak introducing a feature size loss, was an elegant solution at the introduction of polysilicon gate. For decades, major teams worldwide have been working on a huge number of solutions to reduce the bird's beak, to planarize and reduce strain at the active area edge. These solutions were rich of imaginative constructions named SWAMI (Sidewall Masked Isolation), Poly Buffer LOCOS, SILO (Sealed Interface Local Oxidation of Silicon), SuperSILO, FuROX, etc., aiming at a bird's beak reduction and planarization of the topography with extra process costs as compared to the initial process. The whole microelectronics business has been using them intensively until the early 2000s, and still adopt them for specific solutions in the More-Than-Moore diversification domain. None of the modified LOCOS solutions could totally suppress the Kooi effect (the so called "white ribbon"), because the combined use of silicon nitride and steam oxidation inherently causes it. A sacrificial oxidation removes the nitrided silicon at the active area edge and allows the growth of a reliable non-thinned gate oxide. Kooi and Appels proposed very quickly (in 1970) to adopt such a solution to eliminate the Kooi effect.

Only SILO could prove zero bird's beak compatible with zero defect provided that a thin nitride (10 nm) was sealed to the active area by 1 nm Rapid Thermal Nitridation (RTN) [26], [27] or later on by a transfer under vacuum in the LPCVD reactor. The ultimate scaling limits of LOCOS type isolation schemes came from the field oxide thinning and 2-dimensional (2D) increase in bird's beak value appearing in small geometries. SuperSILO brought a drastic reduction of the bird's beak and of the 2D effects down to 100 nm active area width [27]. Meanwhile, STI was making progress thanks to Chemical Mechanical Polishing (CMP) planarization.

From the early 1980s, various approaches to achieve a workable STI were carried out in the semiconductor companies worldwide (such as Toshiba, [28]) using a non-selective etchback of a thin resist and deposited oxide bilayer. This technique suffered from uniformity issues and residues due to slight deviations from 1/1 selectivity etching. Bijan Davari, IBM, declares: "I realized the potential of STI around 1985 for both logic and memory applications. This



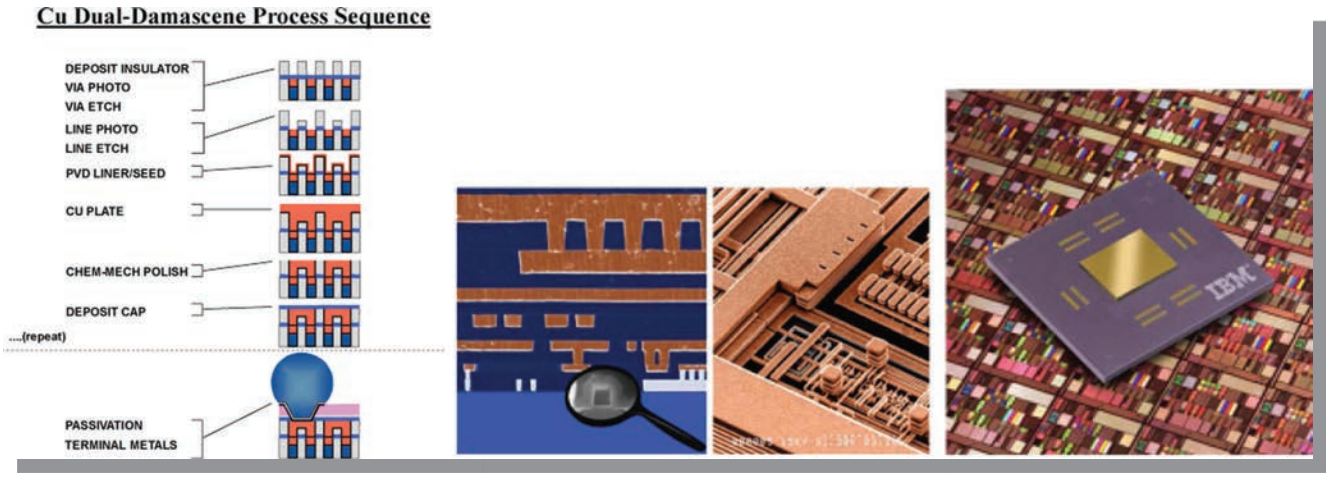
(left) STI by using sacrificial deposited oxide and several resists by Shibata et al. at 1982 IEDM [28]; (right) Planarization by block resist and etch back to alleviate the dishing problem was published by Davari et al. at 1988 IEDM [29]; CMP was added later in 1989 to obtain full planarization.

included all the CMOS technologies for both High-performance and Low-power applications and standalone DRAM." The most important hurdle for STI was the planarization for variable pattern factor isolation structures. The planarization problem resulted in too much "dishing" in large isolation areas and not adequate removal of the deposited field insulator in small isolation areas.

Besides the optimization of gate insulator breakdown, junction leakage (areal and peripheral) and field doping, a large number of CMP techniques (see also January 2019 Newsletter issue), were tested for the very first time in the FEOL process. Bijan continues: "We achieved a breakthrough around 1988 by demonstrating a perfectly planar STI process for a very demanding variable pattern factor 16Mb DRAM technology at IBM. This was achieved by a combination of chemical-mechanical polishing (CMP) and reactive-ion-etching (RIE) with dummy patterns that were generated prior to RIE by an automated placement algorithm based on the pattern factors of the underlying isolation and the adjacent structures. We created the design tools for the pattern generation that was subsequently used in all our products [30]. The STI technology then became the industry standard for device isolation. It took us about 3 years to go from test site, single device isolation experiments to fully functional circuits, and then another 2 years to product. Our first product was a 16 Mb DRAM with STI and deep trench for storage capacitance." Davari was the IEEE 2005-JJ.Ebers and 2010 A. Grove Awards recipient.

Geometric downscaling revealed limitations in materials properties such as aluminum: another major breakthrough was needed for interconnects. The introduction of copper (Cu) on-chip multilevel interconnects (BEOL, back end of line) took a long path since the 1980's, when the limitations of aluminum (Al) wiring at smaller geometries due to scaling started to appear. The first attempt to solve scaling issues concentrated on the flattening of topography while keeping Al for metal wiring. In strong synergy with the efforts carried out on STI (hereabove), CMP was introduced by IBM in 1991 to planarize interlevel dielectrics (ILDs) on pre-etched metal lines, and to polish separate interlevel studs, or "vias" made of tungsten [30]. The obtained planarization enabled stacking of multiple wiring levels at constant minimum pitch, and improved lithographic patterning.

Important efforts were carried out to keep the conventional subtractive-etched/ILD backfill scheme to introduce Cu metallization. Its higher reflectivity pushed towards hard-mask lithography and perfect planarization of topography. The absence of volatile Cu etching byproducts at room temperature required etching temperatures



(Left)double damascene schematic process flow; (right) Publicity photos from CMOS/Cu BEOL technology announcement, showing 6-level Cu dual damascene wiring, and world's first Cu BEOL production chip (PPC750) [35] (D.Edelstein by courtesy).

higher than 200 °C (at 250 °C: by NTT [31], or at 220 °C by Rensselaer Institute [32]). The passivation of Cu lines was very critical and requested anti-corrosion treatments included in the etching steps. Further, since Cu ions can diffuse rapidly through SiO_2 dielectric, and can potentially poison Si devices, each Cu wire had to be encapsulated by a diffusion barrier. This requirement would have been quite difficult for subtractively-etched Cu lines, with their exposed and reacted sidewalls and top surfaces. These Cu etching difficulties coupled with the need for high-performing planarization pushed towards a different paradigm. That was the Damascene or Dual Damascene scheme with its ILD patterning, conformal metal fill, and excess metal CMP developped by IBM (see figure, Newsletter january 2019 issue and [33], [34]). Dual damascene had been introduced earlier for DRAM W interconnects [30], and emerged for Cu (VMIC 1993) [35]. Finally, IBM discovered that by modifying the recipe for electrolytic Cu plating used for packaging interconnects, they could fill high aspect-ratio lines and vias with no voids or seams, with a "superfilling" plating process that improved as the wires got narrower. It produced a quantum leap improvement in electromigration reliability (assuming integration with a proper diffusion barrier). This winning combination has kept the door open for Moore's Law BEOL scaling, extending Cu BEOL for over 20 years and 9 generations in manufacturing [35].

Dan Edelstein, IBM, says: "In the mid 1980's, IBM started the initial drive to migrate from Al(Cu) to Cu/low-k BEOL, initiated by my colleague C-K Hu, to meet our growing needs for bipolar-based mainframe CPU high-current circuits (with high EM reliability). In the early 1990's, the needs switched to low-parasitic capacitance, higher-density and lower-cost CMOS wiring." Edelstein adds: "Besides matched CTEs and high modulus for SiO_2 ILD vs. passivation, I had found in the literature that SiO_2 possessed a very low Cu solubility limit, despite the high diffusivity of Cu atoms, and OH-catalyzed Cu ionization in BEOL-level electric fields leading to much faster Cu ion drift diffusion."

The team had to respond the fundamental questions of deposition, patterning and containing the interconnect material. "The retained options were: 1) PVD Cu seed + damascene (superfilling) electrolytic plating, 2) (Dual) Damascene dielectric patterning with 2-step CMP of Cu/barrier, or 3) Full encapsulation of Cu lines and vias with diffusion barriers of TaN/Ta bilayer liner plus Si_3N_4 dielectric cap. The combination of these barriers with SiO_2 interlevel dielectric, plus the additional Si_3N_4 barriers between FEOL and BEOL provided redundant protection against Cu corrosion, migration, interline leakages, and FEOL device poisoning."

The first functional microprocessor product was demonstrated in Q4 1997, as early-user hardware, on a 0.22 µm production high-performance CPU chip (PowerPC 750 for Apple). It took approximately 3/4 year to qualify this for high-volume production. "The much less mature Cu technology demonstrated the expected frequency improvement (ISSCC 1998) [35], and had tighter clock skew distributions, electromigration lifetimes and statistics way beyond the spec limit." During the past two decades, the SiOx dielectric has evolved by doping and density reduction into SiOF, SiCOH with low k SiCN(H) caps, and ultralow-k porous SiCOH (IEDM 1999 and 2006, IITC 2004) [35]. Copper/airgap for 2 fatline levels was introduced into manufacturing by Intel in 14 nm [36]. For the sub-10 nm nodes, Co or Ru wiring for the finest BEOL levels, or Cu encapsulation by Co, were envisaged (already presented by Komatsu at MRS MAM 2007) to limit/suppress electromigration [35], [37], in spite of higher Co and Ru resistivities that might be recovered for 7 nm barrierless Cu lines. D. Edelstein, A. Grill and C-K Hu are the 2019 Cledo Brunetti Award recipients for their contribution to Cu/Low K technology.

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Upcoming Technical Meetings

2019 IEEE International Electron Devices Meeting (IEDM)

by Gary Dagastine and Chris Burke

Fast-growing and diversified applications of semiconductor technologies in areas such as artificial intelligence, mmWave/5G communications, automotive and the Internet of Things are driving the development of new processors and memories, special-purpose accelerators, 3D architectures, power devices, quantum computing devices and other novel materials and devices. In response, and to better serve the needs of participants, the 2019 IEEE International Electron Devices Meeting (IEDM) (December 7–11, 2019 in San Francisco) is making modifications to its technical subcommittee structure to better align with these technology trends.

The IEDM is the world's premier and the most influential forum for the unveiling of breakthroughs and new concepts in advanced semiconductors. "The content of papers submitted to and presented at the IEDM needs to reflect the ongoing and future trends to best serve our authors and attendees," said Suman Datta, IEDM 2019 Technical Program Chair and Stinson Chair Professor of Electrical Engineering at the University of Notre Dame. "Therefore, based on input from attendees, members of the IEDM Executive Committee, and the IEDM 2018 Technical Subcommittee Chairs, we have decided to make modifications to our technical subcommittee structure this year to better align the IEDM technical program with these developing trends."

Prospective paper authors will benefit from knowing these major changes:

- A new **Emerging Device & Compute Technology (EDT)** subcommittee, co-chaired by Kuan-Lun (Alan) Cheng of TSMC and Iuliana Radu of Imec, will seek papers on emerging devices, circuits and architectures that support new computing models like neuromorphic, in-memory, approximate and quantum computing, Ising state machines, continuous time dynamical systems, lifelong learning machines, etc.
- **Memory Technology (MT)** – Chaired by Ming Liu of the Chinese Academy of Science, the scope of this subcommittee has been expanded beyond traditional memory technologies to include novel memory devices (e.g., PCRAM, FeFETs, RRAM, various flavors of MRAM), along with in-memory computing and processing-in-memory techniques.
- A new **Advanced Logic Technology (ALT)** Technical Subcommittee replaces both the former Circuit & Device Interaction and Process & Manufacturing Technology subcommittees. Chaired by Sandy Liao of Intel, this new subcommittee will seek papers in the areas of platform technologies, advanced CMOS, unit and integrated process advancements in both FEOL/BEOL, Ge, gate-all-around (GAA) devices, monolithic 3D, NCFETs and TFETs.
- A new **Microwave, Millimeter Wave and Analog Technology (MAT)** subcommittee, chaired by Erik Lind of Lund University, replaces the former Compound Semiconductor & High-Speed Devices subcommittee. It expands the scope to include mixed-signal technologies, energy-harvesting circuits, analog front-end, tunable passives, antenna arrays, beam-formers, filters, switches, non-reciprocal devices, LNAs and PAs.
- A new **Power Devices & Systems (PDS)** subcommittee, chaired by Jun Suda of Nagoya University, will seek papers on topics including existing and new wide-bandgap transistors; new applications ranging from power delivery to automotive to smart grid; compact models of power devices and interactions with passives, thermal management; etc.
- A new **Reliability of Systems & Devices (RSD)** subcommittee, chaired by Gaudenzio Meneghesso of the University of Padova, aims to revitalize and revamp the field of reliability, given that it is as much about devices as systems. This subcommittee will encompass all aspects of reliability from variation to aging to design-for-manufacturability (DFM).

The following three IEDM technical subcommittees stay as they are:

- **Modeling and Simulation (MS)** subcommittee chaired by Lee Smith of Synopsys

- **Optoelectronics, Displays and Imagers (ODI)** subcommittee chaired by Lars Zimmermann of IHP
- **Sensors, MEMS, and BioMEMS (SMB)** subcommittees chaired by Duygu Kuzum of the University of California, San Diego.

Paper submission deadline
Paper submission deadline for IEDM 2019 is July 26, 2019.

Further information about IEDM
For registration and other information, visit www.ieee-iedm.org.

Follow IEDM via social media
- Twitter: www.ieee-iedm.org/twitter
- LinkedIn: www.ieee-iedm.org/linkedin
- Facebook: www.ieee-iedm.org/facebook

2019 IEEE International Flexible Electronics Technology Conference

August 11–14, 2019, Vancouver, Canada

https://attend.ieee.org/ifetc-2019/

Welcome Participants!
On behalf of the Organizing Committee, it is our pleasure to welcome you to join us at the 2019 *IEEE International Flexible Electronics Technology Conference* (IEEE IFETC 2019) during August 11–14, 2019 at the *Simon Fraser University at Harbour Centre*, 555 W. Hastings Street, Vancouver, BC, Canada.

The 2nd IEEE IFETC 2019 is a premier conference for scientists, researchers, engineers, developers, and end-users to exchange technical research milestones and perspectives in the field of flexible electronics and their applications, including but not limiting to the following topical areas:

- Flexible transistors
- Flexible photovoltaics
- Flexible RFID and NFC Devices
- Flexible antennas and microwave devices
- Flexible energy harvesting
- Flexible sensors
- Flexible lighting and displays
- Smart textiles and wearables
- Chips and circuit design for flexible electronics
- Novel materials and processes for flexible electronics

The conference is expected to offer more than 150 presentations including 5 plenary/keynotes, 5 tutorials, over 40 invited talks by internationally renowned experts in the field, and more than 100 contributed technical presentations.

We sincerely invite your participation to the excellent technical programs of IEEE IFETC 2019 to be held at one of the most beautiful places in Canada, located on the scenic waterfront overlooking the Coastal Mountains and Howe Sound in downtown Vancouver.

We look forward to seeing you in Vancouver, Canada for IEEE IFETC 2019!

Sincerely,
Ravi Todi, Steering Committee Chair
& George Xiao, Woo Soo Kim,
General Co-Chairs

Society News

Message from EDS President-Elect

Dear EDS members:

Meyya Meyyappan
EDS President

I want to focus on the EDS educational activities this time. This is the most important service we can provide to our members, in my opinion. I think our members expect it too and find it valuable. Our profession constantly faces changes, in terms of disruptive technologies, new areas and applications (Internet of things, for example) and others. It is hard to keep up with everything happening in our own fields. Therefore, education beyond the traditional classroom becomes very important, and this is where EDS can play a key role.

For starters, we have a very successful Distinguished Lecturer (DL) program, which allows Chapters to organize an event for their members to hear leading EDS experts describe their cutting edge research activities. The EDS and the local chapter together partly cover the expenses of the lecturer. While the DL program is centered on a single lecturer, the Mini-colloquium (MQ) program collects 4–6 DLs in a single full-day event. More recently, EDS was one of the first Societies to introduce a webinar program that allows any member around the world to listen to an expert lecture right at their desk. We have been running monthly webinars for over three years now and it has been received enthusiastically in all ten regions. The lectures are archived on the EDS website for future on-demand viewing by the members.

At the last BoG meeting in San Francisco, a Summer School program was conceived for a potential start in 2020 as another educational offering. The Summer School, spanning 3–5 days, is expected to focus on a theme with a few experts serving as lecturers. This is not meant to be a longer version of a MQ or workshop or a different version of a conference, and we do not want a large number of speakers giving their canned one-hour seminars. This is more pedagogical on an emerging topic in the EDS field of interest where a deep immersion over 3–5 days can give the attendees a fast start in this area. We are aiming this for the graduate students, postdocs, early career professionals and anyone wishing to enter a new field. Detailed tutorial-style lectures may be complemented by hands-on activities in the labs, computer work, equipment/tool demo or industry visits. We will issue a call for proposals, and individual members, chapters or some combination can respond with their selection of the topic, lecturers and the venue. The EDS subsidy will help defray travel costs of the lecturers.

I would like to remind we offer MS and PhD student fellowships every year. More information can be found on the EDS website. Please nominate deserving students, and you will see that the process is simple and streamlined. We also recognize leaders in education with the EDS Education Award. This is to recognize those who go that extra mile beyond routine educational activities, for example, a wildly popular textbook, innovative educational tools, continuing education, promotion of EDS-related curriculum in developing regions of the world and other worthy efforts. Again, please nominate a deserving colleague, and the details can be found on the EDS website under Awards.

Finally, many of our members routinely develop innovative educational tools and concepts on their own, either as a part of their day job or as a hobby or simply out of the goodness of their heart to serve the community. We at EDS take pride in promoting them as we have a great reach all across the globe. A classic example is the Snap Circuit program our current EDS President Fernando Guarin initiated in 2011 to teach high school students about electronic circuits. Professor Muhammad Hussain from KAUST has just created a virtual tool to get training on device fabrication and associated equipment in cleanrooms (see related story in this issue of the Newsletter), which EDS is promoting now. This is a remarkable tool for students to get device fabrication training right at their desk and I expect it to become popular, especially in Regions 9 and 10 where access to such facilities is limited. If you have any innovative educational tools or ideas, or know of someone who does, please contact me or one of the EDS Officers and we will work with you to promote it to the community-at-large in all ten regions.

Message from the Editor-in-Chief

Dear Readers,

Carmen M. Lilley
EDS Newsletter
Editor-in-Chief

First, I want to thank all the readers who have given me feedback on changes to the newsletter to improve access via our new html format and making suggestions for the newsletter and articles. I encourage you to please continue to send me your suggestions and ideas at clilley@uic.edu. In this issue, you will find information about our very active student chapters around the globe, with their efforts in professional development of EDS members and outreach to their local community. I think you will find their news highlights to be positively inspiring in promoting education in the fields of IEEE and EDS to a diverse community of youths from around the world. I hope you enjoy the April issue and we look forward to sharing our July issue with you celebrating 25 Years of a Renewed Newsletter.

Sincerely,
Carmen

Announcement of Newly Elected EDS BoG Members

The EDS Board of Governors members-at-large election was held on December 2, 2018 in San Francisco, California. I am pleased to present the results of this election and short bios of the upcoming team that will lead EDS in years to come.

Bog Members-At-Large

A total of seven members were elected for a three-year term (2019–2021). Two of the seven electees are serving a second term, while the other five have joined the board for the first time. The backgrounds of the electees span a wide range of professional and technical interests. The following are the results of the election and brief biographies of the individuals elected.

Second Term Electees:

Navakanta Bhat received his Ph.D. in Electrical Engineering from Stanford University, in 1996. Then he worked at Motorola's Advanced Products R&D Lab in Austin, TX until 1999. He is currently a Professor and Chair at Centre for Nano Science and Engineering, Indian Institute of Science (IISc), Bangalore. His current research is on Nanoelectronics and Sensors. He has more than 240 publications and 24 patents. He was instrumental in creating the National Nanofabrication Centre (NNfC) at IISc, benchmarked against the best university facilities in the world. He is the recipient of IBM Faculty award and Infosys Prize 2018. He is Fellow of IEEE and INAE. He was the Editor of IEEE Transactions on Electron Devices, during 2013–2016. He is EDS Distinguished Lecturer and the chair of Nanotechnology Technical Committee of EDS. He is the founder and promoter of a startup called "PathShodh Healthcare", which builds point-of-care diagnostics for diabetes and its complications.

Murty Polavarapu is based in the Washington, DC area and is engaged in developing advanced memory and logic products for defense and aerospace markets especially for space applications. His experience also includes introduction of advanced DRAM and Flash memory products into commercial manufacturing at Toshiba and Micron. He holds Masters degrees in Physics from India, Electrical Engineering from Howard University and Technology Management from University of Pennsylvania. He has been an active IEEE volunteer at EDS, Nanotechnology Council, IEEE-USA and Member and Geographic Activities (MGA). He currently serves on the IEEE MGA Board and also on the IEEE Governance Committee. Polavarapu also served as a United States Peace Corps volunteer teacher in rural Fiji on a leave of absence. He has been recognized with IEEE Regional Activities Achievement Award, Dominion Semiconductor President's Award and IBM Outstanding Technical Achievement Award. He has been awarded eleven US patents.

First-Time Electees:

Paul R. Berger is a Professor in Electrical & Computer Engineering at Ohio State University. He is also a Distinguished Visiting Professor at Tampere University in Finland. He received the B.S.E. in engineering physics, and the M.S.E. and Ph.D. (1990) in electrical engineering, respectively, all from the University of Michigan, Ann Arbor.

He has authored over 120 articles, 5 book sections and been issued

22 patents with 6 more pending from 60+ disclosures with a Google Scholar H-index of 33. Notable recognitions include NSF CAREER Award (1996), DARPA ULTRA Sustained Excellence Award (1998), Faculty Diversity Excellence Award (2009) and Outstanding Engineering Educator for State of Ohio (2014). He has been on IEDM, ISDRS, EDTM commitees. He chairs the Columbus IEEE ED/PHO Chapter. He is Chair of the EDS technical committee on Electronic Materials and a member of Flexible Electronics committee. He is a Fellow and Distinguished Lecturer of IEEE EDS.

Maria Merlyne De Souza received the B.Sc. in Physics and Mathematics ('85) from the University of Bombay, BE in Electronics and Communications Engineering ('88) I.I.Sc, Bangalore, and PhD ('94) from the University of Cambridge, UK. She subsequently joined De Montfort University, where she became Professor of Electronics and Materials in 2003. She is currently Professor of Microelectronics at the University of Sheffield since 2007. She was elected Fellow of the Institute of Physics in 2002 and the Institute of Engineering Technology in 2006. She has published over 200 articles in Journals and conferences. She has served on the Editorial Board of JPhys D '15–'18, Associate Editor of IEEE Trans in Nanotechnology ('09–'14), technical and Executive committee member of IEDM ('12–'17), technical committee member of IEEE-IRPS (2003-2013), member of the IRT Nanoelectronic Council of France ('17–'20), reviewer of key field technologies of Helmholtz Association, Forschungszentrum Jülich, 2017. She is a registered STEM ambassador in UK.

Kazunari Ishimaru is an IEEE Fellow and Deputy Director with Institute of Memory Technology Research and Development, Toshiba Memory Corporation. He conducted research on high

speed SRAM, advanced logic, Flash and emerging memories, TCAD, and compact modeling. He is currently directing Corporate R&D strategy and business-academia collaboration. He graduated Waseda University with MS degree and joined Toshiba in 1988. He was a Vice President of R&D with Toshiba America Electronic Components Inc. from 2006 to 2010. He holds 25 U.S. patents and authored/co-authored over 50 technical papers and several invited talks and short course lectures at various international conferences. He served the IEDM General Chair in 2011, Steering committee member of ESSDERC/ESSCIRC from 2008 to 2016. He is one of the founder member of EDTM conference and a Technical Program Committee Chair in 2018. He is currently serving the IEEE EDS VLSI Technology and Circuit Committee Chair.

Bill Nehrer has developed various technologies over his 30+ years in the semiconductors, spanning from analog CMOS to High Speed BiCMOS and Bipolar, enabling world class products in phased array radar, audio/video single chip solutions, modem, hard disk drive, power management, and high resolution ADCs. His focus is High Reliability and yield optimization in mass production and was elected technical Fellow at Silicon Systems, a Texas Instruments company.

Managing Texas Instruments' High Precision Analog and High Speed BiCMOS roadmap, he directed multiple projects at worldwide TI locations. Joining PDF Solutions in 2004, he managed yield ramp and technology development consulting projects at logic fabs in 90, 65, 45, 32, 28, 20, 14, &10 nm technology. He is currently in FabVantage technology consultancy at Applied Materials since 2018 as Senior Director. Bill holds an MSEE degree in Solid State Electrophyics from the University of Southern California and BS in Chemistry from UCLA.

Camilo Velez is a postdoctoral researcher in microrobotics at Carnegie Mellon University. He had a postdoctoral appointment at University of Florida (UF) to fabricate magnetic materials for high frequency/5G communication devices. Ph.D. in electrical and computer engineering at UF in micro fabrication of magnetic materials. M.Sc. at UF, focused on microfabrication and reliability of III-V semiconductor devices. M.Eng. at Universidad de los Andes in microsystems and B.S. in Electronics Engineering at Pontificia Universidad Javeriana-Colombia. Skilled, hands-on and creative researcher with experimental experience in microsystems, MEMS (microelectromechanical systems), magnetic materials, biomedical devices, and electronics in engineering. With 9 years of experience in research and 2 years in industry, he has contributed to 19 journals and peer review publications, filled 2 international patents, and participate in more than 21 conferences. He is the global Young Professionals EDS committee chair, leading the social media initiative to empower Young Professionals in our society.

I welcome all electees and urge them to get fully engaged in the affairs of the Electron Devices Society. EDS is considered to be a volunteer-led volunteer-driven organization and we expect nothing less from all to continue this tradition.

Samar Saha
EDS Nominations and Elections Chair
University of California
Riverside, CA, USA

Congratulations to EDS Member, Jagadish Chennupati—one of eight scientists presented with a UNESCO Medal

Jagadish Chennupati, Nassiopoulou Androula Galiouna and Esko Ilmari Kauppinen were among the 10 eminent scientists who received the 8th UNESCO Medals for contributions to the development of nanoscience and nanotechnologies. © UNESCO/Jake Lewis

Eighth UNESCO Medals for Contributions to the Development of Nanoscience and Nanotechnologies

On 22 November 2018, ten eminent scientists and scientific institutions received the UNESCO Medals for contributions to the development of nanoscience and nanotechnologies during a ceremony held at UNESCO headquarters, Paris. The medal is awarded each year by the Director-General of UNESCO to prominent scientists, public figures and organizations that contributed to the development of nanoscience and nanotechnologies in the spirit of UNESCO's priorities.

The fields of nanoscience and nanotechnology have been developing for just a few decades, but they now contribute to the economy of all countries and almost every human life. "*Today, we meet to celebrate exceptional scientists and practitioners from around the world, who are pushing back the frontiers of scientific knowledge of what lies beyond our world and to transform our lives for the benefit of all*", said Miguel Clusener-Godt, Director of UNESCO's Division of Ecological and Earth Sciences. "*They impact electronics and computing, medicine, materials and manufacturing, energy and transportation… Nanoscience and nanotechnology have the potential to foster new developments in science, technology and innovation via the dissemination of new knowledge and applications.*"

This is why the Medal was established in 2010 at the initiative of the International Commission responsible for developing the Nanoscience and Nanotechnologies theme for the Encyclopedia of Life Support Systems (EOLSS). Since then, 46 Medals have been awarded to prominent scientists, institutions and public figures, such Isamu Akasaki, winner of the 2014 Nobel Prize in Physics, Zhores Alferov, winner of the Nobel Prize in Physics in 2000, and Chunli Bai, President of the Chinese Academy of Sciences.

The 2018 UNESCO Medals for contributions to the development of nanoscience and nanotechnologies were awarded to:

Sergeev Alexander Mikhaylovich–Russian Federation

President of the Russian Academy of Sciences, Deputy Chairman of Russian Presidential Council for science and education.

His expertise in plasma physics, nonlinear dynamics of optical systems and highly sensitive optical measurements are internationally recognized. He has made important contributions to the fields of optical tomography of bio-tissues, and for created of the most powerful laser that can generate impulses with peak power of hundreds petawatts.

Tatartchenko Vitali Antonovitch–France

Consultant at the Aix-Marseille University in France, Vice-Chairman of COSPAR (International Committee of Space Research).

He provided the theoretical basis of PeTa effects (Perelman-Tatartchenko effect)—the physical phenomenon of characteristic radiation accompanying first order phase transitions—and demonstrated its existence experimentally. On the basis of the PeTa effect he developed a new conception of cavity-less lasers and models for cavitation luminescence, sonoluminescence and laser induced bubble luminescence.

Fursenko Andrei Aleksandrovich–Russian Federation

President of the Supervisory Board of the Russian Scientific Foundation, Assistant of the President of

the Russian Federation, Chairman of the Academic Council of the Foundation "Centre for Strategic Research North-West".

He directed the development of the national programme "Development of nanotechnologies in Russia" as Minister of Education and Science of the Russian Federation. He is the author of over 100 scientific publications, notably on technological innovation.

Ismail Elnaggar Mohammed– Egypt and United States of America

Founding Director of the Khalifa Semiconductor Research Center in the United Arab Emirates.

His many achievements include the development of a self-powered wearable device that can predict the onset of a heart attack ahead of time.

Kauppinen Esko Ilmari – Finland

Manager of the NanoMaterials Group at the Department of Applied Physics of the Aalto University School of Science.

His research focuses in gas phase synthesis of nanomaterials, including carbon nanotubes and polymer-drug composite nanoparticles and their characterization with advanced electron microscopy methods. These fields create new opportunities for drug delivery, inhaled at the micro and nano scales, which are very promising to treat diabetes and many other diseases.

Nassiopoulou Androula Galiouna – Greece

Director of Research and Head of the "Nanostructures for Nanoelectronics, Photonics and Sensors" research group at the National Centre for Scientific Research Demokritos in Athens, President of the General Assembly of the European Institute of Nanoelectronics.

She pioneered the fabrication of vertical silicon nanowires on the Si wafer and developed innovative applications of Si nanowires, nanocrystals and porous Si, which include low-loss transmission lines and antennas on the Si wafer working up to 210 GHz, thus enabling fast communication on the Si chip, nanocrystal memories, high capacitance density microcapacitors for energy storage, high performance miniaturized Si thermal sensors applied in a respiration system and a flow meter for gas engine etc.

When receiving her medal, she stressed the importance of caution when dealing with nanostructures, since their properties are not yet fully known and of aiming for societal benefits in all research. Through miniaturization, Microelectronics made devices faster and cheaper and revolutionized computing and communication systems. This has been now expanded to the general field of Nanotechnology, fostering applications in all fields of life, including new medical applications, new drugs and drug delivery systems, she explained. "*Safety issues should thus be always one of the main priorities to be studied, discovered and applied.*

(...) Finally, as scientists we should stay committed and engaged that Nanoscience and Nanotechnology and its innovative applications stay within the spirit of Unesco for sustainable development for all, against poverty and for a peaceful world, for the profit of all societies."

Zehetbauer Michael Josef – Austria

Head of the Faculty Group "Physics of Nanostructured Materials" at the University of Vienna.

He has been working on increasing the efficiency of functional materials such as nanostructured thermoelectrics, hydrogen storage materials, and biodegradable implant materials.

Jagadish Chennupati – Australia

Head of the Semiconductor Optoelectronics and Nanotechnology Group of the Australian National University; Convenor of the Australian Nanotechnology Network.

He has made important contributions in the field of semiconductor nanotechnology, and established a pioneering research programme in Australia in semiconductor nanotechnology and optoelectronics.

Mansurov Zulkhair – Kazakhstan

Director-General of the Institute of Combustion Problems, Doctor of Science, Professor.

He has made important contributions in the production of nanocarbon materials and carbon nanotubes and graphene. His research focuses on hydrocarbon combustion kinetics and mechanisms, the structure of cold and sooting flames, and investigation the functions of nanocarbon materials.

Chekhonin Vladimir Pavlovich– Russian Federation

Vice President of the Russian Academy of Sciences. Founder and Head of the Department of Medical Nanobiotechnologies of the Russian National Research Medical University.

His fields of research include development of nanotechnological visualization systems and the targeted delivery of therapeutic agents and genetic material to target cells, and investigation of nanotechnological approaches to genodiagnostics and bioprotection in socially significant diseases. This includes the targeted delivery of diagnostic compounds to cancer cells, which can bring us closer to better understanding and treating oncological diseases.

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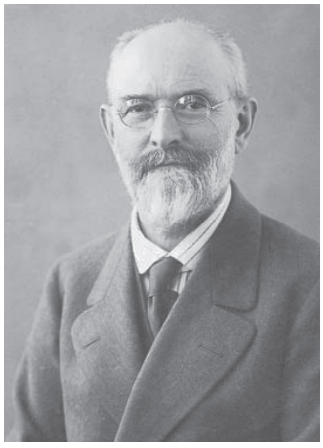
IEEE ROBERT BOSCH
MICRO AND NANO ELECTRO MECHANICAL SYSTEMS AWARD



Robert Bosch (1861-1942)
Inventor, Entrepreneur, Founder of Robert Bosch GmbH

The Robert Bosch Micro and Nano Electro Mechanical Systems Award was established by the IEEE Electron Devices Society in 2014 to recognize and honor advances in the invention, design, and/or fabrication of micro- or nano-electromechanical systems and/or devices. The contributions to be honored by this award should be innovative and useful for practical applications.

This award is sponsored by the IEEE Electron Devices Society with financial support from Robert Bosch LLC. It is intended that the award will be presented annually to an individual or to as many as three individuals whose achievements and contributions are judged to meet the selection criteria for the award. The award will be presented at an IEEE conference of the winner's choice. It is not necessary for the recipient(s) to be a member(s) of IEEE.

The recipient will receive a US$10,000 honorarium, travel expenses to attend the award presentation, a bronze medal, and a certificate. In the event that more than one awardee is selected, the cash honorarium will be equally divided among the recipients. Each recipient will receive a bronze medal and a certificate.

Please visit the EDS website for more information on this award: http://eds.ieee.org/robert-bosch-micro-and-nano-electro-mechanical-systems-award.html.

Nominations for this award should be made using our online nomination form and submitted before midnight (EST) on October 2. Letters of recommendation must be sent directly to l.riello@ieee.org according to the same schedule.

2019 IEEE EDS Robert Bosch Micro and Nano Electro Mechanical Systems Award Winner

The 2019 IEEE EDS Robert Bosch Micro and Nano Electro Mechanical Systems Award was presented to Hiroyuki Fujita, Advanced Research Lab of Canon Medical Systems Corp., Japan, at the 2019 IEEE MEMS Conference, Korea, January 2019. This prestigious award recognizes and honors advances in the invention, design, and/or fabrication of micro- or nano-electromechanical systems and/or devices.

Hiroyuki Fujita

For pioneering contributions in microactuators, optical-MEMS, and bio-nano-MEMS and strong leadership in the science of MEMS

Hiroyuki Fujita is Director of Advanced Research Laboratory of Cannon Medical Systems Corporation from 2017. He is also a Professor of Tokyo City University and Professor Emeritus of The University of Tokyo, where he served as a Professor of Institute of Industrial Science of the University over 38 years. He was a visiting professor in MIT and UC Berkeley. He received the B.S., M.S. and Ph.D. degrees in Electrical Engineering from The University of Tokyo in 1975, 1977 and 1980, respectively. He is currently engaged in the investigation of MEMS/NEMS and applications to bio/nano technology and IoT. Major research projects include MEMS-in-TEM experiment for simultaneous visualization and measurement of nanomaterials, vibrational energy harvesters using ionic liquids, and bio molecular/cellular characterization using MEMS tools. He has published more than 300 academic papers. He received many awards including l'Ordre des Palmes Academiques from Government of France, Docteur Honoris Causa from Ēcole Normale Supērieure de Cachan, The Prize for Science and Technology -Research Category from Ministry of Education, Culture, Sports, Science and Technology and Outstanding Achievement Award from The Institute of Electrical Engineers of Japan.

Kurt Petersen
2019 EDS Bosch Award Chair

2018 EDS Distinguished Service Award

Dr. Shuji Ikeda

The IEEE Electron Devices Society (EDS) is extremely proud of the services that it provides to its members. Its members generate the premier new developments in the field of electron devices and share these results with their peers and the world-at-large by publishing their papers in EDS journals and presenting results in its meetings. This is a global activity that is effective because of the efforts of numerous volunteers. Many of these volunteers labor in relative obscurity, with their only reward being the satisfaction that they receive in being an important part of a successful organization, namely of the IEEE Electron Devices Society. One means of thanking these volunteers is to recognize their contributions through the EDS Distinguished Service Award.

The recipient of the 2018 EDS Distinguished Service Award was Dr. Shuji Ikeda, Tei Solutions Co. Ltd., Tsukuba, Japan, and the award presentation took place at the International Electron

Devices Meeting (IEDM) in San Francisco, on December 3, 2018.

Shuji Ikeda received the B.S. degree in Physics from the Tokyo Institute of Technology, Japan in 1978, M.S. degree in Electrical Engineering from the Princeton University, USA in 1987, and PhD degree. in Electrical Engineering from the Tokyo Institute of Technology, Japan in 2003. He joined the Semiconductor Division, Hitachi ltd., Tokyo, Japan in 1978, where he was engaged in research and development of the state-of-the-art SRAM processes and devices. He was also working on developing process technology for LOGIC, embedded DRAM, embedded Flash memories, and CMOS power RF devices as well as transfer of technology to mass production line. In April 2005, he joined the SEMATECH/ATDF at Austin, Texas, as the Director of Technology, where he developed different types of technologies including scaled CMOS, non-classical CMOS, new materials and tools. In 2008, he established tei Technology, LLC at Austin, where he creates new business models and provides total (business/technology) solutions to the customers. He also founded tei Solutions Inc., R&D foundry, in Tsukuba, Ibaraki, Japan in 2010. His main focus is integrating emerging technology onto semiconductor manufacturing technology to create innovative products, including bio sensors, DNA sequencers, and various kinds of IoE (Internet of Everything) devices. He received several awards for his unique business model, Joyo Bank Manufacturing Award, 2013, and Tokyo Institute of Technology Venture Business Award, 2014. Shuji is a fellow of IEEE.

Shuji Ikeda's services to IEEE EDS are noteworthy and lasting. One of the important roles of his career in IEEE EDS is serving as the General Chair of IEDM 2002. As the first General Chair from Asia, he boosted Asian contributions to the IEDM and focused on manufacturing technology. His other major service to EDS is the launching of the EDTM (Electron Devices Technology and Manufacturing) conference in 2017. The EDTM was planned to focus on manufacturing, especially in Asia. As a chairman of the Ad Hoc Committee on Asian Flagship Conference, and VLSI Technology and Circuits Technical Committee, Shuji discussed with committee members, other EDS colleagues, and EDS executives once a week over the phone and face to face for three (3) years. Through the EDTM, we could try anything good to enhance EDS activities, that are quite different from other conferences. Thanks to the leadership from EDS executives, Shuji started the EDTM with great success in 2017 at Toyama, Japan. And, EDTM continues, the 3rd EDTM 2019 was held during March 13–16 in Singapore.

He and his wife, Hiroko, were classmates at Kunitachi High School, Tokyo. They are proud parents of Yuki, Ayano both are teachers for handicapped students and Sho, SDF personnel. All of them are not engineers, though.

Samar Saha
EDS Awards Chair
Milpitas, CA

2018 IEEE EDS J.J. Ebers Award Winner

Dr. Michael Shur

The 2018 J.J. Ebers Award, the prestigious Electron Devices Society award for outstanding technical contributions to electron devices, was presented to Dr. Michael Shur of Rensselaer Polytechnic Institute, Troy, NY, at the International Electron Devices Meeting in San Francisco, on December 3, 2018. This award recognizes Dr. Shur's "For pioneering the concept of ballistic transport in nanoscale semiconductor devices".

Dr. Michael S. Shur received MSEE Degree (with honors) from St. Petersburg Electrotechnical Institute (LETI) and PhD. and Dr. Sc. Degrees from A. F. Ioffe Institute. He was awarded Honorary Doctorates by St. Petersburg State Technical University and University of Vilnius. He is Patricia and Sheldon Roberts Professor of Solid State Electronics and Professor of Physics, Applied Physics, and Astronomy at Rensselaer Polytechnic

Institute. Dr. Shur is co-founder, President and CEO of Electronics of the Future, Inc. and a co-founder of Sensor Electronics Technology, Inc. Dr. Shur is Life Fellow of IEEE, APS, ECS, and SPIE, Fellow of the National Academy of Inventors and several other professional societies. He is Distinguished Lecturer of IEEE EDS and IEEE Sensors Council. His awards include IEEE Research and Teaching Awards, ECS Electronic and Photonics Award, Tibbetts Award for Technology Commercialization, RPI Faculty Awards, Senior Humboldt Research Award, and Best Paper Awards. Dr. Shur was listed by the Institute of Scientific Information as Highly Cited Researcher. His h-index is 108. In 2009, he was elected Foreign Member of the Lithuanian Academy of Sciences. His work has ranged from the new concept of the ballistic transport in nanostructures and plasmonic devices to the development and commercialization of deep UV LEDs and novel color rendition engines based on the statistical color figures of merit.

He and his wife, Paulina, were born, met and married in the Soviet Union. They came to the United States as refugees in 1976, when Michael joined Professor Lester Eastman's group at Cornell. Paulina had a Russian Ph. D. in theatre and film. She went back to school and received MFA degree in theatre directing from the University of Virginia. After graduation, she became Founder and Artistic Director of the Magic Mirror Theatre in Charlottesville, VA. Her best production was an opera based on her own libretto "The Age When Women Lived and Died for Love." Then she joined the RPI Electronics Arts Department as a faculty member. Paulina and Michael have two daughters—Luba (a lawyer who also graduated from the University of Virginia) and Natasha (a medical doctor who got her MD from the Albert Einstein School of Medicine).

Joachim N. Burghartz
2018 EDS J.J. Ebers Award Chair
Institute for Microelectronics Stuttgart
Stuttgart, Germany

IEEE ELECTRON DEVICES SOCIETY
J.J. EBERS AWARD

Nominate:
J.J. Ebers Award
on-line nomination form:
http://bit.ly/2THINQF

Submission Deadline:
July 1, 2019

Contact:
If you have any questions regarding the EDS J.J. Ebers Award, please contact Laura Riello of the EDS Executive Office at l.riello@ieee.org

Visit:
http://eds.ieee.org/jj-ebers-award.html

CALL FOR NOMINATIONS

The IEEE Electron Devices Society invites the submission of nominations for the 2019 J.J. Ebers Award. This award is presented annually by EDS to honor an individual(s) who has made either a single or a series of contributions of recognized scientific, economic, or social significance to the broad field of electron devices. The recipient(s) is awarded a plaque and a check for $5,000, presented at the IEEE International Electron Devices Meeting (IEDM).

ELECTRON DEVICES SOCIETY®

2018 EDS Education Award Winner

Dr. Muhammad Ashraful Alam and Dr. Fernando Guarin, EDS President

The EDS Education Award recognizes an IEEE/EDS Member from an academic, industrial, or government organization with distinguished contributions to education within the fields of interest of the IEEE Electron Devices Society. Dr. Muhammad Ashraful Alam was recognized at the International Electron Devices Meeting in San Francisco, CA December 3, 2018 as the 2018 EDS Education Award winner. The award cites Dr. Alam "*For educating, inspiring and mentoring students and electron device professionals around the world*".

Dr. Muhammad Ashraful Alam is the Jai N. Gupta Chair Professor of Electrical Engineering at Purdue University where his research and teaching focus on physics, fundamental limits, and technology of classical and emerging semiconductor devices. He received the BSEE degree from Bangladesh University of Engineering and Technology in 1988, MSEE degree from Clarkson University in 1991, and a Ph.D. degree from Purdue University in 1994.

From 1995 to 2001, he was with Bell Laboratories, Murray Hill, NJ, where he made fundamental contributions to laser dynamics, the design of optoelectronic integrated circuits, and the reliability ultra-thin gate dielectrics. From 2001–2003, he headed the IC Reliability Group at Agere Systems. Since joining Purdue in 2004, Dr. Alam has published over 350 papers on a broad range of More-Moore and More-than-Moore technologies related to self-heating in nanoscale and power transistors, sensitivity limits of biosensors, percolative transport in flexible electronics, atom-to-farm modeling of solar cells.

For his contributions, he has been elected a fellow of IEEE, American Physical Society, and the American Association for the Advancement of Science. He is also the recipient of the 2006 IEEE Kiyo Tomiyasu Award for contributions to device technology for communication systems, and 2015 SRC Technical Excellence Award for contributions to semiconductor reliability physics.

Prof. Alam views research and teaching as two sides of a coin because teaching forces one to understand a concept deeply so that it can be explained simply. The simple explanations connect the concepts in unexpected ways suggesting new ideas of creative research. With this perspective, Prof Alam has made important contributions to graduate and undergraduate education: More than 350,000 students worldwide have learned some aspect of semiconductor devices from his web-enabled courses. For additional details, see the "Teaching" and "Blogs" sections of his website: https://sites.google.com/view/alam-research-group/home

Durga Misra
2018 EDS Education
Award Chair
NJIT
Newark, NJ

2019 EDS EDUCATION AWARD
CALL FOR NOMINATIONS

The IEEE Electron Devices Society invites the submission of nominations for the EDS Education Award. This award is presented annually by EDS to honor an individual who has made distinguished contributions to education within the field of interest of the Electron Devices Society. The recipient is awarded a plaque and a check for $2,500, presented at the IEEE International Electron Devices Meeting (IEDM).

The nominee must be an EDS member engaged in education in the field of electron devices, holding a present or past affiliation with an academic, industrial, or government organization. Factors for consideration include achievements and recognition in educating and mentoring students in academia or professionals in the industrial or governmental sectors. Specific accomplishments include effectiveness in the development of innovative education, continuing education programs, authorship of textbooks, presentation of short-courses at EDS sponsored conferences, participation in the EDS Distinguished Lecturer program, and teaching or mentoring awards.

Since this award is solely given for contributions to education, the nomination should exclude emphasis on technical contributions to engineering and physics of electron devices.

Nomination forms can be found on the EDS website: http://eds.ieee.org/education-award.html

The deadline for the submission of nominations for the 2019 award is September 1, 2019.

2018 EDS Early Career Award Winner

The EDS Early Career Award recognizes young IEEE EDS members who have made outstanding contributions in an EDS field of interest during the early years of their professional career after graduation.

The 2018 EDS Early Career Award was presented to Manan Suri of Indian Institute of Technology-Delhi, New Delhi, Delhi and Lukas Czornomaz of IBM Research—Zurich, Zurich, Switzerland at the EDS awards dinner held in conjunction with the International Electron Devices Meeting in San Francisco, on December 2, 2018.

Manan Suri is an Assistant Professor at the Indian Institute of Technology-Delhi. His research interests include- Neuromorphic Hardware, Advanced Non-Volatile Memory Technology and its Emerging Applications. Dr. Suri has filed several patents, authored books and published more than 50 papers in reputed international conferences and journals. He is one of the very few young scientists to be featured on not one but rather two MIT Technology Review Innovator Under 35 lists. He was recognized as an Inventor in the MIT-TR 35 Global list, as well as one of the top 10 Indian innovators on the MIT-TR India list, for the year 2018.

The National Academy of Sciences recognized Dr. Suri's work with the Young Scientist Award2017, and the Institute of Engineers honored him with the Young Engineers Award-2016. Dr. Suri received the Laureat du Prix (Outstanding PhD Thesis Award) from the French Nanosciences Foundation in 2014. Dr. Suri is a visiting scientist at CNRS and serves as an advisor, consultant and steering committee member for leading global neuromorphic hardware companies. In past, he has worked with NXP Semiconductors-Central R&D, Belgium and CEALETI, France. Dr. Suri received his PhD from Institut Polytechnique de Grenoble (INPG) in 2013, M.Eng. and B.S from Cornell University in 2010 and 2009 respectively. Backed by pioneering R&D efforts, Dr. Suri recently founded a Deep-Tech AI/ Neuromorphic Hardware Startup called CYRAN AI Solutions.

Lukas Czornomaz (Member, IEEE) is a member of the Research Staff at IBM Research – Zurich in Switzerland. He was born in 1988 and received his engineering degree in physics and material sciences from the National Institute of Applied Sciences in Toulouse (France) and PhD in Nanoelectronics and Nanotechnology from the University of Grenoble Alpes (France).

Since joining IBM in 2010, he has been focusing his research on the integration of functional materials and devices with CMOS for logic, high-speed RF and photonics applications. Notably, he developed key integration methods for III-V compound semiconductors on Si yielding the first and only demonstrations to date of hybrid InGaAs/SiGe CMOS circuits on Si substrates, as well as state-of-the-art logic and RF performance for III-V MOSFETs on Si. More recently, he is exploring how this platform can be leveraged for cryogenic electronics for Quantum computing as well as how it can impact the field of integrated optics for high-speed optical communication. In addition, in 2018 he has joined the team managing IBM Research's world-wide Industrials and Internet-of-Things (IoT) strategy.

He is key author of more than 50 filed patents, 80 research contributions and 25 invited talks or tutorials including more than a dozen papers at IEDM and VLSI. He is or has been a member of the technical program committee of the IEEE IEDM, IEEE ESSDERC and IEEE EDSSC conferences. He received several awards and recognitions including VLSI Best Student Paper Award (2016), IBM Master Inventor (2017), CS Industry Innovation Award (2017), 3x IBM Outstanding Technical Achievement Award (InGaAs/SiGe CMOS–2017, CELO III-V Epitaxy Technology–2018, 3D Monolithic Technology–2018).

His dedication to the co-integration of dual-channel transistors and his strong taste for technical deep-dives in very heterogeneous topics strangely translated in his private life as being the happy father of twins and being an enthusiast diver exploring the deep waters across the globe.

Fernando Guarin
2018 EDS Early Career Award Chair
Global Foundries
Hopewell Junction, NY

CALL FOR NOMINATIONS

2019 IEEE EDS Early Career Award

Description: Awarded annually to an individual to promote, recognize and support Early Career Technical Development within the Electron Devices Society's field of interest

Prize: An award of US$1,000, a plaque; and if needed, travel expenses not to exceed US$1,500 for a recipient residing in the US and not to exceed US$3,000 for a recipient residing outside the US to attend the award presentation.

Eligibility: Candidate must be an IEEE EDS member and must have received his/her first professional degree within the 10th year defined by the August 15 nomination deadline and has made contributions in an EDS field of interest area. Nominator must be an IEEE EDS member. Previous award winners are ineligible.

Selection/Basis for Judging: The nominator will be required to submit a nomination package comprised of the following:

- The nomination form that is found on the EDS web site, containing such technical information as the nominee's contributions, accomplishments and impact on the profession or economy and a biographical description.
- A minimum of two and a maximum of three letters of recommendation from individuals familiar with the candidate's technical contributions and other credentials, with emphasis on the specific contributions and their impacts.

The basis for judging includes such factors as: the demonstration of field leadership in a specific area; specific technical contribution(s); impact on the profession or economy; originality; breadth; inventive value; publications; honors; and other appropriate achievements.

Schedule: Nominations are due to the EDS Executive Office on August 15th each year. The candidate will be selected by the end of September, with presentation to be made in December.

Presentation: At the EDS Awards Dinner that is held in conjunction with the International Electron Devices Meeting (IEDM) in December. The recipient will also be recognized at the December EDS BoG Meeting.

Nomination Form: Complete the nomination form by August 15, 2019. All endorsement letters should be sent to l.riello@ieee.org by the deadline.

For more information contact: l.riello@ieee.org or visit: http://eds.ieee.org/early-career-award.html

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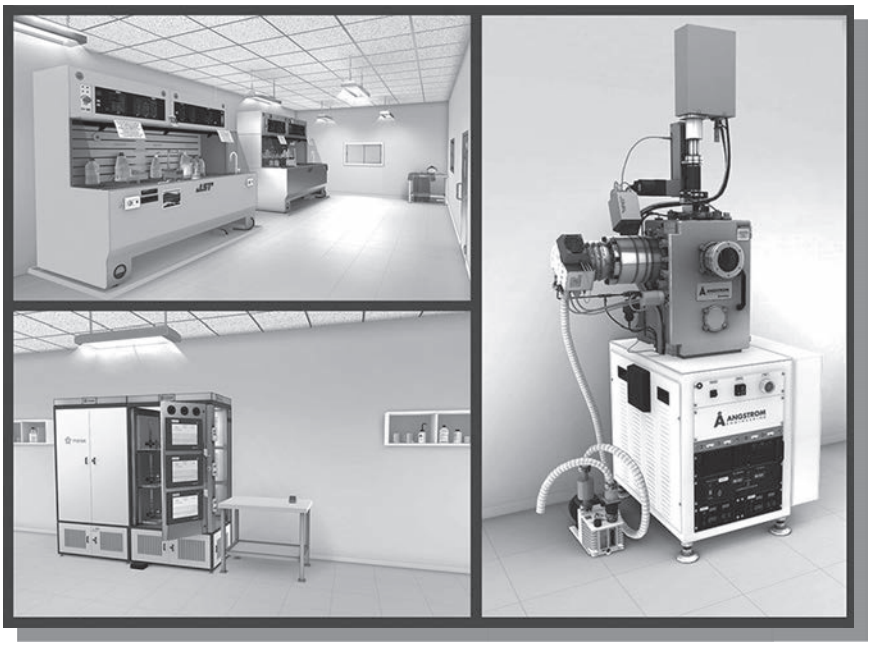
Muhammad Mustafa Hussain, PhD



vFabLab™ is an online based virtual environment, which is designed to help training on semiconductor device fabrication processes and associated CMOS technology equipment for anyone before accessing the cleanroom facilities in person. Inspired by the vision to provide access to thousands of students and other enthusiasts who do not have access to expensive cleanroom facilities, IEEE Electron Devices Society Distinguished Lecturer, Editor of IEEE Transactions on Electron Devices and IEEE EDS Region 8 Vice Chair Dr. Muhammad Mustafa Hussain, Professor, Electrical Engineering, KAUST and Visiting Professor, EECS, University of California, Berkeley has conceptualized and devised this online based virtual environment. An interested user needs to register for an account after watching an introductory video and can access the full version without any fees. Please visit https://vfablab.org/. All the data are secured and not used or traded under any circumstance. The virtual lab trains the user in end-to-end device fabrication sequence using well-tested process recipes. After each of the training session, the trainee can participate in an interactive Q&A. This platform is designed for desktop or laptop only at this moment. A mobile App version of this tool will become available in the summer of this year. An advanced Virtual Reality based platform will be launched next year. Professor Hussain envisions this platform to be an open access and open source dynamic platform, which will integrate multi-disciplinary lab/experiment—based components and will serve as catalyst for more impactful CMOS and non-CMOS technology development from both processing and equipment perspectives. For example, current modules for a specific processing step are based on recipes and equipment from one vendor, but in the future experienced users may be able to add their own tested recipes and instructions for equipment from other vendors. " This is a remarkable educational tool developed by Professor Hussain" said EDS President-elect Meyya Meyyappan, who added "students can get device fabrication training right at their desk and this virtual tool is going to be very popular, especially in Regions 9 and 10 where a vast majority of our members do not have access to advanced facilities." The first phase of this program development was sponsored by Dr. Mootaz Elnozahy, Dean, Computer Electrical Mathematical Science and Engineering Division of KAUST. For more information, please contact: info@vfablab.org.

Updates from the 2018 EDS Masters Student Fellowship Winners

Carmen M. Lilley
EDS Student Fellowship Committee Chair

The Electron Devices Society Masters Student Fellowship Program was designed to promote, recognize, and support Masters level study and research within the Electron Devices Society's field of interest.

Neel Chatterjee is converting to the PhD program from the MS program at University of Minnesota.

I am currently working on modelling, simulation and fabrication of metal oxide nanocrystalline thin film transistors.

Yu-Chieh Chien is currently doing his internship project at Imec with the Department of Large Area Electronics. Here, his research is focusing on reliability study and device integration on novel a-IGZO devices.

Since winning, I have been largely aspired by this fellowship that pushed me to work harder than before.

Carmen M. Lilley
EDS Student Fellowship Committee Chair
University of Illinois at Chicago
Department of Mechanical Engineering
Chicago, IL, USA

Updates from the 2018 EDS PhD Student Fellowship Winners

Carmen M. Lilley
EDS Student Fellowship Committee Chair

The Electron Devices Society PhD Student Fellowship Program was designed to promote, recognize, and support PhD level study and research within the Electron Devices Society's field of interest. The 2016 EDS PhD Student Fellowship recipients were:

Chen Jiang—University of Cambridge, England

Junkai Jiang, University of California, USA

Yuanyuan Shi, Rovira I Virgili University, Spain. B

Chen Jiang is a PhD candidate at the University of Cambridge, who research supervisor is Professor Arokia Nathan. He worked on exploring novel electronic devices for low-power, low-cost electronics, encompassing device fabrication, and device physics and modeling. He has a breakthrough in printed organic transistors, of which the power is as low as nanowatt and the transconductance is approaching the thermionic limit. This work has been recently published in Science (DOI: 10.1126/science.aav7057). His work has opened new potential for wearable/implantable real-time sensing. A video demonstrates this potential can be found online (http://science.sciencemag.org/highwire/filestream/722768/field_highwire_adjunct_files/1/aav7057s1.mp4).

Junkai Jiang I am extremely honored to receive this prestigious award from the IEEE Electron Devices Society that recognizes technological innovations by young Ph.D. student researchers. Being the third student from the Nanoelectronics Research Lab (NRL) at UCSB to receive this award, I would like to specially thank my advisor, Professor Kaustav Banerjee, not only for his constant encouragement and support, but also for his inspirational guidance to identify and pursue cutting-edge research of the highest caliber, which helped me to progress steadily during the past several years of my doctoral research. On the basis of previous studies of emerging 2D materials conducted in the NRL directed by Professor Banerjee, my research is focused on on-chip interconnects and passives uniquely enabled by low-dimensional carbon nanomaterials such as graphene. Supported by this award, I am now working on integrating graphene and its intercalation compound in a CMOS-compatible process and their application in multilayer interconnect scheme to establish its readiness for large-scale semiconductor manufacturing.

Yuanyuan Shi is currently pursuing her PhD degree in Nanoscience at Rovira i Virgili University, under the supervision of Prof. Mario Lanza. She worked 12 months at Stanford University (H.-S. Philip Wong's group) on 2D materials based electronic synapses for neuromorphic applications, and her results were published in Nature Electronics and IEDM 2017. Yuanyuan has published 45 articles, two book chapters, and two international patents (one of them received 1 M$ investment).

She has attended 13 international conferences, and in 6 of them gave an oral presentation. She has received the 2018 Chinese Government Award for Outstanding Self-Financed Students Abroad. She is a student member of IEEE, EDS, and RSC, and she serves as an active reviewer for several international journals, such as Scientific Reports, Thin Solid Films and ChemElectroChem.

Carmen M. Lilley
EDS Student Fellowship
Committee Chair
University of Illinois at Chicago
Chicago, IL, USA

Make Some Time to View New Webinars Available in The EDS Collection

EDS is many things to its members—scientific publisher, technical conference sponsor, networking resource—but at its core EDS is a community of learning. From undergraduate students and PhD candidates to tenured professors and world-renowned researchers, EDS provides device engineers from across the spectrum engaging and enriching educational opportunities.

As part of our commitment to enhancing the value of membership in EDS, we are pleased to present the EDS Webinar Archive. The online collection provides our members with on-demand access to streaming video of past events. Recently held webinars can be accessed here, http://eds.ieee.org/webinar-archive.html

Topic: Thin Film Transistor Integration Strategies for Ultra Low Power and High Gain
Presented by: Arokia Nathan

Abstract
This webinar will review the integration of oxides and fully printable organics for newly emerging application areas related to wearables and the Internet of Things. We will discuss the critical design considerations to show how device-circuit interactions should be handled and how compen-

sation methods can be implemented for stable and reliable operation. In particular, the quest for low power becomes highly compelling in wearable devices. We will discuss thin-film transistor operation in the different regimes, and review device properties when operated in the deep sub-threshold regime or in near-OFF state, addressing the pivotal requirement of low supply voltage and ultralow power leading to potentially battery-less operation.

Topic: High-Performance III-N Devices and Integration Technologies for Advanced System Applications
Presented by: Patrick Fay

Abstract
Gallium Nitride (GaN) and related III-N materials offer the promise of exceptional levels of performance for RF, microwave, and mm-wave applications, as well as for power conversion and control. This outstanding performance potential is due in large part to the combination of a large band gap with high critical electric field, high carrier mobility and saturation velocity, and the effects of spontaneous and piezoelectric polarization that enable high sheet carrier concentrations to be achieved without extrinsic doping. These features have led to remarkable device performance, ranging from devices with ft/fmax near 500 GHz in ultra-scaled HEMTs to high-power, high-voltage rectifiers and transistors capable of handling voltages well above 1500 V and 10 A by using vertical device architectures on bulk GaN substrates. For these devices to have maximum system-level impact, however, heterogeneous integration with Si-based electronics and compatibility with advanced packaging platforms is needed. In this talk, recent demonstrations of high-performance GaN-based devices for RF through mm-wave applications, as well as for power conversion and control will be described, and novel advanced processing techniques that promise to enable these devices to be heterogeneously integrated with Si and advanced packages while retaining the unsurpassed performance possible with GaN will be discussed.

Chapter News

IEEE Introduces New Volunteer Expense Reimbursement Platform

Say goodbye to the tedious and inefficient paper-based expense report process. Beginning in Q4 2018, IEEE began rollout of its new Volunteer Expense Reimbursement tool, Concur. A cloud-based expense reporting and reimbursement platform, Concur is designed to create a fast and efficient electronic reimbursement experience for IEEE volunteers.

Among other benefits, volunteers will enjoy faster reimbursements of expenses, the ability to track real time status of expense reports, a convenient mobile app that lets you build, update, or approve expense reports while on the go, and the ability to upload images of receipts at any time.

Get an overview of the new platform, its multi-phase rollout schedule, and how to contact Concur's user support desk *here*. View a brief informational video *here* (Note: Features such as Concur Request and TripLink will not be immediately available for expense reimbursement). View a comprehensive video tutorial *here*. For general questions, contact IEEE's project team at concurfeedback@ieee.org.

Event Conduct and Safety Statement

IEEE believes that science, technology, and engineering are fundamental human activities, for which openness, international collaboration, and the free flow of talent and ideas are essential. Its meetings, conferences, and other events seek to enable engaging, thought-provoking conversations that support IEEE's core mission of advancing technology for humanity. Accordingly, IEEE is committed to providing a safe, productive, and welcoming environment to all participants, including staff and vendors, at IEEE-related events.

IEEE has no tolerance for discrimination, harassment, or bullying in any form at IEEE-related events. All participants have the right to pursue shared interests without harassment or discrimination in an environment that supports diversity and inclusion. Participants are expected to adhere to these principles and respect the rights of others.

IEEE seeks to provide a secure environment at its events. Participants should report any behavior inconsistent with the principles outlined here, to on site staff, security or venue personnel, or to eventconduct@ieee.org.

SAVE THE DATES—IEEE EDS Mini-Colloquium in Tarragona, Spain

Dear IEEE EDS members,

In April, two DLs took place.

On April 1st, the Kuei-Shu Chang-Liao Distinguished Lecture was held in Grenoble. Detailed information is available from Francis Balestra (francis.balestra@grenoble-inp.fr).

The second DL was on April 4th, the Joao Martino Distinguished Lecture in Tarragona. Here, Benjamin Iniguez Nicolau (benjamin.iniguez@urv.cat), is the responsible contact for further information.

Please keep the following upcoming MQ of Region 8 in mind. On May 24th, the Spain Mini-Colloquium in Tarragona will be held. Detailed information is available from Lluis Marsal (lluis.marsal@urv.cat).

~ Mike Schwarz, Editor

Save the Date—IEEE EDS Mini-Colloquium "Nanoelectronics—Technology, Design, Modeling"

By Krzysztof Górecki

An EDS Distinguished Lecturer Mini-Colloquium "Nanoelectronics—Technology, Design, Modeling" will be carried out (while preparing this note) in Rzeszow, Poland, on June 26, 2019. The MQ will give an extensive view at numerous aspects of nanoelectronics.

The following experts will take part in the MQ and share their expertise with the audience:

- Prof. Shinichi Takagi (The University of Tokyo) with a lecture "Tunneling FET technology for ultra-low power logic applications";
- Prof. Andrzej Strójwąs (Carnegie Mellon University) with a lecture on the state-of-the art processes and their diagnostics;
- Dr. Arkadiusz Malinowski (GlobalFoundries) with a lecture on integration of processes for FinFET-based IC manufacturing;
- Dr. Rajiv V. Joshi (DL) (IBM Research Division Yorktown Heights, NY) with a lecture on low-power and/or variability aware IC design (to be confirmed);
- Prof. Henryk Przewłock (DL) (Institute of Electron Technology, Warsaw) with a lecture on a deep insight into photoelectric measurements of MIS systems;
- Prof. Marcelo Pavanello (DL) (Centro Universitario FEI) with a lecture "Performance and modeling of Nanowire-based MOSFETs";
- Dr. Farzan Jazaeri (EPFL) with a lecture on modeling of devices in the ultra-low temperature range;
- Prof. Mike Brinson (London Metropolitan University) with a lecture "Equation-Defined template and synthesis driven compact modelling of semiconductor devices";
- Dr. Władek Grabiński (DL) (MOS-AK) with a lecture on theFOSS tools for support of IC modeling and design with special emphasis on Verilog-A standardization;

The Mini-Colloquium will be organized by the ED Poland Chapter with collaboration of Gdynia Maritime University, Instytut Technologii Elektronowej (ITE), Warsaw, and Department of Microelectronics and Computer Science, Lodz University of Technology. The MQ will be held in Grand Hotel Rzeszów Sp. z o.o. ul. Kościuszki 9, 35-030 Rzeszów, Poland.

The details and registration form for the MQ are available on the EDS website https://eds.ieee.org/lectures.html?eid=603. Participation in the MQ will be free of charge.

~ Daniel Tomaszewski, Editor

Report of the 2018 IEEE S3S Conference

by Ali Khakifirooz

The 2018 IEEE S3S Conference was held October 15–18, at the Hyatt Regency San Francisco Airport. This year marked the 44th anniversary of the conference and attracted more than 190 attendees from around to discuss the latest advancement in SOI technology, 3D integration, low-voltage devices and low power circuits. The conference started with six plenary talks and was followed by 101 technical presentations through 2 parallel tracks and a poster session. The plenary talks were:

- John Pellerin, Deputy CTO and Vice President of GLOBALFOUNDRIES' Worldwide Research and Development, "Enabling market innovation through differentiated FDSOI technology."
- Jan Rabbaey, Donald O. Pederson Distinguished Professor, University of California, Berkeley, "Powering the human intranet."
- Joe Macri, Corporate Vice President, Product CTO and Corporate Fellow of AMD, "Left, right or up. Living in a 3D world."
- Gurtej Sandhu, Senior Fellow and Vice President, Micron Technology, "The memory futures."
- David Divincenzo, Director of the Institute for Quantum Information, RWTH Aachen University, "Components of high-fidelity solid state quantum computers."
- Thomas Piliszczuk, Executive Vice President at Soitec, "Material and device innovation for IoT, automotive and mobile connectivity applications."

The conference continues to provide excellent educational opportunities. This year, we held the 24th short course on Thursday on "Emerging applications of FDSOI technology" covering a wide spectrum of FDSOI circuit design topics such as low-power and high-performance logic, low-voltage SRAM, power management and PPA optimization, EDA tools, as well as applications in automotive and mmW and THz design. This full-day short course attracted more than 50 attendees and was a successful continuation of last year's short course on the same topic.

Dr. John Pellerin giving a plenary talk at 2018 IEEE S3S Conference

In addition, we also offered a half-day tutorial on Quantum Computing on Tuesday afternoon where experts from academia and research institutions taught fundamentals of this emerging field from basics of quantum error correction, to design of quantum computing circuits and interfacing to classical world and to Si MOS-based qubits and scalable quantum processors. The tutorial was well received by the audience and sparked lively discussions throughout the session and during breakout.

On Monday evening, we hosted a very exciting rump session entitled: "Is 3D really a replacement for Moore's law" organized and moderated by Prof. Paul Franzon of North Carolina State University. Panelists included Carlos Diaz (TSMC), Robert Patti (nHanced Semiconductors), Sung-Kyu Lim (Georgia Institute of Technology), and Sergey Shumarayev (Intel).

During the Monday reception we held a special poster session in which students participating in Stanford's SystemX program presented their work. Based on positive feedback we have received from S3S attendees this year as well as in the past two years where students from Berkeley's E3S center presented their work, we plan to continue our partnership with local universities to bring more technical content to the S3S attendees. We also partnered with the CoolCubeTM/3D VLSI Open Workshop organized by Leti, IRT NanoElec and Qualcomm as we have done in the past few years.

We are planning a special issue of the IEEE Journal of Electron Devices Society that will cover extended versions of a selected group of the papers presented at the conference, as we did last year. Dr. Nobuyuki Sugii of Hitachi and myself are serving as the Guest Editors of the journal and are on track to publish the special issue in early 2019.

The 2019 edition of the conference will be held October 14–17, at San Jose DoubleTree. On behalf of the organizing committee of the conference, it is my pleasure to invite you to attend the conference. For more information please visit the conference website s3sconference.org. Deadline for paper submission is May 25th and look forward to your strong participation.

~ Kyle Montgomery, Editor

ED Schenectady Chapter Distinguished Lectures

by Devika Sil

EDS Distinguished Lectures given by IEEE Fellows Mukta Farooq and Rajiv Joshi

The IEEE Electron Devices Society (EDS), Schenectady Chapter along with the IBM Albany Technical Vitality Council, SUNY Poly and Tokyo Electron Limited hosted the 2018 IEEE Nanotechnology Symposium (ANTS). The ED Schenectady Chapter was the sole sponsor for this event which was held at the SUNY Poly campus in Albany on November 14–15, 2018. The conference featured oral presentations and posters by authors from industry, academia and research institutions. The goal of the conference was to promote cross-functional and interdisciplinary research and provide the opportunity to present recent work related to semiconductor scaling, packaging, manufacturing, memory technologies, artificial intelligence and nanosciences. There were 144 registered attendees for the Symposium with 39 presenters. There were also two EDS Distinguished Lectures given by Mukta Farooq, IBM, IEEE Fellow and Rajiv Joshi, IBM, IEEE Fellow. Mukta gave an overview lecture on Heterogeneous Integration and Rajiv's talk was titled "Brainstorming in Silicon."

The conference also featured 4 invited talks by Nathan Cady from SUNY Polytechnic Institute, Myung Hee Na from IBM, Anuradha Murthy Agarwal from MIT, and Robert Hull from RPI. A BEOL tutorial was given by IBM Engineers Prasad Bhosale, Koichi Motoyama and Son Nguyen. The plenary lecture was delivered by Dr. John Cohn, IBM Fellow. John's talk was titled "Digital Disruption: An Engineer's Perspective on Life, the Internet of Things and the Importance of Play." Overall this year's conference was a successful event and well attended by members of academia and industry.

~ Rinus Lee, Editor

Gift of IEEE Membership Now Offers Society Membership

Members and non-members can now add Society membership when giving the Gift of IEEE Membership. The new option to add Society memberships is currently available as part of the half-year membership period, where IEEE and Society memberships are half price. Give the Gift of IEEE Membership for half price is available for the entire half-year period (March 1st through August 15th).

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SAVE THE DATE—Symposium on Schottky Barrier MOS Devices "Towards Neuromorphic and Quantum Computing Applications" Organized by ED France Chapter & Universite Paris-Sud

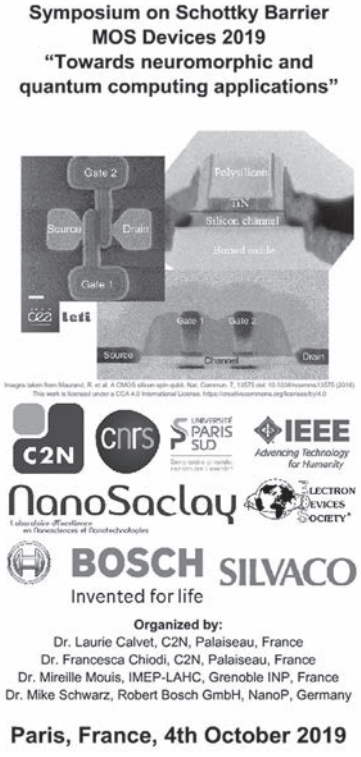
A symposium on Schottky Barrier MOS (SB-MOS) devices is planned for October 4th at the new Center for Nanoscience and Nanotechnology laboratory in Palaiseau, France. This is the third meeting of an enthusiastic group of Schottky barrier researchers and this year it is sponsored by LabexNanoSaclay, the IEEE ED France chapter, the Robert Bosch GmbH and Silvaco Inc.

This year the theme of the symposium is "Towards neuromorphic and quantum computing applications" organized by Dr. Laurie Calvet (C2N, Palaiseau, France), Dr. Francesca Chiodi (C2N, Palaiseau, France), Dr. Mireille Mouis (IMEP-LAHC, Grenoble INP, France) and Dr. Mike Schwarz (Robert Bosch GmbH, NanoP THM, Germany) and the staff at the Centre of Nanoscience and Nanotechnology at the Université Paris-Sud.

The symposium starts on October 4th at 9:00 am and the following speakers have confirmed their invitations: Prof. Benjamin Iniguez (DEEEA, Universitaet Rovira I Virgili), Dr. Laurie E. Calvet (C2N, CNRS-Université Paris-Sud), Dr. Mike Schwarz (Robert Bosch GmbH, NanoP THM, Germany), Dr. David Green/Dr. Ahmed Nejim (Silvaco Inc.), Dr. John Snyder (JCAP, LLC), Dr. Francesca Chiodi (C2N, CNRS-Université Paris-Sud), Dr. François Lefloch (CEA, Grenoble), Dr. Fabrice Nemouchi (CEA, Grenoble).

Attendees are welcome to attend the symposium. Further information are present at https://ssbmos.blogspot.com

~ Mike Schwarz, Editor



ED NIT Silchar Student Chapter Organizes Mini-Colloquium

by T R Lenka

The ED NIT Silchar Student Chapter successfully organized an EDS Sponsored Mini-Colloquium (MQ) on November 3, 2018 with Distinguished Lectures by Prof. C. K. Sarkar, Prof. G. N. Dash, Prof. Manoj Saxena. Prof. C. K. Sarkar delivered a talk on "Electronic and Biochemical Applications of Green Synthesized Noble Metal Nanoparticles." Prof. G. N. Dash delivered a talk on "SiGe Bandgap Engineering for Bipolar VLSI Design," and Prof. Manoj Saxena delivered a talk on "Novel Junction-Less (JL) Transistor Designs."

(left to right) Dr. S. K. Tripathy (Faculty), Dr. T. R. Lenka (Faculty Advisor), Prof. F. A. Talukdar (HOD & Branch Counselor), Prof. Manoj Saxena, Prof. C. K. Sarkar, Prof. Sivaji Bandyopadhyay (Director, NIT Silchar), Prof. G. N. Dash, Prof. S. Baishya (Dean Academic, NIT Silchar), Dr. Koushik Guha (Treasurer)

Sixty enthusiastic participants comprising of IEEE EDS members and student members and non-members of NIT Silchar attended the program.

IEEE EDS Distinguished Lecture—ED Uttar Pradesh Section—Kanpur Chapter

by Yogesh Chauhan

The ED Uttar Pradesh Section Kanpur Chapter, jointly with the Department of Electrical Engineering, IIT Kanpur, organised a DL talk on "Electromigration Simulation at Circuit Levels," by Prof. Tan Cher Ming (Electronic Department, Chang Gung University, Taiwan) on September 05, 2018. The program was inaugurated with an informative talk on the benefits of IEEE and EDS memberships for researchers. Then, Prof. Ming explained in a comprehensive manner electromigration, one of the dominant failure mechanisms for interconnects in ULSI. Extensive investigations on the understanding of electromigration and methodologies to improve interconnect EM lifetime were presented. He highlighted the method to perform electromigration modelling at the circuit level. Examples were shown for digital, analog and RF circuits. In order to make the method practical for implementation, the ways to speed up the modelling in complex circuits were also presented. The talk was attended and nicely received by over 60 attendees, which included students, researchers and faculty members.

Participants of the EDS Distinguished Lecture at IIT Kanpur

The ED Kanpur Chapter, jointly with the Department of Electrical Engineering, IIT Kanpur organized a DL by Prof. Shunri Oda, IEEE Fellow and Professor, Department of Physical Electronics and Quantum Nanoelectronics Research Center, Tokyo Institute of Technology, on November 16, 2018. Dr. Oda delivered a lecture on "Low-dimensional-structure devices for future electronics." He focused on one of the major application targets for future electronics, which is wearable communication tools with low-power consumption. He emphasised that 2D materials and 1D nanowires attract attention not only because these materials would be suitable for the fabrication of TFETs, but also various novel applications such as sensors, displays would be possible.

Another lecture by Dr. Bhaskaran Muralidharan, Professor, Department of Electrical Engineering at IIT Bombay, who spoke on "Series quantum resistors—Electronic analog of optical phenomena for Spintronics" on October 29, 2018. In his talk, while keeping the motif of "multiple quantum resistors," he drew attention to next generation applications in the realm of spintronics and energy conversion, commonly referred to as spin-caloritronics. The talks were successfully attended and received by over 50 attendees, which included students and faculty members.

IEEE EDS Distinguished Lecturers at ED Meghnad Saha Institute of Technology Student Branch Chapter

by Manash Chanda

The chapter in association with Department of ECE, Meghnad Saha Institute of Technology (MSIT) organized two IEEE EDS Distinguished Lectures by Prof. Subir Kumar Sarkar of the Dept. of ECE, Jadavpur University, Kolkata, India on July 31, 2018 on "Renovation and Innovation in nano-device structures for performance improvement" and "Computation without power dissipation." More than ninety students attended the event.

The chapter in association with Department of ECE, MSIT organized one day Industry Academia Meet at VLSI Lab, Dept. of ECE, MSIT on August 14, 2018. In the program, Mrs. Hena Roy, Principal Engineer, Centre for Development of Advanced Computing (C-DAC), Kolkata discussed various cutting-edge embedded technologies and motivated the students towards research on embedded systems. More than thirty-eight students

attended the event. The chapter organized the "Tech-Intellect"- a student paper contest chaired by Dr. Swapnadip De on November 25, 2018 at the hotel Pride. The Student Paper Contest was organized to practice and improve both written and verbal communication skills of the undergraduate student member. Throughout an engineer's career, he/she will be constantly called upon to communicate ideas to others. Researching, writing, and presenting a paper provides a student with invaluable early experience in expressing ideas related to engineering. 10 out of 36 student papers were accepted for presentation and 18 IEEE student members participated in the contest. An IEEE membership awareness program was arranged by the EXECOM members on November 30, 2018.

ED Meghnad Saha Institute of Technology Student Branch Chapter

~ Manoj Saxena, Editor

Chapter Educational Outreach

Engineers Demonstrating Science: an Engineer Teacher Connection (EDS-ETC) by ED Malaysia Chapter

by Rosminazuin Ab Rahim, Norfarahidah Za'bah & Aliza Aini Md Ralib

Several EDS-ETC events were held by ED Malaysia in the fourth quarter. ED Malaysia participated in the Science, Technology, Engineering & Mathematics (STEM) Teachers Colloquium organized by the Malaysian Ministry of Education on 14th August 2018 at Universiti Malaysia Kelantan. A total of 50 participants attended the colloquium and ED Malaysia was represented by Dr. Rosminazuin from IIUM. An exhibition booth was set up to promote Teacher-In-Service Program (TISP) as well as EDS-ETC among teachers and students. A Train-the-Trainer Program was held at IIUM to train undergraduate and postgraduate students as facilitators for EDS-ETC school programs on October 4, 2018. A total of 7 IIUM students were trained to use the Elenco Snap Circuits® Kits.

An EDS-ETC@Avicenna Race was held on October 20, 2018 at IIUM and targeted to instill interest in the field of electrical and electronics engineering among school students. In addition, the program also strengthens the mentor-mentee (IIUM students-school students) bonding through interactive activities and was attended by 100 school students and 80 university students.

EDS-ETC@Orphan3.0 was also held on October 20, 2018 and was a community service program for 100 underprivileged students at Rumah Penyayang Darul Ilmi Gombak. The underprivileged students were happy and excited to explore the wonderful world of electronics using the Snap Circuits® Kits.

And last but not least, Persatuan Saintis Islam Malaysia (PERINTIS Youth) and ED Malaysia jointly organized a young scientist program, "Young Muslim Explorer," which was held at the Kulliyyah of Engineering IIUM on December 1, 2018 and was participated by 22 young school students.

EDS-ETC programs held by ED Malaysia Chapter

~ P. Susthitha Menon, Editor

IEEE Electronic Exploration Camp IEEE ED/SSC HK Joint Chapter and the ECE Department of HKUST

by Yang Chai

As a continuation of a series of successful STEM (science, technology, engineering and mathematics) educational activities to inspire children to study and work in electronic engineering or related areas, the IEEE Electron Devices and Solid-State Circuits (ED/SSC) Hong Kong Joint Chapter and the Department of Electronic and Computer Engineering (ECE) of the Hong Kong University of Science and Technology (HKUST) co-organized a three-day Electronic Exploration Camp from December 27–29, 2018 at the scenic campus of HKUST, with state-of-the-art multimedia teaching facilities.

Schoolchildren getting to the campus of HKUST for the exciting three days of learning and fun

Both boys and girls took pleasure in the electronic circuit construction with instructional guidance by university student helpers

The series was initiated by Prof. Mansun Chan in 2012 and this is the 7th time for the event, with several dozen schoolchildren coming to HKUST to explore fascinating electronic technologies through electronic circuit construction sessions and lab tours. Through learning and trying to build a few interesting electronic circuits, in particular a running light indicator, an electronic piano and an infrared detector, participating kids have been introduced to major areas of ECE, namely digital integrated circuits, photonics, signal and multimedia processing. They also learned some key electronic engineering concepts such as voltage and current, signals, electrical measurements, clock generation and the use of mathematics in engineering, that are taught in electronic engineering programs at the university. While touring around the research and teaching laboratories, they were also exposed to other technology pillars of ECE such as nanosystem fabrication and applied electromagnetics and wireless communications. They were captivated by various experimental demonstrations in the research labs, especially when they were allowed to try the demonstrations by themselves. From previous years' successes, 18 student helpers were recruited in giving instructional guidance to 112 schoolchildren in the electronic circuit construction and other educational activities over the three days. With the skills developed in the camp, the participants have been encouraged to participate in the forthcoming IEEE Electronic Endeavor Match to be held on April 27, 2019 at HKUST. It is a competition for the participants to test their ability to understand the conceptual circuit diagrams and then build the functional electronic circuits on a breadboard in the shortest time.

IEEE Electronic Exploration Camp—ED Guangzhou Chapter

by Zhangang Zhang

ED Guangzhou Chapter co-hosted the 2018 IEEE Electronic Exploration Camp in Guangzhou. On July 26th, forty-eight local high school students from Guangzhou practiced the exploration course entitled "Exploration of Internal Structure of Chips", including interactive theory teaching, optical microscope operation, electron microscope and 3D X-ray equipment visit. The combination of theory and practice of this activity effectively stimulated the interest of middle school students on the chip structure. This year is the first time that the IEEE Electronic Exploration Camp has landed in Guangzhou. The series of activities have been carried out successively at the University of California (San Diego), the Hong Kong University of Science and Technology, Peking University, and the Institute of Microelectronics of the Chinese Academy of Sciences.

2018 IEEE Electronic Exploration Camp Participants

~Ming Liu, Editor

EDS-ETC by ED Netaji Subhash Engineering College Student Chapter

by T R Lenka

The ED Netaji Subhash Engineering College Student Chapter and the Alumni Association of National Gems (AANG), organised a workshop for the students of class XII of National Gems Higher Secondary School on August 24, 2018 on "Familiarization with various electronic components using Snap Circuits Kit" as an activity of the IEEE Electron Devices Society's EDS-ETC initiative to impart the knowledge of electronics among school students and inspire them to join Electrical and Electronics Engineering. Snap Circuits® kits, containing components to make more than 600 interesting projects, were provided by EDS for making the subject of electronics more interesting to students and giving hands on training on basic circuit making.The workshop commenced with an introduction to the wide platform provided by the field of electronics. It was followed by an interactive session where basic circuits were built using the components of the kit. Almost 35 enthusiastic students participated.

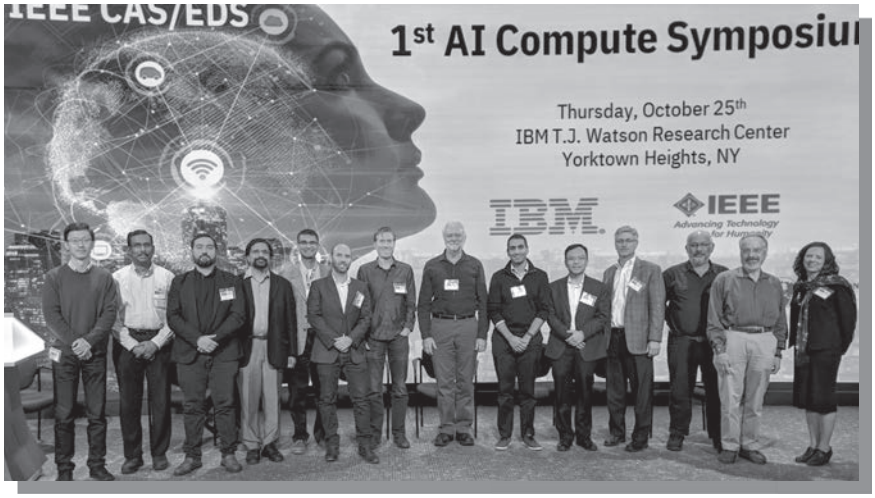
Workshop "Familiarization with various electronic components using Snap Circuits Kit"

~ Manoj Saxena, Editor

USA, Canada & Latin America (Regions 1-6, 7 & 9)

IEEE CAS, IEEE EDS, and IBM Research 1st AI Compute Symposium

—by Rajiv Joshi, Matt Ziegler, Arvind Kumar, Eduard Alarcon



Committee and Invited Speakers, L to R: Xin Zhang (IBM), Krishnan Kailas (IBM), Eduard Alarcon (UPC Barcelona Tech), Rajiv Joshi (IBM), Arvind Kumar (IBM), Matt Ziegler (IBM), Mike Davies (Intel), Rob Aitken (AMD), Naveen Verma (Princeton University), Wei Lu (University of Michigan, Ann Arbor), Todd Hylton (UC San Diego), Andreas Andreou (John Hopkins), Mark Wegman (IBM), Pamela Abshire (University of Maryland)

Together with the IEEE Circuits and Systems Society (CAS) and the IEEE Electron Device Society (EDS), IBM Research led the 1st AI Compute Symposium at the IBM T.J. Watson Research Center THINKLab in Yorktown Heights, NY, on October 25, 2018. This symposium brought together dreamers, thinkers, and innovators across industry and academia together for a one-day symposium focusing on cutting-edge research addressing AI Compute challenges and future directions of AI. The symposium consisted of two keynotes, six invited talks, a student poster session, and a panel discussion. The event was free of charge and had over 155 attendees from IBM, various companies and universities. IBM along with IEEE showcased leadership and advancement in the AI-Compute domain.

Keynote talks were delivered by Lisa Amini from IBM and Rob Aitken from ARM. Lisa Amini provided an overview of research projects from the MIT-IBM Watson AI Lab, which has recently celebrated a one-year anniversary. Amini described three tiers of AI research spanning narrow, broad, and general AI. She posited that the AI research community is beginning a journey into broad AI, whereas general AI is still a long-term goal for the future. Rob Aitken followed with a keynote address describing how many emerging AI problems present dynamically changing goals and rules, rather than the fixed goals and rules of conventional computing problems. Aikten also presented practical approaches for decomposing complex problems into manageable components that may provide a path for tackling complex AI challenges. Finally, he concluded that the IoT need distributed systems with AI and ML applications as IoT involves real time, explain-ability and security.

Following the keynotes, Mike Davies from Intel and Jeff Burns from IBM gave invited talks during the "Industry Perspectives" session. These talks provided a landscape of industrial research for both the near and long term, spanning architectural design, circuit design, and semiconductor technology. Mike Davies' talk focused on Intel's Loihi neuromorphic chip as well as future directions in neuromorphic research. Although Loihi is a digital chip, this avenue of research pushes beyond conventional von-Neumann architectures. On the other hand, Jeff Burns' talk focused on current efforts and future plans for deep learning acceleration. Burns described a vision beginning with specialized digital accelerators in the near term with enhancements based on analog circuit design and future device technology in the future.

Next, in the "Bio-inspired Computing" session, Andreas Andreou from Johns Hopkins University provided a number of examples of bio-inspired chip designs, many of which are components in systems that solve complex problems of interest to organizations like DARPA. In arguably the most provocative talk of the day, Todd Hylton from the University of California, San Diego, proposed the concept of thermodynamic computing as a potential future direction for computing research. Its evolution can be biased through programming, training and rewarding.

The third session on "Emerging Technologies" included talks by Wei Lu from the University of Michigan and Naveen Verma from Princeton University. Lu described recent research progress on RRAM (resistive random access memory) device and chip-level design and fabrication. He described how RRAM can provide a platform for neuromorphic computing, which is a

promising direction for future AI computing. Naveen Verma delivered a case for circuit and architectural approaches for in-memory computing, another topic of high interest to the community. He presented measurement results from several fabricated chips providing compelling evidence for in-memory computing potential.

The symposium also had a well-attended student poster session, where about 30 students presented compelling research spanning numerous topics in AI computing. Two best poster presentations were awarded. One award was given to Sohum Datta from UC Berkeley for work on "A 2048-dim General-purpose Hyper-Dimensional Processor." A second award was given to Jingcheng Wang from the University of Michigan for "Neural Cache: Bit-Serial In-Cache Acceleration of Deep Neural Networks."

The symposium closed with a panel discussion entitled "Artificial Intelligence or Artificial Stupidity: How smart will smart AI be?" The panelists included the keynote and invited speakers, as well as IBM Fellow Mark Wegman. A lively and at times heated debate ensued where topics from the progress in AI research to AI ethics were touched upon. Todd Hylton presented a case that while progress in narrow AI challenges have made progress, the community is far from approaching true intelligence. At times Andreas Andreou and Mark Wegman sparred over the future of AI research progress, while Naveen Verma wound up as the mediating voice. The panel discussion is scheduled to appear on IEEE TV in the near future.

Overall, the general consensus of attendees, speakers, and organizers was that day provided a great platform for educational forum and lively discussions related to the most current compelling topics in the computing field. Additional publications based on the symposium technical content are planned to provide educational resources for anyone interested. This year's AI-Compute symposium will be held on October 17, 2019 at T.J. Watson research center and student posters in this field are welcome. Although early in the stages, future events based on AI Compute are being planned by IBM and IEEE. Please see the following website, http://ibm.biz/AIcompute symposium, for updates.

Students in the clean room at University of Sao Paulo (USP) during the workshop

The organizers Joao Martino, Paula Agopian from University of Sao Paulo and the students of the 2018 microfabrication class

ED South-Brazil Chapter

—by Joao Antonio Martino

The annually **Hands on Microfabrication of SOI nMOSFET** for educational application was organized by the Polytechnic School of University of Sao Paulo and ED South-Brazil chapter. This is the only one SOI technology microfabrication course in Latin America. The graduate and undergraduate student were selected from different universities and research centers of Brazil. The course gave students an opportunity to study the main step process parameters to perform the microfabrication (clean room) and the electrical characterization of the SOI nMOSFET fabricated during the course. This hands on microfabrication was held at University of Sao Paulo on July 23–27, 2018 (40 hours) resulting in students fabricating a self-aligned polysilicon-gate Fully Depleted SOI nMOSFET. This course is opened for everyone of ED Region 9. The only limitation is due to the clean room facilities (12 students per course). For additional information, contact Prof. Joao Antonio Martino (martino@usp.br).

~ Edmundo Guiterrez, Editor

Europe, Middle East & Africa (Region 8)

2018 International Student's Projects Conference (IEEESTEC 2018)

—by Danijel Danković

The 11th International IEEESTEC Student's Projects Conference was held on November 29, 2018, at the Faculty of Electronic Engineering, University of Niš, Serbia. The conference was organized with the support of the Electrical Engineering Students' European Association local committee Niš, the IEEE Student Branch Niš, and the Faculty of Electronic Engineering at Niš. The event was also supported by the joint IEEE Electron Devices and Solid State Circuits Chapter, the IEEE Microwave Theory and Techniques Chapter, IEEE WIE Affinity Group and the IEEE Serbia and Montenegro Section. The event was also supported by the Serbian Academy of Sciences and Arts (SASA), Branch Niš, and Ministry of Education, Science and Technological Development of the Republic of Serbia.

IEEESTEC 2018 Conference opening

Presentation of practical projects

The welcome and opening speech was delivered by Danijel Danković, conference chair. The opening speech was followed by provost Dragan Denić, dean of Faculty of Electronic Engineering Dragan Mančić, and vice dean of Faculty of Electronic Engineering Nebojša Dončov. The conference proceeding contains 85 papers, covering a wide range of topics, such as electronics, information technologies, computing, microelectronics, telecommunication, power engineering etc. Based on evaluation of the quality of the papers, best paper awards were presented. Additional awards, the IEEE Women in Engineering award, the MTT Special award, and award for the best paper proposed for the IEEE Region 8 Student Paper Contest 2019 were given. Also, awards were assigned for the papers with the best practical implementation.

All participants had the opportunity to present posters and demonstrate their projects. The conference was visited by over than 500 high school and academic students. There were three types of workshops for students of high school and elementary school: Arduino programming, workshop with ELENCO Snap Circuits® Kits and workshop for basic electronic circuits realized on a breadboard.

It is important to note that this year, paper from our conference proposed for the IEEE Region 8 Student Paper Contest 2018, entitled "Fooling a neural network with common adversarial Noise," by Nikola Popović and Marko Mihajlović, won the third place in this competition in Marrakech in Morocco.

More information about IEEESTEC conference can be found at http://ieee.elfak.ni.ac.rs

~ Marcin Janicki, Editor

ED Romanian Chapter

—by Cristian Ravariu

The ED Romania Chapter held an exciting talk by Distinguished Lecturer Prof. Vijay K. Arora from Department of Electrical Engineering and Physics from Wilkes University on "What's Next Beyond

Prof. Arora gives an exciting talk to the ED Romania and IEEE members with a large audience of students, professors, and specialists from industry

BMOS-5 nm". The meeting was held on November 1, 2018, in Universitatea Politehnica Bucuresti, Bucharest, Romania. The visit of Professor Arora in Romania to meet the Electron Devices Society members and Romanian specialists occurred between October. 31-Nov. 2, 2018. The visit was accompanied by a series of round tables, discussions, contacts with students and EDS members, and the exciting colloquium. Prof. Arora emphasized that nanowire devices, tunneling devices and new electron devices will inherently be the focus of the electron device community in the next decade, and especially beyond the year 2020 when CMOS reaches its physical limits. More than 50 people attended the colloquium. The event was supported by IEEE Romania Section, and by the local chapter ED Romania. It was co-sponsored by the IEEE EDS DL Program, by the SSCS Romania local chapter, and by the Project PN-III-P4-ID-PCE-2016-0480 TFTNANOEL nr. 4/2017-2019.

~ Daniel Tomaszewski, Editor

Asia & Pacific (Region 10)

EDS Distinguished Lectures—ED Taipei Chapter

—by Steve Chung

The ED Taipei Chapter together with the EDS NCTU student chapter held three invited talks in the fourth quarter of 2018. The first event was given on November 21, in which Prof. Albert G. C. Liang, National University of Singapore, was invited to give a talk titled, "Non-volatile Electronics based on Spin-Torque Switching Mechanism." In this talk, he first gave the general introduction of spintronics, different spin-torque switching mechanisms in MTJ, and then some potential applications in logic and memory devices and oscillators. In an MTJ, one of the two key magnetic layers is a switched (free layer FL) between a parallel (P) and anti-parallel (AP) state with respect to the other layer with a fixed magnetization direction (pinned layer PL). Recently, it is discovered that free layer(FL) switching can be effectuated via different schemes like spin-transfer torque (STT), spin-orbit torque (SOT), and an electric field (voltage-controlled magnetization switching VCMS). These

ED Taipei, Invited Talk November 21, 2018
(Row 1 from left) Speaker (Prof. Albert Liang), Speaker (Prof. Manan Suri), seminar chair (Prof. T. H. Hou) with audience

ED Taipei, Invited DL Talk November 23, 2018
(from left) The seminar chair (Prof. Steve Chung, 6th) and speaker (Prof. Yang Chai, 7th) with the audience

effects open a new avenue for novel device operations in logic and non-volatile memory applications. This talk was attended by around 35 graduate students and professors.

The second talk, on the same day, was given by Prof. Manan Suri from IIT Delhi, and the talk was titled "Moving Towards A Memory Centric Age." First, he described the factors that contribute to the ever increasing importance of memory, i.e., saturation of Moore's law and the ease of generating enormous amounts of data. A fundamental shift in the vastly successful Von Neumann computational paradigm is needed to overcome the bottlenecks associated with data-intensive real time applications. This is where, next generation advanced Non-Volatile Memory (NVM) begins to play a very significant role. He introduced their activities on the directions of computing, storage, sense and security.

The third talk is a DL talk, given by Prof. Yang Chai, from Hong Kong Polytechnic University, on Nov. 23. His talk was titled "Two-dimensional materials: Raman Spectroscopy and Electron Device." First, he introduced how to use the Raman spectra to examine a specific edge feature in a newly observed forbidden Raman modes, which are originally undetectable from the body region. He also presented a detailed study on group-10 transition metal dichalcogenides (PtS_2, $PtSe_2$) for the channel materials of transistor, exhibiting widely tunable bandgap, high mobility and stability. This talk was attended by around 40 graduate students, professors, and several industry leaders.

The premier event on VLSI in the region as well as a leading technology conference worldwide for over 30 years, 2019 VLSI-TSA and VLSI-DAT will be held April 22–25, 2019 in Hsinchu, Taiwan, see https://expo.itri.org.tw/2019VLSITSA. Both are technically sponsored by the IEEE EDS and SSCS, and will hopefully attract more than 800 attendees each year. Further information and inquiries, please contact Miss Anny Huang, vlsitsa@itri.org.tw.

EDS Distinguished Lecture—ED Xian Chapter

—by Yuming Zhang

On November 21, 2018, Prof. Ru Huang, a Distinguished Lecturer of EDS, gave a lecture titled "Emerging Devices for Different Low Power Applications in Post-Moore Era" at Xidian University, China, under the auspices of ED Xian Chapter. The lecture started with an overview of overall development, the typical features and the technical challenges of Post-Moore era, with a focus on emerging devices for different low power applications. Multi-gate nanowire transistors with performance and power tradeoff for highly-scaled technology were then discussed. Devices with steep subthreshold swing utilizing new operation mechanisms for power-constrained applications, including tunneling devices and negative capacitance FETs (NCFETs), were highlighted. Also, a tunnel-Schottky hybrid device was presented with the best figures of merit. The physical origins of the NCFET operation were analyzed. Artificial neuron circuits and electronic synapses based on the new low power architecture for neuromorphic computing and the different realization methods were presented by comparison. Finally, Prof. Huang examined the future trends of IC technology. The lecture lasted for 90 minutes and attracted over 400 attendees, including approximately 50 professors and over 350 graduate students.

EDS Distinguished Lecture—ED Tsinghua Student Chapter

—by Yancong Qiao

The ED Tsinghua Student Chapter held one invited talk on October 26, 2018. The invited lecturer was Prof. Hei Wong from City University of Hong Kong. He gave a talk titled "More Moore, More than Moore, and Some More." It is anticipated that CMOS devices will continue to shrink, in accordance to the Moore's Law, for some more generations by additional technology and device structure innovations in the ultimate scale. Though, there should be many challenges ahead in every aspect of device structure, material engineering, as well as fabrication technology. A number of "More-than-Moore" strategies have been worked out to boost the digital intelligence systems without relying on device scaling. In this talk, Prof. Wong highlighted some of these issues with some

ED Xian, DL Talk on November 21 Left to right: Xiaohua Ma, Yuming Zhang, Ru Huang (Distinguished Lecturer), Yintang Yang, Zhangming Zhu, Genquan Han

ED Tsinghua Student Chapter invited talk on October 26th by Prof. Wong

ED Tsinghua Student Chapter invited talk on November 4th by Dr. Zhao

personal remarks on prospects in the technology development, especially on the next generation 5G mobile computing devices.

The ED Tsinghua Student Chapter held an invited talk on November 4, 2018. The lecturer was Dr. Bin Zhao, CTO and VP of Engineering, Iotelligent Semiconductor. He gave a talk titled, "Power Management Solutions Enabled by Mixed-Signal Technologies and Intelligence." Many electronic products are essential in our daily life, which include not only PCs with microprocessors and memory chips, but also: wireless/mobile communication devices, portable multimedia devices, large-scale/high-definition displays, various entertainment systems, home appliances, healthcare wearable devices, smart sensing and IoT. As increased performance and/or more diversified features are realized in these electronic products, power dissipation has emerged as a critical challenge under the consideration of energy conservation, chip/system thermal limitations, and product usage time before battery recharging. Mixed-signal IC technologies and design have been critical for communications by providing the needed data conversion between analog and digital signals. They enable the best signal processing in either digital or analog/RF domains to achieve the required performance in a cost effective way. Mixed-signal technologies and design intelligence also provide formidable solutions for efficient power management in various applications mentioned above. In this talk, Dr. Zhao reviewed and discussed the challenges in power management and the innovative solutions enabled by mixed-signal design and technologies for the advantages in performance, power efficiency and cost.

EDS Distinguished Lecture—ED Guangzhou Chapter

—by Zhangang Zhang

ED Guangzhou Chapter co-hosted the 2018 Reliability Physics Annual Meeting of China. The conference was held on October 31-November 2, 2018 at China Electronic Product Reliability and Environmental Testing Research Institute. Over 150 engineers, academics and students attended this event and enjoyed the wonderful keynote speeches and session presentations.

Professor Wenyan Yin, an IEEE Fellow, gave a distinguished lecture titled "High Reliability Demands of Electronic Devices: Simulation Design Methods of Multiple Physical Field Processes" on October 26, 2018, at IEEE ED Guangzhou Chapter. Over 30 engineers, academics and students attended this event and enjoyed the discussions with the speaker.

ED Guangzhou Chapter co-hosted the 2018 Reliability Physics Annual Meeting of China

ED Guangzhou Chapter, invited talk on October 26th by Prof. Yin

EDS Distinguished Lecture—ED Beijing Chapter

—by Kangwei Zhang

On November 6, 2018, Prof. Suman Datta from University of Notre Dame visited the Institute of Microelectronics of Chinese Academy of Sciences (IMECAS). He delivered a lecture titled "From Ferroelectrics to Ferroelectronics" hosted by the ED Beijing Chapter. Research discovery of ferroelectricity in doped hafnium dioxide thin films has ignited tremendous activity in exploration of ferroelectric FETs for a range of applications from low-power logic to embedded non-volatile memory to in-memory compute kernels. In this talk, Prof. Datta presented key milestones in the evolution of Ferroelectric Field Effect Transistors (FeFETs) and the emergence of a versatile Ferroelectronic platform. Prof. Datta began with a critical review of steep slope FeFETs for logic applications. Nonvolatile memory in logic circuits (such as non-volatile flip flops and SRAM) using FeFETs had been discussed in the context of incidental or intermittent computing targeted for extremely energy constrained applications. Next, Prof. Datta discussed the application of FeFETs as an analog multi-level weight storage and weight update unit for accelerating in-situ hardware training for deep neural networks. At last, Prof. Datta concluded with his current understanding of the physics of multi-domain switching in doped HfO_2 thin films, and its significance for various ferroelectronic applications. More than 40 local professionals and graduate students attended the meeting.

~ Ming Liu, Editor

ED Beijing distinguished lecture on November 6th by Prof. Datta

ED Malaysia Kuala Lumpur Chapter

—by Rosminazuin Ab Rahim, Norfarahidah Za'bah and Aliza Aini Md Ralib

ED Malaysia Technical Lecture Series 2018

ED Malaysia kicked off with its local technical lecture series in an effort to promote electron devices collaborative research and membership among its members. Prior to the lecture series, an EDS membership overview was given. The first lecture series was given by Dr. Susthitha titled "Kretschman based Surface Plasmon Resonance" and Dr. Ramdzan Buyong titled "Dielectrophoresis Manipulation: Versatile Mechanism of lateral, vertical and combination of both" on September 26, 2018 at MMU Cyberjaya. A total of 15 participants attended the event. The second lecture series was held on November 1, 2018 at IIUM Gombak Kuala Lumpur. The speakers were Dr. Zubaida Yusoff who gave a lecture titled "An Overview of RF Power Amplifier design for 5G Base Stations," and Dr. Ahmad Sabirin Zoolfakar with a lecture titled "Engineering and Tuning Transition Metal Oxides on Enhancing Sensing Properties" at IIUM. A total of 20 participants attended the event. The final lecture series for 2018 was held on 4th December 2018 at UPM Serdang and was attended by 15 participants. Dr. Suhaidi Shafie gave a talk on "Dye Sensitized Solar Cell" and Prof. Norhayati Soin spoke on "Physical Unclonable Function security enabled FPGA for medical solutions in IOT." These events were very well received both by students and academia and we hope to continue the lecture series for 2019.

EDS Malaysia Technical Lecture Series 2018

ED Malaysia Professional Short Courses 2018

ED Malaysia held two professional short courses in the fourth quarter of 2018. The "Photoluminescence" (PL) short course was conducted on October 10, 2018 at IMEN, Universiti

Participants of EDS Malaysia' professional short courses

Kebangsaan Malaysia (UKM) by Dr. Abdul Rahman Mohamad, a research fellow at IMEN. A total of 20 participants attended the short course and they were briefed on the theory of PL followed by hands-up usage of the PL equipment at IMEN. On November 27–28, 2018, another short course on the "Taguchi Method for Robust Product and Processes" by Professor Emeritus Prakash Apte, previously from IIT Bombay was held at IMEN, UKM. The course successfully attracted 20 participants from academia and industry. Upon completion of the lecture on theory and applications, participants presented their case study where the Taguchi method can be used. Both programs were held successfully and will be held on an annual basis.

~ P Susthitha Menon, Editor

ED Netaji Subhash Engineering College Student Chapter, Kolkata

—by Ayush Thakur and Saheli Sarkhel

The ED Netaji Subhash Engineering College Student Chapter in association with the Department of ECE, organized a one-day seminar on August 4, 2018. Prof. Ashutosh Dutta, Senior Wireless Communication Systems Research Scientist at Johns Hopkins University Applied Physics Labs (JHU/APL) presented a talk on "Security in SDF/NFV and 5G networks-Opportunities and Challenges." The lecture session commenced with a brief introduction of IEEE membership and its benefits for students and professionals. It was followed by the evolution of network technology from 1G to 4G, while exposing the loopholes which could lead to a security breach. The second part of the talk primarily focused on the new opportunities and challenges in dealing with 5G technology. Almost 45 participants including students and faculty members showed up for the event along with the 13 members of this chapter.

Team ED NSEC Student Branch Chapter with Dr. Saxena

In addition, the chapter and Department of ECE at Netaji Subhash Engineering College (NSEC), in association with ED University of Calcutta student chapter, organized a one day national seminar on "VLSI Circuits and Applications in Industry" on October 10, 2018. Mr. Avishek Bhattacharya, Technical Consultant and Hardware Specialist of Hewlett and Packard Enterprise, India and Mr. Sayantan Sharangi, Design Engineer 2, Cores-BGL, AMD India Pvt. Ltd., Bangalore, India presented their valuable lectures on the aforementioned topic. The lecture session commenced with a brief overview on the "Practices, Trends and Challenges in modern day VLSI Industry" by Mr. Sharangi, highlighting several state-of-the-art techniques being adopted by the modern VLSI industry to cope up with the challenges associated with device operations in sub nanoscale regime. This session was followed by another on the popular trends of Artificial Intelligence and Cloud Computing in industry by Mr. Bhattacharya, highlighting on the internship prospects for the budding engineers. Almost 75 participants including students and faculty members showed up for the event along with the 25 student members of this chapter. The photos taken during the seminar shows overwhelming response from the students and faculty members in presence of our speakers suggest that the seminar was a great success.

The chapter in association with the Department of ECE, NSEC organized an IEEE DL on "Recent advances in Tunnel Field Effect Transistor for sensing applications" on November 24, 2018 by Dr. Manoj Saxena, Associate Professor, Department of Electronics, Deen Dayal Upadhyaya College, University of Delhi. The lecture session commenced with a brief introduction to an IEEE membership and various benefits provided by IEEE, especially for students. It was followed by the evolution of transistors, the disadvantages of MOSFETs and a path to the creation of TFETs. The second part of the talk comprised on the working principle of TFETS and its various benefits and applications. TFETs are used in the field of biomedical research because of its extreme sensitivity to small changes in the surrounding. It helps in finding markers of various diseases or even a specific one. The talk was very informative and explained the concept of TFETs and the new ways of usage for its characteristics. Almost 40 participants including students and faculty members attended the event along with the members of the chapter. The students were

really motivated and excited to carry out their own projects and research. The photos taken during the seminar shows the overwhelming response from the students in presence of our speaker and suggests a great success of the seminar.

ED Calcutta Chapter

—by Angsuman Sarkar and Manash Chanda

Lecture at the ED Calcutta Chapter

A one-day IEEE EDS outreach program was successfully organized by the chapter in association with the ECE Department, RCCIIT on July 10, 2018. Participants were acquainted to various device scaling phenomena and Ultra Low Power design approach for their prediction. It helped the participants to get some ideas of this branch of Electronic Devices and also it indicated some new research dimensions for the research scholars. Prof. Subir Kumar Sarkar, IEEE EDS DL lucidly illustrated the requirement of device scaling and its impact on MOSFET Device Scaling. In his lecture, he discussed the historical aspects of device scaling to the present day scenario. Dr. Manash Chanda clarified the Ultra Low power design approach and elaborated on Sub-threshold Adiabatic Logic. The IEEE EDS Membership was explained by Dr. Angsuman Sarkar and caused immense interest among the participants. Overall, the program was productive and it provided some new ideas as well as research challenges to the participants.

Another one day IEEE EDS DL was organized by the Chapter in association with the Department of Electronics & Communication Engineering of Guru Nanak Institute of Technology, on September 4, 2018. Prof. Chandan Kumar Sarkar, IEEE EDS DL delivered a talk on III-V Device Materials and applications. Student members, along with the faculty members and research scholars benefitted, as they were inspired by new ideas to pursue in their research. Dr. Angsuman Sarkar discussed the benefits of the IEEE Membership and Dr. Manash Chanda discussed the device and Circuit Co-design approach for ultra low power system. On the whole, the response from the participants was enthusiastic and it can be concluded that this endeavor of the organizing committee was successful.

IEEE ED Kolkata Chapter organized the Electron Device Kolkata Conference (IEEE EDKCON) 2018 during November 24–25, 2018 at Pride Plaza, Kolkata. IEEE EDKCON 2018 had called for the submission of papers in multiple topics, ranging from Device Modeling and Simulations to Process and Manufacturing Technology, from FPGA and Real time Embedded Systems to Biodegradable and Flexible Electronic Devices. There was an overwhelming response by authors from both academia and industry. A total of 129 out of 338 submissions were included in the technical program committee. The conference had three plenary talks and four keynote talks, and had participation of fifteen EDS DLs and seven IEEE Fellow Members.

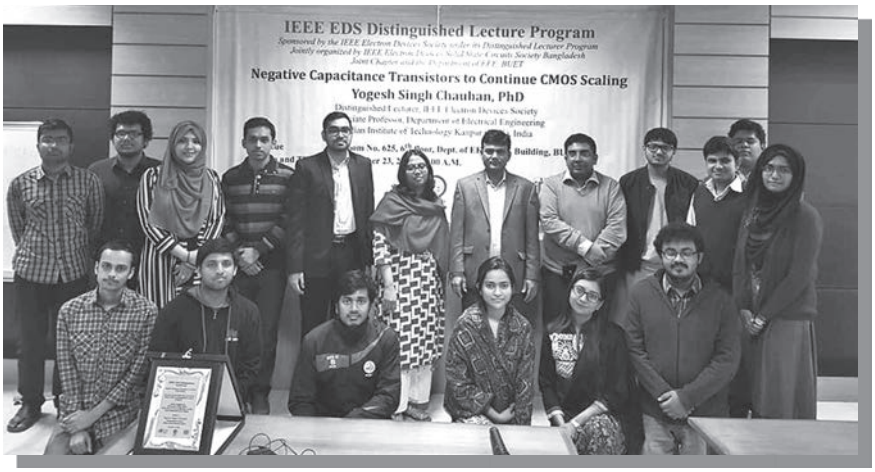
The chapter also arranged an outreach program on December 17, 2018 at Acharya Prafulla Chandra College, Sajirhat, New Barrackpore aimed at developing the professional identity in IEEE's designated fields of interest in technology and engineering among the students and faculty members. In addition, membership benefits were discussed. Prof. Sanatan Chaterjee, IRPEL, Calcutta University; Dr. Angsuman Sarkar, Chairman, IEEE ED Kolkata Chapter and Dr. Atanu Kundu, Ex Chair, IEEE ED Kolkata Chapter delivered technical talks in this outreach program. Almost 80 members participated in the program. Out of 80, almost 15 IEEE Members and 10 IEEE Student members participated in the program.

ED/SSCS Bangladesh Chapter

—by Mahnaz Islam

The ED/SSCS Bangladesh Chapter and the Department of EEE, BUET jointly organized a talk on "Innovation in low-carbon vehicle technologies-vehicle to grid (V2G) systems and integrated powertrain solutions" on April 1, 2018. The talk was given by Dr. Rishad Ahmed, Design Engineer, Dynex Semiconductor, UK. A total of 31 participants, with 10 IEEE members, attended the talk. Dr. Ahmed discussed three specific technologies being developed by Dynex to tackle the current automotive power electronics challenges i.e. double-sided cooling of IGBT and Si-SiC hybrid modules, integrated inverter-machine for the EV powertrain and integrated inverter-converter system for the EV traction drive and low-voltage power supply.

The chapter, IEEE ComSoc Bangladesh Chapter and the Department of EEE, BUET jointly organized a talk on "Smart heterostructure design to overcome the efficiency bottleneck of deep UV photonics" on April 04, 2018 at the Department of EEE, BUET. The talk was given by Dr. SM (Moudud) Islam, Post-Doctoral Research Associate, Cornell University, where in he discussed the choice of semiconductor material substrate for deep-UV photonic devices and challenges associated with electrical efficiency of the photonic devices in the shorter wavelength DUV regime. A total of 33 participants with 23 IEEE members attended the talk.



Attendees of Distinguished Lecture by Professor Yogesh Singh Chauhan, IIT Kanpur

IEEE ED/SSCS Bangladesh Chapter, IEEE EDS BUET Student Branch Chapter and Department of EEE, BUET jointly organized a talk on "A Road to Professional Development" on July 4, 2018 at the Department of EEE, BUET. The talk was given by Professor Dr. Hasina F Huq, Associate Professor, University of Texas Rio Grande Valley (UTRGV). She addressed challenges and advances in gallium-nitride based biosensor research and potential of the graduate programs in the USA. Total of 22 participants with 12 IEEE members attended the talk.

IEEE ED/SSCS Bangladesh Chapter and Department of EEE, BUET jointly organized an "Interactive Panel Discussion on Career and Opportunity in VLSI Industries by Ulkasemi Private Limited" on December 12, 2018 at the Department of EEE, BUET. A total of 90 participants with 26 IEEE members attended the discussion. Panel Members comprising of Md Enayetur Rahman, CEO and Co-Founder, Ulkasemi Ltd; Fazlul Karim, Project Manager, Ulkasemi Ltd; Farshad Ibne Fazle, Member of Technical Staff, Ulkasemi Ltd.; Shafaitul Islam Surush, Senior Engineer (IC Physical Design), Ulkasemi Ltd. And Shajib Barua, Senior Engineer (Circuit and System design), Ulkasemi Ltd. offered interactive setting for the students and faculty to interact with the Ulkasemi team regarding innovation and development in the field of VLSI to conceive and scale projects of both technological excellence and financial viability.

IEEE ED/SSCS Bangladesh Chapter and IEEE EDS BUET Student Chapter jointly organized the "Membership Drive 2018" on October 30, 2018 at the Department of EEE, BUET. A total of 40 participants attended the discussion. Mahnaz Islam—Secretary of IEEE ED/SSCS Bangladesh Chapter, Yeasir Arafat—Membership Development Coordinator, IEEE ED/SSCS Bangladesh Chapter and Chair and Vice-chair of IEEE EDS BUET Student Chapter discussed the organization's work and the benefits of becoming a member.

On December 23, 2018, the chapter and Department of EEE, BUET jointly organized a Distinguished Lecture by Professor Yogesh Singh Chauhan, IIT Kanpur, India on the topic "Negative Capacitance Transistors to Continue CMOS Scaling." He discussed the physics and modelling of various NCFET structures and impact of this new transistor on circuits including processors. A total of 20 participants with 16 IEEE members attended the Distinguished Lecture.

AP/ED Bombay Chapter

—by Anil Kottantharayil

The IEEE AP/ED Bombay Chapter during the last quarter organized talks by Dr. Veerabhadrarao Kaliginedi, Institute of Materials, EPFL, Lausanne, Switzerland and Prof. Karthik Shankar, University of Alberta, Edmonton, Canada. The talks were attended by students, research staff and faculty of IIT Bombay, and students and faculty members from educational institutions in and around Mumbai. Dr. Kaliginedi, in his talk titled "Charge transport at Electrode|Molecule interface: From Molecular Electronics to energy research applications," presented the working principles of molecular measurement techniques, i.e., STM break junctions (STM-BJ), mechanically controllable break junction (MCBJ), conducting probe AFM (CP-AFM)

Dr. Veerabhadrarao Kaliginedi delivering his talk

techniques and data analysis procedures used to extract conductance properties of molecular junctions and also discussed the molecular conductance measurement results obtained from several case studies that have direct impact on electrocatalysis and energy research.

In his talk titled "TiO_2 nanotube and nanorod arrays: Playgrounds to study unusual heterojunctions, hot electron phenomena and nanophotonic effects," Prof. Karthik Shankar discussed n-type semiconducting TiO_2 nanotube and nanorod arrays synthesized by the simple bottom-up nanofabrication processes of electrochemical anodization and solvothermal growth respectively. Both the talks received a good response.

Mr. Deepak Maheshwari along with Dr. P. Hemalatha Reddy and workshop organizers

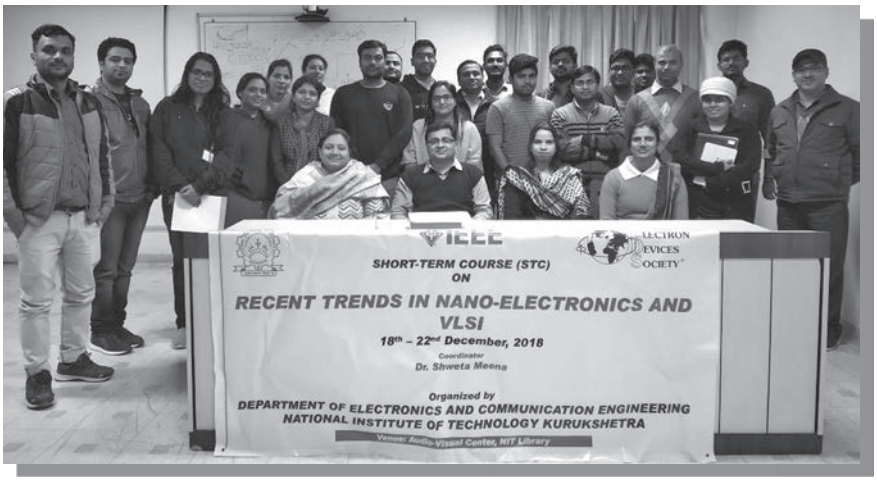
ED Delhi Chapter

—by R. S. Gupta and Sneha Kabra

On August 20, 2018, Mr. Jeff Yeh, Director, Customer Engineering Division, and Mr. Chuck Huang, Associate Vice President, Technical Marketing Division, WIN Semiconductors Corp, Taiwan conducted technical session on "Present technologies offered by WIN Semiconductors in GaAs and GaN," which was jointly organized in association with Department of Electronic Science, UDSC and Solid State Physics Laboratory, Delhi. Discussions were held on present technologies offered by WIN in GaAs as well as GaN. Various other services like packaging and dedicated RF characterization of high frequency devices offered by WIN were also explained. The technology nodes available with WIN in GaAS and GaN were discussed along with measured data of different technology nodes.

Professor R. S. Gupta, ED Delhi Chapter-Chair and Dr. Rishu Chaujar along with participants of the Faculty development program

A Two-day workshop on "Internet of Things (IoT) for creating smart homes and cities" was organized by Sri Venkateswara College, University of Delhi, in collaboration with the IEEE-ED Delhi Chapter during September 14–15, 2018. The speakers were Mr. Deepak Maheshwari, Director-Government Affairs, India, ASEAN & China, Symantec Corporation, and Mr. Amritansh Ranjan, Embedded Engineer, i3indya Technologies, New Delhi, India. The event was Co-sponsored under the DBT Star College Scheme. The workshop started with an invited lecture from Mr. Deepak Maheshwari on "Internet of Things (IOT) Security and Privacy." The lecture gave an insight into the security concerns and risks involved in implementation of IOT ecosystem, challenges regarding the security of data and data protection framework. The prospect of artificial intelligence as the new frontier for security and privacy was also discussed briefly along with IOT policy. The lecture was followed by a hands-on workshop by resource person from i3indya technologies. The participants were given a brief introduction about IOT, its future and the role of technology in developing smart systems. Then, hands-on practice was carried out on ATmega 8 microcontrollers, in which various projects were designed.



Atttendes of short-term course held December 18–22, 2018 at NIT Kurukshetra

The chapter and Delhi Technological University, Delhi jointly organized a Faculty Development program on "Recent Trends in Material Science and Engineering" from September 17–21, 2018 at Delhi Technological University. The main objectives of the program were to upgrade the knowledge, skills and training for science and engineering faculty. Distinguished scientists and faculty were invited to give lectures on emerging areas in the field of technology. Several areas in the field of material science, nanotechnology, quantum photonics, magnetoelectric measurements and device applications were covered to give the insight in the present state-of-the-art of these topics.

The Department of Instrumentation of Shaheed Rajguru College of Applied Sciences for Women (SRCASW), University of Delhi in collaboration with the chapter organized a talk on "Recent Trends in VLSI Technology: A brief Introduction to Layout Designing" by Mr. Neeraj Kapoor, Layout Design Engineer from Synopsys India Pvt. Ltd. on October 12, 2018 at SRCASW. The talk was conducted in a series of "TECHNEXUS" (an annual technical festival of the Instrumentation Department). He explained the fabrication steps involved in making a semiconductor chip along with the steps involved in its designing and different design steps, including logic development, verification and its implementation. He also touched upon FinFET technology to introduce students about the state of the art of the current VLSI industry. Around a hundred participants, including students, research scholars and faculty members attended the talk.

A one-week short-term course was held from December 18–22, 2018 at NIT Kurukshetra in collaboration with IEEE ED Delhi Chapter. The purpose of this course was to acquaint the participants of recent technologies in nanoelectronics and VLSI. There were 32 participants from various premier Institutions like IIT Madras, NIT Trichy, NIT Surathkal, Thapar Engineering College Patiala, DTU, etc. who attended the course. Prof. Vijay Arora, (Wilkes University, USA) gave lectures during the first three days on Nano CMOS, transport in nanowires, transport in 1D and 2D materials. Dr. Manoj Saxena (Deen Dayal Upadhyaya College, University of Delhi, Delhi) delivered four lectures on MOSFET, FINFET, TFET and HEMT. The Front-End circuit design and Back End Flow & layout Design were discussed by Mr. H S Jatana (SCL, Dept. of Space, ISRO, Mohali). Dr. Atul Nishad (NIT Warangal) delivered a lecture on VLSI interconnects and GNR FETs. The final session was by Mr. Harender Kumar (Integrated Microsystem) on hands on training on Synopsis QuantumWise ATK tool. The course ended with celebratory function on December 22, 2018.

ED NIST (National Institute of Science & Technology) Student Chapter, Berhampur, Orissa

—by Ajit K. Panda

The IEEE ED NIST student chapter organized a technical lecture on December 19, 2018 at the National Institute of Science and Technology, Berhampur, Odisha on "Research Trends in Biomedical Engineering." Forty-eight faculty members attended the lecture from different streams

Dr. Satya Sopan Mahato (left) is presenting a memento to Dr. Rutuparna Panda

August 9, 2018 at NIST, Berhampur, Odisha on "Recent Advances on Digital Signal Processing"

to enhance their research activities. Prof. R. P. Panda from VSSUT-Burla discussed different engineering applications in the biomedical area. Prof. Panda summarized the wide research areas and important research publications for current industry problems and solutions to overcome these problems.

IEEE ED NIST Student Chapter organized a half-Day workshop on August 9, 2018 at NIST, Berhampur, Odisha on "Recent Advances on Digital Signal Processing." The lecture was delivered by Prof. G Panda of IIT, Bhubaneswar. Faculty members attended from different nearby institutes and universities. Prof. Panda discussed real time problems and a holistic approach to finding solutions for them. He talked about adoptive signal processing and how to make the system intelligent and smart by introducing algorithms effectively.

ED Heritage Institute of Technology Student Chapter

—by Mousiki Kar

The chapter and IEEE EDS Centre of Excellence organized a technical lecture by Professor Vincenzo Piuri (IEEE Fellow and Professor of Computer Engineering at the Università degli Studi di Milano) on September 24, 2018. He spoke on the topic "Ambient intelligence: convergence of artificial intelligence, machine learning, biometrics, cloud-computing, and internet-of-things." The talk was attended by around 370 participants.

In addition, a talk titled "Microelectronics Technology" was delivered by Prof. S.N. Biswas, former Professor IIEST and HITK on November 21, 2018 which was attended by 285 participants.

ED Institute of Engineering & Management Student Branch Chapter

—by Soumyarup Roy

The IEEE ED Institute of Engineering and Management Student Chapter organised it's 3 technical symposium on November 3, 2018. The symposium was held in the seminar hall of the Institute of Engineering and Management. There were about 40 students present in the auditorium attending the lecture. The topic of the lecture was "Introduction To TFET, Working Principle and Applications" delivered by Prof. Manash Chanda.

Snapshots of the Lecture Session by Prof. Vincenzo Piuri

Talk delivered by Prof. S.N. Biswas

IEM IEEE ED student members with Prof Dr.Manash Chandra (centre left) and Prof Dr.Angsuman Sarkar (centre right)

ED Indian Institute of Technology—Roorkee Student Branch Chapter
—by Sourabh Jindal

The chapter organized a technical talk by Mr. Neeraj Paliwal, semiconductors engineering leader based in Silicon Valley on "Future of Computing: Domain Specific Architectures Build for Security and Energy Efficiency" on November 16, 2018. The event was successfully held in the Department of ECE, IIT Roorkee. Around 45 participants including faculty, research scholars and graduate students from IIT Roorkee attended this talk. This talk provided an overview of the latest challenges and opportunities for building a "Secure and Energy Efficient Domain-Specific Computing Systems." Further he talked about tremendous progress in computing performance (approx. one million times) during the last forty years, primarily driven by IC technology innovation. He also discussed the top application domain AI, or more specifically defined as "deep learning" computing workloads.

IEEE ED IIT Roorkee student chapter organized a technical talk by Dr. Dipendra Singh Rawal, who is Scientist-G in the Solid State Physics Laboratory (DRDO), Delhi on "AlGaN/GaN/SiC HEMT Device Technology for MMIC Applications" on December 10, 2018. Around 40 participants attended this talk. He discussed AlGaN/GaN HEMT device technology developed on 75 mm SiC substrate to deliver enhanced RF power output up to C-band applications with reliable and reproducible performance. Further, he talked about the process improvements and technical results achieved on in-house fabricated depletion mode GaN HEMT devices.

On December 12, 2018, a technical talk on "Towards Energy Efficient Nano-Electronics with Steep Slope Transistors" was delivered by Professor Qing Tai Zhao, Senior Research Scientist, PGI 9, Research Center, Jeuelich (Forschungszentrum Juelich, Germany). He discussed his research on Silicon based TFETs and gate all around Silicon nanowire complementary TFETs. Further, he discussed NC FETs with doped HfO_2 as a ferroelectric layer. Around 35 participants attended this lecture.

On December 14, 2018, a DL was delivered by Prof. Ramachandra Achar, Department of Electronics, Carleton University, Ottawa, Ontario on "Signal Integrity and High-Speed Interconnects." He discussed the rising demands for faster computing and communication, and the effects associated with the interconnects limiting the performance of high-speed designs. The talk covered the signal integrity modelling and analysis for design and validation of modern VLSI designs. About 40 students attended the lecture.

~ Manoj Saxena, Editor

Qing Tai Zhao and attendees at the IEEE technical talk, December 12, 2018 at IIT Roorkee

Prof. Ramachandra Achar and attendees at the IEEE DL' December 14, 2018 at IIT Roorkee

EDS MEETINGS CALENDAR

THE COMPLETE EDS CALENDAR CAN BE FOUND AT OUR WEB SITE: HTTP://EDS.IEEE.ORG. PLEASE VISIT.

2019 30th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC)	06 May - 09 May 2019	Saratoga Springs, NY USA
2019 IEEE 11th International Memory Workshop (IMW)	12 May - 15 May 2019	Monterey, California, USA
2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)	19 May – 23 May 2019	Shanghai, China
2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)	02 Jun – 04 Jun 2019	Boston, MA USA
2019 International Interconnect Technology Conference (IITC)	02 Jun – 06 Jun 2019	Brussels, Belgium
2019 Silicon Nanoelectronics Workshop (SNW)	09 Jun – 10 Jun 2019	Kyoto, Japan
2019 Symposium on VLSI Technology	09 Jun – 14 Jun 2019	Kyoto, Japan
2019 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)	12 Jun – 14 Jun 2019	Xi'an, China
2019 IEEE 46th Photovoltaic Specialists Conference (PVSC)	16 Jun - 21 Jun 2019	Chicago, Illinois

2019 Device Research Conference (DRC)	23 Jun – 26 Jun 2019	Ann Arbor, MI
2019 20th International Conference on Solid-State Sensors, Actuators and Microsystems & Eurosensors XXXIII (TRANSDUCERS & EUROSENSORS XXXIII)	23 Jun - 27 Jun 2019	Berlin, Germany
2019 IEEE 26th International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)	02 Jul – 05 Jul 2019	Zhejiang, China
2019 26th International Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD)	02 Jul - 05 Jul 2019	Kyoto, Japan
2019 IEEE International Flexible Electronics Technology Conference (IFETC)	11 Aug – 14 Aug 2019	Vancouver, BC Canada
2019 34th Symposium on Microelectronics Technology and Devices (SBMicro)	26 Aug – 30 Aug 2019	Sao Paulo, Brazil
2019 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)	04 Sept – 06 Sept 2019	UDINE, Italy
2019 IEEE 31st International Conference on Microelectronics (MIEL)	16 Sept – 18 Sept 2019	Nis, Serbia
ESSDERC 2019 - 49th European Solid-State Device Research Conference (ESSDERC)	23 Sept – 26 Sept 2019	Cracow, Poland
2019 8th International Symposium on Next Generation Electronics (ISNE)	09 Oct – 11 Oct 2019	Zhengzhou, China

2019 International Semiconductor Conference (CAS)	09 Oct – 11 Oct 2019	Sinaia, Romania
2019 IEEE International Integrated Reliability Workshop (IIRW)	13 Oct – 17 Oct 2019	South Lake Tahoe, CA
2019 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)	14 Oct – 17 Oct 2019	TBD, CA, USA
2019 IEEE BiCMOS and Compound semiconductor Integrated Circuits and Technology Symposium (BCICTS)	03 Nov – 06 Nov 2019	Nashville, TN USA
2019 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)	04 Nov – 07 Nov 2019	Westminster, CO
2019 IEEE International Electron Devices Meeting (IEDM)	09 Dec – 11 Dec 2019	San Francisco, CA
2019 IEEE 50th Semiconductor Interface Specialists Conference (SISC)	11 Dec – 14 Dec 2019	San Diego, CA
2020 33rd IEEE International Conference on Microelectronic Test Structures (ICMTS)	06 Apr – 09 Apr 2020	Edinburgh, Scotland, UK

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EDS Vision, Mission and Field of Interest Statements

Vision Statement
Promoting excellence in the field of electron devices for the benefit of humanity.

Mission Statement
To foster professional growth of its members by satisfying their needs for easy access to and exchange of technical information, publishing, education, and technical recognition and enhancing public visibility in the field of Electron Devices.

EDS Field of Interest
The EDS field-of-interest includes all electron and ion based devices, in their classical or quantum states, using environments and materials in their lowest to highest conducting phase, in simple or engineered assembly, interacting with and delivering photo-electronic, electro-magnetic, electromechanical, electro-thermal, and bio-electronic signals. The Society sponsors and reports on education, research, development and manufacturing aspects and is involved in science, theory, engineering, experimentation, simulation, modeling, design, fabrication, interconnection, reliability of such devices and their applications.