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TECHNICAL BRIEFS

DEVELOPING EUV LITHOGRAPHY FOR HIGH-VOLUME MANUFACTURING—A PERSONAL JOURNEY

ANTHONY YEN

Among the papers presented by TSMC at the annual IEEE International Electron Devices Meeting (IEDM) held in San Francisco in December 2019, one reported that “we started the volume ramp of the enhanced 7 nm technology with EUV insertion in 2019,” and another one announced that the “true 5 nm platform technology is on schedule for high volume production in 1 H 2020... more than ten EUV layers are employed to replace at least 4 times more immersion layers at cut, contact, via and metal line masking steps for process simplification, faster cycle time and better reliability & yields.” Presentation of these two papers signified the entry of the world’s semiconductor manufacturing into the EUV era. At the December 2020 IEDM, TSMC further states in a paper that its “5 nm node presents ~30% minimum metal pitch scaling through the finest of EUV approaches coupled with innovative barrier/liner, ESL/ELK, and Cu reflow engineering.” A clear example of EUV lithography in

The first to commercial 5 nm - TSMC



Apple's latest iPhone features a new processor using TSMC's 5nm process
The A14 die size is ~88 mm²
~10% smaller than the A13
Transistor count is up from 8.5B to 11.8B

Apple's A14 processor, from TechInsights' presentation at SEMI Industry Strategy Symposium 2021.

(continued on page 3)

YOUR COMMENTS SOLICITED

Your comments are most welcome. Please write directly to the Editor-in-Chief of the Newsletter at
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NEWSLETTER DEADLINES

ISSUE	DUE DATE
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April	January 1st
July	April 1st

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DEVELOPING EUV LITHOGRAPHY FOR HIGH-VOLUME MANUFACTURING—A PERSONAL JOURNEY

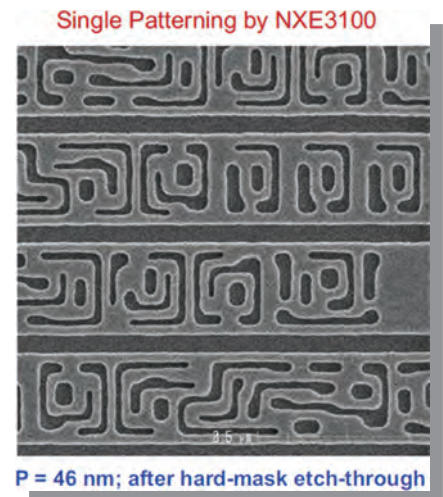
(continued from page 1)

high-volume manufacturing (HVM) is the application processor inside every Apple iPhone 12 in the world, fabricated using TSMC's EUV-enabled 5 nm process.

Secure the Future of Moore's Law

Developing EUV lithography for HVM at TSMC started in 2007. Prior to this, EUV had already had a 20+ year history, mostly in research labs in the US, Japan, and Europe, including those at ASML and Cymer—a specialist in lithographic light sources later acquired by ASML, my current employer. Laboratory research demonstrated its superior resolution and concluded that the technology had no showstoppers; it also finalized on the use of 13.5 nm-wavelength extreme-ultraviolet (hence the name EUV) radiation from laser-produced plasma (LPP) of tin as the light source and vacuum-deposited molybdenum-silicon bilayers as the reflective coating for the mirrors making up the imaging optics. While 193 nm immersion lithography, whose development in 2007 was nearly complete, would provide near-term extension of optical lithography, a new lithography technology with much better resolution would be needed in the long term to secure the future of Moore's Law. With the use of 4x-reduction projection imaging employing the 6-inch square photomask, EUV lithography, though using entirely reflective rather than mainly refractive optics, could be considered an extension of optical lithography and was thus most attractive among the several next-generation lithography technologies being pursued at that time. In fact, ASML by then had decided on EUV as the next-generation technology it would offer to its customers.

The responsibility of developing EUV lithography for HVM at TSMC fell on my shoulders. To identify all the bottlenecks, experiments had to be carried out on the then available EUV exposure tools, called scanners. There were two in the world. Marking the end of the 20+ year research phase of EUV, ASML shipped in 2006 two prototype EUV scanners, called alpha demo tools (ADT), one to a consortium in Albany, New York and the other one to imec in Belgium. Since TSMC was a core partner of imec, I dispatched a researcher there for a long-stay. The imec ADT had a very low throughput and was very often down. However, we saw encouraging images on the few exposed wafers. Under the leadership of then head of R&D (later co-COO of TSMC) Shang-yi Chiang, we ordered a development tool from ASML, model NXE3100, the successor of the ADT. Because the LPP light source was put to use for the first time, its reliability was poor and the source power never went above 10 watts, less than 1/25 of the output power of the current EUV exposure tools. But I was convinced that this would not be the killer roadblock to the project, for the next-generation light source under development in Cymer's laboratory had already demonstrated an output power several times higher than 10 watts, though only in bursts. The most important thing to scrutinize at that time was the quality of the imaging optics, made by ASML's partner ZEISS. Although both ADT and NXE3100 had a numerical aperture (NA) of 0.25, the quality of NXE3100's optics was much improved over that of the ADT, for we could already obtain from it lithographic patterns (see SEM photo below; P stands for the minimum pitch) intended for the 10 nm generation! Besides, the next-generation exposure tool from



ASML, the NXE3300, would have an imaging optics with 0.33 NA, meaning even better resolution! Encouraged, and again with Shang-yi's support, we marched on and ordered the NXE3300 which would arrive at TSMC in 2013. Towards the end of 2012, I was asked by Chairman Morris Chang on the success rate of EUV lithography. I replied "80%." He said "You are optimistic! So-and-so told me only 50%!" I was indeed being optimistic; but I had my reasons.

We Are All In

ASML knew from the beginning that EUV development was a high-risk and high-reward undertaking, to the degree that its competitors never planned to develop this technology for HVM. The president of one ASML competitor said to me, "EUV will not work and ASML will have lost all its development money." It was quite normal to hold this view at that time. But I knew that ASML had the best chance to succeed. First, ASML went all in, investing the substantial resources the project demanded. Second, CTO Martin van den Brink was on top of this technology to the minutest detail. Third, co-development with future users of this technology



Author on the way to the cleanroom

like TSMC both spread risk and increased resources and drive. For its part, TSMC also directed its resources to maximize its chance of success. Our EUV effort was guided by Shang-yi, with full support from the chairman. As for me, I put my whole heart into developing the technology. Every day I donned my bunny suit and went into the clean room to spend time with my scanners. I was told that I was the only director-level person at TSMC who entered the clean room every day, not sure whether such a remark was meant as a compliment. But I knew that I could not give orders from my office or meeting rooms; I had to see the machine in order to assess whether to stop it for a new experiment or let it continue to run so that more wafers could be exposed on that day, based on its prevalent condition. To speed up development, we carried out joint development with ASML: many experiments were carried out on TSMC's NXE3300, after initial trials in the Netherlands or the US.

On the road to EUV HVM, the biggest fear in people's mind was the inability to eventually attain the 250 watt output power from the light source, which was required for a reasonable throughput of these expensive scanners. TSMC's first NXE3300 had its first light at the end of October 2013. I mentioned above that the most important aspect was the resolution of the imaging optics; this was no longer an issue by then. And we turned our focus to the source power. For some time, we struggled with no more than 10 watts. But continued ex-

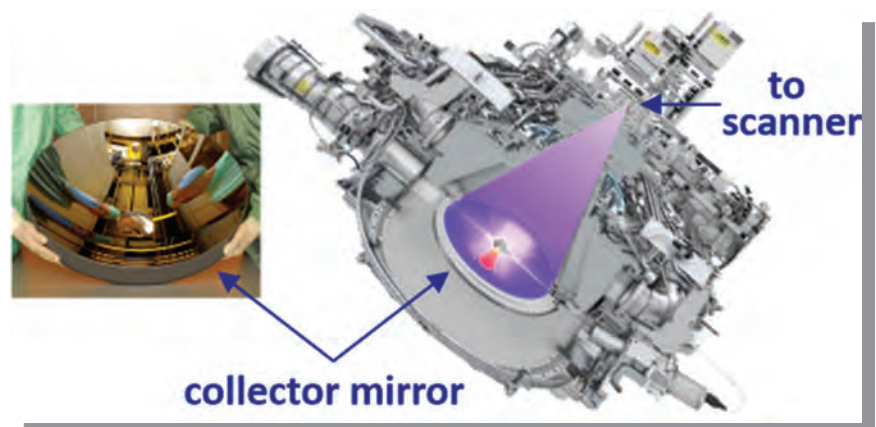
periments led us to 40 watts by the spring of 2014. Further experimentation could not lead to higher power: power could be made higher but stability suffered. For the entire summer of 2014, we carried out experiment after experiment in Hsinchu, the Netherlands, and the US.

EUV light is generated by LPP in the source vessel, at one focus of the 0.65m-diameter ellipsoidal collector mirror—the most important component in the vessel. Light is then directed to the mirror's other focus where a very small opening lets it into the scanner proper. To maintain the EUV output power, the mirror has to be kept clean from tin debris and vapor that is generated by the laser zapping of molten tin droplets, 50,000 times per second, which can quickly contaminate the mirror's surface and reduce its reflectivity. The billion-dollar game was to find the optimal operating condition to minimize tin contamination of the collector mirror at the highest possible stable output power. The interplay of the laser power, gas pressure, gas flow and hardware configuration around the mirror determined how high the stable EUV output power you could have for the scanner. Here is the chemistry behind it: atomic hydrogen is produced by EUV irradiating the molecular hydrogen gas introduced into the space around the collector mirror; the reactive atomic hydrogen then removes the tin deposited on the mirror's surface by forming with it the

gaseous tin hydride that is pumped out of the vessel. So the idea is to use EUV generated by tin to clean up the mess left by tin!

The watershed moment came on an evening in October 2014, I went into the clean room after a quick meal in TSMC's cafeteria to meet up with my people and an ASML team led by Bruno La Fontaine for a joint experiment, using the latest set of parameters coming from Cymer in San Diego. With real-time fine adjustments, the digital readout of the power meter continued to climb, steadily. By 9 pm, we reached 90 watts of output power. I immediately realized: EUV HVM would be a success. Why? From 90 watts to 250 watts, the multiplication factor was less than 3, while we had managed to climb from 10 watts to 90 watts, a multiplication factor of 9! Walking out of the clean room towards the gowning area, I sighed and felt euphoric. I will not forget this event for the rest of my life.

I asked for more resources to continue my development of EUV lithography. The senior VP replied, "500 wafers a day! I want to see 500 wafers per day from your machine for a month before giving you more resources!" Though emotional, this was a fair request, as the 90 watt power output had to translate to a sustainable tool throughput. I was wowed with Frits van Hout who at the time led ASML's EUV business unit. We decided to tackle the main



A setup for generation of EUV beam

roadblock: frequent scheduled machine downs in order to replace emptied tin droplet generator and fogged (with tin) collector mirror and the ensuing alignment of their replacements; to get to 500 wafer exposures per day, we had to minimize the frequencies of these replacements. We formed the so-called One Team of ASML and TSMC engineers, worked day and night, and finally succeeded in implementing a new tin droplet generator along with a new algorithm for the laser bombardment, halving the volume of every tin droplet that shot out while not losing the EUV energy it generated. With only 50% of tin consumption in every bombardment, the new droplet generator solved the problems of too-frequent droplet generator replacement and aggravated mirror contamination at the same time, and achieved 500 wafer exposures per day on average for a consecutive 4-week period in the second quarter of 2015.

Thereafter, One Team made continual improvements on many fronts, including further extension of the collector mirror's lifetime by carrying out many rounds of experiments with improved operating parameters. I want to thank the many ASML colleagues with whom I worked closely throughout my years at TSMC as the leader of EUV development.

A New Infrastructure

EUV lithography has so far been semiconductor industry's biggest technology development program. To ensure its success, TSMC, Intel, and Samsung together gave ASML over €1 B of R&D money in ensuing five years starting 2013. For itself, ASML acquired Cymer in 2012 for \$2.5 B, and paid €1 B to acquire 25% of ZEISS SMT in 2016 and promised to provide it with €760 M of R&D money in the next six years. All this was to ensure the success of EUV lithography.

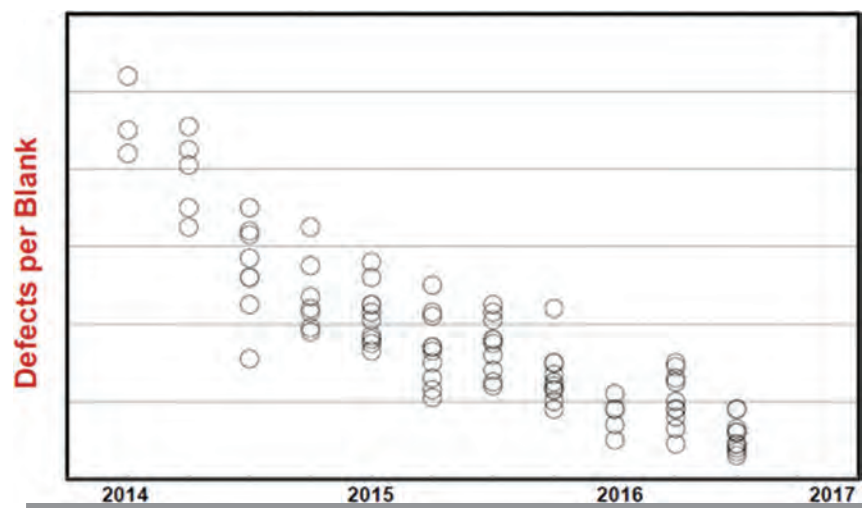
But EUV lithography is more than just the scanner, it also requires a dedicated infrastructure including, among other components, photore-

sist and photomask. In fact, photo-mask itself is a sub-ecosystem. By then, resists for 193 nm lithography based on the mechanism of chemical amplification were quite mature and the same technology could be extended to formulate EUV resists. However, resist suppliers soon realized that EUV HVM could not happen in the next couple of years and became hesitant to direct resources to the development of EUV resists, except JSR, supported by its visionary president Nobu Koshiba. With JSR, we carried out a long-term collaboration that ensured the supply of quality EUV resists to my scanners for years, for which I am very grateful.

Developing masks for EUV lithography at TSMC was also my responsibility. For the multilayer reflective mask blanks, we worked closely with Hoya, whose blanks had many defects in the beginning. Nonetheless, Junichi Horikawa, director of Hoya's mask blanks business, asked us to purchase a fixed number of blanks per month in order to maintain his mini-production line of EUV blanks. We agreed to his request, for otherwise we would only get mask blanks produced in a laboratory environment! In order to identify and locate these defects accurately, we worked with KLA's engineers to adapt one of its 193 nm mask inspection tools to

the exclusive inspection of defects in mask blanks. Once this tool became available, we were able to give constant feedback to Hoya's engineers every time we received a new batch of blanks so that processing parameters could be adjusted and improvements made on the next batch. We also worked closely with Gudeng to develop the dual-pod, the special storage case for EUV masks to keep them clean, and with Holon to adapt its mask SEM for elemental identification of mask fall-on defects. In 2011, TSMC became members of SEMATECH (for the second time) in the US and EIDEC in Japan which were dedicated to the development of the EUV infrastructure. EUV aerial-image measurement (AIMS) tool and actinic mask blank inspection tool were specific pieces of equipment whose development was supported by funds from the member companies of these consortia.

Developing EUV for HVM consists of developing the scanner, the infrastructure, and the lithography processing technology. Although this article tries to recount my personal journey with EUV, credits should go to all hard-working members of my former team at TSMC, tenacious colleagues at ASML, ZEISS, and Cymer, R&D colleagues at other semiconductor companies, relevant consortia



Native defects in EUV mask blanks were driven down over time

and research institutes, imec, all the suppliers in this ecosystem, and the supportive top management in these organizations. This was a grand joint effort. But to make the EUV technology successful, this was our one and only choice. At the 2015 SPIE Advanced Lithography symposium, a question came from the audience, "What's your plan B?" "There is no plan B!" I replied, for I already had confidence that our plan A would succeed.

EUV Saves Moore's Law

With 20+ years of research and 12+ years of intensive development, EUV lithography finally succeeded in its adoption in HVM. Moore's Law

was saved. Otherwise, the roadmap of logic semiconductor technology would have ended at the HVM of the 7 nm generation, in 2018. Instead, we are seeing the HVM of the 6 nm and 5 nm technology generations, and CC Wei, the present CEO of TSMC, announced in Q3 of 2020 that the 3 nm generation would be in HVM in the second half of 2022.

Just as 193 nm immersion lithography extended Moore's Law by ten years (five generations of integrated circuit technology), EUV lithography, with the next-generation 0.55 NA scanner already under development, is set to extend it by at least another ten years. By then, the world's semiconductor industry will be churning

out chips beyond the 1 nanometer technology generation.



Anthony Yen is Vice President and Head of Technology Development Center at ASML. He was with TSMC and led its development of EUV lithography for HVM prior to joining ASML. He did his undergraduate studies in electrical engineering at Purdue University and his graduate studies at MIT, earning his master's, engineer's, doctoral, and MBA degrees there. He is a fellow of the IEEE and SPIE.

A REVIEW OF THE 2020 ESSDERC— ESSCIRC CONFERENCE ANNUAL EUROPEAN FORUM FOR THE PRESENTATION AND DISCUSSION OF RECENT ADVANCES IN SOLID-STATE DEVICES AND CIRCUITS

THOMAS ERNST (CEA-LETI, GENERAL CHAIR)

FRANÇOIS ANDRIEU (CEA-LETI, ESSDERC TPC CHAIR)

ANDREA CATHELIN (STMicroelectronics, ESSCIRC TPC CHAIR)

The aim of **ESSCIRC** and **ESSDERC** is to provide an annual European forum for the presentation and discussion of recent advances in semiconductor devices and circuits. The level of integration for system-on-chip design is rapidly increasing.

This is made available by advances in semiconductor technology. Therefore, more than ever before, a deeper interaction among technologists, device experts, IC designers and system designers is necessary. ESSCIRC and ESSDERC are governed by a common Steering Committee and share Plenary Keynote Presentations and Joint Sessions bridging both device and circuit communities.



CEA-Leti, STMicroelectronics, Grenoble INP and SOITEC were very proud to organize the 50th European Semiconductor Device Research Conference (ESSDERC) and the 46th European Semiconductor Circuits Conference (ESSCIRC), which was to be held in Grenoble in September 2020. Unfortunately, faced with the global pandemic situation, the organizing committee of ESSDERC 2020 Grenoble and the ESSCIRC-ESSDERC steering committee decided to offer a virtual reduced format for the 2020

conference. We would like to thank the organizing team who created and generated the new conference format in collaboration with two IEEE societies. As well as the administrative team set up around the company Sistema Congressi.

We hope that a large number of speakers scheduled to speak-face, will be able to accept invitations to present at the 2021 conference. Even in a virtual environment, the conference was still able to offer two excellent tutorials, eleven workshops, with 100 invited speakers. The educational events were organized on demand and live. Participants were able to access the various educational sessions from 7 September 2020 to November 15, 2020.

The peer selected paper submission section was replaced with IEEE journals special issues for ESSCIRC: IEEE SSC-L Special issue with 140 papers submitted vs. 200 papers submitted regularly to the physical conference and for ESSDERC: IEEE TED brief Special Issue with 45 papers submitted vs. 90 papers submitted to the physical conference.

The first tutorial **Is Quantum Computing a myth or reality?** was chaired by **Maud Vinet** (CEA-Leti) and **Farhana Sheikh** (Intel), divided into an introduction and four sessions, each offering the industrial and academic point of view. The presenters in this tutorial provided a strong foundation in physics and engineering to the audience, demystifying the field of Quantum Computing. The broader electrical engineering community from materials to devices and circuits were invited to learn more about this emerging area of research and development. The objective was to provide a global picture of current hot topics: Materials, Control, Error Correction, Semiconductor-based Spin Qubits, Superconducting Spin Qubits, and Design Tools (such as simulation, CAD, modeling, and emulation).

The workshop **Emerging solutions for imaging devices, circuits and systems**, was divided into seven sessions. It discussed leading edge and frontier technologies for image sensors opening up new dimensions in the current landscape, chaired by **Matteo Perenzoni** (FBK) and **Albert Theuvsissen** (Harvest Imaging). Imaging as usually conceived—visual pictures—is going to remain just a subset of the possibilities. The workshop addressed which technologies, devices, circuits and systems are needed to explore the dimension of wavelength, beyond visible to uncover invisible details, and of modality from quantum to computational imaging, to overcome the limitations of classical imaging. The content was tailored to image sensor designers and device engineers willing to stay up-to-date with the latest emerging

topics that could become the next big thing in imaging, with the possibility to link these to relevant application cases.

Hold by **Gabriel Molas** (CEA-Leti) and **Mahmut Sinagi** (TSMC), the workshop (divided into seven sessions) **Non-volatile memories: opportunities and challenges from devices to systems**, interested a wide range of spectators; from device users to circuit designers and system architectures and will aim to improve the interdisciplinary understanding of the potential and challenges of non-volatile memory technologies. Memories continue to be one of the keys to achieving better performance and energy efficiency at the system level. While NAND Flash has been the widely used non-volatile memory solution, new NVM technologies have emerged that offer interesting power / performance/area tradeoffs. This workshop focused on non-volatile memory technologies and discussed the opportunities they can offer for system implementations as well as the challenges associated with different technologies.

The next generations of wireless communication, 5G and beyond, will bring a revolution in the way people will be connected. For the first time, mm-wave frequencies are being considered providing the required bandwidth, high data-rates and low latency for enhanced mobile broadband, massive IoT and mission-critical control. This will bring new challenges for the technologies enabling this next generation of mobile communication. The workshop: **New 5G integration solutions, and related technologies** (from materials to system), chaired by **Nadine Collaert** (IMEC) and **Stefan G. Andersson** (Ericsson), addressed topics going from the system level all the way down to the technologies that will be key for 5G applications. It included presentations of on-going and starting EU projects Taranto and Beyond 5 as well as leading companies from industry. This workshop was open to

all students, researchers and industry partners who wanted to learn more about 5G and beyond, its opportunities and challenges.

Growing adoption of electric vehicles along with the rising trend of lightweight vehicles has been a key driver for power semiconductor devices, including diodes, silicon-controlled rectifiers (SCRs), thyristors, gate turn-off thyristors, power MOSFETs, and many others used for control and conversion of electric power. Recent progress in the wide-band-gap semiconductor such as GaN and SiC, combined with traditional Si-based insulated gate bipolar transistors (IGBTs) and MOSFETs offers multiple choices for system designers of each specific application. This workshop **Advances in device technologies for automotive industry (power devices, SiC, GaN)** chaired by **Ionut Radu** (Soitec) and **Stefan Decoutere** (IMEC) brought together experts from both academia and industry providing a comprehensive view of power devices, technologies and applications.

The sixth workshop chaired by **Sylvain Clerc** (STMicroelectronics) and **Keith Bowman** (Qualcomm), was dedicated to the **Embedded monitoring and compensation design for energy or safety constrained applications**. Integrated circuit performance has been long constrained by power and reliability. This trend is expected to continue in future SoCs and emerging IoT processors in autonomous vehicles and other applications. Meanwhile, technology scaling faces an increased sensitivity to device variability, ageing and environmental changes. In this context, adaptive designs have emerged to compensate these variations to mitigate the costs, performance penalties, and energy-efficiency losses. This embedded monitoring forum was organized for recent key contributors in the field to present their views for how to tackle these variability challenges. The aspects of monitoring system architecture, placement, accuracy

and matching were described along with the time to react to improve performance, reliability and energy efficiency.

Machine learning and AI continue to grow across almost all areas of application. While initially confined to data centers, AI now is pushed more and more to the extreme edge to process various types of sensor information directly to avoid the need for energy-hungry data transfer to the cloud. To be efficient, the energy efficiency requirements in these “tiny-AI” use cases are stringent and range from milliwatts (for example for embedded image and video processing) all the way down to microwatts (for example for keyword spotting or other always-on functions). For the design of corresponding circuits two approaches are competing: highly optimized, digital Von Neumann architectures and emerging alternative computing paradigms based on in-memory computing (IMC) and associated analog computations. While the Von Neumann approach has a head start, these new ideas are catching up. Which one prevails for what kind of applications and how to solve many of the issues with a totally different architectural approach was the central theme of this workshop **Edge AI and In-Memory-Computing for energy efficient AIoT solutions** chaired by **Andreas Burg** (EPFL) and **Marion Verhelst** (KU Leuven). It is moreover important to realize that both paradigms can also strongly take advantage of emerging technologies, such as 3D stacking and novel memory devices. As such, the workshop addressed both the ESSDERC and ESCIRC communities and targeted discussions among circuit and architecture experts, but as well technology and device experts, to explore the potential of beyond CMOS technologies for edge AI solutions.

Denis Rideau (STMicroelectronics) and **Philippe Blaise** (Silvaco) presented a tutorial **Ab-initio new materials and process developments**. This tutorial introduced atomistic methods

such as Density Functional Theory (DT), Molecular Dynamics (MD) and Non-Equilibrium Green's Functions (NEGF). Novel simulation techniques to determine atomistic details of bulk and device properties were addressed, with special emphasis on applications to materials for nano/opto electronics. The tutorial explored the potentialities of atomistic methods in predicting the physics of these new materials and structures, including defects and their electrical and optical properties. It also triggered a discussion how to bridge the results of simulations with experiments and spectroscopic signatures.

Borivoje Nikolic (University of California, Berkeley) in his workshop **RISC-V cooking session** detailed step-by-step a generation and implementation of a Berkeley University RISC-V SoC mapped on a demonstration technology. The attendance went through each generation/configuration steps until RTL level design simulation.

Thierry Baron (CEA, LTM/UGA) and **Audrey Dieudonné** (UGA) in their workshop **Toward sustainable IoT from rare materials to big data**, proposed to bring together academics and industrials in Social, Economics, and Physics/Chemistry and Technological Sciences to exchange knowledge about innovative solutions to develop a more sustainable nanoelectronics ecosystem. The access to raw materials is a major economic and geopolitical stake for the 21st century. Key resources/materials being used today in the emerging devices for the Internet of Things (IoT) must be substituted or drastically reduced in the near future. Tens of billions of electronics objects are being disseminated all over the world in homes, buildings, cars, roads, etc., therefore it is obviously a major concern to develop a sustainable electronic industry mindful of its impact right from the conception of these objects to their final use/consumption.

Emerging monolithic/sequential 3D integration of CMOS circuits reaches high interconnection densi-

ties of close to 10^8 per mm^2 . Consequently, inter-tier vias do no longer require any significant sacrifice of layout space. Combining 3D CMOS tiers of different technology nodes offers now a unique opportunity for cost effective and high performance mixed signal architectures in particular. Technology development and architecture showcases of the 3D-MUSE EU-project were presented by **Philip Häfliger** (UiO university of Oslo) at the workshop **High density 3D CMOS Mixed-signal opportunities**.

Chaired by **Wladek Grabinski** (MOS-AK), **MOS-AK** is a HiTech forum to discuss the frontiers of electron device modeling with emphasis on FOSS simulation-aware compact/SPIICE models and its Verilog-A standardization. The specific workshop goal was to classify the most important directions for the future development of the electron device models, not limiting the discussion to compact models, but including physical, analytical and numerical models, to clearly identify areas that need further research and possible contact points between different modeling domains. This workshop was designed for device process engineers (CMOS, SOI, BiCMOS, SiGe, GaN, InP, and others) who are interested in device modeling; ICs designers (RF/Analog/Mixed-Signal/MEMS/SoC/Bio/Med and related) and those starting in that area as well as device characterization, modeling and parameter extraction engineers. The content was beneficial for anyone who needs to learn what is really behind the IC simulation in modern device models.

Finally, **Dominique Thomas** (ST-Microelectronics), **Klaus Pressel** (Infineon) and **Rainer Pforr** (Zeiss) closed this event by a presentation on **IPCEI on Microelectronics: Innovative technologies for shaping the future**. In December 2018 the European Commission approved a project proposal of four EU member states—France, Germany, Italy and the UK—to start an Important

Project of Common European Interest (IPCEI) on Microelectronics. The project's overall objective is to enable research and development and first industrial deployment of innovative technologies and advanced electronics components (e.g. chips, integrated circuits, and sensors etc.) that can be integrated in a large set of downstream device applications. The integrated research and innova-

tion project involves 27 direct participants involved in 5 complementary Technology Fields, and involves a large number of partners. The IPCEI on microelectronics will have completed its first two and a half years at the time of the webinar. The direct participants presented highlights of the technologies and devices developed within the project, as well as cooperation spurred by it. The pre-

sentations illustrated each of the 5 Technology Fields: Energy efficient chips; Power semiconductors, Smart sensors; Advanced Optical equipment and Compound materials semiconductors.

It is with these time constraints in mind, that we are offering the 2021 ESSDERC—ESSCIRC conference in a hybrid format. We invite you all to participate.



Did You Know?

IEEE and EDS provide temporary Open Access to top papers from the IEEE Electron Device Letters (*EDL*) and the *IEEE Journal on Microelectromechanical Systems (J-MEMS)*.

Every month, EDL Editors select a small number of particularly remarkable articles as **Editors' Picks**. These are highlighted on the issue cover and enjoy temporary (one month) Open Access. One of these articles is further selected as Cover Article and prominently featured in its main cover graphics. Visit the EDS website for links to the current **EDL Editors' Picks**.

Stay up to date with the latest developments in the MEMS areas with **IEEE RightNow Access for J-MEMS**. Enjoy temporary Open Access (3 months) to select featured papers from the latest **J-MEMS edition**. New selections are available quarterly.

Join us on social media to receive release announcements.



UPCOMING TECHNICAL MEETINGS

2021 IEEE INTERNATIONAL FLEXIBLE ELECTRONICS TECHNOLOGY CONFERENCE (IFETC)

IEEE IFETC 2021

INTERNATIONAL FLEXIBLE
ELECTRONICS TECHNOLOGY
CONFERENCE

August 8-11 | Columbus, OH



On behalf of the IFETC Committees, we would like to invite you to submit a paper for the 2021 IEEE International Flexible Electronics Conference (IFETC-3). The IFETC-3 will be held August 8–11, 2021, at the Columbus Convention Center in downtown Columbus, Ohio. We intend to present this meeting in a hybrid format with short courses, plenary & invited talks all being simulcast for remote viewing. In person-attendees will also be able to attend contributed talk and poster sessions with presentations from both in-person and remote presenters. If needed, due to COVID-19, we are prepared to pivot to full hybrid to keep everyone safe.

Please visit the Invitation from the Conference Chair (<https://ifetc.org/program-invitation.php>) and the Abstract Submission (<https://ifetc.org/web/present-abstracts.php>) web-

pages to learn more about abstract submission and the different topical areas. You may also download the full Call for Papers (<https://ifetc.org/web/downloads/2021-IFETC-CALLFORPAPERS.pdf>) to learn more about our plans for this year's conference. I am pleased to inform you that IFETC 2021 is present also on social media, i.e. LinkedIn: <https://www.linkedin.com/company/75516602/admin/> and Twitter: <https://twitter.com/Ifetc>.

IFETC-3's Technical Program covers a wide range of cutting-edge developments in printed and flexible electronics. IFETC, started in Ottawa, Canada (2018) is a new EDS-lead international conference, focusing upon printed and flexible hybrid and non-hybrid materials, devices and systems. It will rotate between the Americas, Asia and Europe, head-

ing to Shanghai, PRC in 2022. IFETC aims to bring together a wide variety of stakeholders, from chemists, materials scientists, physicists, to mechanical and electrical engineers, the fabrication and manufacturing communities, as well as end-users, e.g. packaging and medical communities.

The IFETC-3 extended abstract submission deadline was March 15, 2021. On behalf of the Conference, International Advisory and Steering Committees, we look forward to welcoming you to IFETC-3!



*Prof. Paul R. Berger, Ph.D.
General Chair, 2021 IEEE
International Flexible Electronics
Conference, <https://ifetc.org>*

2021 IEEE INTERNATIONAL INTERCONNECT TECHNOLOGY CONFERENCE (IITC)

[HTTPS://IITC2021.ORG/](https://iitc2021.org/)



The 24th edition of IITC is sponsored by the IEEE Electron Devices Society and is co-sponsored by the Japan Society of Applied Physics as the premier conference for interconnect technology devoted to leading-edge research in the field of advanced metallization and 3D integration for ULSI applications.

IITC 2021 Will Be Held Virtually, July 6–9, 2021

To reflect the international character of the conference expressed, among others, by the participation of around 300 people from many countries, IITC is organized sequentially in Asia, Europe, and North America. IITC was held for the last time in Asia in 2018 in Taiwan and for the last time in Japan in 2013. IITC 2021 will be back in Japan in the historic city of Kyoto, Kyoto Research Park.

A decision will be made in April whether to hold the IITC in Kyoto in a virtual only or hybrid format.

The conference presents various papers describing innovative research and development on all aspects of BEOL/MOL/3D interconnects and metallization, including design, unit process, integration, and reliability. The conference attracts professionals from industry, academia, and national laboratories in semiconductor processing, interconnect design, materials and equipment development.

Over the past 20 years, miniaturization of interconnects has been promoted based on Cu damascene process. However, the Cu damascene interconnect faces performance barrier due to further miniaturization. Zsolt Tókei of imec told about this in “Inflection points in

interconnect research and trends for 2 nm and beyond in order to solve RC bottleneck” at the Focus Session “Advanced Logic Technology—Future Interconnect Technology” of IEDM 2020. New materials replacing Cu and new integration processes replacing damascene are attracting attention. Attention is also being paid to the importance of backside power delivery, heterogeneous integration, STCO, and so on. IITC 2021 will discuss the latest interconnect and 3D integration technologies for “inflection point.”

Workshop and Technical Program

Prior to the technical program, a workshop on “Metallization Technologies and Their Applications in IoT and AI Devices” by seven leading experts will be held on July 6, 2021.

Workshop Agenda

Title	Speakers
Innovation to Open New Paradigm for ICAC5/GX/DX	Manabu Tsujimura (EBARA)
Reliability challenges in advanced interconnects	Olalla Varela Pedreira (imec)
Metallization challenges in 3D NAND	Masayoshi Tagami (KIOXIA)
STT-MRAM Technology—Applications and Scalability Challenges	Kang Ho Lee (Samsung)
3D Stacking Technologies for Advanced CIS	Yoshihisa Kagawa (Sony Semiconductor Solutions)
Extending Silicon Technology for High-Bandwidth Optical Communications and Neuromorphic Computing	Bert Jan Offrein (IBM)
NanoBridge Technology for Low-power and Rad-hard AIoT Applications	Munehiro Tada (Nanobridge Semicon.)

In the technical program, our keynotes will be given by two outstanding technology leaders:

- **Prof. Mitsumasa Koyanagi**, Senior Research Fellow, New Industry Creation Hatchery Center, Tohoku University, "3D Heterogeneous Integration for Intelligent Mobile System"
- **Dr. Gitae Jeong**, Corporate EVP, Head of Corporate Office/Technology Development, Samsung Electronics, "Foundry Challenges and Opportunities Near the End of Moore's Era"

During the opening ceremony, the IITC committee will bestow the Michel Lerme Best Paper Award and Lam Research Best Student Paper Award to the 2020 recipients.

The technical program also includes invited, contributed, and poster papers presenting original and state-of-the-art work.

Throughout the conference, whether virtual or hybrid, there will

Confirmed Invited Speakers	
Topics	Invited Speakers
Advanced Interconnect	Kichul Park (Samsung)
	Koichi Motoyama (IBM)
Integration/patterning	Nelson Felix (IBM)
	Bob Socha (ASML)
DTCO	Gary Lauterbach (Cerebras)
RC Scaling	Mauro Kobrinsky (Intel)
MOL Contacts	Nicolas Breil (AMAT)
Reliability	TBD
3D	Perrine Batude (CEA-Leti)
	David Lehninger (Fraunhofer)
Memory	Sumio Ikegawa (Everspin)
	Elisa Vianello (CEA-Leti)
Novel System	Junichi Koike (Tohoku Univ.)
Beyond Cu	

be opportune moments to network and chat with industry peers and meet the conference exhibitors and sponsors.

For more information, please visit IITC2021 website <https://iitc2021.org/>.

IITC committee members look forward to seeing you virtually at IEEE IITC 2021!

Susumu Matsumoto
Tower Partners Semiconductor Co., Ltd.

22ND INTERNATIONAL VACUUM ELECTRONICS CONFERENCE (IVEC 2021)

By NATANAEL AYLON, ROBERTO DIONISIO, FELIX MENTGEN, JOHN JELONNEK, PHILIPPE THOUVENIN



We are very delighted to announce that this year's International Vacuum Electronics Conference (IVEC 2021) will be held as a virtual conference during the time frame April 27–30, 2021. At the conference, senior scientists and young researchers from all over the world will share and discuss their latest research and innovations in vacuum electronics.

This year, the organizers are very excited to connect the classic vacuum electronics community with the research community on vacuum nanoelectronics and a specific focus session is dedicated to this upcoming topic. The organizers are very thankful for the strong support of the vacuum nanoelectronics community for helping to set up this connection.

The organizers are looking forward to the participation of a large number of researchers from the field of vacuum nano electronics.

Originally planned to take place in the heart of the city of Rotterdam, the conference will have to be held virtually for the second time in a row. Having the ESA Conference Bureau as partner for the organization of this

year's conference, the organizers are convinced that this will be an exciting virtual event.

The IVEC mini courses will be dedicated to technologies that are necessary to develop and operate vacuum tubes and related systems, with a focus on space applications. The plenary talks will provide a broad overview of exciting research topics, such as vacuum nanoelectronics based on Si and III-Nitride semiconductor and the role of vacuum electronics for future accelerators and electric propulsion. These will be complemented by a talk on new developments in THz vacuum electron devices and applications in

wireless communication and imaging systems, particularly in China.

As in earlier years, another highlight will be the talk of this year's recipient of the John R. Pierce Award for excellence in vacuum electronics. Special attention is also devoted to the support of enthusiastic young scientists to ensure a bright future for the field. This is recognised by the presentation of the prestigious IVEC Best Student Paper Award and complemented by the presentation of the Vacuum Electronics Young Scientist Award (VEYS) that is aimed at recognizing outstanding contributions from early career researchers and

young professionals in the field of Vacuum Electronics.

In the tradition of IVEC, there will be unique opportunities to establish new and maintain existing friendships with colleagues, interact with customers and end-users, and meet students and academic researchers. All of this will be facilitated by setting up interactive virtual rooms for discussion and exchange.

The conference website (www.ivec2021.org) is the best source of information on technical subject categories, paper submission, registration and other important news.

We are looking forward to meeting you virtually at IVEC 2021!

"VLSI SYSTEMS FOR LIFESTYLES TRANSFORMATION" IN NEW NORMAL SOCIETY ENVISIONED AT THE 2021 SYMPOSIUM ON VLSI TECHNOLOGY, IN KYOTO, JAPAN

<https://vlsisymposium.org/>

The 2021 Symposia on VLSI Technology & Circuits will deliver a unique perspective built on the theme of **"VLSI system for Lifestyle Transformation"**. The conference will be held from June 13th to 19th. Originally planned in Kyoto, JAPAN, this week-long event will be offered in a fully virtual format due to COVID-19 pandemic, like the event last year. The symposia are jointly sponsored by the IEEE Electron Device Society (EDS) in cooperation with the IEEE Solid-State Circuits Society (SSCS) and the Japan Society of Applied Physics (JSAP).

VLSI technology and circuits will provide global opportunity promoting interactions between technologists and designers discussing the reality of applications nowadays and the break-throughs for the future. From process integration and advanced devices architecture to circuits designs



KIYOMIZU temple, Kyoto, JAPAN. Nearby VLSI symposia hotel

and systems, VLSI symposia cover innovation in a wide range of domains such as artificial intelligence, connected objects, autonomous vehicles, and biomedical applications.

To illustrate this interaction, this year the Symposia will propose three special joint focus sessions to facilitate discussion and exchanges between designers & technologists

in the following topics: "Circuit and technology for quantum computing," "Advanced packaging and 3D integration," and "Photonics interconnects & compute." Four plenary talks are programmed for the overall symposia. For Technology side:

- Siyoung Choi (President and Head of the foundry business, Samsung)

- Om Nalamasu (CTO, Applied Material).

And for Circuit side:

- Prof. Satoshi Matsuoka (Director, Riken Center for Computer Science)
- Mr. Mark Papermaster (CTO and EVP, Technology and Engineering, AMD)

Three evening panel discussions are foreseen: "Science, technology and education for new normal society", "New Generation Chip Makers vs. the Incumbents?" and "3D heterogeneous integration overview".

Helping the participants for the better understanding on advanced devices & process architecture, VLSI symposia will start with full-day short courses. Three themes based on mi-

croelectronic foundation are proposed to attendees, again this year, in relation with most important applications of our industry:

- for technology side: "Advanced process and device technology toward 2 nm-CMOS and emerging memory"
- for circuit side: "Advanced sensors circuits and systems for IoT"
- for joint side: "Computing paradigm shift including memory and new devices"

Following the symposia, a full-day Forum is arranged discussing about the post-COVID19 era, exhibiting technology for a "new normal life or remote work", and "Virtual Everything from robotic to low-power communication".

We cordially invite you to attend to the 41st Symposium of VLSI Technol-

ogy. For further information please visit the VLSI Symposia website mention below: www.vlsisymposium.org.

Committee organization staff:

Technology Symposium Chairman:
Shinya Yamakawa (Japan)
SONY semiconductor solutions

Technology Symposium Co-Chairman:
Tomas Palacios (USA)
MIT

Technical Program Chairman:
Katsura Miyashita (Japan)
Toshiba Electronic Devices & Storage

Technology Program Co-Chairman:
Gosia Jurczak (Belgium)
Lam Research

IEEE Resource Centers

EDS is excited to announce we have joined with IEEE Resource Centers to offer electron device educational content. Find short courses, technical panels, workshops, and more on [our Society's new resource center!](https://resourcecenter.eds.ieee.org/) Make this your first stop to find electron device technical training. New offerings added as they become available. Visit: <https://resourcecenter.eds.ieee.org/>



High-value technical resources accessible from any location, any time

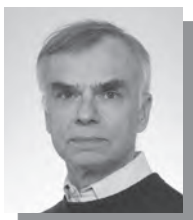
Thousands of peer-reviewed technical resources are available on demand and accessible from anywhere. Developed by experts in industry and academia, these resources support continuous learning as well as virtual instruction and professional development during the current challenging times.

Find valuable on-demand technical training in the IEEE Resource Centers



SOCIETY NEWS

MESSAGE FROM THE EDITOR-IN-CHIEF



*Daniel Tomaszewski
EDS Newsletter
Editor-in-Chief*

Dear Readers, Members of the IEEE EDS Community, welcome to the IEEE EDS Newsletter issue April 2021.

First of all, I would like to share with you sad information, that Prof. Ninoslav Stojadinović, the former EDS Newsletter Editor-in-Chief passed away at the end of 2020. From a number of EDS members we received requests to commemorate Prof. Stojadinović in the Newsletter. This shows how a respected person he was. In this issue we publish the obituary of Prof. Stojadinović, written by M K Radhakrishnan, his friend, and successor on the EiC position.

The second important message regards changes in the EDS Newsletter editorial team. Manoj Saxena has been appointed as EDS Newsletter Associate Editor-in-Chief. This position has been established by the Newsletter Oversight Committee. Manoj is an Associate Professor in Department of Electronics, Deen Dayal Upadhyaya College, University of Delhi, New Delhi, India. Until the end of 2020 he served as the EDS Newsletter Regional Editor for Region 10—South Asia. He holds a position



*Manoj Saxena,
EDS Newsletter
Associate Editor-in-
Chief*

of EDS Distinguished Lecturer. Moreover, since January 1 we have two new Regional Editors. Dr. Soumya Pandit has been appointed as the Regional Editor for Region 10, South Asia.



*Soumya Pandit, EDS
Newsletter Regional
Editor*



*Sharma Rao
Balakrishnan, EDS
Newsletter Regional
Editor*

Newsletter. At this point I would like to express our gratitude to the outgoing Regional Editor P. Susthitha Menon for her dedication and excellent job. Susi, all the best to you!

As usually, the issue contains articles in the Technical Briefs Section. The feature one, on development of the EUV Lithography in TSMC in close cooperation with ASML, was written by Anthony Yen. I would like not to reveal the details of this article, however I was personally impressed with Tony's care and attention to detail. The second Technical Brief reports the ESSDERC'2020 conference which was held in a completely non-standard virtual format due to COVID-19. Since 2020 the pandemic has been strongly affecting the technical conferences. It is reflected by the contents of the Upcoming Technical Meetings section, which announces this time four important events which will be held either virtually or in a hy-

Soumya is with Institute of Radio Physics and Electronics, University of Calcutta, India. Dr. Sharma Rao Balakrishnan has been appointed as the Regional Editor for Region 10, South East Asia, Australia & New Zealand. Sharma is with Faculty of Engineering and Built Environment, Universiti Sains Islam Malaysia. It is my great pleasure to welcome them and wish a fruitful work for the EDS

brid mode, namely: 22nd International Vacuum Electronics Conference (IVEC), 2021 Symposium on VLSI Technology (VLSI), 24th International Interconnect Technology Conference (IITC), 2021 IEEE International Flexible Electronics Conference (IFETC). We wish the attendees and the organizers great events, interesting topics and fruitful discussions.

Thanks to Manoj Saxena we are willing to intensify the presentation of Young Professionals and Women in Engineering in the Newsletter. Following the idea dated 2015 of M K Radhakrishnan, Editor-in-Chief, we will interview outstanding young members of EDS. Prominent women—scientists and engineers will present their careers and achievements as well. They all will show students, young engineers, and researchers, opportunities of work in a demanding, though fascinating domain of electron device development, as well as advantages of EDS membership. In this issue you can read four articles in these series. I hope that you will find them interesting.

As the topic of YPs is discussed, I would like to share with you information, that the article on an impressive progress of semiconductor R&D in India, written by Udayan Ganguly and Sandip Lashkhare, and published in the previous issue of the Newsletter aroused a lively discussion on LinkedIn. The discussion has shown the relevance of this topic for the electron device-related community in India.

The Regional News section brings articles on daily activities (meetings, workshops) of several Chapters in US, South America, Asia, Europe. Among them there is a pretty broad, technical report on the 3rd IBM IEEE CAS/EDS AI Compute Symposium, and the

article on VIII Congresso Brasileiro de Energia Solar (CBENS), accompanied by interesting impressions from the IEEE member delegate.

Regarding the Regional News section, a drop of contributions from the Chapters is noticeable. Probably it is a consequence of the pandemic. It is

our concern to address this issue in the coming months.

Dear Readers, if you have any suggestions, comments regarding the Newsletter contents, please do not hesitate to contact me or Manoj Saxena. We will be very glad to receive your feedback.

Finally, I would like to express my thanks to all the Authors of articles in this issue, to the Regional Editors and all the members of the Editorial Team.

*Sincerely,
Daniel Tomaszewski*

IN MEMORY OF PROF. NINOSLAV D. STOJADINOVIĆ

By MK RADHAKRISHNAN



*Prof. Ninoslav D.
Stojadinović*

NINOSLAV D. STOJADINOVIĆ, a dynamic academician who pioneered in developing microelectronics research in central Europe (Serbia Montenegro) passed away on 25 December 2020 as a result of COVID-19 infection. Nino was a dedicated volunteer instrumental in initiating a number of EDS activities in the Region including Chapters and Conferences.

Ninoslav was born in Niš, Serbia on 20 September 1950. He received his B.S.M.S. and Ph.D., all in Electrical Engineering from University of Niš in 1974, 1977 and 1980 respectively. Later he joined the Faculty of Electronic Engineering in University of Niš, where he became a Full Professor in 1991. He was Head of the Department of Microelectronics and Dean of the Faculty. Nino led the Serbian Academy of Science and Arts (SASA) in various capacities: as Vice-Director of SASA Research Center and President of SASA Branch in Niš (2016–20).

Stojadinović was a visiting professor at Technical University of Wien and was a member of International Scientific Advisory Boards at Center for Nanotechnologies, Clemson University (USA) and Center of Excellence in Micro and Nanotechnology, Warsaw University of Technology (Poland). He was associated with

Griffith University (Australia), Brown University (USA), National Technical University of Athens (Greece) and Technical University of Sofia (Bulgaria) as a member of expert's commissions. Nino was a member of European Expert Commission for the Seventh Research Framework Program EC FP7 (from 2005) and consultant of National Science Foundation of Taiwan Government (NSFTG) from 2008.

Nino mentored 48 Dipl. Ing., 13 Master and 17 Ph.D. theses during his four decades of academic career. He authored more than 250 technical papers and authored/co-authored 3 books. He was a member of the Editorial Board of Microelectronics Journal (Elsevier) and its Editor-in-Chief (1993–1995). Nino was a Regional Editor and the Editor-in Chief of Microelectronics Reliability (Elsevier) journal from 1996 to 2017. Since 2013, he has been Editor-in-Chief of Facta Universitatis journal Series: Elec-

tronics and Energetics. Also, he was a member of Scientific and/or Programme Committees of more than 50 international scientific meetings including MIEL conference, which he groomed as its Chair (1989-onwards) to become a prominent microelectronics conference in Europe.

Nino was one of the very active IEEE EDS volunteers in the Europe Region from mid 1980s and was Chair of IEEE Serbia & Montenegro Section (2002–05). He was the founder Chair of IEEE EDS/SSC Chapter in Niš Serbia. He was a member of EDS AdCom (2001–2005) and Region 8 SRC Chair. Nino was Regional Editor (1998–2001) and Editor-in Chief (2002–2012) of the IEEE EDS Newsletter, during which the Newsletter was redesigned to the present format. Nino served as IEEE EDS Distinguished Lecturer for more than 20 years and was IEEE Life Fellow.

Ninoslav Stojadinović had significant political and diplomatic experience. He was a member of Assembly of the Republic of Serbia (1997–2000), member of Assembly of the State Union of Serbia and Montenegro, and its representative to the Parliamentary Assembly of the Council of Europe (2004–2006). Nino was Ambassador of the Republic of Serbia to the Kingdom of Sweden (2005–2011) and Bosnia and Herzegovina (2011–2013). He was Deputy Speaker of Assembly of the Republic of Serbia (2014–2016). Nino is survived by his wife Anđelka and son Dragan.



CONGRATULATIONS TO THE 16 NEWLY ELECTED IEEE ELECTRON DEVICES SOCIETY FELLOWS

EFFECTIVE JANUARY 1, 2021

Deji Akinwande

for contributions to wafer-scale graphene synthesis and application to flexible devices

Hideaki Aochi

for contributions to three dimensional flash memories

Benton Calhoun

for contributions to sub-threshold integrated circuits and self-powered systems

Yogesh Chauhan

for contributions to compact modeling of Si and GaN transistors

Vasilis Fthenakis

for contributions to photovoltaics technology

Robert Henderson

for contributions to solid-state single photon imaging

Ali Keshavarzi

for contributions to low-power circuits and devices in scaled CMOS technologies

Chang-jin Kim

for research of surface-tension-based microelectromechanical

Gourab Majumdar

for contribution to power semiconductor devices and intelligent power module

Jun Ohta

for contributions to CMOS image sensors and devices for biomedical applications

Bryan Root

for leadership in improving semiconductor reliability test methods

Ashwin Seshia

for contributions to resonant-based inertial and mode-localized sensors

Tetsuya Suemitsu

for contributions to high-frequency high-electron-mobility transistors

Takatoshi Tsujimura

for contributions to the development of organic-light-emitting diode systems

Yifeng Wu

for contributions to Gallium Nitride microwave and power conversion devices

Shinji Yuasa

for contributions to MgO-based magnetic tunnel junctions

*Samar Saha
EDS Fellows Chair*

NEW EDS SERVICE



NEW!

EDS Podcasts Available to Everyone!

EDS is pleased to announce our new podcast series. Join us as we host interviews with some of the most successful members of our Society sharing their lives and careers. Their insight and wisdom will be invaluable inspiration and knowledge for those in the engineering field. Stay tuned to our social media channels and website for future announcements on upcoming events.



EDS HUMANITARIAN PROGRAMS

IEEE EDS members, the world's leading electron device engineers, bringing to life the IEEE mission of advancing technology for the benefit of humanity.

The Society funds many volunteer-designed projects, with a focus on under-served communities around the world. Recent initiatives have included low-cost ventilators and cashier sanitizer boxes developed for use during the Covid-19 pandemic; engineering short courses for students and professionals; student labs at universities; STEM classes and sum-

mer schools on renewable energy, robotics and circuits, designed especially for young students; community technology literacy workshops; funding to cover registration fees for engineering students to attend IEEE technical conferences; as well as sponsored placement opportunities for current and newly graduated students to spend time in industry on topics aligned with our Society's field of interest.

Many EDS members collaborated with other IEEE programs and volunteers to assist indigenous and

rural communities with water quality monitoring, irrigation systems, environmental disaster emergency alerts, and solar-powered desalinization projects.

Note that some projects were completed before the Covid-19 pandemic, but others were reprogramed to be held virtually when possible. Several projects are temporarily on hold until it is safer for in-person events to resume. Visit our Society website often to learn about new projects as they are completed: <https://eds.ieee.org/about-eds/eds-humanitarian-projects>




Towards a Smart Village through solar-powered desalinization for the Indigenous Wayúu peoples living in the Guajira peninsula desert

Paul R. Berger¹, Carlos Cachazo², Mauricio Pardo³ and Neil Mendez Turizo⁴

¹Ohio State University, Columbus, Ohio USA
²SIERGROU, Barranquilla, Colombia
³Universidad del Norte, Barranquilla, Colombia
⁴Servicio Nacional de Aprendizaje (SENA), Riohacha, Colombia





Working with Wayúu Village Elders

The Wayúu: High incidence of asthma in children and elderly




Implementation Stage IEEE and UniNorte!

Portable system with batteries and filters inside and solar panels mounted outside like an umbrella



Salt infused soil for millennia



Poor, salty and contaminated water



Rusty, donated shipping container cut shorter & ventilation added






AWARDS & CALLS FOR NOMINATIONS

2021 IEEE EDS ROBERT BOSCH MICRO AND NANO ELECTRO MECHANICAL SYSTEMS AWARD WINNER

The 2021 IEEE EDS Robert Bosch Micro and Nano Electro Mechanical Systems Award was presented to Professor Chang-Jin Kim, University of California, Los Angeles, CA, USA, at the 2021 IEEE MEMS virtual Conference, January, 2021. This prestigious award recognizes and honors advances in the invention, design, and/or fabrication of micro- or nano-electromechanical systems and/or devices.

Professor Chang-Jin "CJ" Kim received his B.S. from Seoul National University, M.S. from Iowa State University, and Ph.D. from the University of California, Berkeley, all in mechanical engineering. After a postdoctoral visit to the University of Tokyo, he joined the faculty at the University of California, Los Angeles (UCLA) in 1993, where he is a Distinguished Professor, holds the Volgenau Endowed Chair in Engineering, and has an appointment in Mechanical and Aerospace Engineering Department, a joint appointment in Bioengineering Department, and a membership in California NanoSystems Institute (CNSI). Directing the Micro and Nano Manufacturing Lab, Prof. Kim performs research in micro electro mechanical systems (MEMS) and Nanotechnology, including design and fabrication of micro/nano



*Professor Chang-Jin "CJ" Kim
For pioneering surface-tension-based micro-electromechanical systems (MEMS) that led to electrowetting digital microfluidics and superhydrophobic drag reduction*

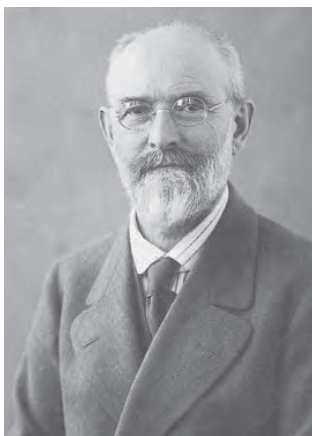
structures, actuators, and systems, with a focus on utilizing surface tension as a mechanical force. The recipient of Research Excellence Award (Iowa State Univ.), TRW Outstanding Young Teacher Award (UCLA), National Science Foundation (NSF) CAREER Award, Association for Laboratory Automation (ALA) Achievement Award, Samueli Outstanding Teacher Award (UCLA), and Ho-Am Prize in Engineering (the Ho-Am

Foundation), Prof. Kim has served on numerous professional and governmental activities, including General Chair of the 2014 Institute of Electrical and Electronics Engineers (IEEE) International Conference on MEMS. An American Society of Mechanical Engineers (ASME) Fellow and an American Institute for Medical and Biological Engineering (AIMBE) Fellow, he is currently serving on the Editorial Board of the IEEE Journal of MEMS, on the Editorial Advisory Board for the Institute of Electrical Engineers of Japan (IEEEJ) Transactions on Electrical and Electronic Engineering (TEEE), on the Editorial Board of Micro and Nano Systems Letters, as a Co-Editor-in-Chief of Functional Composites and Structures, on the International Steering Committee of the International Conference on Solid-State Sensors, Actuators and Microsystems (Transducers), and on the International Steering Committee of Electrowetting Conference. A member of the Council of Korean Americans (CKA), Prof. CJ Kim has also been active in the commercial sector as a scientific advisor, consultant, and founder of start-up companies.

*Osamu Tabata
EDS Bosch Award Chair*



IEEE ROBERT BOSCH MICRO AND NANO ELECTRO MECHANICAL SYSTEMS AWARD



Robert Bosch (1861-1942)

Inventor, Entrepreneur, Founder of Robert Bosch GmbH

The Robert Bosch Micro and Nano Electro Mechanical Systems Award was established by the IEEE Electron Devices Society in 2014, to recognize and honor advances in the invention, design, and/or fabrication of micro- or nano-electromechanical systems and/or devices. The contributions to be honored by this award should be innovative and useful for practical applications.

This award is sponsored by the IEEE Electron Devices Society, with financial support from Robert Bosch LLC. It is intended that the award will be presented annually to an individual or to as many as three individuals whose achievements and contributions are judged to meet the selection criteria for the award. The award will be presented at an IEEE conference of the winner's choice. It is not necessary for the recipient(s) to be a member(s) of IEEE.

The recipient will receive a US\$10,000 honorarium, travel expenses to attend the award presentation, a bronze medal, and a certificate. In the event that more than one awardee is selected the cash honorarium will be equally divided among the recipients. Each recipient will receive a bronze medal and a certificate.

Please visit the EDS website for more information on this award:

<https://eds.ieee.org/awards/robert-bosch-micro-and-nano-electro-mechanical-systems-award>.

Nominations for this award should be made using our [online nomination form](#), and submitted before midnight (EST) on October 2nd. Letters of recommendation must be sent directly to l.riello@ieee.org according to the same schedule.



CONGRATULATIONS TO ASIF KHAN 2020 IEEE EDS LESTER F. EASTMAN AWARD WINNER



Lester F. Eastman

Professor Asif Khan, University of South Carolina, Columbia, SC, USA, was selected as the first IEEE EDS Lester F. Eastman Award winner. The Lester F. Eastman Award is given to recognize individuals with outstanding achievement in high-performance semiconductor devices and is named after the late Professor Lester F. Eastman.

Asif Khan is a Carolina Distinguished Professor in the Electrical Engineering Department at University of South Carolina. From 1979 to 1985 he worked at Honeywell Inc. in Minneapolis, Minnesota as a Senior Principal Research Scientist. There, he initiated research in metal-organic chemical vapor deposition and fabrication of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ solar-blind ultra-violet (UV) sensors. From 1985 to 1987 he worked on the optical recording project at 3M Corporation in Saint Paul, Minnesota. For the next 10 years (1987–1997) he served as the Vice President of the Optoelectronics Division of APA Optics in Blaine, Minnesota. Since 1997 he has been working at the University of South Carolina.

His research at APA Optics and South Carolina resulted in the first demonstrations of high-quality AlGaIn-GaN heterostructures. This enabled him and his teams to demonstrate for the first time the key



Asif Khan
University of South Carolina,
Columbia, SC, USA

building blocks for III-N high-frequency and high-power electronic devices and deep ultraviolet light emitting diodes (LEDs). These first demonstrations included: (i) GaN metal-semiconductor field-effect transistor (1992); (ii) 2-dimensional electron gas in GaN-AlGaIn heterojunction (1992); (iii) GaN-AlGaIn high electron mobility transistor (HEMT) (1993); (iv) GaN-AlGaIn insulated-gate HEMT (1999); (v) AlInGaIn-based UV-B/UV-C LEDs (2001); and (vi) high-power sub-280-nm UV-C LEDs (2002). More recently, his South Carolina group has pioneered novel ultra-high voltage ul-

trawide bandgap AlGaIn-channel HEMTs and integrated photonic circuits of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ -based UV-C LEDs, photodetectors, and waveguides.

Asif was the founding member of two South Carolina small businesses which commercialized the technology that his South Carolina research group developed. These businesses, Nitek Inc. and Sensor Electronic Technology Inc. were later acquired by Seoul Semiconductor and Seoul Viosys Company as their US subsidiary. He is the recipient of the University of South Carolina Russell Research Award for Science and Engineering (2002) and the State of South Carolina Governor's Award for Excellence in Scientific Research (2015).

Asif received his B.S. (Hons) and M.S. degrees from the University of Karachi and his Ph.D. from MIT. He is a Fellow of the IEEE. He serves as a member of the international advisory committee of the International Workshop on Nitride Semiconductors (IWN) and the International Conference on Nitride Semiconductors, the two major gatherings of the III-N research community. He lives with wife Rubina in Irmo, South Carolina.

James C.M. Hwang
EDS Lester F. Eastman Award Chair



IEEE EDS LESTER F. EASTMAN AWARD

CALL FOR NOMINATIONS

The IEEE Electron Devices Society invites the submission of nominations for the Lester F. Eastman Award. This award is presented annually to honor an individual who has made an outstanding achievement in high-performance semiconductor devices. The recipient is awarded a certificate and a check for \$2,000, presented at the IEEE International Electron Devices Meeting (IEDM).

Description: To recognize individuals with outstanding achievement in high-performance semiconductor devices

Prize: \$2,000 and a plaque

Funded: Funded by the Lester F. Eastman endowment fund and the IEEE Electron Devices Society

Eligibility: Any person active in the field of semiconductor devices, whether or not they are members of the IEEE Electron Devices Society, are eligible for the award. The EDS Lester Eastman Award cannot be given to a candidate for the same work for which an IEEE Technical Field Award, IEEE Medal, or other society level award was previously received.

Basis for Judging: Criteria considered by the selection committee will include an impact on the field of semiconductor devices. Evidence should include examples of leadership and professional interaction. Tangible supporting evidence in the form of publications, patents, and/or transition(s) to practice should be provided.

Presentation: Annually, at the International Electron Devices Meeting (IEDM)

Visit: <https://eds.ieee.org/awards/lester-f-eastman-award>

Donate: <https://www.ieeefoundation.org/Eastman>

Contact: If you have additional questions, contact the EDS Executive Office at eds@ieee.org

Nomination form: [Nomination form link](#)

Deadline to submit nominations: July 1st

2020 IEEE EDS J.J. EBERS AWARD WINNER

Professor Arokia Nathan of University of Cambridge, Cambridge, United Kingdom, was selected as the 2020 J.J. Ebers Award winner. The J.J. Ebers Award is the most prestigious award of the IEEE Electron Devices Society for outstanding technical contributions to electron devices. This award recognizes Professor Nathan "For contributions to thin film transistors and flexible/foldable electronics integration strategies".

Arokia Nathan is a leading pioneer in the development and application of thin film transistor technologies to flexible electronics, display and sensor systems. In a research career spanning over thirty years, he has had a profound impact on the design and development of TFT circuit architectures that greatly enabled the realization of commercial OLED displays, high-resolution image sensors, and large area 3D touch sensor systems. His research has resulted in 600 publications including 4 books. A prolific inventor, his ideas led to over 110 patents and the establishment of four companies to commercialize the technology: IGNIS Innovation developing fully-compensated TFT-OLED rigid and flexible displays, Cambridge Touch Technologies on 3D smart-skin for human-machine interactivity, ACXEL Technology on high-resolution digital fluidics for in-vitro and single-cell diagnosis, and CamXT on TFT compact modeling and parameter extraction.

Following his PhD in Electrical Engineering, University of Alberta, Canada in 1988, he joined LSI Logic



Arokia Nathan, 2020 IEEE EDS J.J. Ebers Award Winner

USA working on advanced multi-chip packaging. Subsequently he was at the Institute of Quantum Electronics, ETH Zürich, Switzerland, before joining the Electrical and Computer Engineering Department, University of Waterloo, Canada. Here he held the DALSA/NSERC Industrial Research Chair in sensor technology and then the Canada Research Chair in nanoscale flexible circuits, and in 2000 led the establishment of the Giga-to-Nanoelectronics Centre. In 2006, he joined the London Centre for Nanotechnology, University College London as the Sumitomo Chair of Nanotechnology. He moved to Cambridge University in 2011 as the Chair of Photonic Systems and Displays, and directed a large multi-disciplinary research team on heterogeneous integration of sensors, TFTs and en-

ergy devices for wearable technologies. He is currently a Bye-Fellow and Tutor at Darwin College, University of Cambridge.

In recognition for his role in TFT technology and flexible electronics, he was awarded the NSERC E.W.R. Steacie Fellowship in 2001, the Royal Society Wolfson Research Merit Award 2006, and the BOE Distinguished Contribution Award for TFT Compact Modeling and Circuit Design 2016. He was a China 1000 Talent Plan Laureate 2013 and received the Jiangsu Friendship Award 2014. In 2019, the University of Waterloo bestowed upon him Doctor of Science honoris causa in recognition for his leadership in undergraduate program development in Nanotechnology Engineering.

Arokia Nathan had leadership roles in IEEE with service to EDS, Photonics Society and the Solid State Circuits Society. He served on the Board of Governors of EDS and on Editorial Boards of IEEE Proceedings, IEEE Trans. Devices, Materials, and Reliability, and IEEE Electron Device Letters. He also served as Editor-in-Chief of IEEE/OSA Journal of Display Technology and as Guest Editor for a two-part Special Issue on Flexible Electronics Technology in the Proceedings of the IEEE in 2004. He is a Fellow of IEEE (USA), an IEEE/EDS Distinguished Lecturer, a Chartered Engineer (UK), and Fellow of the Institution of Engineering and Technology (UK).

*Samar Saha
EDS J.J. Ebers Award Chair*

IEEE ELECTRON DEVICES SOCIETY J.J. EBERS AWARD

Nominate:

J.J. Ebers Award
on-line nomination form:

<https://ieeeforms.wufoo.com/forms/xl0lxns05xzwir/>

Submission Deadline:

July 1, 2021

Contact:

If you have any questions regarding the EDS J.J. Ebers Award, please contact Laura Riello of the EDS Executive Office at l.riello@ieee.org

Visit:

<https://eds.ieee.org/awards/j-j-ebers-award>

**CALL FOR NOMINATIONS**

The IEEE Electron Devices Society (EDS) invites the submission of nominations for the 2021 J.J. Ebers Award. This award is presented annually by EDS to honor an individual(s) who has made either a single or a series of contributions of recognized scientific, economic, or social significance to the broad field of electron devices. The recipient(s) is awarded a plaque and a check for \$5,000, presented at the International Electron Devices Meeting (IEDM) or any one of the EDS's flagship conferences.

2020 IEEE EDS DISTINGUISHED SERVICE AWARD

The IEEE Electron Devices Society (EDS) is extremely proud of the services that it provides to its members. EDS members generate the leading edge developments in the field of electron devices and share these results with their peers and the world-at-large by publishing their papers in EDS journals and presenting results in its meetings. This is a global activity that is effective because of the efforts of numerous volunteers. Many of these dedicated volunteers labor in relative obscurity, with their only reward being the satisfaction that they receive in being an important part of a successful organization, namely of the IEEE Electron Devices Society. One means of thanking these volunteers is to recognize their contributions through the EDS Distinguished Service Award.

The recipient of the 2020 EDS Distinguished Service Award was Professor Jacobus Swart, State University of Campinas, FEEC/UNICAMP, South Brazil. Please visit the IEEE EDS website to view the award presentation video.

Jacobus W. Swart received his B. Engineering and Dr. Engineering Degrees in 1975 and 1981 respectively, from the Polytechnic School of the University of São Paulo, Brazil. After his Dr. Degree, he worked at the following institutions: K. U. Leuven, Belgium, 1982-83, as a post-doc, CTI, Campinas, 1984; University of São Paulo, 1985-88, as Assistant Professor; SID Microeletrônica, 1986, as process engineering; RTI, USA, 1991, as a Visiting Scientist and since 1988



Jacobus Swart, 2020 IEEE EDS Distinguished Service Award winner

at State University of Campinas, as Full Professor until retirement in 2013, when he assumed a position as collaborator professor. He served as director of the Center for Semiconductor Components, from April 1998 to April 2005. From May 2007 until June 2011 he was on leave from the University to serve as General Director of CTI, a national research center. During this time he was the coordinator of the IC Brazil program, leading ASIC design training centers and a network of local design houses. He was the leader of a large research network in Brazil, called INCT NAMITEC, from 2001 until 2016. Since 2013 he provides service to imec, Belgium, as their representative in Brazil. Dr. Swart has published around 300 papers in Journals and Conferences covering his research work on mate-

rials, fabrication processing, device characterization and modelling and ASIC design. He is ranked as fellow researcher, level 1A (highest) at CNPq and is a Fellow of the São Paulo State Academy of Science and of National Engineering Academy.

He is a Life Fellow of IEEE and served on different positions for EDS, as secretary, BoG member, Distinguished Lecturer, member of many committees, Region 9 Subcommittee for Regions and Chapters (SRC) Chair, founder and chair of South Brazil EDS chapter and advisor of EDS student chapter at UNICAMP. He was member and/or chair of many organizing conference committees in Region 9, especially in Brazil, including conferences as SBMicro, ICCDCS and LAEDC. He was president of SB-Micro Society for two terms, and promoted the SBMicro conference as a technically co-sponsored conference of EDS.

Jacobus was born in The Netherlands in 1950 and emigrated to Brazil with his parents and ten brothers and sisters in 1958, as farmers. He was the only one that did not follow the farming profession. He met and married Nilza during undergraduate studies and they have three children: Hugo, Laura and Julia, two Electronics Engineers and one Economist. Presently, he and Nilza are blessed with ten grandchildren. EDS is proud to extend this recognition for his many years of selfless dedicated service.

*Fernando Guarin
EDS Awards Chair*

2020 IEEE ELECTRON DEVICES SOCIETY EDUCATION AWARD WINNER

The EDS Education Award recognizes an IEEE/EDS Member from an academic, industrial, or government organization with distinguished contributions to education within the fields of interest of the IEEE Electron Devices Society. Professor Valipe Ramgopal Rao was selected as the 2020 EDS Education Award winner. The award cites Professor Rao *“For educational leadership and establishing Nanoelectronics research programs in India.”*

Prof. V. Ramgopal Rao is currently the Director at IIT Delhi. Before joining IIT Delhi as the Director in April 2016, Dr. Rao served as a P. K. Kelkar Chair Professor for Nanotechnology in the Department of Electrical Engineering, IIT Bombay. Dr. Rao has over 450 research publications in the area of nano-scale devices & sensors and is an inventor on 45 patents and patent applications. For his research contributions, Dr. Rao is elected a Fellow of IEEE, a Fellow of the Indian National Academy of Engineering, the Indian Academy of Sciences, the National Academy of Sciences, and the Indian National Science Academy. Prof. Rao's work is recognized with many awards and honors in the country and abroad. Prof. Rao was an Editor for the IEEE Transactions on Electron Devices during 2003–2012 for the CMOS Devices and Technol-



Professor Valipe Ramgopal Rao

ogy area and currently serves on the Editorial Advisory Board of ACS Nano Letters. He is a Distinguished Lecturer, IEEE Electron Devices Society and interacts closely with many semiconductor industries both in India and abroad.

Prof. Ramgopal Rao has helped create a vibrant ecosystem for nanoelectronics education, research and entrepreneurship in India. Prof. Rao was the Chief Investigator for the path-breaking Center of Excellence in Nanoelectronics (CEN) project at IIT Bombay, set up jointly with IISc Bangalore, by the Government of India. Prof. Rao was also the archi-

tect and the Chief Investigator for the Indian Nanoelectronics Users Program (INUP), which initiated Nanoelectronics activities in over 200 institutions in the country. The INUP program has impacted the research activities of over 10,000 researchers in India so far.

Prof. Rao played a key role in driving the emergence of a vital industry-academia collaboration in India through the Ministry of Electronics & Information Technology (MeitY) and the Department of Science & Technology, Govt. of India programs. Based on his leadership in education and research and through his involvement with the institutes in formulating the proposals, MeitY has set up seven National Centres of Excellence in the field of Nanoelectronics across the country, leading to a significant growth of this vital sector in India. Prof. Rao is also responsible for setting up the country's first Prototype Manufacturing Facility at IIT Bombay for use by the Small & Medium scale industries for developing products and prototypes in the area of Nanoelectronics. For more information about Prof. Ramgopal Rao's current research activities, please visit <https://www.ee.iitb.ac.in/~rrao/>.

*Muhammad Ashraful Alam
2020 EDS Education Award Chair*



2021 EDS Education Award Call For Nominations



The IEEE Electron Devices Society invites the submission of nominations for the EDS Education Award. This award is presented annually by EDS to honor an individual who has made distinguished contributions to education within the field of interest of the Electron Devices Society. The recipient is awarded a plaque and a check for \$2,500, presented at the IEEE International Electron Devices Meeting (IEDM).

The nominee must be an EDS member engaged in education in the field of electron devices, holding a present or past affiliation with an academic, industrial, or government organization. Factors for consideration include achievements and recognition in educating and mentoring students in academia or professionals in the indus-

trial or governmental sectors. Specific accomplishments include effectiveness in the development of innovative education, continuing education programs, authorship of textbooks, presentation of short-courses at EDS sponsored conferences, participation in the EDS Distinguished Lecturer program, and teaching or mentoring awards.

Since this award is solely given for contributions to education, the nomination should exclude emphasis on technical contributions to engineering and physics of electron devices.

The nomination form can be found on the EDS website: <https://eds.ieee.org/awards/education-award>

The deadline for the submission of nominations for the 2020 award is September 1, 2021.

2020 IEEE Electron Devices Society Early Career Award Winners

The EDS Early Career Award recognizes young IEEE/EDS members who have made outstanding contributions in an EDS field of interest during the early years of their professional career after graduation.

The 2020 EDS Early Career Award winners are as follows: Harshit Agarwal from the Indian Institute of Technology, Jodhpur, India and Max Shulaker of Massachusetts Institute of Technology, Cambridge, MA, USA. Please visit the IEEE EDS website to view the award presentation video.

Harshit Agarwal, Indian Institute of Technology, Jodhpur, India



Dr. Harshit Agarwal is Assistant Professor in the Dept. of Electrical Engineering, Indian Institute of Technology (IIT), Jodhpur, India.

He received the PhD degree from IIT-Kanpur in 2017. Before joining IIT-Jodhpur, he worked with the

BSIM group as post-doc fellow cum Center Manager of Berkeley Device Modeling Center, University of California, Berkeley, USA for 3 years. Dr. Agarwal is highly fascinated with Nanoelectronics. In this era of the Internet of Things (IoT) and Artificial Intelligence (AI), there is a need of faster and low power transistors. His research group at IIT-Jodhpur works in compact modeling, simulation and characterization of emerging transistor and memory devices for AI, IoT and neuromorphic applications. His other research interest includes steep-slope devices, advanced CMOS architecture including nanosheet and nanowire for sub-3 nm technology nodes, 2D semiconductor devices and their compact modeling, modeling for millimeter wave applications etc. His work on development of new capacitance matching technique for negative capacitance transistors selected for the front cover of IEEE Electron Device Letters (EDL). It also featured in EDL list of popular documents for nine

consecutive months, while topping the list for 3 months.

Dr. Agarwal has developed SPICE compact models for the logic, analog, and RF applications, which are used worldwide both in academia as well as in industry for circuit design, simulations and device-circuit co-optimization. He is a lead developer of the BSIM based compact model of high-voltage devices. These models are rigorously tested for accuracy and numerical robustness before being used for circuit design prior to actual fabrication, thereby saving lots of cost and time. Dr. Agarwal is a member of IEEE Electron Devices Society Compact Modeling Committee, is recipient of two IEEE best paper awards, has delivered talks on compact modeling at various workshops and featured twice in IEEE EDS list of golden reviewers of EDL and TED. He has published one book and more than 60 articles in journals and conferences of international repute including IEDM, EDL, TED etc.

**Max Shulaker, Massachusetts
Institute of Technology,
Cambridge, MA, USA**



Max Shulaker is an Associate Professor in the Department of Electrical Engineering and Computer Science, where he leads the NOVELS (Novel Electronic Systems Group) at MIT. His research group focuses on

the broad area of nanosystems: understanding and optimizing multidisciplinary interactions across the entire computing stack to enable the next generation of energy-efficient computing systems. Key breakthroughs from the group range from low-level nanomaterial synthesis to novel fabrication processes and circuit designs for emerging nanotechnologies, up to new system architectures. His passion lies in transforming fundamen-

tal scientific advances into working systems that promise to impact and improve our daily lives. Through their unique approach, Max and his students have demonstrated some of the most advanced beyond-silicon electronic systems realized to-date, with applications ranging from next-generation computers to healthcare.

*Ravi Todi
EDS Early Career Award Chair*



2021 IEEE EDS EARLY CAREER AWARD CALL FOR NOMINATIONS



Description: Awarded annually to individuals to promote, recognize and support Early Career Technical Development within the Electron Devices Society's field of interest

Prize: An award of US\$1,000, a plaque; and if needed, travel expenses not to exceed US\$1,500 for each recipient residing in the US and not to exceed US\$3,000 for each recipient residing outside the US to attend the award presentation.

Eligibility: Candidates must be an IEEE EDS member and must have received his/her first professional degree within the 10th year defined by the August 15 nomination deadline and has made contributions in an EDS field of interest. Nominators must be IEEE EDS members. Previous award winners are ineligible.

Selection/Basis for Judging: The nominator will be required to submit a nomination package comprised of the following:

- The nomination form can be found on the EDS web site, containing such technical information as the nominee's contributions, accomplishments and impact on the profession or economy and a biographical description.
- A minimum of two and a maximum of three letters of recommendation from individuals familiar with the candidate's technical contributions and other credentials, with emphasis on the specific contributions and their impacts.

The basis for judging includes such factors as: the demonstration of field leadership in a specific area; specific technical contribution(s); impact on the profession or economy; originality; breadth; inventive value; publications; honors; and other appropriate achievements.

Schedule: Nominations are due to the EDS Executive Office on August 15th each year. Candidates will be selected by the end of September, with presentation to be made in December.

Presentation: At the EDS Awards Dinner that is held in conjunction with the International Electron Devices Meeting (IEDM) in December. The recipients will also be recognized at the December EDS BoG Meeting.

Nomination Form: Complete the nomination form by August 15, 2021. All endorsement letters should be sent to l.riello@ieee.org by the deadline.

For more information contact: l.riello@ieee.org or visit: <http://eds.ieee.org/early-career-award.html>

WOMEN IN ENGINEERING

LEDA LUNARDI—HER JOURNEY AND WORDS OF MOTIVATION FOR WOMEN IN SCIENCE AND ENGINEERING

LEDA LUNARDI, PROFESSOR, ELECTRICAL AND COMPUTER ENGINEERING
NORTH CAROLINA STATE UNIVERSITY



My journey: In my wildest dreams, I could never imagined to have the career I have today even if I have tried. In my family,

I am the first generation not only to attend college but also to obtain advanced degrees: first a M.Sc. in Physics from University of São Paulo, Brazil, and then a PhD in Electrical Engineering from Cornell University, New York. At the time I finished my PhD, it was the first thesis in the USA on the topic of AlGaAs/GaAs Heterojunction Bipolar Transistors for microwave operation, giving me a few opportunities to start a professional career in the USA.

As a member of the technical staff in AT&T (then Bell Labs) in Murray Hill, I joined the heterojunction high mobility transistors' group. Achievements of this group were then among the best results in the digital circuits domain. The goal was to develop HBT-based digital circuits for telecommunication applications. The work started almost from scratch. With talented collaborators, we published the first demonstration of GaAs-based HBTs decision circuits along novel transistor structures facilitating the circuit manufacturing. At the same time, other groups started reporting advanced progress in different InP-based HBTs because of the compatibility with the optical wavelength.

Next, I moved to another group in Holmdel that was doing research

on InP-based HBT integrated receivers. There we demonstrated the first InP-based monolithically integrated photoreceiver operating at 10 Gb/s and 20 Gb/s followed by multichannel wavelength division multiplexing (WDM) photoreceivers. The photoreceiver operating at 10 Gb/s was outstanding, yet these results were even more significant because it was the first time that a monolithically integrated photoreceiver outperformed hybrid versions by more than 6 dB in signal-to-noise ratio.

Since then, after more efficient modulation formats and new optical fibers had emerged, my research interest has changed considerably. Some of the important results obtained with students and collaborators as at NC State are: integrated circuits with amorphous Indium Gallium Zinc Oxide (IGZO) thin film transistors made by pulsed laser deposition, compact modeling of InAs-based Tunneling Field Effect Transistor, and the polymer-based dielectric mirrors able to regulate the light intensity and to tune incident wavelengths for display applications.

Future research: There are several opportunities already happening in devices' research, which is a rich field and maintains solid since the invention of the bipolar junction transistor almost 70 years ago. Today the difference is that digital technology permeates every bit of the infrastructure of the human life in our society, with electronic devices embedded into everything.

No matter what applications are needed: new advances in materials, new developments on processes, new improvements on design tools, new architectures and new manufacturing techniques to overcome power dissipation, improve energy efficiency, or increase switching speed, new devices will be invented.

Words of Motivation for Women EDS Student Members to pursue Science and Engineering

Looking at my career in Science and Engineering, I wish I could translate the satisfaction in working in Science and Engineering. The constant learning and challenges that I faced made me learn and grow. I enjoyed all discussions, the profound knowledge of my colleagues and all the professionals I met.

For women in particular, engineering is a liberating profession because you can have a well-paid job and be independent. As an electrical engineer, there are many areas for specializations with the option to be multidisciplinary. The further you educate yourself the greater your job responsibility will be. You have the ability to improve yourself, and see how far you can advance in your career. As an engineer, you can change and influence our society.

Still there is some progress to make in gender diversity in Science and Engineering. In the USA, women make up less than 30% of the science and engineering college educated workforce. It is changing though. Before the pandemic started in 2020, some universities like USC and NC

State reported that their colleges of engineering enrollment included a larger percentage of women in their first year classes.

Leda Lunardi has been a professor since 2003 at the Electrical and Computer Engineering Department at North Carolina State University in Raleigh, NC. She holds a Ph.D. degree in electrical engineering from Cornell University in Ithaca, NY. Her research areas are in fabrication and modeling of electronic and optoelectronic devices, and microelectromechanical devices. Before joining

academia, she spent several years doing R&D at AT&T (then Bell Labs), and JDS Uniphase. In addition to her research, Dr. Lunardi has managed several NSF grants for STEM research and education to encourage women and underrepresented minority students to graduate in engineering and science and pursue graduate degrees. Dr. Lunardi has been a volunteer for more than three decades in professional organizations. She has served on numerous IEEE executive and technical committee conferences, editorial board of journals, and national and international governments' ad-hoc

committees for grants and projects reviews. Among her present activities, she is the chair for the 2021 IEEE Fellow Committee, chair of the 2021 IEEE Jun-ichi Nishizawa Medal Committee, and member of the 2021 IEEE Cleo Brunetti Award and the 2021 IEEE EDS Lester Eastman Award committees. She has authored and co-authored more than 100 publications and conference proceedings, been granted 5 patents, and given invited talks, plenary addresses, and short courses at conferences. She is an IEEE Fellow and co-shared the IEEE Photonics Society Engineering Achievement Award.

WOMEN IN ELECTRON DEVICES SOCIETY

MANIJEH RAZEGHI, DOCTORATE D'ÉTAT ES SCIENCES PHYSIQUES



Manijeh Razeghi

Professor Manijeh Razeghi is a pioneering leader in the area of III-V compound semiconductor materials and optoelectronic devices. For more

than 40 years she has been blazing a trail, developing new semiconductor materials and then using them to realize practical semiconductor optoelectronic devices including a wide range of light emitting diodes and lasers emitting at wavelengths from the terahertz, to the infrared, all the way to the deep ultraviolet. Prof. Razeghi performed her graduate studies at Université de Paris where she obtained her M.S. in Materials Science in 1976, her Ph.D in Solid State Physics in 1978, and her Docteur ès Sciences in Physics in 1980. From 1981 to 1992 she was a Senior Research Scientist and then Head of the Exploratory Materials Laboratory at Thomson-CSF (Orsay, France). There she pioneered

the scientific study, development, and implementation of most major modern epitaxial growth techniques. Prof. Razeghi is especially known as a pioneer in the development of the MOCVD (Metal-Organic Chemical Vapor Deposition) crystal growth technique for the growth of InP, GaInAs/InP and GaInAsP/InP based materials. This semiconductor growth technique is still the leading method for mass production of telecommunication optoelectronics. The key to successfully taking advantage of these materials is that the physical properties and quantum structures need to be truly dominated by the physics of the material and not by uncontrolled defects, dislocations and surface states. This is exactly where Razeghi's artistry for materials magic comes into play. She, for the first time, managed to produce the material quality with MOCVD that was good enough to observe the subtle quantum-physical effects predicted and calculated by theoreticians with such excitement.

She was able to use this material to investigate basic semiconductor

physics. This included the first quantum well heterostructures, the first superlattices, observation of the quantum Hall effect in this material system, the first demonstration of two-dimensional electron gas and two-dimensional hole gas in this material, and the first observation of room temperature excitons in GaInAs/InP superlattices. These contributed to the realization of a plethora of novel optoelectronic devices including lasers, optical waveguides, InP based Gunn diode for radar systems, a number of field effect transistors, InP-based photodiodes, and their monolithic integration. The capstone of these transformative discoveries was the realization of the important 1.3 and 1.55 μm laser diodes and photodetectors necessary to fuel the coming optical fiber telecommunication revolution.

Her scholarly work in France both generated and stimulated scientific research in this field for many years and was being relentlessly studied by world scientists from all over the Americas to Asia and Europe. This

early work leading up to, and including, the development of the first 1.3 and 1.55 μm laser diodes was documented in what has become one of the most seminal volumes ever written on MOCVD growth: "The MOCVD Challenge: Volume 1: A Survey of GaInAsP-InP for Photonic and Electronic Applications" (1989) Adam Hilger Publishing and Institute of Physics Publishing. This book received rave reviews, with Pierre Aigrain in the Foreword of this book writing: "*Manijeh Razeghi has been recognized all over the world for her ability to achieve astonishingly brilliant results with MOCVD technologies. Simply reading the book may not be quite enough for every engineer to do fully as well as she does. But it is a necessary step in that direction.*"

Then in 1991, Manijeh Razeghi left France and came to the United States, where she joined Northwestern University in Evanston, Illinois, from among a long list of major US institutions attempting to attract her. She was appointed as a Walter P. Murphy Chair Professor of Electrical Engineering and Computer Science. There, she founded the Center for Quantum Devices to continue her pioneering works, and devoted her research activities to studying III-V semiconductor materials for a wide range of quantum optoelectronic devices, including lasers, LEDs, photodetectors, and focal plane arrays, covering a very wide spectral band from the deep ultraviolet (down to a wavelength of $\sim 0.2 \mu\text{m}$) to the very long wavelength infrared ($\sim 32 \mu\text{m}$), and most recently all the way out into the terahertz (the elusive boundary between radio and photonic sources).

Within a few years of joining Northwestern University, Prof. Razeghi established herself anew and continued generating a whole impact on optoelectronics. Within three years, she had used her MOCVD skills to develop GaInAsP/GaAs semiconductor materials and designs for the first high-power aluminum-free diode

lasers emitting at 808 and 980 nm. There were existing AlGaAs designs at these wavelengths, but they were inherently unable to meet all the stringent requirements imposed by modern applications. The main failing was that aluminum oxidizes very easily, and during laser fabrication and high-power operation these oxides would form dark defects that absorbed power and destroyed the laser. The crucial technology was the development of the material and design to eliminate aluminum from the lasers ("aluminum-free"). The lasers that Manijeh Razeghi developed did not suffer from aluminum oxidation, and thus showed long-lifetime and very high output power. The availability of these lasers revolutionized the high power diode laser industry and their applications in the early 1990's, including diode pumped solid-state lasers and erbium doped optical fiber amplifiers for telecommunications. She also used the GaInAsP/GaAs material system to realize heterostructures and superlattices, demonstrating for the first time a two-dimensional electron gas in this system. This discovery led to the first heterojunction field effect transistor (HFET), modulation-doped FET (MODFET), two-dimensional electron gas FET (TEGFET) based on this material. She also started to use the GaInAs/InP material system to realize the first Quantum Well Infrared Photodetectors (QWIPs), the first multi spectral QWIPs, and the first focal plane array, based on this material system.

Based on the pioneering work leading up to and including this discovery, Prof. Razeghi released her second major book: "The MOCVD Challenge: Volume 2: A Survey of GaInAsP-GaAs for Photonic and Electronic Applications" (1995), Adam Hilger Publishing and Institute of Physics Publishing. The content of this volume, like Volume 1, is her own work and achievements for the MOCVD growth, characterization and fabrication of optoelectronic devices, including high-power aluminum-free lasers,

based on the GaAs-GaInAsP material system. Again this book received rave reviews with Jerome B. Cohen, the Dean of the McCormick School of Engineering at Northwestern, writing: "*This book is another example of her ability to do cutting-edge research and her desire to educate. It is a text of the fundamentals of semiconductor crystal growth and materials characterization leading into many of the important concepts in advanced device design and fabrication.*"

Since then Manijeh Razeghi has continued to demonstrate herself as a world renowned pioneer of III-V semiconductor materials research, quantum device physics, and photonic source technology. In every material system she has worked, she has not only developed the fundamental material, but has created a wide array of practical optoelectronic devices, many of which have required new physics—pushing the boundaries of what was thought possible using III-V semiconductors.

Speaking of new physics, Razeghi has also become a world leader in the pioneering development of Quantum Cascade Lasers (QCLs). QCLs are based on the same InP material system which she first developed while working in France. These devices are unipolar lasers that use intersubband transitions in quantum structures, the novel physical effects which have become possible with the growth of complex hetero-structures. They have made it possible to produce lasers emitting at nearly arbitrary wavelengths ranging from the mid-infrared all the way into the THz spectral regions. These spectral regions have been utilized in industry for many years for chemical/biological spectroscopy, but the old source technologies (like gas lasers and parametric oscillators) were bulky and far from mass manufacturability. The QCL technology is transformative in that QCLs are capable of ultrasensitive chemical/ biological detection but have the size, weight, and power of standard semiconductor laser

diodes. This has ushered in a new era of portable sensing. In addition, thanks to other beneficial properties of this wavelength range, there has been a significant development of these sources for free-space communications and as an infrared countermeasure to safeguard aircrafts from heat-seeking missiles.

Soon after QCLs had been introduced as only a cryogenically-cooled laboratory curiosity, Manijeh Razeghi drove the technology forward, maturing it into a commercial technology capable of room temperature, high power, continuous-wave operation over a wide range of wavelengths (3–12 μm). This included both the highest power and highest efficiency QCLs ever demonstrated. Other novel developments included two-dimensional photonic crystal distributed feedback (PC-DFB) sources for high power, single-frequency operation and multi-wavelength QCL arrays for wide wavelength coverage and rapid tunability.

Based on this pioneering quantum cascade laser work, Prof. Razeghi developed recently novel THz sources operating at room temperature. The terahertz is a novel region of the electromagnetic spectrum situated between the infrared and microwave. The unique properties of materials at these wavelengths allow new sensing applications that will revolutionize chemical/biological sensing and airport/border security, as well as applications for a non-destructive package inspection and astronomy. However, up until recently, the lack of convenient, compact diode laser sources has prevented realization of these applications. Razeghi developed the highest power terahertz lasers, and though still in development, she projects that mW-class, compact, room temperature THz sources will be available soon. Once realized the inherent mass production potential of semiconductor lasers will enable many new exciting applications. Finally, Razeghi played a crucial role in the development of the wide band-

gap AlInGaN semiconductor material system. This material system has revolutionized visible photonics sources with the recent introduction of blue LEDs and lasers. For the first time, it has become possible to have practical high-efficiency, long-lifetime, semiconductor-based, solid-state lighting. Razeghi played a role in the development of this material system for blue lasers, which have gone on to be used in next generation data storage. Her contributions have more recently focused on LEDs in the deep ultraviolet (<280 nm), leading to the first demonstration of LEDs at 280 nm or shorter. All wavelengths are at the heart of the next generation of fast and reliable chemical and biological agent sensors, and portable water purification systems.

In addition to her pioneering work on photonic source technology, Prof. Razeghi has also found time to pursue detectors and focal plane array imagers based upon these novel III-V compound semiconductor materials. She realized the first InAs and InGaAs Quantum Dot Infrared Photodetectors and focal plane arrays. In parallel, she pioneered in the area of QWIPs on InP for mid, long and very long wavelength spectral bands (4–19 μm) and demonstrated the first multi spectral QWIP on InP. Moreover, she developed the molecular beam epitaxy of InAs/GaSb type II quantum heterostructures, photodetectors and even focal plane arrays operating in the mid, long, and very long wavelength infrared spectral bands (3–32 μm). This pioneering work enabled the demonstration of the first infrared camera based on this material system. This technology is beginning to reshape the infrared sensing industry and it is possibly leading to a technological revolution, with a direct impact on medical applications, manufacturing thermal imaging, fire-fighting, pollution monitoring, surveillance, law enforcement, as well as dense applications. In the deep ultraviolet spectral band (200–400 nm), Razeghi's innovative ideas concern-

ing wide bandgap AlInGaN based semiconductors and their quantum structures led her to demonstrate high efficiency photodetectors, Geiger-mode avalanche photodiodes, and solar-blind focal plane arrays with world record characteristics.

In addition to her unparalleled contributions to basic and applied research related to photonic source technology, Prof. Razeghi has also demonstrated herself as an accomplished educator. She has created and manages the Graduate and Undergraduate Programs in Solid State Engineering (SSE) at Northwestern University. She directly oversees many assistant and research professors, and many adjunct professors. She regularly takes time out of her tireless research schedule to teach fundamental undergraduate courses and generate interest and motivate the next generation of scientists. She prepared several text books, including *Fundamentals of Solid State Engineering* (4th edition), *Technology of Quantum Devices*, *Introduction to Carbon Atom*, to name a few.

Manijeh Razeghi received the Doctorate d'état ES Sciences Physiques from the Université de Paris, France, in 1980. She was the Head of the Exploratory Materials Laboratory at Thomson-CSF (France) during the 80's where she developed and implemented modern metalorganic chemical vapor deposition (MOCVD), vapor phase epitaxy (VPE), molecular beam epitaxy (MBE), GasMBE, and MOMBE for entire compositional ranges of III-V compound semiconductors for spectrum range from deep UV to THz. Developing these tools was fundamental in enabling her to achieve high purity semiconductor crystals with a consistency and reliability that was often unmatched, thereby leading to new physics phenomena in InP, GaAs, GaSb, and AlN based semiconductors and quantum structures. She realized the first InP Quantum wells and Superlattices and demonstrated the marvels of quantum mechanics

in the low dimensional world. She joined Northwestern University, Evanston, IL, as a Walter P. Murphy Professor and Director of the Center for Quantum Devices in Fall 1991, where she created the undergraduate and graduate program in solid-state engineering. She has authored or co-authored more than 1000 papers, more than 34 book chapters, and 20 books, including the textbooks Technology of Quantum Devices (Springer Science Business Media, Inc., New York, NY U.S.A. 2010) and Fundamentals of Solid State Engineering, 4th Edition (Springer Science Business

Media, Inc., New York, NY U.S.A. 2018). Two of her books, MOCVD Challenge Vol. 1 (IOP Publishing Ltd., Bristol, U.K., 1989) and MOCVD Challenge Vol. 2 (IOP Publishing Ltd., Bristol, U.K., 1995), discuss some of her pioneering work in InP-GaInAsP and GaAs-GaInAsP based systems. The MOCVD Challenge, 2nd Edition (Taylor & Francis/CRC Press, 2010) represents the combined updated version of Volumes 1 and 2. She holds more than 60 U.S. patents and gave more than 1000 invited and plenary talks. Her current research interest is in nanoscale optoelectronic quantum

devices. Dr. Razeghi is a Fellow of MRS, IOP, IEEE, APS, SPIE, OSA, Fellow and Life Member of Society of Women Engineers (SWE), Fellow of the International Engineering Consortium (IEC). She received the IBM Europe Science and Technology Prize in 1987, the Achievement Award from the SWE in 1995, the R.F. Bunshah Award in 2004, IBM Faculty Award 2013, the Jan Czocharlski Gold Medal in 2016, the 2018 Benjamin Franklin Medal in Electrical Engineering, and many best paper awards. She is an elected life-Fellow of SWE, IEEE, and MRS.

MERCEDES ARRUIZ—WEBINAR “SELF-EMPOWERMENT” A JOINT WIE AND YP EVENT

By MIKE SCHWARZ

The Affinity Group Women in Engineering (WiE) and Young Professionals of the IEEE Germany Section organized a webinar with Mercedes Arruiz. The WebEx seminar took place on October 13, 2020.

Mercedes is from Argentina. She is an entrepreneur woman always searching how to grow during crises and who developed as an empowerment coach after years of personal development.

She was an IEEE member while studying biomedical engineering in

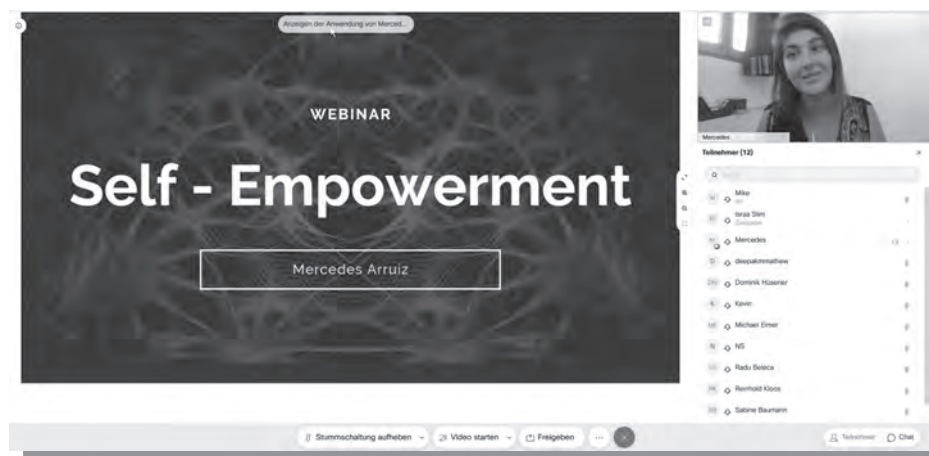
the San Juan National University, leading groups not only in the student branch, but also in Region 9, Student Professional Awareness Activities (SPAA) and RoadShow.

For 5 years she delivered conferences about leadership, teamwork and motivation at Nationals and Regional Meetings and now she is sharing webinars with students from R9 about conscious leadership.

The webinar discussion had the title: “Self-Empowerment.” The webi-

nar was attended by 16 participants from different countries and had a fruitful exchange of experiences on how to self empower. Especially, points like “Inner peace”, “Self truth”, “Awareness”, and many more were addressed and discussed. It was a pleasure to share the thoughts. The audience enjoyed the webinar and gave a huge “thank you” to Mercedes and the organizers.

More webinars and joint events of WiE and the YPs are very welcome!!!



WebEx webinar organized by WiE and YP Germany - Mercedes Arruiz and participants

EDS YOUNG PROFESSIONALS

CAN BAYRAM: REFLECTIONS FROM AN EDS YOUNG PROFESSIONAL



The Young Professional guest in this issue of the Newsletter is Can Bayram, Electron Devices Society's 2014 Early Career Award winner

and a faculty member at University of Illinois at Urbana-Champaign. His perceptions about EDS and views regarding professional development and career growth are reflected in the discussion. Here are the excerpts of the interview with Can Bayram made by Manoj Saxena, the Newsletter Associate Editor-in-Chief.

Manoj Saxena: What was the specific temptation, if any, which made you join IEEE EDS, the premier global society in the field of electron device engineering, at first?

Can Bayram: I joined EDS because my mentors have been EDS members. EDS being a major influencer in my research field (through its highly respected conferences and impactful journals) is the reason I have been a member since then.

MS: You won the prestigious EDS Early Career Award, an honor most of the young professionals aspire. How do you consider this recognition and what are your plans to further develop your research career?

CB: I am honored to have been recognized as the 2014 Early Career Award Winner. Early Career Awards are essential mechanisms for encouraging young professionals to conduct impactful research. This recognition not only celebrates our impact but also brings a spotlight to our future

work. After almost a decade of research and development, we are now exploring commercialization of our technologies, which could bring our awarded research into our daily lives.

MS: As a Young Professional, how do you position your interest in your own field with the activities and services you perform as an EDS member/volunteer?

CB: EDS membership benefits allow me to gain discounted conference registration, unique access to valuable and timely content (e.g. the newsletters and webinars), and networking. In reciprocity, I volunteer as the Chair of the IEEE EDS Optoelectronics Technical Committee and as an Editor in the IEEE Transactions on Electron Devices. As a service, I am giving, what EDS provides me (e.g. time and funds savings, technical and professional peer expertise), back to the EDS.

MS: What are your thoughts about the EDS membership and its paybacks? Whether the EDS membership benefited you at any time in your career growth? If so, how?

CB: I am a seasoned IEEE member for the last 17 years, and an EDS member during the last 13 years. I have been a student, young professional, regular, and, now, senior member. EDS is one of the few societies where each career level can find valuable technical, educational, and networking content. Given its large member size and diverse geographical and technical member database, it also provides many career growth and leadership opportunities in various forms such as organizing

conferences, topical meetings, and special issues.

MS: As an YP, how do you consider the EDS Society as a whole and what are the changes or developments you would like to see in evolving this professional body as a group devoted to humanity and its causes?

CB: Today, internet connectivity is rapidly becoming a basic utility for the world's population. Digitization of valuable EDS content will enable timely and scaled access, enabling opportunity for members to grow through online learning, remote employment, and networking. Increased engagement through social platforms, encouragement of regional activities, and traveling speaker events might help members and the public stay up to date with the EDS and its impact.

MS: What are your suggestions and recommendations for those young professionals who may aspire to join EDS?

CB: EDS will inspire you for what you can accomplish. Societies such as EDS offer many platforms for providing young professionals valuable insights on career options. Engaging early is not a requirement, but certainly has its benefits. I encourage young professionals to focus on their careers and let their work inspire many.

MS: As an EDS Young Professional and a young researcher in the field, how do you consider the prospects of scientific research in this field for the progress of Humanity as a whole?

CB: The NAE President John Anderson once said, “*Science is about discovery, engineering is about creating*”. Since the discovery of the electron in 1897 by Thomson, we have been exploring its unique properties and creating new methods to tailor them. The NAE’s Great Engineering Achievements of the 20th Century highlight how much we have progressed. Still, there is much to discover, and many engineering challenges to overcome. The NAE’s Grand Challenges for Engineering specifically cite making solar energy economical, enhancing virtual reality, reverse-engineering the brain, and developing the tools of scientific discovery. These specific challenges and others can only be overcome through scientists and engineers, working together.

Can Bayram is an Associate Professor in the Department of Electrical and Computer Engineering, a resident faculty at the Nick Holonyak, Jr Micro and Nanotechnology Laboratory, and an affiliate faculty of the Carle Illinois College of Medicine of University of Illinois at Urbana-Champaign, IL, USA. He is an expert in III-V materials and photonic and electronic devices. He has performed more than 3,000+ epitaxial growths with metalorganic chemical vapor deposition systems and fabricated detectors, light emitting diodes, solar cells, resonant tunneling diodes, and transistors in class 100 and 1000 cleanrooms totaling 20,000+ hrs equipment usage. His current research interests lie in the intersection of novel III-V materials, hetero-structures, and photonic

and electronic devices. Particularly, his research group explores III-V materials and novel devices, hetero-integration of III-Vs on unconventional platforms such as graphene, silicon and diamond, heat transport across/through semiconductors, efficiency drop mechanisms and remedies in AlInGaN emitters, and ultra-fast THz photonics/electronics. Prof. Bayram’s work has been recognized widely. He is the recipient of the International Union of Pure and Applied Physics Young Scientist Prize in Optics, IEEE Nanotechnology Council Early Career Award, an NSF CAREER Award, a CS Mantech Best Paper Award, an AFOSR Young Investigator Award, the IEEE Electron Devices Society Early Career Award, and many Best Paper Awards.

SHIMENG YU: REFLECTIONS FROM AN EDS YOUNG PROFESSIONAL



Prof. Shimeng Yu
Georgia Institute of
Technology, Atlanta,
Georgia, USA 30332

The Young Professional guest in this issue of the Newsletter is Shimeng Yu, Electron Devices Society’s 2017 Early Career Award winner and a faculty member at Georgia Institute of Technology,

Atlanta. His perceptions about EDS and views regarding professional development and career growth are reflected in the discussion. Here are the excerpts of the interview with Shimeng Yu made by Manoj Saxena, the Newsletter Associate Editor-in-Chief

Manoj Saxena: What was the specific temptation, if any, which made you join EDS which is the largest professional organization in the globe, at first?

Shimeng Yu: I joined EDS as a student member in 2010 when I was pur-

suing the master’s degree at Stanford University. In that year, I had opportunities to present my research papers on resistive random-access-memory (RRAM) in the EDS sponsored conferences such as IEEE International Memory Workshop (IMW) and IEEE International Electron Devices Meeting (IEDM). Those were my initial experiences attending technical conferences, interacting with peer students, and learning from senior professionals. I was grateful to receive the EDS Masters Student Fellowship in 2010. This student fellowship deeply motivated me to further pursue the research in the semiconductor devices. Later I was fortunate to receive the EDS PhD Student Fellowship in 2012. My EDS journey started as a student member in those years.

MS: You won the prestigious EDS Early Career Award, an honor most of the young professionals aspire. How do you consider this recogni-

tion and what are your plans to further develop your research career?

SY: It was my great honor to receive the prestigious EDS Early Career Award in 2017, 4 years after I started my own research group. I regarded it as an appreciation by the community for my technical achievements as a junior faculty member. At that time, I had been fully engaged with EDS activities with dozens of publications in IEDM, IEEE Electron Device Letters and IEEE Transactions on Electron Devices. Meanwhile, I have extended my research from devices to circuits and systems as well. I believe a holistic approach to solve the fundamental challenges in the technology scaling is critical, therefore a design-technology co-optimization or even system-technology co-optimization is highly demanding in the future.

MS: As a Young Professional, how do you position your interest in your own field with the activities

and services you perform as an EDS member/volunteer?

SY: My volunteer roles in EDS include reviewers for EDS journals, and technical program committee member for EDS sponsored conferences such as IEDM, Symposium on VLSI technology and IEEE Electron Devices Technology and Manufacturing (EDTM). By serving the community, I could learn the latest research trends in the field and also I have an opportunity to shape the future research directions (by selecting/promoting good papers). I am glad to see many ideas that my research group pioneered have become popular among EDS colleagues later, including using RRAM for physical unclonable function and customizing 3D NAND for compute-in-memory. Furthermore, our open-source model and simulator (i.e. RRAM compact model and NeuroSim benchmark framework) are being widely used in both academia and industry today.

MS: What are your thoughts about the EDS membership and its paybacks? Whether the EDS membership benefited you at any time in your career growth? If so, how?

SY: The EDS membership is rewarding, and I have benefited a lot from the EDS Masters and PhD Fellowships as well as Early Career Award. It not only gives us the opportunities to earn these awards, but also provides us the access to the online educational resources. Recently, EDS has promoted a series of webinars to help a wider participation in virtual lectures during the pandemic, and I gave a presentation in one of the webinars about the recent progress on compute-in-memory technologies. Also, I enjoyed the new initiative that EDS launched on the podcast interview, and the first interview was with Prof. Chenming Hu, a well-respected pioneer in our field, who gave many useful advices to young professionals.

MS: As an YP, how do you consider the ED Society as a whole and what are the changes or developments

you would like to see in evolving this professional body as a group devoted to humanity and its causes?

SY: Frankly speaking, I see there is a declining interest among the new generations of students towards semiconductor devices (or in general hardware), simply because of the blooming in machine learning (or in general software). But we have to keep in mind that the technological foundation of new applications powered by AI today is still the integrated circuits and semiconductor devices. Also I would like to point out that many traditional Internet (or system) companies (Google, Facebook, Amazon, Microsoft, and even Tesla) are developing their own silicon program. My suggestion for our EDS educators and researchers is to embrace the wave of AI/machine learning and train the students with interdisciplinary skills. The opportunities are two-folded: 1) Devices for AI, meaning developing new device technologies that suit AI hardware acceleration (e.g. new multibit memories); 2) AI for devices, meaning applying AI techniques to improve device technologies optimization (e.g. materials screening, manufacturing process control).

MS: What are your suggestions and recommendations for those young professionals who may aspire to join EDS?

SY: Young professionals including graduate students and even undergraduate students are all welcome to join EDS and get the benefits of the educational resources as aforementioned. Attending premier EDS conferences, and subscribing EDS flagship journals are the first steps to success.

MS: As an EDS Young Professional and a young researcher in the field, how do you consider the prospects of scientific research in this field for the progress of Humanity as a whole?

SY: I feel that semiconductor technologies can do more especially in the context of the pandemic today.

For example, fast genomic sequencing requires domain-specific hardware accelerators for processing TB data. To analyze the virus from raw sequenced data to biologically interpretable output is critical to understand how COVID-19 has mutated and what that means for its spread and eventual treatment.

Shimeng Yu is an associate professor of electrical and computer engineering at the Georgia Institute of Technology. He received the B.S. degree in microelectronics from Peking University in 2009, and the M.S. degree and Ph.D. degree in electrical engineering from Stanford University in 2011 and 2013, respectively. From 2013 to 2018, he was an assistant professor at Arizona State University. Prof. Yu's research interests are the semiconductor devices and integrated circuits for energy-efficient computing systems. His expertise is on the emerging non-volatile memories (e.g., RRAM, ferroelectrics) for applications such as deep learning accelerators, in-memory computing, 3D integration, and hardware security. Among Prof. Yu's honors, he was a recipient of NSF Faculty Early Career Award in 2016, IEEE Electron Devices Society (EDS) Early Career Award in 2017, ACM Special Interests Group on Design Automation (SIGDA) Outstanding New Faculty Award in 2018, Semiconductor Research Corporation (SRC) Young Faculty Award in 2019, ACM/IEEE Design Automation Conference (DAC) Under-40 Innovators Award in 2020, and IEEE Circuits and Systems Society (CASS) Distinguished Lecturer for 2021-2022, etc. Prof. Yu served or is serving many premier conferences as technical program committee member, including IEEE International Electron Devices Meeting (IEDM), IEEE Symposium on VLSI Technology, ACM/IEEE Design Automation Conference (DAC), ACM/IEEE Design, Automation & Test in Europe (DATE), ACM/IEEE International Conference on Computer-Aided-Design (ICCAD), etc. He is a senior member of the IEEE. Lab website: <https://shimeng.ece.gatech.edu/>

IEEE YP GERMANY—ELECTIONS

The IEEE Young Professionals Germany affinity group has elected new ExCom members for the term 2021/2022. An exciting new leadership team has been built to establish YP activities in Germany. Two members of the former ExCom enable smooth transition. Past ExCom leadership team succeeded in their term from mid 2019 to 2020 with 31 events, including

- DL on Autonomous Driving Testing & Validation,
- Carlos Soares (NASA Jet Propulsion Laboratory) lecture on JPL Missions,
- IEEEYP Germany AG company visit at Bosch (virtual),
- Mercedes Arruiz Webinar “How do we properly manage our working and living situation after COVID-19” a Joint WIE & YP Event,
- IEEE MQ “Non-Conventional Devices and Technologies”,
- Symposium on Schottky barrier MOS devices.

The new ExCom consists of:

- Chair—Ahmed Hussein
- Vice Chair—Ashan Sheikh
- Treasurer—Giulio Sistilli
- MAG Lead—Ertug Olcay
- Secretary—Prithvi Thyagarajan
- Activities Lead—Marc Vizcarro i Carretero

- Webmaster—Alan Blumenstein

They established a healthy leadership team, well organized and highly motivated to be part of the IEEE community. Joint events and close collaboration with WIE were established. Furthermore, the new ExCom chair, Ahmed Hussein welcomes the past ExCom members to participate in the regular meetings and contribute with innovative ideas as in the past.

Further information is available at <https://www.ieee.de/groups-programs/young-professionals.html>

Here are some brief bios on the new ExCom members:

Ahmed Hussein



Dr.-Ing. Ahmed Hussein received the BSc Degree in Mechatronics Engineering from the German University in Cairo (GUC), Egypt, in June 2012. In May 2013 he received the MSc Degree in Mechatronics Engineering from the German University in Cairo (GUC), Berlin campus, Germany, working on optimization of multiple robot systems cooperation. In September 2018, he received the PhD Degree in Electrical Engineering, Electronics and Automation from Universidad Carlos III de Madrid (UC3M), Spain. During the doctoral degree period, he worked with the Intelligent Systems Lab (LSI) research group, where he was one of the team leaders of the Intelligent Campus Automobile (iCab) project, working on the development and implementation of localization, mapping, planning, control, communication and cooperative driving techniques for multiple self-driving vehicles. Currently he is an Autonomous Driving Concept Developer at IAV GmbH in Berlin, Germany.

Ahsan Qamer Sheikh



Ahsan Qamer Sheikh received his Bachelor's in engineering from NED University of Engineering & Technology, Karachi, Pakistan in 2017. He started to work with a U.S. based consultant firm Pinnacle. In 2018, his interest in research brought him to Germany to pursue his Master's degree in Infrastructure Planning at University of Stuttgart. His research interest focuses towards signal processing and use of artificial intelligence for

railway transportation. Sheikh has also served as research assistant at University of Stuttgart. He has been associated with IEEE since past six years with focus towards students activities, membership drives, humanitarian projects and goal-oriented workshops. He has also served as Section Student Representative (SSR) of IEEE Karachi Section in 2016. Currently, he is enrolled in the class of 2020 of IEEE Volunteer Leadership Training program.

Giulio Sistilli



Giulio is an Engineer expert in Computers, Telecommunication and Ground stations. Through his career he had the opportunity to work for important players in the telecommunication sector like Ericsson and Huawei, and later in space agency DLR. He pursued a Master in Business Administration leading him to be a technical director. Giulio has international experience having worked in different countries and in different positions. He is Senior Member of IEEE and MENSA member.

Ertug Olcay



Ertug Olcay received the B.Sc. degree in Automotive and Combustion Engine Technology and M.Sc. degree in Mechatronics and Information Technology from Technical University of Munich, Germany, in 2013 and in 2016, respectively. From 2016 to 2020, he worked as a research assistant at the Chair of Automatic Control, Technical University of Munich towards his Ph.D. degree. He spent some time at the University of Texas in Austin as a visiting

researcher. In 2020, he became a Post-Doctoral researcher at the Chair of Agrimechatronics, Technical University of Munich. Dr. Olcay is an IEEE member and served as reviewer for IEEE Transactions on Systems, Man and Cybernetics, and for IEEE Transactions on Neural Networks and Learning Systems. His current research interests are AI-based predictive maintenance for agricultural machinery, guidance and navigation of agricultural vehicles. His hobbies are reading books, jogging and cycling.

Prithvi Thyagarajan



Prithvi Laguduvan Thyagarajan received in 2016 her Bachelor's in Engineering from Visvesvaraya Technological University, Bangalore, India. She worked as a research assistant for the Center for airborne systems (2016-2017) in the field of radar signal processing. With a keen interest in the field, she went on to pursue her Master's in 2017 in Signals and Systems at the Technical University of Delft. She graduated in 2019 with a thesis focusing on exploring the design and performance analysis of STEREOID which is one of the candidates of ESA's Earth Explorer 10 mission. Currently, she is an early-stage researcher in the Marie Skłodowska-Curie Innovative Training Network Project MENLAOSNT (Multimodal Environmental Exploration Systems Novel technologies) in the field of Tomographic Synthetic Aperture Radar Reconstruction. Her research interests include Synthetic Aperture Radars, Array Processing,

Radar Imaging, Radar Polarimetry and Remote Sensing.

Marc Vizcarro i Carretero



Marc Vizcarro i Carretero is a young radar engineer actively involved in the European Defense industry. He holds a BSc and MSc (cum laude) in Electrical Engineering from the Polytechnic university of Catalonia in Barcelona and TU Delft respectively. Marc possesses a broad range of international professional experience from companies such as in Indra Sistemas (Madrid, Spain), Thales Nederland (Delft, the Netherlands) and Fraunhofer FHR (Bonn, Germany). In them he was mainly involved in radar development activities for both defense and civil applications such as: validation of SSR and IFF systems, signal processing for drone detection and polarimetric phased array design for weather radar.

In October 2019, Marc became an antenna design engineer at HENSOLDT Sensors (Ulm, Germany) working in the Active & Passive Antennas department. In this new role he is mainly involved in state-of-the-art Active Electronically Scanned Array (AESA) conceptual design, development and validation activities for military sensors (namely radar and electronic warfare).

Alan Blumenstein

Alan Blumenstein made his Bachelor's degree in the Universidad Nacional De Asuncion, Paraguay in the area of Mechatronics and his



Master's degree in Universidad de Oviedo and the Karlsruhe University of Applied Sciences in the area of Mechatronics and Micro-Mechanics Systems.

During his Bachelor's he was involved in the creation of the first student branch of Paraguay at Universidad Nacional de Asuncion. He was the chapter vice president and president. He helped with the organization of the National Branch reunion of Argentina and the third National Sumo Robot competition. As the chapter President he represented the students of mechatronics and also as the career coordinator. Besides, he was also an Assistant Professor in several subjects. After that he got involved in the creation of the Paraguayan section. He was also in charge of the awards in the section and also in charge of the first ever National Robotic Competition and also of the first edition of the National Congress of Paraguay, Aranducon. During his Master's degree he was shortly involved with the student branch of Universidad de Oviedo.

As a professional Alan was in charge of the robotic laboratory of the Universidad Nacional de Asuncion, and started his own company Deda-lo that worked mostly in the area of non-conventional marketing. Today Alan works at Swarco Traffic Systems as an embedded software developer. He is a passionate in robotics and astrophysics, he enjoys learning about new technologies such as quantum computers and artificial intelligence.

~Mike Schwarz, Editor



Call for Nominations – EDS Student Fellowships for 2021

The IEEE Electron Devices Society invites nominations for the 2021 PhD, Masters and Undergraduate Student Fellowships. These annual awards are given to promote, recognize, and support graduate, masters, and undergraduate level study and research within the EDS field of interest. For both Masters and PhD, it is expected that at least one fellowship will be awarded to a student in each of the following geographical regions: Americas, Europe/Middle East/Africa, and Asia/Pacific. For the Undergraduate, it is expected that at least one fellowship to each eligible student in each of the IEEE geographical Regions 8, 9, and 10 and two fellowships in Regions 1-7 not exceeding one from Region 7.

Please visit the EDS website links below to access information about these Fellowships.

EDS Masters Student Fellowship

Prize: US \$2,000 and an award plaque

Submission Deadline: May 15, 2021

EDS PhD Student Fellowship

Prize: US \$5,000 and travel funds to attend the IEDM for presentation of an award plaque

Submission Deadline: May 15, 2021

EDS Undergraduate Student Scholarship

Prize: US \$1,000 and an award plaque

Submission Deadline: May 15, 2021

Please help to promote the EDS Student Fellowships by distributing this information to your colleagues and students. If you have any questions or need further information, please do not hesitate to contact Stacy Lehotzky by email at s.lehotzky@ieee.org. Thank you!

CHAPTER NEWS

ED KANPUR CHAPTER—2020 EDS CHAPTER OF THE YEAR AWARD WINNER

By AMIT VERMA, PAST CHAPTER CHAIR AND YOGESH S. CHAUHAN, CURRENT CHAPTER CHAIR

Our chapter is located in the city of Kanpur in Uttar Pradesh, India, A city with a population of over 3 Million, located on the banks of the Ganges River. We are located inside the green campus of Indian Institute of Technology Kanpur (better known as IIT Kanpur). This EDS chapter was established in 2016. The motivation for starting the chapter came after we attended several EDS meetings especially with IEDM. Senior EDS colleagues such as Renuka Jindal, Samar Saha and M K Radhakrishnan, etc. motivated us to start the chapter once we had sufficient number of active EDS members which consisted of faculty members and students. Founding chair Y. S. Chauhan worked hard to make it active and organized several workshops, short-courses and MQs. Within four years of starting the chapter, we were thrilled to hear that our chapter was selected for the Chapter of the Year Award. It

is also worth mentioning that two of the former EDS members—Pragya Kushwaha and Harshit Agarwal, from our chapter were awarded IEEE EDS Early Career Awards in 2019 and 2020, respectively, and one member (Nilesh Pandey) was awarded IEEE EDS Master Fellowship in 2019.

The regular activities of the chapter include mini-colloquia and nanoelectronics workshops in the subsequent years. They are quite popular. Attendance of some of these events was going up to 200 including both students and faculty members from universities and institutes all over India. Additionally, we also regularly host EDS Distinguished Lecturers and other speakers for technical seminars and interaction. Last year brought unprecedented challenges with campuses shutting down, students sent back to their homes, forcing classes and meet-

ings to be held online. IEEE activities in our chapter including planned mini-colloquia in summer 2020 were also disrupted and cancelled. As the saying goes, "In every adversity, there is an opportunity," Covid times also have bought the opportunity of hosting the speakers online. We actively contacted EDS Distinguished Lecturers and other researchers with matching research themes for giving online seminars and many of them kindly agreed. Online seminars are convenient for the speakers as they don't have to take a break from their teaching/research/administrative responsibilities and travel over long distances. At the same time, chapters can host many more speakers with limited funds and members can join the seminars no matter where they are located. Even after this pandemic ends, online activities and seminars will continue to be a big part of our activities.

SPOTLIGHT ON THE ED SPAIN CHAPTER'S ACTIVITIES AND AWARDS

By BENJAMIN INIGUEZ

The ED Spain Chapter, with more than 40 members, has been one of the most active ED chapters worldwide in the last years. As a result of the numerous activities it organized, and its efforts to attract new members, the ED Spain Chapter obtained the ED Chapter of the Year Award at worldwide level in 2012, and the SRC EDS Region 8 Chapter of the Year Award in 2016. Furthermore, it demonstrated to be one of the most active IEEE Chapters in

the Spain Section, which led it to obtain the Best IEEE Spain Chapter in 2013.

Some activities organized by the ED Spain Chapter became periodical. The Spanish Conference on Electron Devices (CDE), held every two years in Spanish cities since 1997, is co-organized by the Chapter. It is the major Electron Device event in Spain at national level, being also open to researchers worldwide since the working language is English. Besides,

an EDS Mini-Colloquium is held as a registration-free satellite event of CDE. Held one day prior to CDE, this MQ uses to include 4 talks conducted by EDS Distinguished Lecturers (DLs) working in other countries, as well as additional presentations given by the DLs affiliated with Spanish institutions. This MQ, usually attended by many PhD students in Spain, is also a tool to explain to the public the structure and goals of EDS, and promote EDS membership. The next edition

of CDE and its satellite MQ will take place on June 9–11 2021 in Seville.

Another important periodical activity is the Annual Graduate Student Meeting on Electronic Engineering. Held in Tarragona in June or July since 2003, it consists of several plenary talks delivered by top researchers in different areas of Electronic Engineering (with emphasis on Electron Devices and Sensors) and PhD student presentations in oral or poster form. This event offers PhD students an opportunity to give some of their first oral/poster presentations of their research results, and to interact among them as well as with the invited top researchers. This event is organized by the University Rovira i Virgili (URV) and the ED Spain Chapter, which uses to invite at least one EDS Distinguished Lecturer, who introduces EDS to the attendees (mostly PhD activities) and encourages EDS membership. In 2020 the Electronic Engineering had to take place

virtually, but hopefully it will be held as an in-person (fully or partially) event in 2021.

The ED Spain Chapter participated in the organization of the Spring EDS Governance Meeting, held in Tarragona on May 25–26 2019. A Mini-Colloquium with 6 DLs was held one day before that Governance Meeting.

The Chapter also has a large experience in training events. In particular, it created and organized two editions of a Training Course on Compact Modeling, and sponsored one edition of the SINANO Modeling Summer School (September 25–28 2018), with a MQ associated to it.

Besides, every year, the ED Spain Chapter organizes DL talks and usually at least one MQ not related to bigger events. Due to the pandemic, during 2020, all events had to be virtual, but the Chapter managed to sponsor two virtual thematic MQs: one about Photonics and Photovol-

taics (with 3 DLs, July 31), and one about Compact Device Modeling (with 6 DLs, December 18). We hope that in-person events organized by the Chapter will restart around the middle of 2021.

The ED Spain Chapter uses social media for internal communication. In particular, there is one Whatsapp group for the members of the Chapter, and one more for the members of the Executive Board. There is also a Messenger Group for the ED Spain Chapter.

Since 2019, Prof Benjamin Iñiguez (University Rovira i Virgili, Tarragona) is the Chair of the ED Spain Chapter. The other members of the Executive Board of this Chapter are: Vice-Chair Lluís F. Marsal (University Rovira i Virgili), Secretary Rodrigo Picos (University of the Balearic Islands), Vice-Secretary Tomás González (University of Salamanca) and Treasurer Enrique Miranda (Autonomous University of Barcelona).

BRINGING STEM TO LIFE (AMAZING GRAPHITE)—TRAIN THE TRAINERS ONLINE SESSION

By: ALIZA AINI MD RALIB, ROSMINAZUIN AB RAHIM, SHARIFAH FATMADIANA WAN MUHAMMAD HATTA AND MAIZATUL ZOLKAPLI

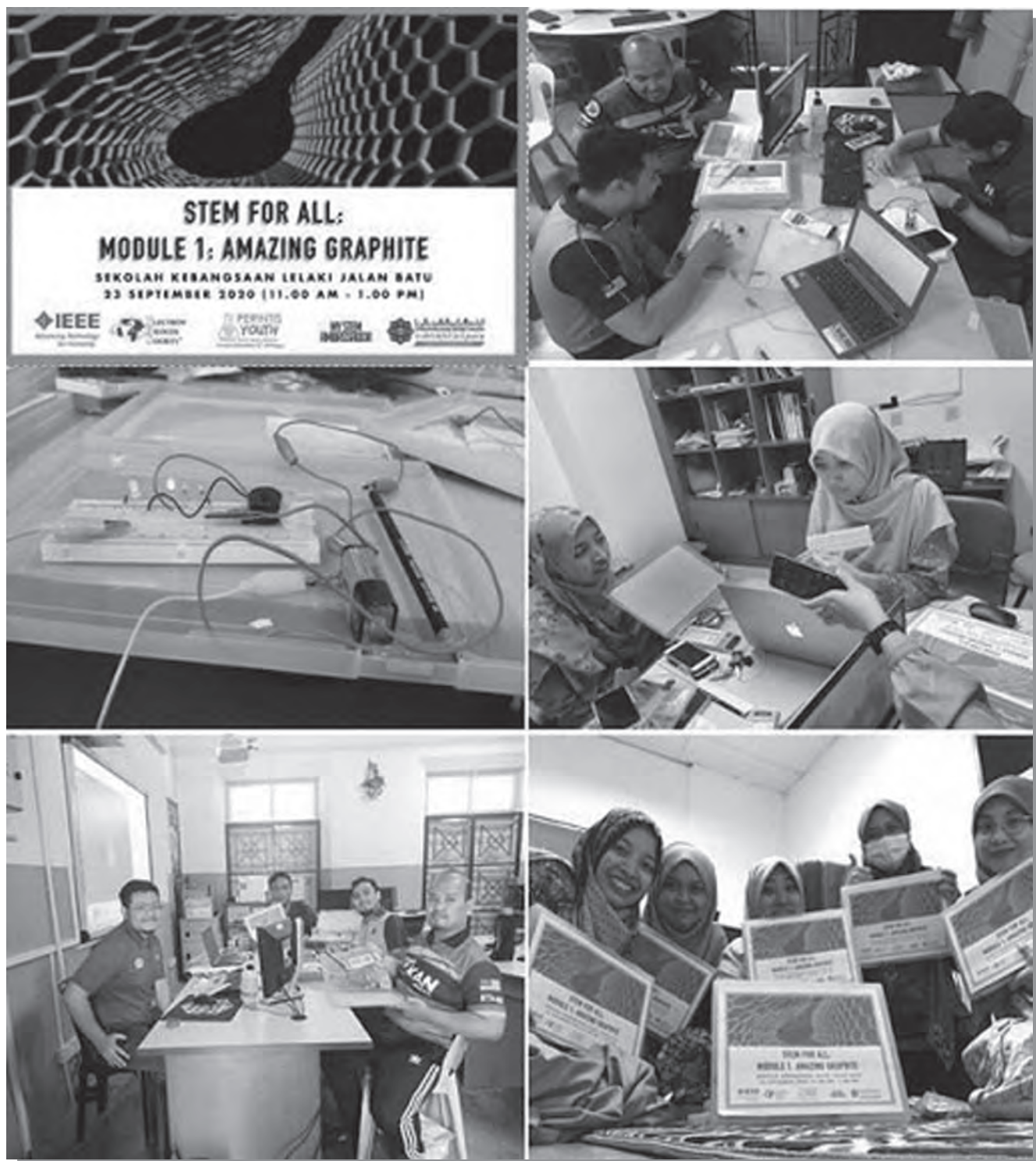
In the spirit of promoting the advancement of technology to the schoolteachers and students, IEEE Electron Devices Society (EDS) Malaysia Chapter organized a community service and educational event, Bringing STEM to life (Amazing Graphite) with the sponsorship from IEEE Region 10 EA Fund and IEEE Malaysia Section. In the spirit of leveraging technology for a better tomorrow, the event aimed to expose the world of electronics to the children at Sekolah Kebangsaan Jalan Batu through Science, Technology, Engineering and Mathematics (STEM) learning using Elenco Snap Circuits Kits provided by the IEEE EDS-ETC Program. Lo-

cated in the city of Kuala Lumpur, Sekolah Kebangsaan Lelaki Jalan Batu is among the underprivileged schools selected under 'Sekolahku Universitiku (MySchool MyUniversity)' program. Due to the COVID-19 pandemic situation, the session was conducted online on 23 September 2020. Two trainers (IEEE EDS members) from Kulliyyah (Faculty) of Engineering, International Islamic University Malaysia and six teachers from Sekolah Kebangsaan Lelaki Jalan Batu participated in the session.

The session began with the introduction on the basic concept of conductivity with graphite and nanotechnology. The hands-on session focused on the concept of series and

parallel circuits using graphite pencils. The module was designed by referring to IEEE resources such as TryEngineering and Teacher-in-Service (TISP) Lesson Plans on graphite modules. The session certainly helped the children to experience the real world application of electronics and boost their interests in electronics. Furthermore, we believe that the teachers will disseminate the knowledge to the students to spark their interest in STEM by exposing them to the various applications of graphite. In addition, the engagement of IEEE members with the local community will be cultivated through this program.

~Sharma Rao Balakrishnan, Editor



Train the trainers - participants were Science Teachers from Sekolah Kebangsaan Lelaki Jalan Batu while the trainers were IEEE EDS member and lecturers from International Islamic University Malaysia

REGIONAL NEWS

USA, CANADA & LATIN AMERICA (REGIONS 1-6, 7 & 9)

3rd IBM IEEE CAS/EDS AI Compute Symposium (AICS'2020)

—by Rajiv Joshi, Arvind Kumar,
Matt Ziegler, Xin Zhang, and
Krishnan Kailas

The 3rd IBM IEEE CAS/EDS AI Compute Symposium, known as (AICS'20), was held over two days on 21–22 October 2020. The symposium was also an initiative supported by IBM Academy of Technology (<https://www.ibm.com/blogs/academy-of-technology/>). Dr. Joshi has been the main interface for CAS and EDS for organizing this successful event. The symposium was very well attended and received positive responses from the audience. It was organized as a virtual symposium for the first time due to the pandemic situation across the globe. More than 650 folks from academia, industry, research organizations including 380 IEEE members registered from over 45 countries. The salient features of the symposium included high quality keynote and invited talks, over 40 student posters, best paper poster awards, and excellent panel discussions. **The theme of the symposium was “From Atoms to Applications.”**

Keynote talks were delivered by **Dr. Mukesh V. Khare** (VP IBM Research), **Prof. Rob Knight** (Director and Professor at UC San Diego) and **Pamela Norton** (CEO of Borsetta).

Dr. Mukesh V. Khare presented an exciting vision of “*What’s Next in AI: Our Vision for the Future of AI Hardware.*” The talk highlighted the theme that we have reached a turning point in computation. As the global pandemic and warming climate present

challenges, the next generation of computers will define and respond to these and future crises. The IBM Research AI Hardware Center is focusing on the development of a new, scalable computing platform that uses the power of AI and the flexibility of the hybrid cloud to create a virtually limitless pool of computing power and capabilities that can be applied to the challenges we face.

Prof. Rob Knight followed up with a keynote “*Using AI to Understand the Human Microbiome and its Role in COVID-19.*” The human microbiome harbors an immensely complicated collection of genes and cells that outnumber “our” own and are redefining the concept of what it means to be human. Grappling with data of this complexity requires artificial intelligence techniques. Highlighting the collaboration between IBM and UCSD in the Artificial Intelligence for Healthy Living, he showed applications of cutting-edge techniques to understand the microbiome, discovering how it changes with age and disease to recommend modifications to diet, lifestyle and medications that can increase health throughout the lifespan. Of particular interest during today’s unprecedented COVID-19 pandemic are studies regarding how the microbiome affects those who are the most impacted by SARS-CoV-2, including the elderly and those with specific microbiome-lined comorbidities. These techniques will be generally applicable to other illnesses and will help us bridge the previously disparate fields of infectious and chronic disease.

Following Prof. Knight’s keynote, **Prof. Deji Akinwande** (Endowed Professor Electrical and Computer Engineering University of Texas, Austin) described how atomic level research can expand the applications of AI. His talk entitled “*Atomic Memory: From Single Defects to Analog Switches*

and Computing,” focused on the discovery of the memory effect in 2D atomically-thin nanomaterials, providing a greater scientific understanding and advancements for engineering applications. Non-volatile memory devices based on 2D materials are an application of defects and is a rapidly advancing field with rich physics that can be attributed to vacancies combined with metal diffusion. In particular, the talk highlighted his group’s pioneering work on monolayer memory (atomistors) that could enable various applications including zero-power devices, non-volatile RF switches, and memristors for neuromorphic computing.

Next, **Prof. James J. DiCarlo, MD, PhD** (Professor, Co-director at Quest for Intelligence, Department head, investigator of Institute for Brain Research, M.I.T) enlightened the audience with “*Reverse Engineering Visual Intelligence.*”

The brain and cognitive sciences are hard at work on a great scientific quest—to reverse engineer the human mind and its intelligent behavior. Yet these fields are still in their infancy. Not surprisingly, forward engineering approaches that aim to emulate human intelligence (HI) in artificial systems (AI) are also still in their infancy. Yet the intelligence and cognitive flexibility apparent in human behavior is an existence proof that machines can be constructed to emulate and work alongside the human mind.

The talk predicted that these challenges of reverse engineering human intelligence would be solved by tightly combining the efforts of brain and cognitive scientists (hypothesis generation and data acquisition), and forward engineering aiming to emulate intelligent behavior (hypothesis instantiation and data prediction). As this approach discovers the correct neural network models, those models will not only encapsulate our understanding

of complex brain systems, they will be the basis of next-generation computing and novel brain interfaces for therapeutic and augmentation goals (e.g., brain disorders).

Further, the talk focused on one aspect of human intelligence—visual object categorization and detection—and how work in brain science, cognitive science and computer science converged to create deep neural networks that could support such tasks. These networks not only reach human performance for many images, but their internal workings are modeled after—and largely explain and predict—the internal workings of the primate visual system. Yet, the primate visual system (HI) still outperforms current generation artificial deep neural networks (AI), suggesting that the brain and cognitive sciences can offer new clues.

These recent successes and related work suggest that the brain and cognitive sciences community is poised to embrace a powerful new research paradigm. More broadly, our species is at the beginning of its most important science quest—the quest to understand human intelligence. In short, his talk motivated the audience to engage that frontier alongside us.

The following speaker, **Dr. Laurens van der Maaten (Research Director at Facebook AI Research in New York)** talked about “*Exploring the Limits of Weakly Supervised Pretraining*.” State-of-the-art visual perception models for a wide range of tasks rely on supervised pre training. ImageNet classification is the de facto pretraining task for these models. Yet, ImageNet is now nearly ten years old and is by modern standards “small.” Even so, relatively little is known about the behavior of pretraining with datasets that are multiple orders of magnitude larger. The reasons are obvious: such datasets are difficult to collect and annotate. This talk covered a unique study of transfer learning with large convolutional networks trained to predict hashtags on billions of social media images. The experimental

data demonstrated that training for large-scale hashtag prediction led to excellent results. Improvements on several image classification and object detection tasks were shown and the highest ImageNet-1k single-crop, top-1 accuracy to date: 85.4% (97.6% top-5) reported. Extensive experimentation provided novel empirical data on the relationship between large-scale pretraining and transfer learning performance.

On the second day of the symposium **Pamela Norton (CEO, Borsetta)** gave a keynote on the importance of security, entitled “*Securing the Future of AI on the Edge with Intelligent Trusted Chips*.” To usher in this new edge economy, we need to ensure that the convergence of AI, new compute processing and intelligent chips migrating to the edge will protect our privacy and security. This keynote explored a framework to protect our privacy, security, and create new opportunities for all in this emerging new economy.

The following speaker, **Prof. Dheerisha Kudithipudi (Director of the MATRIX AI Consortium and the Robert F McDermott Endowed Chair in Engineering and Professor in ECE & CS University of Texas, San Antonio)** gave a talk entitled “*Neuro-Inspired AI: Compact and resilient models for the Edge*.” Neural plasticity offers insights into designing artificial intelligent systems. As the convergence of these two fields is in a nascent phase, there is a critical knowledge gap in designing neuromorphic systems that can support on-device learning with heterogeneous plasticity. She presented a recent in-silico learning system from the Nu.AI lab based on a CMOS/Memristor architecture. It emulated a biomimetic sequence memory algorithm inspired by the neocortex with structural and intrinsic plasticity mechanisms. The salient feature included a synthetic synapse representation that supports dynamic synaptic pathways for compact memory. The structural plasticity in the synaptic pathways was emulated in the memristor de-

vice’s physical behavior and the synaptic modulation is achieved through a custom training scheme.

Jay Gambetta (IBM Fellow and VP of Quantum Computing, IBM) next presented a quantum roadmap in a talk entitled “*Quantum circuits, and the Future of Quantum Technology in the Cloud*.” In the past few years, quantum computing has moved beyond the laboratory setting and has been accelerated through cloud access. It is a new kind of computing that uses the same physical rules that atoms follow to manipulate information. At this very fundamental level, quantum computers execute quantum circuits much like a computer executes logic circuits, but by using the physical phenomena of superposition, entanglement, and interference, to implement mathematical calculations that are out of the reach of even the most advanced supercomputers. He gave an overview of the IBM quantum effort to increase the device performance of superconducting qubit systems to produce quantum circuits with higher fidelity and how IBM is linking the computational difficulty of these circuits towards quantum applications. This is an exciting era where cutting edge research, system and software development are pushing the frontier forward, bolstered by an engaged and growing quantum computing community.

In the final talk of day two **Prof. Laurent Daudet (CTO and Co-Founder, LightOn; Professor at Université de Paris)** presented “*Unlocking Transformative AI with Photonic Computing*.” Recent large-scale AI models, such as OpenAI’s GPT-3 for NLP, open a wide range of economic opportunities, with possibly even more impact than deep learning had in the last decade. However, training these models requires massive amounts of computing power. This talk covered LightOn’s view on how future AI hardware should be designed for addressing some of the hardest computing challenges, such as in natural language processing (NLP), recommender

systems, and big science. In particular, the talk highlighted how Light-On's Optical Processing Units (OPUs) can be seamlessly integrated into a variety of hybrid photonics/silicon pipelines implementing state-of-the-art Machine Learning algorithms.

The symposium also featured a poster session. Out of 44 poster papers, 4 best poster papers were awarded. The list of winners was as follows:

- Tianyu Jia, Yuhao Ju, Russ Joseph and Jie Gu, "NCPU: A Binary Neural Network that Emulate RISC-V CPU at the Conjunction of Neuromorphic and Von-Neumann Architectures", Northwestern University, Evanston, Illinois
- Seah Kim and Hasan Genc, "Gemmini: Enabling Systematic Deep-Learning Architecture Evaluation via Full-Stack Integration", University of California, Berkeley, California
- Sanjeev T. Chandrasekaran, Sumukh Bhanushali, Imon Banerjee and Arindam Sanyal, "Towards intelligent wearable health monitors using reservoir computing CMOS IC", State University of New York at Buffalo, New York
- Minh Truong, "Data-Oriented Processing-Using-Memory with Emerging Memory Technology", Carnegie Mellon University, Pittsburgh, Pennsylvania

The symposium closed with a panel discussion entitled **"What will be the currency of future AI computation?"** The panel, moderated by Dr. Arvind Kumar, consisted of Pamela Norton, Prof. Dheerisha Kudithipudi, Dr. Sidney Tsai, Prof. Laurent Daudet, Prof. James J. DiCarlo, and Dr. Kristan Temme, representing expertise in security, analog AI, optical computing, brain science, and quantum computing. Each panelist gave an initial point of view on the panel topic, followed by questions from the audience. The initial points of view suggested benefits for each approach, but there was a general consensus that no one approach would dominate, and heterogeneous computing with se-

cure translation between 'currencies' would be needed. Technical questions were posed on a range of topics, such as the combination of approaches, emulation of Hebbian learning, plasticity and its importance, the longevity of current DNNs, and the role of Quantum Computing in AI. The panel ended with some questions from the audience seeking advice from the panelists for early researchers in the field.

Special thanks to Cindy Goldberg (IBM) and Brittian Parkinson (CAS) for all the publicity help.

Please visit the symposium webpage for more information about this year's symposium and future editions: <https://www.zurich.ibm.com/thinklab/Alcomputesymposium.html>

~Rinus Lee, Editor

VIII Congresso Brasileiro de Energia Solar (CBENS) A Hybrid Experiment Serving the Solar and EDS South American Communities

—by *Carla Andrade*¹,
*Ricardo Rüther*², and
*Lawrence L. Kazmerski*³

¹*Congress Chair, Federal University at Fortaleza (UFF) Brazil,*

²*Chair ABENS, Federal University at Santa Catarina (UFSC) Brazil,*

³*University of Colorado Boulder USA*

The **"VIII Congresso Brasileiro de Energia Solar (CBENS)"** took place October 26 to 29, 2020. This is the premier solar-energy conference in Brasil and serves many academic through industry technical organizations throughout South America. For the first time, CBENS was sponsored by the IEEE EDS—specifically because of its technology focus on photovoltaics and solar technologies and the link of many participants to the IEEE PVSC. This was the 8th in the series of these solar energy conferences—held on a 2-year schedule. But like so many conferences scheduled around the world, this was not "business-as-usual" in its design and operation. The serious

Impressions from an IEEE member delegate:

I was privileged to be able to be part of CBENS in Fortaleza—yes I did travel specifically to be part of this important conference during this difficult time. Certainly, I was motivated not only by my interest in PV R&D, but also by my longtime association with the IEEE, the EDS, and the IEEE PVSC—going back 50-years. With the help and encouragement from Brazilian and IEEE PV colleagues Ricardo Rüther (ABENS Chair) and Antonia Sonia Diniz (also a member of the EDS Technical Committee), we brought up the need for expanding the EDS influence and student membership into South America with the EDS Technical Committee headed by **Dr. Juzer Vasi and EDS Jr. Past President Fernando Guarin**. Their interest and endorsement at the IEEE PVSC in Chicago, and the incredible help (and patience!) of **Dr. Jacobus Swart** at UNICAMP in Campinas, the EDS Brazil representative, made it possible for us to make this IEEE link to the VIII CBENS. COVID, of course, was a concern for me and the other participants. But safety was a major concern: my temperature was taken at 2 separate places before entering the meeting hall; everyone was mandated to wear a mask—even when speaking; and delegates' seats were separated >2-meters. No banquets; no social events; no receptions. But the design of the hybrid meeting was quite professional and successful in both technical exchanges and bringing the community together. These are difficult times—but this meeting serves as an example of how professionals continue overcome even such unanticipated barriers. Thank you Fernando, Jacobus, and Juzer—but especially the IEEE EDS!

~L.L. Kazmerski, Fellow IEEE

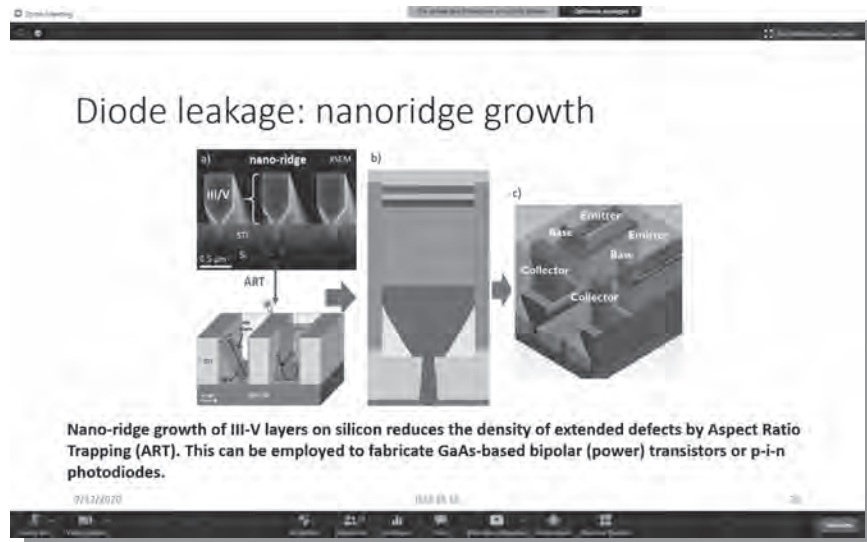
COVID situation caused a delay from the original date in early June 2020. Then, the format for the conference had to be altered—to a well-designed hybrid format, with a simultaneous “in-person” event in Fortaleza, Brasil, and a “virtual” venue. The on-site Fortaleza participation was limited to 100, with typically 60 attending. Complementing were 400 participants via the internet. There were 209 oral and 90 poster presentations. All these were viewed during the conference time—and available for 30 days following the event. The Congress included 2 workshops, 6 plenary sessions, 4 roundtable panels—as well as 3 business and networking sessions and 6 short-courses. The virtual component was very successful in engaging a larger student participation in the CBENS—estimated to be about 1/3 of the web-attendees. A special highlight was the well-organized **Women in Solar Energy** session that was formatted to provide lively interactions among the participants. An ingenious “word prioritization matrix” was used to identify areas of concern for these scientist and engineers for career and professional development. Certainly, this session had benefit and impact on the more than 150 women and men who were part of this special offering. ABENS (the Associação Brasileira de Energia Solar, www.abens.org.br) is the Brazil professional organization responsible for CBENS and voted to hold the next CBENS in Florianópolis, Santa Catarina, in the April–June timeframe 2022.

EUROPE, MIDDLE EAST & AFRICA (REGION 8)

Eddy Simoen DL—“Impact of Defects on Semiconductor Materials and Devices”

—by Mike Schwarz

The IEEE EDS Distinguished Lecture on “Impact of defects on semicon-



Prof. Eddy Simoen lecture “Impact of defects on semiconductor materials and devices”—one of the slides

ductor materials and devices” was held on 7 December 2020. It was organized by the EDS Germany Chapter and co-sponsored by the NanoP from THM—University of Applied Sciences. The DL was attended by 17 participants, with 10 IEEE participants and 7 guests.

Prof. Mike Schwarz, ED Germany Chapter chair, kindly introduced Prof. Simoen from imec and the University of Ghent, Ghent, Belgium.

Prof. Simoen started with a motivation, in which he stressed an impact of defects on semiconductor material and device characteristics. Afterwards, he continued his lecture with a detailed overview on the defect formation in hetero-epitaxy systems. Then he explained the electrical impact of defects and gave a lot of insights in various measurement methods, e.g. DLTS. He discussed GR noise and GR noise spectroscopy as further measurement methods to detect defects. Then he presented several case studies, e.g. “Impact on leakage InGaP & GaAS p-i-n diodes” and “GR noise spectroscopy of GaN-on-Si MOSHEMTs. Finally, he concluded his talk by a summary with all important effects.

A huge “thank you” to all participants and Eddy Simoen.

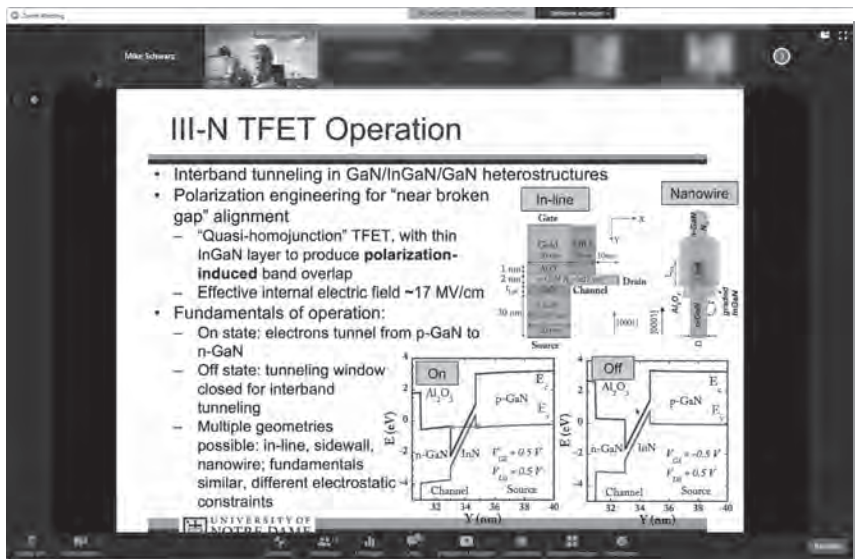
Patrick Fay DL—III-N Nanowire FETs for Low-Power-Applications

—by Mike Schwarz

The IEEE EDS Distinguished Lecture on III-N Nanowire FETs for Low-Power-Applications was held on 23 November 2020. It was organized by the EDS Germany Chapter and co-sponsored by the NanoP from THM—University of Applied Sciences. The DL was attended by 17 participants, with 9 IEEE participants and 8 guests.

The IEEE DL was opened by Prof. Mike Schwarz, ED Germany Chapter Chair. He kindly introduced Prof. Fay from the University of Notre Dame, Indiana, USA, and the participants.

Prof. Fay started with a motivation of III-N compounds application in low power system applications. He pointed out that heterogeneous integration of III-N FETs sets new challenging fields for researchers. The question arises, if GaN can play a role in low power systems? The speaker continued with some background information and properties of GaN and III-N semiconductors. He presented their advantages and challenges. It is well known that material characteristics strongly influence the device parameters. However, a key factor determining applicability of III-N FETs in low power applications



Prof. Patrick Fay during the lecture III-N Nanowire FETs for Low-Power-Applications

is low enough subthreshold slope of the transistor characteristics. This requirement is common for all the field-effect devices in low power solutions. If achieved then not only logic, but also analog and further emerging applications can benefit from the superior III-N properties.

Prof. Fay continued and presented GaN-based nanowires for low power applications. He offered GaN nanowire FETs, details on the process, e.g. material growth, oxide deposition, etc. Furthermore, the lecturer discussed the gate capacitances for c- and m-plane substrates. Afterwards, experimental results as transport characteristics and output characteristics with remarkable on-current of $130\mu\text{A}/\mu\text{m}$ and with $I_{\text{on}}/I_{\text{off}}$ ratio larger than 10^8 were presented. Possible enhancements of the devices were also shown.

A second part of the lecture dealt with TFETs made of III-N semiconductors. After a short introduction into the basic principles, Prof. Fay promised such devices to be another option for low power solutions. He referred to TFET design possibilities and showed some simulation results for GaN/InGaN/GaN heterostructures and their TFET performances. Further investigations of III-N Nanowire TFET scalability were presented. Finally, the speaker showed actual experimental results of

such III-N Nanowire TFET, published in 2020 by A. Chaney et al. at Cornell.

After the presentation several questions allowed for a fruitful discussion on various topics. A huge "Thank you" to all participants and Patrick Fay.

Michael Shur DL—Counter Intuitive Physics of Ballistic Transport in the "State-of-the-Art Electronic Devices"

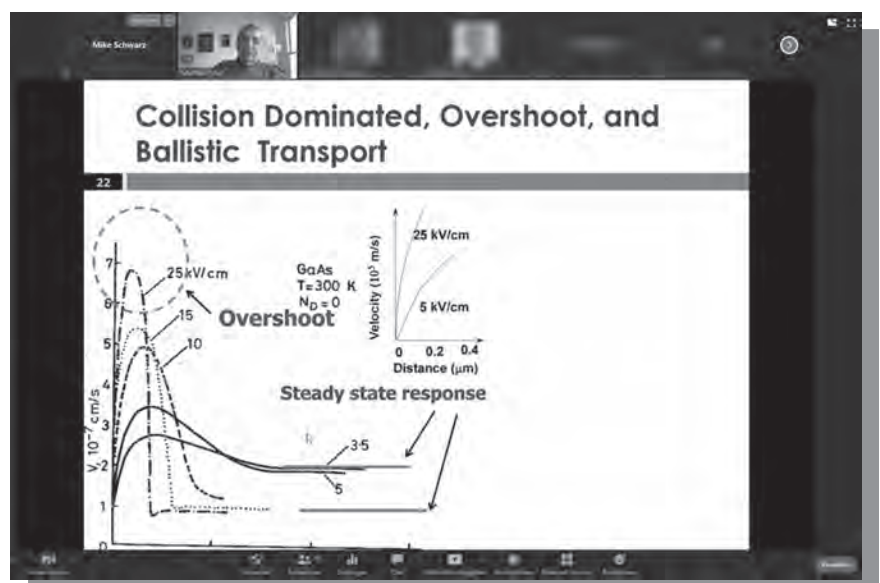
—by Mike Schwarz

The IEEE EDS Distinguished Lecture on Counter Intuitive Physics of Ballistic Transport in the "State-of-the-Art Electronic Devices" was held on 16 November 2020. It was organized by the EDS Germany Chapter and co-sponsored by the NanoP from THM—University of Applied Sciences. The DL was attended by 30 participants, with 17 IEEE participants and 13 guests.

Prof. Mike Schwarz, ED Germany Chapter Chair, opened the IEEE DL in Zoom. He warmly welcomed Prof. Shur from Rensselaer Polytechnic Institute, New York, USA, and the participants to be part of this DL.

Prof. Shur started with a motivation on the "industrial face of nanotechnology". He continued with the question "What is ballistic transport?" and answered it from the physics point of view. Furthermore, he addressed the question "Why is it important?", and gave examples on ballistic mobility and ballistic impedance. Afterwards, he shared knowledge on plasmonic devices and THz electronics technology.

A huge "Thank you" to all participants and to the lecturer.



Prof. Michael Shur during the lecture Counter Intuitive Physics of Ballistic Transport in the "State-of-the-Art Electronic Devices"

ESSCIRC-ESSDERC 2020

Summary

—by Francis Balestra

Under the current sanitary situation worldwide, the organizing committee decided earlier in 2020 to organize a virtual event in September 2020 with only educational events.

The peer selected paper submission section has been replaced with IEEE journals special issues:

- For ESSCIRC: IEEE SSC-L Special issue: 140 papers submitted (vs. 200 papers submitted to the “non-virtual” conference)
- For ESSDERC: IEEE TED Special Issue: 45 papers submitted (vs. 90 papers submitted to the “non-virtual” conference)

Thirteen educational events have been organized with overall 100 speakers covering both electronic circuit and device technologies. Very high levels of educational agenda and presentations have been carefully prepared by the session chairs together with the corresponding speakers.

1. TUTORIAL | Quantum Computing: Myth or Reality?

Chairs: Maud Vinet (CEA) and Farhana Sheikh (Intel)

2. WORKSHOP | Emerging Solutions for Imaging Devices, Circuits and Systems

Chairs: Matteo Perenzoni (FBK) and AlbertTheuvsen (Harvest Imaging)

3. WORKSHOP | Non-Volatile Memories: Opportunities and Challenges from Devices to Systems

Chairs: Gabriel Molas (CEA) and Mahmut Sinangil (TSMC)

4. WORKSHOP | New 5G integration solutions, and related technologies (from materials to system)

Chairs: Nadine Collaert (imec) and Stefan G. Andersson (Ericsson)

5. WORKSHOP | Advances in device technologies for automotive industry (power devices, SiC, GaN)



Chairs: Ionut Radu (Soitec) and Stefaan Decoutere (IMEC)

6. WORKSHOP | Embedded monitoring and compensation design for energy or safety constrained applications

Chairs: Sylvain Clerc (ST) and Keith Bowman (Qualcomm)

7. WORKSHOP | Edge AI and In-Memory-Computing for energy efficient AIoT solutions

Chairs: Andreas Burg (EPFL) and Marian Verhelst (KUL)

8. WORKSHOP | Ab-initio simulations supporting new materials & process developments

Chairs: Denis Rideau (ST) and Philippe Blaise (Silvaco)

9. WORKSHOP | RISC-V cooking session

Chairs: Bora Nikolic (BWRC)

10. DISSEMINATION WORKSHOP | Toward sustainable IOT from rare materials to big data

Chairs: Thierry Baron (CEA, LTM/UGA) and Audrey Dieudonné (UGA)

11. DISSEMINATION WORKSHOP | High Density 3D CMOS Mixed-Signal Opportunities

Chair: Philipp Häfliger (UiO University of Oslo)

12. MOS-AK WORKSHOP | Compact/SPICE Modeling and its Verilog-A Standardization

Chair: Wlodek Grabinski (MOS-AK) and Daniel Tomaszewski (ITE Warsaw)

13. IPCEI on Microelectronics: Innovative Technologies for Shaping the Future

Chairs: Dominique Thomas (ST), Klaus Pressel (Infineon), Rainer Pforr (Zeiss)

The presentation materials are available for registered users on the ON24 digital platform provided by IEEE. Moreover, the video of the interactive, Live Sessions are now available on the ON24 platform.

Regarding the attendees, 400+ registrations have been recorded with a good balance between Industry (~40%), Academia (~40%) and Research Institutes (~20%). Information on the conference can be found here: <https://www.esscirc-essderc2020.org/>

ASIA & PACIFIC (REGION 10)

ED Malaysia Kuala Lumpur Chapter

—by Aliza Aini Md Ralib,
Rosminazuin Ab Rahim,
Sharifah Fatmadiana Wan
Muhammad Hatta and
Maizatul Zolkapli

Online Webinar on Final Year Project Preparation

The ED Malaysian Chapter together with Kulliyah (Faculty) of Engineering, International Islamic University Malaysia (IIUM) conducted on 30 October 2020, a webinar for IIUM ECE final year project (FYP). This discourse is one of the requirements to obtain an undergraduate degree in the Kulliyah (Faculty) of Engineering, IIUM. Two speakers shared their experiences on how to conduct the final year project. Ir. Ts. Dr. Maizatul Zolkapli from Universiti Teknologi MARA presented on “How to write a good literature review,” while Prof. Teddy Surya Gunawan from IIUM shared on “How to write a good FYP report.” The webinar managed to attract 77 audiences. The program lasted for two hours and received positive feedback from the audience.

Online Webinar on MIMOS Semiconductor (MYSEM): An Overview of Wafer Fabrication

—by Dr. Ir. Hazian Mamat

On 4 December 2020, The ED Malaysian Chapter together with the ECE

Department, Kuliyah (Faculty) of Engineering, IIUM successfully conducted an online webinar entitled "MIMOS Semiconductor (MYSEM): An overview of wafer fabrication" by Ir. Dr. Hazian Mamat who is a senior engineer from MIMOS Berhad Malaysia. The webinar managed to attract 73 participants. The audience were mainly from final year project engineering students, postgraduate students from Kuliyah (Faculty) of Engineering, IIUM and also IEEE EDS members. An overview of the wafer fabrication process in the cleanroom was presented by the invited speaker. Dr. Ir. Hazian also explained about the facilities available at MIMOS as an exposure to the students which are related to the wafer fabrication. The program lasted for an hour. The program received positive feedback from the audience.

Let's Talk: Electronics Reliability

The ED Malaysia Chapter initiated a new technical talk series called "Let's Talk" which is an online program with three panels of speakers, on the 4 December 2020—two panels were from academia and one was from the industry. The first edition of this series focused on the topic of "Electronics Reliability," and managed to attract 40 participants. The participants consisted of academics from Malaysia, United Kingdom and Turkey. The first panelist was Professor Ir. Dr. Norhayati Soin (University of Malaya) whose topic was "Overview of Reliability in Semiconductor Electronics." The second panelist was Ir. Ts. Dr. Azrif Manut (Universiti Teknologi MARA) whose topic was "MOSFET Reliability," while the third panelist was Mr. Mohd Hanif Kamaruddin, a Principal Engineer from Infineon Technologies (Kulim), whose topic was "Fast Wafer Level Reliability Testing." The moderator was Dr. Sharifah Fatmadiana (University of Malaya). Each panelist was allocated a 10 minutes' session to talk on the topic and a Q&A session was allocated at the end of the final talk. The program

lasted for an hour and received positive feedback from the audience.

IEEE Regional Symposium on Micro and Nanoelectronics (RSM) 2021

The ED Malaysia Chapter is pleased to welcome everyone to participate in the 2021 IEEE Regional Symposium on Micro and Nanoelectronics (RSM) on 2–4 August 2021. This bi-annual technical conference since 1997 aims to bring together researchers from industry and academia to gather and explore various issues and trends in the field of semiconductor electronics. This will be the 13th RSM organized by the Electron Devices Chapter of IEEE Malaysia Section and technically co-sponsored by the IEEE Electron Devices Society. Over the last twenty-four years, RSM conference series has become the prominent international forum on semiconductor electronics embracing numerous aspects of the semiconductor technology including circuit and device modelling and simulation, photonics and sensor technology, MEMS technology, packaging technology, failure analysis and reliability, materials and devices for nanoelectronics. Please visit the website for further details <https://ieeemalaysia-eds.org/rsm2021>.

~Sharma Rao Balakrishna, Editor

ED Tainan Chapter—IEEE EDS Invited Lecture

—by Wen-Kuan Yeh

The ED Tainan Chapter held one invited lecturer presentation at Hsinchu, Taiwan on 21 October 2020. Prof. Ting-Chang Chang (IEEE Fellow, Chair Professor, Department of Physics, National Sun Yat-Sen University) gave a talk in Taiwan Semiconductor Research Institute (TSRI). The lecture topic was "Low Temperature Passivation for Semiconductor Devices." This talk focused on the high pressure/low temperature technology for the improvement of semiconductor devices and applications including Si-based CMOSFET, Resistive RAM, high power SiC and some bio-chips. Prof. Chang's technical contributions in non-volatile memory, advanced MOSFET and thin film transistors have had a major impact on the field, as is evidenced by his patents which are in use by Taiwan's leading tech companies. Prof. Chang is an expert in NVM and TFT research who has made many technology breakthroughs to enhance device performance and to solve reliability issues. These breakthroughs have had an important impact on the global semiconductor industry. To date, more than 80 doctoral students and 200 master's students have graduated under his guidance, and many of them have followed his



Prof. Ting-Chang Chang; invited talk for ED Tainan Chapter; 21 October 2020

footsteps and expanded his influence in the semiconductor industry. About 40 attendees and several professors of universities from Hsinchu, Taiwan attended this talk.

ED/SSC Hong Kong Chapter - 2020 Student Symposium on Electron Devices and Solid-State Circuits

—by Qiming Shao

On 25 October 2020, the 2020 Student Symposium on Electron Devices and Solid-State Circuits (s-EDSSC) was held online via the Zoom platform. It was organized by the IEEE Hong Kong Joint Chapter of ED/SSC Societies and the Department of Electronic and Computer Engineering at the Hong Kong University of Science and Technology. The s-EDSSC Symposium serves as a platform for undergraduate and graduate students who work on, or have an interest in the field of ED/SSC to present their results and exchange ideas with peers and senior researchers in the community.

The participants were from different universities in Hong Kong and mainland China. Thirteen submitted papers were selected for presentations. After presentations, the commit-

tee selected five of the best student papers, based on the quality of the manuscripts and presentations. Each awardee received a certificate and a cash award of HKD 500. The nominated awardees were originally from Hong Kong, mainland China, and foreign countries, showing a good diversity in terms of a geographical affiliation. The attendees exhibited their interests by asking many questions and provided a very positive feedback on the 2020 s-EDSSC. More information about the 2020 s-EDSSC can be found on the IEEE HK ED/SSC Chapter website: <https://r10.ieee.org/hk-edssc/>.

~Ming Liu, Editor

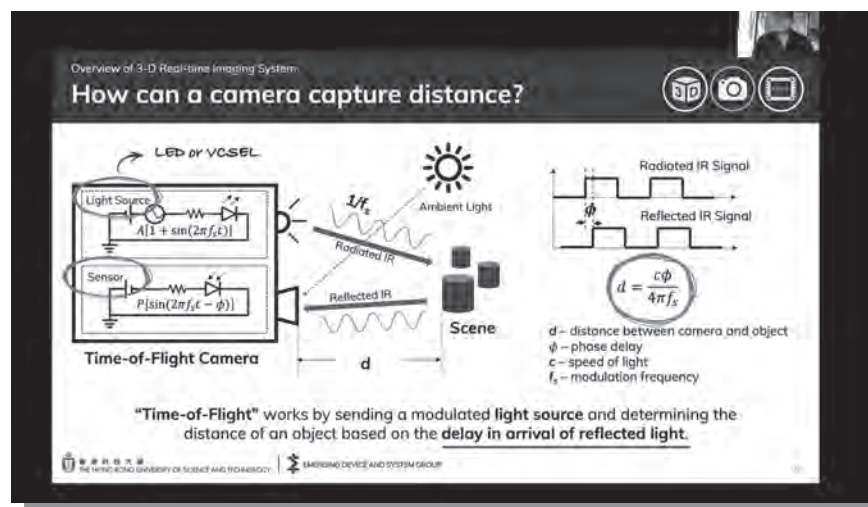
ED Delhi Chapter Mini-Colloquium on “Emerging Nano Devices and Circuits—The Roadmap Ahead”

—by Harsupreet Kaur

The Department of Electronic Science, University of Delhi South Campus and ED Delhi Chapter jointly organized the IEEE Electron Devices Society Distinguished Lecture Mini-Colloquium on “Emerging Nano Devices and Circuits—The Roadmap Ahead.” The Mini-Colloquium

was held virtually from 5–9 October 2020. Six talks were given during the week-long Mini-Colloquium. The MQ inaugural talk was delivered by Prof. Hiroshi Iwai, Tokyo Institute of Technology, Japan, on “End of CMOS miniaturization and technology development before and after.” Prof. Iwai discussed the evolution of the CMOS technology, the innovations and emerging trends that are expected to lead to a paradigm shift in technology. The second talk was also held on 5 October 2020 and was delivered by Prof. Ajit Panda, NIST Berhampur, Odisha, India, on “Semiconductor Devices for 5G Communication.” The next day Prof. Sorin Cristoloveanu, IMEP - INP Grenoble MINATEC, France, delivered a talk on “Sharp switching transistors based on electrostatic doping.” On 7 October 2020, Prof. Joachim N. Burghartz, Institute for Microelectronics Stuttgart (IMS CHIPS), Germany delivered a talk “Ultra-thin Chips—a New Paradigm in Silicon Technology.” Both speakers apprised the participants about various novel aspects and emerging trends in these areas. On 8 October 2020, Prof. Xing Zhou, Nanyang Technological University, Singapore gave a talk “Future III-V/CMOS Co-Integrated Technology and Hybrid Circuit Design.” Recent advancements made in the area of III-V/ CMOS co-integrated technology were also highlighted. The concluding talk was held on 9 October 2020 and was given by Prof. Frank Schwier, Technische Universität Ilmenau, Germany, on the topic “2D Devices and 2D Electronics.” Prof. Schwier discussed various aspects related to 2D materials and devices and also apprised the participants about the upcoming trends in this area. The Mini-Colloquium was widely attended by over 100 researchers, engineers and students who enjoyed this series of interesting lectures.

~Soumya Pandit, Editor



A screenshot from s-EDSSC presentation (via Zoom) titled “Compact Modeling of Current-Assisted Photonic Demodulator (CAPD) for Time-of-Flight CMOS Image Sensor” (given by Cristine Jin Delos Santos Estrada, one of the best student paper award winners)

EDS MEETINGS CALENDAR



THE COMPLETE EDS CALENDAR CAN BE FOUND AT OUR WEB SITE:
[HTTP://EDS.IEEE.ORG](http://eds.ieee.org). PLEASE VISIT.

<u>2021 22nd International Symposium on Quality Electronic Design (ISQED)</u>	07 April – 08 April 2021	Virtual Event
<u>5th IEEE Electron Devices Technology and Manufacturing Conference (EDTM)</u>	08 April – 11 April 2021	Chengdu, China Hybrid Event
<u>2021 IEEE 34th International Conference on Microelectronic Test Structures (ICMETS)</u>	12 April – 15 April 2021 Postponed to 2022	Cleveland, OH
<u>2021 IEEE Latin America Electron Devices Conference (LAEDC)</u>	19 April – 21 April 2021	Virtual Event
<u>2021 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA)</u> <u>2021 International Symposium on VLSI Design, Automation and Test (VLSI-DAT)</u>	19 April – 22 April 2021	Hsinchu, Taiwan
<u>2021 22nd International Vacuum Electronics Conference (IVEC)</u>	27 April – 30 April 2021	Virtual Event
<u>2021 32nd Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC)</u>	10 May – 13 May 2021	Virtual Event
<u>2021 International Siberian Conference on Control and Communications (SIBCON)</u>	12 May – 14 May 2021	Kazan, Russia
<u>2021 IEEE International Memory Workshop (IMW)</u>	15 May – 18 May 2021	Virtual Event

<u>2021 33rd International Symposium on Power Semiconductor Devices and ICs (ISPSD)</u>	29 May – 02 June 2021	Nagoya, Japan Hybrid Event
<u>2021 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)</u>	06 June – 08 June 2021	Atlanta, GA Hybrid Event
<u>2021 20th International Workshop on Junction Technology (IWJT)</u>	11 June – 12 June 2021	Virtual Event
<u>2021 Silicon Nanoelectronics Workshop (SNW)</u>	12 June – 13 June 2021	Kyoto, Japan
<u>2021 Symposium on VLSI Technology and Circuits</u>	13 June – 16 June 2021	Virtual Event
<u>2021 Device Research Conference (DRC)</u>	20 June – 23 June 2021	Virtual Event
<u>2021 IEEE 48th Photovoltaic Specialists Conference (PVSC)</u>	19 June – 24 June 2021	Virtual Event
<u>2021 International EOS/ESD Symposium on Design and System (IEDS)</u>	23 June – 25 June 2021	Chengdu, SICHUAN, China
<u>2021 IEEE International Interconnect Technology Conference (IITC)</u>	05 July – 08 July 2021	Kyoto, Japan
<u>2021 9th International Symposium on Next Generation Electronics (ISNE)</u>	10 July – 12 July 2021	Changsha, China
<u>2021 IEEE International Flexible Electronics Technology Conference (IFETC)</u>	08 Aug – 11 Aug 2021	Columbus, OH Hybrid Event
<u>2021 35th Symposium on Microelectronics Technology and Devices (SBMicro)</u>	22 Aug – 26 Aug 2021	Campinas, Brazil
<u>2021 28th International Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD)</u>	01 Sept – 04 Sept 2021	Kyoto, Japan

<u>2021 IEEE 32nd International Conference on Microelectronics (MIEL)</u>	12 Sept – 14 Sept 2021	Virtual Event
<u>2021 International Semiconductor Conference (CAS)</u>	06 Oct – 08 Oct 2021	Virtual Event
<u>2021 16th European Microwave Integrated Circuits Conference (EuMIC)</u>	10 Oct – 11 Oct 2021	London, United Kingdom
<u>2021 IEEE/ACM International Conference On Computer Aided Design (ICCAD)</u>	31 Oct – 03 Nov 2021	Munich, Germany
<u>2021 IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)</u>	06 Nov – 08 Nov 2021	Redondo Beach, CA
<u>2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)</u>	05 Dec – 08 Dec 2021	Monterey, CA
<u>2021 IEEE 52nd Semiconductor Interface Specialists Conference (SISC)</u>	08 Dec – 11 Dec 2021	San Diego, CA
<u>2021 IEEE International Electron Devices Meeting (IEDM)</u>	11 Dec – 16 Dec 2021	San Francisco, CA



Call for Papers
for a Special Issue of
IEEE Transactions on Electron Devices
on
“Solid-State Image Sensors”

Over the last decade, solid-state image sensors have sustained impressive technological developments as well as growth in existing markets such as camera phones, automotive cameras, security and industrial cameras and medical/scientific cameras. This has included; sub-micron pixels, high dynamic range sensors for automotive and machine vision, time-of-flight sensors for 3D imaging, 3-dimensional integration (wafer level stacking) for small and efficient imaging systems on a chip, sub-electron read noise pixels and avalanche photodetectors for single-photon imaging, detector structures for non-cooled infrared imaging, and many others. Solid-state image sensors are also taking off into new applications and markets (IoT, 3D imaging, medical, biometrics and others). Solid-state image sensors are now key components in a vast array of consumer and industrial products. This special issue will provide a focal point for reporting these advancements in an archival journal and serve as an educational tool for the solid-state image sensor community. Previous special issues on solid-state image sensors were published in 1968, 1976, 1985, 1991, 1997, 2003, 2009 and 2016.

Topics of interest include, but are not limited to:

- Pixel device physics (New devices and structures, Advanced materials, Improved models and scaling, Advanced pixel circuits, Performance enhancement for QE, Dark current, Noise, Charge Multiplication Devices, etc.)
- Image sensor design and performance (New architectures, Small pixels and Large format arrays, High dynamic range, 3D range capture, Low voltage, Low power, High frame rate readout, Scientific-grade, Single-Photon Sensitivity)
- Image-sensor-specific peripheral circuits (ADCs and readout electronics, Color and image processing, Smart sensors and computational sensors, System on a chip)
- Non-visible “image” sensors (Enhanced spectral response e.g., UV, NIR, High energy photon and particle detectors e.g., electrons, X-rays, Ions, Hybrid detectors, THz imagers)
- Stacked image sensor architectures, fabrication, packaging and manufacturing (two or more tiers, back-side illuminated devices)
- Miscellaneous topics related to image sensor technology

Submission Instructions:

When submitting your manuscript through the IEEE’s web-based ScholarOne Author Submission and Peer Review System (<https://mc.manuscriptcentral.com/ted>), please indicate that your submission is for this special issue.

Manuscripts should be submitted in a double column format using an IEEE style file. Please visit the following link to download the templates:
http://www.ieee.org/publications_standards/publications/authors/author_templates.html

Submission deadline: July 30, 2021

Publication date: June 2022

Guest Editors:

1. Mr. R. Michael Guidash, R.M. Guidash Consulting, USA
2. Dr. Daniel Van Blerkom, Forza Silicon – Ametek, USA
3. Dr. Guy Meynants, Photolithics, KU Leuven, Belgium
4. Dr. Rihito Kuroda, Tohoku University, Japan



Call for Papers
for a Special Issue of
IEEE Transactions on Electron Devices
on
"Spintronics-Devices and Circuits"

Spintronics is one of the emerging fields for the next-generation nanoscale devices offering better memory and processing capabilities with improved performance levels. It demonstrates great potential in the post-Moore era. Ever since the discovery of Giant Magneto-Resistance (GMR) effect in 1988, spintronics has shown a rapid progress. Recent advances have expanded this technology to the entire electronics industry of sensors, memories, oscillators, quantum information processors, computer architecture, brain inspired computing and various other fields. Spintronics is now one of the most researched areas and is on the verge of becoming a mainstream technology. A hard disk drive (HDD) invented by IBM in 1956, now has a global market revenue of approximately \$12bn. Other emerging field of application for this technology is magnetic field sensors that showcased a market revenue of ~ \$19b in 2018. The magnetic memory production at major foundries such as Samsung, Globalfoundries, Western Digital and TSMC marks the adoption of spintronics technology. However, in order to meet the ever-increasing demands of the industry, innovation in terms of modeling, design, materials, processes, circuits and applications are required. This Special Issue of the IEEE Transactions on Electron Devices will feature the most recent developments and the state-of-the-art in the field of spintronic devices, circuits and new architectures for high performance.

Topics of interest include, but are not limited to:

Materials: Ferromagnets, Antiferromagnets, 2D material for better spin manipulation and spin logic devices, Heusler alloys, dilute magnetic semiconductors (DMS), half-metallic ferromagnet (HMF)...

Transport mechanism: Spin accumulation, injection and detection in spin devices, spin pumping techniques, angular momentum transportation by spin polarized currents, spin waves, magnons, spin hall effect, spin transfer torque, enhancement in spin diffusion length and coherence time...

Spintronics devices: STT-MRAM, SOT-MRAM, VCMA-MRAM, domain-wall, skyrmions, nano-oscillators, sensors etc. Low power and high-speed switching schemes for spintronic devices.

Optoelectronics and Spintronics: All-optical switching of magnetization, inverse magneto-optical effects, single shot optical switching, modeling circuit and architecture level design for ultra-fast laser excitation...

Memories: High storage density MRAM, enhancement in power efficiency and speed.

In-memory computing: Spintronics based in-memory computing/ processing circuits/ architectures and applications...

Quantum Computing: Quantum information processing, protocol for communication, computation and sensing, algorithms, spin qubit, systems and applications, spintronics-based quantum memories...

Neuromorphic computing: Hardware implementation of neural networks, analog and digital, architectures and applications...

Fabrication: Fabrication and characterization of novel materials and devices, hybrid spintronics integration and fabrication...

Spintronics based circuits: Reconfigurable and programmable spintronics based circuits, Security applications including RNG and PUF, ADC/DAC, reliability and power performance analysis of spintronics based devices and circuits...

Submission instructions: Please visit the following link to download the templates: http://www.ieee.org/publications_standards/publications/authors/author_templates.html In your cover letter, please indicate that your submission is for this special issue. Submission site: <https://mc.manuscriptcentral.com/ted>

The papers must present original material that has not been copyrighted, published or accepted for publications in any other archival publications, that is not currently being considered for publications elsewhere, and that will not be submitted elsewhere while under considerations by the Transactions on Electron Devices.

Submission deadline: 30 September, 2021

Publication date: April 2022

Guest Editors:

1. Prof. Brajesh Kumar Kaushik, Department of Electronics and Communication Engineering, Indian Institute of Technology Roorkee, INDIA (*Lead Guest Editor*)
2. Dr. Sanjeev Aggarwal, Everspin Technologies Inc., USA
3. Prof. Supriyo Bandyopadhyay, Department of Electrical and Computer Engineering, VCU College of Engineering, USA
4. Prof. Debanjan Bhowmik, Department of Electrical Engineering, Indian Institute of Technology Delhi, INDIA
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9. Prof. Kaushik Roy, School of Electrical and Computer Engineering, Purdue University, USA
10. Prof. Ashwin A. Tulapurkar, Department of Electrical Engineering, Indian Institute of Technology Bombay, INDIA



EDS VISION, MISSION AND FIELD OF INTEREST STATEMENTS

Vision Statement

Promoting excellence in the field of electron devices for the benefit of humanity.

Mission Statement

To foster professional growth of its members by satisfying their needs for easy access to and exchange of technical information, publishing, education, and technical recognition and enhancing public visibility in the field of Electron Devices.

EDS Field of Interest

The EDS field-of-interest includes all electron and ion based devices, in their classical or quantum states, using environments and materials in their lowest to highest conducting phase, in simple or engineered assembly, interacting with and delivering photo-electronic, electro-magnetic, electromechanical, electro-thermal, and bio-electronic signals. The Society sponsors and reports on education, research, development and manufacturing aspects and is involved in science, theory, engineering, experimentation, simulation, modeling, design, fabrication, interconnection, reliability of such devices and their applications.