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Newsletter

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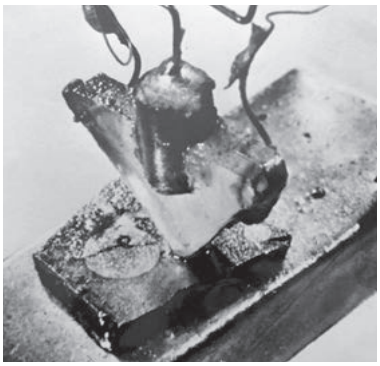

Photo Courtesy: Bell Labs '47

The year 1905 is well known as the "Miracle Year" because Albert Einstein published four papers that changed the laws of physics and were significant contributions to the foundation of modern physics. Similarly, November 1947–January 1948 were the three magical months that paved the way for modern-day electronics. This was done by three brilliant scientists who were members of the Mervin Kelly's Solid State Physics Group and Semiconductor Sub-Group at Bell Labs, which were given the challenging task of creating a solid-state semiconductor switch that could replace the vacuum tube. The famous physicists—Walter Brattain and John Bardeen managed to make the first working transistor, now known as the point-contact transistor. The invention was made on December 16, 1947. A week after that, the device was officially demonstrated to Bell Labs executives as a "magnificent Christmas present." In January 1948, William Shockley demonstrated the junction transistor. All three received The Nobel Prize in Physics (1956) and as per Nobel Prize Committee—"In 1947 John Bardeen and Walter Brattain produced a semiconductor amplifier, which was further developed by William Shockley. The component was named a "transistor"."

The Electron Devices Society has decided to celebrate the year 2022–2023 as the 75th Anniversary of the Transistor. As the history of this invention and of its consequences is much more involved and interesting, it is imperative that the leading EDS Luminaries share the scientific & technological developments which took place in the last 75 years, with the current generation of researchers. Popularizing talks at Conferences and Mini-Colloquia, Technical Articles in the EDS Newsletter, Webinar Series shall be a part of the

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ELECTRON DEVICES SOCIETY

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NEWSLETTER DEADLINES

Issue	Due Date
October	July 1st
January	October 1st
April	January 1st
July	April 1st

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Invention of the Transistor 75 Years Ago; The Origin of Device Miniaturization Towards Super-Intelligent Society

HIROSHI IWAI

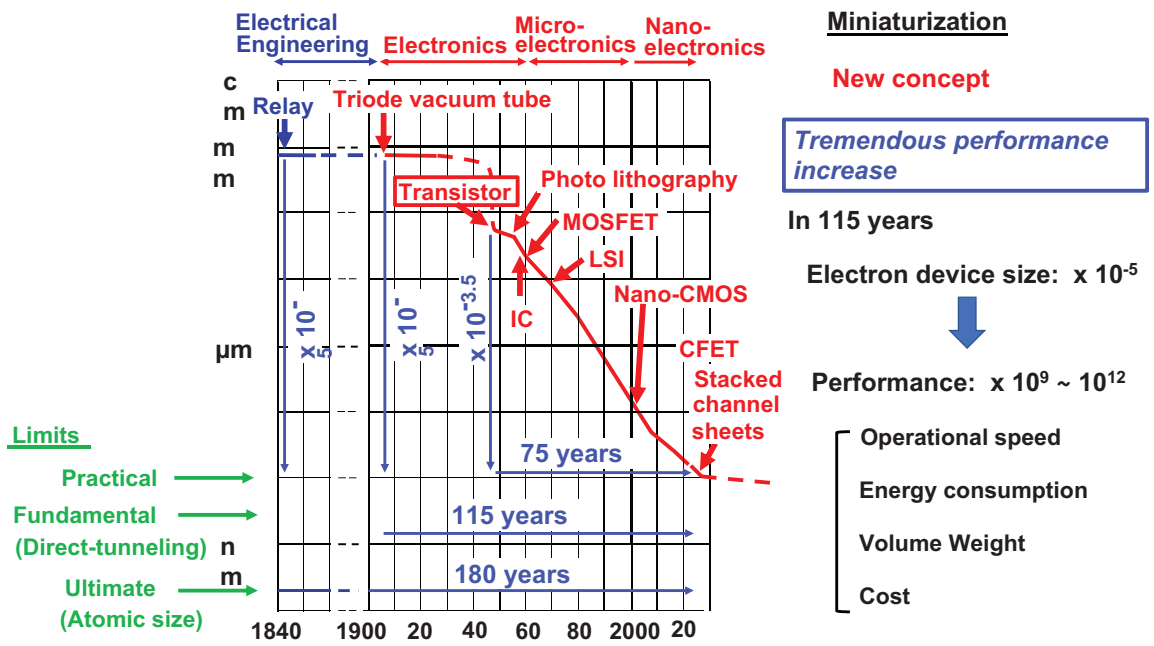
1. Before the Transistor

In the middle of the 19th century, electrical engineering provided us with a **big technological leap, i.e., instantaneous long-distance transportation of 'energy' and 'information' through electric wires.** The 'information transportation' was conducted at the end of the 1830's by the electric telegraph with 'relays' used as the amplifier of the decaying signal (Morse code) propagating on a long wire [1]. **The relay was the first electric device which amplified electric signal, but it had a function of only digital signal amplification** by the mechanical switch controlled by the signal current flowing in the electromagnet coil.

Then, 60 years later, wireless telecommunication started with a strong demand for the analog signal amplification. **The analog signal amplification was realized by the invention of the 'triode vacuum tube' in 1906** [2]. The electron current in a vacuum tube between the cathode and anode was directly modulated by the potential of the 'grid electrode' inserted in the electron current flow. The analog signal imposed on the grid bias was transferred into the electron current and amplified. The grid bias can also switch on/off the electron current. The triode vacuum tubes had been widely used for telecommunication and machine control since then. **This was the beginning of 'electronics' that enabled the manipulation of electron movement in the devices for many applications.**

2. The Road to the Transistor

However, the vacuum tubes were not suitable for low power-consumption operation and also for very high-frequency operation at microwave range due to the difficulty of the size reduction. **It would be quite natural to imagine that replacing the vacuum tubes by solid-state amplifiers could solve the above problems.** The idea was to modulate the lateral current in a solid-state material by the vertical electric field applied by the 3rd terminal, i.e., 'grid' or 'gate'. This is the analogy to the triode vacuum tubes and the idea of the 'Field Effect Transistor (FET), although the term 'transistor' did not exist at that time. **However, different from the case of electron current in the vacuum, controlling the electron current in solid-state materials by the vertical electric field was not easy because of the high-density charges of electrons and ions existing in the solid-state materials.** Thus, it was assumed to be necessary to use an 'extremely-thin semiconductor film' as the solid-state material. The first recorded ideas of the FET were filed as patents without any experimental data in 1925 for MESFETs [3] and 1928 for MOSFETs [4]. Although semiconductors had been already used for commercial crystal rectifiers [5]–[7] from the beginning of the 20th century, the physics of semiconductors such as band theory [8] using quantum mechanics was not known at all until the 1930's. At that time, there were even no concepts of holes and p-n junctions, and the quality of the semiconductor materials was not sufficient at all [9]. Later in 1945–1948, W. Shockley of Bell Telephone Laboratories thought of an idea of MOSFETs [9]–[12] independently from the previous MOSFET ideas. His idea was **to modulate the carrier density at the semiconductor surface by the band bending caused by the vertical electric field from the gate electrode. He predicted the amount of the carrier density modulation based on the calculation using the band theory**. However, the experimental carrier density modulations on Si, Ge and Cu_2O were 3–4 magnitudes of order smaller than those of the theoretical calculations [9]–[12] because of the existence of the fixed electrons trapped at the surface states [13]. (The accumulation layer conduction with the majority carriers of the MOSFET is shown in W. Shockley's works [10], but the inversion layer conduction with the minority carriers was not recognized by his works [10], [12]. The inversion type of the conduction was found by J. Bardeen in 1947 [14] and the inversion layer conduction used in today's MOSFETs was clearly described later by L. Brown's paper [15] published in 1953). W. Shockley's group continued the research for preventing the trapped surface charge effect, and



Trend of minimum line width used for devices and performance increase

fortunately, J. Bardeen and W. Brattain found, on December 16, 1947, **current amplification phenomena when they put the 2 gold point-contact electrodes (emitter and collector electrodes)—with the separation of 50 μm—directly onto the n-type Ge surface** [9]–[11], [16], [17]. The Ge substrate was connected to the base electrode from the backside. The injection of holes from the emitter electrode under the positive bias condition modulated the potential of Ge near the collector electrode and enhanced the electron current between the base and collector electrodes. **This was the first solid-state amplifier and named 'transistor' as a contraction of 'trans-resistance'.** The amplification mechanism was different from that of FET, and this transistor is later called 'point-contact bipolar transistor' because both majority and minority carriers contribute the amplification.

3. The Transistor as the Origin of the Device Miniaturization and the World After the Transistor Invention

The point-contact bipolar transistor had soon evolved to the junction bipolar transistors (BJT's) [9], [11], [18] in 1948 in order to prevent the mechanical instability of the contact. Monolithic **integrated circuits started using BJT's in 1958 [19] and 59 [20]. In 1960, the first MOSFET was realized by choosing thermally-grown oxide on Si as the gate oxide [21]** in order to significantly decrease the surface trapped charge density. MOSFETs replaced the BJTs in Large Scale Integrated circuits (LSI's) by the end of 1960's because of the ease of their integration due to the planar structure.

Now, the minimum line width used for nano-CMOS VLSI is about 15 nm. The minimum line width has decreased about 10^5 times since the first vacuum triode in the past 115 years, and $10^{3.5}$ times since the first transistor in the past 75 years, respectively, as shown in the figure. Because of the size decrease, the performance—such as operational speed, energy/power consumption, volume, weight, and cost of electric systems/machines improved billions—trillions of times. The invention of the transistor 75 years ago was the origin of electron device miniaturization, and it was a great technological leap for the progress of intelligent society. Miniaturization of the electron devices towards micro-/nanoelectronics was an extremely important concept. Without the tremendous miniaturization of the transistors in the past 75 years, today's intelligent society with the internet, and AI would not exist.

4. Future of the Transistor

According to IEEE IRDS (International Roadmap for Devices and Systems) 2021, '3 nm' logic CMOS technology will start production this year (2022), and we can still expect the merit in size, operational-speed and power-consumption. It should be noted that the 'logic technology names' such as '5 nm' or '3 nm' are just 'inflated names' and have nothing to do with the real physical size used in the devices. Indeed, it is a bad custom of the logic CMOS industry. Real minimum line width such as the gate length is about 15 nm for the '3 nm technology' according to the IRDS 2021. At this moment, **the downsizing limit of the minimum line width—such as the**

gate length and metal wire width—is thought to be about 10 nm because of the significant increase in leakage current of MOSFETs and resistance increase and reliability degradation of interconnects. So, the scheme of device miniaturization, having continued since the invention of the transistor, could reach the limit in several years. Even if we could solve those problems by the introduction of new materials/technologies, it should be noted that 3 nm is the 'fundamental limit' caused by the direct-tunneling leakage current, and that 0.3 nm is the 'ultimate limit' due to the atomic size. **Thus, there will be no 'pico-technology' after 'nano-technology', and the end of the device miniaturization is not so far.**

However, the progress of the integrated circuits with Moore Law will continue by the 3D integration. In IEDM 2020 and 2021, there were many publications of 3D MOSFETs such as CFETs (Stacked nano-sheet channel n- and p-MOSFETs) [22]. The progress of the 3D integration will reach a limit in 10–20 years because of the increasing heat density and cost increase. However, demands for high-performance semiconductor devices with low-power consumption will keep increasing in the future super-intelligent society, and the technology optimization of the devices for each specific application will continue after that. Future intelligent society will create many new business fields such as 6G communication or autonomous driving, which will require new functions and performances. We will have so many things to do for future logic, memory, telecommunication, power, and sensor devices to optimize for the new businesses.

In the long term, the next leap of technology will be the introduction of bio systems. This does not necessarily mean to introduce the algorism of the bio system on semiconductor devices, but also means to use existing bio systems, and the cooperation between the electronics and bio systems becomes important. Even though the champion player of the 'Go' game cannot win the AI player because the human brain cannot keep concentration only for one thing for long hours without rest and cannot memorize and remember huge volume of data accurately, bio systems such as brains composed by neurons are much efficient than the semiconductor AI system in most of the cases.

Dr. Hiroshi Iwai is a semiconductor device engineer who contributed to the development of LSI technologies at Toshiba, Tokyo Institute of Technology, and NYCU for almost half a century since 1973. He was the IEEE EDS President (2004–2005) and the IEEE Division I Director (2010–11). He is an IEEE Life Fellow, an IEEE EDS Eminent Lecturer and an IEEE IRDS committee member.

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(continued from page 1)

various activities undertaken by the "75th Anniversary of the Transistor Adhoc Committee" with an aim to provide technical information and education to enlighten EDS members. This shall be a mark of tribute to the men and women who have contributed to the Transistor Story—Discovery, Development, and Applications which has had a lasting impact on people's lives and has benefited mankind where it serves good in social relations, caring for the Earth, science, technology, engineering, and economy.

Manoj Saxena
75th Anniversary of the Transistor
Adhoc Committee Chair

SUPERCONDUCTOR ELECTRONIC DEVICE TECHNOLOGY ROADMAPPING WITHIN THE IRDS

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Abstract—For superconductor electronics to meet the needs expected for applications such as quantum computing or large-scale digital computing, significant improvements will be required, especially in circuit density and complexity. Key to improvement are innovations in superconductor devices and logic families. Technology roadmaps are under development to provide goals and timelines.

Index Terms—superconductor electronics, superconductor devices, technology roadmapping, Josephson junctions

I. Introduction

Scaling of CMOS electronics has driven a broad spectrum of applications through increased performance and complexity. The International Roadmap for Devices and Systems (IRDS), which succeeded the International Technology Roadmap for Semiconductors (ITRS) in 2017, does not limit its scope to semiconductor devices. The roadmap drivers now focus on application requirements and include a broader range of non-semiconductor technologies. Within the ITRS, the Cryogenic Electronics and Quantum Information Processing (CEQIP) International Focus Team has published reports since 2018. Superconductor electronics (SCE) is one of three areas specifically covered by the CEQIP team.

Applications of superconductor electronics such as large-scale digital computing could provide benefits such as higher clock frequencies, faster data movement, and lower energy per computation. Neuromorphic computing for large-scale artificial intelligence applications needs energy-efficient solutions and might be a natural fit for superconductor circuits that naturally use pulse-based logic. Quantum computing using superconducting circuits requires operation at temperatures around 10 mK where the energy loss in semiconductor control and interface circuits seems prohibitive at full scale.

However, considering that the largest superconductor computing system built to date has just over one million switching elements, such large-scale applications will require significant increases in overall system complexity. Superconductor electronic circuits in their present forms are unlikely to meet the expected future requirements. New devices, circuits, fabrication processes, and architectures are needed.

A full discussion of the applications, drivers, and technology ecosystem for superconductor electronics is not possible in this short article. For further information, see the latest available IRDS CEQIP report [1]. This article will focus on device developments needed for superconductor electronics.

II. Essentials of Superconductor Electronics

Superconductivity occurs in some metallic materials within limits of temperature, current density, and magnetic field. Superconductor wires have zero resistance for dc electric currents up to some critical

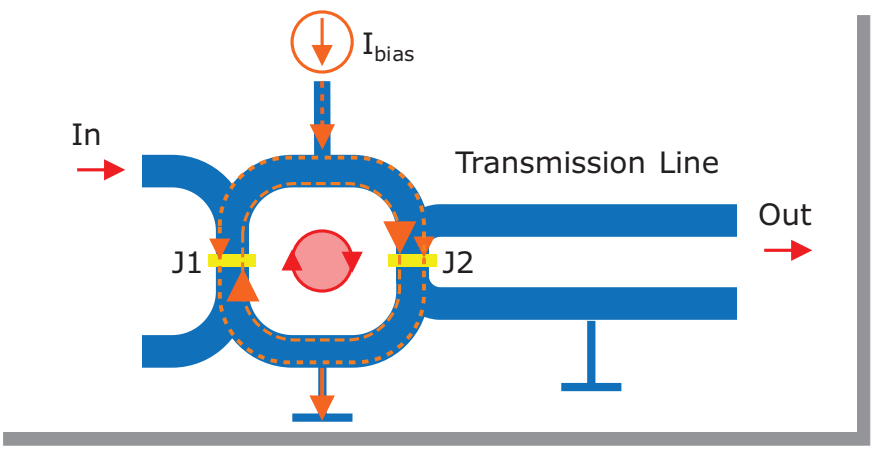

Figure 1. Single flux quantum (SFQ) circuit example: A superconducting loop (blue) with two Josephson junctions (J1, J2) between input and output circuits. Currents in the loop (orange) come from a bias current (I_{bias}, <<<) and a SFQ in the loop (– – –). Note that the sum of the currents passes through J2, whereas the difference of the currents passes through J1. When J2 switches, it transfers the SFQ from the loop to the transmission line, on which it propagates at the speed of light on the line.

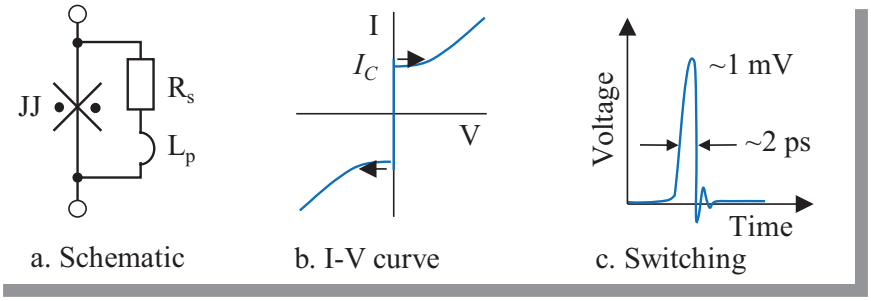

Figure 2. Josephson junction switching element used in SFQ logic. (a) Josephson junction (JJ) with external shunt resistor for critical damping, (b) Current-voltage characteristic, (c) Voltage pulse during switching.

current, I_C, determined by the geometry and properties of the wire.

Current and inductance are important in superconductor circuits, whereas charge and capacitance are important in conventional CMOS circuits, making them significantly different from each other. Fig. 1 shows a simple example superconductor digital circuit.

A Josephson junction consists of two superconducting electrodes connected by a weak link that has a critical current much lower than the electrodes (Fig. 4a). The current through a Josephson junction is a function of the superconducting phase difference across the junction. Common junctions with barrier materials such as aluminum oxide have a sinusoidal relationship, $I = I_C \sin(\varphi)$, so the current is zero when there is no phase difference. The nonlinear current-phase relationship is a feature exploited by devices such as qubits.

An important superconductor circuit element, the critically damped Josephson junction (JJ), is shown in Fig. 2. Increasing the current above I_C causes the junction to leap forward in phase by 2π, which produces a voltage pulse across the critically damped JJ that integrated over time equals a flux quantum Φ_0 = 2.07 mV·ps. Feeding a baby is analogous to how Josephson junctions operate: A small stream of drink is no problem, but exceeding some maximum rate causes the baby to spit up, in the case of Josephson junctions, one flux quantum at a time.

Single flux quantum (SFQ) logic uses the presence of a flux quanta to signifpy a digital '1'. The voltage pulses generated by junction switching cause flux quanta to move between loops in a circuit. If the current generated in the loop by the flux quantum $I = \Phi_0/L$ is greater than the critical current of a JJ in the loop, the JJ switches, removing the flux quantum from the loop. If the loop inductance is sufficiently large that no critical currents are exceeded, the flux quantum can remain in the loop. Switching pulse widths are on the order of picoseconds, allowing simple circuits to operate at clock frequencies exceeding 100 GHz.

Challenges of Josephson junctions include low gain. Fan-out greater than one requires the use of splitters, typically using 3 JJs to make a 1:2 splitter. Leakage currents can be a problem unless current flows are carefully balanced or resistors are used to isolate subcircuits. Currents and inductances are interdependent, which makes the design of even moderately complex circuits difficult without good electronic design automation (EDA) tools.

III. Devices and Circuits

One driver for improved circuits and devices can be seen by comparing the CMOS NAND2 gate with the MAJ-3 adiabatic quantum flux parametron (AQFP) gate. AQFP is one of several superconductor electronic logic families. Fig. 3 shows that the area of the superconductor gate set was roughly 25,000 times larger in 2020. Even comparing the areas at an equivalent feature size of 350 nm, the area is about 60 times larger, indicating that reductions in feature size alone will not be sufficient.

While every superconductor logic family is different, a few approaches to reducing circuit area are broadly applicable.

1) Inductors
   a) Decrease wire width

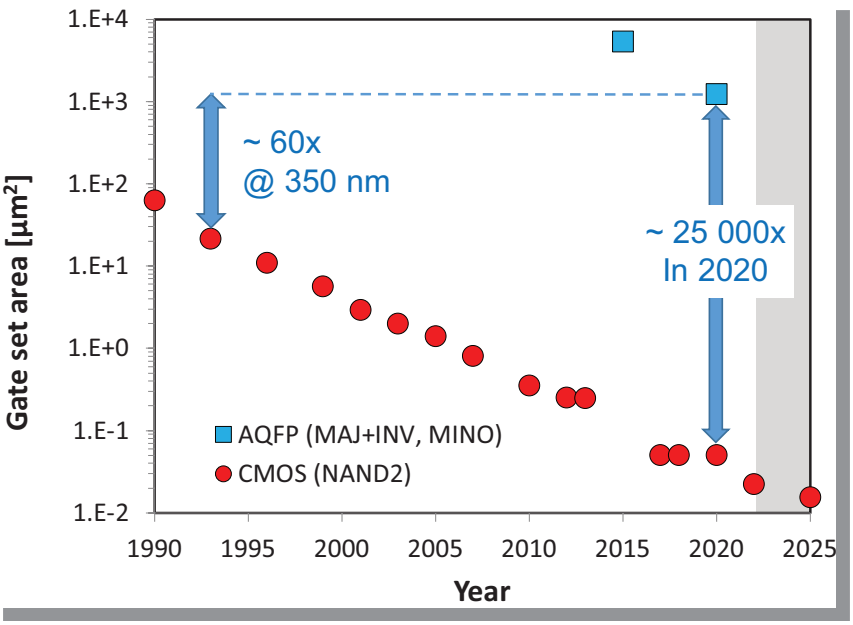

Figure 3. Gate set areas for CMOS and AQFP, a superconductor logic family. The comparisons are at 2020 and at minimum feature sizes of 350 nm.

b) Multiple wiring layers
c) High kinetic inductance materials
d) Transformers: avoid, if possible

2) Josephson junctions
a) Increase critical current density, J_c
b) Resistive weak link to avoid shunt resistors
c) Multiple junction layers
d) Phase-shift junctions to reduce inductors and bias currents

3) Interconnects
a) Narrower transmission lines, which require higher J_c junctions to drive the increased impedance
b) Striplines with decreased dielectric thicknesses to decrease impedance

Following are some superconductor devices, roughly in chronological order of need.

A. Improved Nb Josephson Junctions (0-Junctions)

Improvements are needed in standard Josephson junctions fabricated with insulating barriers. Consider the current process for fabricating Nb/Al-AlO_x/Nb 'trilayer' junctions. Niobium deposited on the bottom layer forms columnar grains with surface roughness of several nanometers, which is significant as the insulating barrier layer is only about 1 nm thick. An aluminum layer deposited on top of the lower Nb electrode greatly smooths out the surface, but Al is not superconducting at typical operating temperatures (~4 K), so the thickness variation contributes to tunneling current density variation across the junction. The Al layer is oxidized in a controlled atmosphere, typically at room temperature, before deposition of the Nb top electrode. The resulting amorphous aluminum oxide barrier has both structural and compositional defects that affect the conductivity over nanometer length scales. Supercurrent tunneling depends exponentially on barrier conductivity, which accentuates small variations.

Sputter deposition of Nb can't fill gaps smaller than about 100 nm. The superconducting properties of Nb are also sensitive to stress and to poisoning by oxygen or hydrogen, limiting fabrication temperatures to below about 180 °C, far below the ~400 °C temperature limit for CMOS processing at the back end of the line. A consequence is that standard CMOS processes require performance-limiting modifications for use with Nb junctions. SiO_2 deposited at low temperatures contains H and OH that comes out if heated too much. After etching to define the junction, wet anodization of the Nb is sometimes performed to seal the barrier region from contamination, although this is not a standard semiconductor foundry process.

Producing junctions with critical current variations less than 1% has been difficult for junctions with critical current densities greater than 100 μA/μm^2 and diameters less than about 1 μm. Junction critical currents must be about 100 μA at 4 K due to noise considerations. Combined, these constraints have limited minimum junction diameters to roughly 1 μm. Shrinking junction sizes would require greater control over formation of the barrier layer to achieve both higher critical current density and lower variation, which might be possible even with aluminum oxide barriers.

Replacing the barrier layer with a thicker, resistive material is an alternative and has the advantage of providing junctions that do not require shunt resistors, which often require more area than the junction itself [2]. Barrier replacement requires development of a process capable of yielding predictable, uniform, and stable properties using materials compatible with the Nb superconductor.

B. NbN or NbTiN Josephson Junctions (0-JJ)

NbN or NbTiN are superconductor materials that might be able to replace Nb. They can be fabricated with lower surface roughness and critical temperatures T_c > 9 K for layers deposited on a compatible buffer layer and with film thickness greater than about 20 nm. Epitaxial NbN layers and junctions have been demonstrated recently [3], [4] and should reduce variations.

The primary challenge has been development of a compatible junction barrier with predictable, uniform, and stable properties. Development of processes suitable for 300 mm wafer fabrication will require additional time and effort. Another challenge is that most NbN film deposition uses reactive sputtering, which has difficulty filling gaps below about 250 nm. Chemical vapor deposition (CVD) or atomic layer deposition (ALD) are suitable for 300 mm fabrication and are better able to fill small gaps, but they can be more susceptible to superconducting property degradation due to contamination.

C. Passive Transmission Lines (PTL)

Transmission lines like the one shown in Fig. 1 allow pulses to move with very low loss or dispersion at the speed of light on the line, typically about c/3 for Nb striplines. Such transmission lines provide data movement capability that could be a significant advantage for superconductor electronics.

A challenge is that the center conductor must be about 4 μm wide using present Nb stripline and junction technology [5]. More compact transmission lines are needed.

D. Phase-shift devices

Current supplied to SCE circuits is commonly used to both compensate for energy dissipated and to shift superconducting phase differences within the circuit. The phase shifts bias Josephson junctions in the circuit to control the direction of travel for flux quanta. Superconductor phase engineering is an important part of SCE circuit design without analogy in CMOS circuit design.

Phase shift elements set or change the superconducting phase φ between locations in a superconducting circuit. The phase difference across an inductor is given by $\varphi_L = 2\pi IL/\Phi_0$, where I is the current, L is the inductance, and Φ_0 is the magnetic flux quantum. Using an inductor to provide a phase difference involves a tradeoff between inductance and current. Large inductances can require too much circuit area, whereas large dc external currents can become difficult to supply without creating magnetic fields that affect circuit operation. For example, with an average junction critical current I_C = 200 μA and bias of 0.7 I_C = 140 μA, a chip with just one million junctions would require a bias current of 140 A! Even at a typical 2.6 mV dc supply voltage, such large currents create significant problems.

Alternating currents (ac) can provide bias currents to many more junctions but require transformers or capacitors to supply current to subcircuits. Transformers rely on magnetic coupling, which does not scale to small sizes, and capacitors add another device type.

Phase-shift devices that do not require provision of a continuous supply current include persistent current loops [6] and phase-shift junctions. Junctions with a magnetic barrier material (Fig. 4c) can have a current-phase relationship that is shifted by π radians, thus the name pi-junction (π-JJ), with $I = I_C \sin(\phi - \pi) = -I_C \sin(\varphi)$. The energy-phase relation (EPR), $E/E_{J0} = \cos(\varphi) - 1$, has minima at $\pm\pi$ and provides a stable phase shift current within a superconducting loop that can include regular Josephson junctions (0-JJs). Junctions with phase shifts other than π are called anomalous Josephson junctions, φ_0-JJs, or ψ-JJs [7]. Other phase relationships such as $I = I_C \sin(2\varphi)$ might be achievable with devices like the composite junction shown in Fig. 4d.

Advantages of using such phase-shift devices include reduced external current supply to the chip, reduced power distribution network area, and improved operating margins due to the stability of the current [8]. In AQFP logic, π-JJs can completely eliminate the large output transformers [9].

A challenge is that the current direction generated by a single π-JJ is undetermined. One approach is to design loops to work with current flow in either direction, for example by replacing a single, resistively shunted junction with a loop containing two unshunted junctions and a π-JJ [10]. Another approach is to design connecting loops such that the currents are constrained to flow in one direction. A junction with a set polarity could be better, if fabricable.

Other challenges include incorporation of magnetic materials in commercial fabrication processes and the need for an additional junction layer with the different barrier material.

E. Memory Elements

Using Josephson junctions to make memory cells has advantages and disadvantages similar to CMOS SRAM. However, the device count for a JJ memory cell is even higher and the density is much lower. Needed is memory with significantly higher storage density and access times not too much lower than all-JJ memories.

One example is the spin-valve Josephson junction (SVJJ) shown in

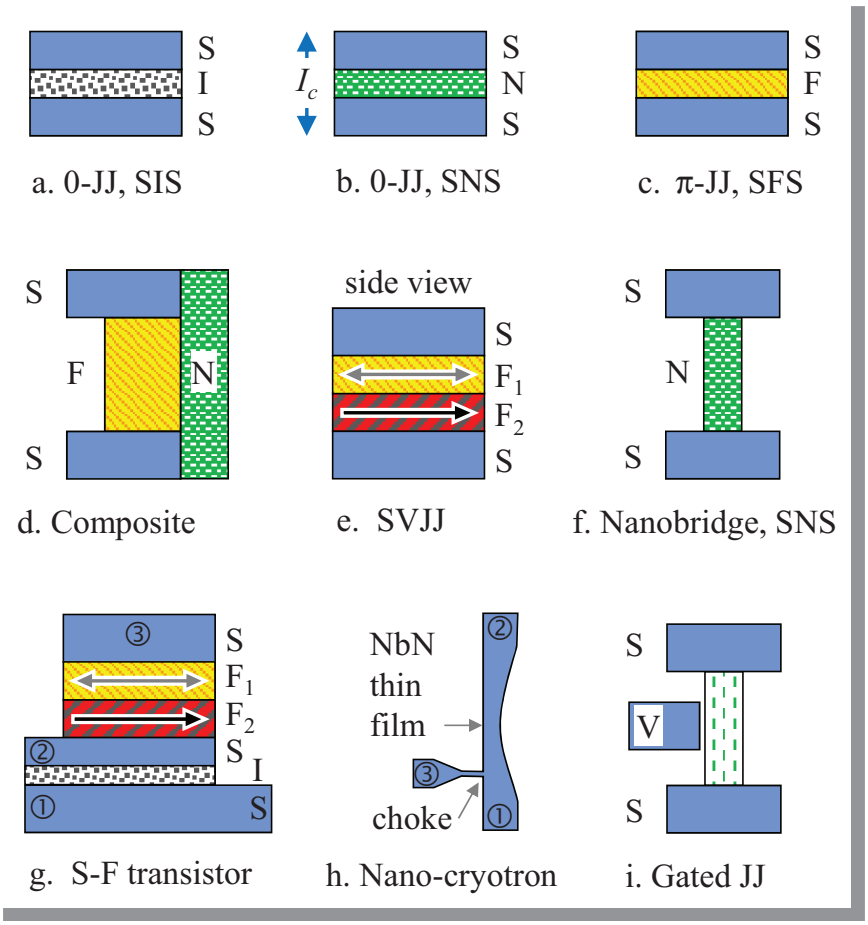

Figure 4. Superconductor (S) switching devices. (a) 0-JJ: Josephson junction with insulating (I) barrier, (b) 0-JJ: Josephson junction with normal metal (N) barrier, (c) π-JJ: Josephson junction with a ferromagnetic (F) layer creating a π phase shift, (d) Composite: junction with SFS and SNS in parallel, (e) SVJJ: spin valve Josephson junction, (f) Nanobridge junction, (g) S-F transistor: SVJJ on top of an SIS junction, (h) Nano-cryotron with 3 terminals, (i) Gated JJ: Nanobridge with voltage (V) applied to a third electrode.

Fig. 4e, which contains a hard magnetic reference layer and a soft magnetic layer switchable by magnetic fields provided by superconducting control lines. The critical current of the SVJJ is higher when the two F layers are magnetized in opposite directions.

The IRDS CEQIP report includes several other memory elements under development or consideration [1].

F. Weak Link Junctions

Shrinking the size of Josephson junctions below 90 nm might require significantly different devices. Josephson junctions can be produced using weak links in a variety of forms including nanobridges between the superconducting electrodes (Fig. 4f) [11]. The materials are typically metals or even superconductors weakened by the small size. Dimensions of conductive nanobridges must be on the order of the superconducting coherence length in the bridge material, which is ~40 nm for Cu in close proximity to a strong superconductor, ~10 nm for Nb thin films, and ~5 nm for NbN or NbTiN.

Multi-layer or exotic materials might provide improved nanobridge properties. For example, topological insulators have conducting surface or edge states that might be less sensitive to dimensional variations.

Challenges include interfacial effects in composite junctions (e.g., SNS), sensitivity to operating temperature, additional materials (if required), and fabrication on nanometer scales with adequate control of variation.

G. Multi-terminal switching devices

Both JJs and quantum phase-slip junctions (QPSJs) are two-terminal devices, which require more components to perform typical logic functions. Multi-terminal superconductor switching devices might reduce device count and increase circuit density. One approach is to stack a spin-valve junction on top of a regular Josephson junction to make a JJ transistor (Fig. 4g). Another approach uses nano-cryotrons with three or four terminals (Fig. 4h). Challenges include fabrication process complexity and development of new logic families.

Recent discovery of a control effect in superconducting devices [12] could lead to development of multi-terminal, gated JJs (Fig. 4i). Challenges include reduction of the switching voltage to a level compatible with the overall circuit, avoidance of supercurrent tunneling from the control electrode, and development of a new logic family.

H. Quantum Phase-Slip Junctions (QPSJ)

QPSJs are a dual to Josephson junction devices with the roles of phase and charge interchanged as well as current and voltage devices [13]. QPSJs have a critical voltage, V_C, above which an electron pair tunnels through the junction. A charge island consisting of two QPSJs and a capacitor is the main element in QPSJ-based logic circuits. Different connections between charge islands can be used to make different logic gates. Advantages of QPSJs relative to JJs include voltage control and far less sensitivity to magnetic fields. Nanowire QPSJ devices also might have some fabrication advantages over Josephson junctions, although fabrication experience with NbN nanowires indicates that challenges remain, particularly in device variability and operating temperature.

IV. Technology Roadmapping

The development of superconductor electronic systems is an example of an open innovation technology funnel (Fig. 5). New approaches enter, die, recombine, spin off, and some pass to the next level. Technology roadmapping activity is an inverse funnel, becoming more detailed and specific as systems requirements become clearer and the component technologies mature. The process is aided by models and figures of merit (FoM). See [14] for a recent and open access article on the process of technology roadmapping in the face of evolving applications and emergent technologies.

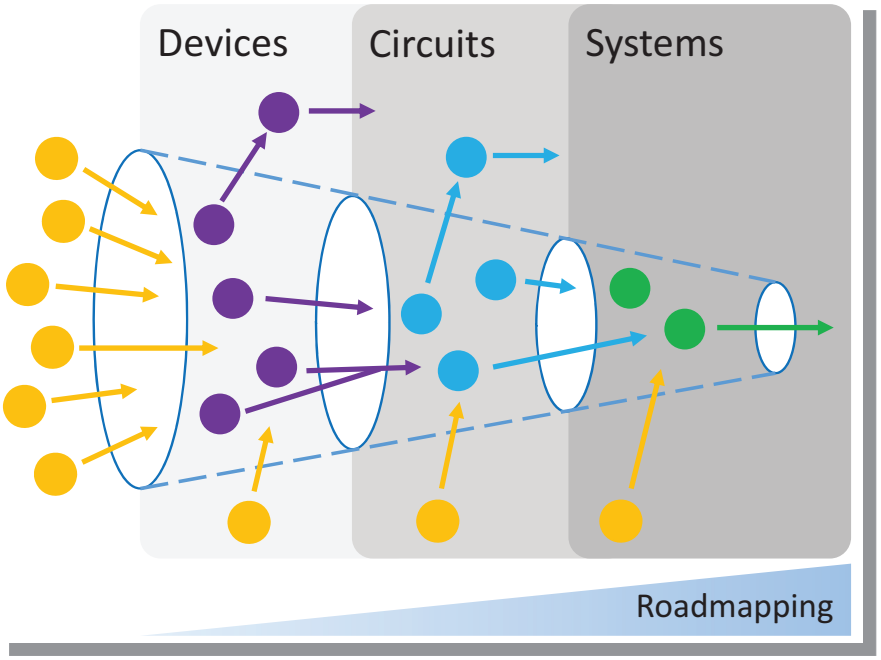

Figure 5. Open innovation technology funnel.

V. Conclusion

The technology roadmapping process for applications that might use superconductor electronics started with the identification of roadblocks and needs. Identification of superconductor devices, circuits, and technologies that might contribute to solutions is in progress. The next step is to model and evaluate candidates against figures of merit and to develop timelines. The effort is a volunteer IEEE activity open to those interested in contributing.

Acknowledgements

IRDS CEQIP team members since 2018 have contributed to the reports that form the base for this article. Special thanks to Anna Herr, Pascal Febvre, Igor Soloviev, and George Tzimpragos for discussing, reading, and editing this article.

D. Scott Holmes (M 2010–SM 2012) received the B.S. degree in mechanical engineering from the Massachusetts Institute of Technology in 1979, M.S. degrees in materials science and in nuclear engineering from the University of Wisconsin–Madison in 1986 and a joint Ph.D. in materials science and nuclear engineering & engineering physics from the University of Wisconsin–Madison in 1989.

From 1990 to 1999 he was a Senior Engineer/Scientist with Lake Shore Cryotronics. From 1999 to 2010 he was a Learning Strategist with Talsico, LLC. From 2010 to 2019 and 2020 to present he has been a Lead Technologist with Booz Allen Hamilton in the Washington, DC area. During 2019 he was a Program Manager at DARPA in the Microsystems Technology Office.

Dr. Holmes is a member of the IEEE Council on Superconductivity as a representative of the Electron Device Society and chairs the Cryogenic Electronics and Quantum Information Processing (CEQIP) International Focus Team (IFT) for the International Roadmap for Devices and Systems (IRDS).

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2021 IEEE Semiconductor Interface Specialists Conference (SISC)

William Vandenberghe

The 52nd IEEE Semiconductor Interface Specialists Conference (SISC) was held on 8–11 December, 2021 in a hybrid format with on-site presentations at the Bahia Resort Hotel, San Diego, CA, alongside virtual presentations and recordings. The virtual participants were able to tune in live and watch on-demand recordings. Despite the difficulties imposed by the COVID-19 pandemic and the start of the omicron surge, the 52nd SISC was a big success with a total of 53 on-site and 71 virtual attendees.

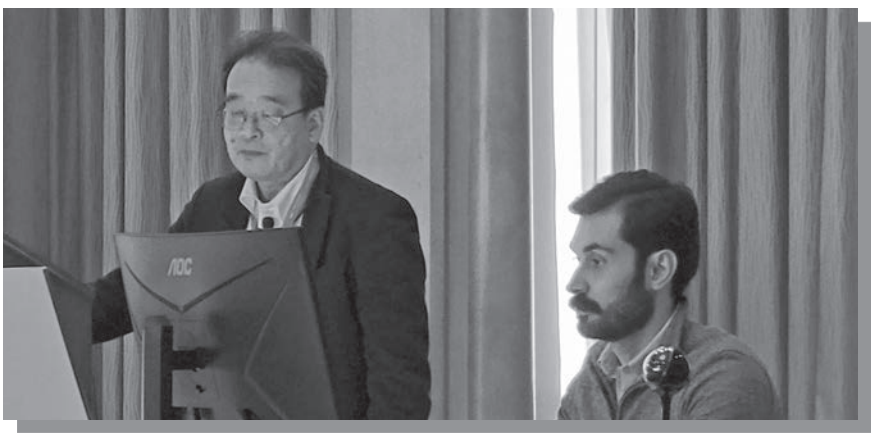
The meeting started with a Wednesday evening on-site tutorial by Prof. Robert (Bob) Wallace from the University of Texas at Dallas. A long-time participant and authority in the SISC community, Prof. Wallace educated the SISC audience on "Physical Characterization of Advanced Device Materials". Prof. Wallace gave an overview of the wide range of surface characterization techniques that are available and outlined the detection limits of various techniques.

After the tutorial, the conference continued with 43 contributed papers and 51 posters presented in 13 sessions. A total of 11 invited speakers gave an overview of the state-of-the-art in power electronics, atomic-layer deposition, III-V semiconductors, ferroelectrics, and oxide electronics.

Unfortunately, in 2021 Prof. T.P. Ma and Prof. Mark Reed, two highly esteemed members of the IEEE community and very frequent attendees of the SISC conference, passed away. SISC had two special sessions in their respective honor with three invited speakers in each. In the T.P. Ma session, chaired by Prof. Wallace, Prof. Alan Seabaugh from the University of Notre Dame, Prof. James Tour from Rice University, and Barry Merriman from Roswell Biotechnologies paid homage to Mark Reed and his legacy in Nanoelectronics and Molecular Electronics. The T.P. Ma session was chaired by a former

SISC tutorial presented by Prof. Wallace (at the podium) from the University of Texas at Dallas

IBM's Huiming Bu presents in the "Tribute to TP" Ma session



UT Dallas Ph.D. student Ali Saadat (right) operating the main conference computer and presenter Dr. Yasuo Cho from Tohoku University, Japan (left)

SISC's annual limerick contest hosted by 2019 SISC Limerick contest winner Dina Triyoso (right front)

T.P. Ma student and the 2021 SISC general chair: Prof. Wenjuan Zhu from the University of Illinois Urbana-Champaign. Dr. Huiming Bu from IBM, Dr. An Chen from the Semiconductor Research Corporation (SRC), and Prof. Peide Ye from Purdue University paid tribute to T.P. Ma.

To manage the interaction between the on-site attendees and the virtual attendees, Mr. Ali Saadat, a Ph.D. candidate from the University of Texas at Dallas operated the main conference computer. Ali had to rapidly switch between on-site presentations, remote presentations, and recordings. He had to ensure that for all three presentations modes, on-site and remote participants could see the slides, hear the audio from on-site presenters, hear the question and answers, and broadcast the two cameras capturing on-site activities. Ali's task became even more interesting when on Thursday morning, no internet was available at the Bahia Hotel and the conference had to run through a hotspot!

With the sizeable on-site attendance, SISC was able to bring back its limerick contest in 2021. The limerick contest is a long standing tradition at SISC and was hosted by the SISC 2019 Limerick contest winner, Dr. Dina Triyoso from Tokyo Electron Ltd. The 2018 Limerick contest winner Prof. Paul Hurley put up a strong limerick again lamenting the absence of the SISC hospitality suite this year

Back to SISC were we all meet
And after a banquet that's such a great treat
Now to discussions that are quicker
And slicker with liquor
Hey! ... Where's the hospitality suite?

but ultimately after long deliberation, UC San Diego Ph.D. student Aaron McLeod won with

The largest question of them all:
Why is your font that small?
The attendees are blind
And we're running behind
Please, dear god, pass the Tylenol

A best student paper was established in 1995 in honor of Prof. E.H. Nicollian and the winner of the 2021 SISC Ed Nicollian Award is Nujhat Tasneem from Georgia Institute of Technology. The winner of a new award, instituted in honor of Prof. T.P. Ma, the 2021 T.P. Ma Award for Best Student Poster goes to Simon Mellaerts from KU Leuven.

The 2021 Executive committee consisted of Ex-Officio John Robertson from Cambridge University, General Chair Wenjuan Zhu from the University of Illinois, Technical Program Chair William Vandenberghe from the University of Texas at Dallas, and Arrangements Chair Peide Ye from Purdue University.

William Vandenberghe
2021 Technical Program Chair
Associate Professor
Department of Materials Science and Engineering
University of Texas at Dallas

The 2022 IEEE VLSI Symposium on Technology & Circuits, Now Merged as a Single Event With the Theme: Technology & Circuits for the Critical Infrastructure of the Future

Now in its 42nd year of delivering a unique convergence of technology and circuits for the microelectronics industry, the Symposia on VLSI Technology & Circuits will be merged into one Symposium to maximize the synergy across both domains. The newly merged 2022 IEEE VLSI Symposium on Technology & Circuits is organized around the theme: "Technology & Circuits for the Critical Infrastructure of the Future." The five-day hybrid event, combining both live sessions onsite at the Hilton Hawaiian Village, as well as on-demand access to selected presentations, is scheduled for 13–17 June 2022 in Honolulu, Hawaii. The Symposium will feature advanced VLSI technology developments, innovative circuit design, and the applications they enable, such as artificial intelligence, machine learning, IoT, wearable/implantable biomedical applications, big data, cloud / edge computing, virtual reality (VR) / augmented reality (AR), robotics, and autonomous vehicles.

The week-long Symposium will continue its reputation as the microelectronics industry's premiere international conference integrating technology, circuits, and systems with a range and scope unlike any other conference. In addition to the technical presentations, the Symposium program will feature a demonstration session, evening panel discussions, joint focus sessions, short courses, workshops, and a special forum session that provides a focused discussion on a specific topic relevant to the Symposium theme.

Short Courses on Key VLSI topics

- Monolithic & Heterogeneous Integration
- Advances in Application-Specific Computing Systems & Technologies
- Electronics That Drive the Next Generation Smart Car

Plenary Sessions

- "Holistic Patterning to Advance Semiconductor Manufacturing for the 2020s and Beyond," by Martin Van den Brink, President & CTO, ASML
- "Semiconductor Innovations, from Device to System," by Yuh-Jier Mii, Senior Vice President for R&D TSMC
- "From System-on-Chip (SOC) to System on Multichip (SoMC) Architectures: Scaling Integrated Systems Beyond the Limitations of Deep-Submicron Single Chip Technologies," by Chris Patrick, Senior Vice-President, Qualcomm
- "The Rise of Memory in the Ever-Changing AI Era – From Memory to More-Than-Memory," by Seok-Hee Lee, President & CEO, SK Hynix

Focus Sessions include BEOL processes, new concepts for transistor scaling, 6G, compute-in-memory, biomedical technology, and 3D heterogeneous integration.

In addition, three **Evening Panel Sessions** have been announced:

- "What Will It Take To Bring New Material From Lab To Manufacturing?"
- "Building The 2030 WorkForce: How to Attract Great Students And What to Teach Them"
- "Supply Chain & Foundry Future"

The Symposium program also features a multi-speaker **Forum Session** on "VLSI for Infrastructure and Infrastructure for VLSI."

A series of workshop sessions will be held during the Symposium program to provide additional learning opportunities for participants:

Technology Workshops

- Heterogeneous Integration – The Next Scaling Frontier: Material & Process Challenges
- Machine Learning Applications in Semiconductor Processes and Equipment Development

Circuit Workshops

- The Emerging Ecosystem of Open-Source Chip Design
- Analog/RF Circuits for IoT
- Recent Advances in Radar, mmWave, and Sub-THz: Technology, Packaging, & Circuits

Joint Workshop

- Cryogenic Electronics for Quantum Computing

Special events at the Symposium include mentoring events for Women in Engineering and Young Professionals, sponsored by the IEEE Electron Devices Society and the Solid State Circuits Society.

Best Student Paper Awards for each track Symposium are chosen based on the quality of the papers and presentations. The recipients will receive a monetary award, travel cost support, and a certificate. For a paper to be reviewed for this award, the lead author and presenter of the paper must be enrolled as a full-time student at the time of submission, and must indicate on the web submission form that the paper is a student paper.

Further information about the Symposium is available at: http://www.vlsisymposium.org.

Sponsoring Organizations

The IEEE VLSI Symposium on Technology & Circuits is sponsored by the IEEE Electron Devices Society, in cooperation with the IEEE Solid-State Circuits Society and Japan Society of Applied Physics, in cooperation with the Institute of Electronics, Information and Communication Engineers.

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The fourth edition of the IEEE Latin American Electron Devices Conference, LAEDC 2022, is a three-day meeting to be held in Cancún, México from 4–6 July in a hybrid format with both in-person and virtual options that will enable participants from all over Latin America and other geographies to attend at low cost.

LAEDC is an international and flagship conference sponsored by the IEEE Electron Devices Society (EDS) in Latin America, that provides a unique global opportunity to bring together specialists, senior scientists, students as well as young researchers to share and discuss their latest research and innovations in all Electron Device related fields. Proceedings will be published by IEEE and the accepted papers will be available on IEEE Xplore. The best papers presented at the conference will be considered for publication in a special issue of the *IEEE Journal of the Electron Devices Society*.

Continuing with the tradition of the past editions, the 4th IEEE LAEDC will be covering technical areas including all electron-based devices, electron devices for quantum computing, RF-MMW-5G, semiconductor, MEMS and Nanotechnologies, packaging-3D integration, sensors and actuators, display technology, modeling and simulation, reliability and yield, device characterization, biomedical devices, circuit-device interaction, novel materials and process modules, technology roadmaps, electron device engineering education, electron device outreach, optoelectronics, photovoltaic and photonic devices and systems, energy harvesting and will also have a strong component of technology based Humanitarian Projects and STEM.

For more information, please contact laedc@ieee.org | https://attend.ieee.org/laedc-2022/

Fernando Guarin
IEEE Fellow
EDS Senior Past President

49th IEEE Photovoltaic Specialists Conference (PVSC), Philadelphia

It is with distinct pleasure and anticipation that you are invited to join the 49th IEEE Photovoltaic Specialists Conference on 5–10 June in Philadelphia at the spectacular Pennsylvania Convention Center. For 60 years, PVSC has been the premier scientific and technical conference focused on all areas of photovoltaics from fundamental science to commercial applications and, increasingly, to deployment, policy, and resources. The PVSC is strongly committed to creating an inclusive, respectful conference environment that welcomes participation from people of all races, ethnicities, genders, ages, abilities, religions, and sexual orientations because we are more innovative and enriched when we reflect the diversity of our photovoltaics and broader community.

Technical Program: We continue that tradition by offering a diverse technical program divided into eleven areas and featuring several special and joint technical sessions highlighting our cross-cutting synergies. We will have a slate of exciting keynote, plenary and invited speakers giving up-to-date research summaries and breakthroughs. A day dedicated to tutorials from leading experts in seminal areas will enable students and scientists joining the field or any participants to expand their knowledge to new areas. The conference will also include several exciting cross-cutting themes and joint areas such as "Advanced Resource Management for 100% Renewable Electricity", "Hybrid Tandem/Multijunction Solar Cells" and "Challenges and opportunities on grid and microgrid integration of PV systems".

New this year: Publication of a conference proceeding will be optional. Full papers are encouraged but short abstracts will otherwise be used as the publication of record. Authors will have the option of submitting their evaluation abstract or a longer conference proceeding by the 31 May 2022, publication deadline. Exceptional submissions will be recommended for expedited review and publication in the *IEEE Journal of Photovoltaics*. Also, we have merged former Technical Areas on III-V and on space in new Technical Area 3 on III-V, Space and Concentrator Photovoltaics.

If you would still like to contribute technically, please submit your abstract before our late submissions deadline on 8 April 2022.

Venue & Hotel: The conference will be held at the Pennsylvania Convention Center in the heart of Philadelphia. The exhibits area will provide a chance to learn about some of the latest developments in characterization, materials and manufacturing. All these events will be enhanced by ample opportunities for networking to form new collaborations and friendships as well as renew old acquaintances. For accommodation, plenty of rooms are reserved in the Marriott Philadelphia Downtown Hotel conveniently connected to the Convention Center. The Hotel has all the amenities you want from a conference hotel to allow networking including extra meeting and gathering sites. Its location in Center City puts the conference within walking distance of countless great restaurants, museums and, yes, historical sites.

Awards: We will be presenting the awards for the prestigious William R. Cherry Award, along with the Stuart R. Wenham Young Professional Award. We will also present awards for Best Student Presentation and the Best Poster Award. Additionally, to encourage and invest in the next generation of photovoltaic researchers, engineers and specialists, middle and high school competition for students around the world and of all ages (4th to 12th grade) will be held.

On behalf of all the dedicated volunteers who comprise the PVSC Organizing, Cherry, and International Committees, we look forward to personally welcoming you to Philadelphia for the 49th IEEE PVSC. Further details and registration can be found at: https://ieee-pvsc.org/PVSC49

Bill Shafarman
49th IEEE PVSC Chair

2022 IEEE International Interconnect Technology Conference (IITC)

HTTPS://IITC-CONFERENCE.ORG/

We are excited to announce the 25th edition of IITC sponsored by the IEEE Electron Devices Society as the premier conference for advanced interconnect technology devoted to leading-edge research in the field of advanced metallization and 3D integration for ULSI applications.

IITC 2022 will be held in a hybrid format 27–30 June 2022 in San Jose, California. Given the international nature of the interconnect research community, IITC is organized sequentially in Asia, Europe and North America. The conference was held last year in the historic city of Kyoto, Japan and in 2022 it will return to the west coast of the United States. We are tentatively planning to proceed with a traditional in-person conference in San Jose with an option to attend virtually for those who may be subject to pandemic-related travel restrictions. On-demand content will be available.

The conference presents various talks, papers and posters covering innovative research and development in all areas of research related to BEOL/MOL/3D interconnects, including design, unit process, integration, reliability and packaging. This conference attracts professionals from industry, academia and national laboratories in semiconductor processing, interconnect design and equipment development.

Workshop

Prior to the technical program, a workshop focused on "Advanced Packaging and 3D Integration" will be held on Monday, 27 June. We plan to have seven industry experts give technical presentations covering the latest progress in the field of packaging and 3D integration.

For more information, please visit the IITC 2022 website at https://iitc-conference.org/ The IITC committee members look forward to seeing you either virtually or in-person at IEEE IITC 2022!

Hui Jae Yoo, Intel
2022 IITC General Chair

MILAN 2022
ESSDERC
ESSCIRC

52nd European Solid-State Device Research Conference and 48th European Solid-State Circuits Conference

The aim of ESSDERC and ESSCIRC is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits. The level of integration for system-on- chip design is rapidly increasing. This is made available by advances in semiconductor technology. Therefore, more than ever before, a deeper interaction among technologists, device experts, IC designers and

system designers is necessary. While keeping separate Technical Program Committees, ESSDERC and ESSCIRC are governed by a common Steering Committee and share Plenary Keynote Presentations and Joint Sessions bridging both communities. Attendees registered for either conference are encouraged to attend any of the scheduled parallel sessions, regardless to which conference they belong. In 2022, ESSDERC and ESSCIRC will be held 19–22 September 2022, at the University of Milan-Bicocca (Milan, IT), that is well connected (metro, bus, train) with Milan downtown. The conference will provide a balanced mix of keynote and plenary talks, device circuits and joint sessions with prestigious invited speakers, workshop and tutorials, exhibits, and technical presentations. Camera-ready four-page papers are due by 12 April 2021. Papers presented at the conference will be considered for the "Best Paper Award" and "Best Young Scientist Paper Award". The selection will be based on the results of the paper selection process and the judgement of the conference participants. The 2022 Award Ceremony will take place during ESSDERC/ESSCIRC 2023.

ESSDERC and ESSCIRC have evolved over the last years to follow recent R&D device, circuit and system fast-growing topics. Besides the traditional ESSDERC and ESSCIRC tracks, a number of JOINT tracks have been introduced, to encourage and facilitate interactions between circuit, system and device researchers.

ESSDERC/ESSCIRC encourages submissions in all areas of solid-state devices, circuits and systems, **with special emphasis on**: Analog, Power and RF Devices – Electron Device Simulation and Modelling - Advanced Technology, Processes and Materials - Neuromorphic Computing, Advanced Memories, AI Accelerators, in-Memory-Computing, Security – Advanced Computing Devices and Circuits: Advanced CMOS, Post-CMOS, Quantum Computing – Sensors, MEMS, Bioelectronics, Biomedical Electronics, Optoelectronics, Display and Imaging – Analog Circuits – Data Converters – RF and mm-Wave Circuits - Frequency Generation – Wireless and Wireline Interfaces – Integrated Power Electronics and Power Management – Digital Circuits & Systems

Conference Highlights and Opportunities

4 joint keynote presentations
3 ESSDERC keynote presentations
3 ESSCIRC keynote presentations

Invited papers with overall coverage of all aspects of advanced devices and circuits

Presentation of IEEE and ESSDERC/ESSCIRC Awards

ESSDERC/ESSCIRC Welcome Reception on Tuesday, 20 September 2022
ESSDERC/ESSCIRC Gala Dinner on Wednesday, 21 September 2022

Tutorials and Workshops

For the call for papers and other information, visit the ESSDERC and ESSCIRC 2022 website at www.esscirc-essderc2022.org and join the ESSCIRC – ESSDERC LinkedIn group.

The **ESSXXRC** 2022 committee members look forward to seeing you in Milan, Italy!

Andrea Baschirotto
2022 ESSXXRC General Chair
University of Milan-Bicocca

Society News

From the Desk of the President....

Ravi Todi PhD
IEEE Fellow
EDS President

Dear Electron Devices Society colleagues,

I am most pleased to inform you of upcoming plans to conduct a Strategic Planning Workshop. The results will play a significant role in the continuous quest of the Society to achieve ever higher levels of excellence. We strive to be an indispensable resource for those who want to achieve success in our field. We exist for the benefit of our members and for our profession as well as for the greater good of humanity. Some of you may remember that four years ago we engaged in a similar initiative which produced, among other things, four strategic goals which we have striven to use in guiding us in how we develop and resource programs for your benefit. We intend to build upon these to quicken the pace to becoming a stellar Society in IEEE and a magnet for new members because of the value we create for you.

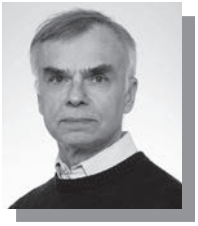
The Workshop will be structured in three parts. (1) Where are we now? (2) Where do we want to be in 2032? (3) How will we get there?

The output of the Workshop will be presented to the Board of Governors in the form of recommendations for action and will be made public in a subsequent Newsletter Issue. The recommendations will include a statement of our vision for EDS in 2032, a statement of our core values, a list of strategic goals and most importantly a recommendation for a deployment plan. Included in the deployment plan will be a short list of Key Performance Indices (KPIs) which will be quantitative, will be reviewed regularly and will be owned by members accountable for results. This will be one of the means used for driving initiatives aimed at realizing our vision and converting our strategic goals into action.

In keeping with our tradition of coordinating our Board of Governors Meeting with a major conference, we will be tentatively holding the summer meeting on June 12 prior to and in conjunction with the *2022 IEEE Symposium on VLSI Technology and Circuits* set for June 12–17. The Strategic Planning Workshop will be on June 10–11 and will precede the Board Meeting. The Workshop participants will be a select group of past, present, and future leaders of the Society. All other EDS members are invited to observe the deliberations if you find yourself in this locale on these dates. But whether you are attending or not we will be soliciting your inputs. Comments or questions are welcome and can be submitted to *eds@ieee.org.*

Ravi Todi PhD
IEEE Fellow
EDS President

Message from EDS Newsletter Editor-in-Chief



Daniel Tomaszewski
EDS Newsletter
Editor-in-Chief

Dear Readers, Members of the IEEE EDS Community,

Welcome to the IEEE EDS Newsletter issue April 2022.

First of all I would like to express our great concern and warmest greetings to people, to IEEE community, and to EDS members and volunteers in Ukraine. Kateryna Arkhypova, the Newsletter Regional Editor for Region 8 Eastern Europe is one of them. She lives in Kharkiv, the second largest city of Ukraine, which has been so heavily experienced by the war. May peace return there and allow Ukrainian society to have dreams, rebuild the country and work in safe living conditions.

On behalf of the Newsletter editorial team I would like to congratulate the newly elected EDS Executive Committee Members, EDS BoG Members-at-Large, Chairs of the Standing and Technical Committees and wish them a fruitful work on promoting excellence in the field of electron devices for the benefit of humanity and on fostering professional growth of its members (after EDS Vision and Mission Statements).

In this issue, we are launching a series of articles celebrating the 75th Anniversary of the invention of transistors, which contributed not only to unprecedented advances in technology, but also to the tremendous social changes we are witnessing.

The series is coordinated by Manoj Saxena, 75th Anniversary of the Transistor AdHoc Committee Chair. We are more than happy that the first article in the series was written by Prof. Hiroshi Iwai. We are looking forward to the next articles.

In the Society News we share with you an article by EDS President, Ravi Todi on the upcoming undertakings concerning Strategic Planning. We are looking forward to news on this important activity in the next Newsletter issues.

The Technical Briefs section brings us the article by Scott Holmes on low-temperature electronics, a new installment of the series related to the International Roadmap for Devices and Systems IFT Reports. Besides, please find information about the recent edition of the SISC technical conference. I hope that SISC, concerning an important branch of the electron devices domain, will be present in EDS issues regularly. For the last time it was announced in 2017, whereas it was reported in 1996 (!). To finalize a topic of reporting the technical meetings I would like to add that 4th IBM IEEE CAS/EDS AI Compute Symposium (AICS'21) is broadly summarized in Regional News.

The Upcoming Technical Meetings section presents advertisements of the important conferences which will be held in 2022: LAEDC, VLSI, IITC and ESSDERC. Besides, please find in the Regional News section an advertisement of European Microwave Integrated Circuits Conference (EuMIC) 2022. Dates of other conferences sponsored or supported by EDS you may find in the Conference Calendar published at the end of this issue or on the website https://eds.ieee.org/conferences.

In the EDS Young Professionals section Dr. Avirup Dasgupta, 2021 IEEE EDS Early Career Award Winner answers questions by Manoj Saxena, whereas in the EDS Women in Engineering section Dr. Kelin Kuhn, a world-renowned materials scientist, comments on Murphy's laws.

In the Humanitarian Projects News, Chapter News, and Regional News sections we present traditionally articles on achievements and on activities carried out day by day by the EDS chapters worldwide. Among them, there was the IEEE EDS STEM Program conducted in Malaysia.

Dear Readers, if you have any suggestions, comments regarding the Newsletter contents, please do not hesitate to contact the editorial team. We will be very glad to receive your feedback. Interesting views will be presented with the consent of the authors, along with our replies in the Letters to Editors section.

Finally, I would like to express again my thanks to all the article Authors and to all the members of the Editorial Team. I hope that the Readers will find the issue interesting and informative.

Sincerely,
Daniel Tomaszewski

ECE Professor Marvin White wins Emmy Award for Historic Engineering Achievements

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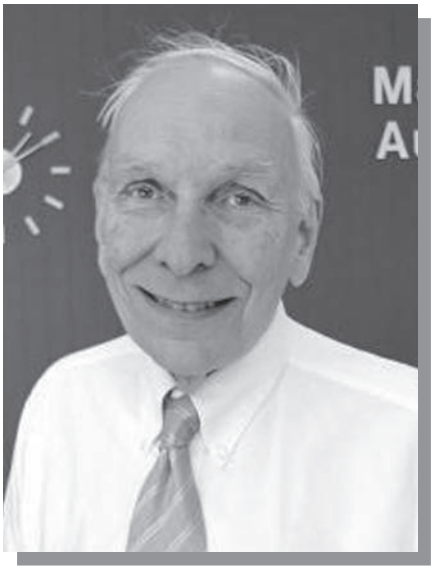
The National Academy of Television Arts and Sciences announced Professor Marvin White, of the Ohio State University, won an Emmy® for his work in Technology and Engineering. According to the Engineering Achievement Committee, the award helps honor the "tool makers" of the industry who crafted the modern television viewing experience. White said he never dreamed of winning a Tech Emmy® someday. "The whole thing was quite a surprise," he said. White, a professor of Electrical and Computer Engineering(ECE) at Ohio State, and Northrop Grumman received the award for work on Correlated Double Sampling for Image Sensors, which showed excellence in engineering creativity.



White's pioneering technological contributions and patents span decades in the field of engineering. Many are still found today in personal cameras, televisions, satellite imaging systems; even the Hubble Space Telescope.

"Screen actors are always cited for Oscars. Stage performers are similarly proud of their Tony Awards. Television journalists are quick to add an Emmy® Award to their resume – and with good reason," the committee letter to White states. "Your work on Correlated Double Sampling (CDS) for Image Sensors showed excellence

in engineering creativity and you join a distinguished group of honorees that are chosen each year by dozens of industry experts and peers."

This year's recipients will be honored at the 73rd Annual Technology & Engineering Emmy® Awards Ceremony tentatively scheduled for April 25th at the Wynn Hotel in Las Vegas, Nevada.

"Historically, TV began with Image Orthicons and Vidicons to capture scenes at low-light levels, but were later replaced by light-weight, high-resolution, solid-state imagers," White said. "In the late 1960s and early 1970s at Westinghouse, I and a team of engineers worked on a way to process images from these solid-state imagers and we called the method Correlated Double Sampling or CDS, which is widely used today."

The Technology & Engineering Emmy® Award was actually the first among any awards issued in 1949, said Adam Sharp, CEO & President, NATAS.

"It laid the groundwork for all the other Emmys to come," he said. "We are extremely happy about honoring these prestigious companies, where the intersection of innovation, technology, and excitement in the future of television can be found."

White joined the Ohio State ECE faculty in 2010 after many years teaching at Lehigh University in Bethlehem, PA, where he was the Sherman-Fairchild Professor of Electrical and Computer Engineering and Director of the Sherman-Fairchild Center for Solid State Studies. He also served two decades at Westinghouse Electric Company, as well as serving stints at the National Science Foundation and Naval Research Laboratory. He has authored or co-authored over 300 technical papers, contributed chapters to four books, and has 27 U.S. patents.

The professor is a member of the U.S. National Academy of Engineering, an IEEE Life Fellow, and served as a distinguished national lecturer of the IEEE Electron Devices Society. He received several awards for his contributions to the development of high-sensitivity, solid-state cameras, and imagers and for major contributions to progress in semiconductor devices including the IEEE Electron Devices Society's 1997 J. J. Ebers Award, and the IEEE 2000 Masaru Ibuka Consumer Electronics Award. In 2011, he received Ohio State's Distinguished Alumnus Award.

Announcement of Newly Elected Officers & BoG Members

Fernando Guarin
2021 EDS Nominations and Elections Chair

The Electron Devices Society (EDS) Officers and Board of Governors (BoG) members-at-large election was held in December 2021 via email. I am pleased to present the results of this election and short biographical information of the incoming team that will lead EDS in the years to come.

Officers

The following volunteers were elected as Officers beginning 1 January 2022:

President-Elect

Bin Zhao received his Ph.D. degree from California Institute of Technology. He has been with SEMATECH, Rockwell, Conexant, Skyworks, Freescale, Fairchild, ON Semiconductor, and has worked on advanced VLSI technology development and design implementation of analog/mixed-signal, power management, and RF IC products. He has authored and co authored over 200 journal publications and conference presentations, has authored three book chapters, and holds over 100 issued patents. He has served as the Founding Co-Chair, Technical Working Group of RF and Analog/Mixed-Signal IC Technologies for Wireless Communications, International Technology Roadmap for Semiconductors (ITRS); IEEE EDS VP of Conferences; IEEE EDS VP of Publications; Chair, Editorial Steering Committee, IEEE Journal of Microelectromechanical Systems (J-MEMS); and Chair, IEEE Johnson Technology Award Committee. He is an IEEE Fellow and currently serves as the Chair of IEEE Conference Committee. He is a member of the IEEE Technical Activities Board, IEEE Publications Services and Products Board, and IEEE IoT Activities Board.

Secretary

MK Radhakrishnan is an academician and technical consultant in the field of electron device failure analysis and reliability, and founder director of NanoRel LLP Technical consultants Singapore from 2004. Previously, he was a Senior Member

of the Technical Staff at the Institute of Microelectronics, Singapore, an Adjunct Professor at the National University of Singapore, and a Scientist at the Indian Space Research Organization. Currently he is an Editor of the *IEEE Journal of the Electron Devices Society* (JEDS). He has served as Editor of the Journal of Semiconductor Technology and Science and Guest Editor to IEEE TDMR. He was the Technical Chair of the IEEE IPFA in 1995 and 1997, General Chair of IPFA 1999 and IEEE IEDST 2009, and Co General Chair of IEEE EDTM 2019. As an IEEE EDS volunteer he served as an IEEE EDS Region 10 SRC Vice Chair, Regional Editor and the Editor in Chief of the EDS Newsletter, a member of the IEEE EDS Board of Governors, and IEEE EDS Vice President of the Regions & Chapters. He is an IEEE Life Senior member, Fellow of IETE, Member of the EDFAS and ESDA, and serves as an IEEE EDS Distinguished Lecturer.

Treasurer

Roger Booth received a PhD in Electrical Engineering from Michigan State University, and is a Senior Member of IEEE. He currently works for Qualcomm, and his career has included time at IBM, TowerJazz and Booz Allen Hamilton (at DARPA). He has spent most of his career working on RF/Analog CMOS processes, but has experience with SOI, SiGe, and high power RF processes.

BoG Members-at-Large

A total of seven members were elected for a three-year term (2022–2024). Five of the seven electees are serving a second term, while the other two have joined the board for the first time. The backgrounds of the electees span a wide range of professional and technical interests. The following are the results of the election and brief biographies of the individuals elected.

Mario A. Aleman is a PhD student at Villanova University in Sustainable Engineering. He received his MSc in Electrical Engineering from Berlin Technical University in Germany (2012) and BSc in Electronics Engineering from the National University of Engineering in Nicaragua (2007). He has been a consultant in the field of energy efficiency and ICT for development during the last years.

Mario is an IEEE Senior Member and Vice Chair of the IEEE Smart Village for the Latin America Working Group LAWG, and active member of the Humanitarian Activities Committee HAC. He is also the recipient of the 2015 IEEE MGA Leadership Award, 2014 IEEE Region 9 Theodore Hissey Outstanding Young Professional Award, 2012 Ashoka›s Changemaker Award, 2008 Ib-Vogt Scholar of the Year, 2008 Outstanding Social Entrepreneur from the International Youth Foundation, 2006 ERA European Union, and 2006 TIC Young Americas Business Trust YBT.

Paul R. Berger is a Professor in Electrical & Computer Engineering at Ohio State University and Physics (by Courtesy). He is also a Distinguished Visiting Professor at Tampere University in Finland. He received the B.S.E. in engineering physics, and the M.S.E. and Ph.D. (1990) in electrical engineering, respectively, all from the University of Michigan, Ann Arbor.

He has authored >250 referred publications & presentations with >115 plenary, keynote, panelist, invited talks. He has 5 book sections, 25 issued patents, and a Google Scholar H-index of 37.

Some notable recognitions for Dr. Berger were an NSF CAREER Award (1996), a DARPA ULTRA Sustained Excellence Award (1998), a Faculty Diversity Excellence Award (2009) and Outstanding Engineering Educator for State of Ohio (2014).

More recently Berger hosted as General Chair the 2021 IFETC meeting and was selected as the Founding Editor-in-Chief for the IEEE Journal on Flexible Electronics.

Yogesh Singh Chauhan is a professor at Indian Institute of Technology Kanpur. He is the developer of several industry standard models: ASM-HEMT, BSIM-BULK (formerly BSIM6), BSIM-CMG, BSIM-IMG, BSIM4 and BSIM-SOI models. His research interests are characterization, modeling, and simulation of semiconductor devices.

He is the Fellow of IEEE and INAE. He is the Editor of IEEE Transactions on Electron Devices and Distinguished Lecturer of the IEEE-EDS. He is the chair of IEEE-EDS Compact Modeling Committee. He is the founding chairperson of IEEE EDS U.P. chapter and chairman-elect of IEEE U.P. section. He has published more than 300 papers in international journals and conferences.

He received Ramanujan fellowship in 2012, IBM faculty award in 2013 and P. K. Kelkar fellowship in 2015, CNR Rao faculty award, Humboldt fellowship and Swarnajayanti fellowship in 2018. He has served in the technical program committees of IEDM, SISPAD, ESSDERC, EDTM, and VLSI Design conferences.

Maria Merlyne De Souza received her PhD from the University of Cambridge. She is Professor of Microelectronics at the University of Sheffield and a Distinguished

Lecturer of the IEEE EDS. She was elected Fellow of the Institute of Physics in 2002 and the Institute of Engineering Technology in 2006. She has published over 200 articles in Journals and conferences. She has served on the editorial boards of several journals, technical and Executive committee member of several conferences including IEDM, IEEE-IRPS, EUMW and is member of the IRT Nanoelectronic Council of France. She is a registered STEM ambassador in the UK.

Patrick Fay is a Professor in the Dept. of Electrical Engineering at the University of Notre Dame; he received a Ph.D. in electrical engineering from the University of Illinois at Urbana-Champaign in 1996. His research focuses on the design, fabrication, and characterization of microwave and millimeter-wave electronic devices and circuits, as well as the use of micromachining techniques for the fabrication of RF through sub-millimeter-wave packaging. He established the High Speed Circuits and Devices Laboratory at Notre Dame, which includes device and circuit characterization capabilities at frequencies up to 1 THz. He also oversaw the design, construction, and commissioning of the 9000 sq. ft. class 100 cleanroom housed in Stinson-Remick Hall at Notre Dame, and has served as the director of this facility since 2003. Prof. Fay is a fellow of the IEEE, and has published 11 book chapters and more than 350 articles in scientific journals and conference proceedings.

Kazunari Ishimaru is an IEEE Fellow and Senior Fellow with Institute of Memory Technology Research and Development, Kioxia Corporation. He conducted research on advanced logic, SRAM, Flash and emerging memories, TCAD, and compact modeling. He is currently directing Corporate R&D strategy and business-academia collaboration. He graduated Waseda University with MS degree and joined Toshiba in 1988. He was a Vice President of R&D with Toshiba America Electronic Components Inc. from 2006 to 2010. He holds 25 U.S. patents and authored/co-authored over 80 technical papers and several invited talks and short course lectures at various international conferences. He served the IEDM General Chair in 2011, Steering committee member of ESSDERC/ESSCIRC from 2008 to 2016. He is one of the founder member of EDTM conference and a General Chair in 2022. He is currently serving the IEEE EDS Vice President of Meetings and Conferences.

Bill Nehrer has developed various technologies over his 30+ years in the semiconductors, spanning from analog CMOS to High Speed BiCMOS and Bipolar, enabling world class products in phased array radar, audio/video single chip solutions, modem, hard disk drive, power management, and high resolution ADCs. His focus is High Reliability and yield optimization in mass production and was elected technical Fellow at Silicon Systems, a Texas Instruments company.

Managing Texas Instruments' High Precision Analog and High Speed BiCMOS roadmap, he directed multiple projects at worldwide TI locations. Joining PDF Solutions in 2004, he managed yield ramp and technology development consulting projects at logic fabs in 90, 65, 45, 32, 28, 20, 14, &10nm technology. He was with FabVantage technology consultancy at Applied Materials from 2018 thru 2021 as Senior Director and now in private practice. Bill holds an MSEE degree in Solid State Electrophysics from the University of Southern California and BS in Chemistry from UCLA. He established the yield & manufacturing subcommittee for EDTM and was the semiconductor manufacturing technical chair for EDS.

I welcome all electees and urge them to get fully engaged in the affairs of the Electron Devices Society. EDS is a volunteer-led volunteer-driven organization and we expect the incoming volunteer leaders will continue this tradition going forward.

Fernando Guarin
2021 EDS Nominations and Elections Chair
Global Foundries

IEEE EDS Fellows Elected in 2022

Since 1963, IEEE has acknowledged those individuals who have contributed to the advancement of engineering science and technology. The honor of Fellow is bestowed on the recipient who has had an extraordinary record of accomplishments in any of the IEEE fields of interest. To learn more about the IEEE Fellow Program: https://www.ieee.org/membership/fellows/index.html.

Congratulations to the 25 EDS members elected to IEEE Grade of Fellow in 2022.

Lay-kee Ang—for contributions to electron emission and space charge effects in nanodiode and quantum materials

Anirban Bandyopadhyay—for leadership in silicon RF-SOI technologies

Seth Bank—for contributions to the growth of optoelectronic materials by molecular beam epitaxy

Subhashish Bhattacharya—for contributions to power conversion systems and active power filters

Zhihong Chen—for contributions to the understanding and applications of low-dimensional nanomaterials

Tarek El-Bawab—for contributions to the definition, recognition, accreditation criteria, and program development of modern network-engineering education

Edmundo Gutierrez—for contributions to education and infrastructure in the field of electron devices in Latin America

Tony Heinz—for contributions to spectroscopic techniques, nanophotonics, and optical nanomaterials

David Horsley—for development of micro-electromechanical systems for ultrasonic transduction

Kevin Kelly—for contributions to compressive imaging

Sarah Kurtz—for contributions to photovoltaic devices and systems reliability

Ioannis Kymissis—for contributions to thin-film electronics for displays and sensors

Hang-ting Lue—for contributions to charge-trapping memories and 3D NOR flash

Philip Neudeck—for contributions to silicon carbide electronics and crystal growth

Anh-Vu Pham—for contribution to organic packaging technologies

Eric Pop—for contributions to phase-change memory

Chuan Seng Tan—for contributions to wafer bonding technology for 3D packaging and integration

Florian Solzbacher—for the development of tools enabling applied and translational neuroscience and neural engineering

Nobuyuki Sugii—for contributions to fully depleted silicon-on-insulator technology

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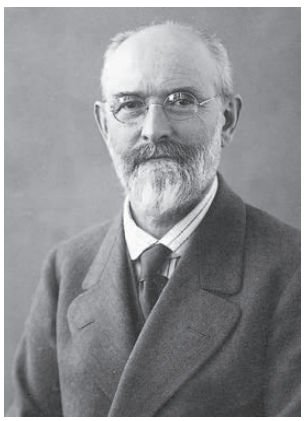
IEEE ROBERT BOSCH
MICRO AND NANO ELECTRO MECHANICAL SYSTEMS AWARD



Robert Bosch (1861-1942)
Inventor, Entrepreneur, Founder of Robert Bosch GmbH

The Robert Bosch Micro and Nano Electro Mechanical Systems Award was established by the IEEE Electron Devices Society in 2014, to recognize and honor advances in the invention, design, and/or fabrication of micro- or nano-electromechanical systems and/or devices. The contributions to be honored by this award should be innovative and useful for practical applications.

This award is sponsored by the IEEE Electron Devices Society, with financial support from Robert Bosch LLC. It is intended that the award will be presented annually to an individual or to as many as three individuals whose achievements and contributions are judged to meet the selection criteria for the award. The award will be presented at an IEEE conference of the winner's choice. It is not necessary for the recipient(s) to be a member(s) of IEEE.

The recipient will receive a US$10,000 honorarium, travel expenses to attend the award presentation, a bronze medal, and a certificate. In the event that more than one awardee is selected the cash honorarium will be equally divided among the recipients. Each recipient will receive a bronze medal and a certificate.

Please visit the EDS website for more information on this award:
https://eds.ieee.org/awards/robert-bosch-micro-and-nano-electro-mechanical-systems-award.

Nominations for this award should be made using our online nomination form, and submitted before midnight (EST) on October 2nd. Letters of recommendation must be sent directly to l.riello@ieee.org according to the same schedule.

Congratulations to Erhard Kohn
2021 IEEE EDS Lester F. Eastman Award Winner

Erhard Kohn

Erhard Kohn is a professor at Ulm University, heading the Institute of Electron Devices and Circuits until to his retirement in 2009. Since then, he has been visiting professor to the Technical University of Vienna, Notre Dame and presently NCSU.

He received his Dr. Ing. degree from the Technical Univ. of Aachen (Germany) in 1975 with work on GaAs based field effect transistors, highlighted by the realization of an integrated differential MESFET amplifier pair with integrated current source (IEDM 1974). After 2 years at the University of Newcastle upon Tyne (UK) this was followed by an approx. 15 year period going through industrial research before returning to academia.

Stations were AEG Telefunken in Germany, Thomson CSF-DAG in France and Siemens Corp. Research in Princeton, NJ. At Thomson CSF the challenge was to set up a GaAs IC pilot line technology for analogue and digital applications based on ion-implantation. This work was accompanied by 5 subsequent sabbaticals to Cornell University in Lester Eastman's group. It was a unique experience and the beginning of a long lasting relationship with Lester and Cornell. During the 1980's the Siemens Company decided to set up a semiconductor technology department at their NJ Research and Technology Laboratory, extending their Munich based GaAs activities. Drawing heavily from Lester's experience, the first GaAs HEMT crossing the 100 GHz threshold could be demonstrated. However, the many changes did also represented a heavy load on his family, especially his 2 children, but was perfectly mastered by Renate, his wife.

In 1989 the Inst. of Electron Devices and Circuits was established at Ulm University. Work moved to III-nitrides and diamond, two wide bandgap materials with ceramic-like stability and ultra-hard properties. Investigating both materials side by side enabled many new device structures, covering the field of electronics, biochemistry, electrochemistry, thermal management as well as MEMS sensors and actuators. As an example, InAlN/GaN HEMT operation at 1000 °C in vacuum could be demonstrated, not expected for an In-containing III-nitride compound. The key was a native 2D-oxide passivation layer discovered in a "golden experiment" by accident, the technology also permitting diamond overgrowth of fully processed GaN devices. The work resulted in more than 130 journal contributions and more than 300 conference and workshop presentations and the formation of 2 spin-off companies.

Erhard had been a distinguished IEEE lecturer and served on the board of the German IEEE-EDS chapter. For many years he was the European Chair and a Trustee of the DRC and for 10 years an executive board member of the Elsevier Diamond conference.

ELECTRON DEVICES SOCIETY®

James C. M. Hwang
EDS Lester F. Eastman Award Chair

IEEE Electron Devices Society
J.J. Ebers Award
Call for Nominations

The IEEE Electron Devices Society (EDS) invites the submission of nominations for the 2022 J.J. Ebers Award. This award is presented annually by EDS to honor an individual(s) who has made either a single or a series of contributions of recognized scientific, economic, or social significance to the broad field of electron devices. The recipient(s) is awarded a plaque and a check for $5,000, presented at the IEEE International Electron Devices Meeting (IEDM) or any one of EDS's flagship conferences.

For more information: https://eds.ieee.org/awar ds/j-j-ebers-award

J.J. Ebers Award on-line nomination form:
https://ieeeforms.wufoo.com/forms/xl0lxns05xzwir/

Submission Deadline: 1 July 2022

Questions: Please contact Laura Riello of the EDS Executive Office, at l.riello@ieee.org

IEEE EDS Fellows Elected in 2022

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Tetsuzo Ueda—for contributions to development and commercialization of III-V compound semiconductor technologies

Daniel Van Der Weide—for contributions to ultrafast terahertz electronics and biomedical applications of microwave technologies

Huili Grace Xing—for contributions to GaN high-electron-mobility transistors

(Jianhua) J. Joshua Yang—for contributions to resistive switching materials in memory and neuromorphic computing

Uisik Yoon—for contributions to bio-microelectromechanical systems (BioMEMS) technologies for opto-electrical neural interfaces and microfluidic biochips

Carl Zetterling—for contributions to silicon carbide devices

2021 IEEE EDS Distinguished Service Award

Samar Saha
2021 IEEE EDS Distinguished Service Award winner

The IEEE Electron Devices Society (EDS) is extremely proud of the services that it provides to its members. EDS members generate the leading edge developments in the field of electron devices and share these results with their peers and the world-at-large by publishing their papers in EDS journals and presenting results in its meetings. This is a global activity that is effective because of the efforts of numerous volunteers. Many of these dedicated volunteers labor in relative obscurity, with their only reward being the satisfaction that they receive in being an important part of a successful organization, namely of the IEEE Electron Devices Society. One means of thanking these volunteers is to recognize their contributions through the EDS Distinguished Service Award.

The recipient of the 2021 EDS Distinguished Service Award was Dr. Samar Saha, Prospicient Devices, Milpitas, California. Please visit the IEEE EDS website to view the award presentation video.

Samar Saha works as the Chief Research Scientist at Prospicient Devices, Milpitas, California and is an Adjunct faculty in the Electrical Engineering department at the Santa Clara University, California, USA. Since 1984, he has worked in various technical and managerial positions at National Semiconductor, LSI Logic, Texas Instruments, Philips Semiconductors, Silicon Storage Technology, Synopsys, DSM Solutions, Silterra USA, and SuVolta. In academia, he was a faculty member in the Electrical Engineering departments at Southern Illinois University at Carbondale, Illinois; Auburn University, Alabama; the University of Nevada at Las Vegas, Nevada; and the University of Colorado at Colorado Springs, Colorado.

At Prospicient Devices he is working on exploratory device research to develop next generation integrated circuit devices for advanced technology at the nanometer nodes. He has authored over 100 research papers; two books entitled, FinFET Devices for VLSI Circuits and Systems, CRC Press, Florida (2020) and Compact Models for Integrated Circuit Design: Conventional Transistors and Beyond, CRC Press, Florida (2015); one book chapter on Technology Computer-Aided Design (TCAD), titled, Introduction to Technology Computer-Aided Design, in Technology Computer Aided Design: Simulation for VLSI MOSFET, C.K. Sarkar (Editor): CRC Press, Florida (2013). He was awarded 12 US patents. His patent on double-halo metal-oxide-semiconductor field-effect transistor has contributed significantly to continued scaling of planar-complementary metal-oxide-semiconductor (CMOS) technologies that has a global impact on CMOS IC chip business with a total value over USD 300 billion per year.

In the IEEE, he has served as the 2016–2017 elected President of the Electron Devices Society (EDS) and currently serving as a member of the IEEE Fellow Committee. Previously, He has served as the Senior past and Junior past President of EDS; EDS Awards chair; Vice President of EDS Publications; an elected member of the EDS Board of Governors; EDS fellow evaluation committee member; Editor-In-Chief of IEEE Quest-EDS; Chair of EDS George Smith and Paul Rappaport awards; editor of IEEE Region-5&6 EDS Newsletter, Chair of EDS Compact Modeling Technical Committee, Chair of EDS North America West Subcommittee for Regions/Chapters, a member of the IEEE Conference Publications Committee; a member of the IEEE TAB Periodicals Committee; and the Treasurer, Vice Chair, and Chair of Santa Clara Valley–San Francisco/EDS chapter.

In editorial board, he served as the head guest editor for the *IEEE Transactions on Electron Devices* (T-ED) Special Issues (SIs) on "Advanced Compact Models and 45-nm Modeling Challenges" and "Compact Interconnect Models for Giga Scale Integration," as well as the head guest editor for the *IEEE Journal of the Electron Devices Society* (J-EDS) Special Issues from the selected Extended Papers presented at 2020 EDTM, and selected Extended Papers presented at 2021 CAD-TFT; and as a guest editor for the T-ED Special Issue on "Advanced Modeling of Power Devices and their Applications" and the J-EDS SI on Flexible Electronics from the Selected Extended Papers presented at 2018 IFETC.

His key accomplishments in IEEE EDS include, launching of the 1st IEEE Electron Devices Technology and Manufacturing (EDTM) Conference, Toyama, Japan (2017); co-founding and launching of the 1st IEEE International Flexible Electronics Conference (IFETC), Ottawa, Canada (2018); co-founding and 1st General Chair of the International Conference on Computer-Aided Design on Thin Film Transistor Technologies (CAD-TFT), Cambridge, UK (2008); Establishing the 1st IEEE EDS Center of Excellence, Kolkata, India (2017); establishing EDS's first Five-year Strategic Planning (2017); establishing five annual undergraduate fellowships award and one annual Lester Eastman award (2019); and Launching the IEEE Journal of Photovoltaics (2011) as well as the *IEEE Journal of the Electron Devices Society* (2013).

Dr. Saha has been living in the San Francisco Bay Area/Silicon-Valley for the last four decades. He received the PhD degree in Physics from Gauhati University and an MS degree in Engineering Management from Stanford University. He is a Distinguished Lecturer of EDS, an IEEE Life Fellow, and a Fellow of the Institution of Engineering and Technology (IET), UK.

EDS is proud to extend this recognition for his many years of selfless dedicated service.

Fernando Guarin
EDS Awards Chair

2022 EDS EDUCATION AWARD
CALL FOR NOMINATIONS

The IEEE Electron Devices Society invites the submission of nominations for the EDS Education Award. This award is presented annually by EDS to honor an individual who has made distinguished contributions to education within the field of interest of the Electron Devices Society. The recipient is awarded a plaque and a check for $2,500, presented at the IEEE International Electron Devices Meeting (IEDM).

The nominee must be an EDS member engaged in education in the field of electron devices, holding a present or past affiliation with an academic, industrial, or government organization. Factors for consideration include achievements and recognition in educating and mentoring students in academia or professionals in the industrial or governmental sectors. Specific accomplishments include effectiveness in the development of innovative education, continuing education programs, authorship of textbooks, presentation of short-courses at EDS sponsored conferences, participation in the EDS Distinguished Lecturer program, and teaching or mentoring awards.

Since this award is solely given for contributions to education, the nomination should exclude emphasis on technical contributions to engineering and physics of electron devices.

The nomination form can be found on the EDS website:
https://eds.ieee.org/awards/education-award

The deadline for the submission of nominations is 1 September 2022.

Congratulations to Avirup Dasgupta and Jiaju Ma 2021 IEEE EDS Early Career Award Winners!

Avirup Dasgupta, an IEEE Senior Member, is an assistant professor in the department of Electronics and Communication Engineering at the Indian Institute of Technology Roorkee (IITR). He is a founding member of the Circuits and Devices Research Group (CiDeR Group) at IIT Roorkee and is the director of the Device Research Lab (DiRac Lab) at the department of Electronics and Communication Engineering, IIT Roorkee. He is a compact model developer with the Compact Model Coalition, the BSIM group and the Berkeley Device Modeling Center, UC Berkeley.

He completed his undergraduate, graduate and doctoral studies at the Indian Institute of Technology Kanpur (IITK). Following this, he worked as a postdoctoral scholar at the Department of Electrical Engineering and Computer Science, University of California Berkeley (UC Berkeley). He worked as the lead developer and the manager of the BSIM group and the Berkeley Device Modeling Center (BDMC), UC Berkeley.

Dr. Dasgupta's work primarily involves the analysis, modeling and design of semiconductor devices. One of the key areas of his work is to develop compact models for SPICE simulations. He is the developer of the IITK-RPTM model and a co-developer of the industry standard BSIM-BULK, BSIM-IMG, BSIM-CMG, BSIM-SOI and ASM-HEMT models. His research interests include semiconductor device physics, modeling and design for various applications including logic, memory, RF, power, quantum computing, space applications, neuromorphic computing as well as genome sequencing and computational psychopathology. Apart from working on the development and design of the latest and upcoming semiconductor devices with various industry sponsors and academic collaborators, his research group is also working on pushing the boundary of mathematical modeling for computer-aided-design using artificial intelligence.

Avirup spent his early years in the city of Durgapur, West Bengal, India. In 2008, he was recognized by the National Council of Educational Research and Training, Government of India as a *National Talent Scholar*. He has continued to be recognized for his performance and contributions ever since. Apart from multiple journal and conference publications, Dr. Dasgupta also serves as a reviewer for various journals and conferences. He enjoys teaching students at various level and has been rewarded for his teaching excellence.

Apart from the research and academic work, Avirup is passionate about automobiles. He shares this passion with his wife and the couple can often be found on weekend drives or motorcycle rides. Avirup also plays multiple musical instruments, creates digital artworks, and loves playing soccer.

Jiaju Ma is a pioneering inventor and entrepreneur in the field of CMOS image sensor and Quanta Image Sensor. Ma is the co-inventor and designer of the first CMOS image sensor pixel devices with deep sub-electron read noise that enables photon counting and photon-number resolution without using electron multiplication, generally referred to as a Quanta Image Sensor (QIS). This innovative device can clearly distinguish individual photoelectrons and has a small pitch size that enables mega-pixel resolution and which is compatible with standard CMOS image sensor manufacturing processes for mass production. The low-noise photon-counting pixel device that Ma co-invented and developed is being commercialized at Gigajot Technology (Pasadena, CA), a start-up co-founded by Ma. Because of its superior low-light imaging capability, high resolution and high dynamic range performance, this technology is considered an enabling technology for advanced scientific, space, and defense applications. This technology is also receiving a broader interest from consumer-level applications such as security, automotive, and mobile imaging, as an improvement over current CMOS image-sensors.

Ma received his B.S. in Applied Physics from Nankai University, China, and his Ph.D. in Engineering Sciences from Dartmouth College, New Hampshire, USA. His Ph.D. thesis work was focused on the development of the ultra-low-noise pixel devices, referred to as "jot", to enable photon-counting sensitivity within a small pitch size. After graduating from Dartmouth in 2017, Ma decided to continue devoting his work on the development of QIS and commercialize this technology. He co-founded Gigajot with Dr. Eric Fossum and Dr. Saleh Masoodian and moved the startup to Pasadena, CA. At Gigajot, he serves as CTO and leads the engineering work to further advance the performance and readiness of this technology for mass production in both high-performance and consumer applications. Under his leadership, Gigajot announced the world's first commercially available QIS products in 2021, marking the dawn of a new era in solid-state imaging.

Ma has over 50 technical publications and holds over 20 US patents and patent applications. He is a member of Institute of Electrical and Electronics Engineers (IEEE) and IEEE Electron Devices Society (EDS). He was a member of the technical committee of the International Image Sensor Workshop (IISW) in 2019.

CALL FOR NOMINATIONS
2022 IEEE EDS Early Career Award

Description: Awarded annually to individuals to promote, recognize and support Early Career Technical Development within the Electron Devices Society's field of interest

Prize: An award of US$1,000, a plaque; and if needed, travel expenses not to exceed US$1,500 for each recipient residing in the US and not to exceed US$3,000 for each recipient residing outside the US to attend the award presentation.

Eligibility: Candidates must be an IEEE EDS member and must have received his/her first professional degree within the 10th year defined by the August 15 nomination deadline and have made contributions in an EDS field of interest area. Nominators must be IEEE EDS members. Previous award winners are ineligible.

Selection/Basis for Judging: The nominator will be required to submit a nomination package comprised of the following:

- The nomination form that is found on the EDS web site, containing such technical information as the nominee's contributions, accomplishments and impact on the profession or economy and a biographical description.
- A minimum of two and a maximum of three letters of recommendation from individuals familiar with the candidate's technical contributions and other credentials, with emphasis on the specific contributions and their impacts.

The basis for judging includes such factors as: the demonstration of field leadership in a specific area; specific technical contribution(s); impact on the profession or economy; originality; breadth; inventive value; publications; honors; and other appropriate achievements.

Schedule: Nominations are due to the EDS Executive Office on 15 August each year. Candidates will be selected by the end of September, with a presentation to be made in December.

Presentation: At the EDS Awards Dinner that is held in conjunction with the International Electron Devices Meeting (IEDM) in December. The recipients will also be recognized at the December EDS BoG Meeting.

Nomination Form: Complete the nomination form by 15 August 2022. All endorsement letters should be sent to l.riello@ieee.org by the deadline.

For more information contact: l.riello@ieee.org or visit: http://eds.ieee.org/early-career-award.html

Ravi Todi
2021 EDS Early Career Award Chair

Murphy's Laws and Their Importance in Engineering

Kelin J. Kuhn (IEEE Fellow)

As I reflect over my electrical engineering career, perhaps the most relevant insights I can offer are on the significant role played by "Murphy's Law" (and its various corollaries). I present three stories from different phases of my career to illustrate the importance of these laws in modern engineering.

Murphy's Third Law: Everything takes longer than you think.

In my very first engineering job, my boss taught me about Gantt charts. At a high level, Gantt charts are a type of bar chart used in project planning to illustrate a project schedule. The horizontal axis is time, the vertical axis is a list of tasks, and the length of time to complete each task is represented by the length of the horizontal bar on the chart. (A Gantt chart is the official name for the default charts created by Microsoft Project.) My boss had a well-tested method for creating Gantt charts. His first step was to write down every single task in the project. His second step was to determine the length of time for each task. The way my boss determined the length of time for each task was to talk with the various content experts for each task and get their best estimate for the time it would take to complete the task. He would take this best estimate and MULTIPLY it by π (yes, π = 3.14159 etc.) and put this revised time in the chart. Of course, my first question upon hearing this approach was "Why are you multiplying the expert's time estimates by π?" My boss explained (very seriously) that people had done studies on estimation and determined that most people are off about a factor of three when they estimate the length of time it takes to

do something. He then added (with a twinkle in his eyes) that he used π because it sounded more technical. At the time, I laughed and didn't take this very seriously. However, as time passed and my engineering career evolved, I realized that my old boss (and his "rule of π") was disturbingly accurate. Gantt charts I made using the estimates given by content experts were invariably about a factor of three too optimistic. Pretty soon I was multiplying all the estimates in my Gantt charts by π as well! It was a fabulous (and quantitative!) example of Murphy's Third Law: *Everything takes longer than you think.*

Murphy's Sixth Law: If you perceive that there are four possible ways in which a procedure can go wrong, and circumvent these, then a fifth way, unprepared for, will promptly develop.

One of the jobs I had as a semiconductor process integration engineer was to follow-up on excursions that occurred in the factory. One of the things I learned very quickly was this job was Murphy's Sixth Law in action. People work very hard to prevent procedures from going wrong in a semiconductor factory, and yet new ways, unprepared for, will promptly develop. As an example, on one occasion I was responsible for investigating an excursion in a wafer cleaning operation. A box of wafers had failed end-of-line electrical test, and subsequent physical analysis showed the transistors on these wafers had been severely etched. A combination of the physical analysis and the flow of the box through the factory narrowed the issue to a single wafer cleaning operation. The model was that a potent acid had somehow been introduced into the usually benign wafer cleaning step. The first hypothesis was that the wrong recipe had been introduced at the wafer cleaning tool. However, the tool had numerous fail-safes and interlocks to prevent exactly this kind of accident from happening. Furthermore, follow-up on the tool showed everything had been done properly. The right recipe had been run in the right way at the right time.

So … we continued to investigate.

The next hypothesis was that somehow acid had been introduced into the tool during a preventative maintenance (PM) operation. Of course, PMs have a number of internal procedures and cross-checks to prevent this type of error. Furthermore, everything showed the PMs on the tool had been done properly. More tellingly, data analysis showed the damaged box of wafers was not the first box through the tool after a PM (nor the last box before a PM) but roughly midway in the cycle. Thus, the PM was not responsible.

So … we kept hunting.

By this point, we had exhausted the possibilities at the tool itself and we started to investigate the plumbing for the cleaning tank. The hypothesis here was the input feed lines for the tank had somehow become contaminated with acid. The first problem with this explanation was there were multiple valves (both physical valves and automatic valves) to prevent the possibility of acid entering the tank during a wafer cleaning cycle. The second problem with this explanation was there was a purge cycle before the actual wafer cleaning cycle – the purpose of the purge cycle being to clear any contamination out of the lines.

HOWEVER, during investigation of the feed lines to the tank, we found our first clue. Someone noticed that a routine sample collection process for the acid tank had been logged – and the time of the sample collection was exactly the same as our excursion!

Another day or so of investigation and we finally understood the excursion. First, the automatic valve protecting the wafer cleaning tank from being contaminated by acid had failed. Second, it had failed in a way that kept its electronic sensor thinking it was fine—so it was still showing a green light. Third, although the automatic valve had a back-up manual valve, the routine sample collection procedure required the manual valve to be opened briefly (of course, after checking that the automatic valve had a green-light). Finally, the sample collection procedure just happened (Murphy again!) to occur at the worst possible time (right after the purge-cycle) meaning that the acid was introduced directly into the wafer cleaning tank during the fill cycle (rather than before the fill cycle, when it would have simply been purged out again). So, there were four separate levels of protection (automatic valve, green-light, manual valve, and purge-procedure) and the system STILL failed because the sample collection occurred precisely as the tank was filling. It was a fabulous example of Murphy's Sixth Law: *If you perceive that there are four possible ways in which a procedure can go wrong, and circumvent these, then a fifth way, unprepared for, will promptly develop.*

Murphy's Eighth Law: If everything seems to be going well, you have obviously overlooked something.

One of my roles as a process integration engineer was to develop a process for transistor isolation. (The transistor isolation is a region of oxide that surrounds each transistor and keeps it from shorting to other transistors.) This process has two parts. The first part is to develop an etch which creates a trench of a suitable depth and width for good isolation. The second part is to fill the trench with an appropriate oxide. The challenge here is that the etched trench has a high aspect ratio (it is both narrow and deep) and it is very difficult to fill the trench without creating a large void in the oxide. As such, significant experimentation is required to optimize both the etched trench and the subsequent oxide fill to create well-behaved void-free isolation regions. This story begins with an isolation process that had an issue with a central buried void in the middle of the isolation oxide. This void was undesirable, because if the void filled with polysilicon it would create a yield defect between adjacent poly lines. As such, I had been running an extensive effort to create an isolation fill process that would reduce or eliminate the void. The main metric for monitoring the success of this process was to measure the wafers at a particular point in the process flow by counting the defects using a special kind of wafer inspection microscope. Over a period of some months, a number of recipes were developed for the isolation fill, and the results were looking increasingly good. By the time the lead box of wafers for the technology was ready to be processed at the isolation module, I had two processes available. The first was the "baseline" process—which was still having significant issues with void defects. The second was the "new" process—which was delivering zero defects as measured by the wafer inspection microscope. So, at the meeting to decide what to run on the lead lot, I enthusiastically presented all the data; and we elected to run the lead box of wafers on the "new process". All of the wafers. Well, what happened was that the "new" process had created a new kind of void. The new void was so small that it wasn't detectable by the wafer inspection microscope. However, it was just devastating to yield. So, when the lead box of wafers reached yield testing—pretty much everything failed. The yield analysis reports of the time showed defects as black dots on the wafer—and the entire wafer map was black with failed dots. For ALL the wafers. It was a fabulous example of Murphy's Eighth Law: *If everything seems to be going well, you have obviously overlooked something.*

So, in conclusion, as I reflect over my electrical engineering career, I continue to believe that Murphy's Law (and its corollaries) are AT LEAST as important to electrical engineering as Maxwell's Equations!

Dr. Kuhn received her B.S. in Electrical Engineering from the University of Washington, Seattle, WA (magna cum laude) in 1980 and the M.S. and Ph.D. in Electrical Engineering from Stanford University, Stanford, CA in 1985. From 1987-1997 she held faculty positions at the University of Washington (in Seattle) in Materials Science and Engineering and Electrical and Computer Engineering. She left the University in 1997 as a tenured Associate Professor of Electrical and Computer Engineering. During this period in her career, her expertise included III-V molecular beam epitaxy and optoelectronics. Key milestones during this period of her career include the NSF Presidential Young Investigator award (1991–6), the University of Washington Distinguished

Teaching Award (1995), and single-author on a textbook (Laser Engineering, Prentice-Hall, 1998, ISBN 0-02366921-7). From 1997–2014 she held a variety of technical positions at the Intel Corporation (in Hillsboro). She retired from Intel in 2014 as an Intel Fellow in the Technology and Manufacturing Group. During this period in her career her expertise included process integration and device physics. She was involved in Intel's CMOS manufacturing process technology development for the 0.35 micron, 130 nm, 90 nm, 45 nm, 22 nm, 14 nm, 10 nm and 7nm technology nodes. Key milestones during this period of her career include the IEEE Paul Rappaport Award (2013) and IEEE Fellow (2011). From 2014–2015, she held the Mary Shepard B. Upson Visiting Professorship at Cornell, with a focus on Materials Science and Engineering. She continues a strong relationship with Cornell, presently holding an adjunct Professorship in Materials Science and Engineering. Her present work at Cornell involves the NSF PARADIM project. Key milestones during this period of her career include the IEEE Frederik Philips Award (2016), and publication of CMOS and Beyond: Logic Switches for Terascale Integrated Circuits (Co-editor with Prof. Tsu Jae King Liu, Cambridge Press, 2015).

Dr. Avirup Dasgupta
Department of Electronics and Communication Engineering, IIT Roorkee, India

2021 IEEE EDS Early Career Award Winner

The Young Professional guest in this issue of the Newsletter is Avirup Dasgupta, Electron Devices Society's 2021 Early Career Award winner and a faculty member at the Department of Electronics and Communication Engineering, IIT Roorkee, India. His perceptions about EDS and views regarding professional development and career growth are reflected in the discussion. Here are the excerpts of the interview made by Manoj Saxena, the Newsletter Associate Editor-in-Chief, with Avirup Dasgupta.

Manoj Saxena (MS): What was the specific temptation, if any, which made you join EDS which is the largest professional organization in the globe, at first?

Avirup Dasgupta (AD): I joined EDS during my M.Tech studies when I started pursuing research actively. Several renowned researchers in the field of semiconductor devices were all associated with EDS; which motivated me to be a part of this community. At first, I bought the IEEE and EDS membership to primarily get access to the various journals and to avail of discounts at various IEEE conferences. However, the EDS membership proved significantly more beneficial than I had expected. EDS provided a platform to gain access to notable professionals and the latest developments in my area of work.

MS: You won the prestigious EDS Early Career Award, an honor most young professionals aspire to. How do you consider this recognition and what are your plans to further develop your research career?

AD: I am honored to have received the prestigious EDS Early Career Award. I am grateful that my contributions to the EDS field of interest have been recognized. In my opinion, this would not have been possible without the constant support I have received from various people throughout my life: be it my family, my friends, my supervisors, mentors, collaborators, or peers. I am grateful to have such good people in my life. I wish to keep contributing to the electron devices community, and to humankind as a whole, through my action research in the field of semiconductor devices, especially in compact modeling, machine-learning augmented modeling, devices for future technologies, non-volatile memories, and devices for quantum computing. In my opinion, we are at a time of change in the semiconductor community where lots of novel materials, device engineering concepts, paradigm-shifting modeling ideas, and new technologies are being looked at to select the best paths for the future. I am happy that I am a part of this significant worldwide effort and will continue to contribute to it.

MS: As a Young Professional, how do you position your interest in your own field with the activities and services you perform as an EDS member/volunteer?

AD: I feel my interests in my research field align well with EDS member/volunteer activities. I volunteer as a reviewer for multiple EDS journals and have been on the technical program committee for various conferences. These, in my opinion, are a good way to stay aware of what is happening in the research community. Also, I have delivered talks at sessions organized by various EDS chapters and have recently started organizing talks with my local chapter to learn more about the present and future of semiconductor devices from various experts. These activities make me a more aware researcher and keep me motivated in the field.

MS: What are your thoughts about the EDS membership and its paybacks? Whether the EDS membership benefited you at any time in your career growth? If so, how?

AD: The EDS membership has been of great benefit to my professional growth. It has provided an opportunity to connect and network with various professionals from around the world, which has been extremely beneficial for my professional

growth. EDS has introduced me to various mentors and collaborators who have been instrumental in my career development.

MS: As a YP, how do you consider the ED Society as a whole, and what are the changes or developments you would like to see in evolving this professional body as a group devoted to humanity and its causes?

AD: I think the ED Society is doing a great job at nurturing young professionals while also recognizing and celebrating contributions from leading experts. I have seen EDS conduct surveys and continuously question its ideas and get feedback from all members. This continued drive to evolve and the attention to feedback are a few reasons that make this society so relevant and useful for all members.

MS: What are your suggestions and recommendations for those young professionals who may aspire to join EDS?

AD: I would suggest all young professionals with an interest in the field of Electron Devices be a member of EDS at the earliest. I actively suggest the same thing for all my students as well. The most important benefit of EDS is that it provides a platform for young professionals to network with various people around the world. This is a huge boon for people willing to take their careers forward and especially for young professionals who can use this to get various opportunities.

MS: As an EDS Young Professional and a young researcher in the field, how do you consider the prospects of scientific research in this field for the progress of Humanity as a whole?

AD: The field of electron devices is at the core of our modern life. Every aspect of our social, personal, and professional lives is governed by electronics; and electron devices are the basic building blocks. The prospects of scientific research in this field are very bright and the scope is ever increasing. As we develop more complex systems, we encounter more challenges which in turn lead this field to widen and become more interdisciplinary. It wouldn't be an exaggeration to say that electron devices have become one of the key components of the progress of humanity and it will be more so in the future.

Avirup Dasgupta is an assistant professor in the Department of Electronics and Communication Engineering. Indian Institute of Technology Roorkee (IITR). He is also affiliated with the Centre for Photonics and Quantum Communication Technology at IITR. He currently leads the Device Research Lab (DiRac Lab) where his team works on the current as well as future semiconductor devices and advanced modeling techniques. He also works as a developer with the BSIM group and the Berkeley Device Modeling Centre (BDMC), University of California Berkeley. He is a co-developer of the industry-standard BSIM-BULK, BSIM-IMG, BSIM-CMG, BSIM-SOI, ASM-HEMT, and IITK-RPTM models. Dr. Dasgupta completed his undergraduate, graduate, and doctoral work at the Indian Institute of Technology Kanpur (IITK). He has worked as the manager of the Berkeley Device Modeling Centre and as a postdoctoral scholar in the BSIM group at the Dept. of Electrical Engineering and Computer Science, University of California Berkeley.

EDS PODCAST SERIES

EDS is pleased to announce our new podcast series. Join us as we host interviews with some of the most successful members of our Society sharing their lives and careers. Their insight and wisdom will be invaluable inspiration and knowledge for those in the engineering field. Stay tuned to our social media channels and website for future announcements on upcoming events.

FOLLOW OUR SOCIETY ON SOCIAL MEDIA!

Call for Nominations – EDS Student Fellowships for 2022

The IEEE Electron Devices Society invites nominations for the 2022 PhD, Masters and Undergraduate Student Fellowships. These annual awards are given to promote, recognize, and support graduate, masters, and undergraduate level study and research within the EDS field of interest.

Please help to promote the EDS Student Fellowships by distributing this information to your colleagues and students. If you have any questions or need further information, please do not hesitate to contact Stacy Lehotzky by email at s.lehotzky@ieee.org. Thank you!

For access to more information and applications: https://eds.ieee.org/education/student-fellowships

EDS Masters Student Fellowship

Prize: US $2,000 and an award plaque

Submission Deadline: 15 May 2022

EDS PhD Student Fellowship

Prize: US $5,000 and travel funds to attend the IEDM for presentation of an award plaque

Submission Deadline: 15 May 2022

For both Masters and PhD, it is expected that at least one fellowship will be awarded to a student in each of the following geographical regions: Americas, Europe/Middle East/Africa, and Asia/Pacific.

EDS Undergraduate Student Scholarship

Prize: US $1,000 and an award plaque

Submission Deadline: 15 May 2022

For the Undergraduate, it is expected that at least one fellowship to each eligible student in each of the IEEE geographical Regions 8, 9, and 10 and two fellowships in Regions 1–7 not exceeding one from Region 7.

IEEE EDS STEM PROGRAM: ELECTRONICS IN CODING AND ROBOTICS

BY P SUSTHITHA MENON, NAVAKANTA BHAT, BADARIAH BAIS, TAN EU GENE, AHMAD SABIRIN ZOOLFAKAR, BERNARD LIM, JAGADHESWAN RAJENDRAN, AZRUL AZLAN HAMZAH, FERNANDO GUARIN

In order to excite young minds, IEEE Electron Devices Society (EDS) created the Engineers Demonstrating Science: an Engineer Teacher Connection or EDS-ETC program in 2011, led by Fernando Guarin. Since then, the STEM Educational program has reached out to 15,650 students from 10 Regions involving 50 EDS local Chapters. The goal of the program is to enable EDS chapter members to visit local schools or host events designed to engage teachers and young students in the field of electrical engineering using Elenco Snap Circuits® kits.

In an effort to further expand the program in the era of the 4th Industrial Revolution (IR4.0) and Artificial Intelligence (AI), there is a need to educate pre-university kids on the fundamentals of electron devices in frontier areas such as Coding and Robotics. Therefore, IEEE EDS Educational Activities under the leadership of Navakanta Bhat and Fernando Guarin funded USD 10,000 for the project Extended EDS-ETC: DIY Robotics in Malaysian EDS Chapters; led by IEEE STEM Ambassador 2021, P Susthitha Menon from the Institute of Microengineering and Nanoelectronics (IMEN), National University of Malaysia (UKM).

Since August 2021, EDS Malaysian Chapters comprising of EDS UKM Student Branch, EDS Malaysia-Kuala Lumpur and EDS/MTT/SSCS Penang Joint Chapter in collaboration with IMEN, UKM have been conducting online workshops related to EDS-ETC, Coding and Robotics. Educational kits sponsored by IEEE EDS are 1) Snap Circuits with Coding (using bluetooth-powered SC controller and enabled via app-driven BOTCode and BLOCKLY codes), 2) Tobbie II Robot which uses micro:bit programmable board for coding using Microsoft MakeCode Editor or Python Editor and 3) Educational Solar Bot.14 Robot which explains the concept of renewable energy where it is powered by solar energy to work on land and water. In addition to these kits, online software-TinkerCAD, Microbit and MakerUno kits were also used for some of the programs.

The program was implemented under the constraints imposed by the COVID-19 pandemic, where movement control order was in place. Therefore, the events were held at homes of EDS members and friends in Malaysia (comprising different states) and their neighborhood areas. Kits were posted to EDS members and a series of workshops including train-the-trainers, student workshops, student competitions, STEM awareness and humanitarian programs were held. The program was divided into several online sessions. Prior to the program, YouTube videos were provided to all trainers and participants as the videos had outlined the step-by-step method to assemble the kits and execute the projects. Also the kits came with clear instruction manuals that trainers and participants could refer to. Participants could execute the projects on their own during their own leisure time with the help of the trainers (on-demand training).

A total of 11 STEM programs were conducted from August—December 2021 consisting of volunteers, teachers and parents; benefitting 417 pre-university kids in Malaysia. Nine STEM programs were conducted online while two programs were held face-to-face with the kids. The programs which include coaching, mentoring and quizzes have been uploaded into IEEE TryEngineering STEM portal (Electronics in Coding and Robotics, link https://stemportal-tryengineering.ieee.org/programs/detail/25dc9dfd-d414-48dc-8ed8-5a990b797d6d). The program was also exhibited during the inaugural IEEE STEM Summit held from 1–6 November 2021 with a total of 44 visitors to the IEEE EDS STEM booth.

The following programs listed below were executed in the EDS Malaysian Chapters in 2021. They were executed both in English and local languages to have a better and wider outreach.

Program 1: Train-the-trainers session and TryEngineering STEM portal (14 August 2021, 55 participants, online)

Program 2: Train-the-students session: Discover Coding kit (29 August 2021, 52 participants, online)

Program 3: Train-the-students session: Solarbot.14 kit: (5 September 2021, 56 participants, online)

Program 4: Train-the-students session: Tobbie II kit: (12 September 2021, 32 participants, online)

Program 5: Online STEM Photo/Video/Quiz Competition: (3 October 2021, 24 participants, online)

Program 6: EDS IEEE Day 2021: TinkerCAD & Microbit STEM Programme for SDG (10 October 2021, 50 participants, online)

Program 7: STEM Talk: My journey as an Electronics Engineer (17 October 2021, 126 participants, online)

Program 8: TinkerCAD and Microbit STEM Program for the Indigenous People of Malaysia (21 November 2021, 29 participants, online)

Program 9: Microbit and MakerUno STEM Program for the Underprivileged Kids of SJKT West Country Timur (5 December 2021, 74 participants, online)

Program 10: Microbit STEM Program for the Pre-University Kids of Batu Grace Orphanage Home (11 December 2021, 80 participants, face-to-face at Batu Grace Home Orphanage Home, Kulim, Kedah, Malaysia)

Program 11: IMEN Junior Electronics and Nanotechnology (IJEN) STEM Program (14 and 21 December 2021, 40 participants, face-to-face at IMEN, UKM, Malaysia)

We hope these STEM efforts from IEEE EDS will be proliferated to other EDS chapters worldwide and empower more EDS members and non-members to undertake humanitarian and STEM educational programs for the benefit of humanity. IEEE EDS would like to thank all the collaborators for the successful execution of all the STEM programs. Watch the full program on YouTube: https://youtu.be/9ZmigicDKK8

EDS STEM Program included in IEEE TryEngineering: https://stemportal-tryengineering.ieee.org/programs/detail/25dc9dfd-d414-48dc-8ed8-5a990b797d6d

Participants of IEEE EDS STEM Program 10, executed at an Orphanage Home in Kulim, Kedah, Malaysia

~Sharma Rao Balakrishnan, Editor

Report from EDS Puebla Chapter, IEEE Puebla Section

IEEE HAC/SIGHT: The $1 shield: low-cost photocatalytic coatings on plastic face shields for SARS-CoV-2 inactivation

by Joel Molina-Reyes

Since the early stages of the COVID-19 pandemics, many scientists have focused their efforts in developing a vaccine that by now has helped to immunize billions of people against the SARS-CoV-2 virus worldwide. This is possible if mature technology is already accessible to effectively process genetically engineered elements like the mRNA (messenger RNA) and others. This in turn, relies on the continuous advancement of several scientific fields, including those used in the semiconductor industry. One of the additional

Development of large area photocatalytic coatings on plastic surfaces and donation to several public organizations in Puebla, Mexico for protection against SARS-CoV-2 virus

efforts being done by the scientific community is the development of highly-efficient photocatalytic materials used as thin-films for coating large-area surfaces of common materials like plastics, metals, ceramics, etc. Upon absorption of visible light, these photocatalytic coatings generate large amounts of reactive oxygen species which, under certain conditions, are able to inactivate the SARS-CoV-2 virions adhered to those surfaces by first degrading their lipid bilayer and then, exposing the contents of these virions to further damage and thus, inactivating them fully. This is exactly what was done at INAOE in Puebla, Mexico after being financed with $5,000 USD by the IEEE HAC/SIGHT "Call for Proposals Focused on COVID-19 Response". In a record time of about 4 months, 7 large-area screen panels and almost 2,000 plastic face shields were coated with our photocatalytic films and ultimately donated to several public organizations in order to better protect the users of these simple but powerful tools against a COVID-19 infection. In this way, technology, students and colleagues as well as IEEE HAC/SIGHT, truly impact our communities even in times of global pandemics, thus confirming the IEEE motto of creating a positive impact for the benefit of humanity.

Link: https://www.youtube.com/watch?v=LtrYO0ti8ac

EDS Cares: Flood Relief for People in Selangor

BY MAIZATUL ZOLKAPLI, AHMAD SABIRIN ZOOLFAKAR, AND NORHAYATI SOIN

Continuous downpours on Friday, 17 December 2021 in Selangor resulted in extensive flooding throughout the Klang valley and major states in Malaysia. The rapid increase of floodwater forced tens of thousands of people to flee their homes causing huge losses and affecting their livelihoods. The EDS Malaysia Chapter managed immediately to organize a flood relief donation drive to provide aid to the victims. A total amount of RM1760 was raised and distributed the donation to eight families who are really in need. Besides, few EDS members took part in communal work to help clean houses of these families. We pray for their safety and may Allah replace their loss with a much better one.

~Sharma Rao Balakrishnan, Editor

EDS members volunteering during the flood incident in Selangor on 18 December 2021

Chapter News

EDS Malaysia Chapter wins Outstanding Medium Chapter Award 2021 and other awards

by P Susthitha Menon

The EDS Malaysia Chapter, chaired by AP Dr. Ir. Ts. Ahmad Sabirin won the IEEE Malaysia Section's Outstanding Medium Chapter Award 2021 during the Section's Annual General Meeting (AGM) held at the Kuala Lumpur Convention Centre (KLCC) on 12 February 2022. The purpose of the award is to recognize the outstanding performance of the best chapter among all technical chapters in Malaysia Section which have successfully served their members and the technical community by voluntary service while retaining membership size.

EDS Malaysia receiving the Outstanding Medium Chapter Award 2021, 2021 IEEE Malaysia Outstanding WIE Volunteer Award, 2021 IEEE Malaysia Outstanding Industry Volunteer Award and 2021 IEEE Malaysia Educational Activities Award from IEEE Malaysia Section

On top of that, several EDS Malaysia Excom members also received due recognition for their achievement in 2021 from IEEE Malaysia Section. They are as follows:

1) 2021 IEEE Malaysia Outstanding WIE Volunteer Award
   –AP Dr. Rosminazuin Ab Rahim
2) 2021 IEEE Malaysia Outstanding Industry Volunteer Award
   –Ir. Bernard Lim Kee Weng
3) 2021 IEEE Malaysia Educational Activities Award
   –AP Dr. Rosminazuin Ab Rahim and Dr. Aliza Aini Md Ralib

In addition, the following volunteers also received their awards from IEEE EDS Malaysia Chapter during the recent AGM on 22 January 2022.

1) 2021 IEEE EDS Malaysia Outstanding Volunteer Award
   –Ir. Ts. Dr. Maizatul Zolkapli
2) 2021 IEEE EDS Malaysia Outstanding Student Volunteer Award
   –Tan Eu Gene
3) 2021 IEEE EDS Malaysia Outstanding Industry
   –Volunteer Award
   Ir. Bernard Lim Kee Weng
4) 2021 IEEE EDS Malaysia Outstanding Portfolio Award: Educational Activities
   –AP Dr. Rosminazuin Ab Rahim and Dr. Aliza Aini Md Ralib

We would like to thank EDS for the continuous support and numerous grants bestowed to EDS Malaysia in 2021, which enabled the team to champion many activities for our EDS members and the general public. Our very active Chapters (EDS Malaysia, EDS UKM SB and EDS Penang Joint Chapter) as well as their main Excom will continue to deliver in 2022 and onwards.

Congratulations to EDS Malaysia Chapter volunteers!

Spotlight On IEEE ED NIT Silchar Student Branch Chapter's Activities

by Trupti Ranjan Lenka

The IEEE ED NIT Silchar Student Branch Chapter (SBC) was established on 6 May 2013 by Dr. Trupti Ranjan Lenka as its founder and a Chapter Advisor. Currently, the ED NIT Silchar SB Chapter is steered by Prof. Fazal A. Talukdar as the Branch Counselor, Dr. Trupti Ranjan Lenka as the Chapter Advisor, Ms. Jagritee Talukdar as a Chair and Samadrita Das as Vice Chair. This Chapter has more than 50 members including 8 Senior Members, 15 Members and 30 Student Members. The ED NIT Silchar SB Chapter and its members are very actively involved in organizing various technical/professional/social events such as Distinguished

Lectures, Mini-Colloquia (MQ), Workshops, Seminars, Short-Term Training Programs (STTP), Faculty Development Programs, International Conferences, Membership Development Programs, etc.

Virtual Adaptability: Due to the COVID-19 pandemic, the organization of in-person activities has come to a standstill. Then, as the virtual mode has become the norm, online meetings and webinars have become the reality and the savior to stay in touch with the community members and to continue our activities.

International Conference: The ED NIT Silchar SB Chapter in association with IEEE Kolkata Section Nanotechnology Council Chapter organized the *1st International Conference on Micro/Nanoelectronics Devices, Circuits and Systems* (MNDCS-2021) which was held during 29–31 January 2021 in a virtual mode. During the conference 8 keynotes, 4 invited talks and 56 oral presentations of research works were held. The conference helped in providing opportunities to young scholars to showcase their talent and connect with their peers, researchers and experts from all parts of the country and from abroad. This initiative was very well received both by the student members and academia.

COVID-19 Awareness: A COVID-19 awareness program was organized on 19 April, 2021 in hybrid mode at NIT Silchar It was followed by distribution of masks and sanitizers.

Distinguished Lectures: The SB Chapter and its members have always emphasized on organizing DL talks, invited talks, workshops and outreach activities to foster learning and innovation among the students for the benefit of the society. The technology proved to be a boon to connect not just with the local, but with the global experts. The SB Chapter organized 7 distinguished lectures on various emerging topics relevant to electron devices, delivered by eminent DLs from Europe, USA, and Canada. These lectures were impossible to conduct as in-person events. Each DL talk had more than 80 attendees including students, faculty members and participants from different parts of the country as well as from the world.

International Workshop: The International Workshop on *Optimization and Intelligence in Electronics Engineering Applications (OIEEA-2021)* was organized by the SBC during 26–30 July 2021 in a virtual mode. In this program 10 speakers (6 from foreign and 4 from India) delivered talks to 255 participants.

Faculty Development Program: A Five-Day Faculty Development Program on "*Recent Trends in Bio-MEMS and Medical Micro Devices: From Device to Application*" was organized 20–24 August 2021 through ATAL Program of AICTE. 14 speakers (2 from Finland and Italy and 12 from India) delivered lecturers and 200 participants attended the program.

Winter School: The SBC organized virtually the 1st ever IEEE EDS sponsored Summer School during 1–5 September 2021 with 20 invited lectures by experts from all over the globe. Around 100 participants from India and abroad, including EDS members and non-members, successfully completed the course. The organization of the EDS Summer School was a great success.

Students' Seminar: Apart from the technical events presented above, a Students' Seminar was held in a hybrid mode with technical presentations on "*Emerging Topics of Micro/Nanoelectronics and VLSI Design*". It was organized in a hybrid mode during 23–24 November 2021 at the Department of ECE, NIT Silchar. The program was attended by around 30 EDS members and student members.

Membership Development: The growth of any organization or society by leaps and bounds, largely depends on its volunteers and their passion to work towards a common cause or goal. The volunteers of this SBC always take up the task to relentlessly work towards achieving the goals of IEEE and EDS in the advancement of technology. The ED NIT Silchar SB Chapter organizes a membership development program from time to time to spread the awareness of EDS membership and its benefits for the betterment of the society. New student members are also given complimentary membership through the EDS Membership Fee Subsidy Program.

Awards and Recognition: The efforts were well appreciated and acknowledged by IEEE Electron Devices Society. On 26 November 2021 the ***Electron Devices NIT Silchar Student Branch Chapter*** received the ***2021 Student Branch Chapter of the Year Award*** for the outstanding contributions of the Chapter throughout the year.

Social Networking: The 1st Annual Social Meet 2021 was organized on 25 December 2021 to witness the celebration of *Merry Christmas* at Borakhai Tea Garden, Silchar, Assam comprising of Peer Networking, Visit to Tea Estate, Meet, Ex-Com meeting, and enjoyment with lots of fun with families and children and EDS Students' Members.

This SB Chapter takes pride in its capable leadership over the years and common technical interests of its members. Consistent and persistent effort by the members and volunteers in conducting versatile activities have been the salient features of the chapters' success story. In all, 2021 proved to be a very successful and remarkable year in terms of the knowledge transformation that took place through these events and reaching out to a wider audience like never before.

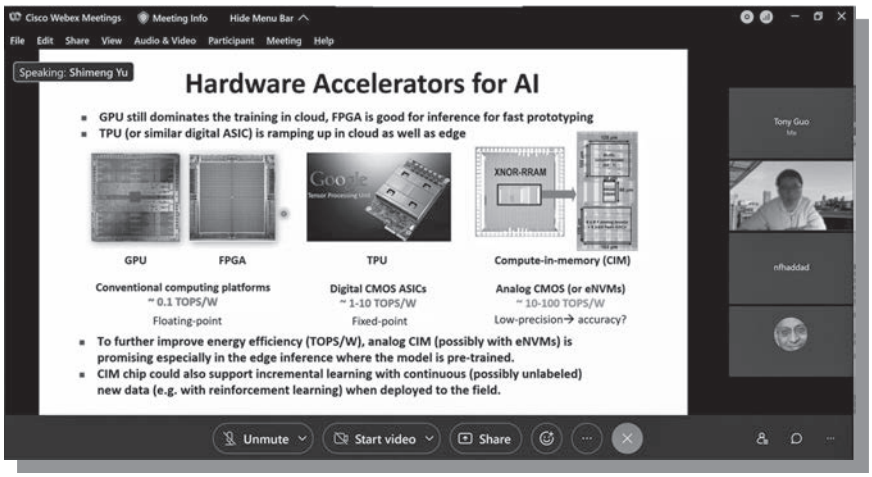
USA, Canada & Latin America (Regions 1–6 & 7)

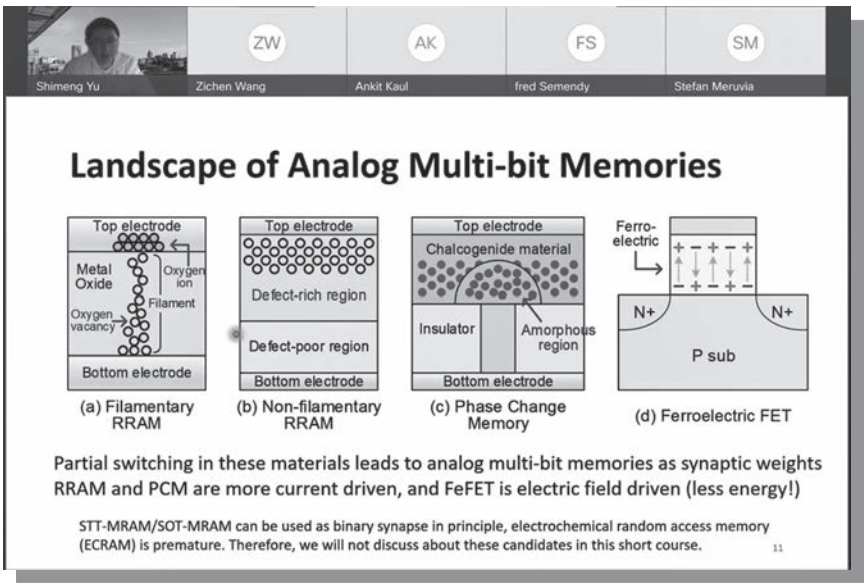
Northern Virginia/Washington Chapter Hosts Distinguished Lecture on "Landscape of Synaptic Weight Memories" by Prof. Shimeng Yu (GIT)

—by Xiangyi "Tony" Guo

The EDS Northern Virginia/Washington Chapter hosted a Distinguished Lecture (DL) on "Landscape of Synaptic Weight Memories" by Prof. Shimeng Yu of Georgia Tech on 11 November 2021. The DL was co-hosted by the Nanotechnology Council Chapter and co-sponsored by EDS Baltimore and Atlanta Chapters. Prof. Shimeng Yu started with the state-of-the-art synaptic devices with a focus on resistive and ferroelectric devices, then highlighted the key device properties that are required for on-chip inference and/or training of deep neural network (DNN) models. He covered the variability and reliability characterization at array-level and then introduced an end-to-end benchmark framework DNN+NeuroSim that is interfaced with PyTorch to evaluate versatile device technologies for DNN inference. A demonstration of the integration of RRAM with peripheral CMOS at 40 nm for a complete compute-in-memory prototype chip was presented in the end. The Q&A section discussed Google TPU devices, ADC speed rate, and future perspectives. Prof. Yu also described the EDS mission, activities and benefits of membership. The DL was attended by 24 IEEE members and six guests.

The lecture video recording and presentation slides can be accessed through vTools, event (ID:284899) Media section. This event is one of the five held in 2021 by the Northern Virginia/Washington Chapter.





Two slides from presentation "Landscape of Synaptic Weight Memories" by Prof. Shimeng Yu, 11 November 2021

2021 IEEE EDS Fall School

—by Mukta Farooq

The Mid-Hudson Valley and Schenectady EDS chapters jointly hosted and organized a two-day "Fall School on Semiconductor Device Technology" 25–26 October 2021. This Fall School, conducted in a live-virtual short course format, was open to both students and professionals and featured subject matter experts and technology leaders across key areas of electron devices and related topics.

Day 1 began with EDS introductory slides shared by Dr. Mukta Farooq, Chair Mid-Hudson EDS, which explained the mission and actions of EDS. Next were opening remarks from Dr. Mukesh Khare, VP of IBM Research and Dr. Tod Laursen, President of SUNY, which were very laudatory towards this effort. They emphasized both the importance of semiconductor technology and the need to educate the next generations in this

Jointly hosted by the EDS MID-HUDSON & EDS SCHENECTADY CHAPTERS

AGENDA – MONDAY, OCTOBER 25 (Times in EDT)

08:30 – 09:00 Opening Remarks – Mukesh Khare, IBM and Tod Laursen, SUNY Poly
09:00 – 10:30 **Santosh Kurinec** (RIT) – MOSFETs: Introduction, Evolution to State-of-the- Art devices
10:30 – 11:00 *Short Break*
11:00 – 12:30 **Rajendra Singh** (Clemson University) – Semiconductor Manufacturing
12:30 – 01:30 *Lunch (Provided for)*
01:30 – 03:00 **Fernando Guarin** (Global Foundries) – Reliability
03:00 – 03:30 *Short Break*
03:30 – 05:00 **Madhavan Swaminathan** (Georgia Tech) – Packaging Design Elements

AGENDA – TUESDAY, OCTOBER 26 (Times in EDT)

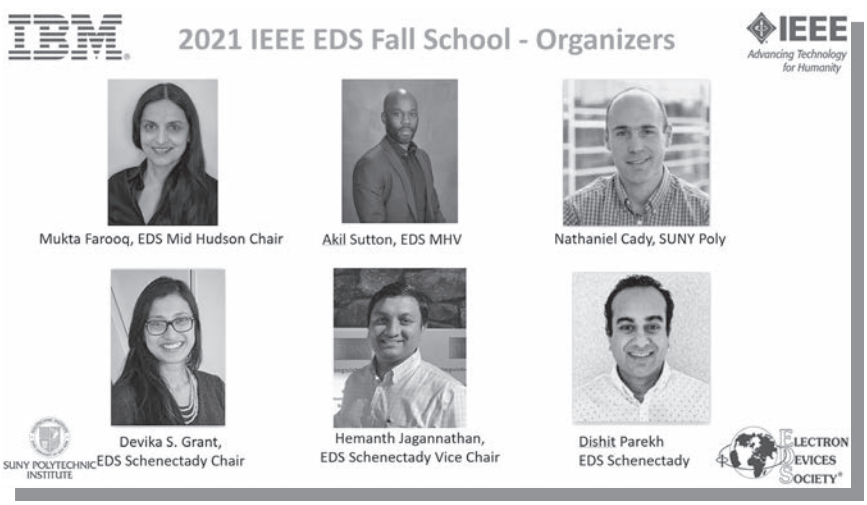
08:45 – 09:00 Opening Remarks – Day 2
09:00 – 10:30 **Onur Mutlu** (ETH Zürich and Carnegie Mellon University) – Memory
10:30 – 11:00 *Short Break*
11:00 – 12:30 **Colin McAndrew** (NXP Semiconductors) – Compact Modeling and Statistical Modeling of Semiconductor Devices
12:30 – 03:00 Lunch (Provided for) & Lightning Talks
03:00 – 04:30 **James Lu** (RPI) – 3D & HI
04:30 – 05:00 Concluding Remarks

critical field, a timely message given the backdrop of global supply chain constraints. With that as a great kick off, we unrolled the agenda to our audience, composed of registrants from Region 1 (Northeast USA), Region 8 (Africa, Europe, Middle East), and Region 10 (Asia Pacific). Special kudos to our Region 8 and 10 attendees who logged in to the lectures, no matter how late it was in their time zones.

Below is a snapshot of the agenda, on Days 1 and 2, where lectures were prepared and delivered by Prof. Santosh Kurinec, Prof. Rajendra Singh, Dr. Fernando Guarin, Prof. Madhavan Swaminathan, Dr. Colin McAndrew, and Prof. James Lu. After each lecture of 75–80 minutes, the audience was invited to ask questions to the instructors, either in live audio format or written in the chat forum. One of 5 organizers moderated each lecture to facilitate the smooth running of the session, and the transmission of questions where needed. On Day 2, a special session of graduate student attendees was organized by Prof. Nathaniel Cady, where students were invited to present 5-minute lightning talks focused on their research. This was done to enable the graduate students to present in a technical forum, and to field questions in their burgeoning areas of expertise.

The event was posted on IEEE vTools platform, and publicized through various channels, including EDS, IEEE Region 1 announcements, and internally in various organizations and academic institutions, through email. Registrations required a nominal fee of $50 for early birds, and $100 for regular attendees (after Oct 10). Early birds were all mailed a complimentary copy of the text book "Guide to the SOTA Electron Devices" by Joachim Burghartz, which we had purchased from EDS with some of the funds we received for the EDS Fall School. In addition, all attendees who paid either of the above amounts, were given lunch coupons for both days. The coupons could be deployed using a food delivery service, to enable attendees to get a hot lunch during both days of the event. A special deeply discounted registration fee was used for Regions 8 and 9. All those who attended the 2 days were mailed a Course Completion Certificate. Additionally, all registrants were emailed pdf copies of the presentations. We, the organizers were gratified to receive comments from attendees, both students and professionals, indicating the satisfaction they felt with the layout of the course, and the delivery of content from the instructors. A sampling of these comments follows:

- *"Hi Dr. Kurinec, Thank you for your amazing presentation! It was the most comprehensive, well-explained and informative lecture on MOSFET and its future trend I have ever seen." – A student.*
- *"I would like to thank you immensely for organizing such an exceptionally rich, informative, engaging and exciting program! Really looking forward to today's sessions" – Professional/Faculty Member.*
- *"Hats off to all of you for taking leadership in arranging the EDS Fall School. We need to bring young blood in EDS and this is one of the best ways to keep momentum going on." – Professional/Faculty Member"*
- *"We would like to thank you immensely for the wonderful experience that the EDS Fall School offered to both students and faculty. The technical content, choice*



of speakers, diversity and comprehensiveness of topics was truly exceptional and extremely rich and valuable. The student feedback about their experience in the Fall School was great, and I also benefited a lot myself during all of the sessions that I attended." —Professional / Faculty Member.

The list of volunteer organizers is as follows:

Mukta Farooq, Chair—EDS, Mid-Hudson Valley, Devika Grant, Chair—EDS, Schenectady, Akil Sutton, Vice Chair—EDS Mid-Hudson Valley, Hemanth Jagannathan—Vice Chair, EDS Schenectady, Nathaniel Cady—Faculty, SUNY Polytechnic, Dishit Parekh—Member, EDS Schenectady.

On behalf of all the organizers, I would like to express our gratitude to EDS for the funding, to the instructors for the great lectures, and to the attendees for making this a fruitful venture. We hope to continue this effort in 2022 and beyond.

~ Rinus Lee, Editor

4th IBM IEEE CAS/EDS AI Compute Symposium (AICS'21)

—by Rajiv Joshi, Arvind Kumar, Matt Ziegler

The 4th IBM IEEE CAS/EDS AI Compute Symposium, known as (AICS'21), was held over two days (13–14 October 2021). The event was very well attended and received great responses from the audience all over the world. The Symposium was also an initiative supported by IBM Academy of Technology (https://www.ibm.com/blogs/academy-of-technology/). Dr. Joshi has been the main interface for CAS and EDS for organizing this successful event. This is the second time the event was organized as a virtual symposium. The audio/video presentation on this virtual platform went smoothly.

More than 2400 viewers over two days, participation from 50 countries, over 54 student posters, best paper poster awards, excellent panel discussions, 11 distinguished speakers from industry and academia were the salient features of this Symposium. There were more than 5200 views on the LinkedIn post about the Symposium. The theme of the Symposium was "From Ground up to Cloud". In short, the Symposium covered a range of topics from device technology, to circuits, architecture, and algorithms -- to make innovations for the cloud with an emphasis on green Artificial Intelligence (AI).

Prof. Hoi-Jun Yoo (Professor of School of Electrical Engineering and the director of the System Design at KAIST, Korea) opened the Symposium with his excellent presentation related to "Training on Chip – Next Wave of Mobile AI Accelerators". Most mobile Deep Neural Network (DNN) accelerators target only inference of DNN models on edge devices, whereas on-device training was out of reach in mobile platforms due to its excessive computational requirements. Training-on-Chip (ToC) with user-specific data is becoming more important than ever because of privacy issues and communication latency of training on remote servers. He highlighted a number of approaches in realizing ToC. General purpose hardware and software co-optimization techniques aiming to maximize throughput and energy-efficiency of DNN training were brought out with examples, such as, sparsity exploitation and bit-precision optimization for training. In addition, application specific training accelerators for Deep Reinforcement Learning (DRL) and Generative Adversarial Network (GAN) were discussed, touching on issues regarding system implementation with the fabricated silicon.

Dr. Teo Laino (IBM Distinguished Research Staff Member) followed up with a very interesting talk about "A Cloud-based AI-driven Autonomous Lab". One of the most significant outcomes of chemistry is the design and production of new molecules. The application of domain knowledge accumulated over decades of laboratory experience has been critical in the synthesis of many new molecular structures. Nonetheless, most synthetic success stories are accompanied by long hours of repetitive synthesis. Automation systems were created less than 20 years ago to assist chemists with repetitive laboratory tasks. While this has proven to be very effective in a few areas, such as high-throughput chemistry, the use of automation for general-purpose tasks remains a tremendous challenge even today. Automation necessitates that chemistry operators write different software for different tasks, each of which codifies a specific and distinct type of chemistry. Meanwhile, in organic chemistry, Artificial Intelligence (AI) has emerged as a valuable complement to human knowledge for tasks such as predicting chemical reactions, retrosynthetic routes, and digitizing chemical literature.

Dr. Laino's talk highlighted the first cloud-based AI-driven autonomous laboratory implementation. The AI assists remote chemists with a variety of tasks, including designing retrosynthetic trees and recommending the correct sequence of operational actions (reaction conditions and procedures) or ingesting synthetic procedures from literature and converting them into an executable program. The AI self-programs the automation layer and makes decisions on synthesis execution using feedback loops from analytical chemistry instruments, with supervision from synthetic chemists. Dr. Laino presented the AI core technology and how it performs across different types of synthetic tasks.

Subsequently, Mr. Gunnar Hellekson (Vice President at Red Hat) gave an exciting talk about an open approach to AI and its integration into the cloud. Business innovation is driven by big ideas, moving faster than ever before. Today, we can do things we could only dream of a few years ago. Massive global changes are shifting the way people live and work

and require organizations to rethink their teams, processes, and technologies to stay competitive. Today, organizations across all geographies and industries can innovate, create more customer value and differentiation and compete on an equal playing field. This new reality demands that enterprises embrace digital transformation and pivot quickly or fail. AI is a critical part of the digital transformation journey for many organizations. Smart cities, wearable health technologies, smart energy grids, autonomous vehicles, manufacturing, and agriculture are just some of the key markets being transformed by AI. Mr. Hellekson pointed out how technology, open source communities and new ways of collaborating are driving business innovations like AI. AI investments across every industry are accelerating to develop differentiated services and gain competitive advantages. The difference between complex hardware and software for key elements like security, data is diminishing. Many businesses are aware of the benefits, but there are a number of challenges delaying their implementation plans. This is the natural home of open source, providing the components and foundation, and creating a space for innovators to come together and share their great ideas in a way that's self-sustainable.

Next, Dr. Evgeni Gousev (Senior Director at Qualcomm) gave a wonderful overview of tinyML: enabling ultra-low power machine learning at the very edge. In his talk, he covered many aspects such as tinyML fundamentals, its markets and values, and gave many examples. He discussed recent developments from Qualcomm and provided information about the tinyML foundation, ecosystem, projects and events and educational activities. Dr. Gousev further defined tinyML as machine learning architectures, techniques, tools, and approaches capable of performing on-device analytics for variety of sensing modalities (vision, audio, motion, chemicals, etc.) at the mW

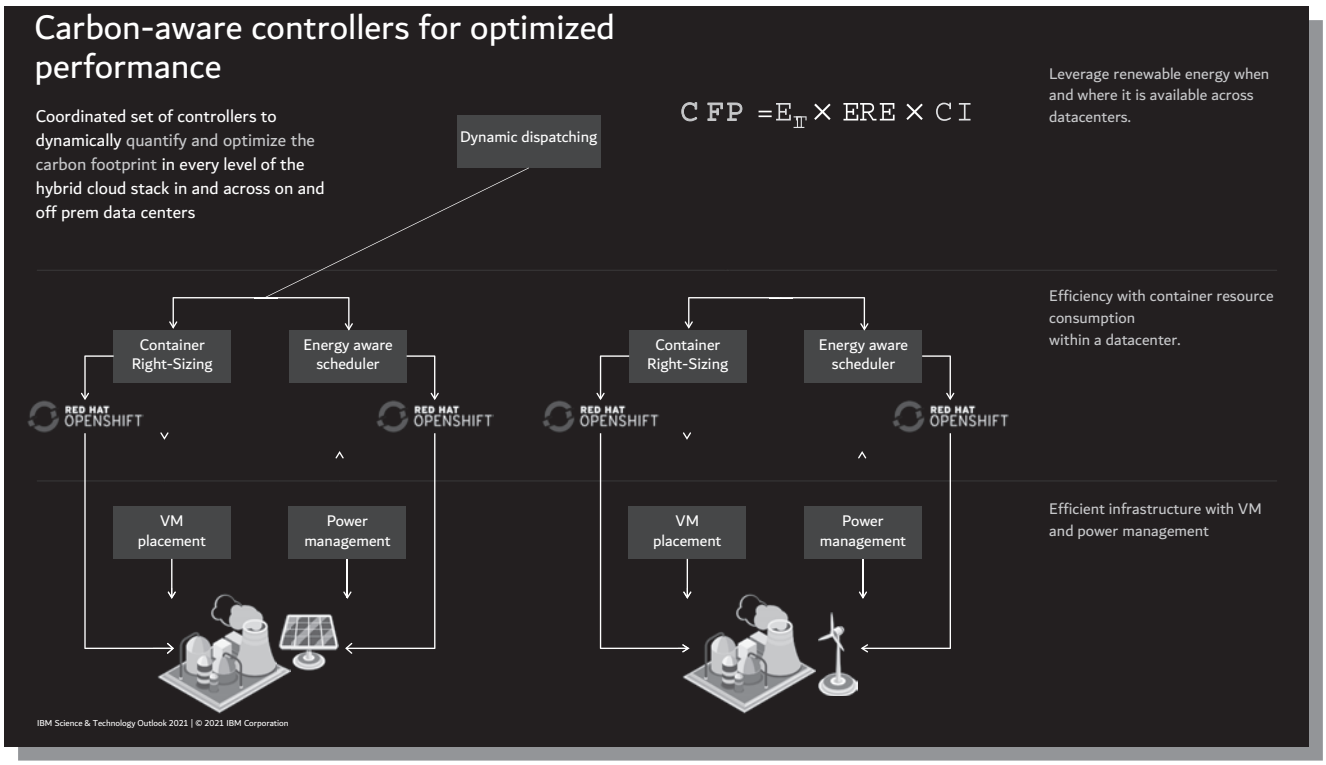
Dr. Tamar Eilam

power range or below, targeting predominantly battery-operated devices. The key tinyML growth drivers include more efficient hardware, energy efficient algorithms, more mature software infrastructure, tools, diverse ecosystems, growing the number of applications, corporate investment, VC investment, and increased startups. It is predicted that 1B tinyML devices would be shipped in 2024 and would approach 5.4B in 2026. The growth is in double digits. He described many useful applications of tinyML, such as, voice recognition, environmental sensors, predictive maintenance, gesture control, and augmented reality.

The final talk on the first day was given by Dr. Venkat Thanvantri (VP of Machine Learning R&D at Cadence). He presented advances in AI/ML for chip design. The emergence of machine learning (ML) has unlocked many new applications and transformed user experiences. Electronics Design Automation (EDA) is an application area that delivers value by providing automation and abstraction. ML technology is having a similarly transformative impact on EDA, accelerating execution of algorithms, improving quality of results, and now significantly improving the productivity of users. In particular, the speaker detailed the use of Reinforcement Learning to automate and optimize results for the digital design and signoff flow.

On the second day of the Symposium, Dr. Suk Hwan Lim (Executive VP at Samsung) addressed fine grained domain specific architectures for diverse workloads. He covered deep learning applications and workloads, domain specific neural processing units/accelerators (NPU), and future directions for NPUs. There are several deep learning (DL) applications – speech recognition, voice activation, text to speech, authentication, image classification, object detection, semantic segmentation and image processing, among others. Training is typically implemented in the cloud, while inference is deployed on the edge. The compute complexity varies by 5-7 orders of magnitude for these applications. Thus, Dr. Lim categorized fine grained diverse processors for diverse applications – micro NPU for audio/always-on applications, general NPUs for small spatial resolutions with deep networks, and image processing NPUs for large special resolutions with shallow networks. Significant improvements in energy, area, efficiency and utilization are needed and can be achieved through algorithms/compiler/architecture/circuits.

Next, Prof. Song Han (Assistant Professor at MIT) described the role of tinyML and how greener AI can be achieved. TinyML and efficient deep learning make AI greener and easily deployable to IoT. AI applications can generate high power and have detrimental effects on the environment. There is a push for data compression, pruning, and other techniques to reduce computation and thereby power. New models can be developed to improve latency and accuracy. Manual design is challenging and automation is needed. Prof. Han has proposed and developed a hardware-aware neural network search called "Once-for-All". While computationally



A slide from the presentation "Responsible Computing " by Dr. Tamar Eilam

expensive, it requires training only once and then produces multiple models which can be used for inference. This approach reduces the data usage and results in less computation and hence a lower carbon footprint. Also, sparse attention and progressive quantization ideas are used to prune the tokens in Natural Language Processing (NLP). Activation is the main bottleneck and not the trainable parameter space. Activation minimization leads to significant memory reduction in the IoT. All the techniques described in his talk can help AI to be greener.

Following Prof. Han's talk, Prof. H.-S. Philip Wong (Willard R. and Inez Kerr Bell Professor, Stanford University) presented "N3XT-3D-MOSAIC: Domain-Specific Technology for AI Compute", noting that 21st century applications are going to be data-centric. Data analytics, machine learning, and AI applications are going to dominate, from data center to mobile and IoT, from collecting and processing, to curating the data, to deriving information. Many systems will need to learn and adapt on the fly. Three-dimensional integration is one of the major technology directions for integrated circuits. Prof. Wong gave an overview of the new materials and device technologies that may need to be developed to realize monolithic 3D integration with multiple logic transistor and memory device layers. He gave two examples of compute-in-memory chips that feature RRAM integration with CMOS logic as an illustration of how future 3D systems may be designed.

Dr. Steve Pawlowski (VP at Micron Technology) next talked about rethinking the memory-compute subsystem. The best machines struggle on workloads requiring higher memory and network performance. The challenge remains to improve overall systems design starting with memory. Dr. Pawlowski described evolving usage models driving compute demands that require vast amounts of data. He suggested current system bottlenecks will get worse unless something is done. New memory-compute architectures will have the greatest impact on systems. However, new architectures will take time to evolve. Market driven use cases can speed adoption. Integration of compute into memory to get greatest energy and performance is a key. New devices must build from and evolve the dominant software ecosystem. Many future neural networks will require higher bandwidths, which increases energy consumption. Memory energy is interconnect dominated. Memory bandwidth is also pin and locality dominated. A closer coupling of memory and compute is the path forward.

Subsequently, Dr. Pradeep Dubey (Senior Fellow at Intel) gave a great talk about the "Era of Ubiquitous AI". Artificial intelligence (AI) is touching, if not transforming, every aspect of our lives. AI is impacting not just what computing can do for us, rather how computing gets done. Fast-evolving AI algorithms are driving demand for general-purpose computing that cannot be met by "business as usual" engineering. At the same time, programmers are often data scientists,

not computer scientists; expecting programmers to figure out increasingly complex hardware on their own just doesn't work. Architects are therefore needed more than ever – chip architects to create new processors, systems architects to design new data centers, software architects to design new frameworks, and AI architects to churn out new models and new algorithms. Are we up to the task? Or do we need to augment human architects with AI to meet the challenge?

The Symposium's concluding talk was given by Tamar Eilam (IBM Fellow). She presented IBM's initiative related to sustainable and responsible computing. IBM traditionally has focused on privacy of data, security, and ethics. Another key consideration is reducing carbon footprint (CF). For example, some AI jobs consume CF equivalent to that of the lifetime of 5 cars. It is predicted that electricity usage in the datacenter would increase by 8% by the year 2030. CF is driving AI to move to the cloud. It is crucial to quantify Carbon Footprint Energy (CFE), which is defined as the product of IT equipment energy, power usage effectiveness (overhead power conversion and cooling), and source of the energy (coal, nuclear, etc.). Organizations need to report CFE to discover hot spots and optimize. To make greener AI, the use of renewable energy, controlling the data utilization, and finding alternate ways to reduce power are essential. In order to do this, workloads need to be monitored, enabling a breakdown of CF by cloud tenant and application.

The Symposium also featured a poster session, organized into 3 parallel tracks. Out of 54 posters, the top 3 best posters were awarded from each track. The list of winners is given on the Symposium website: https://www.zurich.ibm.com/thinklab/AIcomputesymposium.html

The Symposium closed with a panel discussion on Responsible Computing, with four distinguished panelists including Tamar Eilam (IBM), Irena Risch (McGill), Evgeni Gousev (Qualcomm), and Bouchra Bouqata (Amazon). Panelists addressed questions spanning a range of controversial topics, including the environmental impact of datacenter workloads, building trust in AI, eliminating bias in AI, and ensuring data privacy.

Replays of entire two-day Symposium are available on the Symposium website: https://www.zurich.ibm.com/thinklab/AIcomputesymposium.html

Europe, Middle East & Africa (Region 8)

November Workshop of the Aachen Graphene & 2D Materials Center

—by Maike Meyer-Amjadi

On 15–16 November 2021, the Aachen Graphene & 2D Materials Center held its annual workshop in person, in the beautiful coulisse of the SuperC—one of the most scenic buildings of RWTH Aachen University. After almost two years of pandemics, the workshop was an occasion for the Center members to come together, to present and discuss new results and research directions, to reinforce collaborations and establish new ones.

Founded in 2017 as joined initiative of RWTH Aachen University and of AMO GmbH, the Aachen Graphene & 2D Materials Center is a competence center that brings together the complementary expertise and the facilities of Aachen's leading research groups in the field of graphene and two-dimensional (2D) materials. The activities of the Center cover the entire value-chain needed to bridge the gap between basic science and applications, ranging from material science and fundamental physics, through device design and analytics, to manufacturing.

Organized as an internal event, the workshop counted around 100 participants from RWTH Aachen University and AMO GmbH, as well as from cooperating partners such as Aixtron, Infineon, Protemics, ForschungsZentrumJülich, and the regional think-tank Cluster MNWP.NRW. Speakers of the event were the Center's Principal Investigators (see below), as well as Prof. Michael Heuken, Vice-President Advanced Technologies at Aixtron SE and Dr. Gordon Rinke, deputy of the 2D-Experimental Pilot Line at AMO GmbH.

Group picture of the workshop's participants (source: AMO GmbH)

The topics covered in the events spanned a very broad range – from flexible electronics, to quantum devices, from the fundamental properties of graphene and van der Waals heterostructures to high-frequency electronics, and (bio-) sensors. A major highlight of the event was the poster session, with more than 40 posters covering all available stands and walls in the room, and many fruitful discussions and new collaborations forming on the horizon.

The workshop was organized as a hybrid event, with about 20 participants joining via zoom, and the large majority enjoying the face-to-face meeting at SuperC, which took place under strict hygiene requirements: all participants had to present a valid EU Covid-certificate, perform an antigen test before entering the workshop area, and wear masks during the event.

"It was great to have all these in-person discussions", says the spokesperson of the Center Prof. Max Lemme, "For many of the younger students this was the first real-life conference – the first time they could really enjoy discussing their work with scientists and peers outside their research group. For everyone it was really interesting to have a closer look at what is going on in other groups, to learn about different research questions and different methods. There is nothing like a change of perspective to generate new ideas!"

Workshop Program—Monday, 15 November 2021:

- Prof. Dante Kennes (Institute for Theory of Statistical Physics, RWTH), "Moiré heterostructures: a condensed matter quantum simulator"
- Dr. Zhenxing Wang (AMO GmbH), "Flexible Electronics with Graphene: From Devices Towards System"
- Dr. Annika Kurzmann (II Institute of Physics A, RWTH), "2D materials for quantum networks"
- Prof. Christoph Stampfer (II Institute of Physics A, RWTH), "Bilayer graphene for quantum electronics"
- Prof. Michael Heuken (Aixtron SE),"Large area deposition of high quality 2D materials" Dr. Gordon Rinke (AMO GmbH), "The 2D Experimental Pilot Line at AMO"
- Prof. Sven Ingebrandt (Institute of Materials in Electrical Engineering 1, RWTH) "Biosensors based on two-dimensional materials and interfaces: fundamentals, opportunities and challenges"
- Prof. Daniel Neumaier (Bergische Universität Wuppertal & AMO GmbH), "Stable TMDC encapsulation and flexible logic circuits"

Poster Session—Tuesday, 16 November 2021

- Prof. Max Lemme (AMO GmbH
- & Chair of Electronic Devices, RWTH), "Electronic Devices based on 2D Materials: MEMS, Photodiodes and Memristors"
- Prof. Markus Morgenstern (II Institute of Physics B, RWTH), "Scanning probe microscopy on exfoliated 2D materials"
- Prof. Andrei Vescan (Compound Semiconductor Technology, RWTH), "Metal-organic vapor phase deposition of 2D-TMDCs"
- Prof. Renato Negra (Chair of High Frequency Electronics, RWTH), "Graphene for high-frequency electronics"
- Prof. Joachim Knoch (Chair of Semiconductor Electronics, RWTH) "Multigate Field-Effect Transistors"

Benjamin Iñiguez DL on "Roadmap of Flexible Electronics"

—by Mike Schwarz

Prof. Iñiguez from the Department of Electronic, Electrical and Automatic Engineering, University Rovira i Virgili, Spain wanted to hold the distinguished lecture in person at the NanoP Competence Center of the Technische Hochschule Mittelhessen (THM)—University of Applied Sciences in Gießen, Germany. However, due to the increasing number of people infected by COVID in Germany and Europe and due to the announced new regulations, the lecture organizer—EDS Germany Chapter, the lecture co-sponsor—THM, and Prof.

Benjamin Iniguez showing the technology status and potential solutions for flexible electronics

Iñiguez decided to shift the planned hybrid lecture to a fully virtual mode. This was the only option which made sense in that situation. The distinguished lecture on **"Roadmap of Flexible Electronics**" was held online on 23 November 2021. The DL was attended by 33 IEEE participants, as well as other non-IEEE members.

Benjamin's distinguished lecture gave an overview and perspective on the concept roadmap of flexible electronics. The talk gave some market share values and focused on the most promising organic and oxide semiconductor materials. Different devices, their applications and potential stakeholders were shown. Afterwards, a technology status was reported by Prof. Iñiguez, including the challenges and potential solutions.

The lecture finished with some recommendations with focus on modeling, especially where modeling can support technology finding solutions. The lecture concluded with highlighting an increasing demand by wearables and the need for flexible electronics which are biodegradable.

Sorin Cristoloveanu DL on "Revolutionary Nano-Devices With Electrostatic Doping"

—by Mike Schwarz

He was dressed very well, wearing a jacket and a suit. We are talking of a virtual meeting of course. Profession is his second name! Whom are we talking about? Sorin Cristoloveaunu for sure… I met him for the first time in Grenoble in 2011, when I was a PhD student, now we share thoughts during a distinguished lecture. Isn't that crazy???

The distinguished lecture on **"Revolutionary nano-devices with electrostatic doping"** was held on 25 October 2021. It was organized by the EDS Germany Chapter and co-sponsored by the NanoP from THM—University of Applied Sciences and University Rovira i Virgili. The DL was attended by 17 IEEE participants, as well as other non IEEE members.

The distinguished lecture of Sorin from IMEP-LAHC, Minatec, France gave an outstanding perspective on the concept of electrostatic doping, offering advantages and examples of different types of devices, e.g. Charge Plasma Devices, RFETs, Carbon Nanotube Electrostatic Devices, and many others.

After introducing the topic and giving typical applications of NWs and 2D materials, Sorin illustrated the electrostatic doping by the "Hocus-Pocus Diode". He showed different configurations due to electrostatic doping (see picture) which led finally to a fully virtual diode. The metamorphosis of several PIN diodes and its impact on their IV characteristics, as well as the metamorphoses of the TFETs, Z^2-FETs and their applications were presented. A comparison of the Field-Effect Diode (FED), Z^2-FET and Z^3-FET concluded the part of the talk on FDSOI devices with electrostatic doping. It was an honor to meet Sorin again after so many years and to have with him a great virtual dinner in the evening.

~ Mike Schwarz, Editor

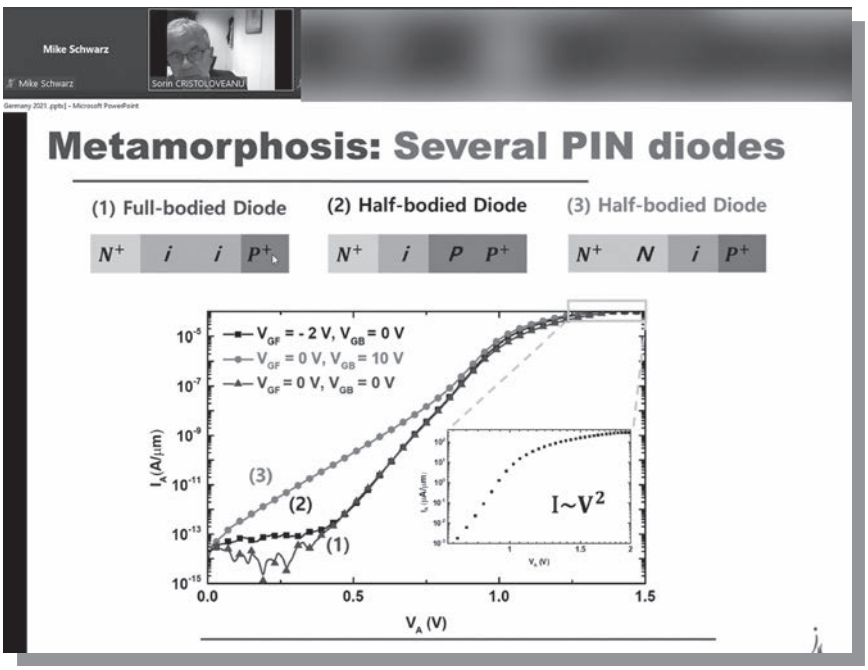
The 17th European Microwave Integrated Circuits Conference (EuMIC) 2022

26–27 September 2022, Milano Convention Centre

EuMIC 2022

The 17th European Microwave Integrated Circuits Conference

The 17th European Microwave Integrated Circuits Conference (EuMIC), as part of the European Microwave Week 2022, is a 2 days event scheduled for 26 - 27 September 2022 in the Convention Centre in Milan, Italy. The EuMIC conference is jointly organized by the GAAS® Association and EuMA, and is the premier European technical conference for RF and microwave electronics, and opto-electronics. It has established itself as a key contributor to the success of the overall European Microwave Week and remains the largest scientific event in Europe related to microwave integrated circuits.



Sorin Cristoloveanu showing the metamorphosis of several PIN diodes and its impact on their IV characteristics

The aim of the conference is to showcase recent notable achievements and trends within industry and to encourage the exchange of scientific and technical information covering a broad range of high-frequency related topics, from materials and technologies to integrated circuits and applications; encompassing all relevant aspects such as theory, simulation, design, and measurement. Research and innovation in this field help to create the crucial enabling infrastructure for new and emerging information and communication applications.

Whilst traditionally, the EuMIC conference has focussed mostly on III-V semiconductor technologies, we are particularly keen to encourage more Si based contributions as we recognise the rapidly progressing applicability of CMOS/SOI solutions for microwave/millimeter-wave applications.

Technical Sessions

The EuMIC 2022 solicits papers within the following broad technical areas:

- Modeling, Simulation of Devices *and Circuits*
- Technologies, Devices and IC-Processes
- Integrated Circuit Design
- Emerging Techn*ologies and Applications*

Lively industrial panel sessions, Focus and Special Sessions will also be organized. Keynote speakers from industry and academia will present invited talks on hot topics. Tailored short-courses and workshops will complement the programme.

Publications

EuMIC 2022 papers will be subjected to a standard review process and IEEE conference publishing guidelines. The accepted papers presented at the meeting will be available to download electronically and will be published on IEEE *Xplore*. Selected papers will also be nominated by the TPC for a Special Issue of the International Journal of Microwave and Wireless Technologies, published by Cambridge University Press. This Special Issue will be published in open access, with the article processing charges covered by the European Microwave Association (EuMA).

Awards

The Best Conference Paper and the Young Engineer Paper will be awarded by the EuMIC Technical Programme Committee and the EuMW Steering Committee.

As part of the fellowship award, an essay competition is also promoted to students enrolled in a full time Ph.D. or graduate degree programme in microwave electronics. Applications should be sent to the email address brazilaward@eumw2022.org by 1 September 2022.

Reduced registration fees are offered for students as well as senior persons aged 65 years or more. The European Microwave Association will also provide up to six student grants of €750 and free EuMIC registration, https://www.eumweek.com/students/StudentOverview.html

Important Dates

- 25 March 2022: Abstract submission deadline
- 6 June 2022: Notification of acceptance

COVID-19 Watch

Milan remains safe. EuMIC 2022 is planned as an in-person/on-site event. Meanwhile, we are closely monitoring the development of the global COVID-19 outbreak. A contingency plan will allow virtual presentations and participation for those with travel restrictions and concerns. Both safety and participation experiences will be ensured for EuMIC 2022, https://www.eumweek.com/conferences/eumic.html

Paolo Colantonio
University of Roma Tor Vergata, Italy
EuMIC 2022 Chair
eumic.chair@eumw2022.org

Latin America (Region 9)

ED Puebla Chapter

IEEE EDS Distinguished Lecture: Reliability of Nanoscale Semiconductor Devices, Focusing on but not Limited to Noise and Bias Temperature Instability

—by Joel Molina-Reyes

On 22 November 2021, Prof. Gilson Wirth from the Electrical Engineering Department at the Universidade Federal do Rio Grande do Sul (UFRGS) delivered an online Distinguished Lecture on the topic of "Reliability of nanoscale semiconductor devices, focusing on but not limited to Noise and Bias Temperature Instability". The Lecture was given for all the graduate students and faculty members of the Electronics Department of INAOE. In this lecture, Prof. Wirth presented some of the main effects playing a major role on the reliability of today's digital and analog designs, as well as effects that are expected to become relevant in future technologies. His talk also included some modeling techniques at the physical-level and their applicability in the IC design flow.

Prof. Wirth talked extensively on the phenomena of charge capture and emission by defects (traps) that are close to the dielectric-semiconductor interface and that are known to be the major source of low-frequency noise in modern MOS devices and also play an important role in Bias Temperature Instability (BTI). The basic mechanisms involved in charge trapping and de-trapping were presented, including a critical discussion of key parameters such as trapping/de-trapping time constants and the amplitude of the fluctuations induced by single traps. Additionally, Prof. Wirth introduced a novel physics-based modeling and simulation approach that is based on the relevant microscopic quantities that play a role in

both low-frequency noise and BTI. This modeling approach is valid at both DC and large signal biasing, and may be applied to time domain (transient) and frequency domain (AC) analysis, thus showing great applicability given that time domain analysis is relevant for the analysis of digital and mixed-signal circuits. In digital circuits for example, the random-telegraph noise (RTN) chronological statistics (especially trap occupancy switching), has a direct impact on circuit performance and reliability, e.g. signal degradations like jitter happen when a trap switches state. The applicability of the model presented by Prof. Wirth, was demonstrated by the evaluation of logic gates and circuits, especially by the case study of inverters and ring oscillators. Given that our graduate students at the Electronics Department of INAOE are working in the fields of microelectronics, nanoelectronics and integrated circuit design (analog, digital or mixed), this talk was relevant and of great interest for students related to the advance fabrication and design of electron devices and circuits.

ED Costa Rica Section Chapter ED Student Chapter at Instituto Tecnologico de Costa Rica

Renewable Energies: For a Future ¡Pura Vida!

—by Danny Xie-Li, and Esteban Arias-Mendez

Human activities have been the driver of increasing greenhouse gas emissions. Costa Rica, a natural paradise, is a leading world model in the renewable energy field, intending to be the country with less dependence on burning fossil fuels. Vulnerable communities are affected in this long-term risk scenario, which requires ways to mitigate the effects. STEM education can help to develop skills and raise the scientific literature to find innovative solutions to deal with the problems of the 21st century.

IEEE EDS Summer School Costa Rica 2021, about renewable energy

In December 2021, the IEEE EDS Summer School Costa Rica 2021 took place. It was sponsored by IEEE Electron Devices Society (EDS) and organized by the EDS Costa Rican Chapter with the EDS Student Chapter at Instituto Tecnológico de Costa Rica (TEC). It had the main objective to bring together specialists and students, to introduce concepts, opportunities, and projects in fields related to electronic devices for renewable energy production.

We had more than 30 students from different engineering domains from local universities: TEC, Universidad de Costa Rica (UCR), and Universidad Invenio. The program included technical conferences, workshops, technical visits to renewable energy production plants: solar, wind, and geothermal as well as recreational and social activities. One of the special visits was to the Plasmas Lab, and also to Laboratorio de Investigación de Energía Eólica (LIENE).

Among the national prominent lecturers who collaborated with us were professor Dr. Iván Vargas with the conference *"Energy of nuclear fusion"*, professor M.Sc. Gustavo Richmond with a talk *"Introduction to Wind Energy"*, Jose Luis Uribe, from Hewlett Packard Enterprise (HPE), Mariela Vázquez and Eng. Luis Carlos-Rosales, from Intel Costa Rica, Mauro Enrique-Arias, from Instituto Costarricense de Electricidad (ICE). We had local collaboration from HPE, Aruba Networks, Intel Costa Rica, Procter & Gamble, Mobilize.NET, Sama as well as with Escuela de Computación and Unidad de Posgrado from TEC.

During the pandemic, we have seen an accelerated transformation to adopt digital technologies, which make it possible to take immediate actions with the cooperation in every front to support our society in terms of accelerating net-zero greenhouse gas emissions. We hope this Summer School helped students to be active and conscientious people about these fields.

ED Puebla Chapter

IEEE EDS Distinguished Lecture: Modeling integrated Passive Components for High Frequency Applications

—by Joel Molina-Reyes

On 2 December 2021, Dr. Roberto Stack Murphy Arteaga from the Electronics Department of INAOE delivered an online Distinguished Lecture on the topic of "Modeling integrated passive components for high frequency applications" in conjunction with our 2021 IEEE EDS Summer School on Superconducting Qubits (https://www-elec.inaoep.mx/~nanoMX/). In this lecture, Dr. Murphy presented an interesting perspective on the modeling of some of the passive components used in modern ICs that, along with

billions of transistors, form the core of the technology that we use every day in many conventional and emerging electronic applications.

Dr. Murphy stated that as technology evolves, more and more functions and applications are readily implemented using CMOS circuitry so that wireless electronics have become common in our daily life. The development of these circuits involves extensive research leading to accurate models for simulation, which have to include all the effects associated with the circuit, which are embedded in the substrate. As the frequency of operation increases, many more effects, which are negligible at lower frequencies, become apparent, up to the point that some can become dominant in the high frequency range. RF modeling of the MOS transistors has thus been the object of extensive research over the past few decades, and a continuous field of endeavor. Better models — electrical, physical, mathematical and for simulation - have to be developed on an almost daily basis since higher operating frequencies can be reached as the devices become smaller, and hence, faster. But ICs are not made solely of transistors. Many passive structures have to be built on the same chip to attain the desired function of the circuit, such as resistors, capacitors, inductors, transformers and interconnects. In this talk, Dr. Murphy presented the models of an integrated inductor and of a coplanar waveguide, compared to measurements up to 60 GHz. These are common devices now present in several modern RF ICs. An important effect associated with them are RF signal losses due to the ground shields that are built underneath these structures to reduce electromagnetic interference. Finally, Dr. Murphy gave interesting recommendations to students aiming to pursue a graduate degree in advanced applied electronics, and whose talents are required at several tech companies where R&D activities are now being focused on emerging technologies like the superconducting quantum-bit technology.

ED Puebla Chapter

2021 IEEE-EDS Summer School on Superconducting Qubits (nanoMX2021)

—by Joel Molina-Reyes

On 1–3 December 2021, INAOE virtually held the IEEE EDS Summer School on Superconducting Qubits (https://www-elec.inaoep.mx/~nanoMX/) with more than 60 undergraduate/graduate students attending from several locations across Mexico, Chile and Spain. Even though the Covid-19 global situation delayed and restricted a direct interaction between attendees, this event provided several learning options during 3 days-long program:

- 14 invited talks by 7 national and 7 foreign speakers

IEEE EDS Summer School on Superconducting Qubits (nanoMX2021)

- A virtual tour in 4 different INAOE laboratories
- A virtual lab for remote measurement of electron devices
- A virtual poster session for students
- 1 panel session "Superconducting Qubits for Quantum Science and Technology"

We planned truly interesting and easy-to-follow talks so that all of the attendees could see the importance of an emerging technology that can change the way in which data can be processed, stored and transmitted. This was achieved by studying the fundamental blocks (superconducting Josephson junction and coplanar waveguide). The covered topics were:

- Status of the microelectronics development in Mexico
- Atomic-layer deposition of ultrathin insulating films
- Advanced materials' characterization techniques
- Electron transport in nanoscaled materials
- Physics and technology of spin qubits
- Physics and technology of superconducting qubits (SQ)
- Theory, physics, modeling and simulations of SQ
- Design, fabrication and characterization of SQ
- Quantum circuits and quantum computing
- Cryogenic characterization of integrated materials and devices
- RF characterization of integrated materials and devices
- Challenges for enhanced quantum performance of SQ

The demonstration of a virtual laboratory for measuring electron devices from anywhere with internet connection, will provide a huge opportunity for many students interested in testing several electron devices and simple circuits that were fabricated at INAOE in the past. Some of these electron devices and circuits are solar cells, MOSFETs, digital inverters, differential pairs, RLC tank circuits and RC filters. This is possible since the Electronics Department of INAOE, as the first in Latin America, has enabled fabrication of CMOS-based integrated circuits (LSI scale) since 1984 and is now pursuing the development of a BiCMOS process down to a 0.35 μm technology node. For the organization of this IEEE-EDS Summer School, INAOE took advantage of their expertise and infrastructure for advanced fabrication of electron materials and devices and successfully arranged a multi-purpose event related to the topic of superconducting quantum-bit technology.

~ Joel Molina, Editor

Asia & Pacific (Region 10)

ED Malaysia Chapter

2021 ED Malaysia and RSM2021 Appreciation Ceremony and Meeting

—by Maizatul Zolkapli, Ahmad Sabirin Zoolfakar, and Norhayati Soin

The ED Malaysia and RSM2021 appreciation ceremony and meeting was held from 18–19 December 2021 at Impiana KLCC Hotel. The ceremony was held as a token of appreciation to all committee members who have contributed to ensure the success of the 2021 IEEE Regional Symposium on Micro and Nanoelectronics (RSM) which was held on 2 - 4 August 2021. In conjunction with the ceremony, the 10th IEEE EDS Committee Meeting was also held. During the meeting, the Advisor, Chair and Past Chair presented appreciation letters to all members of the committee. Prof Dato' Dr. Burhanuddin Yeop Majlis, the advisor and the founder of EDS Malaysia was honoured to give a short speech during the opening of the ceremony.

2021 IEEE EDS Malaysia Chapter Postgraduate & Undergraduate Final Year Project Award

—by Aliza Aini Md Ralib and Rosminazuin Ab Rahim

The ED Malaysia Chapter sponsored 16 awards for the 2021 Undergraduate Final Year Project (FYP) and Postgraduate Awards program which was organised by several universities in Malaysia. The awards are given to encourage the authors of FYP and of the postgraduate projects related to the field of VLSI and MEMS/NEMS to build their careers in these fields. The winners are listed below. Congratulations to all the winners!

2021 ED Malaysia Postgraduate Award Winners:

1) **Outstanding project in Material, Process and Product.**
   Name of the winner: AHMAD FAIRUZABADI MOHD MANSOR

Members of EDS during the EDS and RSM2021 appreciation ceremony

University: International Islamic University Malaysia (IIUM)
Project title: Personalised Medical Device for Optimal Chemotherapy Treatment

2) Outstanding project in MEMS & Nanoelectronics
Name of the winner: NURUL AMIRA FARHANA BINTI ROSLAN
University: International Islamic University Malaysia (IIUM)
Project title: Geometric Parameter Optimization of Screen-Printed Electrode (SPE) for electrochemical based sensing applications

3) Outstanding project in Nanophotonics
Name of the winner: UMAHWATHY A/P SUNDARARAJU
University: Institute of Microengineering and Nanoelectronics (IMEN), Universiti Kebangsaan Malaysia (UKM)
Project title: Development of MoS2/h-BN/Graphene Hybrid Photodetector for Self-Powering Application

2021 ED Malaysia Undergraduate Final Year Project Award Winners:

1) Nur Aliah Nasution from International Islamic University Malaysia, IIUM
Project title: Design and analysis of hybrid energy harvesting antenna on chitosan-based piezoelectric substrate.
2) Soumik Bhattacharjee from Manipal University
Project title: Design and finite element modelling of multi-channel quartz crystal microbalance for odour characterization of volatile organic compounds.
3) Mohd Zainal Nurdin from Multimedia University, MMU
Project title: Design and simulation of the envelope tracking supply modulator for the 5G power amplifier system.
4) Nurul Amira binti Anang Othman from Universiti Teknologi MARA, UiTM
Project title: The development of an IoT-based solar battery monitoring system.
5) Loh Jing En from Universiti Malaya, UM
Project title: Optimization of gate-all-around nanowire field effect transistor (GAA NWFET) and study of its application as a biosensor.
6) See Ying Jie from Universiti Malaysia Perlis, UniMAP
Project title: Design, simulation and analysis of MEMS Capacitive Pressure Sensor.
7) Kok Hui Yee from Universiti Putra Malaysia, UPM
Project title: Evaluation of 8-bit Vedic Multiplier using monolithic 3D integration technology.
8) Siti Nurazlina binti Zaida from Universiti Pertahanan Nasional Malaysia
Project title: Fibre based pH sweat sensor.
9) Anas Akasyah bin Abdul Patas from Universiti Sains Islam Malaysia, USIM
Project title: Ardu-electrochromic film for home safety and privacy purposes.
10) Pritigavane d/o Mogan from Universiti Teknikal Malaysia Melaka
Project title: Taguchi method analysis in designing an 18 nm graphene/TiO_2/WSix device.
11) Ng Wee Wei Ki from Universiti Tun Hussein Onn Malaysia, UTHM
Project title: CMOS-based instrumentation amplifier for biomedical application.
12) Tan Wei Lun from Universiti Teknologi Malaysia, UTM
Project title: Development and evaluation of authentication algorithm using SRAM PUF.
13) Muhammad Taufiq Asri bin Mohammad Nazari from Universiti Kebangsaan Malaysia, UKM
Project tile: Design of a low-dropout linear regulator in 0.13 µm CMOS technology.

STEM Online Workshop: Let's Make Green Electronics

—by Aliza Aini Md Ralib, Rosminazuin Ab Rahim and AHM Zahirul Alam

In the spirit of promoting STEM to the students, an online workshop "Let's Make Green Electronics" was held virtually as an educational and community service programme organised by VLSI and MEMS Research Unit, Kulliyyah of Engineering, International Islamic University Malaysia (IIUM), University of California Berkeley in collaboration with ED Malaysia and Perintis Youth IIUM Chapter. The workshop was aimed to excite the curiosity of the students through an electronic project kit training. Twelve engineering undergraduate students from five universities in Malaysia were selected to participate in the workshop (University Malaya, Universiti Pertahanan Nasional Malaysia, Universiti Putra Malaysia, International Islamic University Malaysia and Monash University Malaysia). Due to the Covid-19 pandemic, the event was conducted online where the participants were guided by trainers. The electronic kits and materials packages that were sponsored by IEEE EDS were sent to the participants.

In this workshop, the participants were trained by Prof Muhammad Mustafa Hussain from University of California Berkeley and Sister Wedyan Babatain, PhD student from King Abdullah University of Science and Technology, KAUST. The participating students were divided into 4 groups to brainstorm creative ideas for their prototype based on the kits given. In total, eight online classes were conducted by the trainers to guide participants on prototype development every weekend from 6 November

– 12 December 2021. The event ended with a prototype presentation by each group and a closing ceremony. Four projects were presented: an energy harvester, a green house monitoring, a touchless toilet system and a floor sense project. This workshop has certainly helped and benefited the students in introducing them to the real-world application of electronics and to cultivate their interests in this field and STEM. The organiser would like to thank the trainers for the guidance and volunteering student assistants making this workshop a successful one.

~Sharma Rao Balakrishnan, Editor

IEEE EDS Distinguished Lecture–ED/SSC Shenzhen Chapter

—by Shengdong Zhang

On 10 November 2021, the ED/SSC Shenzhen Chapter hosted a Distinguished Lecture given by Prof. Yang Chai, associate professor of the Department of Applied Physics at Hong Kong Polytechnic University. The lecture was titled "Bio-inspired in sensor visual adaptation for accurate perception". In this lecture, Prof. Chai demonstrated bionic vision sensors based on molybdenum disulfide (MoS_2) phototransistors, which can exhibit time-varying activation and inhibition characteristics and adapt to wide-range scenes as photo-sensory terminals. The light intensity-dependent characteristics of the MoS_2 vision sensor match well with Weber's law, in which the perceived change in stimuli is proportional to the light stimuli. The gate terminal of phototransistors enables the visual adaptation with highly localized and dynamic modulation of photosensitivity under different lighting conditions at a pixel level, exhibiting an effective perception range up to 199 dB. Through this bio-inspired in-sensor adaptation process in the receptive field, the phototransistor array shows image contrast enhancement for both scotopic and photopic adaptation. This lecture attracted many audiences including faculty members and postgraduate students from the School of Electronic and Computer Engineering and the School of Advanced Materials, Peking University. After the lecture, there was a warm discussion on sensors, synaptic devices, and emerging devices. The lecture was invited and hosted by Shengdong Zhang, Professor of School of Electronic and Computer Engineering, Peking University, and the Chair of ED/SSC Shenzhen Chapter.

ED/SSC Hong Kong Chapter 2021 Student Symposium on Electron Devices and Solid-State Circuits

—by Qiming Shao

On 18 December 2021, the IEEE 2021 Student Symposium on Electron Devices and Solid-State Circuits (s-EDSSC) was held online. In 2021, the IEEE Hong Kong Joint Chapter of ED/SSC, the Department of Applied Physics at the Hong Kong Polytechnic University, and the Department of Electrical and Electronic Engineering at the University of Hong Kong jointly organized the 2021 s-EDSSC. The Symposium served as a platform for undergraduate and graduate students in the field of ED/SSC to present their research results. They could also exchange ideas with peers and senior researchers in the community.

The participants were from different universities in Hong Kong and mainland China. Eleven submitted papers were selected for the presentations. The paper topics covered materials, devices, circuits to systems, showing a diversity of research in the ED/SSC community. The materials topic included silicon, compound semiconductors, two-dimensional materials, dielectric, ferroelectric, and magnetic materials. The devices topic covered logic devices, memory devices, and neuromorphic devices. The circuits topic included linear equalizer, neural network accelerator, and brain-inspired circuits. The systems topic covered hardware-software co-designed camera and video sensing systems. Through the Q&A discussions, the committee members and the students understand more about the student research status. Furthermore, the students are encouraged

IEEE EDS Distinguished Lecture on 10 November 2021, by Prof. Yang Chai from the Department of Applied Physics at Hong Kong Polytechnic University

to participate in more IEEE activities. After presentations, the committee selected a few best student paper recipients based on the manuscript and presentation quality. Every student received a certificate and a cash award of HKD 500. Readers can find more information about the 2021 s-EDSSC on the IEEE HK ED/SSC Chapter website: https://r10.ieee.org/hk-edssc/.

EDS Kansai Chapter

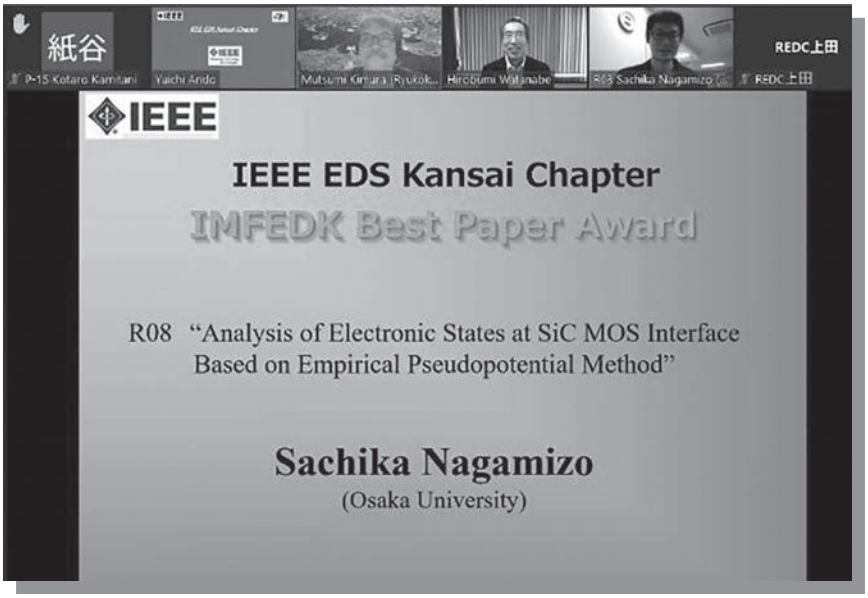
—by Yuichi Ando

Kansai Colloquium Electron Devices Workshop

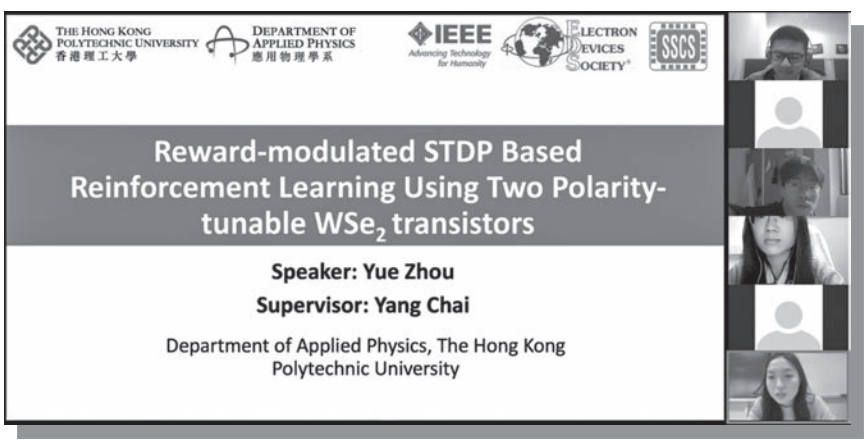
The Colloquium of EDS Kansai Chapter was held online on 28 September 2021. EDS-K Technical Committee members carefully reviewed papers published in the past year from various prestigious conferences and technical journals, such as IEDM, SSDM, and IEEE transactions. Totally 9 papers from authors in the Kansai area were selected to be presented at the Workshop. The award committee also selected one best paper award and one student award. There were totally 51 attendees, including 26 EDS members, who enjoyed the interesting talks.

The International Meeting for Future of Electron Devices, Kansai (IMFEDK2021)

IMFEDK2021 was held online on 18–19 November 2021. The meeting had 10 regular speeches, 2 keynote speeches, 12 invited talks, and 17 poster presentations. Many latest topics of a wide range of fields related to electronic devices (Silicon, Compound, Emerging devices, Circuit, Industrial, etc) were covered. The IMFEDK committee selected the best paper award. The winner's paper was "Analysis of electronic states at SiC MOS interface based on empirical pseudopotential method" by Mr. Sachika Nagamizo of Osaka University. The committee also selected 3 student poster awards. The winners were Miss Aimi Syairah Safaruddin (NAIST), Mr. Kazuki Shimazoe (KIT), and Mr. Kotaro Kamitani (KIT). There was a lively question and answer discussion even though it was an online meeting. The 175 attendees, including 26 EDS members, enjoyed the interesting talk.



IMFEDK2021 Best Paper Award: "Analysis of electronic states at SiC MOS interface based on empirical pseudopotential method" by Mr. Sachika Nagamizo of Osaka University

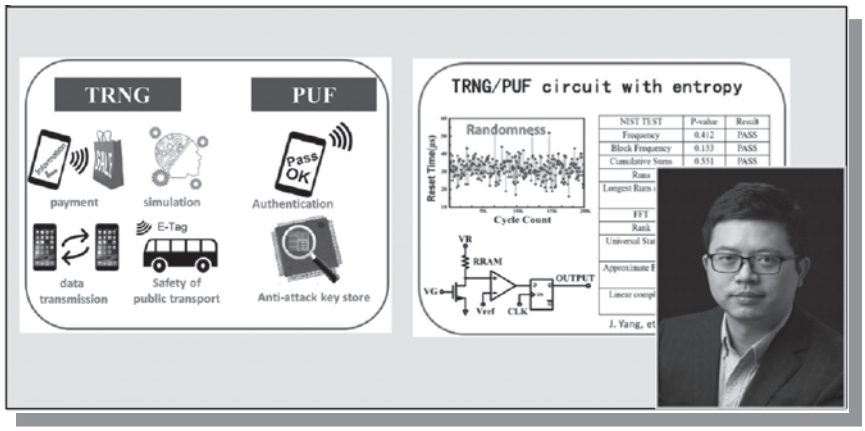


A screenshot from s-EDSSC presentation (via Zoom) titled "Reward-modulated STDP based reinforcement learning using two polarity-tunable WSe2 transistors" (given by Ms. Yue Zhou, one of the best student paper award winners)

IEEE EDS Distinguished Lecture—ED Taipei Chapter

—by Steve Chung

On 24 December 2021, the ED Taipei Chapter held the Invited Talk of Prof. Hangbing Lyu from the Institute of Microelectronics, Chinese Academy of Sciences. The Lecture title was "Integration of resistive switching memory on advanced technology nodes". The lecture was arranged in a virtual format. In this talk, Prof. Lyu first introduced emerging memory types, such as magnetic random access memory (MRAM), resistive switching memory (RRAM), and phase-change memory (PCM), which can bridge the performance gap and trigger the evolution of memory hierarchy. For embedded memory, the challenges of integration into the advanced CMOS platform and periphery circuit design require further



ED Taipei, Invited Talk on "Integration of resistive switching memory on advanced technology nodes", 25 December 2021, via virtual presentation

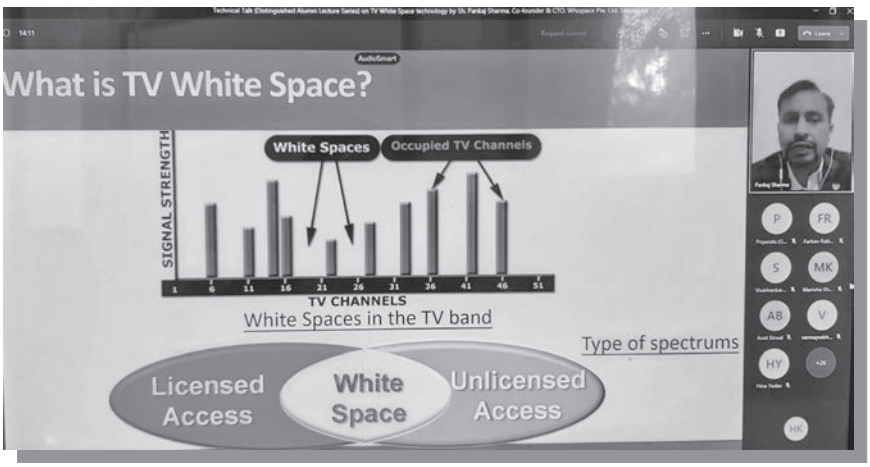
attention. Prof. Lyu then introduced the background and operations of RRAM. He then presented important issues encountered in the development of RRAM for the 28nm node and beyond, such as the high-temperature drift of resistive elements, endurance, retention, and the potential solutions. Several important embedded RRAM products from the industry were reviewed. In the end, he briefly introduced potential applications of RRAM in hardware security, physically unclonable function (PUF)/true random number generator (TRNG), stochastic computing, in-memory computing, etc. This talk was attended by more than 30 graduate students and professors.

~Tuo-Hung (Alex) Hou, Editor

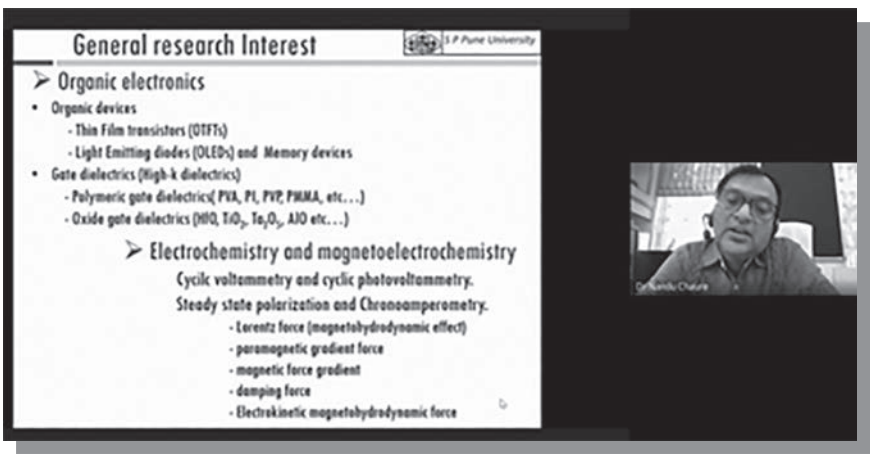
Delhi Section ED Chapter

—by Harsupreet Kaur

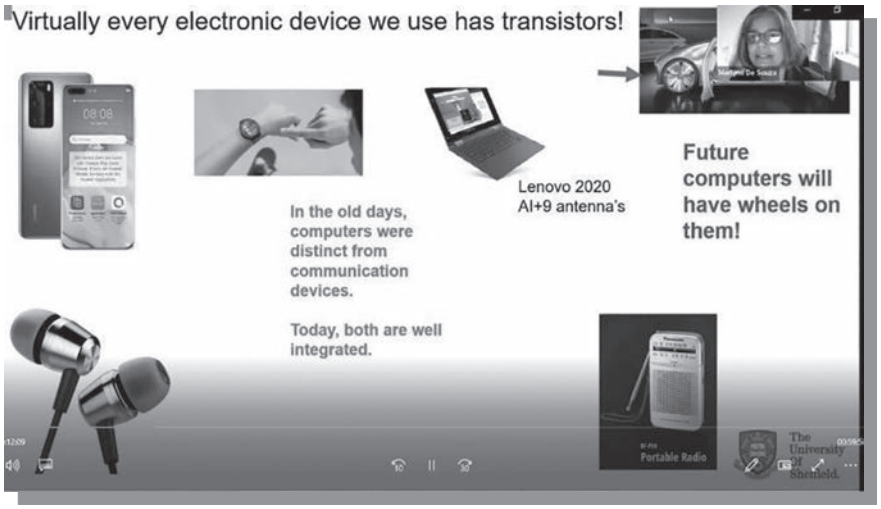
The Chapter in association with the Department of Electronic Science of the University of Delhi, South Campus jointly organized "Distinguished Alumni Lecture Series" during the period September-December 2021. The first talk on "Antennas for RF energy harvesting system design" was delivered by Dr. Nasimuddin, Scientist, SRO, Institute for Infocomm Research, A*STAR, Singapore. It was held on 29 September 2021. On the same day, the second talk was delivered by Dr. Yogesh Verma, Scientist-G, Head, AD Seekers Division, DRDO, Hyderabad on the topic "Phased Array and Gimbel Version Seekers". The lectures aroused great interest among the participants. More than 80 participants attended the talks. The second set of talks in this lecture series was held on 22 October 2021. The first talk of the second set was delivered by Dr. Meena Mishra, Scientist-G, SSPL, DRDO on "Application of GaN based devices in RF Electronics" and the second lecture of this set was delivered by Prof. K. P. Ray, Defence Institute of Advanced Technology (DIAT), Pune on the topic "Microwaves in medical fields including neutralizing COVID-19 virus". The lectures were attended by over 70 participants. The third set of talks in the "Distinguished Alumni Lecture Series" was delivered on November 17, 2021. The first talk was delivered by Sh. Vaibhav Agarwal, General Manager- International Business



Shri Pankaj Sharma delivering his talk



Prof. Nandu Chaure delivering the talk on Solar Photovoltaic Technology



Prof. Merlyne De Souza presenting her talk

Astra Microwave Products Ltd on "Make in India and Opportunities in Defense Sector". The second talk of the third set was delivered by Shri Shiv Dutt, RF Lead Engineer, Sterlite Technology Limited on the topic "Analog RF Front End Architecture". Both talks were very interesting and were attended by over 80 participants. The final talk of this lecture series was presented on 9 December 2021 by Sh. Pankaj Sharma, Senior Manager, Institute of Microelectronics (Agency for Science, Technology & Research) & Co-Founder, Whizpace, Singapore. The topic was "TV White Space technology: Opportunities and Challenges". The seminar was attended by over 70 participants.

The Chapter in association with the Department of Electronics, University of Jammu organized on 6 October 2021 a one day online webinar on "Electronic Devices and their Applications". Two lectures were delivered by Prof. Nandu B. Chaure from the Department of Physics, Savitribai Phule, Pune University and by Prof. Satinder Kumar Sharma of the School of Computing and Electrical Engineering & Center for Design & Fabrication of Electronic Devices, IIT Mandi. The programme was attended by more than 60 participants including faculty members, research scholars and post graduate students from various institutions.

The Chapter organized on 20 October 2021 a Distinguished Lecture on the topic, "Nanoelectronics to Nanotechnology: More Moore and More than Moore" by Professor Durga Misra, Department of Electrical and Computer Engineering, New Jersey Institute of Technology (NJIT), Newark, USA. Prof. Misra discussed the next generation nanoelectronics devices, scaling for sub-14 nm CMOS technology (More Moore), genesis of the bulk/SOI FinFET devices which require effective oxide thickness scaling of gate dielectric beyond 0.7 nm. Prof. Misra highlighted some recent developments and trends in device design and fabrication of electronics devices for IoT technology. The talk was very insightful and was attended by over 45 participants.

The Chapter in association with the Training and Placement Cell, and Internal Quality Assessment Cell of Maharaja Agrasen College, University of Delhi conducted on 21 October 2021 a technical talk titled "Design of Superconducting Synchronous Machines for Low Speed Applications". The talk was given by Dr. David Torrey, Senior Principal Engineer in the department of Electric Power at GE Global Research. The talk focused on the design of superconducting synchronous machines including various aspects of their design and applications. The talk was attended by over 70 participants including 15 IEEE members.

The Chapter organized on 29 October 2021 a Distinguished Lecture on "3D Integration: Above and Beyond Moore's law" by Professor Jesús A. del Alamo, Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, USA. Prof. Alamo discussed the new possibilities to bring together logic circuits and memory and break the "memory wall", the current bottleneck for system performance. The speaker described also the intimate memory and logic integration that will enable artificial intelligence chips capable of efficiently processing very large data sets. The talk was very informative.

On 12 November 2021, the Chapter organized a Distinguished Lecture on the topic "Differentiated Silicon for Non-terrestrial Broadband Internet addressing the digital divide" by Dr. Anirban Bandyopadhyay, Senior Director, Strategic Applications, GLOBALFOUNDRIES, Inc., Santa Clara, California, US. Dr. Bandopadhyay discussed the use of differentiated silicon technologies like partially and fully depleted SOI and Silicon-Germanium to address stringent requirements of large element phased array systems for both satellite and ground station millimeter wave radio. The speaker highlighted the need for foundries to make high volume mm-wave testing of radio hardware both for ground terminals and satellite payloads. Over 60 participants including research scholars, post graduate students and faculty members attended the talk.

On 3 December 2021, the Chapter in association with the Department of Electronics, Maharaja Agrasen College, University of Delhi organized another Distinguished Lecture. The talk was given by Prof. Merlyne De Souza on the topic, "CMOS Scaling: Negative Capacitance and Challenges Ahead". The lecture was attended by around 95 participants. A technical talk by

Ms. Rekha Jain was organized on 4 December 2021. The topic was "5G-ready for the future". The lecture was attended by around 90 participants and the talk focused on various aspects of 5G technology.

ED NIT Silchar Student Branch Chapter

—by T.R.Lenka

The Chapter in association with IEEE Nanotechnology Council Chapter and Department of Electronics and Communication Engineering, National Institute of Technology Silchar organised during 23–24 November 2021 a students seminar program on "Emerging Topics of Micro/Nanoelectronics and VLSI Design". The program was organized in a hybrid mode and was attended by around 30 EDS members and student members. A Thanksgiving Ceremony was organized on 26 November 2021 to celebrate the 2021 EDS Student Branch Chapter of the Year Award of the NIT Silchar, ED15 Student Branch Chapter. The 1st Annual Social Meet 2021 was organized on 25 December 2021 to witness the celebration of Merry Christmas at Borakhai Tea Garden, Silchar, Assam. The Social Meet was followed by an Ex-Com meeting. The program was attended by 16 EDS (faculty) members with their families and 20 EDS student members of M.Tech (Microelectronics and VLSI Design) and PhD program. The program was very successful and was highly appraised by each and every member.

ED Netaji Subhash Engineering College Student Branch Chapter

—by Saheli Sarkhel

The Chapter organized on 18 December 2021 a Distinguished Lecture on "Redesigning Physical Electronics", delivered by Dr. Muhammad Mustafa Hussain of the University of California Berkeley and Dept. of Electrical Engineering, KAUST, Saudi Arabia. Dr. Hussain gave a very informative presentation on the flexible physical System-on-package and explained its implementation in extreme conditions. The presentation was followed by an interactive question and answer session, where the students, as well as faculty members participated. Dr. Hussain cleared all the doubts of the attendees and enlightened them in a path to pursue further studies.

The Chapter organized on 29–30 October 2021 a two – day webinar conducted by the current and erstwhile students of Electronics and Communication Engineering Department on "Introduction to Electronics and VLSI (with Introduction to HDL)" to familiarize students with the ongoing research trends in the world of electronic devices, emerging non-conventional device structures and VLSI design flow. The lectures were followed by a session for hands–on training in HDL (using Verilog). The event had about 24 participants. Both sessions were very interactive where students got the opportunity to learn and expressed interest in this research domain.

Celebration of the 2021 EDS Student Branch Chapter of the Year Award of the NIT Silchar, ED15 Student Branch Chapter: Prof. K. L. Baishnab, Head of Department-ECE (from left); Samadrita Das, Student Branch Chapter Vice-Chair; Prof. F. A. Talukdar, Branch Counsellor; Dr. T. R. Lenka, Chapter Advisor, Dr. Koushik Guha (Treasurer) (rightmost), and EDS Student Members

Bangladesh Section Jt. Chapter

—by S. M. Raiyan Chowdhury

The Chapter organized a Distinguished Lecture on 23 October, entitled "Energy Yield Losses in PV Installations due to Soiling and Mitigation Strategies against the Same". The speaker was Dr. Anil Kottantharayil, SM IEEE, HAL R&D Chair Professor, and FNAE, Electrical Engineering, Indian National Academy of Engineering.

The DL program was preceded by an overview presentation of EDS and SSCS along with its membership benefits. Next, Dr. Kottantharayil provided a comprehensive lecture on malignant effects of soiling in PV systems specially in the Sun belt countries. He also showed the methods for illustrating the impact of soiling based on experiments and simulation modeling. The Lecturer discussed elaborately about the anti-soiling coatings on solar glass, the degradation of these coatings, and the test procedures to examine the durability of the coatings. Afterwards, there was an interactive question-answer and feedback session for the participants. Finally, the program concluded with a note of thanks from Dr. Samia Subrina and a virtual group photo session of the honorable speaker, the hosts, and the attendees of the event. The Chapter hosted another lecture program on December 04, 2021. The topic was "Design and Analysis Consideration in Hybrid

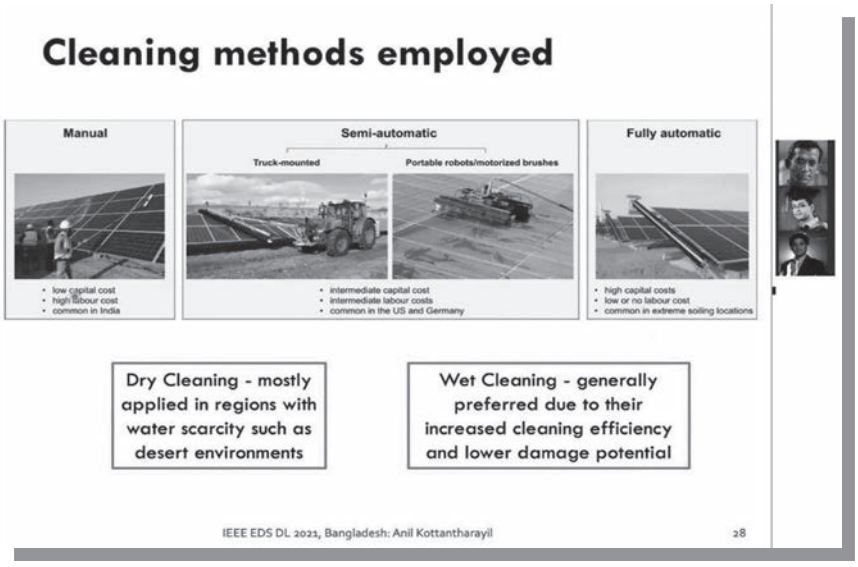


Figure 1: A snapshot from Dr. Kottantharayil Distinguished Lecture, 23 October 2021

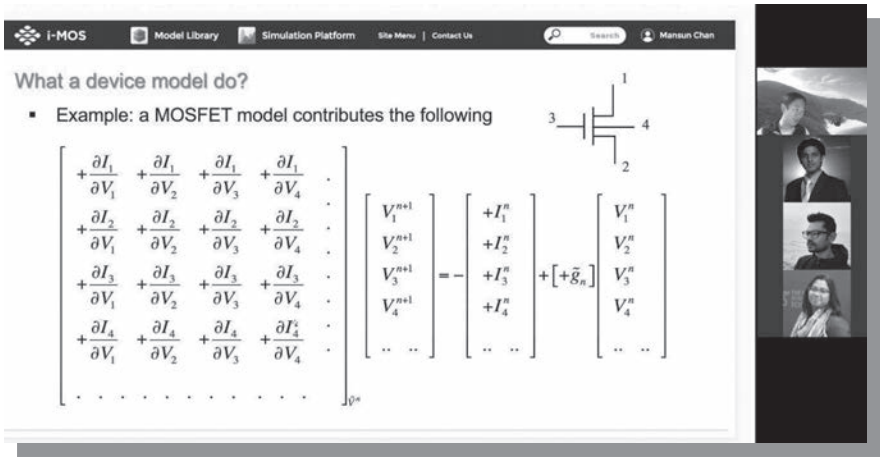


Figure 2. A snapshot from Dr. Mansun Chan Distinguished Lecture, 15 December 2021

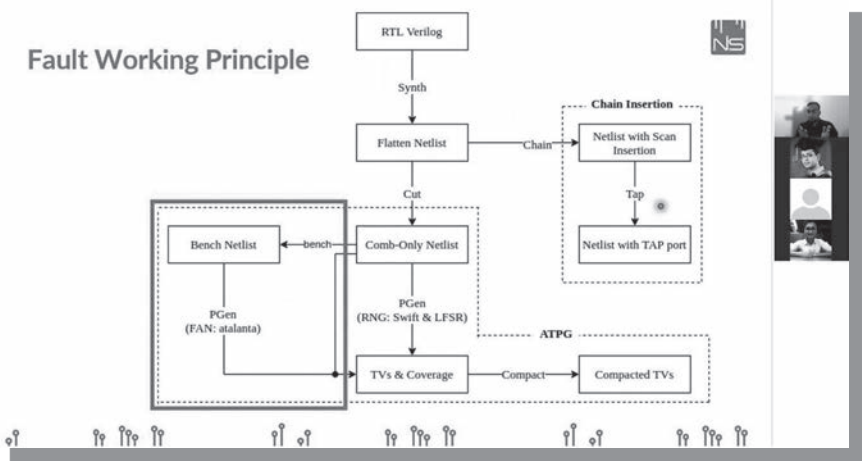


Figure 3. A snapshot from the presentation by Dr. Uday Hasan at the workshop held on 18 December 2021

and Electric Propulsion System". The speaker was Dr. Syed Jaffrey Al Kadry, SM IEEE. Dr. Kadry conducted an interactive lecture using modern tools and techniques to model, design and simulate advanced hybrid propulsion systems from the power electronics point of view. He showed the participants the recent research trends of hybrid propulsion systems and scope for future development. The lecture program came to end with a note of thanks from the chairperson, Dr. Samia Subrina.

The chapter organized another Distinguished Lecture on December 15, 2021. The topic was "Circuit Simulation and Compact Modeling Beyond Device Physics". The speaker was Dr. Mansun Chan, Professor and Chair, Department of Electronic and Computer Engineering (ECE), Hong Kong Institute of Science and Technology, Clear Water Bay, Kowloon, Hong Kong.

Dr. Chan provided a comprehensive lecture on circuit applications, CAD tools, and circuit simulation methodologies, including transfer function simulation, transient simulation, frequency-domain simulation, and reliability simulation. He showed also that along with a development of the "more-than-Moore" focus, an effective circuit simulator needs to be capable of handling the accelerated development of new types of devices and to allow designers to perform simulation for circuit evaluation before these technologies eventually mature. Methodologies to speed up the process to bring the emerging device data to circuit simulation platforms for early circuit evaluation were also discussed in detail. The program was drawn to a close with the note of thanks from Dr. Samia Subrina.

The Chapter organized on December 18, 2021 a workshop "How to Test a Complex Chip using Open Source Tools". The instructor of the workshop was A.K.M. Uday Hasan Bhuiyan, Senior Design Engineer, Team Lead, DFT Team, Neural Semiconductor Limited.

Figure 4. Attendes of the workshop led by Dr. Ahsan at BUET Campus on 20 December 2021

Dr. Uday Hasan showed the overview and basics of the Density Functional Theory (DFT) tool and trained the participants in its practical implementation and performance analysis. The talk was followed by an interactive question-answer and a feedback session. Finally, the workshop concluded with a note of thanks from the chairperson, Dr. Samia Subrina and a virtual group photo session.

The Chapter in association with the Department of Electrical and Electronics Engineering (EEE), Bangladesh University of Engineering and Technology (BUET) organized on 20 December 2021 a lecture "How an IC (Integrated Circuit) is born in Semiconductor Industry". It was conducted at West Palashi Campus, Department of EEE, BUET. The honorable lecturer of the program was Dr. A.K.M. Ariful Ahsan, Technical Leader, Product Reliability Area, Inter Corporation, Oregon, USA, and Adjunct Faculty of Oregon Institute of Technology (OIT) and Portland State University (PSU), USA.

Dr. Ahsan's lecture comprised a big picture of the Integrated Circuit (IC) research & development and design & manufacturing in semiconductor industries. The lecturer talked about some fascinating stories of transistor development, scaling, design and process challenges, inventions, and business/cultural highlights. The talk was followed by an interactive question-answer and a feedback session. Finally, the workshop concluded with a note of thanks from the chairperson, Dr. Samia Subrina and a virtual group photo session.

Additionally, the Chapter arranged several executive committee meetings and membership drive programs for spiriting up the chapter activities.

ED Muffakhamjah College of Engineering and Technology Student Branch Chapter

—by Maliha Naaz

The Chapter organized a workshop on "Hands-on Electronics" for 2nd year students of various disciplines. The workshop was attended by 46 participants including 23 IEEE Student members. The sessions were conducted in two batches and the participants were trained on various basic electronic components and devices like resistor, transistor, diode, capacitor and on how to use them to make circuits for practical applications. The participants got the live demonstration of three different projects namely Fire Alarm, Mobile Phone Charger And Water Level Indicator. The participants were provided with necessary components to make the projects on their own. The workshop was concluded by the demonstration of soldering of electronic components on a veroboard.

The Chapter also organized on the 3rd of December a webinar on the topic "Wearable Electronics" for the 2nd year Students of all the branches. The virtual talk was delivered by Ms. Maliha Naaz, one of the faculty members of the College. The webinar was attended by around 45 students including 15 IEEE Student Members of various disciplines.

Mr. Anutham explaining concepts during the "Hands-on Electronics" workshop

EDS MEETINGS CALENDAR

THE COMPLETE EDS CALENDAR CAN BE FOUND AT OUR WEB SITE: HTTP://EDS.IEEE.ORG. PLEASE VISIT.

2022 International Symposium on VLSI Design, Automation and Test (VLSI-DAT)	18 April – 21 April 2022	Hsinchu, Taiwan Hybrid Event
2022 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA)	18 April – 21 April 2022	Hsinchu, Taiwan Hybrid Event
2022 23rd International Vacuum Electronics Conference (IVEC)	25 April – 29 April 2022	Monterey, CA USA
2022 33rd Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC)	02 May – 05 May 2022	Saratoga Springs, NY USA
2022 IEEE International Memory Workshop (IMW)	15 May – 18 May 2022	Dresden, Germany Hybrid Event
2022 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EuroSOI-ULIS)	18 May – 20 May 2022	Udine, Italy
2022 34th IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD)	22 May – 26 May 2022	Vancouver, BC Canada
2022 IEEE Symposium on VLSI Technology & Circuits	12 June – 17 June 2022	Honolulu, HI USA
2022 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)	20 June – 22 June 2022	Denver, CO USA
2022 China Semiconductor Technology International Conference (CSTIC)	21 June – 22 June 2022	Shanghai, China

Device Research Conference (DRC)	26 June – 29 June 2022	Columbus, Ohio, USA
2022 IEEE International Interconnect Technology Conference (IITC)	27 June – 30 June 2022	San Jose, CA USA
2022 IEEE Latin American Electron Devices Conference (LAEDC)	04 July – 06 July 2022	Cancun, Mexico
2022 29th International Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD)	06 July – 09 July 2022	Kyoto, Japan
The 29th edition of the IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)	18 July – 20 July 2022	Singapore
2022 IEEE International Flexible Electronics Technology Conference (IFETC)	21 Aug – 25 Aug 2022	Qingdao, China
2022 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)	07 Sept – 09 Sept 2022	Granada, Spain
2022 44th Annual EOS/ESD Symposium (EOS/ESD)	19 Sept – 24 Sept 2022	Reno, NV USA
2022 IEEE 48th European Solid State Circuits Conference (ESSCIRC) and IEEE 52nd European Solid-State Device Research Conference (ESSDERC)	20 Sept – 23 Sept 2022	Milan, Italy
2022 17th European Microwave Integrated Circuits Conference (EuMIC)	26 Sept – 28 Sept 2022	Milan, Italy
2022 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)	16 Oct – 19 Oct 2022	Phoenix, AZ USA
2022 14th International Conference on Advanced Semiconductor Devices and Microsystems (ASDAM)	24 Oct – 27 Oct 2022	Smolenice, Slovakia

2022 International EOS/ESD Symposium on Design and System (IEDS)	09 Nov – 11 Nov 2022	Chengdu, China
2022 International Electron Devices Meeting (IEDM)	03 Dec – 08 Dec 2022	San Francisco, CA USA
2022 IEEE 50th Semiconductor Interface Specialists Conference (SISC)	08 Dec – 11 Dec 2022	San Diego, CA USA

Inaugural issue of *IEEE Journal on Flexible Electronics* (J-FLEX)

IEEE is pleased to announce the publication of the inaugural issue of *IEEE Journal on Flexible Electronics* (J-FLEX). IEEE J-FLEX is an exciting journal covering research in the broad area of flexible and printed electronics and sensors and systems on flexible, disposable, stretchable and degradable substrates. A joint publication of IEEE Sensors Council, IEEE Electron Device Society and IEEE Circuits and Systems Society, the journal provides authors a convenient and efficient process to communicate their multidisciplinary research results to the vibrant global flexible electronics community. The interdisciplinary and multinational Editorial Board of IEEE J-FLEX, reflects the composition of the research community the journal is serving. Following a streamlined peer-review process, overseen by a leading editorial board, the inaugural issue comes with the introductory editorial piece by Prof. Ravinder Dahiya, the first Editor-in-Chief of IEEE J-FLEX, and seven scientific papers which include one review article and six research articles coving different areas such as electronic waste, sustainable electronics, flexible antenna for sensing and wireless area/body networks, biofuel cells, energy harvesters, thin film transistors, organic transistors and flexible microfluidic devices.

The review article focusses on the growing issue of electronic waste and lays an emphasis on the need for electronics industry to transition to more sustainable practices. The article presents a brief contextual summary about how the international management of Waste Printed Circuit Boards and legalization have evolved over the past 20 years, and reviews existing materials used in PCBs, their evolution towards flexible PCBs and eventually the additively manufactured PCBs and resource efficient printed electronics. An overview of the potential solutions and new opportunities arising from the greater use of sustainable materials and resource-efficient manufacturing is also presented in this article.

The inaugural issue presents a membrane less enzymatic biofuel cell utilizing carbon nanotubes coated carbon cloth as bioelectrodes. The bioelectrodes are integrated on a paper substrate to develop an economical and disposable patch-type wearable biofuel cell.

Another paper included in the inaugural issues presents amorphous indium-gallium-zinc oxide thin-film transistors and circuits on flexible polyimide substrate. The paper shows the advantages of incorporating fluorination in the construction of circuit building blocks, leading to higher gain, wider noise margins, more tightly distributed transition voltage and larger output swing.

We hope that you will find these articles useful to stimulate your research into the fast-growing area of Flexible Electronics. We welcome submissions via the journal's submission and peer review website at https://mc.manuscriptcentral.com/jflex. Please visit the homepage at https://ieee-jflex.org to learn more.

Call for Papers for a Special Issue of

IEEE Transactions on Electron Devices

on

"From Mega to nano: Beyond one Century of Vacuum Electronics"

Vacuum electron devices were born more than one century ago and were, until the discovery of the transistor, the only existing electronic devices. From the first valve, "tubes" evolved over years and years of development into a variety of devices with specific purposes (magnetron, klystron, TWT, gyrotron) but a common unique feature, high output power to enable a wide range of fundamental applications, from space to healthcare, nuclear fusion, and many others.

After one century, vacuum electronic devices have evolved with the use of new materials, microfabrication processes, simulation tools. New frontiers are explored in the millimeter wave and sub THz range and in the nanometric domain. Vacuum electron devices are the only family of devices with size ranging from a few meters, Megawatt klystrons for particle accelerators, to nanometers, new nano vacuum transistors, spanning eight orders of magnitude in size.

This Special Issue of the IEEE Transactions on Electron Devices aims to value the great diversity in this family of devices by reporting the latest research results and the state of the art in the field of Vacuum Electronic Devices.

The Special Issue will include invited and open call papers from the Vacuum Electronics community and any other related disciplines or area of applications. Papers must be new and original material that has not been copyrighted, published or accepted for publication in any other archival publication, that is not currently being considered for publication elsewhere, and that will not be submitted elsewhere while under consideration by the Transactions on Electron Devices.

This Special Issue will be published in June 2023.

The topics of interest include, but are not limited to:

Vacuum Electronics Devices (VEDs)

- Slow-wave devices
- Klystrons and IoT's
- Fast-wave devices
- CW and pulsed-power devices
- Magnetrons and other cross-field devices
- Plasma-filled devices
- Field-emission devices

Technologies and phenomena

- Fabrication techniques
- Novel materials (dielectrics, etc.)
- Components (guns, collectors, windows)
- Electronic power conditioners and supplies
- Linearizers and system integration
- High Power Microwave
- Multipactor
- Reliability
- RF breakdown

Vacuum Electron Sources

- Thermionic cathodes
- Field emission cathodes
- Photo cathodes
- Emission physics

Emerging technologies in vacuum electronics

- Simulation based design
- Advanced manufacturing
- Metamaterials
- Vacuum transistors
- RF-materials Interaction

System and Applications

- Space
- Nuclear fusion
- Healthcare
- Defense
- Radar
- Accelerators
- High data rate communication

Submission instructions

Manuscripts should be submitted in a double column format using an IEEE style file. Please visit http://www.ieee.org/publications standards/publications/authors/author templates.html to download the templates.

When submitting your manuscript through the IEEE's webbased ScholarOne Author Submission and Peer Review System (https://mc.manuscriptcentral.com/ted), please indicate that your submission is for this special issue.

Submission deadline: 31 October 2022 **Publication Date: June 2023**

Call for Papers for a Special Issue of *IEEE Transactions on Electron Devices* on "Dielectrics for 2D electronics"

Since their first fabrication in 2004, two-dimensional (2D) materials have shown outstanding physical, chemical, mechanical, electronic, thermal, optical and magnetic properties in multiple proof-of-concept laboratory experiments. However, exploiting such properties to fabricate advanced solid-state electronic devices and circuits requires overcoming multiple industry-relevant challenges. In 2017, 2D materials were mentioned for the first time in the international roadmap of devices and systems (IRDS) as a potential solution for "channel material technology inflection", and since 2020 IRDS reports also consider 2D materials as a potential solution for "beyond-CMOS as complementary to mainstream CMOS". Some products including 2D materials are already being commercialized, although the 2D materials are mainly used for low-integration-density sensors.

The introduction of 2D materials in high-integration-density circuits, such as transistor-based memories and microprocessors, still requires considerable research efforts. In 2019, TSMC and IMEC reported breaking advances in the integration of 2D materials in ultra-scaled solid-state microelectronic devices and presented the first mass-production-compatible 2D materials-based field-effect transistors (FET) with channel lengths below 100 nm. However, the interaction of 2D materials with adjacent traditional dielectrics (i.e., Si0 2, Hf0 2, Aii0 3, Ti0 2) is highly problematic; while the (theoretical) absence of dangling bonds in the 2D materials provides enormous opportunities, the large amount of defects at the interface to the insulators has a dramatic impact on the performance and reliability of the FETs. The presence of native defects in 2D materials synthesized with industry-compatible techniques (such as chemical vapor deposition) can also be a problem.

In this special issue, we will delve deep into the problem of dielectrics for 2D electronics and present a state-of-the-art compilation of the most sophisticated solutions developed so far to minimize this issue. These will include the development of seed interfacial layers, the use of materials that can form a van der Waals interface with 2D materials, and the use of 2D layered dielectrics, among many others. This special issue will also study the performance of electronic devices using 2D materials, with special emphasis to the dielectric that has been employed and how the interaction between the 2D material and the dielectric can be enhanced. All articles will present original material that has not been copyrighted, published or accepted for publications in any other archival publications, that is not currently being considered for publications elsewhere, and that will not be submitted elsewhere while under considerations by IEEE Transactions on Electron Devices. Review papers on relevant aspects within the field of "Dielectrics for 2D electronics" are also welcome.

Topics of interest include, but are not limited to:

Design of novel dielectrics for 2D electronics

Study of the morphological and electrical properties of alternative dielectrics, such as hexagonal boron nitride (h-BN), native layered oxides like BhSe0 5, mica, and calcium fluoride (CaF2) . Treatment of 2D materials to increase their band gap and use them as dielectric, such as oxidized MoS2• Design of special interface seed layers and films to reduce defective bonding at the interface between 2D conducting and semiconducting materials and the dielectric. Characterization and modeling of the properties of these dielectrics. Novel device architectures like 2D materials for ferroelectric FETs and ferroelectric tunnel junctions are also within the scope of this special issue.

Reliability of dielectrics for 2D materials based FETs

Reliability of 2D materials-based FETs using traditional dielectrics (i.e. Si0 2, Hf0 2, Ah0 3, Ti0 2) as well as their alternatives, including tunneling current, charge trapping and de-trapping, stress induced leakage current, soft breakdown, hard breakdown, progressive breakdown, channel hot carriers degradation and bias temperature instability, among others. The effect of the anisotropic thermal conductivity and permittivity of 2D materials on the performance and reliability of the devices is also of considerable interest.

Dielectric issues that affect the figures-of-merit of 2D materials based electronic devices

Development of 2D materials-based devices (like conventional FETs, memristors, photodetectors) and circuits (like operational amplifiers and logic gates) made of 2D materials, with special emphasis on dielectric issues, including impact of dielectrics as capping layer on 2D electronics, such as remote phonon scattering effects and electrostatic doping effects. Special attention should be put on the main figures-of-merit and how they compare with their counterparts made of traditional materials.

Submission Deadline: 30 September 2022 **Publication Date: April 2023**

EDS Vision, Mission and Field of Interest Statements

Vision Statement
Promoting excellence in the field of electron devices for the benefit of humanity.

Mission Statement
To foster professional growth of its members by satisfying their needs for easy access to and exchange of technical information, publishing, education, and technical recognition and enhancing public visibility in the field of Electron Devices.

EDS Field of Interest
The EDS field-of-interest includes all electron and ion based devices, in their classical or quantum states, using environments and materials in their lowest to highest conducting phase, in simple or engineered assembly, interacting with and delivering photo-electronic, electro-magnetic, electromechanical, electro-thermal, and bio-electronic signals. The Society sponsors and reports on education, research, development and manufacturing aspects and is involved in science, theory, engineering, experimentation, simulation, modeling, design, fabrication, interconnection, reliability of such devices and their applications.