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75TH ANNIVERSARY OF THE TRANSISTOR

PERSPECTIVES ON LOW-VOLTAGE TUNNEL TRANSISTORS FOR BEYOND CMOS LOGIC

ALAN SEABAUGH
DEPARTMENT OF ELECTRICAL ENGINEERING, UNIVERSITY OF NOTRE DAME, NOTRE DAME, IN 46556

In this, the 75th year anniversary of the transistor, complementary metal oxide semiconductor field-effect (CMOS) transistors continue to advance, from fin structures to nanosheets and to angstrom technology nodes. In the wake of this development, discussions continue on steep-subthreshold-swing transistors which still hold promise to outperform CMOS at low voltage, but have so far fallen short of the performance needed for applications. It is worth reviewing the development of the tunnel field-effect transistor (TFET) with the aim to stimulate new ideas and fresh consideration of the paths taken and the technical challenges. For a deeper dive, there is a chapter in the just published Springer Handbook of Semiconductor Devices [1] on tunnel field-effect transistors, and there are many recent reviews, search e.g. "TFET review."

The TFET is an MOS technology and shares many of the structural attributes needed for a transition into a foundry process. A complementary TFET with comparable current drive at lower supply voltage than Si CMOS would enable lower power dissipation without sacrificing speed. The TFET could readily move into the design ecosystem with the primary new device attribute being the steep subthreshold

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Issue	Due Date
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January	October 1st
April	January 1st
July	April 1st

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Perspectives on Low-voltage Tunnel Transistors for Beyond CMOS Logic

(continued from page 1)

swing. In the MOSFET, the current control mechanism is thermionic emission over an energy barrier, and this sets a fundamental limit on the minimum subthreshold swing at 60 mV/decade change in current at room temperature. The TFET relies on electric field control of tunneling and with this current control, the subthreshold swing can be lower (steeper) than 60 mV/decade.

The n-channel TFET, in planar form, differs from the MOSFET in the polarity of the source-channel junction. In the off state, shown in figure 1 (a), electrons in the valence band of the source are energetically blocked from tunneling into the channel. With a positive gate bias these electrons in the source tunnel into the channel, with current injection set by the overlap of the filled valence band and empty conduction band states in the channel; this is labeled the tunneling window, qV_{TW}, in figure 1 (b). The gate voltage simultaneously modulates both the tunneling probability for injection of electrons into the channel and the availability of empty channel states.

There is a long history of experimental and theoretical development of tunneling diodes and transistors leading to the TFET [2], [3]. The realization that low subthreshold swing could be achieved by gating of interband tunneling began to appear in publications in 2003 and 2004 [4]–[6]. In 2004, Joerg Appenzeller reported 40 mV/dec subthreshold swing in a carbon nanotube FET explained by interband tunneling [4]. The promise of a transistor that could outperform Si CMOS at low voltages attracted international attention and substantial research investments over almost a dozen years. The list of semiconductor materials and structural embodiments explored experimentally is extensive: Si, Ge, SiGe, III-Vs, III-Ns, 2D materials, mixed heterojunctions, n-TFET, p-TFETs, pillars, nanowires, ribbons, tubes, vertical tunneling, lateral tunneling, and more. A similar breadth of exploration has taken place in theory and design to seed these device developments and interpret the measured device characteristics.

Selected best reported transfer characteristic of the n-TFETs across materials systems are shown in the accompanying figure 2 [1]. These TFETs were selected to show performance at drain voltages less than or equal to 0.5 V (where they would be expected to operate). To be included here the transistors also needed to exhibit subthreshold swing less than 60 mV/dec over at least one order of magnitude in drain current. Across materials systems, it can be seen that the direct-bandgap III-V materials have demonstrated the highest current drives. In comparison with CMOS, the currents are about an order of magnitude lower than desired to outperform Si at similar voltages. Indirect-bandgap materials such as Si and Si/Ge exhibit still smaller currents since phonons are required to enable the tunneling transitions, lowering the tunneling rates. Steep swings in 3D Ge/2D MoS_2 and carbon nanotubes are also a part of this comparison.

The corresponding subthreshold swings as a function of drain current/width is shown in the companion figure 3. One would like the voltage (V_{60}) at which the subthreshold swing becomes less than 60 mV/dec to occur at a drain current of about 1 μA/μm and then to stay below 60 mV/dec for about 4 decades. The current at V_{60} is denoted I_{60}.

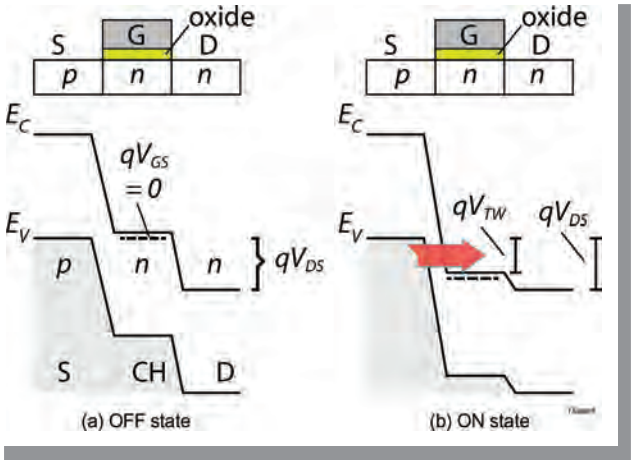

Figure 1. Schematic energy band diagram and cross sections of the tunnel FET.

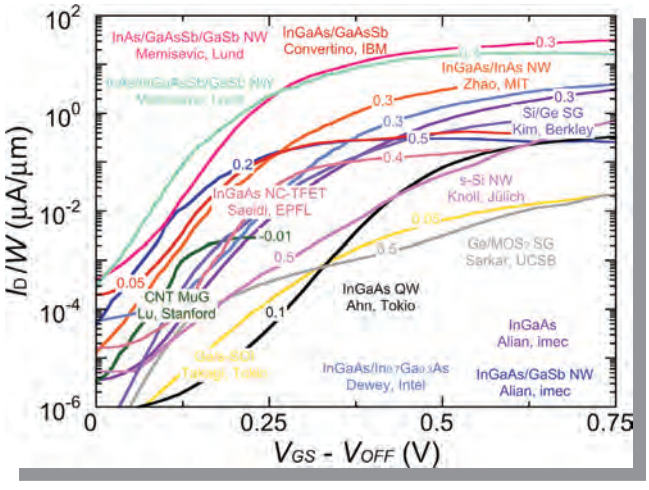

Figure 2. Comparison of selected published n-TFET transfer characteristics. The numbers on the plots are the drain/source voltages. The curves have been shifted to put the current minimum at 0 V. References are given in [1].

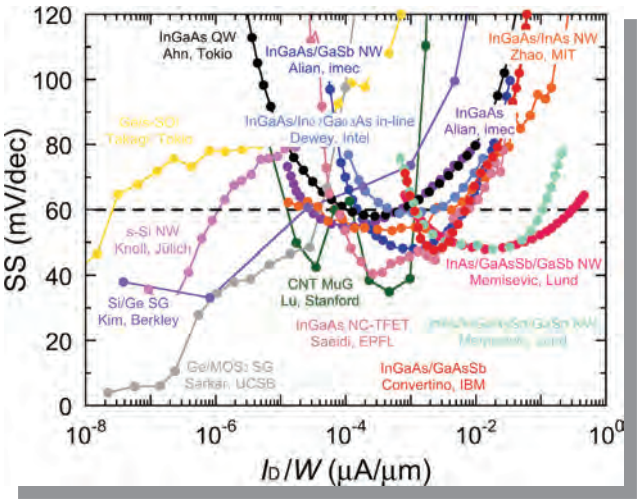

Figure 3. TFET subthreshold swing versus drain current for the n-TFETs shown in figure 2 [1].

The III-V channel materials show an I_{60} approaching the desired 1 μA/μm, and show steep swing for more than 2 decades. The lower limit on this behavior is attributed to trap-assist tunneling, a leakage mechanism whereby electrons from the source valence-band tunnel into traps in the channel traps (surface or bulk) and then are thermally-emitted to the conduction band. Group-IV-containing materials have generally shown lower leakages and this has led to more extended ranges over which the subthreshold swing stays below 60 mV/decade.

While new applications can drive technology development, benchmarks are useful to focus development. For the n-TFET the performance targets which would constitute clear measures of progress relative to the Si n-MOSFET are: drain current exceeding 200 μA/μm at voltages less than or equal to $V_{DS} = V_{GS} = 0.4$ V, with $I_{60} = 1$ μA/μm and maintaining steep subthreshold swing over more than 4 decades. Other measures of progress are the development of a path to a complementary technology and to entry into manufacturing at the leading technology nodes.

To reach these ends will require fundamental studies in materials and devices. Much progress has been made on TFETs, but it is spread widely across semiconductor materials and heterojunctions. Community focus still awaits motivating experimental and theoretical direction. In any particular materials system, how is the abrupt tunnel junction doped, what limits the doping density and abruptness, what is the origin of the band tails, what is the preferred MOS stack and what are the interfacial defects, bulk traps, and border traps? Perhaps there are composite transistor structures that enable TFET operation when the device is operated at low voltages, but enable MOSFET action at high voltages. Perhaps there will be discoveries at the angstrom technology nodes that provide new approaches. Perhaps there are collective mechanisms in complex dielectrics that can be utilized to lower swing without introducing hysteresis. There are many avenues for breakthroughs.

In 1976, approaching the 30-year anniversary of the transistor, William Shockley was asked to write a paper about how the first transistors were conceived and brought to demonstration [2]. A key finding for him in writing this paper was surprisingly "how slow he was and how he missed the junction transistor's key concepts so many times." His message to readers facing conceptual and technical challenges was to "stick with it and not give up." This is clearly a message relevant to TFETs. Experiments show the technical gaps. New solutions are needed to enable manufacturing and commercialization. There are reasons to keep thinking about TFETs.

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75 Years of Compact Models: From Shockley to Sticker Shock

Colin C. McAndrew, Life Fellow, IEEE and Laurence W. Nagel, Life Fellow, IEEE
C. C. McAndrew is with NXP Semiconductors, Chandler AZ 85224 USA
L. W. Nagel is with Omega Enterprises Consulting, Kensington CA 94708 USA

I. Introduction

Today, everyone knows what a "compact" model (a.k.a. a SPICE model [1]) is: an analytical model, hopefully both accurate and computationally efficient, of a (semiconductor) device that is implemented in a circuit simulator and is used for the design of circuits, especially of integrated circuits (ICs).

The archetypical compact model is the Shockley equation for current in a *pn*-junction diode [2]

$$I = I_s\left(exp\left(\frac{V}{\phi_t}\right) - 1\right) \tag{1}$$

where V is the voltage across the diode, ϕ_t is the thermal voltage, and I_S is the "saturation current," which can be calculated from physical and structural parameters.

Simplified compact models are also used by professors to teach the basics of how devices work, and by designers to form mental images of how devices work, to help them innovate new circuits.

The size, complexity, and expectations (yield, reliability, performance, power consumption) of ICs have increased exponentially for many years—Moore's Law—which has led to a concomitant increase in expectations of the capabilities of computer-aided design (CAD) tools, like SPICE, and the compact models in those tools [3], [4].

Here, we give a brief overview of the trajectory of compact models since the invention of the transistor.

Nomenclature: q is the elementary charge, k the Boltzmann constant, T is temperature in Kelvin, $\phi_t = kT/q$, μ is mobility, V_{AB} is the voltage between terminals A and B.

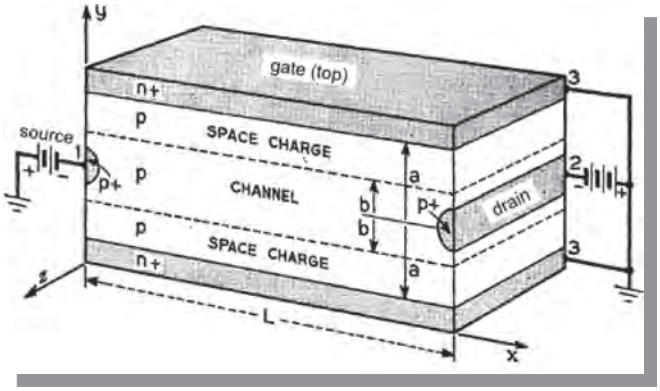

Figure 1. Fig 1 of [5], from 1952, which shows the device abstraction used for Shockley's analysis (terminal labels added).

II. The JFET: A Compact Model Leads the Revolution!

Perhaps the most amazing feat ever in compact modeling was from the master himself: In 1952, Shockley [5] proposed what today we call a JFET, based on what today we call a compact model. The formulation, analysis, and simplifications adopted by Shockley are eerily reminiscent of the generic approach used today for compact models. The most incredible feature of this work was that it *developed a compact model to propose a new form of transistor which did not exist*.

Today, technology computer-aided design (TCAD), which solves the basic partial differential equations that model semiconductor behavior, is commonly used to help investigate proposed device structures. TCAD did not exist in Shockley's day; that he developed a compact model to understand and explain his proposed device is sheer genius.

Another proposal from that paper still permeates our industry. For the terminal names for his (theoretical, not experimentally verified) "unipolar field-effect transistor:"

> *The choice selected is "source" for the electrode through which the carriers flow into the channel, "drain" for the electrode into which the carriers flow out of the channel, and "gate" for the control electrodes that modulate the channel.*

But let us back up a bit.

Once the transistor was invented, the advantages of being solid-state (no energy hungry cathode heaters to boil off electrons, no vacuum sealed glass tubes to compromise reliability, especially under "robust" physical perturbation) were sufficient to pique interest despite its (initially) high cost. However, to move from being a research laboratory breakthrough to being a commercial success, transistors needed to be used in products.

This meant circuit designers needed to mentally understand how transistors worked, and have some form of capability to do ''back of the envelope" (SPICE would not arrive for over two decades) calculations to understand how their circuits behaved, and how to properly design and optimize component values and biasing in their circuits.

The reference for this is the classic "Electrons and Holes in Semiconductors" (with the important subtitle "with applications to transistor electronics") by Shockley

[2]. Many of us older semiconductor engineers considered this the "bible," and cut our teeth digesting it. And many early transistor circuits were designed based on the mental images, i.e., models, espoused in that book.

However, the emphasis in [2] is more on the detailed physics of transistor and *pn*-junction operation than on the key aspects of device behavior, in essence large-signal behavior (from which DC operation and small-signal behavior naturally follow), that are critical to understand transistor behavior to enable circuit design.

III. A Side-Track Into Circuit Simulation

As mentioned previously, the concept of a compact model was introduced more than ten years before computer programs to analyze circuit performance appeared. The original purpose of the compact model was to encapsulate the operational features of a new device and to assist engineers to design circuits that employed that new device. A requirement of these compact models was that they had to be fairly simple and any accompanying equations had to be amenable to evaluation with a slide rule or a calculator. Because compact models were intended to assist engineers with circuit design, it is not surprising that these models were schematic representations of the device, as opposed to lengthy equations. The classic example of this type of compact model is the Ebers-Moll BJT model, published by Bell Laboratories researchers J. J. Ebers and J. L. Moll in 1954 [6], see Fig. 2.

Compact modeling changed drastically with the arrival of circuit analysis programs in the 1960's, followed by the evolution of circuit simulators in the 1970's. Early circuit analysis programs include ECAP from IBM [7] and NET-1 from the Los Alamos National Lab [8]. At about the same time, R. K. Jensen published a paper describing his implementation of the Ebers-Moll model, in ECAP, for DC and transient analysis [9].

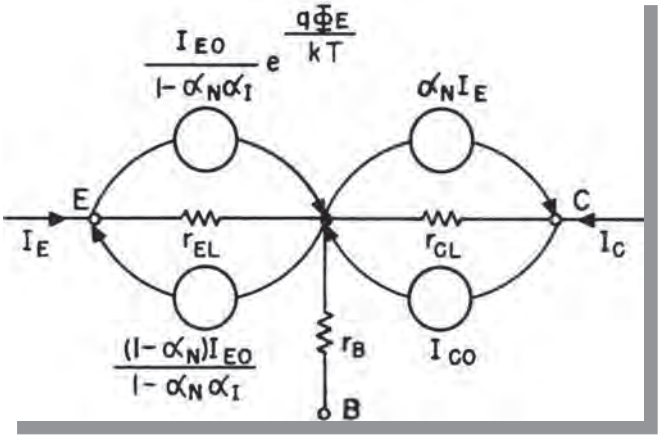

Figure 2. Fig. 5 of [6], from 1954. ϕ_E is the base-emitter bias V_{BE}. The quantities subscripted O are parameters, α_N and α_I are normal (forward, I_C/I_E) and inverted (reverse, I_E/I_C) current "gains."

Combining circuit simulators and compact models had an immense effect on the design community. On the one hand, simplicity was not as relevant, since it was no longer the designer who had to evaluate the device equations. Compact models could therefore include greater complexity to provide a more physical representation of the device. On the other hand, including compact models in a circuit simulator proved to be a difficult task. Simulation algorithms require that the device equations for current, charge, and flux be continuous with respect to voltage, and the algorithms work better if the first derivatives are continuous as well. There is also the tradeoff of accuracy of a model versus the computational complexity of the model. Finally, compact modeling came to require a reasonable knowledge of how circuit simulators work and how to implement a model in a simulator. This was a daunting task for circuit designers and device physicists who were unfamiliar with computer programming. These issues persist in the compact modeling world to this day.

IV. Empirical Compact Models

Notwithstanding the pioneering *pn*-junction diode and JFET models from Shockley, when it came to the bipolar junction transistor (BJT, which Shockley invented after the point-contact transistor of Bardeen and Brattain 75 years ago), the theory lagged a bit.

Experimentally, it was observed that the collector current I_C of a BJT was (closely) proportional to the emitter current I_E over many orders of magnitude of current; the ratio of those currents is now universally known as the quantity α. This observation, along with the Shockley relation (1), was the basis of the Ebers-Moll BJT model [6]. While the Ebers-Moll model was, for its time, quite "physical," through the lens of history it missed the fundamental physics that underlies BJT operation.

Many data-driven approaches to modeling for circuit simulation have been, and continue to be, used. These include interpolation, a.k.a. table-based, models [10], and neural networks [11]. In the power RF community such approaches are considered to be "compact" models [12]; in the broader IC design community they are not [13].

V. Physical Compact Models: Hermann Gummel Sets the Path to the Future

While empirical compact models can be quick to generate, they have some drawbacks; it is difficult to include

- global statistical variation
- local statistical variation (i.e., parametric mismatch)
- geometric scaling, including layout dependent effects (LDEs)
- temperature variation, including self-heating
- fundamental requirements like smoothness, monotonicity, and symmetry

For these reasons, compact models based on physical (structural and layout) parameters and physics-based

analysis are today the norm, and in fact all industry standard models from the Compact Model Coalition (CMC) [14] are physical, not empirical, compact models.

The guiding light, the archetype, for all modern compact models is the Gummel-Poon (GP) model for BJTs [15], which is based on the Gummel integral charge-control relation (ICCR) [16]. The collector-emitter transport current is

$$I_{CE} = A_E \frac{q n_i^2 \phi_t \mu}{t_B N_B} \frac{exp\left(\frac{V_{BE}}{\phi_t}\right) - exp\left(\frac{V_{BC}}{\phi_t}\right)}{q_B} \quad (2)$$

where A_E is the emitter area, n_i is the intrinsic concentration, and t_B and N_B are the thickness and doping of the base, respectively. The normalized base charge q_B (details not shown) embodies both modulation by the bias dependence of the depletion region edges in the base (the Early effect [17]) and modulation by high-level injection.

Figure 3 shows the effect of q_B; how this is included in modern BJT models was pioneered in [15], which was a work of sheer genius.

Once you understand (2) you understand how BJTs work. That is the power of a physical, intuitive, compact model.

VI. MOS Transistor Compact Models

Given the importance of CMOS technology today, it is perhaps surprising how long, tortured, and fractured the development path is to modern MOS transistor models.

MOS transistors come in several flavors, including: bulk (planar), silicon-on-insulator (SOI), dual-gate, tri-gate, and gate-all-around (a.k.a. nanowire or nanosheet) transistors. The basic operation of all is the same: an electric field (from the applied gate bias) transverse to the surface, whatever the device structure, induces a conducting channel, and a longitudinal electric field (from the applied drain-source bias V_{DS}) drives current through the induced conducting channel.

There are 5 general classes of MOS transistor models:

- threshold voltage (V_T) based models
- inversion charge based models
- surface potential based models
- the virtual source (VS) model
- the Taur approach for dual-gate MOS transistors

The first of these is probably the most familiar, as it is how MOS transistor operation is taught in most undergraduate classes and design textbooks. From [18] the drain current in a planar MOS transistor is

$$I_D = \frac{\mu C'_{ox} W}{2L} \{ [V_{GS} - V_T(V_{SB})]^2 - [V_{GD} - V_T(V_{DB})]^2 \} \quad (3)$$

where W and L are the transistor length and width, respectively, C'_{ox} is the oxide capacitance per unit area, and V_T is the threshold voltage, which depends on the voltage w.r.t. the body. The BSIM4 model [19] represents the pinnacle of development of V_T based models, and has been used for the design of more ICs than any other MOS transistor model. However, the drain/source symmetry inherent in (3) was lost over the years, which caused significant issues for simulation of RF CMOS circuits, so V_T -based models have fallen out of favor.

Models based on the (normalized) inversion charge density q_i have been independently developed multiple times, starting in 1987 [20], and culminating in BSIM-BULK [21]. From the 10,000 m level, this approach posits that

$$|q_i| + ln(|q_i|) \propto V_p - V_{ch} \quad (4)$$

where V_p is the pinchoff voltage and V_{ch} is the "channel" voltage. The beauty of this formulation is that it naturally transistions from the approximate exponential variation of q_i with gate bias in weak inversion to the near linear variation in strong inversion.

The surface potential approach is generally recognized as the most physically accurate formulation for MOS transistor modeling, and is also the basis of the CMC standard model for FinFETS [22]. It is too complex to summarize here, interested readers can digest the overview of [23].

A rather different approach to modeling MOS transistors is the "virtual source" formulation [24]. All FET models assume there is no recombination in the channel. Therefore, the product of the inversion charge density $Q_i(x)$ and the average carrier speed $v(x)$ *must be the same at every point along the channel*. So, you only need to model those quantities at one point along the channel to characterize the behavior of the whole transistor. Fig. 4 shows how this approach works: x_o is the position along

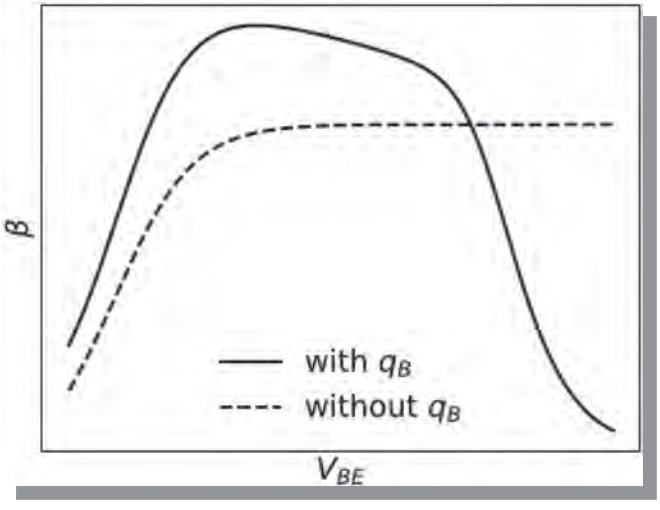

Figure 3. BJT current gain $\beta = I_C/I_B$ from (2) with and without the q_B term included. The behavior with q_B is physically correct, the behavior without q_B, which is exhibited by the empirical Ebers-Moll model, is not physically correct.

the channel of the virtual source, so Q_i and v at that point are used to model I_D.

An innovative approach to modeling dual-gate transistors was pioneered by Yuan Taur [25]. This approach, unlike the other approaches listed above, has not been adopted in any CMC standard model. But it is so different, and so elegant, it warrants attention.

Amazingly, most modern MOS transistor compact models (the exception being the VS model) are based on the "gradual channel approximation," which was first introduced by Shockley for JFETs [5]. In a nutshell, this posits that to solve Poisson's equation for the charge density in the channel, the longitudinal electric field can be ignored, and only the transverse electric field need be considered. Corrections for the inaccuracies of this approximation have been investigated [26], but the fundamental approximation of [5] is still the basis of modeling for all FETs.

VII. Compact Models for Other Devices

The models briefly outlined above are relatively simple. Probably the most complex devices to model are LDMOS transistors, for which modeling of the drift region, which allows them to sustain the high voltages necessary to interface to the real world, is at least as complex as modeling the core MOS transistor. The low-voltage digital circuits in our cars and phones have to interact with the real world at some point, and in many cases LDMOS transistors are the interface.

Even what we consider to be basic, simple devices such as capacitors and inductors are neither basic nor simple in modern ICs: their layouts are increasingly complex, and accuracy requirements for the models, over layout and frequency, continually escalate ... if they didn't, your phone battery may die faster than it already does!

Even resistors are not simple: As undergraduates we are all indoctrinated that $V = I \cdot R$, but integrated resistors are a bit more complex than that: their behavior is affected by depletion pinching, velocity saturation, and self-heating, and they are really JFETs [27].

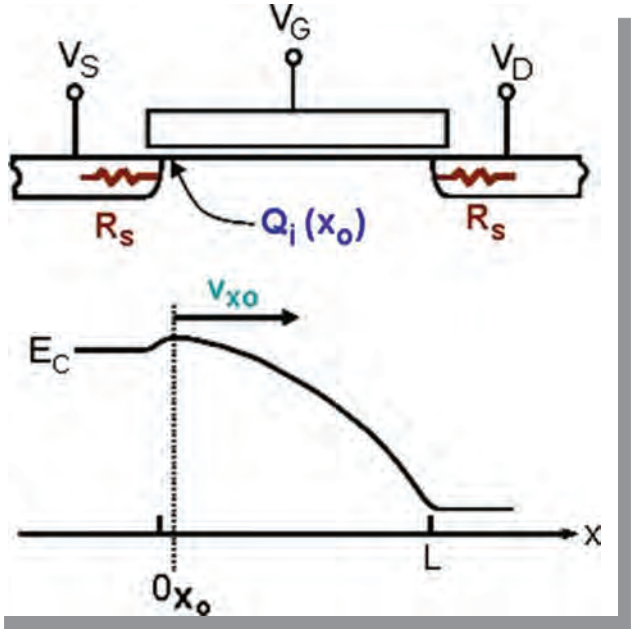

Figure 4. Fig. 1 of [24], virtual source view of MOS transistor operation.

VIII. Why Compact Models are Always Playing "Catch-up"

Compact models are vastly more accurate today than they were 75 years ago. But they are still imperfect; in several aspects embarrassingly so for model developers. With the increasing importance of LDEs and parasitics, and the inability of models to keep up with the cadence of technology development in these areas, there will always be "unsimulatable" effects.

The expectations of how accurate compact model are have continued to escalate, yet the gaps between simulation and reality, especially for compact models, have never been closed as more physical effects come into play and accuracy requirements have become more demanding. The Shichman-Hodges MOS transistor model [18] was revolutionary 50 years ago, but is completely inadequate for today's needs. As technology continues to scale, what "fine details" of modeling bubble up to be make-or-break capabilities continue to evolve.

The expectations for compact models today are much, much more stringent than they were 75 years ago. Circuits have 10^8 more components, supply voltages are significantly smaller so sensitivity to variability is much greater, sensitivity to inaccuracies in models is vastly higher, and many more circuit performance characteristics are important. The capabilities of simulators and compact models have improved astronomically, but the complexity of the circuits that are simulated, and the expectations of the accuracy of those simulation results, have increased at a greater rate. So, basically, the algorithms and models in SPICE are continually playing catch-up.

The reality is that simulation algorithms and compact models have, despite huge steps forward, struggled to keep pace with the increasing expectations of how accurate they should be.

This is not a problem for expert IC designers. It is a huge problem, recognized in both industry and academia, for the "SPICE jockeys" who blindly run, and trust, SPICE simulation results. *There is no substitute for knowledge of how circuits operate and of physical understanding of how devices behave.*

Acknowledgment

An extended version of this article will appear in the commemorative volume, ***75th Anniversary of the Transistor***, IEEE Press-Wiley, 2023.

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THIRD BREAKDOWN: A PHYSICAL MECHANISM FOUND IN HIGH-K METAL-GATE CMOS

STEVE S. CHUNG
CHAIR PROFESSOR, NATIONAL YANG MING CHIAO TUNG UNIVERSITY, TAIWAN

There are two major well-known breakdowns, soft-breakdown and hard-breakdown, in MOSFET's history. Not until 2015, a world-first observation of the breakdown, different from the above two breakdowns, named dielectric fuse breakdown, **dFuse**, was discovered, as a result of CMOS technology moving into the 45 nm node High-k Metal-gate (HKMG) era. Here, we will describe how it was found and how to understand the physics underlying this breakdown mechanism.

1. Introduction

In the history of the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET), the quality of its gate oxide has been a cornerstone of silicon-based semiconductor integrated circuits. The changes of gate dielectrics from conventional SiO_2 gate oxide into high-k materials brought us more challenges to the transistor's reliability, especially when the MOSFET dimension is continually scaled.

At the beginning of 2000, the development of high-k dielectrics embarks a new era of the CMOS technology. The purpose of high-k materials is to solve the leakage current through the transistor's gate [1]–[2]. This led us to further development of the gate stack towards a new era of the so-called high-k metal-gate (HKMG) CMOS generation. Namely, the rapid growth of high-end processors (CPU, GPU, and MCU) and industrial applications such as mobile phones, notebooks, and PAD, to mention a few [3], relies on the technology improvement or breakthrough of various high-quality gate stack films. Depending on the making of high-quality gate dielectrics, it will provide reliable, ultra-low power and low leakage, and high-end IC products.

In terms of the MOSFET's reliability, Time Dependence Dielectric Breakdown (TDDB) [4], Bias Temperature Instability (BTI), mobility degradation [5], stress-induced leakage current (SILC) [6], are major considerations, in which SILC has been a critical issue to the power consumption of CMOS devices. A huge number of published articles have stressed the importance of methods for suppressing the gate current in high-k dielectrics. Numerous high-k materials have been investigated to further reduce the gate leakage current through the improvement in making the interfacial layer between high-k materials and the Si substrate [7]. These results led to the manufacturing of the HfO_2-based dielectrics as the mainstream of gate dielectrics in advanced CMOS devices at 45 nm generation of CMOS technologies [2], see the trend of scaling in Fig. 1.

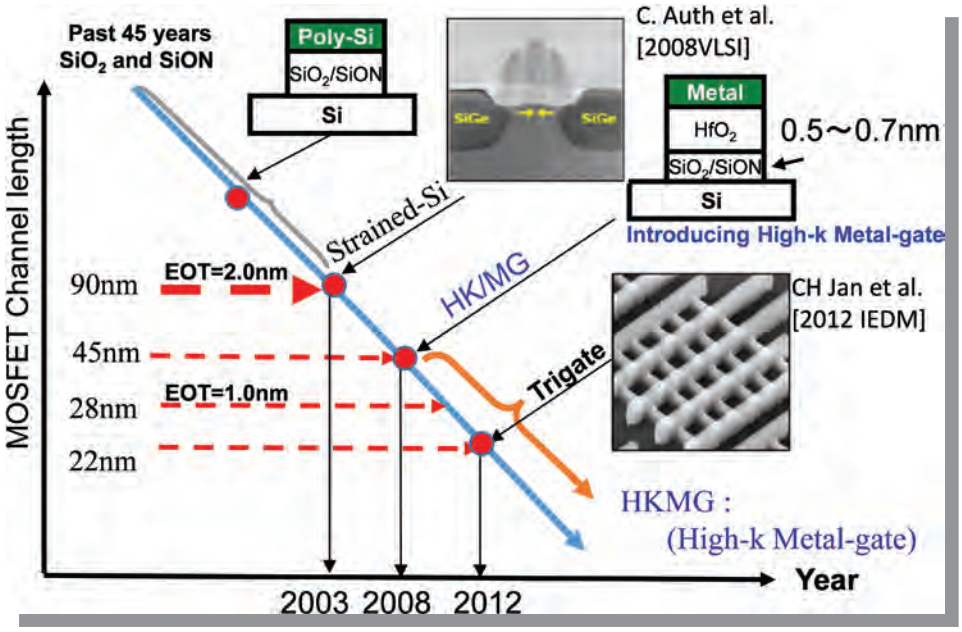


Figure 1. The scaling of MOSFET, courtesy from H. Iwai (TIT) and a redrawing.

2. Experimental Observations

A popular experimental method to examine the reliability of the gate dielectric in MOSFET is the so-called Time-Dependent Dielectric Breakdown (TDDB) [4] which is used to impose stress on the device and to accelerate the transistor's aging. It has a direct impact on the

breakdowns that were observed. The most commonly used test methodology to conduct the TDDB is constant stress, which includes constant voltage stress or constant current stress. That is, a voltage or current is applied to the gate, while its leakage current is being monitored. The time for the oxide to reach breakdown is called the time-to-failure.

Fig. 2(a) is the experimental observation of the transient behavior (i.e., gate current) in the gate dielectric in a 28nm high-k MOSFET [9] under long-term stress of Positive Bias Temperature Instability (PBTI) (i.e., by applying voltage stress on the n-MOSFET with appropriate high temperature). This is to intentionally accelerate the transistor's aging. The gate dielectric has Equivalent Oxide Thickness (EOT) = 1.35 nm, composed of a HfO_2 with a thickness of 2.8 nm and a SiO_2 interfacial layer with a thickness of 1.2 nm. It was observed that there are several switching behaviors in the transient gate current, as in the inset of Fig. 2(b). These switching behaviors came from the interaction between electrons in the Si substrate and traps in the gate dielectric. In the beginning, the gate leakage is small, and then strong current noises are raised, i.e., soft-breakdown occurs. Eventually, the number of traps reaches a critical value, leading to a hard breakdown with a sudden increase in the current. This can be explained by the conceptual diagram in Fig. 2(b) where the breakdown path is assumed to be a percolation path of the traps, connecting together to form a filament, that is, a conduction path with traps nearby serving as a switch to control the current flow through the filaments. The trap location is responsible for the magnitude of the current flow.

2. Fundamentals of Ig-RTN

To understand the aforementioned noises in the percolation path, Random-Telegraph-Noise (RTN) measurement can be employed. RTN is a switching phenomenon of electrical characteristics in a transistor caused by the capture and emission of carriers by the oxide trap, as shown in Fig. 3(a), with two characteristic time constants, τ_c, and τ_e. A real measurement was given in Fig. 3(c), which was named as I_g RTN measurement [10]–[11]. RTN signal, in the form of a repetitive digital waveform with two or more levels, depends on the number of traps [12]. In the following, we will examine first the properties of RTN traps in a high-k gate dielectric. The location of the traps in the MOSFET is strongly related to the conduction path in the gate dielectric, i.e., filament. Also, the conduction path is indirectly related to the breakdown.

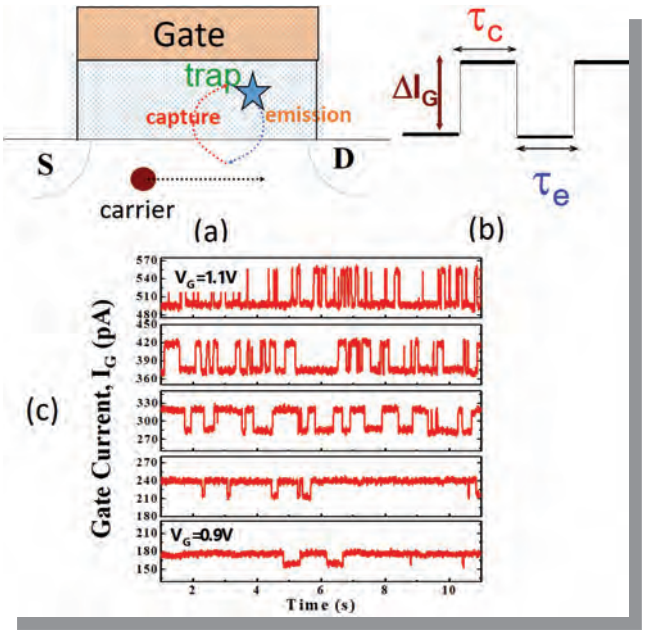


Figure 3. (a) The schematic of trapping and de-trapping in a single RTN, (b) the definition of τ_c and τ_e, and (c) the measured two-level I_g waveforms.

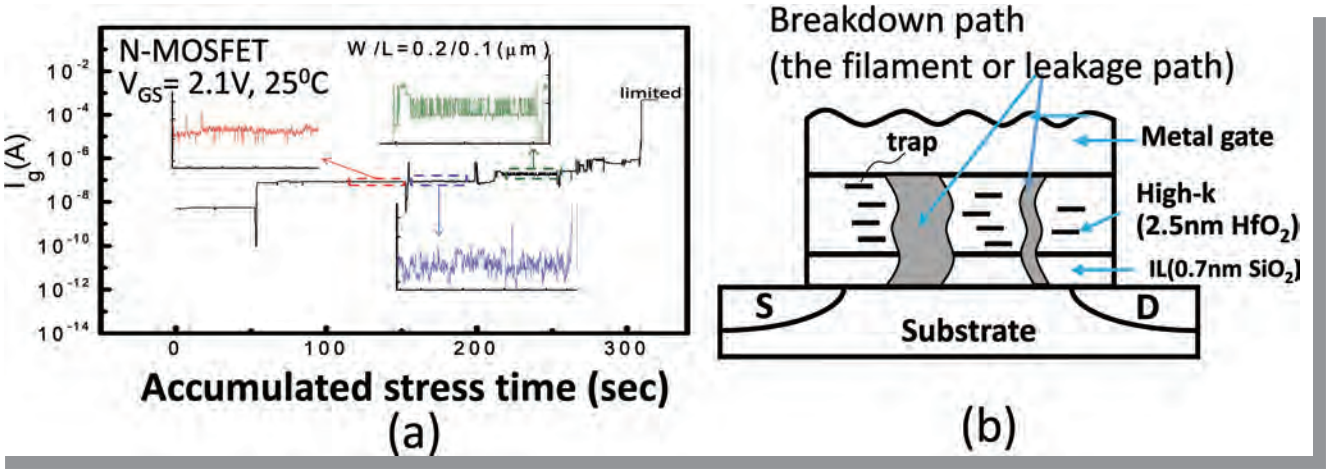


Figure 2. The transient characteristics of TDDB stress-induced gate leakage current. Different RTN signals can be observed as stress time progresses. (b) A conceptual diagram to show the breakdown path caused by the leakage.

3. The Concept of Leakage Path from Experiment

Once we have a measured two-level I_g current and its variation as a function of time at different V_{GS} biases, we may calculate the normalized amplitude of variation of the gate current ($\Delta I_g/I_g$) for various traps, as shown in Fig. 4(a) in the inversion region. But, in the deeper region close to the Si channel region (i.e., inside SiO_2), accumulation region traps in MOSFET can be measured as given in Fig. 4(b). Fig. 4(c) shows the location of the traps in the energy band diagram. Then, we may assume that a *leakage path* or *filament* is formed surrounding the generated traps. Moreover, the fluctuation of the gate current is affected by the trap position. For example, if the trap is very close to the path, the fluctuation will be very large, or it will be smaller when the trap is far away from the path. In this case, it is believed that trap a is closer to the path than that trap c. More importantly, the gate's current path can thereby be traced by the traps. As a result, as the stress time progresses, the gate leakage current path will grow near the traps in dielectrics and the gate current increases with larger amplitudes of fluctuations. In short, as long as we can identify the trap location from the gate through the dielectric and to the silicon substrate, we can always draw a leakage path or a synonym of filament which is responsible for the leakage current.

4. Ig-RTN Transient Measurement Technique-Version 2.0

Fig. 5(a) shows the measurement setup, named Version 2.0 I_g-RTN, i.e., I_g-RTN transient measurement technique [14], which is used to profile the generation of traps as a function of time. First, the constant voltage was carried out and then held for performing I_g-RTN measurement [9] in order to detect the traps where ramped voltages were applied gradually. It was repeated until the dielectric went to breakdown. After gathering traps at a specific time, one can determine the physical location of the generated traps in the dielectric. It was continued until the dielectric reached breakdown.

First, as shown in Fig. 5(b), we applied a constant voltage stress on the MOSFET under V_{GS}= 2.4 V at room temperature, i.e. for V_{GS} voltage a little higher than the normal operating voltage V_{DD} (e.g., for a 28 nm CMOS technology, V_{DD}= 1.8 V). At 10 seconds, we could detect trap #1, close to the SiO_2 interface. After the next 10 seconds, the stress generated a 2nd trap, #1.2. After another 30 seconds, several traps, #2.1 and #2.2 were generated. We repeated the same procedure until the gate dielectric reached a breakdown. The total accumulated time is 660 seconds. The first few traps were generated near the interface of HfO_2 and SiO_2 and then circle around at this interface. Eventually, as time progresses further, it reaches a breakdown [9].

Next, the PBTI stress test is performed at V_{GS} = 2.45 V and 125 °C, on the MOSFET of the same size. Fig. 5(c) demonstrates the experimental result of the constant voltage BTI-induced breakdown path. It shows a different path from the previous one (Fig. 5(b)), in which the trap was generated at the interface of SiO_2 and Si substrate, and then, most of the generated trap is a single trap. In a shorter time, it reached a breakdown. The latter is a hard breakdown (Fig. 5(c)) whereas the former one (Fig. 5(b)) is a soft breakdown. The former traps with longer time form a spindle shape filament (path). The latter exhibits a snake-walking behavior, named "snake path".

5. The Discovery of a Third Breakdown: Dielectric-fuse Breakdown

Based on the above soft-breakdown and hard-breakdown that people usually understood, the transistor will go into soft-breakdown first and then be developed into a hard-breakdown for the gate dielectric to fail. This results in a short path between the gate and the source/drain. However, in the measurement of Fig. 6(a), we applied a higher voltage and shorter duration of pulse on the MOSFET gate, i.e., a higher electric field across

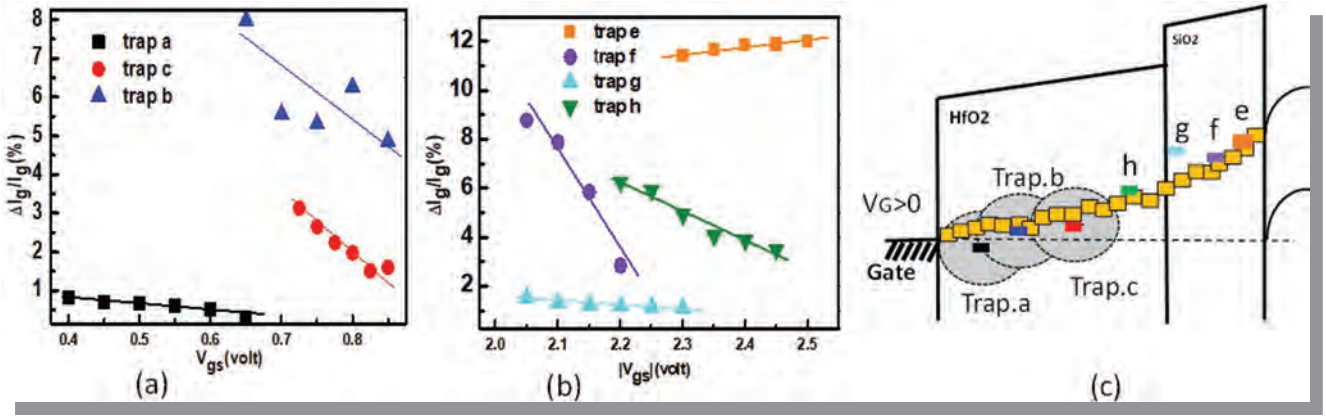


Figure 4. (a) The normalized gate current induced by traps a, b, c, (b) the normalized gate current induced by traps e to h, (c) a leakage path drawn along traps.

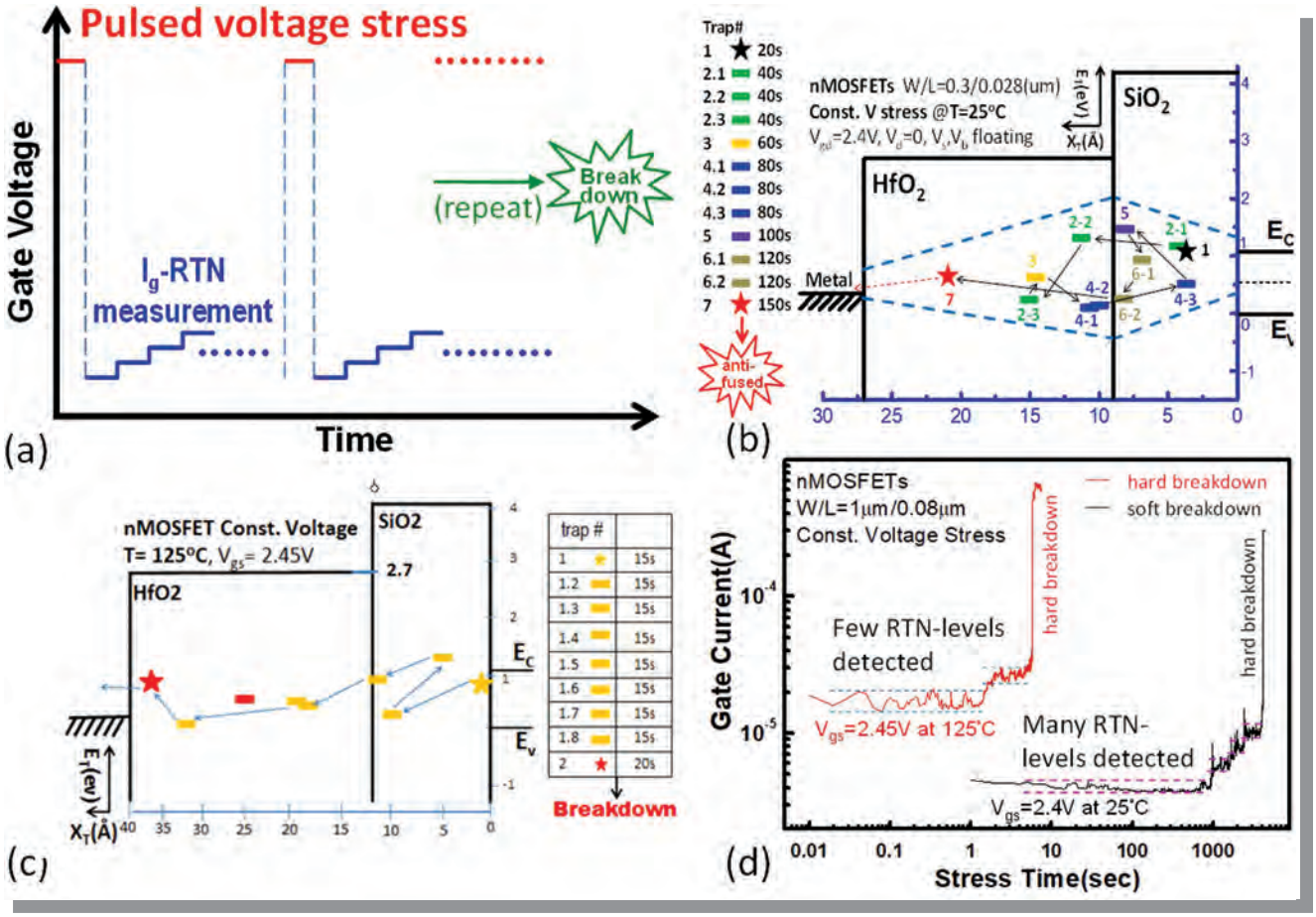


Figure 5. (a) The experiment to extract the generated traps. (b) The evolution of traps versus stress time in n-channel MOSFET under the room temperature voltage stress. (c) The evolution of traps versus time under high-temperature PBTI stress. (d) The transient characteristics of two different types of leakage current. The black curve is a soft breakdown, while the red curve is a hard breakdown.

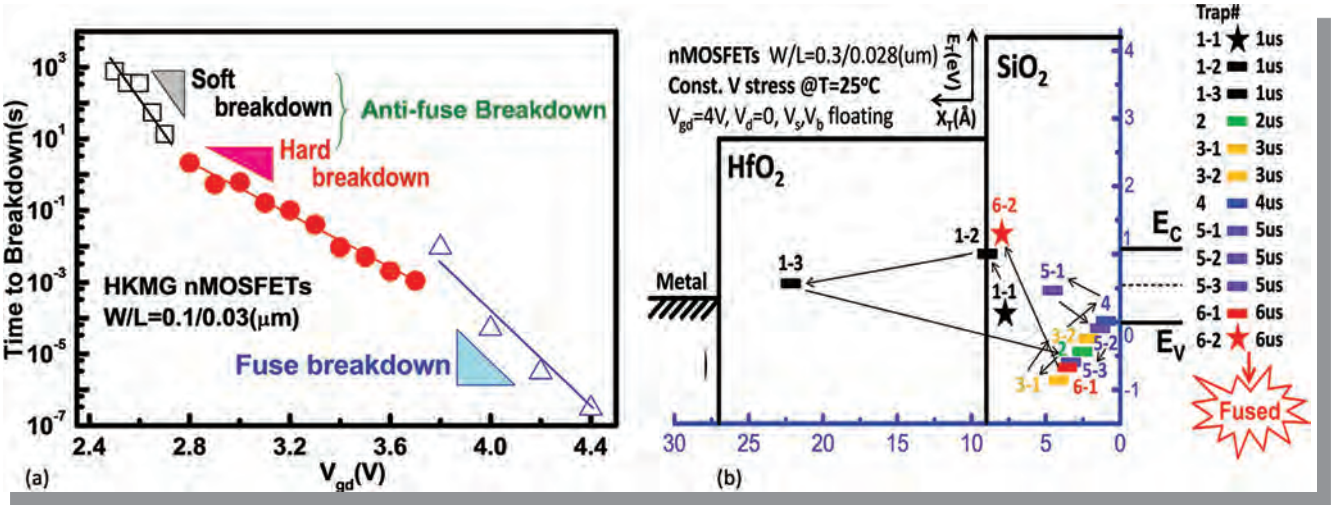


Figure 6. (a) The measured TDDB for three different breakdowns. (b) The evolution of traps versus stress time in n-channel MOSFET under higher constant voltage stress at V_{gd}= 4 V (in the range of fuse breakdown). The leakage path did not create traps in reaching the metal gate (can be compared with Fig. 5(b)).

the high-k/interfacial gate dielectric, the gate dielectric became open and the gate current will be pulled down to a very low level (clockwise); on the other hand, it will be raised to a higher level, labeled as anti-fuse (counter-clockwise), i.e., short. The latter, anti-fuse is the evidence of the hard-breakdown, consistent with Fig. 5(c) and (d),

leading to an increase in the gate current after a breakdown. On the contrary, with an increase in applied voltages, the gate current dropped to a very low level. This is because during the process of trap generation, oxygen ions were annealed out and more oxygen vacancies were left at the interfacial layer. This led to a broken filament between the gate and drain, i.e., no current flowing through the gate, located inside the interfacial layer. As a consequence, after the burn-out of this interfacial layer, the SiO_2 layer exhibits a porous structure. Hence, we gave it a new name called third breakdown- dielectric fuse breakdown, dFuse [13].

After several TDDB tests, we can see the difference between three different breakdowns, as given in Fig. 6(a).

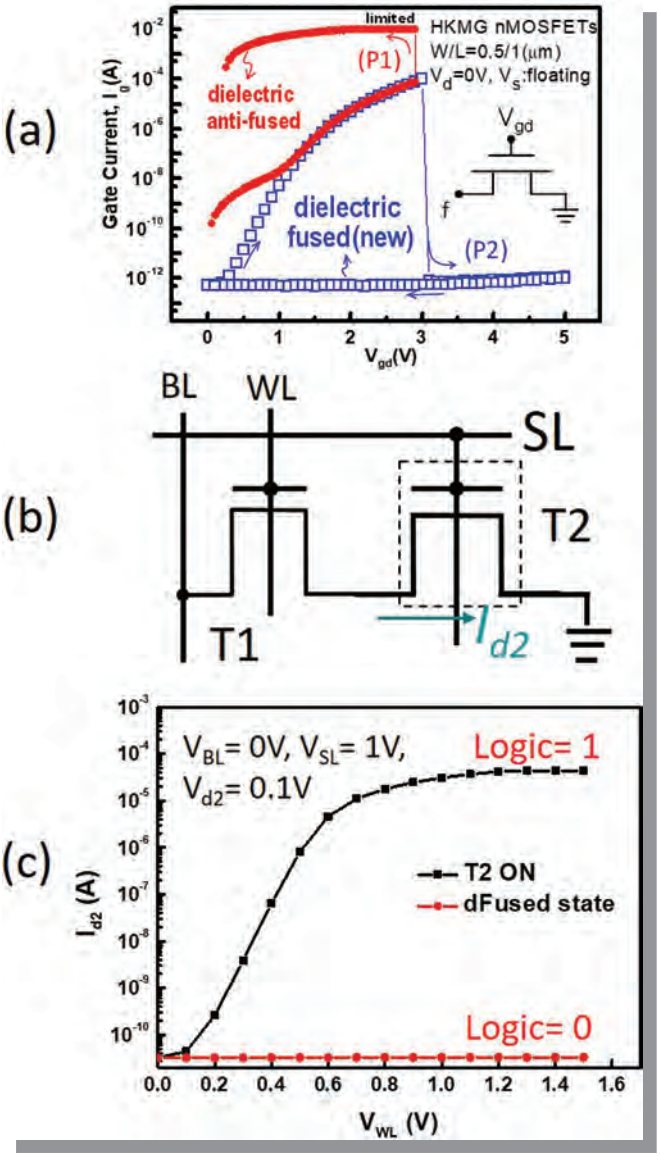


Figure 7. (a) The measured gate currents for the conventional hard breakdown (anti-fused) and a dielectric fuse breakdown. (b) A unit cell of OTP. (c) Two different levels of the measured currents, I_{d2}, represent two logic states.

All three types of breakdown show different slopes in this time-to-breakdown plot. Obviously, the dFuse breakdown takes a shorter time in comparison to the hard-breakdown. To further understand the path development during the dielectric fuse breakdown, Fig. 6(b) shows the results after the dielectric fuse breakdown. Traps are generated at the interface of the high-k/interfacial layer (IL), in which we see the traps were generated and circled around in the IL layer and will not reach the gate for breakdown, which is different from Fig. 5(b). As a result, these IL traps create porosity in SiO_2 and eventually a gap to block the current path going through the gate dielectric. Thus, we see a sudden decrease in the gate current, as shown in Fig. 7(a) (blue-colored curves).

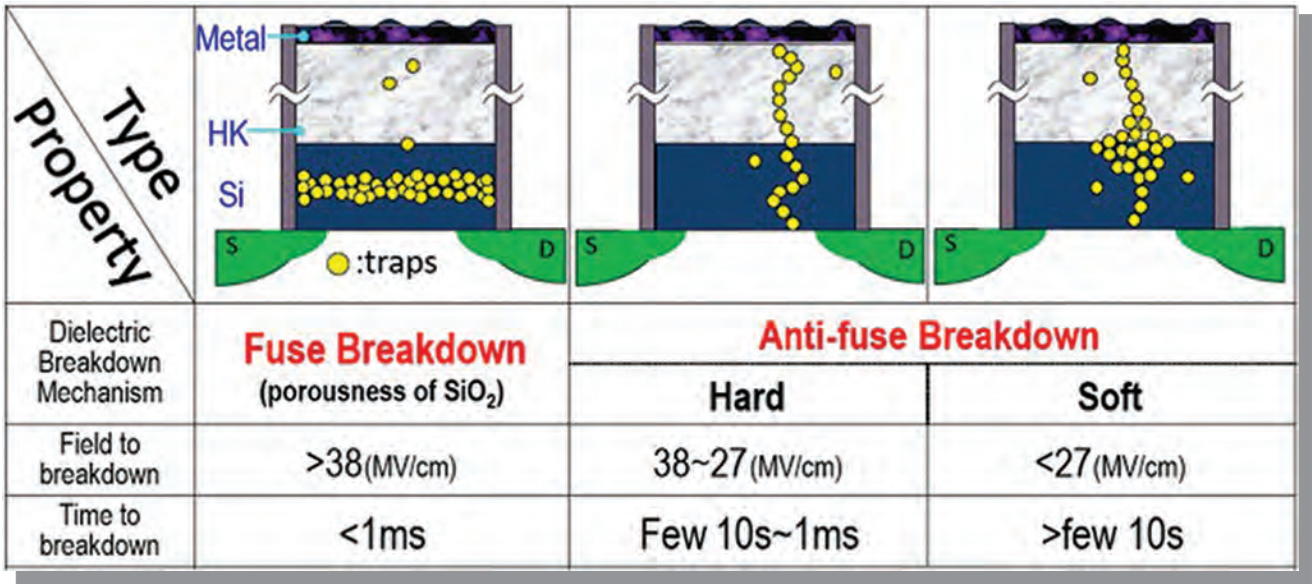
In short, the dielectric fuse, dFuse, breakdown that we observed can be achieved by applying across the gate-to-drain a *higher voltage but shorter pulse, or the same voltage as hard-breakdown but longer time,* to achieve breakdown.

By taking advantage of the observed dFuse breakdown, it may find application to the One-Time-Programming memory (OTP) [14], The architecture of an OTP as a unit cell, shown in Fig. 7(b), consists of a control transistor (T1) and a second transistor(T2) serving as storage. The write operation can be made by applying a pulse with 4.2V high voltage and 1 μsec duration to the T2, it causes damage to the gate dielectric and the gate has no control over the T2 channel with zero drain current. It provides a logic 0, in Fig. 7(c). If instead there is no damage on the T2 gate, the drain current will be read as a high-level current which represents logic 1. Since the gate dielectric is ruptured with a condition of dFuse, it creates a permanent failure of T2 from which T2 remains at logic 0 and could not be recovered. So, this kind of memory is named one-time programming. An example of the MACRO design can be found in [15].

In summary, the difference between hard/soft breakdown and dFuse is shown in the comparison of Fig. 8, in which the dielectric dFuse breakdown creates porosity of the interfacial layer (SiO_2) and the burnout region is along the horizontal direction. The OTP provides us with several applications, in the IoT era, such as key encryption, device identity, code storage in mobile phones, power management in mobile phones, LCD drivers, and code storage in Micro Controller Units (MCU), to name a few.

5. Summary and Conclusions

Since the inception of the first version DC I_g-RTN measurement technique that was developed in 2008 [10]–[11], it brought us more opportunities to understand the reliability of breakdowns, from soft-breakdown to hard-breakdown. Later, it led to the discovery of a third breakdown, named dielectric fuse breakdown, relying on a significant improvement of I_g-RTN transient in 2015 [13].



Type / Property	Fuse Breakdown	Anti-fuse Breakdown	
Dielectric Breakdown Mechanism	(porousness of SiO_2)	Hard	Soft
Field to breakdown	>38 (MV/cm)	38~27 (MV/cm)	<27 (MV/cm)
Time to breakdown	<1ms	Few 10s~1ms	>few 10s

Figure 8. The comparison between dFuse breakdown and anti-fuse (hard- and soft-breakdown).

As a consequence, we will be able to distinguish three different types of breakdown. In addition, both the first DC version and version 2.0 I_g-RTN measurement techniques allow us to understand the reliability physics underlying the ever-increasing leakage in HKMG CMOS as the scaling of transistors continues. In addition to the understanding of physics, the dFuse that was unveiled here will soon find broader applications in the hardware security design, such as the OTP [15], Physical Unclonable Function (PUF) [16] and for use in mobile phones and MCU, such as power management, cryptography, key generation, encryption, etc. More details of the experimental implementations can be found in [17].

Biography

Steve Chung received the Ph.D. degree in Electrical Engineering from the University of Illinois at Urbana-Champaign, Champaign, IL, USA. His Ph.D. advisor was the world famous CMOS co-inventor, Prof. C.T. Sah.

Currently, he is NYCU and UMC Chair Professor at the National Yang-Ming Chiao Tung University (NYCU). He has been the Dean of International Affairs Office and Executive Director of school level research center, (2007–2008). He was a visiting professor with Stanford University, University of California-Merced, between 2001–2009 successively. He has been the consultant of two world largest IC foundries, TSMC and UMC. His recent research areas include: FinFET, flash memory, resistance Memory Technologies, from storage to AI application. He has performed more than 35 times of in-person presentations in IEDM/VLSI and holds more than 40 patents.

He is an IEEE Life Fellow, IEEE Distinguished Lecturer, Senior Editor of Applied Physics-A (Springer), EDS Taipei chapter chair, and with past involvements as IEEE EDS Board of Governor for more than 12 years, EDS Regions/Chapters Chair, and Editor of J-EDS, EDL(2002–2008). Among numerous awards, he has been a recipient of 3-times Outstanding Research Award(NSC), *Pan Wen Yuan award* (2013), Lifetime achievement award as National Inventors (2019), etc.

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Upcoming Technical Meetings

IEEE Symposium on VLSI Technology and Circuits returns to Kyoto, Japan

The 2023 IEEE Symposium on VLSI Technology and Circuits will be held on 11–16 June at the Rihga Royal Hotel, Kyoto, Japan, as an in-person format with on-demand content to deliver on the exciting theme of "Rebooting Technology and Circuits for a Sustainable Future." The 43rd Symposium is jointly sponsored by the IEEE Electron Devices Society (EDS) and IEEE Solid-State Circuits Society (SSCS) as well as the Japan Society of Applied Physics (JSAP).

VLSI Symposium is the premier global venue that promotes synergies between technologists and designers on today's applications and future breakthroughs. From process integration and advanced device architectures to circuit designs and systems, the Symposium covers innovations in a wide range of domains such as artificial intelligence, connected objects, autonomous vehicles, and biomedical applications. To facilitate these interactions, this year's Symposium will offer joint-interest sessions on special areas of Technology and Circuits such as AR/VR/MR/Metaverse and its integration, aerospace applications, BEOL interconnects and BPD/BSPDN, more novel memory devices to continue scaling, new computing, 3D package technologies and system integration.

Four plenary talks by distinguished industry leaders will open the Symposium:

- Surya Bhattacharya (Director, A*STAR IME)
- Partha Ranganathan (Vice President, Google)
- Siva Sivaram (President, Western Digital)
- Hiroyuki Mizuno (Distinguished Researcher, Hitachi)

The two evening panel discussions will focus on the sustainability of VLSI. What is scalable and sustainable in the next 25 years? How can we reboot industry-academia joint research for a sustainable VLSI future?

The Symposium will offer two full-day short courses prior to the technical sessions to prepare participants on Advanced CMOS Technologies for 1 nm & Beyond as well as on Future Directions in High-Speed Wireline and Optical IO. The Symposium will conclude with a full-day Forum focused on Compute Paradigms for Secured Microelectronics and Combinatorial Optimization. The Symposium program also includes a lively demo session and is complemented by six workshops on research and application topics.

We cordially invite you to attend the 43rd IEEE Symposium on VLSI Technology and Circuits. For more information, please visit www.vlsisymposium.org. See you in Kyoto!

Symposium Chairs:
Katsura Miyashita, Toshiba Electronic Devices & Storage Co.
Yusuke Oike, Sony Semiconductor Solutions

Symposium Co-Chairs:
Gosia Jurczak, Lam Research
Borivoje Nikolić, University of California, Berkeley

Program Chairs:
Takaaki Tsunomura, Tokyo Electron Limited
Mototsugu Hamada, The University of Tokyo

Program Co-Chairs:
Vijay Narayanan, IBM
Ron Kapusta, Analog Devices, Inc.

2023 IEEE International Memory Workshop

The 15th International Memory Workshop (IMW) is currently planned as an on-site event on 21–24 May 2023 in Monterey, California. The conference brings the memory community together in a workshop environment to discuss the memory process and design technologies, applications, market needs, and strategies. It is sponsored by the IEEE Electron Devices Society and meets annually in May. The IMW is a premier international forum for both new and seasoned technologists having diverse technical backgrounds to share and learn about the latest developments in memory technology with the global community. The scope of workshop content ranges from new memory concepts in early research to the technology drivers currently in volume production as well as emerging technologies in development. The workshop will start on Sunday, 21 May with a Tutorial Session, followed by Technical Sessions from Monday, 22 May until Wednesday, 24 May. The evening panel discussions will address hot topics in the memory field and active participation and discussions will be encouraged.

Panel discussion IMW 2022

For more information, registration and the actual program check the conference website: https://www.ewh.ieee.org/soc/eds/imw/index.htm

Dirk Wouters
2023 IMW Publicity Chair

2023 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium

The 2023 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS) will be taking place in Monterey, California on 15–18 October, and is the 6th year of the successful merger between the original Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) and the Compound Semiconductor IC Symposium (CSICS). BCICTS is the premier forum for the presentation and discussion of the latest developments in bipolar, BiCMOS, and compound semiconductor circuits, devices, and technology. Coverage includes all aspects of these technologies, including materials, device fabrication, device phenomena, TCAD modeling, compact modeling, integrated circuit design, testing, and system applications. A wide range of integrated circuit technologies are covered, including bipolar and field-effect transistors manufactured using materials such as SiGe, GaAs, GaN, InP, and SiC. The latest results in wireless, analog, RF, microwave, high-speed digital, mixed signal, optoelectronic, millimeter wave, and THz integrated circuits are embraced.

The conference itself will take place at the Monterey Marriott, near many interesting sites located in the city of Monterey, including the Monterey Bay Aquarium, which displays thousands of marine animals and plants in both underwater and interactive exhibits, and both Old Fisherman's Wharf and Cannery Row, with their converted landmark buildings housing popular dining, shopping, and entertainment options. The Monterey Peninsula where the city is situated boasts spectacular views of the Pacific coast and ocean, with numerous options for hiking and exploring, and is also home to the internationally renowned Pebble Beach golf course.

BIXBY CREEK BRIDGE

The Technical Program Committee for BCICTS cordially invites you to submit papers. **The submission deadline is 5 May 2023**. Submissions are encouraged in all areas of advanced circuits, devices, and modeling, with particular emphasis on:

- Bipolar/BiCMOS devices, circuits, and technologies
- 5G ICs, GaN HPAs/LNAs, InP THz PAs
- High-performance RF switch technologies
- GaN HEMT and other wide bandgap power devices
- Analog, RF, and microwave ICs
- mmW and THz ICs
- Process and device technology
- Modeling/simulation
- Optical CMOS/SiGe transceivers
- High-speed digital, mixed signal, and electro-optic ICs

Extended versions of selected papers from the symposium will be invited for publication in the September 2024 issue of the *IEEE Journal of Solid-State Circuits*. The BCICTS will also be offering short course, primer course, vendor exhibition, and plenary/invited talks given by internationally renowned experts in their field. For more details, please visit the BCICTS website at www.bcicts.org.

The BCICTS Committee members look forward to seeing you in-person at 2023 IEEE BCICTS in Monterey!

Munehiko Nagatani
BCICTS Publicity Chair
2023 IEEE BCICTS Organizing Committee

EDS Podcasts Available to Everyone!

Join us as we host interviews with some of the most successful members of our Society sharing their lives and careers. Their insight and wisdom inspire those in the engineering field. Stay tuned to our social media channels for new podcast releases.

Society News

Message from EDS Newsletter Editor-in-Chief

Daniel Tomaszewski
EDS Newsletter
Editor-in-Chief

Dear Readers, Members of the IEEE Electron Devices Society,

Welcome to the IEEE EDS Newsletter issue April 2023.

Several days ago, Joachim Burghartz shared with us the sad information that Prof. Dr. Adolf Goetzberger passed away. He was among the giants in the early stage of semiconductor device technology. Joachim kindly wrote Prof. Goetzberger's obituary.

At the beginning of this year, newly elected EDS officers and BoG members were elected. We congratulate them and wish them fruitful work for our Society.

Dear Readers, I would like to draw your attention to the article by Samar Saha about the history of EDS. It is the first out of three parts of the series which will be presented in subsequent Newsletter issues. I believe that it will be of great interest, especially to younger members of EDS.

We present the next two installments of the series celebrating the 75th Anniversary of Transistor. I kindly invite you to read interesting texts on the main stages of electron device compact modeling and on tunnel transistors. We are very grateful to Larry Nagel, Colin McAndrew, and Alan Seabaugh for these articles. I am also grateful to Manoj for inviting so many outstanding experts to contribute to the series.

The following articles from previous Newsletters will be published wholly or partially in the upcoming celebratory volume, *75th Anniversary of the Transistor*, Eds. Arokia Nathan, Samar Saha, Ravi Todi, IEEE Press-Wiley, 2023:

- Hiroshi Iwai *Invention of the Transistor 75 Years Ago; The Origin of Device Miniaturization Towards Super-Intelligent Society* (issue April 2022)
- B. Jayant Baliga *History and Emerging Designs of Power Transistors* (issue July 2022)
- Chenming Hu *Transistors at 75—Past, Present, and Future* (issue July 2022)
- Dan Fleetwood *Moore's Law Scaling and Radiation Effects in MOS Devices* (issue October 2022)
- John D. Cressler *The Silicon-Germanium Heterojunction Bipolar Transistor* (issue October 2022)
- Yuan Taur *From Invention of the Transistor to VLSI to Ubiquitous Computing* (issue Jan 2023).

In the Technical Briefs section, we present one article by Prof. Steve Chung, concerning the reliability of modern dielectric layers.

We announce three very important conferences sponsored by the Society that will be held this year: the 2023 IEEE Symposium on VLSI Technology and Circuits, the 2023 IEEE International Memory Workshop, and the 2023 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology. Please, find their links to the websites with full information about these events. We are looking forward to interesting reports from them in future Newsletters.

Dear Readers, I would like to draw your attention to the broad report on the 5th IBM IEEE CAS/EDS AI Compute Symposium (AICS'22). The material is presented in Regional News. The Symposium initiated and co-chaired by Dr. Rajiv Joshi gains an increasing audience. Thanks a lot, Rajiv for providing us with summaries of subsequent editions of AICS. The WiEDS section contains also the material concerning the YPs section. It is a summary of the *Women in Semiconductor* Panel Session and *Young Professionals* Meet at ICEE2022, Bangalore India. The Regional News includes rich material from a number of chapters worldwide. Does it show an increasing activity in the chapters? May it happen. I am aware that our Regional Editors contribute to that as well by actively reaching out to the chapters. Thank you very much.

Finally, I would like to remind you that the first issue of the new publication, *Electron Devices Magazine* is approaching. We are looking forward to it and wish the ED-M Editorial Team chaired by Joachim Burghartz a lot of submissions, interesting content, and business success. Please, go to https://eds.ieee.org/publications/ieee-electron-devices-magazine for further details.

Dear Readers, if you have any suggestions, or comments regarding the Newsletter contents, please do not hesitate to contact us. We will be very glad to receive your feedback. Interesting views will be presented with the consent of the authors, along with our replies in the Letters to Editors section.

Sincerely,

Daniel Tomaszewski

Announcement of Newly Elected BoG Members

Cary Yang
2022 EDS Nominations and Elections Chair

The IEEE Electron Devices Society (EDS) Officers and Board of Governors (BoG) members-at-large election was held in December 2022 via email. I am pleased to present the results of this election and short biographical information of the incoming team that will lead EDS in the years to come.

BOG Members-at-Large

A total of seven members were elected for a three-year term (2023–2025). Five of the seven electees are serving a second term, while the other two have joined the board for the first time. The backgrounds of the electees span a wide range of professional and technical interests. The following are the results of the election and brief biographies of the individuals elected.

Constantin Bulucea

Constantin Bulucea received his MS (1962) and Ph.D. (1974) degrees in EE from the Polytechnic Institute of Bucharest. In 1969, he won a one-year government scholarship for graduate studies at UC Berkeley, where he got his second MS degree. Between 1970 and 1986, he led Romania's Research Institute for Electronic Components, ICCE. In 1978, following the model of IEDM, he founded the Annual Conference for Semiconductors, now an international IEEE event. In the US, Dr. Bulucea developed the first rugged MOS trench power transistors of the industry (Siliconix) and several high-performance mixed-signal VLSI processes (NSC and TI). His inventions are protected by 69 US patents. Dr. Bulucea has been an editor of SSE (1978–2012), IEEE EDL (1995–2012), and IEEE J-EDS (2013 -). He is an Honorary Member of the Romanian Academy and an IEEE Life Fellow. In 2018 and 2019 he was on the IEEE/EDS Fellow Evaluation Committee.

Daniel Camacho

Daniel Camacho is an electrical engineer with over a decade of professional experience. Daniel first received his bachelor's degree from Pontificia Universidad Javeriana in Bogota, Colombia in September 2007 and went to receive his master's degree from Southern Methodist University in Dallas, Texas in 2009.

He joined Intel corporation in 2010 and has been working there since then. Daniel has focused his career in the design of analog, mixed-signal and custom digital circuits for high performance applications on advanced fabrication nodes. His work includes but is not limited to Phase-locked Loops, voltage regulators, and Oscillators.

John Dallesasse

John Dallesasse is a Professor of Electrical and Computer Engineering and Associate Dean in the Grainger College of Engineering at the University of Illinois at Urbana-Champaign and has over 20 years of industry experience in technology development and executive management. Prior to joining UIUC he was the Chief Technology Officer and co-founder of Skorpios Technologies developing innovative methods for heterogeneous integration of compound semiconductors with silicon. His technical contributions include, with Nick Holonyak, Jr., the discovery of III-V Oxidation, which has become an enabling process technology for the fabrication of Vertical-Cavity Surface-Emitting Lasers (VCSELs) for optical networking, 3D imaging (mobile phones), and LIDAR applications. John has over 100 publications and conference presentations and 51 issued patents. He serves as the Chair of the Steering Committee for the IEEE Journal of Lightwave Technology and is the Vice President of Technical Committees for IEEE-EDS. He is a Fellow of the IEEE and Optica.

Mario Lanza

Mario Lanza got a PhD in Electronic Engineering (with honors) in 2010 at Universitat Autonoma de Barcelona. In 2010–2011 he was NSFC postdoc at Peking University, and in 2012–2013 he was Marie Curie postdoc at Stanford University. In October 2013 he joined Soochow University as Associate Professor, and in March 2017 he was promoted to Full Professor. Since October 2020 he is an Associate Professor of Materials Science and Engineering at the King Abdullah University of Science and Technology (KAUST), in Saudi Arabia. Prof. Lanza has published over 185 research papers, including 1 Nature, 2 Science, 5 Nature Electronics and multiple IEDM (among others), and has registered four patents (one of them granted with 1 million USD). He is a Distinguished Lecturer of the IEEE Electron Devices Society, and serves on the board of many other journals and conferences, including IEEE IEDM and IEEE IRPS. He works on 2D materials based electronics.

Lluís F. Marsal is a Distinguished Professor at the Department of Electronic Engineering of the Universitat Rovira

Lluís F. Marsal

i Virgili, Spain and was a postdoctoral researcher at the Department of Electrical and Computer Engineering, University of Waterloo, Ontario, Canada.

He received the ICREA Academia Award 2014 and 2021 and has served on the Technical Activities and the Publication Services at conferences sponsored by EDS and as Guest Editor for the IEEE J-EDS. He is the chair of the EDS Spain Chapter and a R8 SRC vice-chair. He is also a senior member of the IEEE and a member of the EDS Distinguished Lecturer program. He has co-authored over 240 research papers, two books, five book chapters and holds four patents. He supervised/co-supervised 20 PhD students and mentored of 10 postdocs. His interests include organic solar cells and hybrid nanostructured materials for optoelectronics and detection platforms.

NG Geok Ing

NG Geok Ing is a Professor at the Nanyang Technological University Singapore, School of EEE. Currently, he holds joint appointment with the A*STAR Institute of Microelectronics serving as the Centre Director of the National GaN Technology Centre. He is also the Programme Director of the Centre for Microsystem Technologies at the Temasek Laboratories@NTU and the Director of the Centre for Micro- and NanoElectronics in the School of EEE. His current research specializations in III-V compound semiconductor devices for high-frequency and Monolithic Microwave Integrated Circuit applications. He has authored and co-authored more than 300 international journal and conference papers and delivered plenary and invited talks at several international conferences. Currently, he serves as the member of the IEEE EDS Board of Governors, Editor of the IEEE JEDS and member of the Steering Committee of the Electron Devices Technology and Manufacturing.

Mayank Shrivastava

Mayank Shrivastava is a faculty member at the Indian Institute of Science, and co-founder of AGNIT Semiconductors. He worked for Intel, IBM and Infineon. He is also instrumental in setting up a $40-million worth GaN prototyping Fab and leading a national effort on 2D Fab and Innovation hub. He is an Editor of the IEEE T-ED, IEEE EDS Distinguished Lecturer and an elected member of the IEEE EDS BoG. He received the prestigious TR35 award (2010), IEEE EDS Early Career Award (2015), DST Swarnjayanti Fellowship (2021), Abdul Kalam Technology Innovation National Fellowship (2021), and the VASVIK award (2021). Besides, he has received over a dozen other national awards and honors of highest repute. His work has resulted in over 200 peer-reviewed publications (majority are in IRPS, IEDM and T-ED) and 47 patents. Most of these patents are either licensed by semiconductor companies or are in use in their products.

Cary Yang
2022 EDS Nominations and Elections Chair

Be Wary of Email SCAMS Targeting IEEE Members

IEEE members and staff should continue to remain alert to the risk of fraudulent emails and to maintain continued vigilance online. Fraudulent email messages have used spoofed addresses to pose as someone known to the recipient and often contain personal details about IEEE members drawn from non-IEEE online sources and from social media sites accessible by search engines. These emails attempt to commit financial fraud by exploiting the professionalism and camaraderie among IEEE members. These fraudulent messages often include a request for urgent assistance and will ask the recipient to transfer funds or goods to a third party.

For more information visit this IEEE webpage, https://mga.ieee.org/news/21-action-items-deadlines/245-cyber-alert-be-aware-and-protect-ieee-from-business-emails-scams

A Brief History of the IEEE Electron Devices Society: Part I

Samar K Saha
Prospicient Devices, Milpitas, CA 95305, USA

As we celebrate the 75th anniversary of the invention of the *Transistor*, we reflect the history of the *Electron Devices Society* (EDS) of the *Institute of Electrical and Electronics Engineers* (IEEE) over the last seven decades.

Since the invention of the *Transistor* [1]–[4], solid-state electronics has made a profound impact on humanity. This unprecedented progress in solid-state device technology over the past seven decades is the result of pioneering contributions and dedicated efforts of the people of the electrical and electronics engineering, specifically electron devices community. The EDS [5] is such a community of the professional association, the IEEE [6]. Currently, in the hierarchy of IEEE, the EDS is one of the 39 technical societies and seven technical councils under the IEEE Technical Activities Board (TAB) [7]. The growth of EDS over the last seven decades is inherently related to the evolution of transistor and transistor manufacturing technology for very large scale integrated (VLSI) circuits and systems enabling the digital ecosystem. Thus, *the history of the IEEE EDS is the story of the global engineering and academic community dedicated to advancing electron and ion devices related to technology for the benefit of humanity*. In this article, we reflect the origins of EDS and its growth becoming a true volunteer-led volunteer-driven global professional organization along with its diverse portfolio of publications as well as meetings and conferences on topics of interest to its technical community. Furthermore, the article also describes the strategic initiatives including educational programs and recognition of its members and luminaries of the electron devices community.

I. Origins of EDS

The origins of the IEEE EDS lie in the year 1952 as a committee of the then professional association, the *Institute of Radio Engineers* (IRE), established in the year 1912 [8]–[11]. However, the *Electron Devices Society* can trace its origins back to the 1930s, when the IRE *Technical Committee on Electronics* used to coordinate Institute's technical activities in the field of electronics; e.g., first three conferences on Electron Tubes starting in 1938 were held under auspices of the *IRE Committee on Electronics* [8]–[11]. In the meanwhile, with the increasing demands for electrical engineering professionals and the solid-state electronics in the 1940s, there had been a huge growth of IRE membership [8]–[11]. In order to address this growth, the IRE committee on electronics coordinating activities on Electron Tubes was extended in 1949 to include *Solid-State Electron Devices*, and renamed the entity to *IRE Committee on Electron Tubes and Solid-State Devices*, often referred to as the "Committee 7" [5], [11]. The committee's first Chairman was Leon S. Nergaard of *Radio Corporation of America* (RCA), who served in that position until 1951 [8]–[11].

Note that the IRE "Committee 7" formed the IRE Professional Group on Electron Devices which would become the IEEE Electron Devices Society in ensuing decades through merger, subsuming different technical functionalities, and name changes (Figure 1) as described below.

IRE Professional Group on Electron Devices: After the invention of the *Transistor* at Bell Telephone Laboratories by John Bardeen and Walter Brattain in December 1947 [1], [2] and William Shockley in January 1948 [3], [4], the solid-state electron devices were beginning to attract major attention. Thus, in order to interact more directly with the rapidly changing electron devices technical community, the IRE "Committee 7" proposed to form a new group under the IRE's Professional Group system in the year 1951 [8]–[11]. By the end of 1951, the proposal was approved by the *IRE Executive Committee* (ExCom). And, on March 5, 1952, the *IRE Professional Group on Electron Devices* (PGED) was established. The *Administrative Committee* (AdCom) of the PGED held its first meeting on March 5, 1952 at IRE headquarters in New York City [11]. The first AdCom volunteers included George D. O'Neill of *Sylvania* as the first Chairman, Leon Nergaard as the founding Vice Chairman, and John Saby of *General Electric* (GE) as the first Secretary [11]. During its formative years, the new IRE PGED was led by highly experienced volunteer leaders. *Thus, on March 5, 1952, the antecedent of the IEEE Electron Devices Society was launched*.

The IRE PGED became the IEEE Professional Technical Group on Electron Devices after the amalgamation of the IRE and American Institute of Electrical Engineers (AIEE) in 1963 to become the IEEE [8], [12].

IEEE Professional Technical Group on Electron Devices: In 1940s, the dynamic growth of radio technology and the emergence of the new discipline of electronics led to stiff competition between the IRE and AIEE [8]–[12], though the AIEE had been the standards of excellence for electrical engineering (EE) professionals longer than the then rival association IRE. The AIEE was founded in 1884 by some of the most prominent inventors and innovators in the then new field of EE including *Nikola Tesla*, *Thomas Alva*

Edison, *Elihu Thomson*, *Edwin J. Houston*, and *Edward Weston* [9]–[12]. In the early 1960s, the IRE and AIEE recognized that their constituencies had been increasingly overlapped with needless duplication of staff, publications, and activities [8]–[12]. Thus, on January 1, 1963, the two institutes formally became one, *the Institute of Electrical and Electronic Engineers* or simply referred to by the letters "I.E.E.E. (pronounced I-triple-E)," in the year after the IRE celebrated its 50th (and the last) anniversary [9]–[13]. Both of these sweeping changes have fundamentally altered the practice of EE in the *United States of America* and throughout the world. On the very same day (January 1, 1963), the IRE PGED became the *IEEE Professional Technical Group on Electron Devices* (PTGED) [5], [11].

After the formation of the IEEE, the duplicate functionalities and committees of the IRE and AIEE related to electron devices were consolidated to form the IEEE Electron Devices Group.

IEEE Electron Devices Group: The IEEE PTGED merged with the *Solid-State Devices Committee* on July 1, 1963 and subsumed the functionalities of the AIEE's technical committees on *Electron Devices* and *New Energy Sources* on May 20, 1964, and was renamed the *IEEE Electron Devices Group* (EDG). On June 23, 1965, the original *IRE Tubes Standards Committee* and *Solid-State Standards Committee* also fell under the new *IEEE Electron Devices Group* [5], [11] which after a decade, became today's *IEEE Electron Devices Society* [5].

IEEE Electron Devices Society: In 1975, the IEEE EDG AdCom petitioned the IEEE TAB to ordain it as a *full-fledged Society* describing its maturity and increasing stability as an entity of the IEEE [11]. Under the Institute's general practices, such a designation indicates that a Group's financial resources are deemed strong enough to survive on its own as a completely independent organization. The petition cited the group's *field-of-interest* (FoI) as "*electron and*

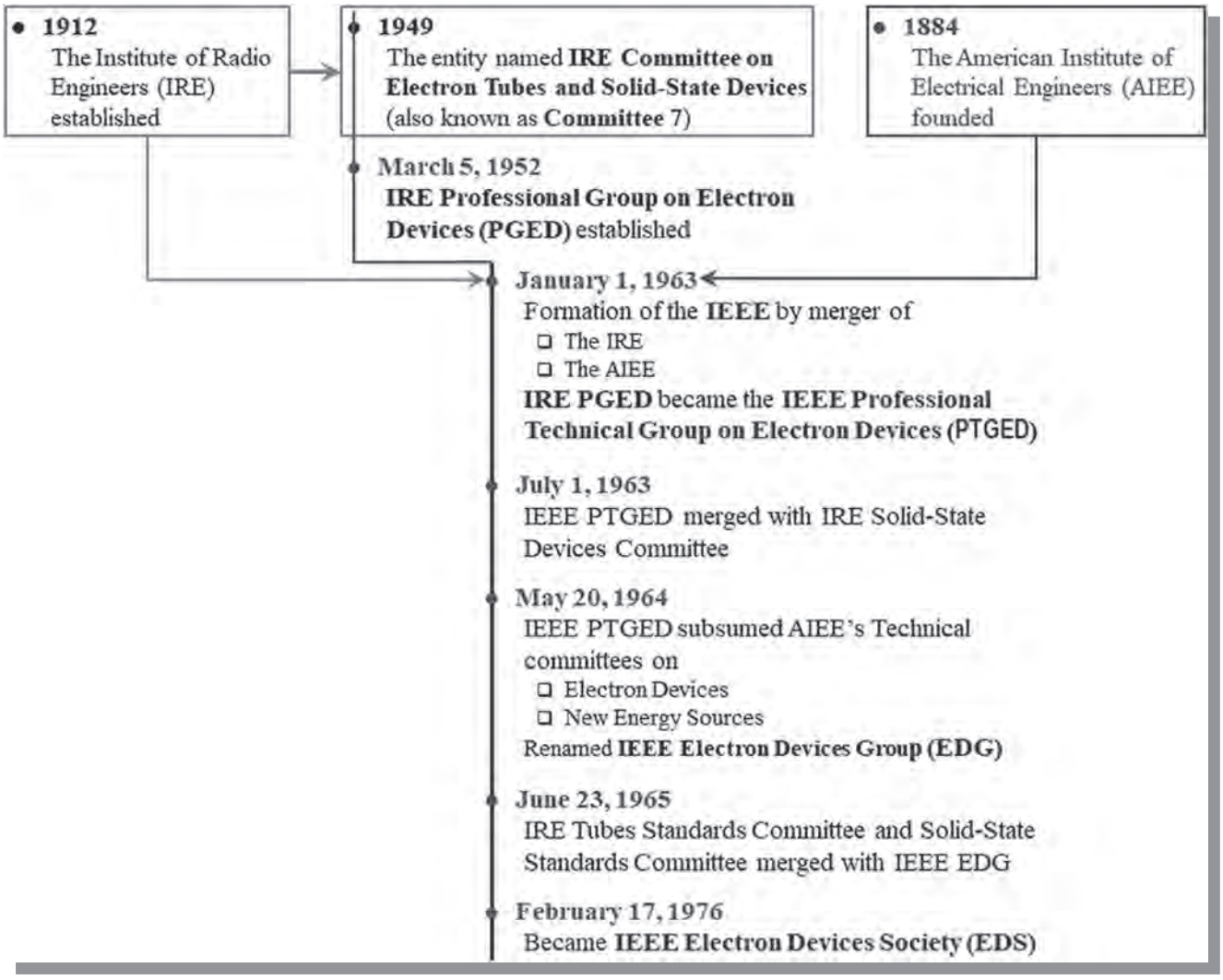

Figure 1. Origins of the IEEE EDS lie on March 5, 1952 as the IRE PGED. And, through mergers, subsuming different functionalities, and name changes in ensuing decades IRE PGED became the IEEE EDS on February 17, 1976.

ion devices including electron tubes, solid-state and quantum devices, energy sources, and other devices which are related to technology." The request was quickly granted. And, on February 17, 1976, the EDG formally became the *IEEE Electron Devices Society*, commonly referred to as the *EDS* [5], [11].

As shown in Figure 1, on March 5, 1952 the IRE PGED was established to interact directly to *electron devices community* and therefore, the origins of the IEEE EDS lie on March 5, 1952 as the *IRE Professional Group on Electron Devices*; which on January 1, 1963 became the *IEEE Professional Technical Group on Electron Devices*; on May 20, 1964 was renamed the *IEEE Electron Devices Group*; and on February 17, 1976 became the *IEEE Electron Devices Society*, EDS.

Throughout the twentieth century (*second millennium*) *to date in the third millennium, the Society has grown to be one of the world's largest associations of electron devices professionals with about 10,000 members in over 160 countries worldwide.*

II. Growth of EDS

After the establishment of the *IEEE Professional Technical Group on Electron Devices*, PTGED on January 1, 1963, the Group's major efforts had been consolidation of its technical activities, membership drive, and formation of chapters in the *United States* (US) *of America and beyond its borders* as well as globalization, sponsor meetings and conferences, launch new journals and a newsletter, and so on as described below.

Consolidation of Technical Activities: The responsibility for consolidating all professional activities of the merged IRE and AIEE groups under the new IEEE PTGED was primarily on Ray Sears of Bell Com, AdCom Chairman from July 1963 to June 1964 and Earl Thomas, Chairman from July 1964 to June 1966 [11]. Thomas setup the new merged organization and its procedures to ensure that the major technical activities previously carried on by the groups and committees being merged are not lost. By the time Thomas stepped down in June 1966, the IEEE EDG activities had been reorganized into *five* associated sub-fields: (1) *Electron Tubes*; (2) *Solid-State Devices*; (3) *Energy Source Devices*; (4) *Integrated Electronics*; and (5) *Quantum Electronics* each under its own technical committee (TC) [11]. Note that the EDS TCs have grown in ensuing decades to diversify its technical activities within the emerging EDS FoI counting 16 at the end of the year 2022 [5].

Membership Drive: The membership drive started as early as in the 1950s by the IRE PGED. Through Group's concentrated efforts to form local chapters around the US, there were active chapters in Boston, Los Angeles, New York City, Philadelphia, San Francisco, and Washington, D.C. as well as lightly active groups in other areas of the country [11]. By December 1953, paid membership in the full IRE PGED exceeded 1,000 engineers and scientists [11]. The Group continued its steady growth, and by December 1959, its membership exceeded 5,000 including students [11]. In the early 1970s, the total (IEEE EDG) membership grown over 9,300 including 32 percent student members and another 16 percent from overseas [11]. Consequently, the EDG was among the largest of the IEEE's professional groups. And, the growth and alignment of the Group continued under the IEEE.

Along with the growth of technical activities within the US, the Group concentrated its efforts to expand its presence beyond the US borders.

Electron Devices Group Beyond US Boarders: During the 1970s, the IEEE EDG expanded its activities beyond US borders. These expansion efforts had actually begun back in the mid-1960s, when the IRE PGED's annual *Fall Washington* D.C. *Meeting* was renamed the *International Electron Devices Meeting* (IEDM) in 1965 [14]. During the late 1960s, non-US membership grown from less than 1,000 to just over 1,500, representing about 16 % of the total membership [11]. The largest foreign contingents were in Canada, Europe, and Japan; the Tokyo Section alone recorded nearly 300 members in 1969. European members took increasing part in the activities of the IEEE EDG, occasionally, cosponsoring meetings such as the *European Microwave Conference* and the *Symposium on Solid-State Device Technology*. There were also frequent exchanges of information with the *Japan Society of Applied Physics*. And in 1972, the annual *Device Research Conference* was held for the first time beyond the US borders at the University of Alberta in Edmonton, Canada [11].

In the mid-1970s, the IEEE EDG experienced membership decline and IEEE EDS membership dropped below 7,000 in 1978 [11]. This decline was partly due to the loss of members by reorganization of the EDS's *Quantum Electronics Council* as a separate *IEEE Group on Quantum Electronics and Applications* in 1977. However, renewed effort to membership drive brought the total number back above 8,000 by the end of the 1970s including over 25 % beyond US borders [11]. At the end of 1970s, the Society became financially healthy posting over $300,000 cash reserves in the bank along with membership growth [11].

In the continued efforts to grow EDS beyond US borders, AdCom began to include Japanese representatives on its roster of elected members during the 1980s. In 1984, for the first time Asian member Takuo Sugano was elected to serve at AdCom followed by Yoshiyuki Takeishi in 1987 [11]. Previously, there had been *two* European members, Adolf Goetzberger and Cyril Hilsum on the committee. Thus, electing Japanese members, the IEEE EDS AdCom became a truly worldwide committee. Besides, the Society's policy to reimburse travel expenses of AdCom members, non-US members have been a regular

and continuing feature of today's EDS AdCom (renamed *BoG* in 2013) [5], [11].

AdCom's efforts for growth and diversification of Society's activities continued to establish EDS as a true global organization.

Managing Growth and Diversification: In the late 1980s, the growth and diversification of EDS technical activities within the US and overseas continued. During the year 1987, the EDS membership grew over 10,000 and had an annual budget exceeding a million US dollars [5], [11]. It published *two* professional journals of its own and cosponsored *four* others. Furthermore, EDS sponsored almost 20 conferences a year and cosponsored with other societies nearly as many more. Thus, the Society's operations had become too complex and far-reaching for an all-volunteer organization. Therefore, during the year 1987, discussions began on the need to hire permanent professional staff to manage the day-to-day operations of the Society [5], [11]. However, such a major financial commitment was constrained mainly due to the expenses of new publications.

In the late 1980s, the EDS financial position improved under the new Treasurer (1988–1991), *Lu A. Kasprzak* of IBM, with annual surpluses often coming in well above $100,000 and reserves exceeding $1.5 million [5], [11]. The total paid membership, including students, was up to more than 11,000. Thus, with finances in much better condition, AdCom seriously considered the question of hiring professional staff. Therefore, the day before its June 1989 meeting, EDS President *Craig Casey* of Duke University, Meeting Committee chair *Michael S. Adler* of General Electric, Treasurer *Kasprzak*, and several past presidents met to discuss this issue. They concluded that such management was indeed required and that the Society's financial position is favorable. The needed office space was available at the new *IEEE Operations Center in Piscataway, New Jersey*. Subsequently, in October 1989, Adler, Casey, Kasprzak, *Friedolf M. Smits* (past Treasurer, 1980–1987), and the incoming EDS President *Lewis Terman* of IBM, decided to recommend the creation of the new, full-time position of EDS *Executive Officer* [5], [11]. And, in December 1990 meeting, AdCom unanimously endorsed their recommendation *to having Society's sprawling activities managed by an Executive Office with full-time staff of salaried personnel*.

EDS Executive Office Established: Upon approval to create a full-time position of *EDS Executive Office* by AdCom, the EDS leadership set out to hire an *Executive Director* [5], [11]. The search committee including Casey, Smits, and Terman interviewed candidates that summer and offered the position to *William (Bill) F. Van Der Vort*, the then Manager of the *Systems Department* at IEEE who had been working at IEEE since 1977. Accepting this offer, Bill started as the *EDS Executive Director* in August 1990 and retired in the year 2009. He led a growing team at the Society's Executive Office in Piscataway, New Jersey to manage the Society's business and finances, coordinate its myriad meetings, and support the editing and publishing of its *Newsletter* and professional *Journals*. After Bill's retirement, Christopher Jannuzzi was hired as the EDS Executive Director in 2010 who served in full capacity through 2015 and parttime in the same position as the supervisor of the EDS Executive office Operations Director, James Skowrenski, during 2016–2019. Since 2020, the EDS Executive office is managed by Operations Manager, Ms. Laura Riello, who has been working at IEEE since 1987 [5].

Upon establishing the EDS Executive office in August 1990, the renewed efforts to globalization of EDS started with increasing technical activities within the EDS FoI.

Globalization of EDS: The efforts to globalization of EDS began during the 1980s adding AdCom members from Asia and Europe. In the 1990s, one of the major initiatives was to complete the globalization efforts to c*onvert the Society into a truly international organization* [5], [11]. In this endeavor, *Roger Van Overstraeten* of Belgium was elected to AdCom, its first European member in more than a decade [5], [11]. Shortly after, it became the standard EDS policy (*EDS Constitution & Bylaws*) to have *at least two elected AdCom* members from IEEE Region-8 (Africa, Europe, and Middle East) and another *two* from IEEE Region-10 (Asia and Pacific) [5]. By implementing this policy, AdCom's total membership grew from 18 to 22, the first of several increases in the 1990s and continues to-date in the early 2023. In order to make Society's growing activities more effective, an *EDS Executive Committee* (ExCom) was established consisting of the *Elected Officers*, *Junior and Senior Past Presidents*, *Chairs* (re-named as the Vice-Presidents (VPs) from the mid-2004) of key committees, and the *Executive Director* [5], [15].

During the 1990s, the Society's efforts to globalization had been a top priority. Under the leadership of EDS Presidents Terman (1990–1991) and Michael Adler (1992–1993), new chapters were established in Australia, Canada, China, Egypt, France, and Germany as well as in other countries [5], [11]. In order to sustain this rapid global expansion, the Society created a new *Regions/Chapters Committee* (SRC) appointing *Cary Yang* of Santa Clara University as the first Chairman. ExCom members occasionally visited these chapters and regions to help foster better communications and membership services [16]. And, the Society started the *Distinguished Lecturer* (DL) *Program* to present leading-edge and exciting technical research by quality lecturers to EDS chapters and members as well as facilitate communications among members, chapters, EDS, and IEEE [16]. In the ensuing decades, the DL program is extended to providing single or multiple DLs by a single or multiple lecturers in a Session and referred to as the "EDS Distinguished Lecturer/

Mini-Colloquia (DL-MQ) Program" [5]. By the time Adler stepped down in 1993, there were 59 EDS chapters in all, with 26 *of them located beyond US* borders; by the end of 1996, more than half of the chapters, 48 out of 85, were outside the US. The new EDS logo, *sporting a lone electron, represented by a spin vector, circling the globe*, was redesigned by Terman in 1992, reflects the Society's broad international character [5], [11]. Thus, at the closing of 1990s, the IEEE EDS, as the true global association for the electron devices community, found itself in an enviable intellectual and financial position. The total number of 99 EDS chapters spread widely across the globe and the total membership exceeded 13,000 including more than 5,000 outside the US [5], [11].

In the third millennium, the Society's global activities continue to grow. At the end of 2022, the EDS chapter grew to 240 including 88 joint chapters and 97 student branch chapters spread across the world with a total number of EDS membership of 10,769 [5]. Note that 37.7 % of total members are from IEEE Region-10 [5]. The declining EDS membership is partially due to the increasing number of students and young professionals seeking careers in the growing wireless networking communications technologies.

In the new millennium, the EDS leadership implemented new initiatives on educational as well as humanitarian activities to better serve the electron devices community.

Educational Initiatives of EDS: The Society continues to launch new strategic initiatives to enhance the value of EDS membership and chapters worldwide including student fellowship, encourage high school students to *Science, Technology, Engineering, and Mathematics* (STEM) education, and humanitarian activities. The EDS has been playing an active role in encouraging younger students to pursue careers in EE. In this effort, the EDS-ETC (*Engineers Demonstrating Science—Engineer Teacher Connection*) program was developed by Mid-Hudson region EDS chapter, New York, USA in the year 2010 through the leadership of Fernando Guarin of IBM, East Fishkill, New York. The EDS-ETC program is a highly successful and sought out program by EDS chapters worldwide [5].

To continue educational initiatives, in the year 2011, the EDS (2010–2011) President Renuka P. Jindal of the University of Louisiana at Lafayette, Louisiana, launched the EDS *webinar series* to deliver live lectures by luminaries within the EDS FoI [5], [17]. The first webinar entitled, "The FinFET 3D Transistor and the Concept Behind It," was offered by Chenming Hu of the University of California, Berkeley on July 27, 2011. The live webinar has been one of the valuable strategic initiatives of EDS. Furthermore, the online repository provides EDS members with on-demand access to streaming videos of the past events [5], [17].

With increasing efforts to globalization and diversification of Society's activities, it became important to rename the Society's governing body to appropriately represent its true Mission.

AdCom Renamed as the BoG: At the June 2012 AdCom meeting in Leuven, Belgium, Renuka motioned to renaming AdCom as the *Board of Governors* to more accurately reflect the volunteer-led volunteer-driven spirit of the Society. The EDS AdCom unanimously voted in favor of the Motion [18]. Subsequently, the change was approved by IEEE TAB. Thus, *from 2013 January, the EDS AdCom became the EDS Board of Governors or BoG*. All roles and functions of the BoG remain the same as the AdCom. However, the "BoG" represents the true governing body of the Society to carry out its envisioned Mission [5].

In order to financially support the growing educational and humanitarian initiatives, the Society moved forward to establish an EDS Mission Fund.

EDS Mission Fund: In the year 2013, under the leadership of President Paul Yu of the University of California, San Diego, the EDS partnered with the IEEE Foundation to establish the *IEEE EDS Mission Fund* of the I*EEE Foundation* [5], [19]. The fund is aimed to greatly enhance the *humanitarian*, *educational*, and *research initiatives* within the EDS FoI by providing members and other constituents of the EDS community with the ability to contribute directly to our mission-driven imperatives, such as the *EDS-ETC* and *EDS Student Fellowship* programs.

EDS Center of Excellence: Another educational program to engage high school students including under-represented girl students in STEM education, an *EDS Center of Excellence* was established at the Heritage Institute of Technology, Kolkata, India in 2017 through the effort of (2016–2017) President Samar Saha of Prospicient Devices, Milpitas, California [20]. This is the first of its kind educational program in EDS and IEEE and is aimed to encourage high school and undergraduate boy and girl students in EE and specifically device engineering, and choose device engineering as their professional career.

With continued changes in the electron devices technical area, the EDS leadership created a dedicated Future Directions Committee to move forward EDS in the future.

Future Directions: Since the formative years, the Society continuously diversified its technical activities in emerging areas to strategically position the Society at par with the changing technical fields. However, with the rapidly changing device technology, it has become crucial to have a formal future directions strategy to move forward EDS in the future device technology areas. In this effort, Samar initiated the EDS first five-year strategic planning with his goal to *build EDS on the foundation of the past to meet the challenges of the future* [20]. In continuation, (2018–2019) President Fernando appointed an ad hoc committee with Samar as the Chairman to continue strategic planning. In order to concentrate efforts on EDS future directions, Meyya Meyyappan, President (2020) of *National Aeronautics and Space Administration* (NASA) created

a Standing *Strategic Directions Committee* in 2020 with Paul Berger of Ohio State University as the Vice President. In 2022, Paul was replaced by Douglas P. Verret as the Vice President of the Future Directions Committee [5].

EDS Podcast: Similar to EDS webinar, the Society under the leadership of Meyya, launched EDS Podcast Series in 2020 to host interviews with some of the most successful members of EDS sharing their lives and careers to inspire students and young professionals. The first podcast was aired on January 15, 2021 with Muhammad Mustafa Hussain of the University of California, Berkeley (now Purdue University, West Lafayette, Indiana) as the host [5].

III. Conclusion

The *Electron Devices Society*, EDS is a volunteer-led volunteer-driven global association of electron devices community of the *Institute of Electrical and Electronics Engineers*. The Society has grown worldwide over the past seven decades and continues to promote excellence in the field of electron devices for the benefit of humanity. *The Society's growth has been culminated by a growing portfolio of top-tiered professional journals and conferences on emerging topical areas which will be presented in the July 2023 Issue of this EDS Newsletter*.

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In Memoriam Prof. Dr. Adolf Goetzberger

The solar pioneer and founder of the Fraunhofer Institute for Solar Energy Systems ISE, Prof. Adolf Goetzberger, passed away on February 24, 2023 at the age of 94. In 1981, as the then director of the Fraunhofer Institute for Applied Solid State Physics IAF, Goetzberger pushed through to spin off a working group and form an independent institute devoted to solar energy systems. Thus, the Fraunhofer Institute for Solar Energy Systems ISE was founded. In the same year, the physicist developed, among other things, the idea of agrivoltaics, the dual harvesting of crops and energy, which is now experiencing its breakthrough in Germany. He contributed his visionary work to numerous expert committees, boards of trustees, commissions and working groups and was honored with many renowned prizes and awards.

Figure 1. Solar pioneer and founder of Fraunhofer ISE, Prof. Adolf Goetzberger, passed away on February 24, 2023 at the age of 94. © Fraunhofer ISE.

Figure 2. Adolf Goetzberger founded the Fraunhofer Institute for Solar Energy Systems ISE in 1981 and headed the institute in Freiburg until his retirement in 1993. © Fraunhofer ISE.

After studying experimental physics, Adolf Goetzberger received his doctorate in 1955 from the University of Munich for his work on the crystallization of vapor-deposited antimony layers. He then moved to the USA to work with William Shockley, Nobel Prize winner and co-inventor of the transistor, later moving to the famous Bell Laboratory in Murray Hill, New Jersey. In 1968, he returned to Germany and became director of the Fraunhofer Institute for Applied Solid State Physics IAF. In 1971, he was appointed honorary professor at the Faculty of Physics by the University of Freiburg and in this capacity supervised numerous diploma and doctoral theses.

In 1983, Adolf Goetzberger was the first German to receive the J. J. Ebers Award from the American IEEE Electron Devices Society for the development of the silicon field-effect transistor.

In the upcoming inaugural issue of the *IEEE Electron Devices Magazine* (ED-M), an article describing Adolf Goetzberger time with William Shockley will be published, authored by myself.

Joachim N. Burghartz

Letter to the Editor

Dear Dr. Tomaszewski,

When I received the January newsletter issue, I sensed a change I could not identify precisely until reading your editorial: the new two-column format! Good choice of a difference; congratulations! Also, congratulations on your succinct yet comprehensive summaries in all issues of this Newsletter.

You asked for comments and suggestions regarding the Newsletter. Currently, I have only one.

In this issue, the similar-sounding names of William Shockley and Walter Schottky were somehow cross-linked while writing or editing the cover-featured article, resulting in the regrettable "Walter Shockley" mistake.

I would also like to add the following for the benefit of young readers who, having powerful TCAD tools at their fingertips, may have only read or heard about Shockley from best-seller writings on his personality.

The "one-month work" on the invention and physics of the bipolar junction transistor resulted in a 55-page article entitled "The Theory of p-n Junctions in Semiconductors and p-n Junction Transistors" published in the 1949 volume of the Bell

System Technical Journal. That article has been the single most referenced paper in the semiconductor literature for several decades. With subsequent generalizations and extensions by others, including Shockley himself, along the same line of physical modeling, it established the engineering of transistor design that was used until the numerical device simulators became commercially available about 20 years later. It is still used in textbooks and the first-order design of p-n junction diodes and bipolar junction transistors. The simulators confirmed the genius of Shockley's intuition in introducing simplification assumptions that have made possible the formulation of a transistor theory in terms of elementary math functions.

Please take my comments as written with the best intention to improve our society's Newsletter.

Sincerely,
Constantin Bulucea
(Texas Instruments, Retired)

Dear Dr. Constantin Bulucea,

Thanks a lot for your very kind e-mail and constructive comments.

Firstly, I apologize to Prof. Sandip Tiwari and the Readers for a serious mistake in the name of William Shockley (Walter Shockley was used) that appeared in the article by Prof. Tiwari. It should not have happened.

Dr. Bulucea, I would like to thank you for your comment concerning the seminal contributions of William Shockley and his key role in the unprecedented flourishing of an engineering branch. I believe that a more detailed presentation of the microelectronics beginnings seen from perspective of a senior expert would be of interest to young researchers and engineers.

I am glad that you have accepted the change in the layout of the Newsletter. In our opinion, the two-column layout gives more flexibility in arrangement of the Newsletter contents. It was the main reason for this change. I am grateful to the EDS Newsletter Oversight Committee for approving our request.

Sincerely,
Daniel Tomaszewski
EDS Newsletter EiC

Awards and Calls for Nominations

2023 IEEE EDS Robert Bosch Micro and Nano Electro Mechanical Systems Award Winner

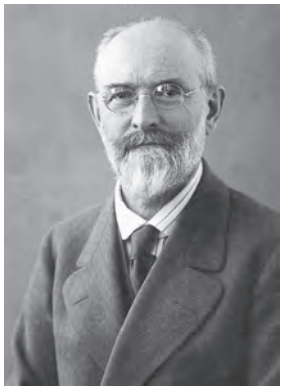
The 2023 IEEE EDS Robert Bosch Micro and Nano Electro Mechanical Systems Award was awarded to Stephen C. Terry, James B. Angell (late) and John H. Jerman. The award was presented to John H. Jerman at the 2023 IEEE MEMS Conference, January, 2023. This prestigious award recognizes and honors advances in the invention, design, and/or fabrication of micro- or nano-electromechanical systems and/or devices.

Osamu Tabata
EDS Bosch Award Chair

John H. Jerman with EDS Past President, Cor Claeys
For pioneering contributions to MEMS by developing and commercializing the microfabricated gas chromatograph

IEEE EDS ROBERT BOSCH MICRO AND NANO ELECTRO MECHANICAL SYSTEMS AWARD

CALL FOR NOMINATIONS



Robert Bosch (1861-1942)
Inventor, Entrepreneur, Founder of Robert Bosch GmbH

The Robert Bosch Micro and Nano Electro Mechanical Systems Award was established by the IEEE Electron Devices Society in 2014 to recognize and honor advances in the invention, design, and/or fabrication of micro- or nano- electromechanical systems and/or devices. Individual contributions should be innovative and useful for practical applications.

This award is sponsored by the IEEE Electron Devices Society with financial support from Robert Bosch LLC. It is intended that the award will be presented annually to an individual or to as many as three individuals whose achievements and contributions are judged to meet the selection criteria for the award. The award will be presented at an IEEE conference of the winner's choice. It is not necessary for the recipient(s) to be a member(s) of IEEE.

Please note: The EDS Bosch Award cannot be given to a candidate for the same work for which an IEEE Technical Field Award, IEEE Medal, or other society level award was previously received.

The recipient will receive a US$10,000 honorarium, travel expenses to attend the award presentation, a bronze medal, and a certificate. In the event that more than one awardee is selected, the cash honorarium will be equally divided among the recipients. Each recipient will receive a bronze medal and a certificate.

Nominations should be made using our online nomination form and submitted before midnight (EST) on 2 October 2023 to the EDS Executive Office. Letters of recommendation must be sent directly to l.riello@ieee.org according to the same schedule.

Congratulations to Oliver Ambacher 2022 IEEE EDS Lester F. Eastman Award Winner

Oliver Ambacher received his diploma and doctor of natural sciences at the Ludwig-Maximilians and the Technical University of Munich with distinction in 1989 and 1993. In 1993 he got a position as a research assistant at the Walter Schottky Institute at the Technical University of Munich, where he dealt with the growth of gallium nitride and its alloys with the help of molecular beam epitaxy and chemical vapor deposition. He was significantly involved in the implementation of the first ultra violet light detectors, surface acoustic wave components, microwave amplifiers and sensors as well as in the research of polarization-induced effects in GaN-based hetero- and quantum structures. In 1998/99 he was offered the Feodor Lynen grant from the Alexander von Humboldt Foundation at Cornell University (USA) to deepen his work in the field of AlGaN/GaN transistors for high-frequency power amplifiers. Following his habilitation in experimental physics in 2000 and his promotion to senior assistant in 2001, he was appointed professor for nanotechnology at the Technical University of Ilmenau a year later. In 2002 he was elected director of the Institute for Solid State Electronics and two years later he was appointed director of the Center for Micro and Nanotechnologies. Since October 2007, Oliver Ambacher has been a professor at the Albert-Ludwigs-University in Freiburg and head of the Fraunhofer Institute for Applied Solid State Physics until 2021.

He acquired a fundamental understanding of polarization-induced effects during a research stay as a young Humboldt fellow in Professor Les Eastman's group at Cornell University (1998–1999). In recent years Oliver Ambacher and his working group designed and demonstrated outstanding, integrated, broadband, low-noise amplifier for applications in cellular base stations for mobile communication. Due to its technical performance, this low-noise amplifier enables mobile communication with the help of various mobile radio standards in our wireless networks, such as 5G, LTE or WLAN. The work resulted in more than 650 journal contributions, about 300 conference and workshop proceedings, 7 books and book chapter and 8 patents.

In 2015 he received the Karl-Heinz-Beckurts-Prize for his contributions to the development of highly efficient power amplifiers based on GaN for the latest generation of mobile phone base stations. In 2018 he was awarded an honorary professorship for power electronics by the Gips-Schüle-Foundation. In 2021 he was awarded the Rudolph-Jäckel-Prize for the development of energy-efficient power electronics.

Erhard Kohn
2022 EDS Lester F. Eastman Award Chair

IEEE EDS Lester F. Eastman Award Call For Nominations

The IEEE Electron Devices Society invites the submission of nominations for the Lester F. Eastman Award. This award is presented annually to honor an individual who has made an outstanding achievement in high-performance semiconductor devices. The recipient is awarded a certificate and a check for $5,000, presented at the IEEE International Electron Devices Meeting (IEDM).

Description: To recognize individuals with outstanding achievement in high-performance semiconductor devices

Prize: $5,000 and a plaque

Funded: Funded by the Lester F. Eastman endowment fund and the IEEE Electron Devices Society

Eligibility: Any person active in the field of semiconductor devices, whether or not they are members of the IEEE Electron Devices Society, are eligible for the award. The EDS Lester Eastman Award cannot be given to a candidate for the same work for which an IEEE Technical Field Award, IEEE Medal, or other society level award was previously received.

Basis for Judging: Criteria considered by the selection committee will include an impact on the field of semiconductor devices. Evidence should include examples of leadership and professional interaction. Tangible supporting evidence in the form of publications, patents, and/or transition(s) to practice should be provided.

Presentation: Annually, at the IEEE International Electron Devices Meeting (IEDM)

Visit: https://eds.ieee.org/awards/lester-f-eastman-award

Donate: https://www.ieeefoundation.org/Eastman

Contact: If you have additional questions, contact the EDS Executive Office at eds@ieee.org

Nomination form: Visit the EDS website

Deadline to submit nominations: 1 July 2023

2022 IEEE EDS J.J. Ebers Award Winner

Professor Albert Wang of the University of California, Riverside, CA, USA, was selected as the 2022 J.J. Ebers Award winner. The J.J. Ebers Award is the most prestigious award of the IEEE Electron Devices Society for outstanding technical contributions to electron devices. This award recognizes Professor Wang "For pioneering contributions to the reliability of 3D heterogeneous integration in Integrated Circuits."

Albert Wang received the BS degree from Tsinghua University, the MS degree from the Chinese Academy of Science and the PhD degree from State University of New York at Buffalo. He is a Professor of Electrical and Computer Engineering at University of California, Riverside, USA. He was a Si Valley IC designer at National Semiconductor before joining Illinois Institute of Technology as an Assistant Professor of Electrical and Computer Engineering. His research covers semiconductor devices, analog/mixed-signal and RF ICs, design-for-reliability for ICs, 3D heterogeneous integration, emerging devices and circuits, and LED visible light communications. He published two books and 300+ peer-reviewed papers, and holds sixteen U.S. patents. His editorial board services include IEEE *Transactions on Circuits and Systems I*, IEEE *Electron Device Letters*, IEEE *Transactions on Circuits and Systems II*, IEEE *Transactions on Electron Devices*, *IEEE Journal of Solid-State Circuits,* and *IEEE Transactions on Device and Materials Reliability*. He has been IEEE *Distinguished Lecturer* for IEEE Electron Devices Society, IEEE Circuits and Systems Society and IEEE Solid-State Circuits Society. He was President of IEEE Electron Devices Society. He was Chair for the *IEEE CAS Analog Signal Processing Technical Committee*. His other committee services include the *International Technology Roadmap for Semiconductor*

Albert Wang, 2022 IEEE EDS J.J. Ebers Award Winner

(ITRS) Committee, *IEEE Heterogeneous Integration Roadmap (HIR) Committee*, *IEEE 5G Initiatives* Committee, *IEEE Smart Lighting Project Roadmap Committee* and *IEEE Fellow* Committee. He was General Chair of *IEEE Electron Devices Technology and Manufacturing (EDTM) Conference* and *IEEE Radio-Frequency Integrated Circuits (RFIC) Symposium*. He served as a Program Director of the National Science Foundation, USA (2019-2021). He was recipient of NSF CAREER Award and IEEE EDS Distinguished Service Award. Wang is a Fellow of National Academy of Inventors, an IEEE Fellow and an AAAS Fellow.

Paul Yu
EDS J.J. Ebers Award Chair

2023 IEEE EDS J.J. Ebers Award
Call for Nominations

The **Jewell James Ebers** Award was established in 1971 with the intention to foster progress in electron devices and to commemorate the life activities of Jewell James Ebers, whose distinguished contributions, particularly in the transistor art, shaped the understanding and technology of electron devices.

Sponsor: IEEE Electron Devices Society

Scope: Honors an individual(s) who has made either a single or a series of contributions of recognized scientific, economic, or social significance in the broad field of electron devices

Eligibility: Previous recipients of this award are ineligible. Self-nominations are not accepted or considered. Members of the EDS Awards Committee and voting members of the J.J. Ebers Award Committee are not permitted to submit or endorse nominations.

Prize: The award consists of a plaque and $5,000

Basis for judging: Nominees shall be judged based on outstanding technical contributions in the following: Field leadership in a specific area, specific contribution, originality, breadth, inventive value, publications, other achievements, honors, duration, nomination quality

J.J. Ebers Award Committee: Committee

Nomination deadline: 1 July 2023

Nomination form: https://ieeeforms.wufoo.com/forms/xl0lxns05xzwir/

2022 IEEE Electron Devices Society Education Award Winner

The EDS Education Award recognizes an IEEE/EDS Member from an academic, industrial, or government organization with distinguished contributions to education within the fields of interest of the IEEE Electron Devices Society. Professor Ilesanmi Adesida was selected as the 2022 EDS Education Award winner. The award cites Professor Adesida "*For outstanding contributions to international education, mentoring and diversity in the field of electron devices"*.

Ilesanmi Adesida is an experienced academic administrator and is currently the University Provost at Nazarbayev University in Kazakhstan where he oversees the institution's entire academic and research programs, including innovative strategic initiatives, awarding of research grants as well as overseeing the creation and implementation of quality assurance programs. Prior to his present appointment, he served as the Provost and Vice Chancellor for Academic Affairs at the University of Illinois at Urbana-Champaign (UIUC). He also served as the Dean of the College of Engineering and the Director of Micro and Nanotechnology Laboratory at UIUC.

Adesida received his BS, MS, and PhD in Electrical Engineering from the University of California at Berkeley. He has also worked as a Visiting Assistant Professor at Cornell University and served as the Head of the Electrical Engineering Department at Tafawa Balewa University in Nigeria. During his tenure as a faculty and administrator at UIUC, he was instrumental in creating many programs including the iFoundry for Innovation in Engineering Education, Illinois First-Year Engineering Experience (iFEX), Applied Research Institute, Advanced Digital Systems Center in Singapore, a new Engineering-Based College of Medicine, and the Siebel Center for Design.

As a faculty member, he designed curricula on semiconductor materials, semiconductor devices, and nanofabrication technologies and taught these courses to thousands of electrical engineering and materials science undergraduate and graduate students. In research, he has made important contributions to the science and technology of nanofabrication and high-speed electronic devices.

Professor Ilesanmi Adesida

He has authored or co-authored over 350 publications and over 250 conference papers including plenary talks. He has mentored and continues to mentor many students and faculty members including women and underrepresented minority groups. Many of these people have gone all over the world to become successful educators, start-up founders, and excellent academic administrators in top universities.

He has won many awards including the Oakley Kunde Award for Excellence in Undergraduate Education, and the TMS John Bardeen Award for outstanding contributions to electronic materials. He was named an outstanding graduate of the EECS Department at the University of California, Berkeley. He was awarded the Distinguished Service Award by the IEEE Electron Device Society of which he served as President in 2006/2007. He served as the Chair of the TMS Electronic Materials Committee. He has also served on many academic and industry Advisory Boards all around the world; and he is an elected member of the National Academy for Engineering.

Hiroshi Iwai
2022 EDS Education Award Chair

2023 EDS EDUCATION AWARD
CALL FOR NOMINATIONS

The IEEE Electron Devices Society invites the submission of nominations for the EDS Education Award. This award is presented annually by EDS to honor an individual who has made distinguished contributions to education within the field of interest of the Electron Devices Society. The recipient is awarded a plaque and a check for $2,500, presented at the IEEE International Electron Devices Meeting (IEDM).

The nominee must be an EDS member engaged in education in the field of electron devices, holding a present or past affiliation with an academic, industrial, or government organization. Factors for consideration include achievements and recognition in educating and mentoring students in academia or professionals in the industrial or governmental sectors. Specific accomplishments include effectiveness in the development of innovative education, continuing education programs, authorship of textbooks, presentation of short-courses at EDS sponsored conferences, participation in the EDS Distinguished Lecturer program, and teaching or mentoring awards.

Since this award is solely given for contributions to education, the nomination should exclude emphasis on technical contributions to engineering and physics of electron devices.

The nomination form can be found on the EDS website:
https://eds.ieee.org/awards/education-award

The deadline for the submission of nominations for the 2022 award is 1 September 2023.

2022 IEEE Electron Devices Society Early Career Award Winner

The EDS Early Career Award recognizes young IEEE/EDS members who have made outstanding contributions in an EDS field of interest during the early years of their professional career after graduation.

The 2022 EDS Early Career Award winner is Girish Pahwa. Please visit the IEEE EDS website to view additional information about the award.

Girish Pahwa is an assistant professional researcher in the department of electrical engineering and computer sciences (EECS) at the University of California (UC) Berkeley. He is also the executive director of the Berkeley Device Modeling Center (BDMC) at UC Berkeley. Before this, he worked as the manager of the BDMC and BSIM (Berkeley Short Channel IGFET model) group and as a postdoctoral scholar at the department of EECS, UC Berkeley.

He received his Ph.D. and M.Tech. Degrees in electrical engineering from the Indian Institute of Technology (IIT) Kanpur in 2020, and his B.Tech. Degree in electronics and communication engineering from Delhi Technological University in 2014.

Girish's research primarily focuses on the device modeling, simulation, and benchmarking of emerging nanoscale technologies. As the chief researcher at the BDMC, he has advanced the BSIM suite of compact models, as the loyalty-free industry standard models, for the simulation and design of ICs for upcoming and emerging applications. He has developed the first industry-standard cryogenic FinFET and FDSOI models for the design of peripheral ICs that need to be in close proximity to the qubits in emerging quantum computing applications. These models can also play a vital role in the design-technology co-development of cryogenic-CMOS ICs to significantly improve the performance and power efficiency of high-performance computing (HPC) systems. He has also developed ferroelectric device models and contributed extensively to the physics and device-circuit co-design strategies of these emerging devices that can potentially reduce CMOS power consumption many folds or enable computing in

memory for artificial intelligence or other applications. He has further contributed to developing industry-standard compact models for high-voltage transistors for power IC applications.

Girish is a member of the Institute of Electrical and Electronics Engineers (IEEE) and the IEEE Electron Devices Society (EDS), also serving as a reviewer of several journals. He has over 45 technical publications in prominent journals and conferences. He received the outstanding Ph.D. thesis award from IIT Kanpur in 2020 for his contributions to the field of novel ferroelectric field effect transistors. He also received the best paper award at the IEEE International Conference on Emerging Electronics (ICEE), Mumbai, India, in 2016.

Apart from research, Girish has a keen interest in volunteering for science education for underprivileged kids. He enjoys painting and reading about the history of science. He is a fitness enthusiast and loves playing table tennis and cricket.

Bin Zhao
2022 EDS Early Career Award Chair

CALL FOR NOMINATIONS

2023 IEEE EDS Early Career Award

Description: Awarded annually to individuals to promote, recognize and support Early Career Technical Development within the Electron Devices Society's field of interest

Prize: An award of US$1,000, a plaque; and if needed, travel expenses not to exceed US$1,500 for each recipient residing in the US and not to exceed US$3,000 for each recipient residing outside the US to attend the award presentation.

Eligibility: Candidates must be an IEEE EDS member and must have received his/her first professional degree within the 10th year defined by the August 15 nomination deadline and have made contributions in an EDS field of interest area. Nominators must be IEEE EDS members. Previous award winners are ineligible.

Selection/Basis for Judging: The nominator will be required to submit a nomination package comprised of the following:

- The nomination form that is found on the EDS web site, containing such technical information as the nominee's contributions, accomplishments and impact on the profession or economy and a biographical description.
- A minimum of two and a maximum of three letters of recommendation from individuals familiar with the candidate's technical contributions and other credentials, with emphasis on the specific contributions and their impacts.

The basis for judging includes such factors as: the demonstration of field leadership in a specific area; specific technical contribution(s); impact on the profession or economy; originality; breadth; inventive value; publications; honors; and other appropriate achievements.

Schedule: Nominations are due to the EDS Executive Office on August 15th each year. Candidates will be selected by the end of September, with a presentation to be made in December.

Presentation: At the EDS Awards Dinner that is held in conjunction with the IEEE International Electron Devices Meeting (IEDM) in December. The recipients will also be recognized at the December EDS BoG Meeting.

NOMINATION FORM: Visit the EDS Website

For more information contact: eds@ieee.org

Bin Zhao
2022 EDS Early Career Award Chair

IEEE ELECTRON DEVICES SOCIETY

Women in Semiconductor Panel Session and Young Professionals Meet at ICEE2022, Bangalore India

By P Susthitha Menon, Mayank Shrivastava, Sushobhan Avasthi, Vinila Bedekar, Pragya Kushwaha, Merlyne de Souza, Shubhangi Bharadwaj, Navakantha Bhat, and Ravi Todi

The 6th International Conference on Emerging Electronics (ICEE2022) sponsored by IEEE Electron Devices Society (EDS) and chaired by Prof. Mayank Shrivastava from IISc Bangalore was held at the Hilton and Hilton Garden Inn Bengaluru Embassy Manyata Business Park from 12–14 December 2022. During the conference, the Women in Semiconductor (WiSEMI) Panel Session was held on 12 December over evening tea. It was moderated by Women in EDS (WiEDS) Chair, P Susthitha Menon. IEEE EDS President, Ravi Todi was present to give his welcoming remarks. A total of 50 attendees were privileged to hear the insights from outstanding women from the semiconductor industry: Bharathi V (Intel), Sushma Nirmala Sambatur (GF), Sumedha Limaye (Intel), Gauri Karve (IMEC), Sneha Revankar (Samsung), Bindu Rao (Intel), Maria Merlyne De Souza (Vice President of Membership, IEEE EDS & University of Sheffield). They spoke in a casual atmosphere, sparked with humor, about their life journeys from the macroscopic to the micro/nanoscopic world and how the ambiance of their work environment encouraged their emergence as leaders. The session was remarkable because of active participation by attendees-budding semiconductor professionals and students who were able to interact freely for well over an hour on topics such as work-life balance, academia versus industry, career pathways, becoming influencers at work, and thereby seeking inspiration from role models.

Women in Semiconductor (WiSEMI) panel session during ICEE2022

Young Professional Meet session during ICEE2022

A Young Professionals Meet was also held during the conference on 14 December and was attended by 30 people. The session was moderated and coordinated by WiEDS member and IEEE EDS Early Career Award Winner, Pragya Kushwaha and by IEEE IISC NTC Student Branch Chair, Shubhangi Bhardwaj. Several mentors and IEEE EDS volunteers were present to guide young and enthusiastic researchers in the field of electronics and semiconductors. They were Maria Merlyne De Souza, Shankar N. Ekkanath Madathil, Gauri Karve, Seena V, Giuseppe Cantarella, Sudhir Kumar, Harshit Agarwal, and Subu Iyer.

IEEE EDS would like to thank all the 20+ ICEE volunteers for making both WiEDS and YP sessions a huge success. The organizers of the sessions would like to especially acknowledge the contribution of IEEE EDS Bangalore Chapter, ICEE 2022, and its volunteers Miss Shubhangi Bhardwaj, President of IEEE Nano Council and Sensor Council Student Chapter at IISC who liaised between the Chair of the organizing committee Prof. Mayank Shrivastava and VP membership, Prof. Merlyne De Souza, Dr. Vinila, Ankit Malik and few others in running a successful membership drive. The success is attributed to an offer of free IEEE membership to the first 100 student attendees, sponsored by IEEE EDS Bangalore Chapter. The ICEE team came up with the idea of providing a custom business card to each student attendee for its use during various networking and mentorship sessions. These business cards were distributed at the IEEE EDS membership booth, offered by ICEE, and accepted by over 70 students who have also signed-up as volunteers for IEEE EDS. ICEE promoted the benefits of volunteering and actively helped create an environment of engagement with its potential new members.

Call for Nominations

PhD and Masters Student Fellowships and Undergraduate Student Scholarships

The IEEE Electron Devices Society invites nominations for our society sponsored Student Fellowships and Scholarships. These annual awards are given to promote, recognize, and support graduate, masters, and undergraduate level study and research within the scope of Electron Device technologies.

EDS Masters Student Fellowship
Prize: US $2,000 and award plaque
Submission Deadline: 15 May 2023

EDS PhD Student Fellowship
Prize: US $5,000 and travel funds
to IEDM for award presentation
Submission Deadline: 15 May 2023

EDS Undergraduate Student Scholarship
Prize: US $1,000 and award plaque
Submission Deadline: 15 May 2023

Please help to promote these funding opportunities to students in your personal and professional network!

ED Malaysia Kuala Lumpur Chapter STEM Programs funded by IEEE EDS Educational Activities in Malaysia

By P Susthitha Menon, Hasnizah Idris, Ahmad Sabirin Zoolfakar, Maizatul Zolkapli, Azrif Manut, Norhayati Soin, Rozina Abdul Rani, Iskandar Yahya, Lee Xiao Xian, and Ahmad Rifqi Md Zain

IEEE EDS Educational Activities funded several STEM programs for schools in Malaysia. They were led by IEEE Education Activities Committee member and IEEE STEM Champion, AP Dr. P. Susthitha Menon from the Institute of Microengineering and Nanoelectronics (IMEN), Universiti Kebangsaan Malaysia (UKM). A total of 6 programs were executed from 12 November till 7 December 2022 in collaboration with many different entities in the states of Terengganu, Kuala Lumpur, Selangor and Kedah.

First off, the STEM4Fun program was conducted on 12–13 November 2022 by IEEE EDS Malaysia Chapter at the Dewan Perdana, Universiti Sultan Zainal Abidin (UNISZA), Terengganu in collaboration with the Faculty of Innovative Design and Technology, UNISZA. The STEM4FUN program includes exposure to cutting-edge technology such as Snap Circuits, green technology, the use of gadgets or technological devices to strengthen students' understanding of STEM subjects, particularly in the field of electron devices. A Train the Trainer Session was held on 12 November for the undergraduate students of the faculty to enable them to be facilitators during the STEM event. On 13 November, a total of 156 school students from 39 schools in the Kuala Nerus District attended the STEM event with their teachers in the presence of the Kuala Nerus District Education Office.

The second STEM program named Gala IR4.0 was held at the Asia Pacific University of Science and Technology and Innovation (APU) Kuala Lumpur on 23–24 November 2022. The program was organized by the Kuala Lumpur Federal Territory Education Department in collaboration with IEEE EDS Malaysia Chapter and IEEE EDS UKM Student Branch. It comprised a STEM exhibition booth, STEM4Fun school event and a career talk for high-school students. The EDS-ETC Snap Circuits kits were displayed at the exhibition booth and prizes were given to students who could build the circuits within the given time. The STEM4Fun event and the career talk were attended by a total of 160 school students from schools in Kuala Lumpur. The attendees were provided with Snap Circuits and Solar Bots as well as the different career paths of becoming an engineer.

The third STEM program "Electronics with Coding and Robotics: Tobbie II @ SK Sultanah Asma," was conducted

Career talk for high school students during Gala IR4.0 STEM program in APU Kuala Lumpur, 23–24 November 2022

Train the student session STEM4Fun at UNISZA on 19 November 2022

Trainers of the STEM event held at SK Sultanah Asma on 26 November 2022

Electronics with Coding and Robotics STEM event at SK Bukit Jalil on 2 December 2022

on 26 November 2022 by IEEE EDS Malaysia in collaboration with the Faculty of Electronic Engineering & Technology, Universiti Malaysia Perlis (UniMAP), and IEEE Sensors & Nanotechnology Council Malaysia Joint Chapter (SNC-MJC). This half-day program was held at SK Sultanah Asma, Alor Setar, Kedah in conjunction with their 100th Anniversary celebration and National Level STEM Carnival TS25. Thirteen volunteers including academic staff and students from the FEET, UniMAP conducted the program which was attended by more than 50 students from Standard 1 to 6. All educational kits were provided by IEEE EDS Malaysia including 1) Tobbie II Robot which uses a micro:bit programmable board and Microsoft MakeCode Editor or Python Editor for coding, and 2) Snap Circuits with coding (using Bluetooth-powered SC controller and enabled via app-driven BOTcode and Blockly codes). During the program, 3 modules were constructed and executed for the Tobbie II, which are Tobbie Explorer, Tobbie Follow Me and Tobbie Light Tracker. Three modules were also implemented using Snap Circuits which included Electric Light, Coding 5 Lights and Coding Challenge: BotCode and Blockly Coding.

The fourth STEM program on Electronics with Coding and Robotics was held on 28 November 2022 in the SK Bukit Kuchai School in Puchong. The program was carried out by the IEEE EDS UKM Student Branch in collaboration with IMEN, UKM. A total of 7 IEEE volunteers, 30 students and 3 school teachers participated in the program. Similarly to the third program, the students had at their disposal the Elenco Discover Coding kits as well as the Tobbie II robot which utilizes the micro:bit board. Quizzes were conducted and prizes as well as certificates were given to the winners. The participating school was awarded with a STEM kit to enable them to continue with STEM events in the future.

Electronics with Coding and Robotics STEM event at SK Bukit Kuchai on 28 November 2022

Organizers and students who participated in the STEM program at Kuala Muda/Yan District Education Office Kedah on 6–7 December 2022

A similar STEM program was replicated at SK Bukit Jalil, Kuala Lumpur on 2 December 2022 by IEEE EDS Malaysia Chapter in collaboration with IMEN, UKM and Universiti Malaya. A total of 5 IEEE volunteers, 30 students and 5 school teachers participated in the program which involved Discover Coding kits, Tobbie II robots, basic micro:bit board and coding introduction. Quizzes were conducted during the program and prizes and certificates were handed

to the winners. Again, a STEM kit was awarded to the participating school so that they may continue pursuing STEM events in the future.

The sixth and last program to be executed using the Education Grant was the Science and Technology Exploration Camp held on 6–7 December 2022 at the Kuala Muda/Yan District Education Office in Kedah. A total of 20 volunteers, 160 school students and their teachers attended the half-day STEM program held on two different days. The program was executed by AT&S Kedah in collaboration with IMEN, UKM. The students carried out experiments involving electrical circuits and hydrophobicity/hydrophilicity of different materials. IEEE EDS Malaysia sponsored keychains for all volunteers and students.

IEEE EDS Malaysia Chapter would like to thank IEEE EDS Educational Activities and IEEE STEM Champion for the financial support in executing STEM programs in Malaysia with the hope that more Malaysian students will opt for STEM-based electronics engineering as their choice of career in the future.

~Sharma Rao Balakrishnan, Editor

ED National Institute of Technology—Silchar Student Branch Chapter

By T.R. Lenka

On 25 December 2022, the Chapter in association with Nanotechnology Council (NTC) Chapter and the Department of Electronics and Communication Engineering, National Institute of Technology Silchar organized at Borakhai Tea Garden, Silchar, Assam the 2nd Annual EDS/NTC Social Meet 2022 to witness the celebration of Merry Christmas. The program was attended by 13 EDS/NTC (faculty) members with their families and children and 18 EDS student members of M.Tech (Microelectronics and VLSI Design) and PhD program. The program was very successful and was highly praised by each and every member of the Chapter.

~Soumya Pandit, Editor

EDS/NTC Social Meet; behind the banner from left: Mr. Rabin Paul—SBC Vice-Chair, Mr. G. Purnachandra Rao—SBC Treasurer, Ms. Samadrita Das—SBC Chair, Dr. T. R. Lenka—Chapter Advisor, Prof. F. A. Talukdar, Branch Counsellor (standing in 2nd row behind Mr. Rao), and EDS/NTC members/student members, faculty members, and their family members

USA, Canada & Latin America (Regions 1–6 & 7)

ED Santa Clara Valley and San Francisco Joint Chapter (SCV/SF)

—by Imran Bashir

The IEEE Electron Devices Society (EDS) San Francisco/ Santa Clara Valley Joint Chapter held its first webinar of 2022 on 2 September with Dr. Yaniv Jacob Rosen who is currently the deputy group leader of the Quantum Coherent Device Physics group at Lawrence Livermore National Laboratory (LLNL). The lecture titled *"The LLNL Quantum Design and Integration Testbed"* described QuDIT, a quantum testbed to explore different methods of implementing quantum computing and sensing. The lecture began with an introduction to quantum computing and its potential to achieve speedup in specific use cases. The lecture outlined the benefits of high-level quantum elements and optimal control techniques designed to solve quantum systems.

The second webinar titled "Design and Modelling Challenges for Very Large-Scale Integrated Quantum Processors in Foundry CMOS Technologies" was conducted on 18 November and the lecturer for that event was Dr. Sorin P. Voinigescu who is a professor at the Electrical and Computer Engineering Department at the University of Toronto. His research and teaching interests focus on the modeling, characterization and fabrication of nanoscale and atomic-scale electronic devices. The lecture covered main challenges in the physical implementation, design, hierarchical modeling and simulation of the scalable qubit array and of the cryogenic control and readout electronics for large scale quantum processors. Details about the impact of process manufacturing, rules restrictions and process variation on qubit design and modeling were outlined. Please visit our website @ https://site.ieee.org/scv-eds/ and join the email list to receive notification of future events and instructions on joining remotely through Zoom.

5th IBM IEEE CAS/EDS AI Compute Symposium (AICS'22)

—by Dr. Rajiv Joshi, Kaoutar El Maghraoui, Arvind Kumar, and Matthew Ziegler

The 5th IBM IEEE CAS/EDS AI Compute Symposium, known as (AICS'22), was held for two days (11–12 October 2022) at the IBM T. J. Watson Research Center. The symposium was also supported by the IBM Academy of Technology (https://www.ibm.com/blogs/academy-of-technology/). Dr. Joshi was the interface for CAS and EDS in organizing this successful event. The theme of the symposium was "Scalability to Sustainability." In short, the symposium covered a range of topics from device technology, to circuits, architecture, algorithms, and sustainability to make innovations for the cloud with an emphasis on green AI.

For the third straight year, the symposium provided a virtual access option, allowing an increase in attendance. The event was very well attended and received great responses from the audience all over the world. Close to 1000 viewers for two days, participation from 50 countries, over 30 student posters, best poster awards, excellent panel discussions, and 11 distinguished speakers from industry and academia were the salient features of this symposium. There were more than 2600 views on the LinkedIn post about the symposium.

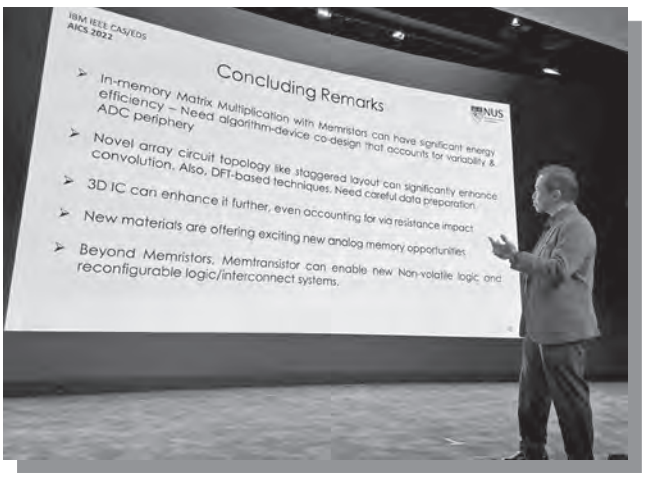
At the beginning, Dr. Rajiv Joshi, lead organizer, and IEEE Life Fellow, gave welcoming remarks, a short history, progress, and the impact of the symposium.

Then Robert Muchsel, Analog Devices fellow, opened the symposium with an excellent presentation related to **"Improving Privacy and Energy Usage by Pushing AI Inference to the Edge of the IoT Frontier."** Although artificial intelligence dominates the tech news, most AI solutions are expensive, big, and energy hungry. The connected nature of these systems also leads to significant concerns relating to privacy and system autonomy. Mr. Muchsel described ADI's true edge AI accelerators, which employ

Robert Muchsel, ADI highlighting AI Challenges

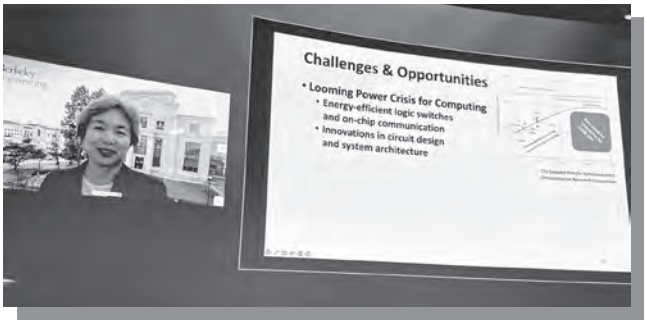
many low-power innovations to enable AI inference on a battery while improving privacy through local computing at the edge.

Professor Aaron Thean, the Dean of the College of Design and Engineering at the National University of Singapore (NUS), followed up with an exciting talk related to "**Novel Material-System Co-Design Opportunities for Analog-Non-Volatile In-Memory Computing and Reconfigurable Edge-AI**." Ultra-low energy and area-efficient electronic systems are required to enable untethered computing at the edge of IoT. To realize self-learning edge-AI systems, conventional solely software-driven deep-learning neural networks become a major roadblock due to the excessive energy expense of training. Hence, fundamental hardware change is likely needed. In this talk, Dr. Thean reviewed how recent material innovations (e.g. Ferroelectric oxides and 2D Material) coupled with new micro-architecture innovations (e.g. novel memory physical layout and monolithic 3D IC) may significantly accelerate in-memory computation. His talk covered wafer-level solution-processed CMOS-compatible use of 2D material (MoS2/WSe2) to enable high-endurance memristors that can have properties superior to conventional oxide RRAMs. Through material-device-aware data encoding, error correction, and novel physical memory layout (staggered + Manhattan arrays), this work aims to simplify the in-memory data process. Dr. Thean showed how one can significantly manage variabilities while accelerating convolution-deep neural network operations and offering substantial low-energy opportunities for Edge-AI systems.



Prof. Aaron Thean, National University of Singapore presents concluding remarks

Subsequently, Professor Tsu-Jae King Liu, Dean of the College of Engineering, University of California, Berkeley gave a very interesting talk about **"Technology Co-Design and Innovation for the Age of Ambient Intelligence."** As practical limits for transistor miniaturization are reached, alternative approaches for improving integrated circuit functionality and energy efficiency at acceptable cost will be necessary to meet the growing demand for information and communication technology. This presentation showcased how technology co-design and innovation can achieve dramatic improvements in computing performance to usher in the "Age of Ambient Intelligence."



Professor Tsu-Jae King Liu, University of California, Berkeley, showcases challenges and opportunities in her talk on Technology and Innovation

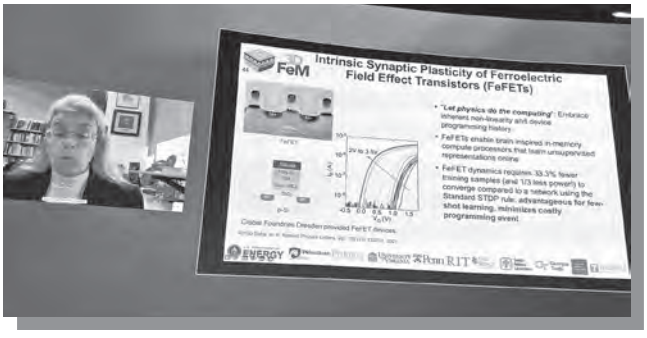
Then Bill Luan, Senior Program Manager, Coral team at Google talked about **"Using Coral for Scalable and Sustainable AI at the Edge."** With the advancement in AI research over the past decade, AI/ML technology has expanded from being only available on cloud-based data centers to becoming available on IoT and edge devices, opening huge opportunities for innovations. Leading this change is the Coral platform from Google, making deploying AI at the edge on a large scale not only possible but also sustainable. This presentation covered the Coral platform in detail, including product features and applications by businesses around the world that are leveraging Coral for deploying innovative edge AI solutions at scale.

Next, Arun Venkatachar, Vice President of AI, Cloud, and Central Engineering Synopsys Inc., gave a wonderful talk related to the "**Confluence of AI & Cloud with EDA**." Investments in AI/ML/Cloud/Big Data to solve EDA problems with ever-increasing complexities of chip design are starting to come to light. Recent product announcements like the DSO.ai from Synopsys revolutionizes chip design by massively scaling the exploration of options in design workflows. Similarly, there are many applications in production solving different challenges in areas like verification, place & route, manufacturing, etc., that have harnessed the power of AI/ML, Big-data and computing to provide a new set of tools and techniques for EDA to address both existing and new challenges. His overall suggestion to other companies is to build good data strategies and compute utilization approaches to harness these benefits across their organizations. They will also need to invest in good data and AI/ML and cloud infrastructures to expedite building these solutions.

The final talk on day one was given by Prof. Jason Cong, Director of the Center for Domain-Specific Computing (CDSC) and Director of the VLSI Architecture, Synthesis,

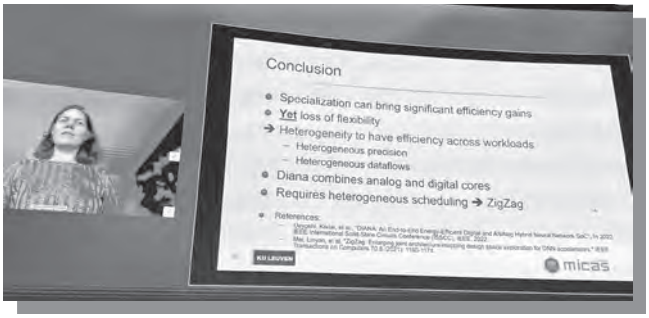
and Technology (VAST) Laboratory at UCLA. The talk focused on "**Automated Synthesis and Architecture Optimization for Deep Learning Accelerator Designs**." AutoSA is an automated compilation framework for generating systolic arrays, and a core acceleration engine for most deep-learning applications. AutoSA is based on the polyhedral framework and incorporates a set of techniques for both computation and communication optimizations. Based on AutoSA, an automated, efficient, and comprehensive design space exploration is performed to achieve optimal systolic array designs for deep learning applications. Dr. Cong's study revealed that a number of widely used heuristics based on "common sense" often lead to sub-optimal solutions, such as limiting to loop count divisors for tiling and pruning based on off-chip data movement minimization. Finally, he showed AutoSA integrated into an end-to-end acceleration framework for deep learning using a flexible and composable architecture called FlexCNN. This approach can deliver high computation efficiency for different types of convolution layers using techniques such as dynamic tiling and data layout optimization. AutoSA and FlexCNN are both open-source projects.

Prof. Susan Trolier-McKinstry, an Evan Pugh University Professor and Steward S. Flaschen Professor of Ceramic Science and Engineering at The Pennsylvania State University, opened the second day with developments in **"New Materials for Three Dimensional Ferroelectric Microelectronics."** In the last decade, there have been major changes in the families of ferroelectric materials available for integration with CMOS electronics. These new materials, including $Hf_{1-x}Zr_xO_2$, $Al_{1-x}Sc_xN$, $Al_{1-x}B_xN$, and $Zn_{1-x}Mg_xO$, offer the possibility of new functionalities. This talk discussed the possibility of exploiting the 3rd dimension in microelectronics for functions beyond interconnects, enabling 3D non-von Neumann computer architectures exploiting ferroelectrics for local memory, logic in memory, digital/analog computation, and neuromorphic functionality. This approach circumvents the end of Moore's law in 2D scaling, while simultaneously overcoming the "von Neumann bottleneck" in moving instructions and data between separate logic and memory circuits. Computing accounts for 5–15% of worldwide energy consumption. In the U.S., data centers alone are projected to consume approximately 73 billion kWh in 2020. While recent efficiency gains in hardware have partially mitigated the rising energy consumption of computing, major gains are achievable in a paradigm shift to 3D computing systems, especially those that closely couple memory and logic. Dr. Trolier-McKinstry's talk covered the relevant materials, their deposition conditions, and what is known about the wake-up, fatigue, and retention processes.



Professor Susan Trolier-McKinstry, Pennsylvania State University describes Ferro-electric materials and their applications

Next, Marian Verhelst, Professor at the MICAS laboratories of KU Leuven and a research director at IMEC, gave a talk related to tinyML, **"Heterogeneous Multi-Core tiny M.L."** She described approaches for powerful machine inference in resource-scarce distributed devices. Developing intelligent applications at ultra-low energy and low latency requires compact computing and memory structures that have very high utilization. This has resulted in a wide variety of proposed state-of-the-art accelerator designs. However, it becomes increasingly clear that intelligent edge devices will need to be equipped with a diverse set of many heterogeneous co-processors, which allow running every workload on the most compatible (combination of) accelerators. Moreover, by using multiple cores in parallel and streaming data between the cores, the required amount of on-chip memory and IO bandwidth can be reduced, leading to area, energy, and latency savings. Dr. Verhelst's talk explained the benefits and challenges of such heterogeneous ML systems, and how they allow scaling up performance at low budgets.

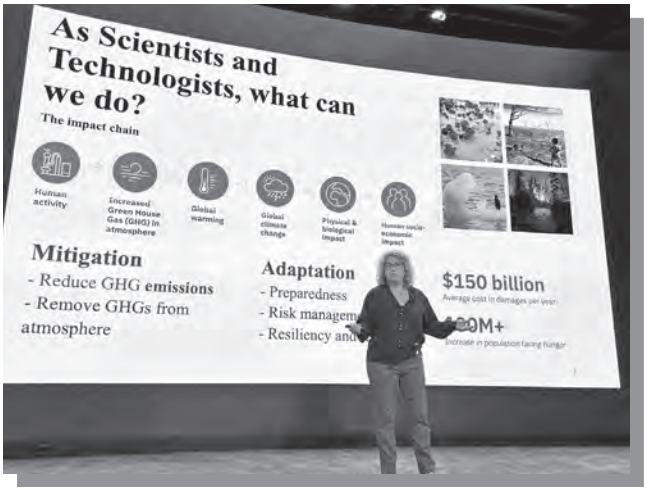


Professor Marian Verhelst, KU Leuven concludes her talk

Dr. Steve Teig, CEO of Perceive, enlightened the audience with **"Machine Learning for Real: Thinking More Carefully About Efficiency, Loss Functions, and GANs."** Deep learning seems to touch every discipline these days, but behind its startling magic tricks, it is surprisingly primitive. It is concerning to note the extent to which today's deep learning relies on folklore: on recipes and anecdotes, rather than on scientific principles and explanatory mathematics. We can only imagine how much more trustworthy, robust, compact, and power-efficient our models would be if we designed them more rigorously. Dr. Teig's assertions were accompanied by some motivating (and occasionally humorous) examples.

Then Dr. Stefanie Chiras, Senior Vice-President, Partner Ecosystem Success, Red Hat, gave a very interesting talk about **"AI at the Open Edge."** Complex use cases and game-changing potential collide when AI is delivered at the edge. This creates a perfect Petri dish for innovation, not only at the technology level but in how different skills and disciplines collaborate. Building frameworks, architectures, and services can reduce the complexity and enable businesses to extract actionable insights by processing data closer to devices, sensors, and other sources. Red Hat sees this opportunity as an extension of the open hybrid cloud, bringing capability all the way out to the far edge…even as far as the International Space Station.

Finally, Dr. Tamar Eilam, IBM Fellow, gave a talk on **"The Road to Sustainable Computing."** She presented IBM's initiative related to sustainable and responsible computing. Dr. Eilam described how to design a sustainable data center. Key important steps include finding pathways to achieve multi-DC sustainability goals incorporating exogenous factors, natural resources, cooling, water, energy for IT, and other constraints within a holistic DC Model. She also emphasized the importance of explainable AI, and contra-factual analysis with a focus on capital and operational cost with environmental impacts, such as, capitalized carbon footprint emissions, operational carbon footprint, and operational water use. Dr. Eilam pointed out the need for utilizing renewable energy, such as solar, wind, wave, etc., energy storage mediums, software platforms, infrastructure, and water usage and heat wastage. The key lies in utilizing sustainable computing by predicting the power consumption, co-optimization of software/system-based behavior, and coupling renewable energy.



Dr. Tamar Eilam, IBM, emphasizes the need for sustainability

The Poster Session followed the keynote talks on day 1 of the symposium. Out of 32 posters, the best posters were awarded from each of the 3 tracks. The list of winners is given on the symposium website.

The symposium closed with a panel discussion on sustainability, with five distinguished panelists including Mr. Robert Muchsel (ADI), Dr. Tamar Eilam (IBM), Prof. Christopher Hill (MIT), Prof. Prashant Shenoiy (University of Massachusetts), and Prof. Aaron Thean (National University of Singapore). Panelists discussed sustainability at all levels, including algorithmic and architecture techniques, data center carbon footprint reduction, product development, and applications where AI can help. Replays of the entire two-day symposium are available on the symposium website: https://www.zurich.ibm.com/thinklab/AIcomputesymposium.html

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~Lawrence Larson, Editor

Europe, Middle East & Africa (Region 8)

IEEE EDS Mini-Colloquium at Addis Ababa Institute of Technology (AAiT)

—by Benjamin Iñiguez

The IEEE EDS sponsored a mini-colloquium organized by the IEEE Ethiopia Subsection and the School of Electrical and Computer Engineering at AAiT on 11 November 2022. The aim of this event was to promote IEEE EDS activities in Ethiopia and to encourage the formation of an EDS Chapter. The mini-colloquium was held in person at AAiT and began with a welcome by the director of the institute Dr. Bikila. This was followed by with contributions from two IEEE distinguished lecturers:

- Professor Benjamin Iñiguez (Universitat Rovira i Virgili, Tarragona, Spain) speaking on "Roadmap and Challenges of Flexible and Printed Electronics"
- Professor Lluis Marsal (Universitat Rovira i Virgili, Tarragona, Spain) speaking on "Progress in High Efficiency Organic Solar Cells"

Professor Arokia Nathan of the University of Cambridge was unfortunately unable to attend to speak on

Attendees at the IEEE EDS sponsors mini-colloquium at the Addis-Ababa Institute of Technology. Distinguished Lecturers, Prof. Benjamin Iñiguez and Prof. Lluis Marsal (front row, second and third from the right)

"Ultra Low Power Interfaces for IoT." The event was closed by Dr. Bisrat, the head of the School of Electrical and Computer Engineering who thanked the IEEE EDS and the distinguished lecturers for their support.

Over 100 attendees enjoyed the opportunity to learn about state-of-the-art research work and ask questions of the distinguished lecturers. The DLs were also very pleased since they were able to expand their horizons and reach out to students and professionals with considerable potential, but who never had the chance to connect to the rest of IEEE professional and research societies. The event has shown that there is scope for future events to utilize the potential in Ethiopia and Africa.

~Stewart Smith, Editor

ED Germany Chapter

—by Mike Schwarz

Rajiv Joshi presented "Memories from Storage to Computing"

The ED Germany Chapter organized a hybrid Distinguished Lecture entitled *"Memories from Storage to Computing"* on 14 December 2022. The lecture was given by Dr. Rajiv Joshi from IBM—T. J. Watson Research Center, IEEE Fellow, and was chaired by Prof. Alexander Kloes and Prof. Mike Schwarz from the Competence Center for Nanotechnology and Photonics (NanoP) of THM—University of Applied Sciences, Germany. The DL was attended by 17 IEEE participants, as well as 43 non-IEEE members onsite and via Zoom video conference system.

After a welcome from Prof. Schwarz, Dr. Joshi stepped directly into the subject of memories. A comprehensive introduction with the essential basics was part of the first minutes of the DL. The first semester's students welcomed the context Dr. Joshi presented, and found many theoretical topics discussed in microcomputer technology lectures, in practical applications.

Then the lecture concentrated on the brick wall of memories, focusing on the memory bandwidth wall. The outcome of the brick wall challenge, postulated back in the past by Dr. David Patterson, was that all components i.e. power wall, memory wall and ILP (instruction level parallelism) wall sum up. From that point of view the need and/or push for low Vmin was obvious during the following discussions. Finally, power dissipation and further attributes play a significant role in memories. Designers have to deal with all the attributes (non-volatility, high density, low power consumption, bit alterability, endurance, low cost, etc.) and there is always an engineering trade off and no holy grail for memories.

Dr. Joshi went through the topic of memory as storage and discussed SRAMs as storage and methods like boosting during read out to stabilize the cells. Afterwards, the impact of variability and considering this domain during designing was addressed. The demand on fast algorithms to explore the tails of statistical variability distributions is required to ensure high yields. After this part of the lecture Dr. Joshi changed the focus on "*From Moore's law to AI law.*" Within this part, various discussions on i.e. the explosion of alternative processing power (CPU ✇GPU ✇NPU) took place. Furthermore, deep learning and enhancing its performance was under consideration by considering building blocks of those and realize them in hardware to allow for computation with memory. Finally, non-volatile memory technologies were compared by experimental data and the design challenges of InMemory Computing

Dr. Rajiv Joshi and the audience

Dr. Rajiv Joshi during the talk "Memories from Storage to Computing"

(IMC) concluded an excellent Distinguished Lecture. This was finished by high level QnA after the lecture. The students particularly liked the conceptual presentation of the basics and the continuous increase in level up to the advanced topics. Finally, it was a very good mixture of low and advanced level topics.

ED Spain Chapter

—by Benjamin Iñiguez

Mini-Colloquium on CAD Modeling and EDA Tools

An EDS Mini-Colloquium (MQ) on CAD Modeling and EDA Tools was organized by the ED Spain Chapter and was held on 28–29 June 2022. The Chair of this MQ was Prof. Benjamin Iñiguez (University Rovira i Virgili, Tarragona, Spain—URV).

Several topics related to the characterization, modeling and applications of different types of semiconductor were addressed by eight speakers. Seven of them are EDS Distinguished Lecturers. Four presentations were in person and four more were virtual.

There were four talks on the morning of 28 June. Dr. Muhammad Nawaz (Hitachi Energy, Sweden) addressed the "Characterization and TCAD modeling based design assessment of ultra-high voltage SiC devices." Prof. Jesús del Alamo (MIT, USA) conducted a lecture on the "Nanoscale InGaAs FinFETs: Band-to-Band Tunneling and Ballistic Transport." Prof. Arokia Nathan (Darwin College, University of Cambridge, UK) addressed in a virtual talk the topic "Physics-Based Parameter Extraction for Thin Film Transistors". Finally, Prof. Lluís F. Marsal (URV) made a presentation about "Characterization and modeling of organic solar cells."

On June 29, two talks were given in the morning and two more in the afternoon. Dr. Elena Gnani (University of Bologna, Italy) presented "Trends and challenges in Nanoelectronics for the next decade." Dr. Wladek Grabinski (GMC, Switzerland) addressed "SPICE and Verilog-A Modelling Using FOSS TCAD/EDA Tools: Technology—Devices—Applications." The last two lectures were virtual and conducted on June 29 in a Joint Session between this MQ and the Graduate Student Meeting on Electronic Engineering. Prof. Enrique Miranda (Autonomous University of Barcelona, Spain) addressed "Compact modeling of memristive devices for neuromorphic computing." Finally, Dr. Samar Saha (Prospicient Devices Inc., CA, USA) talked about "Physical Principles to Formulate Thin Film Transistor Models for Circuit Design."

Graduate Student Meeting on Electronic Engineering

The Graduate Student Meeting on Electronic Engineering was held also in Tarragona on 29–30 June, and included the Joint Session with the MQ mentioned above, two sessions with Ph.D. student presentations (29 June afternoon and 30 June morning), a poster session and two more invited talks. The Chair was Josep Ferré-Borrull, Professor at the University Rovira i Virgili (URV). It is an annual event established and organized by the Department of Electronic, Electrical and Automatic Control Engineering of URV in 2003. It consists of two days of plenary talks given by invited prestigious researchers about selected topics related to electronic engineering, short talks given by last year Doctoral students presenting their last research results, and a poster session where Master and PhD students in this field present their work.

One of the invited talks was given on 30 June by Dr. Luis Fernando da Silva (Federal University of Sao Carlos, Brazil), and was entitled "Functional Materials: Processing and Characterization." The same day, a second invited talk was conducted by Dr. Malgorzata Norek (Military University of Technology, Poland). Its title was "Porous Anodic Alumina (PAA) and Synthesis of Functional Nanomaterials Based on PAA."

A second event which took place on 30 June was a meeting of representatives of EDS chapters in Region 8 and SRC for Region 8. Its format was hybrid. The meeting was chaired by Prof. Benjamin Iñiguez and Prof. Lluís F. Marsal who are currently the Vice-Chair and Chair of EDS SRC Region 8, respectively. Several chapter representatives made short presentations about their recent and planned activities and interests. The presenters were officers of the Chapters in Switzerland, Israel, Greece, Italy, Germany, Serbia and Montenegro (including the Student Branch Chapter at the University of Nis), Macedonia (including the Student Branch Chapter at the University of Skopje), Poland and Romania. Several issues related to the management of the chapters were discussed. In addition, Dr. Fetene M. Yigletu (Addis Ababa Institute of Technology, Ethiopia) explained recent activities related to the topics of EDS and the procedure being followed to from an EDS chapter in Ethiopia.

Dr. Ahmed Nejim giving his talk at the Upskilling Course on Flexible and Organic Electronics

SISPAD 2022

The International Conference on Simulation of Semiconductor Processes and Devices (SISPAD 2022) was organized by the University of Granada. It was held in Granada, Spain on 6–8 September 2022, and was chaired by Prof. Francisco Gámiz. This conference is one of the longest-running conferences devoted to technology computer-aided design (TCAD) and advanced modeling of novel semiconductor devices and nano-electronic structures.

Two satellite workshops were offered on the day before the main conference started (5 September): "Modeling and characterization of 2D materials for More than Moore applications," and "Monte Carlo simulation: Beyond Moore's Law." It included four invited talks: "About Electron Transport and Spin Control in Semiconductor Devices" (Siegfried Selberherr, TU-Wien, Austria), "Mono-material TMD-based heterostructures for nanoelectronics applications" (Farzan Gity, Tyndall Institute of Technology, Ireland), "Semiconductor workforce development through immersive simulations on nanoHUB.org" (Gerhard Klimeck, Purdue University, IN, USA), and "Tunneling leakage in ultrashort-channel MOSFETs—From atomistics to continuum modeling" (Raphaël J. Prentki (Nanoacademic Technologies Inc, Canada).

Upskilling Course on Flexible and Organic Electronics in Tarragona (Spain)

On 24–25 November, the ED Spain Chapter, in collaboration with the University Rovira i Virgili, organized in Tarragona an Upskilling Course on Flexible and Organic Electronics. This course was funded by EDS. Its goal was to provide training in flexible/organic electronics to professionals from both academia and industry.

The course included four lectures (each one with a duration of 3 hours) given by top experts in this field, and short talks by Spanish companies presenting their activities in these sectors. The format of this course was hybrid.

Prof. Arokia Nathan (EDS Distinguished Lecturer, Darwin College, University of Cambridge, UK) targeted the "Ultralow power flexible TFT electronics" in a virtual talk. Dr. Ahmed Nejim (Silvaco Europe Ltd. UK) talked about CAD tools for flexible electronics. His lecture included a hands-on session to learn to use Silvaco TCAD tools. Prof. Jordi Carrabina (Autonomous University of Barcelona, Spain) addressed the design of complex organic electronic circuits. Finally, Prof. Eugenio Cantatore (TU-Eindhoven, The Netherlands) conducted a lecture about smart sensors based on flexible electronics.

In addition, the course included short presentations of representatives of companies, and technological centers and platforms in Spain: the companies Nvision, BitBrain and FlexiiiC, the private technological centers EURECAT, LETIAT and Tekniker) and the technological platform 3NEO.

This course was attended by 37 people. More than a half of them are professionals working in companies and technological centers in Spain. There were also PhD students and senior researchers.

Professionals from companies and technological centers received training in four important subjects in the field of flexible electronics: TFTs, organic circuit and systems design, TCAD and EDA tools and smart sensors.

In addition, the course proved to be a very useful forum to start or strengthen interactions between people working in academia and the industry in the flexible electronics sector in Spain.

~Mike Schwarz, Editor

Latin America (Region 9)

ED Colombia Chapter

EDS Colombia INNOVATION MQ 2022

—by Fernando Guarin, Oscar Javier Rodriguez, and Camilo Téllez Villamizar

By 2022, within a reactivation process in the IEEE Colombian Chapter we are heading to put into action the dream of opening opportunities that are attractive to the business sector and that offer opportunities for our professional volunteers to have the opportunity to grow up. This proposal was called EDS INNOVATION MINI-COLLOQUIA, a space where technical knowledge was the gateway for science, industry, and government to converge on the construction of gates and roads to strengthen the technological development of the country.

For this edition, 4 Distinguished Lecturers were selected from Region 9, which in previous interviews expressed interest in participating in this initiative: Edmundo Gutierrez from Mexico, Gilson Wirth from Brazil, Fernando Guarín from the USA, and Felix Palumbo from Argentina. Through an event with different challenges than the traditional ones, it was planned to be divided into 3 parts in which different actors and objectives of the work team could be presented. The first one held 31 October 2022, comprising the first two parts, and the last session on 1 November 2022.

On 31 October, the University of La Sabana began with a day to raise awareness through the speakers who shared their vision of the sector in the region and how their research and projects throughout their careers have a purpose and contribute to society, showing the potential that exists as a society of professional testimony. On the second day, professional conferences were held simultaneously at the Universidad Nacional de Colombia (Bogotá city) and the Universidad de los Andes, both universities with research groups and IEEE EDS student groups that

A group of participants of ED Colombia INNOVATION MQ 2022

One of the presentations of the 12th Seminar on Advanced Electronic Design

seek to strengthen and recognize the work of these units within the strategic plans of each institution.

As complementary activities, the visit opened spaces where strategic meetings were held to project efforts and activities for 2023 and discuss how this can contribute to the growth of the Colombia Section, not only to increase motivation to be part of the Society, but also to create a path that allows both universities that have already embarked on a path in this area and those that see potential for growth in it, to obtain the support of the Section for strengthening or establishing new lines of research.

Around 100 people, students and professionals participated in the whole event. Please, watch the recorded material from EDS Colombia INNOVATION MQ available on YouTube: https://sites.google.com/ieee.org.co/edscol/inicio?authuser=0

ED Puebla Chapter

12th Seminar on Advanced Electronic Design

—by Roberto Stack Murphy A.

The Twelfth Seminar on Advanced Electronic Design was held at INAOE (Puebla, México) on 21–23 September 2022, after two years of being on-hold due to the pandemic. The seminar consisted of 12 talks, by experts in different fields, both from academia and industry, who presented state-of-the-art developments in analog design, high-frequency circuit design, novel device architectures, mathematical approaches to problems in electronics, uses of artificial intelligence in electronics, solar cell optimization, cryogenic sensors for radio-telescope detectors, antennas and rectennas, and uses of technology for humanitarian purposes. In this last field, the use of homotopy was highlighted for seed classification in agricultural endeavors, having an important impact on crop improvement.

The seminar was organized by the Electronics Department of the INAOE, with the collaboration of the Puebla Section I&Ms, CASS, and EDS Chapters. The 75th anniversary of the invention of the bipolar transistor was highlighted throughout the event, as it is one of the most important milestones in the history of electronics.

The seminar was oriented to students, undergrad and graduate, in electronics and akin fields, as well as to established researchers. The average daily attendance was 60 people, all who had a very good opinion of the talks and the seminar overall. The Electronics Department is beginning to organize the 13th Seminar, programmed for September 2023.

ED Puebla Chapter

2022 EDS 75th Anniversary of the Transistor—Mexico (nanoMX2022)

—by Joel Molina-Reyes

On 12–16 December 2022, INAOE held the hybrid (virtual/in-person) celebration regarding the 75th anniversary of the invention of the transistor with up to 135 registered attendees from 22 universities across Mexico, Honduras and Ecuador, as well as 7 technological industries from Mexico, Sweden and USA. This event provided several learning options during a week-long program:

- 18 invited talks by 9 national and 9 foreign speakers
- 6 talks about INAOE's infrastructure for electron device R&D
- 4 workshops on electron device R&D
- 4 talks on the impact of the semiconductor industry in Mexico
- 1 tutorial by Prof. Leon O. Chua
- 1 poster session/contest for students
- 1 joint recruitment session by two major companies in Mexico

EDS 75th Anniversary of the Transistor—Mexico (nanoMX2022)

- 1 panel session "The past, present and future impact of transistor technology in our societies"

We planned truly interesting and easy-to-follow talks so that all of the attendees could see the importance and impact that the invention of the transistor had and still has in our societies, and how its continuous development keeps producing interesting research topics and applications when the dimensions for modern transistors are in the nanoscale. The covered topics were:

- Status of the microelectronics development in Mexico
- History of transistor development in the World and in Mexico
- INAOE infrastructure for development of electron devices
- Physics and technology of electron materials and devices
- CAD tools for developing electron devices and circuits
- Integrated circuit fabrication technology and its applications
- Integrated circuit design (analog, digital and mixed)
- National research centers developing electron devices
- The impact of the semiconductor industry in Mexico
- iSensMEX: development of sensors and electronics
- Academy + Government + Industry + Society

This event was especially important since it marked 75 years of continuous research and development on advanced electron materials and device architectures which by now, have approached nanoscale dimensions and comprise a global effort involving several countries worldwide. We at INAOE, being the first in Latin America enabling the fabrication of CMOS-based integrated circuits (LSI scale) since 1984 and now pursuing the development of a BiCMOS process down to a 0.35 µm technology node, are happy to celebrate this important anniversary hoping that it could motivate younger generations of brilliant engineers and scientists whose work could further benefit all of our societies.

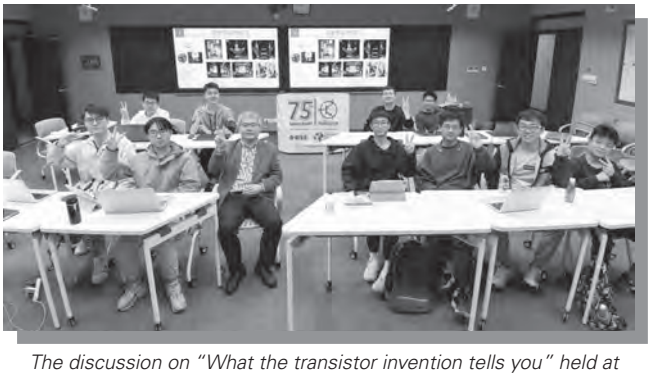
~Joel Molina Reyes, Editor

Asia & Pacific (Region 10)

ED/EP Shanghai Chapter

—by Yu Long Jiang

On 23 November 2022, just one month before the 75th anniversary of the transistor invention, a hot discussion entitled "What the transistor invention tells you" was organized at Fudan University, Shanghai, China. Prof. Yu-Long Jiang, the chair of the ED Shanghai Chapter, first introduced the interesting history of the transistor invention beginning from the era of the vacuum tube. Next, students gave several presentations on what they learned from Bardeen's Nobel lecture and discussed the relationship between bipolar transistors and field-effect transistors, showing a profound understanding of transistor physics, especially the amplification mechanism. All the attendees finally showed respect to the transistor inventors.



The discussion on "What the transistor invention tells you" held at Fudan University, Shanghai, China

ED NCTU Student Branch Chapter

—by Ming-Chun Hong

An invited seminar "*My two cents of pathfinding in memory—Current status and future challenge*" was organized by ED NCTU Student Branch Chapter on 19 December 2022. Dr. Yao-Feng Chang, a Memory Reliability Engineer at Intel, was invited to share his mental journey for memory research and development from school to company. Dr. Chang was an intern at SEMATECH, Austin (ReRAM Program), a research scientist at PrivaTran (a startup company), and a device engineer at Micron Technology (3D SXP project, PCM and selector). He is an expert in the memory field. Not only providing insightful suggestions for the future direction of memory research, he also shared many personal experiences of performing excellent research with the participants. He emphasized the importance of leveraging what you have learned in

The invited seminar "My two cents of pathfinding in memory—Current status and future challenge" by Dr. Yao-Feng Chang. First row, left to right: Prof. Tuo-Hung Hou (NYCU), Dr. Yao-Feng Chang, Dr. I-Ting Wang (NYCU), and Prof. Ying-Chen "Daphne" Chen (NAU)

school when working in the industry. All participants enjoyed Dr. Chang's inspiring talk very much.

ED Kansai Chapter

—by Yuichi Ando

The International Meeting for Future of Electron Devices, Kansai (IMFEDK2022)

IMFEDK2022 was held on 28–30 November 2022 at Kyoto Hall as well as virtually. The presentations covered many latest topics related to electronic devices (Silicon, Compound, Emerging devices, MEMS, circuits, Industrial, etc.). The IMFEDK 2022 included 2 keynote speeches, 13 invited talks, 14 regular speeches and 20 poster presentations. In total, 436 participants joined this three-day meeting.

In the regular session, the IMFEDK committee selected "Multi-Channel Near-Infrared Bandpass Mosaic Filter for Spectral Fundus Imaging," by Ms. Honghao Tang of Nara Institute of Science and Technology to be distinguished with the best paper award. There were also 3 student poster awards selected by the committee: Mr. Masahiro Kaneko (KIT), Mr. S. Kim (Kansai University), and Mr. Kohei Akazawa (OIT).

The best paper award of IMFEDK 2022

During the meeting, we also celebrated the 20th anniversary of EDS Kansai Chapter with the following special events.

- Special session by successive Chapter chairs (Prof. Nozawa, Prof. Ueda, Prof. Taniguchi) and Award Ceremony for Distinguished Service Awards
- Circuit Session in cooperation with IEEE Solid-State Circuits Society (SSCS)
- The award of most-downloaded paper in the last 20 years.

The Audience discussed all the presentations and enjoyed a fruitful time in Autumn Kyoto.

Recent Event

The annual general meeting of the EDS Kansai Chapter was held on 12 January 2023. The new officers of the chapter were elected at the meeting. We also reviewed the Chapter activity results of 2022 and discussed the activity plan for 2023.

ED Japan Joint Chapter

—by Nobuyuki Sugii and Naoki Watanabe

"75th Anniversary of the Transistor" Event at Tokyo

On 16 December 2022, the "75th Anniversary of the Transistor" event was held as an in-person-only gathering at Komaba II Campus, the University of Tokyo. Approximately 60 people participated in the event amid Japan's 8th wave of COVID-19. Firstly, the opening address congratulating the anniversary was given by Dr. Kazunari Ishimaru, IEEE EDS Vice President of Meetings and Conferences, and Prof. Hitoshi Wakabayashi, IEEE EDS BoG Member-at-Large. Then, Prof. Hiroshi Iwai, IEEE EDS Eminent Lecturer, gave a commemorative lecture entitled "Invention of the Transistor 75 years ago; Impact, history and future of nanoelectronics." This lecture brought out not only the 75-year history of the transistor and the evolution of integrated circuit technology but also the inevitability of the advent of semiconductor technology in view of the old history of electrical and electronic technology up to the invention of the transistor.

After the lecture, a workshop on the theme "Thinking about the next 25 years of semiconductors from the standpoint of device engineers, researchers, and educators" was held. This workshop was organized by

"75th Anniversary of the Transistor" event on 16 December, Tokyo

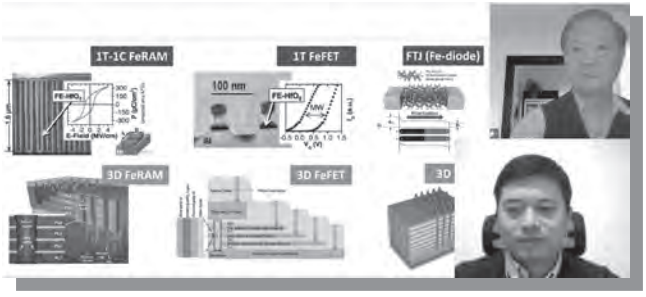
Prof. Masaharu Kobayashi (The University of Tokyo), Prof. Fumihiro Inoue (Yokohama National University), Dr. Kazuyuki Tomida (Rapidus Corp.), and Dr. Hiroyuki Tomita (Tokyo Electron Ltd.). We talked about the attractiveness of the ceaseless evolution of semiconductor technology and high expectations for the future. Many words of encouragement were given to the young researchers who will make the next 25-year history of electron device technology.

The program and announcement of this event are posted on the EDS Japan Joint Chapter's webpage: (https://www.ieee-jp.org/section/tokyo/chapter/ED-15/2022/75th_DL_workshop/75th_DL_workshop.pdf).

ED Taipei Chapter

—by Steve Chung

The ED Taipei Chapter invited Prof. Hangbing Lyu from the Institute of Microelectronics, Chinese Academy of Sciences, to give a talk on 22 December 2022. The lecture entitled "HfO_x based Ferroelectric Materials and Memories" was arranged in a virtual format. The recent discovery of doped HfO_2 ferroelectric material has paved a new way to further scale the ferroelectric memories. Several prototype devices, such as ferroelectric capacitor, switchable diode, tunneling junction, and FeFET, etc., have already shown promising prospects for diverse applications. In this talk, Prof. Lyu introduced first the historical background from materials to devices. Up to now, the HfO_x based ferroelectric materials still have several fundamental problems to be solved, such as the origin of the ferroelectricity, imprint, fatigue and effective method for modulation. Next, the presenter introduced a few methods to solve the above issues. Then, the progress of HfO_x based ferroelectric materials and innovative devices were presented, including one-transistor one-capacitor ferroelectric random-access memory array (1T1C FeRAM), FeFET, Ferroelectric Tunnel Junction (FTJ). The potential applications for (e)DRAM and high-density storage was also addressed. This talk was attended by more than 40 graduate students and professors.



ED Taipei, Invited Talk December 22, 2022 via virtual presentation (Top right- Steve Chung, seminar chair) (Bottom right-Hangbing Lyu, speaker)

~Tuo-Hung (Alex) Hou, Editor

ED Delhi Section Chapter

—by Harsupreet Kaur and Manoj Saxena

To commemorate the centenary celebration of the University of Delhi and the 75th year of the invention of transistors, Department of Electronic Science, University of Delhi South Campus and IEEE EDS Delhi Chapter jointly organized a workshop on "Emerging Devices, Circuits and Systems." It was held 15–18 November 2022. The inaugural talk was delivered by Prof. H. S. Jatana, MIT Pune & IITG EICT (Former Scientist G & Group Head SCL-ISRO) on the topic "Recent Trends and Challenges in Semiconductors and Electronics," followed by these lectures:

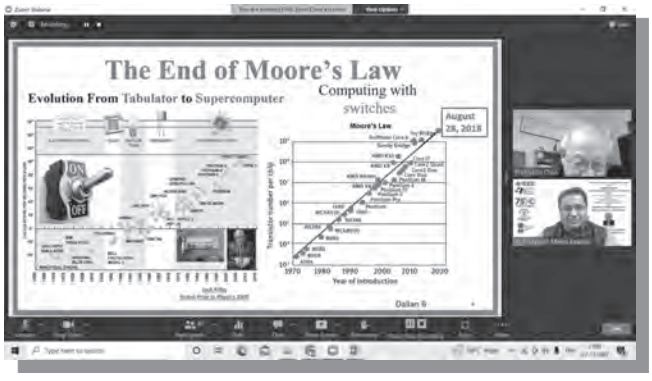
Speakers and participants during the workshop "Emerging Devices, Circuits and Systems," Delhi, 15–18 November 2022

- "Digital VLSI Microfluidic Chip: A Solution to Multi-Dimensional Problematic Issue" by Prof. Subir Kumar Sarkar, Jadavpur University, Kolkata
- Prof. Brinda Bhowmick, NIT Silchar and Prof. Nihar Ranjan Mohapatra on the topics "Application of Emerging TFET Structures as Sensors, Energy Harvesters" and "FinFET based CMOS Technology for SoC Applications: Challenges and Solutions from Analog Perspective" respectively
- Prof. Jai Narayan Tripathi, IIT Jodhpur on "Computational Intelligence for Maintaining Signal/Power Integrity"

- "Few-Layer 2D Semiconductors and Their Heterostructures for Enhanced Photodetection Performance" by Prof. Saurabh Lodha, IIT Mumbai
- Prof. Shree Prakash Tiwari, IIT Jodhpur on "Flexible and Multifunctional Electronic Devices for Green Electronics"
- "Portable Smart Sensors" which was delivered by Prof. Shaibal Mukherjee, IIT Indore

All lectures were very insightful and attracted more than 60 attendees to the workshop.

On 22 November 2022, the Chapter in collaboration with Deen Dayal Upadhyaya College, University of Delhi (under the aegis of DBT Star College Program) organized an EDS Technical Lecture on the topic "Memristor: Workhorse for Post-Moore's and Non—von Neumann Computing" by Prof. Leon Chua, University of California, Berkeley. Seventy-six participants from India, Bangladesh, Taiwan, Italy, Saudi Arabia, United States, United Kingdom and Pakistan attended the engaging talk.



Prof. Chua discussing the evolution of memristors, Delhi, 22 November 2022

On 9–10 November 2022, the International Conference on Electronic and Computational Multidisciplinary Advancement (ICECMA-2022) was organized by the Sri Pratap College under the Cluster University Srinagar. It was an inter-society (internal) event of the IEEE Delhi Section in which the EDS Chapter and the CIS Chapter collaborated and participated. The keynote speaker was Prof. Ramgopal Rao, former Director, IIT Delhi and over 230 participants attended the two day-long conference.

Organizing Committee during the inaugural session of ICECMA-2022

On 2 December 2022, a membership drive program was jointly organized by the Department of Electronics, Sri Venkateswara College and the ED Delhi Chapter for under-graduate students and faculty members. The program was held in a hybrid mode. One of the speakers, Prof. Mridula Gupta apprised the participants about the prospects of revised Electronics curriculum in view of National Education Policy 2020 and about the ED Delhi Chapter and its various activities. Prof. Merylene de Souza, another speaker delivered a lecture on "Defining the Role of Electron Devices Today" and also shared the benefits of IEEE and EDS membership with the participants. The third speaker Dr. P. Susthitha Menon told about her journey right from her IEEE EDS student volunteer days and how the EDS membership helped her in career growth and advancement.

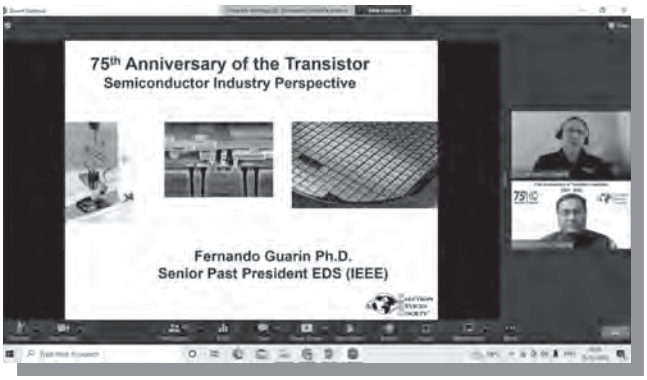
On 12 December 2022, a design competition was organized at Deen Dayal Upadhyaya College in which 57 students of B.Sc(H) Electronics course presented 20 projects.

A virtual Mini-Colloquium (MQ) on "World Transistor Week" was organized as part of the commemoration of "75th Anniversary of Transistor Invention" by the ED Delhi Chapter (New Delhi, India), DBT Star College Status Program, Deen Dayal Upadhyaya College, University of Delhi, and The National Academy of Sciences India—Delhi Chapter. There were 148 delegates from 25 different countries (i.e. Bangladesh, Belgium, Brazil, Canada, China, Colombia, Cyprus, Germany, Greece, India, Indonesia, Italy, Japan, Republic of Korea, Nepal, Netherlands, Nigeria, Peru, Philippines, Russia, Switzerland, Taiwan, United States) who traveled to hear the following lectures:

Participants with the Organizing Committee during the design exhibition on 12 December 2022

- 15 December 2022—Fernando Guarín, Senior Past President of the IEEE Electron Devices Society delivered an IEEE EDS Distinguished Lecture (DL) on "75th Anniversary of the Transistor Semiconductor Industry Perspective"

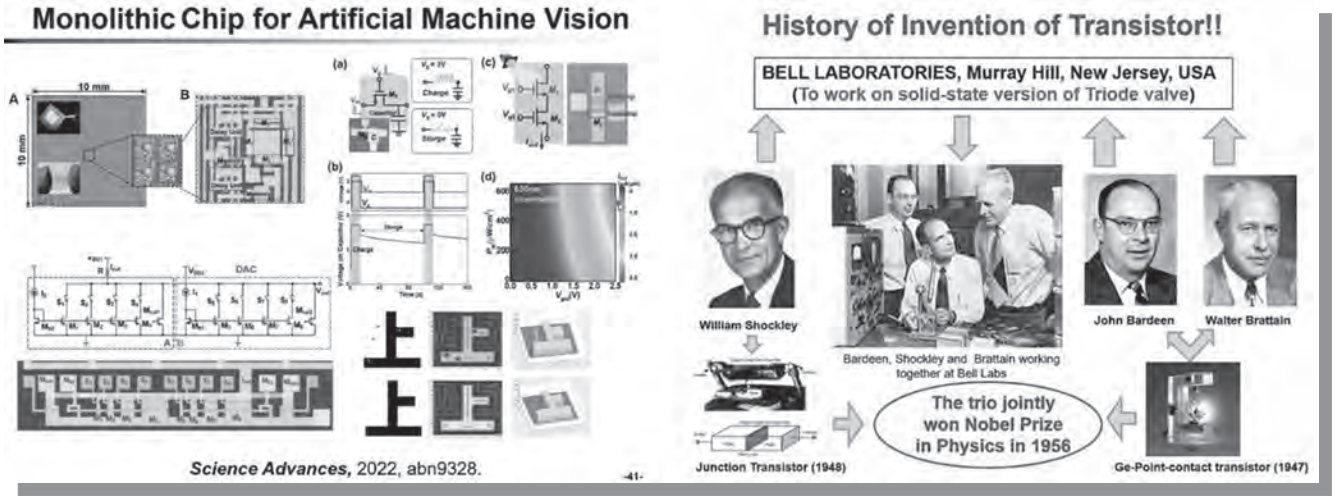
- 16 December 2022—"Transistor Miniaturization—A Bio-inspired Approach" delivered by R. P. Jindal, Past President IEEE Electron Devices Society (2010–2011)
- 19 December 2022—a DL on "Nanotechnologies Enabling Future on-Chip ESD Protection" was delivered by Professor Albert Wang, EDS Past President (2014–2015)
- 21 December 2022—Professor Enrico Sangiorgi, Fellow IEEE, Alma Mater Studiorum Università di Bologna, Italy, delivered a talk on "Wide Bandgap Transistors for Power Applications"



Prof. Guarin discussing perspectives and challenges faced by the semiconductor industry, 15 December 2022

ED IIITDM-Kancheepuram Student Branch Chapter
—by Kumar Prasannajit Pradhan

On 25 October 2022, the Chapter in association with the Department of Electronics and Communication Engineering, Indian Institute of Information Technology Design and Manufacturing (IIITDM) Kancheepuram, organized a Distinguished Lecture (DL) on "Bioinspired in-sensor visual adaptation for accurate perception" by Prof. Yang Chai, Department of Applied Physics, Associate Dean of Faculty of Science (Research), Hong Kong Polytechnic University. Apart from this, on 19–24 October 2022, the Chapter in association with SRM Institute of Science and Technology Kattankulathur organized for the third time its flagship event "Research Opportunities in Semiconductor Materials and Devices (ROSMD-2022)." The event was inaugurated by the keynote talk, delivered by Prof. Parthasarathi Chakrabarti, Director, IIEST Shibpur, on "Semiconductor Crystal Revolution." This was followed by eminent talks of Dr. Kaushik Nayak, IIT Hyderabad on "Exploring Semiconductor Surface States Physics in Diamond Unipolar Devices," Dr. Ravindra Jha, IIT Guwahati on "Room Temperature Operated Resistive Gas Sensors," Dr. Sanjeev Kumar Shrivastava, Chief Operating Officer (I-STEM), CeNSE, IISc Bangalore on "Strengthen the R&D by Sharing Resources and Expertise through I-STEM," Dr. Shubham Sahay, IIT Kanpur on "Reliable and Legitimate Device Characterization Using Commercial TCAD Simulators," Dr. Brijesh Kumar, IIT Roorkee on "Quantum Dot Optoelectronic Devices," Prof. Subhananda Chakrabarti, IIT Bombay on "III-V Compound Semiconductor Materials for Optoelectronic Devices," Prof S. Sundar Kumar Iyer, IIT Kanpur on "Research and Innovation Opportunities in Flexible Electronics," Dr. Avirup Dasgupta, IIT Roorkee on "Machine Learning for Emerging Semiconductor Devices," Dr. Chetan Gupta, Micron Technology (R&D) on "Impact of Technology Scaling on the DRAM Performance and General Parameter Extraction Flow: Optical Modules & their Measurement Techniqu,e, Prof. Subramanian S. Iyer, UCLA on "Study of Charge Transport & Device Physics of Blend Based White Light-Emitting Diode," Prof. Satyabrata Jit, IIT BHU on "Organic Thin Film Solar: An Overview," Dr. T. R. Lenka, NIT Silchar on "Wide-Bandgap Semiconductor Devices for Emerging Nanoelectronics,"



Distinguished Lecture by Prof. Yang Chai delivered on 25 October 2022 and a picture from the inaugural keynote by Prof. Parthasarathi Chakrabarti at ROSMD-2022 on 19–24 October 2022

Dr. Brajesh Rawat on "Electronics Based on 2-D Materials Beyond Graphene," Dr. Jhuma Saha, IIT Gandhinagar on "Integration of III-V and Two-Dimensional (2D) Materials for Optoelectronic Applications."

Dr. K P Pradhan, Faculty Advisor of the Chapter delivered a talk on "Single layer Substitution Doped Graphene FET: From Numerical Model to Extremely Closed-From Region-Wise Model and Application to Synaptic Plasticity." Student Chapter officers had presentations too, with Mr. R. R. Shaik, Vice-Chair of the Chapter delivering a talk on "Ferroelectric Materials Towards Memory and Switching Applications," and Ms. V Rajakumari, Secretary of the Chapter delivering a talk on "Neuromorphic Computing with Emerging Nanoelectronic Devices." The hands-on sessions from the industry Keysight Technology and Impulse Technology on various TCAD tools were also a part of this program.

On 19–23 December 2022, the Chapter in association with the Department of Electronics and Communication Engineering, organized the IEEE EDS sponsored summer school on "Emerging Devices and Circuits to Mimic Biologically Plausible Neuronal Functionalities for Neuromorphic Computing." The inaugural ceremony on 19 December 2022 was a celebration of the 75th Anniversary of the Transistor. On the first day the sessions began with Prof. Saptarshi Das, Penn State University on the topic "Bio-inspired devices for sensing, computing, storage and hardware security based on two-dimensional (2-D) materials." Next, Prof. Jawar Singh, IIT Patna gave a talk on "Devices and circuits for in-memory and brain inspired computing." The third talk on "Brain-inspired computing with memristive devices" was given Prof. Bhaswar Chakrabarti, IIT Madras. On the second day of the school, Prof. Shubham Sahay from IIT Kanpur delivered a talk on "Exploiting neuromorphic networks to predict the future based on the past." Prof. K P Pradhan delivered a talk on "Mimicking of biological behavior through emerging nanoelectronic devices" and Mr. L Chandrasekar delivered a talk on "Single layer substitution doped graphene FET: from numerical model to extremely closed-form region-wise model & application to synaptic plasticity." The hands-on session concerning TCAD implementation of neurons was carried by Ms. V Rajakumari. On the third day of the school, Dr. Sandip Lashkare of IIT Bombay delivered a talk on the topic "Brain inspired in-memory computing," and Dr. Joon-Kyu Han of KAIST Korea gave the talk on "Neuron device based on single transistor latch for neural processing and sensing in neuromorphic hardware." Prof. Tejendra Dixit of IIITDM Kancheepuram delivered a talk on "Optoelectronic Neuromorphic Devices." On the fourth day of the school, Prof. Debanjan Bhowmik gave a lecture on "Spintronic based Neuromorphic Computing," followed by Dr. Jyotismita Mishra of L&T Constructions on "Battery Energy Storage System" and then Dr. Niraj Bagh from Qneuro gave a talk on the topic "Brain-computer interface (BCI) and its applications."

The event concluded with two DLs by Prof. Yogesh Singh Chauhan of IIT Kanpur on "Excelling in academic

Summer school on 19–23 December; participants, cake-cutting during the inaugural ceremony in presence of Prof. K P Pradhan, and DL by Prof. Yogesh Singh Chauhan and Prof. Brajesh Kumar Kaushik

career," and Prof. Brajesh Kumar Kaushik on the topic "Spintronic based devices for neuromorphic computing applications." The event also included presentations by the participants with attractive awards as well as networking sessions.

ED Kanpur Chapter—Uttar Pradesh Section

—by Shubham Sahay

The EDS Chapter of IEEE Uttar Pradesh Section organized on 15–16 December 2022 a Mini-Colloquium with the participation of five Distinguished Lecturers: Prof. Patrick Fay (University of Notre Dame), Dr. Samar K. Saha (Prospicient Devices), Prof. Abhishek Dixit (IIT Delhi), Prof. Anisul Haque (East West University), Prof. Jaydeep Kulkarni (University of Texas at Austin). There were also two technical talks by Prof. Saptarshi Das (Pennsylvania State University) and Prof. Daniele Ielmini (Politecnico di Milano). The speakers gave their talks on topics including bio-inspired sensing, 2D MEMS transistors, hardware security, neural network accelerators, mm-wave transistors, transistor innovations, cryogenic characterization and modeling, bifacial photovoltaics, and compute-in-memory. In addition, the Chapter organized a Distinguished Lecture by Prof. Vikram Dalal (Iowa State University) on perovskite solar cells, a seminar by Prof. Naveen Kadayinti (IIT Dharwad) on sensors, and a workshop to celebrate the "75th Anniversary of Transistors" with technical talks by Prof. Baquer Mazhari of IIT Kanpur and Prof. Saurabh Lodha of IIT Bombay. These events were attended by more than 150 participants from around the world.

ED Nepal Chapter—Uttar Pradesh Section

—by Bhadra Pokharel

The Chapter technically supported a National Conference on Advances in Atmospheric and Materials Science, organized by the Department of Physics, Amrit Science Campus, Tribhuvan University, Kathmandu, Nepal. The program was co-supported by the International Science Program, Uppsala University, Sweden, the Nepal Physical Society (NPS), and the Nepalese Society for Women in Physics. The Conference was attended by about 68 participants from different parts of Nepal; among them were 10 IEEE members.

National Conference on Advances in Atmospheric and Materials Science, Participants and Organizing Committee members outside the conference hall

Prof. Dr. Lok Narayan Jha, former Head of the Central Department of Physics and Senior Physicist of Nepal, inaugurated the Conference. He expressed his views on research and teaching. Prof. Dr. Sekhar Gurung, Prof. Dr. Pradeep Kumar Bhattarai, and Prof. Dr. Nilam Shrestha (NPS President) expressed their views and wished the program success. Prof. Dr. Narayan Prasad Chapagain (faculty, Department of Physics, Amrit Campus) gave the welcome address; Pitamber Shrestha, coordinator, MSc Physics Program, spoke about the Conference; and Dr. Lok Bahadur Baral (Campus Chief), chairman of this program, presented his opinion about the program and closed the inaugural session. There were two keynote lectures: by Prof. Dr. Bhadra Pokharel, past president of the ED Nepal Chapter, and by Prof. Dr. Ram Prasad Regmi, faculty at Tribhuvan University. There were also two invited talks by Dr. Sanju Shrestha, Treasurer of the ED Nepal Chapter, and Dr. Hom Bahadur Baniya, faculty at Tribhuvan University, 21 contributory oral presentations, and 13 poster presentations. On the first day of the Conference, there were 4 scientific sessions. The first session was chaired by Prof. Dr. Neelam Shrestha, the second one was chaired by Prof. Dr. Rameshwor Adhikari, the third one was chaired by Prof. Dr. Narayan Adhikari, and the last one was chaired by Prof. Dr. Rajendra Parajuli. There were also four sessions on the second day of the Conference. The first session was chaired by Prof. Dr. Khem Narayan Poudel, the second one was chaired by Prof. Dr. Hari Prasad Lamichhane, the third one was chaired by Prof. Dr. Narayan Prasad Chapagain, and the fourth one was chaired by Prof. Dr. Indra Bahadur Karki. On the second day of the Conference after the oral talks, a poster session was held chaired by Dr. Manoj Kumar Chaudhary. The closing session was chaired by Prof. Dr. Rajendra Parajuli, who thanked all those who helped make the event a

Workshop to celebrate the 75th anniversary of Transistors by ED Kanpur Chapter

success. Mr. Ramji Karki and Mr. Jhulan Powrel expressed their views about the conference.

ED Calcutta University of Technology Student Branch Chapter

—by Koyel Mukherjee, Apabrita Sengupta, and Soumya Pandit

In order to celebrate the 75th anniversary of the transistor, the Chapter organized a one-day DL that was held on 28 November 2022 at the Institute of Radio Physics and Electronics. The EDS Distinguished Lecturer, Dr. Samar Kumar Saha, delivered his talk on the topic of "Birth and journey of evolution of the transistor till date." This was followed by a technical talk delivered by Prof. P.K. Basu, former professor of the Institute of Radio Physics and Electronics, University of Calcutta. Prof. Basu delivered his talk on the history of the transistor and elaborated the seminal works done by Sir J.C.Bose at Kolkata, India, in the area of radio waves in the microwave spectrum and who was the first to use semiconductor junctions to detect radio waves. Almost 75 under-graduate, post-graduate students, plus research scholars of both the technology and science departments participated in the event.

Participants of DLheld in the J.N.Bhar Auditorium of the Institute of Radio Physics and Electronics, 28 November 2022

~Soumya Pandit, Editor

EDS Mini Colloquium on 75th Anniversary of the Transistor

—by Bejoy Sikder

The invention of the transistor was the greatest event in the history of semiconductor devices and industry. The remarkable phenomenon took place in the late December of 1947 and now the use of transistors has revolutionized modern electronic devices. To commemorate the 75 years of this historical event, IEEE ED/SSCS Bangladesh Joint Chapter organized three Distinguished Lectures (DL) under the title "EDS Mini Colloquium on 75th Anniversary of the Transistor".

The first of the three DLs was held online on 24 November 2022 and the speaker was Prof. Marcelo Antonio Pavanello, Electrical Engineering Department, Centro Universitario FEI Sao Bernardo do Campo, Brazil. In the lecture titled "Performance of Silicon-on-Insulator Nanowire and Nanosheet MOSFETs in a Wide Temperature Range" he explained how nanowire and nanosheet MOSFETs can enable the continuation of MOSFET scaling which is difficult for conventional transistors due to undesirable short-channel effects. Professor Marcelo delineated the performance of such single-level nanowires and nanosheet MOSFETs along with their analytical modeling and their capabilities to operate in a wide range of temperatures from 600 K down to the cryogenic range. The talk was attended by 45 people, among them 18 were IEEE members.

The second online DL "Memristor-based Energy-Efficient Computing-in-Memory Technology" was presented on 1 December 2022 by Professor Dr. Huaqiang Wu, Dean of School of Integrated Circuits, Tsinghua University. In this lecture, Prof. Wu explained the opportunities and prospects of memristor-based computing-in-memory (CIM) technology to overcome the limitations of the conventional Si CMOS based von Neumann computing architecture. He introduced the audience to the operation principles, material exploration, large-scale device integration along with the recent progress of memristor-based CIM technologies. Among the 25 attendees of this lecture, 13 were IEEE members.

The last of these DLs was held in-person at the department of Electrical and Electronic Engineering, Bangladesh University of Engineering and Technology (BUET) on 19 December 2022. Dr. Anisul Haque, Professor, Department of Electrical and Electronic Engineering, East West University, Bangladesh presented the lecture titled "Journey of the transistor". In the birth-month of the transistor, he narrated the history of the development of the first working transistor. The lecture continued describing the early researchers and entrepreneurs who played a pivotal role in the development of the modern semiconductor industry and its hub: the Silicon Valley. The talk concluded by giving the attendees a perspective on the future of transistors. A cake was cut after the end of the lecture to celebrate the 75th anniversary of the transistor. A total of 26 people attended this event and among them 10 were IEEE members. All the DLs were followed by a series of insightful and prospective questions from the audience.

The DL by Dr. Anisul Haque at BUET on 19 December 2022

EDS MEETINGS CALENDAR

The complete EDS Calendar can be found at our web site: http://eds.ieee.org. Please visit.

2023 34th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC)	01 May – 04 May 2023	Saratoga Springs, NY
2023 IEEE International Memory Workshop (IMW)	21 May – 24 May 2023	Monterey, CA
2023 IEEE International Interconnect Technology Conference (IITC) and IEEE Materials for Advanced Metallization Conference (MAM)(IITC/MAM)	22 May – 25 May 2023	Dresden, Germany
2023 35th International Symposium on Power Semiconductor Devices and ICs (ISPSD)	28 May – 01 Jun 2023	Hong Kong
2023 Silicon Nanoelectronics Workshop (SNW)	11 Jun – 12 Jun 2023	Kyoto, Japan
2023 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)	11 Jun – 13 Jun 2023	San Diego, CA
2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)	11 Jun – 16 Jun 2023	Kyoto, Japan
2023 Device Research Conference (DRC)	25 Jun – 28 Jun 2023	Santa Barbara, CA
2023 China Semiconductor Technology International Conference (CSTIC)	26 Jun – 27 Jun 2023	Shanghai, China
2023 IEEE Latin American Electron Devices Conference (LAEDC)	03 Jul – 05 Jul 2023	Puebla, Colombia

2023 30th International Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD)	04 Jul – 07 Jul 2023	Kyoto, Japan
2023 IEEE 36th International Vacuum Nanoelectronics Conference (IVNC)	10 Jul -14 Jul 2023	
2023 IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)	23 Jul – 26 Jul 2023	Pulau Pinang, Malaysia
2023 IEEE International Flexible Electronics Technology Conference (IFETC)	13 Aug – 16 Aug 2023	San Jose, CA
2023 16th UK-Europe-China Workshop on Millimetre Waves and Terahertz Technologies (UCMMT)	31 Aug – 03 Sept 2023	Guangzhou, China
2023 IEEE International Conference on Quantum Computing and Engineering (QCE)	17 Sept – 22 Sept 2023	Bellevue, WA
2023 18th European Microwave Integrated Circuits Conference (EuMIC)	18 Sept – 19 Sept 2023	Berlin, Germany
2023 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)	26 Sept – 29 Sept 2023	Kobe, Japan
2023 45th Annual EOS/ESD Symposium (EOS/ESD)	01 Oct - -6 Oct 2023	Riverside, CA
2023 IEEE International Integrated Reliability Workshop (IIRW)	08 Oct – 12 Oct 2023	South Lake Tahoe, CA
2023 International Semiconductor Conference (CAS)	11 Oct – 13 Oct 2023	Sinaia, Romania
2023 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)	14 Oct – 18 Oct 2023	Monterey, CA
2023 IEEE 33rd International Conference on Microelectronics (MIEL)	16 Oct – 18 Oct 2023	Nis, Serbia

2023 IEEE/ACM International Conference on Computer Aided Design (ICCAD)	28 Oct – 02 Nov 2023	San Francisco, CA
2023 Middle East and North Africa Solar Conference (MENA-SC)	15 Nov – 18 Nov 2023	Dubai, United Arab Emirates
2023 IEEE 10th Workshop on Wide Bandgap Power Devices & Applications (WiPDA)	04 Dec – 06 Dec 2023	Charlotte, NC
2023 International Electron Devices Meeting (IEDM)	09 Dec – 13 Dec 2023	San Francisco, CA
2023 IEEE 54th Semiconductor Interface Specialists Conference (SISC)	13 Dec – 16 Dec 2023	San Diego, CA

Did You Know…

IEEE and EDS provide temporary Open Access to top papers from IEEE Electron Device Letters (*EDL*) and *IEEE Journal on Microelectromechanial Systems* (*J-MEMS*)?

Every month, EDL Editors select a small number of particularly remarkable articles as **Editors' Picks.** These are highlighted on the issue cover and enjoy temporary (one month) Open Access. One of these articles is further selected as Cover Article and prominently featured in its main cover graphics. Visit the EDS website for links to the current **EDL Editors' Picks.**

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IEEE Electron Devices Magazine will be Launched Soon!

I am happy to inform you that the first issue of the **IEEE Electron Devices Magazine (ED-M)** will be published in June 2023. ED-M is the new initiative of the IEEE Electron Devices Society. It will be issued by IEEE with the full financial support of our Society.

Joachim N. Burghartz
Founding Editor-in-Chief

The Magazine focuses on the publication of peer-reviewed tutorial and survey papers related to the wider field of electron devices and their applications. It may also include articles dealing with environmental, societal, and humanitarian issues. Besides, columns by renowned experts will be included, dealing with educational, research, industrial and open topics and sharing personal opinions in a compact format. Also, news related to the Electron Devices Society will be displayed in the Magazine, including the President's Column and conference reports.

The IEEE Electron Devices Magazine will be published quarterly, with issues appearing in March, June, September and December. Most issues of the Magazine will include a "focus section," that will feature topical articles invited by guest editors. Each issue will be displayed in light of the given focus topic. The nearest ones' leading themes will be:

- June 2023: 75th Anniversary of the Transistor
- September 2023: Neuromorphic Computing
- December 2023: Semiconductor Manufacturing
- March 2024: Quantum Computing (tentatively)

In addition to the invited topical articles, contributed technical articles on all topics related to the field of electron devices will be presented. Their Authors are advised to try to match their submissions to the Editorial Calendar, though this is not a strict requirement.

I do hope that you, the readers of the Magazine, will find its contents interesting and may vividly react to them in the letters to the Editor (ED-M-editor@ieee.org). I also strongly encourage you to contribute to the Magazine with your articles and personal opinions.

More information about ED-M, including information about paper submission, indexing, subscription, access, can be found at: https://eds.ieee.org/publications/ieee-electron-devices-magazine

Prof. Dr. Joachim N. Burghartz
Founding Editor-in-Chief
ED-M-editor@ieee.org

EDS Vision, Mission and Field of Interest Statements

Vision Statement
Promoting excellence in the field of electron devices for the benefit of humanity.

Mission Statement
To foster professional growth of its members by satisfying their needs for easy access to and exchange of technical information, publishing, education, and technical recognition and enhancing public visibility in the field of Electron Devices.

EDS Field of Interest
The EDS field-of-interest includes all electron and ion based devices, in their classical or quantum states, using environments and materials in their lowest to highest conducting phase, in simple or engineered assembly, interacting with and delivering photo-electronic, electro-magnetic, electromechanical, electro-thermal, and bio-electronic signals. The Society sponsors and reports on education, research, development and manufacturing aspects and is involved in science, theory, engineering, experimentation, simulation, modeling, design, fabrication, interconnection, reliability of such devices and their applications.