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Technical Briefs

System and High-Volume-Manufacturing Driven More Moore Scaling Roadmap

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1. Introduction

Scaling device features by approximately 30% in each new technology generation supported Moore's Law doubling the number of transistors every 2-years for decades while also improving system performance by concurrently increasing transistor drive current and reducing operating voltage. This combination allowed introduction of new functions in innovative System-On-Chip (SoC) products with better performance and lower cost. The progress of technology scaling has been measured by monitoring PPAC (Performance-Power-Area-Cost) improvements, typically happening with any new technology introduction with a cadence of 2–3 years. However, pure geometric scaling does not provide any longer the necessary PPAC improvements at the system level due to several reasons:

1) limits of practical power dissipation were reached around the middle of the previous decade and this constraint imposed a maximum useable frequency of 5–6 GHz,
2) ideal geometric scaling introduces increasing levels of parasitics that adversely reduce performance,
3) cost of scaling is increasing faster than in the past due to lithographic limitations demanding multiple exposure per layer and therefore making final products very costly,

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System and High-Volume-Manufacturing Driven More Moore Scaling Roadmap

(continued from page 1)

4) there is an increasing imbalance and disconnect between the performance of devices at the die level and the performance requirements of the overall system (e.g. memory bandwidth bottleneck) that creates a significant burden to further enhance system integration and performance. Therefore, for all the above reasons there is a need to concurrently consider overall system and economics trade-offs and introduce items that can provide better system building blocks at the die level other than ideal geometrical scaling.

The ITRS established in 1998 was mainly aimed at transistor density and performance improvements by means of scaling but in this decade the roadmap projections have been re-focused on system constraints; this consideration led to the restructured International Roadmap for Devices andSystems (IRDS). This collection of documents provides the roadmap for logic devices, on-chip interconnect, and memory devices driven by feasible manufacturability routes and system integration requirements.

2. Market Drivers of More Moore Scaling and Roadmap Process

System considerations and cost optimization requirements have driven the need for a unified technology platform where high-performance digital logic needs to enable server applications are considered and also provide support for low power needs to enable mobile computing for the edge applications. Both requirements must be kept into account with equivalent relevance to allow the electronics industry to continue growing at historical (or better) rates. Therefore the mission of the IRDS More Moore (MM) IFT chapter is to provide physical, electrical, and reliability requirements for a unified logic and memory technology platform to sustain power, performance, area, cost (PPAC) "scaling guidelines" for mobile and cloud applications over a time horizon of 15 years for Mainstream/High-Volume Manufacturing (HVM) [1]. Such technology platform identifies the main technology drivers and provides the enabling tools for the following application (Fig. 1):

- Mobile—5G/6G, hetero integration, edge computing, graphics, extreme reality (VR/AR)
- Machine learning at edge and cloud
- High-performance energy-efficient graphics/sensing
- Data/micro servers—cache/buffer memory and accelerator integration, IO, high-performance interposers
- Ultra-low power computing exploiting non-volatility.

More Moore (MM) roadmap guidelines identify technology enablement items for improving the system performance, power, and area in a timely manner; meeting a mobile product cadence of one year, maybe even six months, while providing a scalable product platform for the servers, which must be surviving 10 years, for multiple cloud applications. The first step in the roadmap process is to identify the ground rules and their inherent limits set by the unit process modules, devices, and the impact of any parasitics on performance. The second step is to describe the standard cell scaling parameters and how to further tighten key design rules by means of Design Technology Co-Optimization (DTCO). The third step is then the identification of device architecture and interconnects technology drivers to satisfy System-On-Chip requirements. Finally, optimization of all the above elements brings performance and careful energy management together to collectively enable cost effective system scaling. Since transistor technology alone is no longer sufficient to satisfy the requirements for enhanced memory bandwidth, IO, and outside connectivity demanded by system driven requirements, it is necessary to introduce new 2.5D/3D integration schemes. These integration technologies enable the effective adoption of the needed memory with sufficient bandwidth, increased capacity, and latency parameters required for the various applications listed above. As the final step of this optimization process the various available enablement items are carefully analyzed and

Fig. 1. Two pillars of More Moore application drivers.

the essential items are down-selected to meet product delivery timeline while limiting process complexity to the most relevant innovative module processes to be added to the device technology platform in High-Volume-Manufacturing (HVM).

3. Ground Rules

Determination of ground rules is a critical step in defining both the unit process modules and a realistic economy of scaling [2]. It is of paramount importance to select a set of design ground rules that are as aggressive as possible and yet consistent with high yields in the High-Volume-Manufacturing (HVM) process to assure economic product viability. Lithography technology remains the key process step enabling reduction of device features. However, the limits of single exposure lithography were reached more than a decade ago and additional process steps had to be introduced to maintain scaling of device features by around 30% per technology generation. The most viable solution to achieve the required scaling goal through the years has resulted exposing multiple times any layers that exceeded the lithography capabilities. In few words for illustrative purposes let's consider exposing twice a set of lines and spaces; the first time the set of lines and spaces is exposed in the resist and then the same pattern is re-exposed a second time but offset by half pitch. The outcome is a set of interdigitized lines spaced at half the distance of the original ones. Under practical conditions more complicated sequences and mask combinations are required. This represents a viable engineering approach although it comes with the penalty of doubling or even quadrupling the lithography cost for any layer produced with this process method. Due to the rising process complexity associated with the multiple patterning it is important to carefully allocate the lithography technology to be used with each layer. The feature size that can be produced by any lithography tool is largely determined by the exposure wavelength. This means that design ground rules are determined by keeping into consideration the capability limits of the available lithography tool. For instance 76–80 nm metal pitch can be obtained by using 193i immersion lithography tools (193 nm exposure wavelength) with double or even quadruple exposures. Similarly, 28–30 nm metal pitch can be presently obtained by using EUV tools (13.5 nm) with a single exposure, but 18 nm pitch or lower may require double EUV exposure. These examples show the trade-off between exposure tool selection and design rules. Due to the much lower exposure wavelength of EUV it is possible to achieve much smaller ground rules for the EUV layers with much better tolerance margins as compared to double or quadruple exposure using tools exposing with 193nm wavelength. However, the selection of the lithography tool to be used by layer is not so obvious because careful cost considerations must be done since any exposure done by the EUV tool is as much as 3 times more expensive than the one of a 193i tool. Another careful consideration on how aggressively ground rules are to be scaled is due to considerations about the increased contributions of parasitics to the total performance. In summary, overlay and unnecessary scaling may bring diminishing returns on both transistor performance and also unnecessarily increasing power dissipation. This becomes the case even though area scaling may indeed reduce interconnects parasitics due to a reduction of wirelengths. All these trade-offs must be kept into careful consideration in the complex selection of ground rules (Fig. 2). 2D scaling is expected to eventually reach practical limits around the year 2030 when full 3D stacking technology is expected to become mainstream.

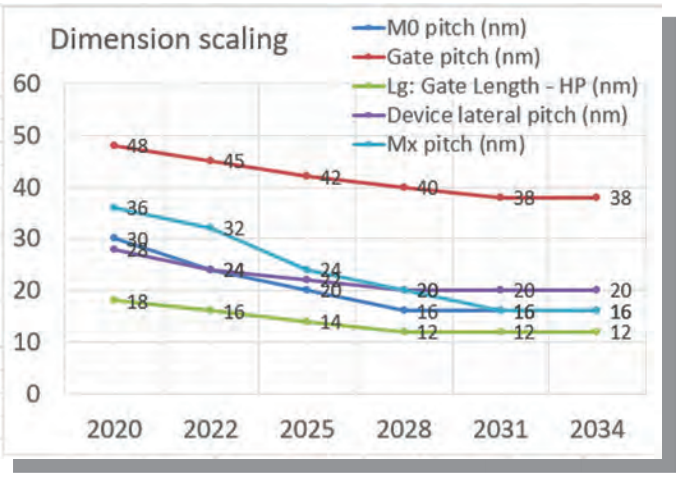


Fig. 2. Evolution of ground rules.

Correcting Nonsense Node Naming

The ITRS had defined technology nodes as the half-pitch of the smallest metal layer in any IC in the 90s. However, in the past 10 years several companies have redefined their own technology nodes by using much smaller numbers than the official definition. This method of naming nodes has by now lost any credibility since there is no longer any relation between the node name and any of the dimensions on the actual ICs that are being produced nowadays. For instance, several companies are talking about 7 nm technology node while in reality it should be named as 18 nm technology node corresponding to half of the 36 nm minimal metal pitch in the actual ICs.

It is important to note that there is no correlation between the naming convention (e.g. 7 nm, 5 nm technology) from different foundries and integrated device manufacturers (IDMs) and the technology capabilities in line with the PPAC requirements.

To further clarify this point the IRDS chose to name the by explicitly putting the key parameters used in defining the ground rules in the technology naming convention, these are: GxxMxxTx where Gxx represents the contacted gate pitch, Mxx represents the tightest metal pitch in nm and Tx represents the number of stacked tiers making up a 3D integrated transistor circuits. This notation illustrates the technology pitch scaling capability as well as 3D stacking capability [3]. On top of pitch scaling there are other elements of relevance such as cell height, Fin depopulation, DTCO constructs, 3D integration, etc. that define the target area scaling (gates/mm^2), which will be explained in the next paragraph.

For sake of completeness the artificially defined industry technology nodes are indicated as a reference in the roadmap.

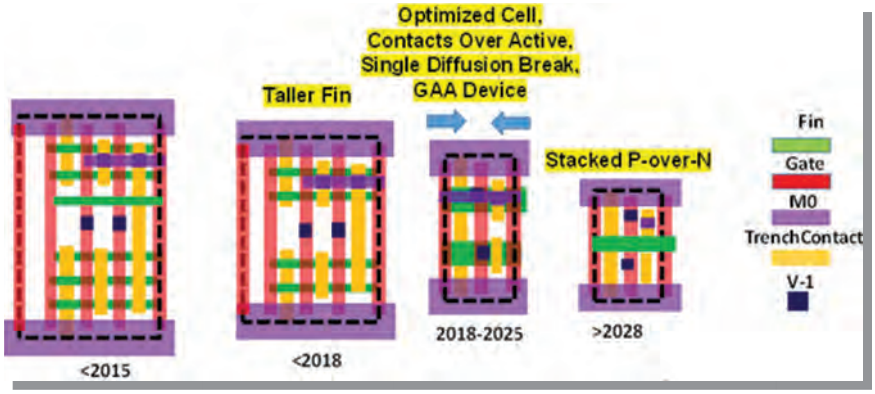


Fig. 3. DTCO-enhanced standard cell scaling evolution.

4. Standard Cell Architecture

As mentioned earlier design rules cannot be aggressively scaled down like in the past and therefore it is necessary to complement their role in reducing the area of the basic cell with novel layout techniques that allow to achieve the desired area reduction goal as well as producing more manufacturable design rules. This methodology is called Design Technology Co-Optimization (DTCO). The basic approach of DTCO consists in reducing the standard cell height and width by combining many design elements enabled by the technology. For instance, reducing the number of active devices in the cell and combining a limited scaling of the width of active devices as well as carefully applying a limited scaling of many secondary rules such as tip-to-tip, tip extension, PMOS-NMOS separation, and minimum metal area rules produce a drastic reduction of the cell height with substantial area savings. Recently further cell height reduction has been demonstrated by placing contact-over-active devices [4]. It is expected that in 2028 PMOS and NMOS devices could be stacked on top of each other allowing a further cell area reduction. This trend in standard cell height and width scaling is illustrated in Fig. 3 with the density scaling of standard cell shown in Fig. 4.

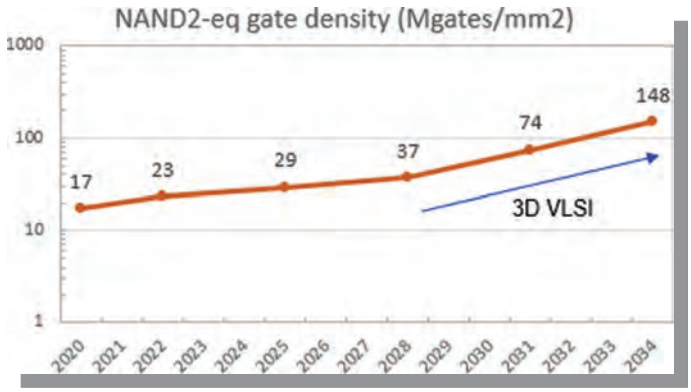


Fig. 4. Standard cell density scaling.

5. Device Structures

In the next 15 years it is forecasted that three phases of scaling will occur (Fig. 5): 1) Extending improvements of FinFET, 2) Transition to gate-all-around (GAA) devices, 3) Sequential integration (3DVLSI) of stacked devices. FinFET has continued to remain the key transistor architecture since 2011 and it will continue to remain the transistor architecture of choice until 2025 or so thanks to continuous electrostatics, drive current and cell architecture improvements such as increasing the Fin height and reducing the width of Fin to keep electrostatics under control [5][6].

In order to continue increasing performance and density it is necessary to increase the transistor output current and this requires improving the electrostatic control of the channel region while also reducing transistor footprint to increase layout density. To accomplish these tasks, it is necessary to make a transition from FinFET to Gate All Around (GAA) structures such as circular tubes or lateral nanosheets; the GAA transition is expected to gradually occur during the 2022–2025 period. Such transition will require the introduction of new process modules like channel release for the build-up of stacked channels, substantial improvements in inner spacer to reduce the effect of parasitic capacitance, increased bottom channel isolation to reduce parasitics, and enhanced replacement-metal-gate modules to provide multiple threshold voltages as the spacing between the nanosheets is reduced. Lateral GAA structure would eventually evolve into full 3D forms by incorporating much thinner channel structures when finally stacking NMOS over PMOS architecture will be adopted.

Use of Si channel material places a lower limit to reducing channel thickness as required when scaling the gate length to 10–12 nm because of a conflicting need for thicker Si nanosheets to avoid surface scattering. The adoption of 2D channel materials will bring an opportunity for further reduction of gate lengths since the conduction mechanism is no longer affected by surface phenomena. The adoption of 2D materials will enable much thinner channels because it will eliminate the effect of dangling bonds at the interface between the conducting channel and the surrounding insulation [7]. Further reduction of capacitance is possible because of gate length reduction and lower dielectric constant of channel materials. However, 300mm manufacturability, 2D material synthesis, and contact engineering will still remain sources of critical challenges to be solved before adopting 2D transistor structures as the foundation of device platform beyond 2028.

Key dimensions for the logic device scaling are shown in Fig. 6. System-on-chip built with GAA devices

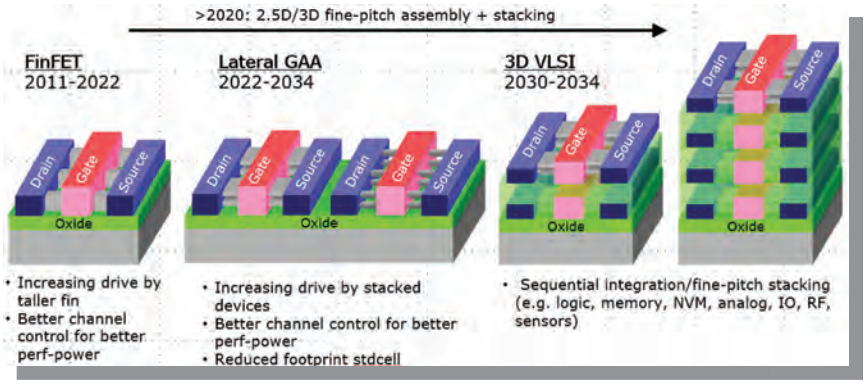


Fig. 5. Evolution of device structures.

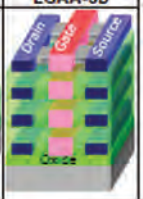
YEAR OF PRODUCTION	2020	2022	2025	2028	2031	2034
	G48M36	G45M24	G42M20	G40M16	G38M16T2	G38M16T4
Logic industry "Node Range" Labeling (nm)	"5"	"3"	"2.1"	"1.5"	"1.0 eq"	"0.7 eq"
IDM-Foundry node labeling	i7-f5	i5-f3	i3-f2.1	i2.1-f1.5	i1.5e-f1.0e	i1.0e-f0.7e
Logic device structure options	FinFET	finFET LGAA	LGAA	LGAA	LGAA-3D	LGAA-3D
Mainstream device for logic	finFET	finFET	LGAA	LGAA	LGAA-3D	LGAA-3D
						
LOGIC DEVICE GROUND RULES						
Mx pitch (nm)	36	32	24	20	16	16
M1 pitch (nm)	32	30	21	20	19	19
M0 pitch (nm)	30	24	20	16	16	16
Gate pitch (nm)	48	45	42	40	38	38
L_g: Gate Length - HP (nm)	18	16	14	12	12	12
Lg: Gate Length - HD (nm)	20	18	14	12	12	12
Channel overlap ratio - two-sided	0.20	0.20	0.20	0.20	0.20	0.20
Spacer width (nm)	7	6	5	4	4	4
Contact CD (nm) - finFET, LGAA	16	17	18	20	18	18
Contact CD (nm) - VGAA						
Device architecture key ground rules						
FinFET pitch (nm)	28.0	24.0				
FinFET Fin width (nm)	7.0	6.0				
FinFET Fin height (nm)	50	60				
Footprint drive efficiency - finFET	3.82	5.25				
Lateral GAA lateral pitch (nm)			22.0	20.0	20.0	20.0
Lateral GAA vertical pitch (nm)			18.0	16.0	14.0	14.0
Lateral GAA (nanosheet) thickness (nm)			7.0	6.0	5.0	5.0
Number of vertically stacked nanosheets			3	3	4	4
LGAA width (nm) - HP			30	20	15	10
LGAA width (nm) - HD			20	11	6	6
LGAA width (nm) - SRAM			7	6	6	6
LGAA total height (nm)			53	48	57	57
Footprint drive efficiency - lateral GAA - HP			4.80	4.59	5.52	5.00
Device effective width (nm) - HP	107.0	126.0	192.0	156.0	160.0	120.0
Device effective width (nm) - HD	107.0	126.0	132.0	102.0	88.0	88.0
Device lateral pitch (nm)	28	24	22	20	20	20
Device height (nm)	50.0	60.0	53.0	48.0	57.0	57.0
Device width (nm) - HP	7	6	25	20	15	10
Device width (nm) - HD	7	6	15	11	6	6
Device width (nm) - SRAM	7	6	7	6	6	6

Fig. 6. Key dimensions for the logic technology scaling.

are expected to utilize several GAA device types. This implies that a typical SoC designer will need to select upfront the type of devices needed based on their threshold voltage and nanosheet widths prior to fabrication. Below are examples of some of the anticipated device choices in 2025:

1) High-density SRAM will need transistors with ultra-low leakage of about 7 nm width,
2) High-density designs will need transistors with moderate leakage of about 15 nm width,
3) High-performance design will tolerate high-leakage transistors of about 25 nm width.

6. 2.5D/3D Integration

Realization of 2D device technologies will enable energy-efficient performance computing, but this will require an architectural adjustment to achieve optimal results. Under these conditions it will be necessary to move the data from the computing logic to the high-capacity memories with high-bandwidth connections. 2.5D systems have already demonstrated to be very efficient in the generations of high-bandwidth memory (HBM) chipsets where stacked DRAM memory cubes (e.g. 128 Gbit/cube) have been put side-by-side in a package with the computing logic die assembled on the same interposer. This technology has demonstrated 64 GB memory with a bandwidth of 2 TB at 512 GB/sec in a single package [7]. In order to keep increasing HBM performance and increasing the total amount of memory in the same package, there will be a need to implement more complex 3D architectures. It is expected that in the next 2–5 years, work-level memory (e.g. 3D SRAM and/or DRAM on top of logic) will be stacked together on logic to provide a low-latency and large bandwidth communication capability between memory and logic.

Most of 3D stacking technology development focuses on bringing high-capacity memory closer to logic because from a performance point of view it is more advantageous than low-capacity embedded memories and it also offers a better performing bus/IO structure by taking advantage of the better interconnect capability associated with the interposer. In the future it is expected that the interposer technology will allow to place various types of chipsets, (i.e., not limited to memory), in the same package and its fabric would also include voltage regulators, decoupling capacitances, buffers, IO, ESD, etc. There are various implementation routes to enable optimal 3D stacked components. As the combination of 3D stacked components will keep on increasing and as more interconnect routes can be placed on the interposer it will be possible to create larger and larger high performance systems in a single package [9].

Die-to-wafer stacking technologies will continue to employ μBump stacking and/or hybrid/dielectric bonding. Either of those technologies requires Thru-Silicon-Via (TSV) in one or more of the tiers to connect the individual dice stacked onto top of the interposer. Integration drivers for this technology are high-bandwidth and high-density memories stacked on logic die. Furthermore, heterogeneous stacking will be allowing integration of new functions and substantial reduction of form factor. However, design/architecture partitioning, thermal management; and IO and power distribution allocation across the design/system network will still present very difficult challenges. Typical pitch of μBumps on these technologies is presently around 40 μm, enabling 625 vias/mm^2, while Cu pad (in hybrid bonding) pitch is around 10 μm, enabling 10,000 vias/mm^2.

Wafer-to-wafer stacking is used in applications where there are no issues related to form factor mismatch. This type of stacking was successfully used in image sensors and HBM (stacked DRAM) applications. In this case μBump pitch is around 40 μm while Cu pad (in hybrid bonding) is around 1–2 μm. Eventually it is expected that this technology could evolve onto the fine-grain and regular fabric suitable for logic-on-logic applications (potentially equalizing the size of different-tier dies) if regular-fabric data-flow micro-architectures will prove successful in the industry.

The technology of sequential integration of multiple tiers of devices relies on the fabricating of subsequent tier using a thermal budget lower than the one used to fabricate any of the underlying tiers. Inter-tier via pitch can be of the order of 50–300 nm in this technology, enabling 100 M vias/mm^2 [10]. It is important to point out that using this integration scheme it becomes possible to independently optimize specific devices in each tier (e.g., threshold voltage, channel material, raised source/drain, strain, etc). Although this technology has many advantages several challenges still lay ahead. Selection of layer-by-layer thermal budgets, integration methodology of high-aspect-ratio vias, selection of cell topology and allocation by layer of interconnection partitioning between fine, median and looser pitch in each tier (e.g. connections between PMOS-tier and NMOS-tier, between standard cells, between standard cell and bitcell) remains a formidable planning challenge. In order to extract the maximum value from this multi-tier architecture it is advisable to select an approach favoring regularity organized layout; this arrangement is ideal to optimize any highly parallel computation and also to accommodate for the fastest memory access while also supporting a very large memory capacity. As time goes by this integrated architecturally driven die layout will make data-centric computing highly successful. It is also possible that this approach may eventually evolve into more general-purpose computing [11]. An example of 3D micro-architecture employing a highly regular layout is shown in Fig. 7; here the sequencer controlling the flow of data across tiers controls computation performance.

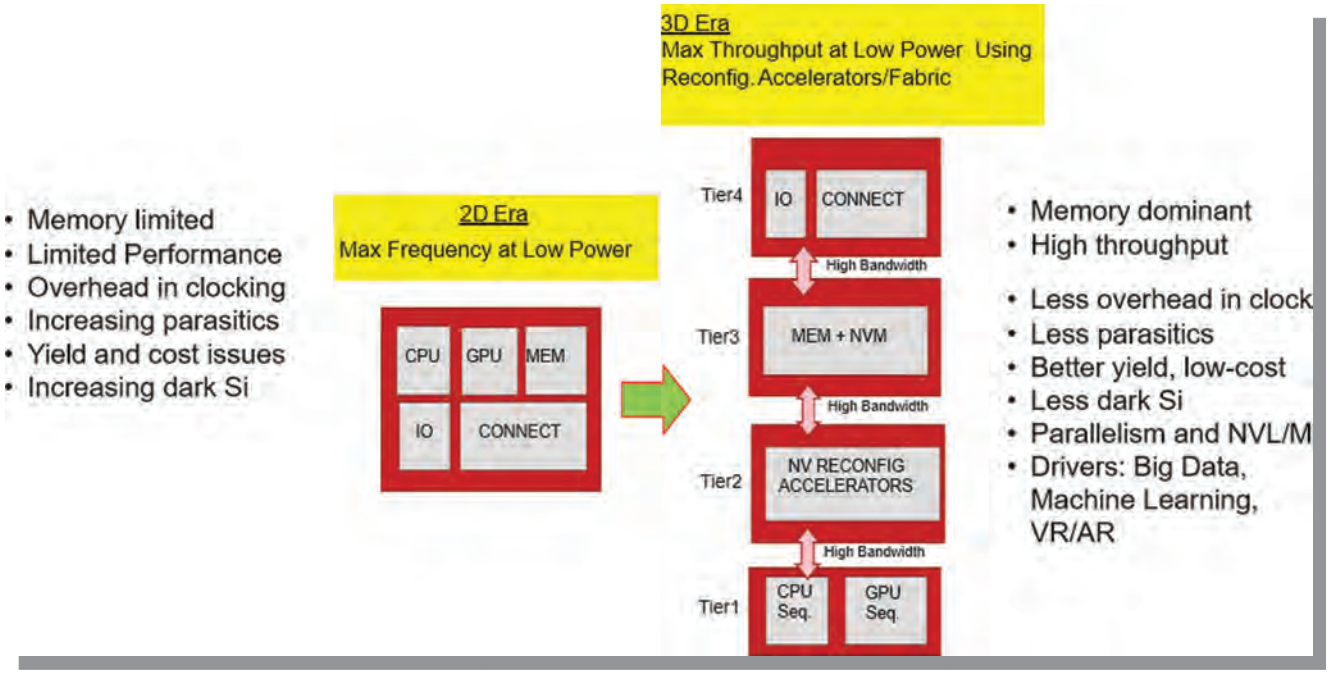


Fig. 7. 3D VLSI enablement with regular fabric.

2022	Steps/ layer	Layer Count	Step Count	Comp	Overall Complexity	Width (nm)	Defect Size (nm)	Density@Chip	Critical Area (cm2) in 80mm2	Dx/wafer	1/(A*Dxi)^n	1/(A*D0i)^n
Gate	2	1	2	1	0.75	18	9.0	32%	0.256	5.0	0.994	0.978
Fin	2	1	2	1	0.75	6	3.0	12%	0.092	136.1	0.980	0.978
Contact Via (VC)	2	1	2	2	1.50	18	9.0	3%	0.027	5.0	0.999	0.978
Contact Metal (MC)	3	1	3	2	2.25	18	9.0	37%	0.296	5.0	0.979	0.978
Local Via (V0)	1	1	1	2	0.75	12	6.0	2%	0.016	17.0	0.999	0.978
Local Metal (M1)	5	1	5	2	3.75	12	6.0	46%	0.370	17.0	0.906	0.978
Tight Pitch Via (Vx)	1	2	2	2	1.50	16	8.0	1%	0.010	7.2	0.999	0.978
Tight Pitch Metal (Mx)	3	2	6	2	4.50	16	8.0	46%	0.370	7.2	0.935	0.978
Routing Via (Vy)	1	14	14	0.5	2.63	40	20.0	1%	0.005	0.5	1.000	0.978
Routing Metal (My)	1	14	14	0.5	2.63	40	20.0	46%	0.370	0.5	0.994	0.978
	21	38	51	SUM	21.00			23%	0.181		0.801	0.800
				AVG	2.100							

Fig. 8. Critical defect dimension, process complexity, and number of defects/wafer analysis for a projected 3nm FinFET technology to get the initial ramp yield of 80%.

7. Yield Considerations

In order to be continuing More Moore scaling on multiple layers will necessitate an increased number of metallization layers, therefore the mask count is bound to increase too, barring any new breakthrough in metallization techniques and lithography. The expected transition of multiple challenging mask layers from 193i lithography to EUV, and from EUV (NA = 0.33) to high-NA EUV (NA > 0.5) will potentially save several masks since the desired resolution of lines and spaces can be achieved by a single exposure as opposed to the present situation where 3 or even 4 exposures per layer are required. However, it is expected that the mask count will resume to escalate after 2031 driven by an increased need for metallization layers required by full 3D integration. As the number of layers keeps on increasing so will process complexity and therefore the defectivity (D0) requirements will accordingly become more severe. To keep the yield under control for an 80 mm² mobile die used as a benchmark for this analysis (Fig. 8) it is necessary that the required D0 level be reduced by 2.2x in 2034 (over 5 logic node transitions)

Besides the expected addition of possible defects due to increased process complexity there is also the risk of increased defectivity due to brand new modules causing altogether severe challenges to yields. These are some of the sources of possible defects: smaller defects that were no relevant in

the past will become more important as device features keep getting smaller, the number of high-aspect ratio structures such as taller fins and GAA architecture will require more and newer conformal deposition processes, high-aspect ratio contacts will challenge contact and via technologies and control of lateral etch technology and sophisticated sidewall/bottom cleans will be required. In few words there is a concern that the process complexity and the number of materials will increase even though most of the issues are not known at present. Eventually beyond 2030 lithography will no longer be able to resolve some dimensions less than 8 nm or so and overlay requirements of fraction of a nanometer will reach a natural limitation. It is suggested that more reliance on self-organizing structures, self-alignment and self-conformal deposition will be viable by then, but these new process steps will also further increase process and material complexity.

8. Summary of Predictions from 2020 Edition of IRDS More Moore Roadmap

Until approximately the year 2010 personal computers and laptops drove technology requirements. In the past decade mobile devices, cloud data centers, AI algorithms and high-performance computing applications have been driving More Moore scaling requirements. The conditions imposed on transistor performance due to power were limitations and those were partially compensated by the industry with Design-Technology-Co-Optimizaion (DTCO). In the future, Lateral-GAA offers reduced leakage and improved performance at lower operating voltages and it is therefore expected to be a viable path for enhanced PPAC values starting as early as 2022. For the successful deployment of GAA any possible capacitance reduction is a key parameter capable of concurrently resolving performance, power, and thermal issues. For further scalability of power and energy it is estimated that adoption of 2D materials for the channel is a good approach for concurrently reducing both channel length and capacitance. However, GAA manufacturability and contact engineering remain critical challenges to adopting 2D material channel device as a device platform beyond 2028.

Innovative embedded memories technologies are significantly gaining momentum via concrete plans of adopting MRAM and stacked SRAM/DRAM solutions since higher bandwidth and capacity requirements are becoming a major bottleneck that are actually becoming more relevant than solving latency limitations. Nevertheless bandwidth, endurance, and latency improvements are needed to adopt NAND-FLASH as an AI memory solution. Multi-level cell schemes seem to be the preferred route to scale up the number of bits per chip in these memories.

2.5D/3D-stacking technologies are motivated by the benefits of stacking memory-on-logic in large chips such as data servers, AI, and network products as multiple vias of communications between chips are increased (e.g., arrays of bumps). by offering an avenue for products bundling more features and reducing time-to-market. 2.5D integration is expected to continue evolving towards transforming the present passive interposers into active interposers. This approach will enable multi-sourcing and interoperability of various chiplets in the package system whereby the interposer will be providing active and passive functions such as voltage regulation, decoupling capacitances, buffers, IO, ESD, etc.

For more information—visit https://irds.ieee.org/editions/2020.

9. Acknowledgments

The authors acknowledge the IEEE IRDS members for their valuable contributions to the IEEE IRDS More Moore roadmap.

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A Review of the 2020 IEEE International Electron Devices Meeting (IEDM)

Dina Triyoso, IEDM 2020 Publicity Chair
Meng-Fan (Marvin) Chang, IEDM 2020 Publicity Vice Chair
edited by Daniel Tomaszewski, EDS Newsletter Editor-in-Chief,
based on the Material Prepared by the IEDM Publicity Team

The annual IEDM conference (www.ieee-iedm.org), sponsored by the IEEE Electron Devices Society, is the world's largest, most influential forum for the unveiling of breakthroughs in transistors and related micro/nanoelectronics devices. The 66th annual IEDM was held virtually December 12–18, 2020 and offered a mix of live-streamed events and on-demand pre-recorded presentations, with a schedule of live Q&A sessions. The expanded schedule was intended to give global attendees enough time to review the more than 220 papers in the IEDM technical program, plus the tutorials and short courses, and to participate in the live-streamed events, such as the plenary presentations, panel discussion and career session.

"This year's format may be different, but what hasn't changed at all is that IEDM once again offered an outstanding technical program that showcased important breakthroughs in key semiconductor and related technologies, which are essential for the progress of modern society," said Dina Triyoso, IEDM 2020 Publicity Chair and Technologist at TEL Technology Center, America, LLC. "We're pleased that, despite the laboratory restrictions and all of the other challenges imposed on us by the pandemic, our community has persevered and driven the state-of-the-art of electronics technology forward yet again."

However, the virtual format provided a few challenges. "Although the virtual experience didn't give us the ability to see our colleagues in person, it did provide unique opportunities which we tried to maximize," said Meng-Fan (Marvin) Chang, IEDM 2020 Publicity Vice Chair, IEEE Fellow, Distinguished Professor of Electrical Engineering at National Tsing Hua University and Director of Corporate Research at TSMC. "For example, if IEDM were a physical event this year, nine technical sessions would run in parallel. An attendee likely would find it difficult to attend all talks of interest. But with recorded presentations available on-demand a week ahead of time, that roadblock was eliminated."

The Conference was initiated by an **opening presentation** by Prof. Suman Datta, the IEDM 2020 General Chair. Prof. Datta underlined that the 66th Edition of IEDM was held in a difficult time of pandemic, which had affected all the societies worldwide. However, he expressed a hope that better days would be ahead. A theme of IEDM 2020, "Innovative Devices for a Better Future" reflected the fact that at a time of great global uncertainty, electronics technology was being used much more broadly than ever before to address the world's most pressing challenges. Prof. Datta introduced the Executive Committee, the Technical Subcommittees and IEDM planners. Thanks to their efforts, the Conference technical program remained at a very good level, with a high number of submissions (580) and a good acceptance rate (231), in spite of the pandemic. Prof. Datta introduced the convenient internet platform used to provide access to both live-streamed and pre-recorded IEDM sessions, to the virtual Exhibit Hall, and to an online networking area. He underlined that on-demand materials would be available for the registered attendees until the end of January 2021. Next, he briefly highlighted the Conference program. Finally, on behalf of Prof. Tibor Grasser, the Technical Program Chair, and Prof. Barbara De Salvo, the Technical Program Vice Chair, Prof. Suman Datta said "Thank you" to all the presenters and organizers of the 66th IEDM and wished them a fruitful Conference.

The Conference participants were able to watch three **Plenary Presentations**, which were live-streamed as 45-minute talks followed by 15-minute Q&A sessions:

- Monday, Dec. 14: Sri Samavedam, Senior VP CMOS Technologies, imec—"Future Logic Scaling: Atomic Channels to Deconstructed Chips"
- Tuesday, Dec. 15: Naga Chandrasekaran, Senior VP of Process R&D and Operations, Micron Technology—"Memory Technology: Innovations Needed for Continued Technology Scaling and Enabling Advanced Computing Systems"
- Wednesday, Dec. 16: Sungwoo Hwang, President, Samsung Advanced Institute of Technology—"Symbiosis of Semiconductors, AI and Quantum Computing"

In partnership with the journals *Nature* and *Nature Electronics,* IEDM 2020 offered a unique **Panel Discussion** entitled "What Can Electronics Do to Solve the Grand Societal Challenges Going Forward?", moderated by Ed Gerstner, Director of Journal Policy & Strategy for Springer Nature. The Panelists were: Jacqueline Mc Glade, Professor Natural Prosperity and Sustainable Oceans, Institute for Global Prosperity and Engineering, University College London, and James Plummer, Professor and former Dean of Engineering, Stanford University. Following a year of global upheaval and acute challenges, the discussion reflected on the place of electronics and the semiconductor industry in the future world. It brought together experts from across science, technology, media, and policy to discuss future directions of microelectronics, and explored the role future technologies can play in addressing grand societal challenges, and in creating a more sustainable, equitable future. It also considered challenges in attracting the best students and the evolution of electronics education to suit future needs. The Panel was live-streamed Thursday, Dec. 17.

IEDM 2020 also included a **Career-Focused Session** featuring industry and scientific leaders talking about their personal experiences in the context of career growth: Prof. Tsu-Jae King Liu, IEEE Fellow, Professor & Dean at University of California-Berkeley, member of the Board of Directors of Intel Corp, and Dr. Heike Riel, IBM Fellow, Head of Science & Technology, Lead of IBM Research Quantum Europe. The session was moderated by Prof. Suman Datta, University of Notre Dame. The session was live-streamed Friday, Dec. 18.

Six **Tutorials**, listed below, were held during the time-frame of IEDM as on-demand pre-recorded talks available beginning Dec. 5, whereas the corresponding live summary/Q&A sessions were held on Saturday, Dec. 12.

- "Quantum Computing Technologies" by Dr. Maud Vinet (CEA Leti)
- "Advanced Packaging Technologies for Heterogeneous Integration" by Dr. Ravi Mahajan & Dr. Sairam Agraharam (Intel)
- "Memory-Centric Computing Systems" by Prof. Onur Mutlu (ETH Zurich)
- "Imaging Devices and Systems for Future Society" by Dr. Yusuke Oike (Sony Semiconductor Solutions)
- "Innovative Technology Elements to Enable CMOS Scaling in 3nm and Beyond—Device Architectures, Parasitics and Materials" by Dr. Myung-Hee Na (imec)
- "STT and SOT MRAM Technologies and Their Applications from IoT to AI Systems" by Prof. Tetsuo Endoh (Tohoku Univ.)

During the time-frame of the Conference, two **Short Courses** were also held. On-demand pre-recorded presentations were available beginning Dec. 6, whereas the corresponding live summary/Q&A sessions took place Sunday, Dec. 13.

- "Innovative Trends in Device Technology to Enable the Next Computing Revolution," organized by Anne Vandooren (imec). This course covered a range of relevant topics, including next generation nanosheet transistors; packaging technologies for 3D integration; RF front-end modules; power delivery/regulation; and monolithic and chiplet integration.
- "Memory-Bound Computing," organized by Ian Young (Intel). The topics included the role of persistent memory for high-performance computing; HBM DRAM and beyond; memory for secure computing; PUFs for hardware security; alternate SRAM technologies; analog memory needs for AI; and one-shot learning with memory-augmented neural networks.

Six **Focus Sessions**, listed below, were held at IEDM 2020 on key emerging technologies. These talks covered a range of topics addressing the gaps, challenges, and opportunities for new approaches and technologies, including system-level issues and requirements; benchmarks of current technologies; and R&D directions for the new materials, devices, circuits, and modeling/manufacturing approaches needed.

- **Device Technologies for Cryogenic Electronics**—Cryogenic electronics refers to the operation of electronic devices at temperatures from –150 °C (–238 °F) to absolute zero (–273 °C or –460 °F). The theoretical performance of electronics in this range is better than that of conventional devices because of improved thermal/electrical conductivity, lower operating power, reduction of parasitic losses, and diminished chemical/metallurgical degradation, to name a few effects. However, much work is needed to realize the full potential of cryogenic devices. The session included the following talks: "CMOS Cryo-Electronics for Quantum Computing" by J. Craninckx et al (imec), "Cryo-CMOS Interfaces for Large-Scale Quantum Computers" by F. Sebastiano et al

(Delft Univ./UC-Berkeley/Intel), "Cryo-CMOS Compact Modeling" by C. Enz et al (EPFL), "Chip Design for Future Gravitational Wave Detectors" by F. Tavernier et al (KU Leuven), "A Low-Power CMOS Quantum Controller for Transmon Qubits" by J. Bardin (Univ. Mass./Google), "III-V HEMTs for Cryogenic Low Noise Amplifiers" by J. Grahn (Chalmers Univ. of Tech/Low Noise Factory AB), "Superconductive Single Flux Quantum Logic Devices and Circuits: Status, Challenges, and Opportunities" by M. Pedram (USC), "Phonon Blocked Junction Refrigerators for Cryogenic Quantum Devices" by M. Prunnila (VTT Technical Research Centre of Finland).

- **GaN and SiC Projections—From Device to System Integration**—Wide-bandgap (WBG) semiconductors have a relatively large energy bandgap versus silicon semiconductors, leading to smaller, faster, and more efficient devices. These capabilities make WBG devices attractive for a wide range of power applications, but converters powered by WBG devices require much innovation. The session included the following talks: "Planar GaN Power Integration—The World is Flat" by K. Chen et al (HKUST), "Progressing –190 °C to +500 °C Durable SiC JFET ICs From MSI to LSI" by P. Neudeck et al (NASA Glenn Research Center/Ohio Aerospace Institute/Vantage Partners), "Advances in Research on 300 mm Gallium Nitride-on-Si(111) NMOS Transistor and Silicon CMOS Integration" by H.W. Then et al (Intel), "GaN Power ICs: Reviewing Strengths, Gaps, and Future Directions" by O. Trescases et al (Univ. Toronto), "Monolithic GaN Power IC Technology Drives Wide-Bandgap Adoption" by D. Kinzer (Navitas), "Gate Drive Concept for dv/dt Control of GaN GIT-Based Motor Drive Inverters" by E. Persson et al (Infineon), "Application of WBG Power Devices in Future Three-Phase Variable Speed Drive Inverter Systems—'How to Handle a Double-Edged Sword'" by J. Kolar et al (ETH Zurich/Politecnico di Torino), "A 16 kV PV Inverter Using Series-Connected 10 kV SiC MOSFET Devices" by R. Burgos et al (Virginia Polytechnic).
- **Future Interconnect Technology**—Interconnect is the wiring which connects transistors and other devices in an integrated circuit (IC). A key interconnect-related issue is that the performance of advanced ICs is limited by the increasing resistance/capacitance of the interconnect as it scales to smaller and smaller dimensions. Another key issue is the need for effective interconnect strategies for a range of 3D and 2.5D chip architecture and packaging possibilities. The session included the following talks: "The Overview of Current Interconnect Technology Challenges and Future Opportunities" by M-H Lee (TSMC), "Inflection Points in Interconnect Research and Trends for 2 nm and Beyond in Order to Solve the RC Bottleneck" by Zs. Tokei (imec), "Narrow Interconnects: The Most Conductive Metals" by D. Gall et al (Rensselaer Polytechnic), "Topological Semimetals for Scaled Back-End-Of-Line Interconnect Beyond Cu" by C-T Chen et al (IBM/Univ. Delaware/Institute of Physics, Academia Sinica/National Univ. of Singapore), "Staggered Metallization with Air Gaps for Independently Tuned Interconnect Resistance and Capacitance" by K. L. Lin et al (Intel), "From Interconnect Materials and Processes to Chip-Level Performance: Modeling and Design for Conventional and Exploratory Concepts" by V. Huang et al (Georgia Institute of Technology/Samsung), "Silicon-Compatible Optical Interconnect and Monolithic 3-D Integration" by K. Saraswat (Stanford).
- **Technologies Enabling 5G and Beyond**—5G is the fifth and next generation of cellular technology, promising much faster network speeds, bandwidth, lower latency, reduced transmission costs per bit and expanded connectivity. It will enable a host of new communications and computing approaches and applications. The session included the following talks: "Millimeter-Wave Multi-Antenna/MIMO Techniques for 5G NR Base-Stations" by R. Hou (Ericsson), "A Deep-Learning-Enabled Universal DPD System" by C.-L. I et al (China Mobile Research Institute), "Millimeter-Wave CMOS Phased-Array Transceiver for 5G and Beyond" by K. Okada (Tokyo Institute of Technology), "PD-SOI CMOS and SiGe BiCMOS Technologies for 5G and 6G Communications" by P. Chevalier et al (STMicroelectronics), "Heterogeneous Integration for High-Frequency RF Applications" by A. Gutierrez-Aitken (Northrop Grumman), "Innovative Smart Cut™ Piezo-On-Insulator (POI) Substrates for 5G Acoustic Filters" by E. Butaud et al (Soitec/TEMIS Innovation/CEA-Leti).
- **Energy Harvesting and Wireless Power Transmission**—Ambient energy is all around us, whether from light, heat, motion, vibration, stray electric/magnetic fields, or other sources. Converting it into electrical power, and transmitting that power without wires, is key to the ability to develop more capable autonomous, wireless, remote, and hard/impossible-to-connect devices for a variety of uses. The session included the following talks: "Toward Solid State 3D Li-ion Micro-Batteries and Microsupercapacitors for Powering Miniaturized IoT Devices" by C. Lethien (IEMN-RS2E), "High-Power Graphene

Micro-Supercapacitors" by R. Kaner et al (UCLA/Max Planck Institute of Colloids and Interfaces/ Ariel Univ), "MEMS Vibrational Energy Harvester for IoT Wireless Sensors" by H. Toshiyoshi (Univ. Tokyo), "High-Voltage Micro-Plasma Switch for Efficient Power Management of Triboelectric Kinetic Energy Harvesters" by P. Basset et al (Univ. Gustave Eiffel/Cambridge Univ./Sorbonne Univ.), "Radiative Wireless Power Transmission: From Indoor to In-Body Applications" by H. Visser (imec), "Wireless Power Transfer for Internet of Things" by Y. Kawahara et al (Univ. Tokyo), "mmWave Backscatter Front-End for 5G-IoT/WPT Applications" by D. Matos et al (Univ. de Aveiro, Sinuta S.A, Instituto Politecnico de Viseu).

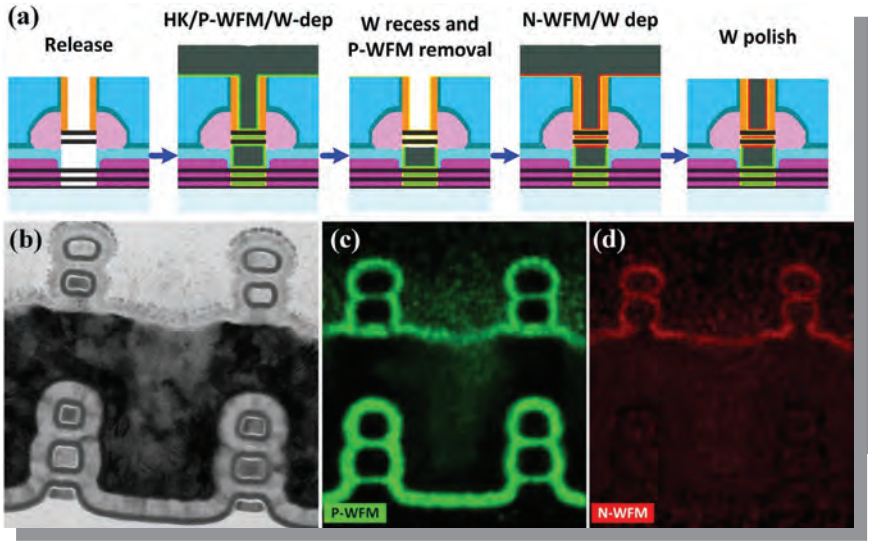
- **DTCO of Advanced Logic and Memory**—Given the increasing sophistication and complexity of semiconductor devices and software design tools, bringing hardware and software developers together to work in an integrated, efficient manner is needed to produce future devices faster and at less cost, but there are many challenges. The session included the following talks: "DTCO Launches Moore's Law Over the Feature Scaling Wall" by V. Moroz et al (Synopsys/IC Knowledge), "Advanced Node DTCO in the EUV Era" by A. Wei et al (Intel), "Next-Generation Design and Technology Co-Optimization (DTCO) of System on Integrated Chip (SoIC) for Mobile and HPC Applications" by Y.-K. Cheng et al (TSMC), "DTCO Including Sustainability: Power-Performance-Area-Cost-Environmental Score (PPACE) Analysis for Logic Technologies" by M. Garcia Bardon et al (imec), "Enabling Efficient Design-Technology Interaction by Spec-Driven Extraction Flow" by H.-L. Changet al (Primarius Technologies/ProPlus Design Solutions), "MRAM DTCO and Compact Models" by J. Song et al (Univ. Minnesota), "Enabling Design Technology Co-Optimization of SRAMs Through Open-Source Software" by M. Guthaus et al (UC-Santa Cruz).

On-demand pre-recorded presentations within the **technical program** were available beginning Monday, Dec. 7. Live-streamed session summaries by the session chairs with Q&A opportunities took place Monday-Friday, Dec. 14–18. Here are summaries of several noteworthy IEDM papers which may be assigned to the following fast developing disciplines:

CMOS Technology: Embracing New Ways to Drive Performance

Stacked NMOS-on-PMOS Nanoribbons: From planar MOSFETs, to FinFETs, to gate-all-around (GAA) or nanoribbon devices, novel transistor architectures have played a critical role in driving the performance predicted by Moore's Law. In the paper #20.6, "3-D Self-Aligned Stacked NMOS-on-PMOS Nanoribbon Transistors for Continued Moore's Law Scaling," Intel researchers described what may be the next step in that evolution: NMOS-on-PMOS transistors built from multiple self-aligned stacked nanoribbons. This architecture employs a vertically stacked dual source/drain epitaxial process and a dual metal gate fabrication process, enabling different conductive types of nanoribbons to be built so that threshold voltage adjustments can be made for both top and bottom nanoribbons. The approach combines excellent electrostatics (subthreshold slope of <75 mV/dec) and DIBL (<30 mV/V for gates ≥30 nm) with a path to significant cell size reduction due to the self-aligned stacking. These devices were used to build a functional CMOS inverter with well-balanced voltage transfer characteristics.

Proving 3D Design Viability: 3D ICs have the potential to drive continued performance according to Moore's Law, but achieving lower interconnect latency and power consumption, improved bandwidth and cost efficiencies is challenging. That's because it is difficult to test 3D IC designs once they are produced. A better linkage of design and test functions with process technology is needed to improve 3D IC performance. In the paper #15.1, "A High-Density Logic-on-Logic 3DIC Design Using Face-to-Face Hybrid Wafer-Bonding on 12 nm FinFET Process," researchers



Paper #20.6: (a) a process flow of the vertically stacked dual metal gate process; (b) a TEM image; (c, d) EDS images of the dual metal gate with N-WFM (WFM = work function metal) on the top two nanoribbons and P-WFM on the bottom three nanoribbons.

from Arm and GLOBALFOUNDRIES described a 3D IC test vehicle that demonstrated the benefits of this approach. It is based on a high-density, face-to-face wafer-bonding technology with 5.76 μm-pitch 3D connections and 12 nm FinFET devices. Its cache-coherent interconnect mesh (to allow synchronized operations in each layer) operated at up to 2.4GHz, with 10x lower bandwidth density (3.4 TB/s/mm^2) and energy usage (0.02 pJ/bit) versus state-of-the-art 2.5D/3D bump-based technologies. The researchers said it was an essential step toward proving the viability of 3D designs for next-generation high-performance, energy-efficient ICs.

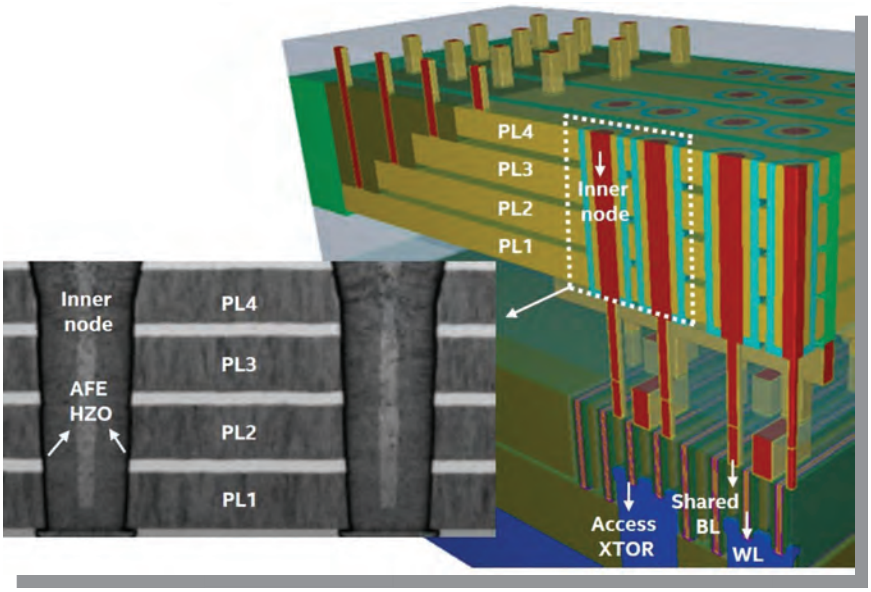
CMOS-Compatible Graphene Interconnects: With continued scaling, conventional dual-damascene interconnect technologies suffer from higher resistance and self-heating, and diminished reliability. Graphene interconnects are good candidates for interconnects in future technology nodes. In the paper #31.1, "Reliability and Performance of CMOS- Compatible Multi-Level Graphene Interconnects Incorporating Vias," a UCSB-led team described a CMOS-compatible solid-phase growth technique they used to build large-area multi-level graphene (MLG) interconnects on dielectric (SiO_2) and metallic (Cu) substrates. The interconnects are BEOL-compatible and incorporate edge-contacting metal vias (versus top contacts), in a doped-MLG/Co-via multi-level structure. The researchers performed scaling analyses which showed that an increase in total via-resistance in the structure is more than compensated for by reduced wire resistance and parasitics, resulting in a ~1.5x improvement in overall circuit performance compared to that of the dual-damascene process.

Making New Memories

High-Density 28 nm FDSOI Embedded PCM Memory for Automotive: Scores of microcontrollers are used in today's vehicles, to monitor and control advanced driver-assistance systems (ADAS), powertrain control, infotainment and comfort systems, and others. These SoCs must offer high-performance, low-power operation and high levels of reliability. As the software code which runs automotive systems grows larger, the need also grows for more code storage in high-density embedded non-volatile memory (eNVM). In the paper #24.2, "High Density Embedded PCM Cell in 28 nm FDSOI Technology for Automotive Micro-Controller Applications," a STMicroelectronics/CEA-Leti team detailed an ultra-dense (cell size = 0.019 μm^2) embedded phase-change memory (PCM) technology for automotive SoCs that meets the stringent AEC-Q100 Grade 0 standard for automotive reliability. It leverages a 28 nm fully depleted silicon-on-insulator (FDSOI) substrate; novel super-shallow trench isolation (SSTI) for the bit line (requiring no trench etch-and-fill); high-voltage (5V) triple-gate-oxide transistors; and a compact bipolar junction transistor (BJT) selector.

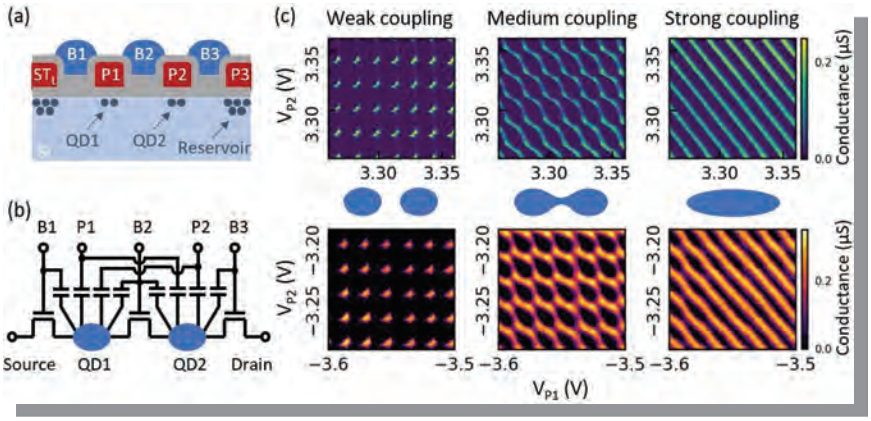
3D Embedded DRAM Using Stacked Anti-Ferroelectric HZO Capacitors: In the paper #28.1, "Anti-Ferroelectric $Hf_xZr_{1-x}O_2$ Capacitors for High-Density 3D Embedded-DRAM," Intel researchers discussed their work using the antiferroelectric (AFE) material hafnium-zirconium-oxide ($HfZrO_2$) to make a 3D deep-trench capacitor for potential use in embedded DRAM memories. It demonstrated endurance of 10^{12} cycles even at elevated temperatures, and a 1.8 V operating voltage. The researchers used these AFE capacitors in a novel memory architecture for ultra-high bit density: a vertical stack based on one access transistor with multiple AFE capacitors in parallel. Each capacitor represents a single memory bit. A significant density boost was achieved by stacking four AFE capacitors in a vertical fashion, with no area increase.

A New Force in Ferroelectric Tunnel Junction Memories: Ferroelectric tunnel junctions (FTJs) are promising for non-volatile memory (NVM) applications like ultralow-power data storage and neuromorphic computing. They feature an ultrathin ferroelectric barrier layer sandwiched between two electrodes. Modulating the barrier resistance or "height" by controlling its polarization prevents or allows the quantum tunneling of electrons through it, enabling the storage or



Paper #28.1: A cross-sectional TEM image of stacked vertical capacitors (4X), along with a cross-sectional representation of the 1T-4C memory architecture, showing a future path toward high-density memory.

retrieval of data. However, finding an optimum barrier material has been challenging. In the paper #4.1, "Multi-scale Simulation of Ferroelectric Tunnel Junction Memory Enabled by van der Waals Heterojunction: Comparison to Experiment and Performance Projection," a University of Florida-led team discussed their work simulating and building a ferroelectric tunnel junction by vertically stacking thin (~4 nm) layers of a van der Waals material ($CuInP_2S_6$) on a layer of graphene to create atomically think heterojunctions at the CIPS-graphene interface. The heterojunctions are sandwiched between an SiO_2 substrate and a top metal (gold) contact. (van der Waals forces are weak attractive/repulsive forces between atoms, molecules and surfaces.) Simulations of the performance of these heterojunctions, verified by laboratory experiments, showed a record-high tunneling electroresistance ratio of ~6 x 10^7, pointing the way to a possible new NVM memory device structure with an exponentially higher ON/OFF ratio than existing devices, and ~1ns read latency.



Paper #38.3: (a) a schematic cross-section of a double dot; (b) equivalent circuit of a double dot; (c) tunable tunnel coupling between the double dot for nMOS (upper) and pMOS (lower) devices. The plunger gates P1 and P2 control the potential of dot 1 and 2, respectively. B2 controls the inter-dot coupling. In the weak coupling regime, dot 1 and 2 are separated. Conductance maps show isolated points when energy levels between dots are aligned. In the medium coupling regime, levels of double dots begin to hybridize. Conductance maps show honeycomb patterns. In the strong coupling regime, two dots merge into one.

Quantum Computing

Qubits Start to Move From Lab to Fab: Qubits are often made from quantum dots, particles a few nanometers in size made from semiconductors. However, qubits are unstable, with short "coherence times" (i.e., how long they can stay in a quantum state). Some quantum computers exist, but they use only a few qubits, are error-prone and fragile, and operate at cryogenic temperatures. Silicon-based quantum-dot qubit systems are attractive for potential use in large-scale quantum processors because they have demonstrated relatively long coherence times and high-fidelity operation in laboratory settings, and because silicon technology is widely used and economical compared to other material systems. But cryogenic material properties and other aspects of qubit design are still not well-understood, and a design platform flexible enough to use in studies of silicon qubit characteristics is needed. In the paper #38.3, "A Flexible 300 mm Integrated Si MOS Platform for Electron- and Hole-Spin Qubits Exploration," imec researchers described the first such platform based on industry-standard 300 mm silicon wafer fabrication technology instead of specialized laboratory processes. It uses both optical and electron-beam lithography to fabricate silicon spin qubits, and enables on-the-fly layout design modifications for devices having either n- or p-type ohmic implants, pitches <100 nm, and uniform critical dimensions down to 30 nm. The researchers said the design platform enabled them to achieve nearly 100% device yields for qubits with 30 nm spacings. They plan to use it to incorporate additional materials and structures into qubits for further study, and to improve cryogenic characterizations.

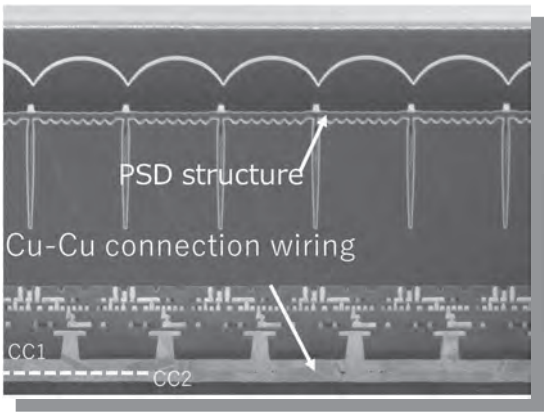
Advances in Imaging

Single-Chip Lidar: Lidar (light detection and ranging) is the optical counterpart of radar and uses laser light instead. It's extremely fast and lends itself to sophisticated data processing, which means that differences in laser light return times and wavelengths can be used to make detailed 3D representations of a target. It's a critical technology for autonomous vehicles, robotics and augmented-reality applications. In the paper #7.2, "Single-Chip Beam Scanner with Integrated Light Source for Real-Time Light Detection and Ranging," Samsung researchers reported the first single-chip lidar beam scanner. It opens up the possibility of ultra-low cost, compact lidar systems because it requires no separate light source, unlike current systems which are larger and use mechanical beam scanners with motors and rotating and mirrors. It integrates a fully functional 32-channel optical phased array, 36 optical amplifiers, and tunable laser diode onto a 7.5 x 3 mm^2 chip, fabricated with III-V-on-Si processes. Also, a calibration algorithm based on machine-learning principles is used in digital signal processing for real-time operation. The device achieved real-time 20 frames-per-second operation, at a resolution of 120 x 20 lines, at 10 meters.

Ultra-High Resolution Mobile CMOS Imager: In the paper #16.2, "A 0.8 μm Nonacell for 108 Megapixels CMOS Image Sensor with FD-Shared Dual Conversion Gain and 18,000e-Full-Well Capacitance," Samsung also

detailed a 0.8 μm-pitch 108-megapixel (Mp) ultra-high resolution CMOS image sensor for mobile applications. As demand for higher-resolution image sensors for smartphones and other mobile devices has grown, the number of pixels they contain has increased from 48 Mp, to 64 Mp, to 108 Mp. Pixel pitch has decreased to enable higher densities, but this has reduced pixel silicon volume as well as the amount of incident light available at each pixel. These reductions have degraded pixel signal-to-noise performance and full well capacity (FWC, or the number of electrons a pixel can collect at saturation level). Samsung researchers got around this with a 3 x 3 shared pixel structure they call Nonacell. It consists of three shared pinned photodiodes, whose signals are summed in the imager's floating diffusion (FD) and whose voltages are averaged. The shared-pixel units can be combined in various ways to achieve optimum performance in changing light conditions—ultra-high 108 Mp resolution for bright outdoor daylight conditions, and 12 MP resolution for low-luminescence indoor light. The work is a step toward much higher image quality for smartphones and other mobile devices.

Low-Power, High-Resolution CMOS Imager for Indirect Time-of-Flight: Indirect time-of-flight (iToF) CMOS image sensors are used for distance measurements in smartphones and gaming systems, and improving their precision while maintaining/decreasing their power consumption is a key goal. In the paper #33.1, "Low Power consumption and High Resolution 1280 x 960 Gate-Assisted Photonic Demodulator Pixel for Indirect Time-of-Flight," Sony researchers will describe how they built a floating-diffusion-storage global-shutter image sensor with a resolution of 1280 x 960 at 10 meters, implemented as a 3D-stacked, back-illuminated iToF sensor. The iToF sensor achieves 18,000e- FWC and 32% quantum efficiency (QE), has a pyramidal surface for diffraction (PSD) structure which improves QE at smaller pixel sizes, and uses 3.5 μm pixels. Low power consumption is achieved with low iToF leakage current and with the use of low-resistance Cu-Cu interconnections. The researchers said these device architectures enabled high-resolution and wide-dynamic-range 3D depth-sensing for both near and far objects.



Paper #33.1: A cross-section of the 1.2M pixel gate-assisted photonic demodulator (GAPD) for iToF.

High-Frequency and Power Devices

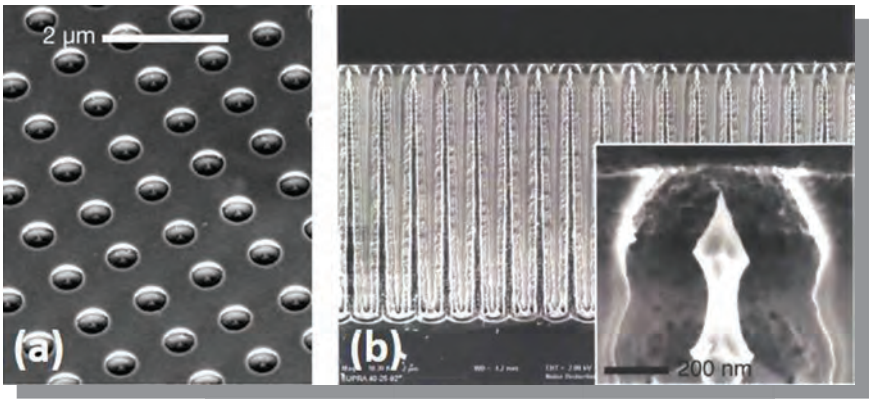
20 GHz p-Channel HFETs: CMOS technology requires both n- and p-channel devices, but the performance of p-channel devices lags, a mismatch which must be addressed to obtain maximum performance and energy efficiency from future chips. In the paper #8.3, "GaN/AlN p-Channel HFETs with I_{max} >420 mA/mm and ~20 GHz f_T/f_{MAX}," Cornell and Intel researchers described the first GaN-based p-channel transistors to break the GHz speed barrier. To build them, the researchers took advantage of the polarization-induced 2D hole gas found in the GaN/AlN heterostructure. (Hole gas refers to the population of free holes in a metallic conductor, which are free to move about within it much like molecules of gas move in a container. "2D" means they are free to move in two dimensions.) The researchers reported that with a scaled source/drain distance and gate length, and low-resistance ohmic contacts, p-channel GaN HFETs demonstrated ON currents >420 mA/mm and f_T/f_{MAX}~20 GHz. When combined with the excellent performance of AlN/GaN n-HFET devices that has been reported previously, these new results are poised to take this wide-bandgap CMOS platform into new application domains in the RF and power electronics arenas.

Lithographically Defined Organic Substrates for RF: Radio-frequency (RF) ICs use ceramic packaging substrates, while digital circuits such as CPUs, GPUs and APUs use organic substrates. Ceramics are well-suited for use with low-loss, high-conductivity metal conductors, but organics support a wider range of dielectric thicknesses, tighter manufacturing variations, low-surface-roughness conductors and finer design rules. All of these are needed for the increased circuit density and performance demanded by tomorrow's high-frequency applications. In the paper #17.5, "Organic Package Substrates Using Lithographic Via Technology for RF to THz Applications," Intel-led researchers detailed a new manufacturing process for low-loss organic substrates. It uses lithographically defined (versus laser-drilled) vias, bringing together tighter process tolerances and copper interconnect in the substrate. The researchers built structures and devices like coaxial and coplanar waveguides, high-Q RF inductors, filters and others in the frequency range from 1–330 GHz, which demonstrated superior electrical performance versus ceramics. They said performance could be improved with new dielectric adhesion techniques and advanced organic dielectric build-up films.

40 kV Silicon Vacuum Transistor: In the Paper #5.2, "Demonstration of a ~40 kV Si Vacuum Transistor as a Practical High Frequency and Power Device," an MIT-led team described the first

Si vacuum transistor operating at ~40 kV and with the potential to have a semiconductor-like footprint. Such a high voltage level is normally reserved for wide-bandgap materials like SiC and GaN. The proof-of-concept device consists of a gated field emission array (i.e., an electron source), a vacuum drift region and a metal anode. Electrons are emitted from the gated field emission array into the vacuum through tunneling, travel through it and are collected at the anode. The vacuum determines the transport properties and the high-voltage isolation. Using this technology as a baseline, the researchers provided intrinsic benchmarks for vacuum transistors. They said the high critical electric field and unbounded carrier velocity of these devices could lead to compact, high-performance vacuum devices able to outperform solid-state devices on all metrics, making them suitable for a range of high-power and high-frequency applications, and also as next-generation X-ray sources.

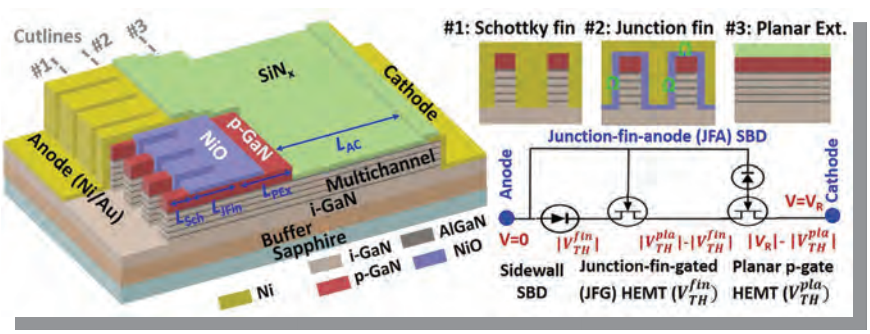
5 kV AlGaN/GaN Power Schottky Barrier Diodes: For years, bipolar Si PN diodes have been the main diode technology used to build high-voltage (1.7–10 kV) rectifiers for industrial motor drives, pulsed power systems, and power grid applications, but the diode performance is limited by poor reverse-recovery times. More recently, unipolar SiC Schottky barrier diodes and junction barrier Schottky diodes have been demonstrated up to 10 kV, and commercialized at 3.3 kV. GaN, however, has superior physical properties to Si and SiC. In the paper #5.4, "5 kV Multi-Channel AlGaN/GaN Power Schottky Barrier Diodes with Junction-Fin-Anode," a Virginia Tech-led team described the first multi-kV operation of lateral AlGaN/GaN Schottky diodes. Built on 4-inch GaN-on-sapphire wafers, the devices consist of a stack of five parallel 2DEG (two-directional electron gas) channels in combination with a fin-based 3D anode structure which wraps the p-n junction around the fins. They demonstrated a 5.2 kV breakdown voltage, specific on-resistance as low as 13.5 mΩ · cm^2, and low off-state leakage current, leading to a 2 GW/cm^2 figure of merit which surpasses that of unipolar SiC Schottky barrier diodes. The results show the potential of AlGaN/GaN multi-channel devices for medium- and high-voltage power applications.



Paper #5.2: (a) Tilted and (b) cross-sectional SEMs for gated FEAs. (a) shows an array of gated sharp tips in the middle of a ~200–300 nm aperture, formed through a self-aligned fabrication process; (b) shows the high aspect ratio nature of the nanowires (~6–10 µm tall) with a diameter of 200 nm. On top of this nanowire a sharp tip exists to concentrate the E-field of the surrounding polysilicon gate.

Noteworthy Papers on Diverse Topics

Large-Area Active-Matrix Microfluidics Platform: In the paper #35.5, "Large-Area Manufacturable Active Matrix Digital Microfluidics Platform for High-Throughput Biosample Handling," a team led by the Suzhou Institute of Biomedical Engineering and Technology at the Chinese Academy of Sciences showed how the mature, highly scalable amorphous silicon (a-Si) thin-film transistor (TFT) technology used in flat-panel displays (FPDs) could be leveraged to create a high-precision, high-throughput, online and programmable microfluidics platform for bio-sample handling. Electrowetting is the modification of the wetting properties of a surface with an applied electric field. An electrode array beneath the surface applies voltage signals in specific locations in sequence, and liquid droplets on the surface in those areas move, merge, mix and/or separate by following the electric field. The team used FPD active-matrix technology to fabricate a chip containing a 32 × 32 pixel array (i.e., an electrode array) in an active area of 10 cm^2. Each pixel can

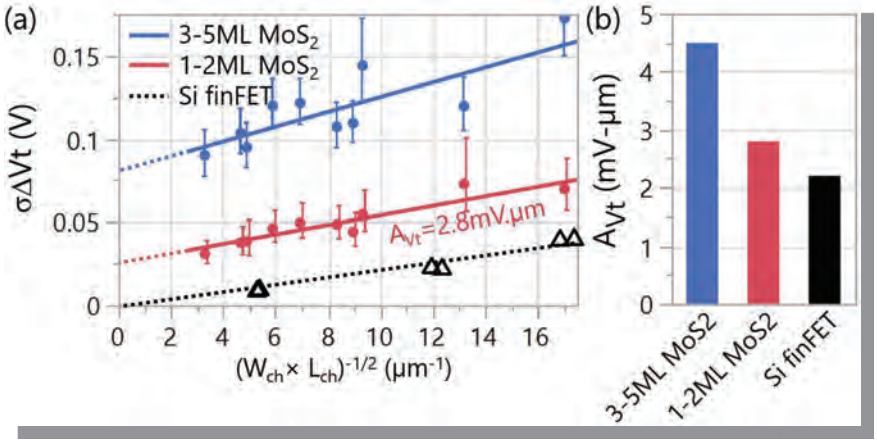


Paper #5.4: (left) A 3D schematic of the multi-channel AlGaN/GaN SBD with junction-fin-anode (JFA). The anode metal is partially removed to show the internal structure. (right) Cross-sections along the cutlines #1- #3, and the equivalent circuit model of the JFA- SBD with the internal voltage distribution at a high reverse bias V_R. The diode in the planar p-gate HEMT represents the planar Ni/p-NiO/p-GaN junction.

be individually or simultaneously addressed, and manipulation of droplets at single-pixel level with a ~1% volume coefficient of variation was shown. This performance is a substantial improvement over the current state-of-the-art (9-pixel resolution and 4% variation), is scalable to larger array sizes, and opens up possibilities for on-chip diagnostics in point-of-care testing.

Nanophotonic, Battery-Free Sensor for Glaucoma Monitoring: Glaucoma, one of the leading causes of blindness, is largely caused by an elevated intraocular pressure (IOP). Current IOP monitoring techniques are imprecise, provide no long-term monitoring, and have difficult readouts. In the paper #14.5, "Nanophotonic Sensor Implants with 3D Hybrid Periodic-Amorphous Photonic Crystals for Wide-Angle Monitoring of Long-Term In-Vivo Intraocular Pressure," a Samsung/Caltech team described a highly miniaturized (500-μm diameter, 200-μm thick) optomechanical nanophotonic sensor implant for long-term, continuous and on-demand IOP monitoring. The battery-free IOP sensor is made of a flexible, spongy medical-grade silicone containing 3D photonic nanostructures, produced using a colloidal self-assembly process. It functions as a pressure-sensitive optical resonator with a sensitivity of 0.1 nm/mmHg, and delivers IOP readings when interrogated with invisible near-infrared light. The researchers implanted eight sensors in the eyes of white rabbits, and demonstrated dynamic and long-term changes of IOP in awake rabbits with an average accuracy of 0.56 mm Hg over the range of 0–40 mm Hg. With further sensor refinements and detector automation, it may become a viable choice for patient-initiated glaucoma management in the home environment.

Resistive-Gate FinFETs Enable Hardware Security: Digital devices are ubiquitous in today's society, but internet attack incidents have increased dramatically in recent years. Software has been used to generate encryption keys, but such passwords are often logical and easily hacked. A hardware-based True Random Number Generator (TRNG) that relies on the randomness of physical phenomena like manufacturing process variations to generate encryption keys can't be easily hacked. However, existing RRAM-based TRNGs don't have all the required features, such as high speed operation, highly reliable performance, and simple circuit design. In the paper #39.3, "Novel Concept of Hardware Security Using Gate-switching FinFET Nonvolatile Memory to Implement True-Random-Number Generator," a National Chiao Tung University-led team described a TRNG device architecture comprising a one-transistor resistance switching memory as a core and a 40 nm peripheral circuit. The core is an integration of a metal-insulator-metal (MIM) capacitor on FinFET platform—essentially, a NOR-type resistance-gate integrated with the FinFET. Its drain current is randomly distributed as a result of time-varying conducting filaments, and the researchers said it was an ideal entropy source for a TRNG. They benchmarked its performance and reported that it passed all relevant NIST statistical tests for security applications.



Paper #3.1: (a) For MoS_2, Pelgrom lines don't cross the origin, hence variability doesn't approach zero in the limit of very large dimensions. Other process-related sources of variability are present. 1–2ML MoS_2 FETs (EOT = 2.6 nm) have higher $\sigma\Delta V_t$ (b) but their slope AV_t approaches the Si FinFET reference (EOT = 0.8 nm).

Understanding Variability in Scaled MoS_2 Transistors: For advanced technology nodes and future transistors with ultra-scaled channel lengths, 2D channel materials like molybdenum disulfide (MoS_2) promise better control of electrostatics than Si FinFETs, and hence better immunity to short-channel effects (SCE), which become a relatively larger performance issue at smaller dimensions. In the paper #3.1, "Sources of Variability in Scaled MoS_2 FETs," an imec-led team performed the first study of variability in nanoscale MoS_2 devices (channel width = 115 nm; length = 30 nm). The researchers looked at sources of variability like MoS_2 thickness, the impact of bilayer islands (i.e., grains) of MoS_2, the impact of a sapphire growth template, and resulting electrical impacts. They simulated and built devices with a median subthreshold slope (SS) of 80 mV/dec and I_{max} >100 μA/μm, and found that thinning the MoS_2 material from three layers to one layer results in strongly reduced SS and threshold voltage variability. Overall, their work showed intrinsic variability is low and comparable with Si FinFETs. The researchers said better control of key process steps like transfer, cleaning and contacts would further lower MoS_2 device variability, making it suitable for future technology nodes.

Highlights of the 2020 IEEE Photovoltaic Specialists Conference

The 47th IEEE Photovoltaic Specialists Conference (PVSC-47) was held this year as an online fully virtual event from June 15 to August 21, 2020. While originally planned as an in-person event to be held in Calgary, Canada, the circumstances surrounding the novel coronavirus (COVID-19) forced cancellation of the Calgary event and a move to a fully virtual conference. Despite the short time period to do this, PVSC-47 was quite successful! A total of 730 papers were presented virtually at PVSC this year with an estimated attendance of nearly 1300 people. PVSC is well recognized as an international conference, and this year was no different with attendance from 60 different countries. The virtual format also allowed attendance by many countries that have not previously attended PVSC, such as Somalia, Togo and Namibia!

Numerous live sessions were hosted during the initial week of the conference from June 15th–19th. These sessions included some of the best papers in each of the technical areas as well as live Q&A and panel sessions with the authors. In addition, the full tutorial program (10 topics) was offered virtually, drawing nearly 400 participants. A number of special topic sessions on hot carriers and III-V technology were also held throughout June, allowing researchers in these areas to connect in a virtual panel format. Importantly, all of the PVSC-47 papers and presentations were available online through the summer until August 21st, allowing our attendees ample time to view and digest the exciting results presented this year. In fact, at the close of the conference, the total cumulative views of PVSC-47 presentations was nearly 250,000!

The highest award presented at the conference, the *William R. Cherry Award*, was presented this year to Dr. James Sites of Colorado State University. Dr. Sites had a great presentation that emphasized the importance of collaboration and teamwork to success between groups adept at electronics, device physics, materials science, chemistry, and manufacturing (key to translating lab success to large scale). Dr. Sites went on to explore a variety of thin film materials, what has worked and what has not, how alloying and grading have been introduced to preferentially adjust bandgaps. He discussed some of the strengths of thin films (low cost manufacturing, non-crystalline material is forgiving), some of the challenges (grain interfaces, hard to optimize all parts of the structure simultaneously), and some of the future outlook (semi transparency for windows/agriculture, flexible, tandem designs). Dr. Sites will be presented with a plaque, as well as our applause and congratulations, in person at next year's PVSC.

Dr. Brett Hallam was this year's *Stuart R. Wenham Young Professional Award* winner, for his work on manipulating hydrogen charge states (advanced hydrogenation) for defect passivation, and development of rapid processes to eliminate a light induced degradation (LID) and a light- and elevated temperature-induced degradation (LeTID), which he and the University of New South Wales (UNSW) hydrogenation team subsequently commercialized. His latest achievement is the demonstration of p-type Cz heterojunction solar cells with stable open circuit voltages >735 mV. Dr. Hallam made a gracious acceptance speech and we look forward to presenting him with a plaque at PVSC-48.

In addition, two newly minted IEEE Fellows in the PV community were recognized at PVSC-47, Drs. Mool Gupta and Steven Ringel. Being named a Fellow is one of the highest honors bestowed by IEEE, reserved for a very select group of members (less than 0.1% per year), in recognition of their extraordinary record of accomplishments. Both Mool (for contributions to laser material and interactions) and Steven (for contributions to compound semiconductor photovoltaics) have made significant and lasting impacts in the field of photovoltaics and we congratulate them on being elevated to IEEE Fellows!

(top) Dr. Seth Hubbard, Conference General Chair, kicks off the 47th PVSC from his virtual headquarters (middle) Dr. James Sites accepts (virtually) the William R. Cherry Award (bottom) Dr. Christian Breyer answering questions following his excellent Keynote address.

Best Student Paper Awards were issued in each of the technical categories. The award winners are listed in the table below. Congratulations to all of these students for their excellent contributions to our field! You can find their proceedings papers on IEEE Xplore.

Area	Last Name	Title	Affiliation
1	Kohei Watanabe	Up-converted photocurrent enhancement in modulation-doped two-step photon up-conversion solar cells	Kobe University
2	Swapnil Deshmukh	Investigating the potential of amine-thiol solvent system for high-efficiency CuInSe2 devices	Purdue University
3	Felix Predan	Wafer-bonded GaInP/GaAs/GaInAs//GaSb four-junction solar cells with 43.8% efficiency under concentration	Fraunhofer ISE
Joint	Markus Feifel	Advances in epitaxial GaInP/GaAs/Si triple junction solar cells	Fraunhofer ISE
4	Saman Jafari	Boron-oxygen related light-induced degradation of Si solar cells: Transformation between minority carrier trapping and recombination active centers	UNSW
5	Shuai Nie	Temperature-dependent photoluminescence imaging using non-uniform excitation	UNSW
6	Noor Hartono	Capping layers design guidelines for stable perovskite solar cells via machine learning	MIT
7	Ryan Hool	Electron irradiation study of metamorphic 1.7 eV GaAsP solar cells	UIUC
8	Sanghyuk Lee	Learning from Tetris: A new approach for the automated configuration of the interconnection layout of BIPV modules for large-scale application	Korea Polytechnic University
9	Bennet Meyers	Solar Data Tools: Automatic Solar Data Processing Pipeline	Stanford University
10	Severin Nowak	A measurement-based gradient-descent method to minimize loss by dispatching DER reactive power	University of British Columbia
11	Michael Hopwood	An assessment of the value principal component analysis for photovoltaic IV trace classification of physically-induced failures	University of Central Florida
12	Amrita Raghoebarsing	Public Survey Regarding the Acceptance of Photovoltaic Systems in Suriname	University of Twente

Outreach, Diversity and Inclusion

Youth Scholar Program Chair Silvana Ayala Pelaez from National Renewable Energy Laboratory (NREL) and Youth Outreach Coordinator Michelle Jordan from Arizona State University (ASU) introduced our youth scholar program. This year there were two contests, the first to produce a 90 second video "pitch" to portray an idea for a project in solar energy. The second, to produce a "future narrative" describing through words or images a vision of what a solar powered world might look like. At least eight of our PV colleagues, identified individually in the presentation, reviewed each submission. The students presented amazing work portraying PV concepts as integrated into society for the near and distant futures. This year's winners are listed below, congratulations to these up and coming PV scientists and engineers!! Links to the videos and narratives can be found at the PVSC-47 website (https://www.ieee-pvsc.org/PVSC47/events-YouthScholars)

Solar Energy Video Pitches Winners

- First place: ***Solar4Students: School Pavilions.*** Alyssa Dora Cortez & Jawed Nur. Incoming 12th graders from Bioscience High School, Phoenix Arizona.
- Second place: ***Hybrid Solar Panels.*** Jasmin Martinez Castillo. Incoming Junior for Bioscience High School, Phoenix Arizona.
- Third place: ***Everlasting.*** Yash and Veer Pahwa. Yash is in 12th grade and Veer is in 9th grade at Tower Hill School, in Wilmington DE.
- Honorary Mentions:
  - ***Makin' it Photovoltaic***. Faith Skinner and Andrew Kallai. Faith and Andrew are rising 12th graders at Appoquinimink High School in Middletown, DE.
  - ***Aqualidad.*** Maryan Robledo. Maryan is a rising Junior at Bioscience High School, in Phoenix AZ.

Future Narrative Winners

- First place: ***Bon City.*** Jazmine Cordon. Jazmine is an incoming 9th grader from Sevilla West Middle School.
- Second place: ***Sincerely, Maisy.*** Bonnie Law & Mallory Creveling. Bonnie and Mallory are 7th graders at Gunning Bedford Middle School, in New Castle DE.
- Third place:
  - ***The Future of New Solar Cell Trees***. Irwin Wang. Irwin is an 8th grader at Odyssey Charter School in Wilmington, Delaware.

- ***S.O.A.R. Since 3040***. Alyssa Dora Cortez. Alyssa is an incoming 12th grader at Bioscience High School, Phoenix AZ.
- Honorary Mentions:
  - ***Follow the Light.*** Venezia Alana Figueroa. Venezia is a 9th grader at Bioscience High School, Phoenix Arizona.
  - ***Miner 145.*** Andrew Zhao. Andrew is a rising senior at Charter School of Wilmington, in Wilmington DE.
  - ***A day in the life in a solar-powered world.*** Aidan Hearn. Aidan is a 7th grader at Northley Middle School, in Aston PA.

The first annual Minority Carriers Panel convened on June 16th, 2020 via zoom webinar, was moderated by Dr. Lyndsey McMillon-Brown, NASA Glenn Research Center, with panelists: Prof. Adrienne Stiff-Roberts, Duke University; Prof. Tyler Grassman, The Ohio State University; Dr. Joe Berry, NREL; and Dr. Nikhil Jain, X Display Company. This event provided many diverse individuals and their allies with the space to connect with one another, identify problems within the PV community and generate solutions to make our PV community accurately representative of the communities that we serve, and inclusive to all. This solutions-based discussion yielded actionable tasks and practices that attendees can implement in their academic and professional spaces to develop diverse teams, facilitate inclusion, and confront injustices and microaggressions. The panelists also provided advice for allies and advocates with guidance to educate themselves about their privilege, become good listeners, practice empathy, and amplify the voices of marginalized individuals.

Jennifer Allyn (Senior Advisor at Women of Renewable Industries and Sustainable Energy, WRISE) and Anne Weisberg (Director of the Women's Initiative at Paul, Weiss, Rifkind, Wharton & Garrison, LLP) presented and facilitated a workshop for this year's Woman in Photovoltaics event on June 18th. Using a combination of lecture and breakout sessions, they introduced concepts of diversity and intersectionality, effects of gender in the workplace and the obstacles it causes. The focus of the workshop was on five "derailers" which negatively affects representation of women in leadership roles, each discussed in detail: unconscious bias, inadequate sponsorship, lack of specific feedback, gender gap in recognition, and work-life conflict. The final portion of the session focused on leading change within an individual's organization, using actionable plans to address each of these details, on both individually and team-wide.

Keynote

Christian Breyer (LUT University Finland) presented the Keynote on the "*Dawn of the Solar Age: On the history of PV in 100% renewable energy scenarios and future prospects*", contrasting a brief history from Becquerel to the first silicon PV at Bell Labs in 1953 with another history you may be less aware of, the exploration of a 100% renewable energy (RE) scenario which has been published in the literature since the mid-1970s. Defossilization of energy resources is critical to our collective future, and towards that goal photovoltaics is likely to contribute as much as 80% from some reports

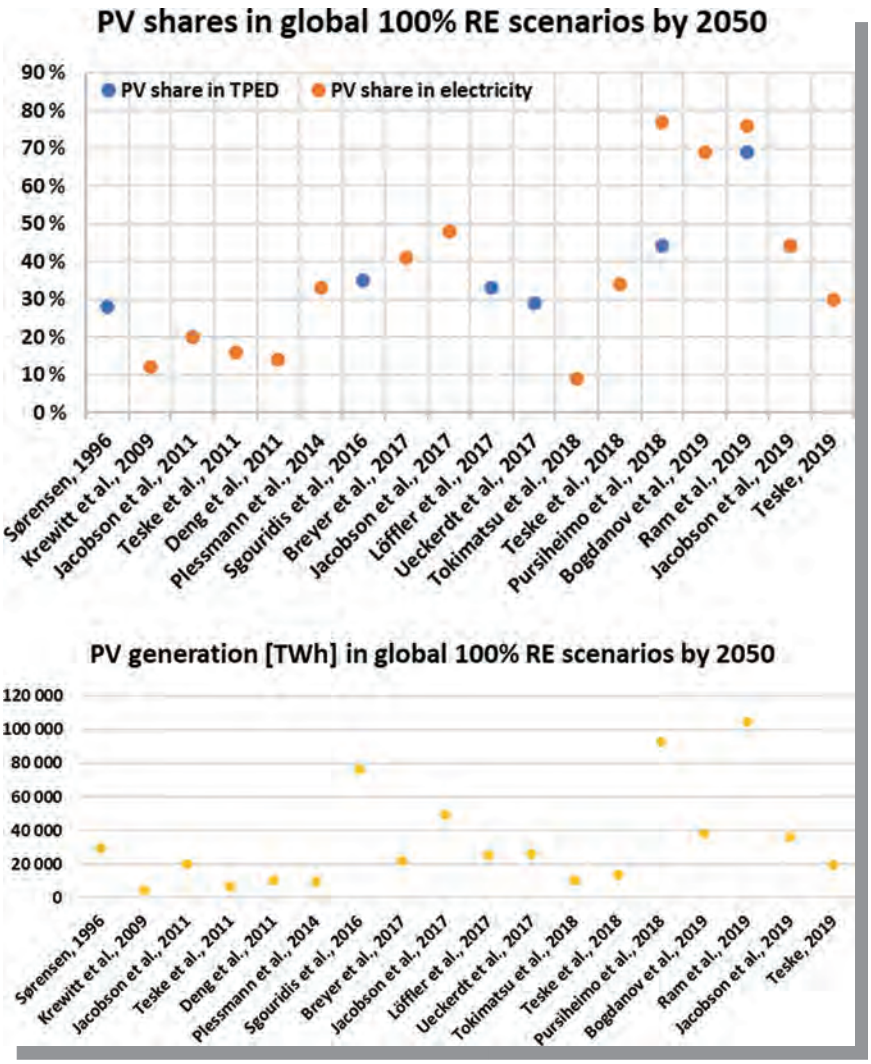


Fig. 1 Data compiled by Dr. Breyer for his keynote address showing various sources for the estimated PV share of generation (top) as well the PV energy production (bottom) in a 100% RE scenario.

(Figure 1 top panel). This demands at least 20,000+ TWh from solar PV by 2050 to support a 100% RE goal (Figure 1 bottom panel). To further work towards this future, better "power-to-x" efficiencies are required for electricity driven chemical processing, heating, steel manufacture, water desalination, to name a few. In discussions following the talk, Dr. Breyer stressed the importance of challenging outdated assumptions about PV prevalent in the literature, asking those tasked with peer review to cross check numbers and hold authors accountable.

Conference Highlights

Continuing with the tradition of the past few years, the 47th PVSC was divided into 12 technical areas covering cutting-edge developments in science and engineering of photovoltaics, ranging from fundamentals to applications, with an emphasis on material science, devices, systems, solar resources and policy related matters. To give readers insights on the conference's vast program, this Technical Brief provides an overview of the conference highlights by area. For more detailed information, the full proceedings are currently available on IEEE Xplore.

Area 1: Fundamentals and New Concepts for Future Technologies

Shanhui Fan (Stanford University) gave the plenary on the thermodynamics of light and implications for harvesting solar energy using the coldness of the universe utilizing nighttime radiative cooling. This effect was demonstrated experimentally using SiO_2 and HfO_2 dielectric layers. When exposed on a rooftop, the sample temperature falls by as much as 5 °C below ambient air temperature, which has implications for closed loop water cooling for air conditioning applications. Dr. Fan also discussed the concept of a thermoradiative generator. In normal conditions, a PV diode generates power by facing a hot sun and absorbing photons. When facing cold space and emitting photons, it still drives an internal current, which shifts a power-generating component from the normal position in the 4th quadrant of an IV sweep to the 2nd quadrant. This was experimentally verified using a temperature controlled emissive surface to an infrared optical diode separated by an optical chopper. The thermodynamics was further explored discussing various efficiency limits with the understanding the heat engine was no longer Sun to Earth via cell, but Sun to universe via Earth.

Eric Chen (ASU) gave an extended talk on enhancing internal reflectance in solar cells with angle- and energy-selective reflectors. This work introduces a modified detailed balance model incorporating the thermodynamic limit, etendue expansion, parasitic losses, and non-radiative recombination, as well as ideal and realistic back reflectors. In exploring the design space, for energy restricting optical coatings, no advantage (versus simple detailed balance results) was seen for band gap energies greater than 1.35 eV. Below that value, improvements are possible which was described comparing energy restriction and angle restriction. Matthew M. Wilkins (University of Ottawa) presented an extended talk identifying optimal band gaps for non-ideal intermediate band (IB) solar cells. Here, a new figure of merit for material quality, ν, is introduced that depends on a product of absorption and diffusion length. *Simudo*, a drift diffusion model for IB devices was made and used to explore the performance function of ν versus material band gap. The conclusion was that ν should be greater than 3.5, and bulk band gaps should target 2.2 to 3.2 eV for optimal efficiency. David K Ferry (ASU) discussed hot carrier solar cells using valley photovoltaics. The authors suggest taking advantage of known characteristics of hot carriers in semiconductors and utilize devices with a Mott barrier configuration. This allows energetically favorable extraction of carriers, excited high into the Γ valley, into metastable states in lower adjacent L valleys. This removes the need for energy selective contacts. This concept was demonstrated in a device incorporating InAlAs and InGaAs. From the data, extrapolated J_{SC} and V_{OC} were promising, but poor performance in the 4th quadrant of the IV curve suggested further complications with carrier extraction, with suggestions of future work currently within reach.

Area 2: Chalcogenide PV Roadmap (Panel)

Chuck Hages (Area 2 Chair) introduced the panel, made up of B.J. Stanbery, Heliovolt/Siva Power; Lorelle Mansfield, NREL; Wyatt Metzger, NREL; Gang Xiong, First Solar; and Xuanzhi Wu, Advanced Solar Power Inc. The panel discussed some of the recent research directions and challenges to CdTe and CIGS systems. This ranged from both device design and materials science parameters such as Ag and S alloying, dopant activation, and bandgap engineering, to manufacturing considerations including improving large area uniformity and efficient material utilization. To further advance understanding, and improve manufacturing, new non-destructive high throughput characterization methods are needed to determine band alignment, carrier density, recombination velocity, and intra-grain potential fluctuations. With more data, we can better understand e.g. disorder impact on V_{OC}, and provide insights on how to engineer solutions. However, this also requires improved theoretical understanding of defect chemistries, phase segregation, and the effects of extended defects. Specifically: for CIGS, more work is needed to understand density of states in alkali-doped alloys; and for CdTe, dopant/impurity interaction and (de)activation mechanisms.

Xuanzhi Wu (Advanced Solar Power, Inc.) discussed building integrated PV. Building energy use makes up 28% of all energy consumption, making it a major contributor to CO_2 emission. CdTe is an excellent candidate for BIPV, from its low temperature coefficient, long lifetime (vs architectural structures) and 19% efficiency allowing cost effective power less than $0.25/W. It can be made black as an external element, or semitransparent, allowing more architecturally interesting colors and patterns with several examples shown. Amit Munshi from Colorado State University discussed use of a cosublimator system for incorporating CdSeTe:As material near the rear of the structure CdSeTe devices. With some modeling, an implied V_{OC} > 980 mV was predicted, with a V_{OC} of 1.0 V within reach with poly CdTe devices. Andrea Cattoni (CNRS) presented on ultrathin $CuInGaSe_2$ solar cells with reflective back contacts incorporating ITO with ZnO diffusion layer. This structure enabled a 29.5 mA/cm^2 experimentally with 32.8 mA/cm^2 expected from simulation. Further simulation incorporating light trapping using TiO_2 nanoimprint predicts 37.2 mA/cm^2 using a 300 nm CIGS absorber with over 20% efficiency.

Area 3: Multijunction and Concentrator Technologies

Ignacio Antón (Universidad Politécnica de Madrid) gave the plenary on static concentrator modules with integrated tracking for area-constricted PV applications (e.g. building integrated (BI)/charging stations). Using micro multi-junctions and flat panel form factor, internal tracking is possible using displacement of only a few mm. This extends effective optical acceptance angles possible with conventional CPV systems which can be further integrated into hybrid modules with diffuse capture by silicon below the CPV. A further alternative (CPV with no diffuse collection mechanism) allows transmission of diffused sunlight, and is adjustable to maximize indoor light by shifting off the micro CPV, and diffusing the sunlight through. The European *Hiperion* project pilot production line, along with Insolight, is investigating highly efficient hybrid CPV/PV modules across countries and industry. 36.4% efficiency at 180x suns under real outdoor conditions was demonstrated.

Felix Predan (Fraunhofer ISE), a student award finalist, presented on a 4-junction wafer bonded GaInP/GaAs/GaInAs//GaSb device with a concentrated efficiency of 43.8%. The ideal bandgap combination presented here (1.9 eV/1.4 eV/1.0eV/0.7eV) has a potential for a 64.5% detailed balance efficiency at 500x taking into account expected radiative limits in each junction. Device EQE showed current densities over 12 mA/cm^2 in each sub-cell. Based on simulations, with some modifications/optimizations, a 50.8% efficiency device is within reach. Wondwosen Metaferia (NREL) gave an extended talk on the incorporation of Al in NREL's dynamic hydride vapor phase epitaxy (HVPE) system. So far, GaInP devices suffer because the necessary window materials (Al-containing) have not been possible due to reactivity of AlCl. Here, $AlCl_3$ was presented as an alternative and used to grow AlGaAs. As a front surface field (FSF) for a GaAs solar cell, it yielded similar external quantum efficiency to a GaInP FSF. While there are still improvements to make, this previously "practically impossible" method has now been proven possible. Finally, the first report of Al-phosphide growth by HVPE up to 2.62 eV was presented. Tarun Narayan and Leah Kuritzky (Antora Energy) presented a world-record demonstration of a >30% thermophotovoltaic (TPV) device. Antora Energy is working towards higher heat systems to act as batteries by electrically heating carbon blocks up to temperatures > 1100 °C at the MW scale. Heat energy is discharged using TPV, which are water cooled to maintain operational temperatures below 100 °C. The proposed system was demonstrated using single junction InGaAs and GaAs devices sourced from NREL. Peak efficiencies of 30% (1300 °C, InGaAs) and 31% (2330 °C, GaAs) TPV were shown.

Area 4: Silicon Photovoltaic Materials and Devices

In Area 4 'Crystalline silicon PV technology' Gabriela Bunea of GAF Energy gave the plenary presentation. In her speech entitled 'It is time to integrate roof & solar' she showed inspiring examples of how the roofing business and PV business can be merged. She shared the companies' experiences and vision on bringing elegant, roof integrated solar options to the American homeowners. The company uses a 60-cell, 360-watt laminate from Solaria with a custom frame that allows it to be waterproof with a lower profile and faster installation. This combined installation benefits from having only one crew for both roofing and integrated PV to realize lower system costs.

Many presentations focused on oxide/polysilicon passivation contacts in area 4 showed that this is currently the hot research topic in the crystalline silicon PV field. A nice example among these contributions is the research from IMEC Belgium presented by Sukhvinder Singh. His work aims at the development of the building blocks for the integration of polysilicon-based passivating contacts in co-plated n-PERT solar cells. Singh showed that both n-poly and p-poly layers could be simultaneously achieved by the sintering of i-poly layers during the $POCl_3$ diffusion and the autodoping from an existing B-doped emitter, respectively. State of the art dark saturation current density values with very high uniformity were measured for n-poly, auto doped p-poly, and boron emitter. The viability of a laser oxidation process to pattern the front p-poly Si layer without measurable damage was demonstrated. Finally, a laser ablation and plating process leading to a

very low specific constant resistivity was demonstrated.

The strength of the IEEE PVSC conferences is the solid base of fundamental research presented, even in an area that covers a mature and commercially dominant technology as c-Si PV. A nice example was the work presented by Rachel Woods from UC Berkeley on novel selective carrier contacts. Her work was focused on exploring wider band gap materials to reduce parasitic absorption of the front contact of silicon heterojunction (SHJ) solar cells. When choosing such a material, hole mobility and valence band (VB) offset with crystalline silicon (c-Si) are often used as starting criteria, but several other material parameters can also influence band bending at the contact interface. Rachel applied a combination of simulation and experiments to suggest future p-type carrier-selective contacts and a better understanding of materials selection criteria in SHJ cells. She found a strong influence on fill factor from thickness, doping, and valence band position, and on V_{OC} from surface defect density. Multi-parameter sensitivity analyses demonstrate that higher valence band offsets can be tolerated at higher dopings. These findings were demonstrated using SHJ cells with a hole selective contact of p-type NiO_x, an underexplored material for SHJ.

Another nice example of fundamental research was the presentation of Sam Jafari from UNSW in Australia. He reported on his new insights related to the boron-oxygen (BO) related light-induced degradation of boron-doped Czochralski (Cz) silicon solar cells. This study highlights the fact that despite decades of LID-related research, new insights can be obtained when using new approaches, such as those presented in this paper. He presented his finding of a transformation between minority carrier trapping and recombination active centers. A minority carrier trap was revealed in the annealed state of boron doped Cz that is removed after degradation. This trap appears to act as a precursor for the BO defect as it is removed at the same rate as the BO defect is generated.

Area 5: Characterization Methods

Teresa Barnes (NREL) gave the plenary presentation on DuraMAT, a research consortium focused on precompetitive research needs in module packaging incorporating four core national labs (NREL, Sandia, Berkeley and SLAC) along with university and industry researchers and an industrial advisory board. Degradation rate vs time has many components, some may be recoverable (PID), some factors may fall off quickly at startup and level off (LeTID), and some may be unrecoverable (cracks). Failures missed by current tests include backsheet cracking, potential induced degradation, grid finger corrosion and delamination, light and elevated temperature induced degradations, snail trails, and delamination. DuraMAT resource consists of core areas: central data resource; multi-scale, multi physics modeling; field module forensics; disruptive acceleration science; and module material solutions. This work utilizes "big data" and high performance computing methods to better develop accelerated tests, understand the results, identify failure modes, and understand materials to speed up the learning cycle. Oki Gunawan (IBM) gave an extended oral presentation on the carrier-resolved photo-hall effect, utilizing a rotating dipole line system for camelback potential carrier confinement. Using lock-in amplification and Fourier transforms, it is possible to characterize a wide range of parameters including recombination lifetime, diffusion length (minority and majority), as well as carrier type, mobility, and density from a single tool. Yoann Buratti (UNSW), a student award finalist, discussed deep learning of electroluminescent (EL) images for end-of-line binning of full and half cells. A data set of 20,000 EL images, with associated IV curves, was used to train a convolutional neural network to bin devices by efficiency bins with actual vs predicted accuracy with an R^2 of over 0.9.

Area 6: Perovskite and Organic Solar Cells

Next to offering the tutorial on perovskite PV technology, Mike McGehee gave a nice presentation on the current status and challenges of this exciting PV technology in Area 6. He discussed the progress at developing both low and high band gap perovskites for tandem solar cells. Both highly stable low band gap cells with greater than 19% power conversion efficiency and triple halide high band gap cells with >20% stability that do not suffer from light-induced phase separation have been realized. In addition, McGehee presented fundamental insides on high band gap perovskites: if Br is used to shrink the lattice, a significant amount of Cl can be incorporated. Cl helps raise the band gap, passivate defects and improve mobility. Overcoming the self-limiting redox reaction between an interface of NiO and perovskites, the adding of a few percent excess of Al was presented to prevent the formation of PbI_2. In addition he shared the results on perovskite-Si tandems with >27% efficiency and all-perovskite tandems with >23% efficiency. This was an excellent introduction to the various hybrid multi-junctions as discussed in great detail in the joint session between Area 3, 4 and 6 entitled 'Battle Royale on Hybrid Tandem Solar Cells'.

Crosscutting: Battle Royale on Hybrid Tandem Solar Cells

Marko Jost (University of Ljubljana, Helmholtz-Zentrum) discussed a 1.68 eV perovskite/CIGS tandem. A Fraunhofer certified 24.2% efficiency was shown, a record for this material

system! To further characterize this, as well as understand long-term stability, a 2-color led light source at 470 nm and 940 nm was developed. This allows individual biasing of Si or CIGS bottom cells to investigate the top perovskite, and vice versa, using full IV curves under different illumination levels. Examining optical optimization on Si or CIGS bottom cells, the top perovskite cell requirements are the same (thickness, Eg), and both systems allow efficiency gains over non-tandems. Incorporating insolation and weather data, a Si-tandem is predicted to perform 6% lower than CIGS.

Frank Dimroth (Fraunhofer ISE) presented a wafer-bonded 34.1% GaInP/AlGaAs//Si tandem incorporating a nanostructured resist with silvered back layer for increased absorption in the Si substrate. Improvements from previous designs included a rear heterojunction top cell, and AlGaAs for middle cell instead of GaAs for better current matching. Two methods were investigated: in the first one, a top tandem was grown inverted, then flipped, bonded to Si, and the GaAs substrate was removed. For the second method, the upper tandem was grown upright on GaAs, then bonded sapphire handle, after removal of the GaAs substrate and CMP, the Si bottom cell was bonded and the sapphire handle was removed. Across wafer uniformity was better in method 1, but better champion devices were obtained in method 2.

Saba Gharibzadeh (KIT), a student award finalist, discussed perovskite based tandems as a path towards 35% efficiency, focusing on voltage loss, reducing non-radiative recombination, and improving surface passivation. Utilizing a 2D/3D perovskite heterojunction, a stable V_{OC} of up to 1.31 V was shown. A full 4-terminal tandem with a Si bottom cell demonstrating 25.7% stabilized efficiency was demonstrated, beating the standalone Si cell. Using an alternative ITO/IZO system for improved transparency over 80% may lead to an efficiency of 27.4%.

Jason Yu (ASU) discussed blade-coated perovskites on textured silicon, built on ASU's development of fully textured tandems, using a solution processed perovskite instead of vacuum deposition for improved manufacturability. Wet etching was used to develop sub-micron sized pyramids on the Si surface, followed by a blade coating process to apply PTAA and perovskite. The effects of including DMSO were presented which can limit voids in the final morphology if included in the correct proportions. A textured PDMS top structure was also used to reduce reflectance. Finally, a 26% tandem device using these features was demonstrated with J_{SC} matched at over 19 mA/cm^2.

Daniel Lepkowski (OSU), a student award finalist, discussed strategies for >23% GaAsP:Si tandem by MOCVD. Recent devices have shown 23.35% efficiency (NREL certified), which is a 10% absolute improvement from the first demonstration of this system 5 years ago. Experimental results of test structures were fit, and used to understand the effects of threading dislocations density on performance. Very recently, a GaAsP top cell was grown with a TDD of $3 \oplus 10^6$ cm^{-2}, projecting 1.27 V at 18.5 mA/cm^2. Using this relationship, it is reasonable to expect efficiencies of >27% for this device once fabricated.

Tony (Shizhao) Fan (UIUC) presented a 25.0% GaAsP/Si tandem by MBE. Using a similar structure to the previous talk, this work focused on reduction of threading dislocations and dark line crystal defects as monitored by EBIC in the 1.7 eV GaAsP top cell. Through incorporation of a non-optically active GaAsP spacer between the metamorphic grade and active layers, as well as an AlGaAsP BSF instead of GaInP, a reduction in defects was shown at the cell level, resulting in a 25% efficient device now. A near term 27% efficiency was predicted through optimizing device doping to further boost V_{OC}.

Area 7: Space and Specialty Technologies

James Kinnison (John Hopkins University Applied Physics Laboratory) gave the plenary on the Parker Solar Probe mission, which just completed its 5th encounter with the sun. Originally proposed in 1958, after 50 years of concepts the current mission, previously known as "Solar Probe Plus", it measures the properties of the solar corona, the acceleration of the solar wind, and mechanisms that create the solar energetic particle environment. The spacecraft requires a substantial heat shield, which shadows the majority of the components. The PV are some of the only components directly facing the Sun. To maintain operation near 150 °C, the PV panels were mounted on an electrically isolated, thermally conductive ceramic, which was water cooled. The arrays split into two sub-sections on movable flaps, a primary one which is completely shaded at closest approach, and a smaller secondary one which gets glancing incidence irradiation. When near Venus, the flaps are extended for complete illumination. Now, 2 years into the mission, performance is exceeding expectations. This mission has returned some impressive data on turbulent coronal flow out from the Sun, as well as other information about the solar environment not possible to observe without being up close.

Bao Hoang (Maxar Infrastructure) discussed orbit raising to GEO using electric propulsion which allows for an 8x increase in specific impulse versus bulky chemical propellants on board, at the cost of extended time spent in high-radiation belts during this transit. This was simulated against several approaches (super-sync and sub-sync) using a variety of models (AE8, AP8, and IRENE (AE9/AP9)) to predict on-orbit performance and degradation of solar cells. Stephen Polly (RIT) presented on the integration of a longpass distributed Bragg reflector ((LP)DBR) below the

middle junction of an inverted metamorphic triple junction for improved radiation tolerance and lattice matching. The LPDBR suppresses parasitic sub-gap reflectance, and a wide range of device designs (DBR, LPDBR, subcell thickness) were simulated in Synopsys Sentaurus, ultimately showing efficiency gains for a thin device incorporating equivalently thick LPDBR vs a traditional DBR. Justin Lee (The Aerospace Corporation) discussed on-orbit results from the AeroCube-10 experiment, for quantitative comparison of solar cell degradation measured *in situ* against modeled, data-driven predictions. It uses a solar cell matrix of varying coverglass thicknesses, dosimeters, and a micro charge particle telescope. Early results show a wide range of data of space environment and solar cell performance, including the 2019 Labor Day storm. This experiment is returning lots of data, and more in-depth analysis and application to on-orbit modeling is still to come.

Area 8: PV Modules Manufacturing and Applications

Itai Suez (Silfab Solar) gave plenary on the emergence of back-contact electro-conductive back sheets. This technology provides structured connections to any back-contact cell technology, and enables the highest power density of any current modeling technology, including shingling, by very close packing of cells without wires or ribbons. A lower temperature interconnect process than typical soldering, it also reduces thermal expansion mismatch between components, leading to higher reliability as demonstrated with dynamic mechanical load, thermal cycling testing, and humidity freeze/thaw cycling results. These modules also run cooler due to the larger lateral conductive area for heat spreading of foils versus traditional polymers. To quantify this, two identical systems (modules, racking, fixed tilt angle, etc.) were simulated in PVSyst at two locations, Las Vegas, and Boston. The conductive back contact system had 2.5% more energy production in Las Vegas (high irradiance, hot day), with 2.7% increase on annualized basis. This was partially from lower temperature, partially from better low light performance. In Boston (lower temperature, lower intensity) there was 4.3% more production on the best day and 3.1% better annualized for the conductive back contact device, showing improvements in multiple environments.

Ian Slauch (University of Minnesota) discussed modeling spectrally-selective reflection in bifacial modules to reduce parasite absorption. Using an idealized case of reflecting 1200 nm and longer, >3 °C cooling is possible for an Al BSF cell, and slightly less for PERC. Realistic mirrors can give 2% more energy and operate 1.5K cooler using realistic stacks of dielectric materials. For bifacial, up to a 3.9K temperature reduction is possible depending on irradiance conditions. Keith McIntosh (PV Lighthouse) presented on simulation and measurement of mono- and bifacial modules in a 1D tracking system using a testing array in Albuquerque, NM. SunSolve was used for simulation, using 3D ray tracing (to account for e.g. frames), a SPICE model, along with the same temperature modules used by PVSyst. Simulations showed and identified sources of non-uniformity in current generation. Silvana Ayala Pelaez (NREL) discussed a field-array benchmark of commercial bifacial PV technologies using publically available data from a 75 kW single axis tracking array at NREL. Results show that the SHJ performs best in the summer when it can run cooler, PERC operated best in the winter with higher albedo from snow with the added benefit that bifacial modules power during cloudy snowy days when monofacial do not. Sanghyuk Lee (Korea Polytechnic University) introduced us on how to use Tetris as a new approach to automated configuration and interconnection layouts for building integrated modules at large scale. A building geometry was modeled to make the most efficient use of light throughout the year, using a polyomino approach which generates Tetris-like shapes which can be easily interconnected with neighbors and build into large standard grids. With the Fraunhofer ISE main building as a test-case, modeling single string layouts, landscape layouts, portrait layouts and polyomino defined layouts, as much as 2.9% improvement in performance was shown for the polyomino design. This paper was awarded the best student presentation in Area 8.

Area 9: PV Modules and System Reliability

Arathi Gopinath (Nextracker) gave the plenary, discussing reactive versus proactive operation and maintenance modalities in the age of mass solar deployment. Weather related events are the number one source of PV insurance claims, which is only increasing due to global climate change. With a goal of 100% up time, preventative maintenance, and the prediction for the need of that maintenance is critical. Nextracker utilizes a wide range of data sources for tracking PV systems, which provide visibility of how a plant is operating, provide insights to understand failure mechanisms, and enable foresight into predicting failures well before they happen to maximize uptime.

Dirk Jordan (NREL) presented a detailed analysis of temperature and installation effects of PV system failures from fleet performance of 100,000 PV systems across the US. These data enable understanding of rates of various hardware faults such as inverter, breaker, wire, ground fault etc., all broken down by scale (residential, commercial, utility). A major find was inverters have significantly lower failure rates when installed in shaded positions. The good news is most systems perform as expected, within 80–90% of their predicted value. Xiaohong Gu (NIST) introduced a method for predicting long term

performance of PV backsheets, linking lab-based experimental exposure with outdoor service performance. This work focused on the PET outer layer, exploring UV (various wavelengths), temperature, and humidity exposure. Damage from carboxylic acid formation and yellowing increases as UV photon energy increases. Humidity does not act alone as a damage factor, but enhances damage caused by UV. This was used to create a predictive model, which shows a close match to data from Arizona, with further granularity in humidity data is needed for matching data from Florida and Maryland data. Nick Bosco (NREL) gave an extended talk on multi-scale modeling of electrically conductive adhesive interconnects for reliability testing. These interconnects are used to bond and connect cells in shingled modules. Traditionally used maximum stress theory is too general for this case, so an alternative approach of strain energy release rate was used to model cohesive and adhesive failures. Determining an accurate stress-free temperature is critical, allowing strain to return to initial minimums after simulated temperature changes. 3D simulations were used to find areas of most interest, which defined boundary conditions for 2D sub-models to explore debond driving force versus growth rate, saving computational time.

Area 10–12: Towards 100% Renewable Energy Special Session

Nancy Haegel (NREL) gave the plenary on trajectories and challenges to TW scale electricity generation with PV. With total energy average power of 18.4 TW in 2018, 3.0 TW was electricity, and 0.066 TW (2.2–2.5%) was PV. Utility scale LCOE is competitive now vs traditional sources around the world, citing US, Germany, and Japan. Further recent work looking at 100,000 systems in the United States, says that most perform as expected, showing a highly reliable product. Progress in efficiency and reliability is working, but there's still work to do to exceed the detailed balance limit and realize the impact of third-generation, tandem, and III-V technologies. TW scale has new challenges, which need to be addressed, including how to deal with PV waste, material availability, Ag reduction/replacement and PV recycling? We need sustainable growth models. At the grid-level, small scale (island) 100% RE is possible and currently demonstrated, but more difficult at larger scale. There is a need for better stability with inverter-based resources, better instantaneous power delivery, and storage such as batteries, pumped hydro and solar fuels.

Next, Marta Victoria (Aarhus University) discussed the synergy with wind and solar towards decarbonization. Marta presented a model incorporating energy storage, transmission, and sector coupling to balance cost and capabilities across Europe. The model contrasted the geographic preference for PV and battery storage in southern countries, with wind and H_2 storage in northern countries. Keiichi Komoto (Mizuho Research Institute) discussed decarbonizing transport. Approaches must consider the source PV generation, the end-use in an electric vehicle (EV) battery, and transfer through any intermediaries such as the grid, storage, and charging stations. Matthew Stocks (Australian National University) explored decarbonizing the urban environment using renewable energy. Energy demands of cooling (air conditioning) dominate within +/- 35 degrees latitude, which encompasses 70% of the world population. More effort is required in suitable seasonal storage mechanisms. Christian Breyer (LUT University) discussed decarbonizing industrial processes which account for 27% of all greenhouse gas (GHG) emissions, and in most of the specific sub-sectors; substitutions are possible to eliminate GHG using "power-to-x" converting electricity to hydrogen, fuels, and feedstocks. This led to a deeper dive on specific industries: chemical, cement, iron and steel, aluminum, and pulp and paper; most of these CO_2 emissions can be eliminated or entirely re-captured.

Special Session on Hot Carrier Solar Cells: Current Status and Bottlenecks

Ian Sellers (University of Oklahoma) moderated a panel (Gavin Conibeer, University of New South Wales; Stephen M. Goodnick, Arizona State University; Jean Francois Guillemoles, IPVF, France; Louise C. Hirst, University of Cambridge; Art Nozik, University of Colorado/NREL) to discuss progress and challenges to the hot carrier solar cell concept, a mechanism to reduce thermalization loss by capturing energy from photons with energies well in excess of the material band gap, normally lost to photons. This technology has the potential to more than double the ~30% detailed balance limit to over 60% efficiency. Panelists discussed the importance of fundamental research, and how carrier and phonon interaction keeps revealing itself to be more complicated as it is investigated. While particular material systems may come into play for cost effectiveness or manufacturability (CIGS, Si, perovskites) hot carrier concepts are not necessarily competing, but can be a complimentary aspect of these devices. The panel discussed the two ways hot carriers can be used, through carrier selective contacts to extract high voltage, or through multiple exciton generation that creates more current through an impact-ionization like process. Topics flowed from valley scattering as a mechanism of slowing down carrier relaxation through bandgap engineering, to thermoelectric devices and how they relate to hot carrier devices. The panel closed on the topic of materials, including nitrides, hydrides, anisotropic materials, and on developing a "new concepts in PV" roadmap and round-robin testing of materials between labs. Finally, a challenge was put to the community to produce hot

carrier devices able to participate in the Si-tandem Battle Royale!

Closing Remarks

While the normal roster of social events and activities planned for Calgary were put on hold this year, we were still able to hold the signature Sun Run 5K race virtually! Participants all ran a 5K in their home locations during the 1st week of the conference and sent in their official times. Congratulations to all of this year's participants, a summary of the event can be found at the PVSC-47 website. As well, this year marks the 40th year of the Sun Run, all thanks to Dr. Larry Kazmerski, who has been organizing this event at the PVSC since 1980. On behalf of all the PVSC community, thank you to Larry for organizing, hosting and bringing so much fun to the PVSC!!

Dr. Larry Kazmerski has been organizing and hosting the PVSC Sun Run since its inception in San Diego in 1980!

The authors acknowledge the full Program and Organizing Committees of the PVSC-47, for bringing together this virtual conference in a very short period of time! Without such a dedicated team, the PVSC would not be possible. We also thank the many authors and presenters who chose to present their outstanding work at PVSC-47, despite the difficult times. Next year the PVSC will be held at the Diplomat Beach Resort near Miami, Florida from June 20–25, 2021.

This article was prepared by Dr. Stephen Polly, the PVSC-47 Daily Highlights Coordinator, Dr. N.J. Ekins-Daukes, PVSC-47 Assistant Daily Highlights Coordinator, Dr. Arno Smets, the PVSC-47 Technical Program Chair, and Dr. Seth Hubbard, the PVSC-47 Conference Chair.

Review of The 2020 IRPS

By Ben Kaczer

The IEEE International Physics Reliability Symposium (IRPS) has been the premiere conference for engineers and scientists to present new and original work in the area of microelectronics reliability for almost 60 years. Drawing participants from the United States, Europe, Asia, and all other parts of the world, IRPS seeks to understand the reliability of semiconductor devices, integrated circuits, and microelectronic systems through an improved understanding of both the physics of failure as well as the application environment.

The 2020 IRPS was originally scheduled to be held at the Hilton DFW Lakes Executive Conference Center, Dallas, TX, between March 29 and April 2, 2020. Due to the COVID-19 pandemic, the conference had to be converted to a virtual event starting on April 28 and running until May 30, 2020—the duration of which the recorded presentations were accessible to the registrants. The virtual event was attended by more than 400 participants.

The conference encompassed a wide range of topics, ranging from Circuit Reliability and Aging, Emerging Memory Reliability, ESD and Latchup, Failure Analysis, Gate/MOL Dielectrics, IC Product Reliability, Memory Reliability, Metallization/BEOL Reliability, Neuromorphic Computing Reliability, Packaging and 2.5/3D Assembly, Process Integration, Reliability Testing, RF/mmW/5G Reliability, Soft Error, System Electronics Reliability, Transistor Reliability, to Wide-Bandgap Semiconductors- GaN. The 2020 Special focus topics were Circuit Reliability and Aging (EDA Tools, Sensors, and Aging Aware Designs), Wide Bandgap Devices (with emphasis on the Reliability of SiC Devices), Reliability issues of Neuromorphic Computing, and Reliability of RF/mmW/5G Devices (CMOS, SiGe BiCMOS, SOI, GaAs).

The conference opened traditionally with two days of Tutorials, which allowed both newcomers and experts to familiarize themselves with new topics or just to refresh their existing knowledge. The Tutorial instructors are authorities in their respective reliability fields—either veteran IRPS presenters for established topics or invited specialists in emerging topics. The first two tracks of "Basics of Semiconductor Reliability" included Basic Reliability Physics, Bias Temperature Instabilities, Self-heating, Terrestrial

Radiation, Plasma-Induced Damage, Electromigration, and Materials Analysis Techniques in Semiconductors. A track of Tutorials on "Memory Reliability" included the topics of Charge Trap Memories, MRAMs, and Phase Change Memories, and was followed by "Power Devices Reliability" Tutorials on GaN Power Devices, and Power IGBT Modules. The last Tutorial track on "Circuit & System Reliability" covered the Introduction to RF and Mixed-Signal Circuit Reliability, Designing for Analog Reliability, and BTI-HCD Reliability Framework.

The Tutorials were followed by Year-In-Review, a segment always appreciated by IRPS attendees, allowing them to quickly catch up on recent developments in multiple areas. In this year's Year-in-Review several speakers covered the past year of literature on Circuit Reliability, including the EDA aspects, RF/mmW/5G Reliability (CMOS/SiGe and GaN HEMT) and Memory Reliability.

The conference proper started with a live welcome address by the General Chair Prof. Gaudenzio Meneghesso, University of Padova, Italy, and an Overview of Technical Program by the Technical Program Chair Dr. Charles Slayman, Cisco Systems, USA. The subsequent Plenary Keynotes were

- Dr. Mike Mayberry, Chief Technology Officer, Intel, USA—The Future of Compute: Reliability and Resiliency in the era of Data Transformation
- Dr. Oliver Häberlen, Senior Principal, Infineon Technologies, Austria—Power Semiconductor Reliability—An Industry Perspective on Status and Challenges
- Dr. Gianluca Boselli, Analog ESD Lab Manager, Texas Instruments, USA—Power scalability challenges in High-Voltage ESD Design

The bulk of the conference then consisted of the presentation of 105 Oral (of which 16 were Invited) and 77 Poster papers, previously selected by 17 subcommittees from 239 contributed submissions. Due to the virtual nature of the conference, the papers were typically presented as prerecorded video clips. Poster presenters were allotted limited time to introduce their work and, to emulate the poster session experience, they could discuss their work with interested audience members in separate video calls.

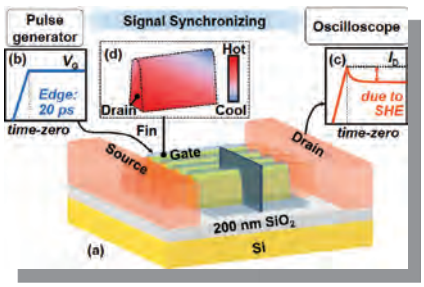
Unfortunately, some popular events, such as the evening IRPS Workshops and a lunch Panel were cancelled due to having to convert the conference relatively abruptly to the virtual format.

The IRPS subcommittees highlighted the following contributed papers:

- C. Prasad *et al.*, Intel—Silicon Reliability Characterization of Intel's Foveros 3D Integration Technology for Logic-on-Logic Die Stacking
- E. Landman *et al.*, ProteanTecs—A novel approach to in-field, in-mission reliability monitoring based on Deep Data
- T. Grasser *et al.*, TU Wien—The Mysterious Bipolar Bias Temperature Stress from the Perspective of Gate-Sided Hydrogen Release
- J. B. Roldan *et al.*, Universidad de Granada—Reversible dielectric breakdown in h-BN stacks: a statistical study of the switching voltages
- Yao-Feng Chang *et al.*, Intel—eNVM RRAM reliability performance and modeling in 22FFL FinFET technology
- T.Y. Lee *et al.*, GLOBALFOUNDRIES—Magnetic Immunity Guideline for Embedded MRAM Reliability to Realize Mass Production
- Tae-Young Jeong *et al.*, Samsung Electronics—Reliability on EUV Interconnect Technology for 7 nm and beyond
- Yiming Qu *et al.*, Zhejiang University—In-Situ Monitoring of Self-Heating Effect in Aggressively Scaled FinFETs and Its Quantitative Impact on Hot Carrier Degradation Under Dynamic Circuit Operation
- T. Uemura *et al.*, Samsung Electronics—Investigating of SER in 28 nm FDSOI-Planar and Comparing with SER in Bulk-FinFET
- Heung-Kook Ko *et al.*, Samsung Electronics—Early Diagnosis and Prediction of Wafer Quality using Machine Learning on sub-10nm Logic Technology
- Hai Jiang *et al.*, Samsung Electronics—Advanced self-heating model and methodology for layout proximity effect in FinFET technology
- Huimei Zhou *et al.*, IBM—NBTI Impact of Surface Orientation in Stacked Gate-All-Around Nanosheet Transistor
- Sandeep R. Bahl *et al.*, Texas Instruments—A Generalized Approach to Determine the Switching Lifetime of a GaN FET
- M. Sampath *et al.*, Purdue University—Constant-Gate-Charge Scaling for Increased Short-Circuit Withstand Time in SiC Power Devices

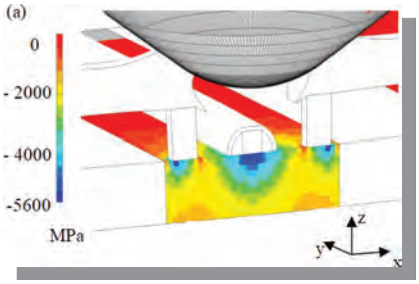
After the conference, the following Awards were announced:

- **Best Paper:** Yiming Qu *et al.*, Zhejiang University—In-Situ Monitoring of Self-Heating Effect in Aggressively Scaled FinFETs and Its Quantitative Impact on Hot Carrier Degradation Under Dynamic Circuit Operation

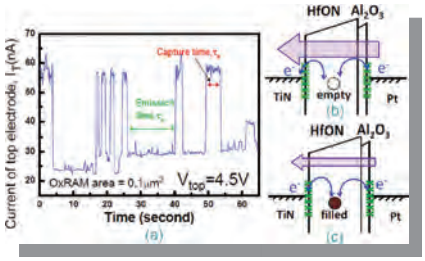


Self-heating effect (SHE) in aggressively scaled SOI FinFETs is experimentally and quantitatively investigated by using a sub-nanosecond characterization technique.

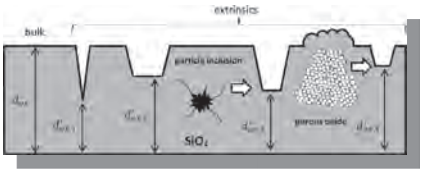
- **Best Student Paper:** A. Kruv *et al.*, imec—On the impact of mechanical stress on gate oxide trapping



Detrapping from individual gate oxide defects is studied under externally-applied local mechanical stress up to ~5 GPa.



Random Telegraph Noise is used to locate traps during the breakdown process in OxRAM dielectric layer.



SiC gate-oxide reliability is governed by extrinsic failures due to tiny distortions in the gate-oxide, which act as local oxide thinning.

- **Best Poster Paper:** E. R. Hsieh *et al.*, *National Chiao Tung University*—A Pulsed RTN Transient Measurement Technique: Demonstration on the Understanding of the Switching in Resistance Memory
- **Best Virtual Presentation:** T. Aichinger and M. Schmidt, *Infineon Technologies*—Gate-oxide reliability and failure-rate reduction of industrial SiC MOSFETs

Next year, IRPS 2021 will be again a virtual event taking place from March 21 to March 25, 2021. More information can be found on https://irps.org/.

Ben Kaczer is IRPS 2021 Publicity Chair and Scientific Director at imec

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Upcoming Technical Meetings

5th IEEE Electron Devices Technology And Manufacturing (EDTM) Conference 2021 March 9–12, 2021, The Century City International Convention Centre in Chengdu, China

HTTPS://EWH.IEEE.ORG/CONF/EDTM/2021/

The IEEE Electron Devices Technology and Manufacturing (EDTM) Conference 2021 is a four-day meeting to be held at The Century City International Convention Centre in Chengdu (China) from March 9–12, 2021. EDTM is a premium conference sponsored by the IEEE Electron Devices Society that provides a unique forum to discuss and collaborate on a broad range of device/manufacturing-related topical areas including materials, processes, devices, packaging, modeling, reliability, and manufacturing and yield. Since its birth in 2017, EDTM has always been an excellent platform to establish contact and collaboration with the vibrating manufacturing community. In its 5th edition EDTM will be held for the first time in China, under the main theme: *Intelligent technologies for smart and connected life.*

Technical Sessions

The EDTM 2021 solicits papers in all types of exploratory device concepts within the following broad technical areas:

- Materials
- Process and tools for Manufacturing
- Semiconductor devices
- Memory technologies
- Photonics, imaging and display
- Power and energy devices
- Modeling and simulation
- Reliability
- Packaging and heterogeneous integration
- Yield and manufacturing
- Sensor, MEMS and Bio-electronics
- Flexible and wearable electronics
- Nanotechnologies
- Disruptive technologies—internet of things (IoT), artificial intelligence (AI), machine learning (ML), neuromorphic & quantum computing

World-class researchers in all areas will deliver invited talks, and submissions will be evaluated for oral and poster presentation. Authors should indicate their preference for oral or poster presentation format when submitting their abstracts.

Publications

EDTM 2021 papers will be subjected to IEEE EDS standard review processes and IEEE conference publishing guidelines. The accepted papers presented at the meeting will be published in the EDTM 2021 proceedings and may be available on IEEE *Xplore*. Besides, the authors of a selected number of high-impact presented papers will be invited to submit an extended version of the same for the consideration of publication in the *IEEE Journal of the Electron Devices Society* (J-EDS). All such submissions must comply with J-EDS author guidelines and will be subjected to the standard IEEE and J-EDS review and publication policy.

Short Courses and Tutorials

EDTM 2021 will start with a set of short courses and tutorials on March 9, 2021. Tutorials teach selected topics from the basics to the state-of-the-arts, allowing the attendees to catch up a topic quickly. Short Courses discuss the latest research and challenges on hot and advanced topics encompassing the EDTM 2021 theme, including heterogeneous integration, artificial intelligence (AI) and machine learning (ML), internet of everything (IoET), 5G+, autonomous systems, industry 4.0, future computing and quantum information processing, all enabled by electron devices.

Important Dates

October 25, 2020: Abstracts submission deadline
December 20, 2020: Notification of acceptance

COVID-19 Watch

Chengdu remains safe. EDTM 2021 is planned as an in-person/on-site event. Meanwhile, we are closely monitoring the development of the global COVID-19 outbreak. A contingency plan will allow virtual presentations and participation for those with travel restrictions and concerns. Both safety and participation experiences will be ensured for EDTM 2021.

Mario Lanza
Soochow University, China
EDTM 2021 Publicity Co-Chair

2021 IEEE Photovoltaics Specialist Conference (PVSC)

Diplomat Hotel, Bay view

It is our great pleasure to invite you to attend the 48th IEEE Photovoltaics Specialists Conference, which will be held from June 20–25, 2021, at the Diplomat Hotel near Miami, Florida, USA.

We live at a special time when solar electricity has become cost competitive with conventional electricity in many locations, enabling remarkable growth of the industry. As was the case in 2019, solar was the biggest contributor to net expansion of electricity generating capacity in 2020. In fact, the IEA PVPS has recently reported that worldwide solar installed capacity has now crossed the half TW mark! The 48th IEEE PVSC will help sustain this fantastic momentum with hundreds of technical papers from around the world, reflecting today's dynamic and expanding markets. The PVSCs have a rich tradition of bringing together students, innovators, researchers and PV leaders in a vibrant and highly integrative forum to share information, gain knowledge, strengthen collaborations and move forward photovoltaic science and technology from basic and applied research into large scale manufacturing and deployments.

If you would still like to contribute technically, please submit your abstract before our late news deadline on April 25, 2021.

Continuing with the tradition of the past few years, the 48th IEEE PVSC will be divided into 12 technical areas covering cutting-edge developments in science and engineering of photovoltaics, ranging from fundamentals to applications, with an emphasis on material science, devices, systems, solar resources and policy related matters. PVSC-48 aims to be a highly interactive venue for both seasoned PV experts as well as entry-level professionals and students. The conference provides a unique opportunity to meet, share and discuss PV-related developments in a timely and influential forum. Please consider contributing to PVSC's tradition as the premier international conference on PV science and technology and help us propel the world towards power from the Sun. As well, we will be presenting the prestigious William R. Cherry Award, honoring the photovoltaics communities' most outstanding scientist or engineer as well as the Stuart R. Wenham Young Professional Award for individuals who have made significant contributions at an early stage of their career.

We are very excited to host our conference at the Diplomat Hotel, near Miami, Florida. Conveniently located next to both the Miami International Airport and the Fort Lauderdale International Airport, the Diplomat Hotel will offer a convenient location to enjoy both the conference and the surrounding attractions, starting with direct access to a private beach, 3 pools, 9 restaurants as well as an Ambassador kids club. As usual with PVSC, we will have a fantastic companion program, with an Everglades National Park tour and alligator sightseeing, a riverboat tour, visits to the beautiful flamingo gardens, and the famous gulfstream racetrack, casino and luxury shopping, as well as many golf courses.

The conference Exhibition will showcase the latest developments in PV characterization and manufacturing equipment, and is set to further enhance attendee awareness on latest tools and instrumentation as well as to facilitate exchange between scientists, technical experts and exhibitors.

Don't miss out on the opportunities offered by the conference social gatherings and networking events to get to know your colleagues better, reconnect with old friends and make new ones. The week kicks off with our Exhibitor Reception on Monday evening at the Convention Center and will conclude with a Conference Reception on Thursday evening.

On behalf of the Organizing, Cherry, and International Committees, we look forward to welcoming you to the 48th PVSC in Miami, Florida!

Further details and registration can be found at https://www.ieee-pvsc.org/PVSC48/

Sylvain Marsillac
Conference General Chair
Old Dominion University

2021 IEEE International Memory Workshop (IMW)

The 13th International Memory Workshop (IMW) will be held online as a virtual event from May 16—May 19, 2021, due to the outbreak of COVID-19. The history of the IMW dates back to the NVSMW (Nonvolatile Semiconductor Memory Workshop) which began in 1976 and which later merged with the ICMTD (International Conference on Memory Technology and Design) to become the IMW. The IMW is sponsored by the IEEE Electron Devices Society and meets annually in May. The workshop covers all types of memory technology, is focused on advancing innovation in memory technology, and is organized in a way that provides excellent professional development and networking opportunities for attendees.

The IMW is the premier international forum for both new and seasoned technologists having diverse technical backgrounds to share and learn about the latest developments in memory technology with the global community. The scope of workshop content ranges from new memory concepts in early research to the technology drivers currently in volume production as well as emerging technologies in development. Topics include new device concepts, technology advancements, scaling and integration, circuit design and reliability, as well as emerging applications. Consistent with the increased importance of memory system architecture and integration, the workshop also includes increasing coverage of the systems in which memories are deployed and the co-evolution of memory technology along with memory systems and applications.

The IMW is the preeminent forum covering the latest developments, innovations, and evolving trends in the memory industry. Typical workshop attendance exceeds 250 attendees, and the technical program begins with a full day short course given by distinguished experts that provides an excellent professional development opportunity for both new and experienced technologists. The single-track technical program spans three days and includes an evening poster session for informal technical discussion with authors as well as a panel discussion where experts discuss and debate a current hot topic. The workshop includes invited talks from industry and research leaders (Key notes in the recent workshops were presented by Kioxia, West Digital, Micron, Applied material, Intel, GLOBALFOUNDRIES, Panasonic, ST Micro, IMEC and CEA-Leti,). Tutorial and highlight in the recent workshops included 3D NAND, DRAM, Embedded memories, Emerging memories and innovation (PCM, RRAM, MRAM, FeRAM…) for storage class memories, data centric architectures, tremendous growth of connected objects, and neuromorphic memory, quantum computing and in-memory computing. The technical program is organized to maximize networking opportunities and facilitate open information exchange among workshop contributors, committee members, and attendees. While organized this year as a virtual workshop, active participation and discussions will be encouraged by real-time Q&A as well as live Panel Discussion Sessions.

On behalf of the organizing committee, I cordially invite you to participate in the 2021 IMW to continue contributing to the advancement of innovation in the rapidly evolving memory industry. For additional information, including the call for papers, key dates, abstract submission instructions, registration information, and technical program details, please visit the IMW website: http://www.ewh.ieee.org/soc/eds/imw/. I look forward to e-meeting you in May 2021.

Zhiqiang Wei
2021 IMW Publicity Chair
Avalanche

Join us at the Latin American Electron Devices Conference, LAEDC 2021 (Virtual Edition)

Esteban Arias-Méndez | Technical Activities
Mario Aleman | General Chair LAEDC 2021

The third edition of the Latin American Electron Devices Conference, LAEDC 2021, will be held virtually April 19 to 21, 2021. This is a conference sponsored by the IEEE Electron Devices Society (EDS). The last editions of the conference were celebrated in Colombia and Costa Rica.

Its main goal is to bring together specialists from all Electron Device related fields. The conference will be geared to students as well as young researchers. Proceedings will be published by IEEE and the accepted papers will be available on IEEE Xplore.

The best papers presented at the conference will be considered for publication in a special issue of the Journal of the Electron Devices Society.

Due to the current pandemic worldwide, all the activities have been planned to be executed in a virtual mode without compromising the quality of the conference and allowing a great interaction of the assistants and sponsors.

For this new format, the authors are requested to send their video presentations of accepted papers before the event, but they are required to be online at the scheduled presentation time to check or clarify and answer questions.

Distinguish Keynote Speakers

Professor David Atienza (EPFL), Professor and Director of Embedded Systems Laboratory, École Polytechnique Fédérale de Lausanne, Switzerland. From IEEE Region 8. Professor Atienza will speak about *Energy-Scalable Many-Core Servers: Follow Your Brain!*.

Professor Martin A. Green, Director of the Australian Centre for Advanced Photovoltaics, School of Photovoltaic and Renewable Energy Engineering, University of New South Wales Sydney, Australia; will make us think about the future of Solar energy with its talk: *Can Solar PV save the World?*

Ravi Todi, Ph.D., Foundry Technology Development at Western Digital, USA; *Semiconductor Industry: A story of unprecedented growth and we are just getting started!*

General Program includes

18 April 2021	***MOS-AK workshop***
19–21 April 2021	*Keynote and invited speakers, scientific paper presentations, humanitarian technology plenary session, student poster presentations, YP & WIE session.*

Many of us will miss the face-to-face format of the conference and being able to interact directly. However, virtual has the advantage of offering us reduced prices to participate and LAEDC 2021 will not be the exception. The reduced rates of this edition will allow great participation of professionals and students. Additionally, student scholarships will be provided thanks to the collaboration of our sponsors.

Invited speakers will complement the research papers to be presented. A poster session will provide the first contact to industry and academy to many students and young professionals.

Looking forward to seeing you in LAEDC 2021, we invite you to check our official website https://attend.ieee.org/laedc-2021/ and social media channels for more information https://www.facebook.com/IEEE LAEDC. Let us know any question at our contact email of the conference LAEDC@ieee.org

LAEDC 2021 Organizing Committee

- Mario Aleman | General Chair | alemani@ieee.org
- Esteban Arias-Méndez | Technical Activities | esteban.arias@tec.ac.cr
- Pablo Moliterno | Web master
- Arturo Escobosa | Technical Activities
- Fernando Guarín | Treasurer
- Jacobus Swart | Organizing Committee
- Lluis F. Marsal | Organizing Committee
- Benjamin Iñiguez Nicolau | Organizing Committee
- Luis Procel | Organizing Committee

Board of Governors Meeting—December 2020

MK Radhakrishnan
EDS Secretary

EDS Board of Governors meeting in December was organized virtually due to the COVID19 pandemic worldwide. The virtual meeting using Webex, comprising 3 hours each from 9:00—12:00 US Eastern time on December 12 and 13, 2020. The meeting was planned to accommodate presentation schedules and to suit the convenience of the Society's global representation comprising almost 18 time zones. Almost all elected members of the BoG and EDS voting Forum members attended the virtual meeting on both days.

EDS President, Meyya Meyyappan welcomed all the attendees and informed them that the meeting would have presentations by all the VPs and other officers as scheduled in the agenda. The Q&A was managed by Ravi Todi, President-Elect, with questions and comments sent to him directly by email or Webex chat. All the motions were presented with the voting to take place via email after the meeting. The presentations were made available through the EDS BoG Agenda link in advance, which allowed everyone to go through them in advance. Highlights of the presentations and deliberations are as follows.

On the first day, December 12, Ravi Todi summarized the details of the virtual ExCom meeting held on December 11, 2020. EDS Secretary's report and Newsletter Status were presented by MK Radhakrishnan and the highlights include the selection of a new Associate Editor-in-Chief for the EDS Newsletter, Manoj Saxena, to join the Newsletter team in January 2021.

Bin Zhao, EDS Treasurer, presented the financial status, reporting a surplus of $1214K in 2019, 50% of which can be utilized for new initiatives. The budget for 2020 has been revised due to the pandemic situation. Both revenue and expenses have been revised with a substantial reduction in conferences related activities.

Kazunari Ishimaru, VP of Meetings informed that almost all the conferences were organized virtually this year. Out of the 17 financially sponsored conferences, 3 were cancelled and 4 technically co-sponsored conferences were cancelled. Most of the conferences may be organized in hybrid format in 2021.

Navakanta Bhat, VP of Education informed the successful organization of 18 webinars in the past 9 months. The approved summer school proposal will be functional next year. For 2021, certification and short courses programs are planned to build and enhance strong industry connection. EDS Podcast featuring interviews with illustrious members of our community will start in 2021 and this will be organized by Muhammad Mustafa Hussain.

Joachim Burghartz, VP Publications & Products informed that all EDS journals (TED, EDL and JEDS) are growing in the number of papers submitted and Impact Factor. The acceptance rate for all three journals remains more or less the same as in the previous year. The processing time is improving for all journals.

Murty Polavarapu, VP Regions and Chapters, reported that EDS has 214 chapters at present with 5 new chapters in Region 9 and 2 student chapters in Region 10. Twelve MQs were

successfully organized in the midst of the pandemic. As per the L31 reports, EDS Chapters had 444 chapter meetings this year. The first ever EDS Global Chapters Summit was organized virtually, which was very successful with an excellent participation from chapters across the globe. Chapter Chairs were able to share best practices and unique issues with the participants. Based on the success of the first event, the summit will be held regularly in the future.

Patrick Fay, VP for Membership informed that the EDS membership growth trends are not very attractive and a decline in membership is observed in almost all Regions except Region 9. Undergraduate student member strength is mostly concentrated in Region 9 and 10, whereas both graduate and undergraduate student memberships are very low in the US. He emphasized the need to have concerted effort to improve the situation.

After brief discussions on the viability of extending virtual DL talks, etc. the meeting was adjourned by Meyya Meyyappan.

The second day's meeting on 13 December 2020 started with the presentation by John Dallessase, VP for Technical Committees. There are 14 TCs and even with the constraints of the pandemic situation, the TCs worked very efficiently with all TCs participating

in various developmental activities as well as in MQs and DLs. Three TC Chairs—Benjamin Iniguez, Juzer Vazi and Claudio Paoloni will be retiring this year and John thanked them for their services.

Paul Berger, VP Strategic Directions, presented a plan for EDS strategic directives to oversee future directions, coordinating with IEEE Future Direction Committee and similar initiatives in sister societies. Certain areas have been identified, for example, Brain initiative, Quantum information processing, In-memory computing, and committees are being organized for initiating action plans.

Suman Datta, 2020 IEDM General Chair presented the latest status of the first ever virtual IEDM this year. The Tutorials and Short courses had excellent participation setting new attendance records. The conference will be virtually available with an interactive platform.

Giovanni Ghione, Editor-in-Chief of TED presented the status of the journal, showing progress in paper submission and acceptance. Jesus del Alamo, Editor-in-Chief of EDL presented EDL status, which shows the cycle time for paper acceptance of EDL as one of the best in IEEE publications. Enrico Sangiorgi, Editor-in-Chief of JEDS, informed that there were 5 successful special issues for JEDS this year and the number of submissions has increased from last year. The impact factor of all three journals has been improving every year.

Camilo Velez, YP Committee Chair, presented Young Professionals committee activities, which have been progressing. EDS visibility in Social Media platforms are very good. Among various platforms, LinkedIn seems to be more useful to increase EDS visibility.

Fernando Guarin presented the Humanitarian Activities summary. In 2020, EDS has spent $126K on 10 projects and $393K on 16 projects from the previous years, 3% of reserve and 50% of operating budget funds. Fernando announced the EDS awards for this year. Robert Dutton was chosen as the EDS Celebrated Member and Arokia Nathan received the J. J. Ebers Award. All other awards were also announced. The results of the BoG election held via online / email earlier were announced. Samar Saha presented the Fellow evaluation details. There are 16 EDS members elevated to IEEE Fellows among the 2021 class of fellows. Patrick McCarren gave a report summarizing EDS office activities.

After discussion, President Meyya Meyyappan thanked all participants from around the globe for their participation and support throughout the year, as well as EDS Staff for their dedicated effort in the midst of the pandemic. He adjourned the virtual meeting at 12:20 pm US Eastern Time.

MK Radhakrishnan
IEEE EDS Secretary

Message from EDS President

Dear EDS members:

Meyya Meyyappan
EDS President

Hope you are all keeping well and safe amid this COVID-19 crisis. I jokingly said at the last mid-year Board of Governors meeting (virtual meeting, of course) that I am poised to continue my virtual Presidency through into 2021. We are all looking forward to the day when we can resume business as before.

In the meantime, we have all adjusted to a new normal, mostly conducting business—including teaching classes—through Webex, Zoom, MS Teams, Skype and others. It appears that students and postdocs are beginning to get limited access to labs in some places. Hope this practice continues and expands in all regions, as research productivity would suffer otherwise tremendously.

In EDS also, we have adjusted to a new normal. The staff has been functioning fine, working from home and conducting all usual business. All our VPs have hit the ground running, taking care of their EDS responsibilities efficiently. First and foremost, all of our regular conferences have shifted to the virtual mode. Only a few have been canceled in 2020. The first-ever virtual conference for us, actually for the entire IEEE, was the EDTM (4th IEEE Electron Devices Technology and Manufacturing Conference, scheduled to be held in Penang, Malaysia), which turned out to be a tremendous success. Since then, we have had several successful virtual conferences. We have had very good support from IEEE Meetings, Conferences & Events (MCE) in terms of logistics including the conference platform tools. Our feeling is, if this practice of virtual events continues for another year or two, IEEE MCE is going to be overwhelmed with the demands from all the Societies and Councils to run virtual events. Therefore, we have

made a prudent decision to invest in creating our own tools and platforms for running the EDS conferences.

As a part of the new normal, we have asked all our chapters to run the DL program virtual. Some chapters have responded. I want to single out the Delhi Chapter and Manoj Saxena for the amazing work they have been doing: 13 DLs in 30 days in the beginning and many more since, with excellent attendance in each case and with attendees far beyond the Delhi borders. I hope all other Chapters follow this lead. Please contact Laura Riello at EDS Office if you need help or further information on running the DL program virtual. We have also been offering webinars on a nearly biweekly basis with an excellent set of speakers on a wide range of topics of interest to the EDS audience. The webinar schedules are announced on the EDS website and also communicated to our broad membership by email. These webinar presentations are archived on the EDS website for on-demand viewing available only to EDS members. Please contact our VP for Educational Activities, Prof. Navakanta Bhat, if you have suggestions for speakers or any input on the webinar series and other educational activities.

Meyya Meyyappan
EDS President

Message from the Chair of the EDS Optoelectronic Devices Committee

Dear EDS Members and Readers,

Can Bayram
Chair, EDS Optoelectronic Devices Committee

It is my pleasure to write this message as the Chair of the EDS Optoelectronic Devices Committee—one of the fourteen technical committees in our society. As a volunteer-driven committee, we serve the society primarily through organizing webinars, creating special invited issues in the EDS journals, and contributing to the conferences through organizing special sessions.

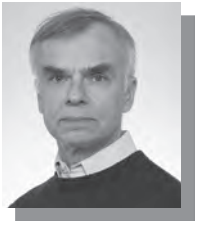
We are in the midst of a cultural change. The ripples of the pandemic will continue to reshape our personal, professional, and academic lives. With reduced travel to conferences, limited access to research facilities, and physically distanced conversations, our committee is encouraging you to benefit from the webinars at https://eds.ieee.org/education/webinars. EDS's webinar series deliver live and archived lectures with luminaries from the field of electron device engineering. With the recent coverage of topics such as photovoltaics, opto-electro-mechanics, detectors, and emitters, you will be certain to foster professional growth from the convenience of your home or office. You can also enjoy the path to commercialization topic webinars. Lastly, our committee solicited a photonic disinfection webinar to enhance the public visibility of the pandemic relief efforts the EDS members and electron devices technologies are behind.

We are strong. The pandemic relief efforts are driven by governments, companies, universities, societies, and non-profit organizations as well as citizen scientists, citizen engineers, and citizen entrepreneurs. Technological solutions to increase virtual presence and to limit pandemic impact on our personal and professional lives are being introduced constantly. As we navigate through the pandemic, it is vital to stay connected as the EDS society and strengthen our resolve to come up with solutions given the strength of our numbers and expertise.

In continuing efforts, our committee is discussing a focused optoelectronic session at the IEDM 2021. We would like your candid opinion of the emerging topics by email to cbayram@illinois.edu.

Can Bayram
Chair of the EDS Optoelectronic Devices Committee

Message from EDS Newsletter Editor-in-Chief



Daniel Tomaszewski
EDS Newsletter
Editor-in-Chief

Dear Readers, Members of the IEEE EDS Community, welcome to the IEEE EDS Newsletter issue January 2021.

This Newsletter issue brings you messages from Prof. Meyya Meyyappan, the President of EDS, and from Can Bayram, Chair of the EDS Optoelectronic Devices Committee. Furthermore, you can read a summary of the EDS BoG virtual meeting, held on December 12–13, 2020.

The Technical Briefs Section is very rich in this issue. It brings highlights of three technical conferences of great importance for the electron devices professionals and enthusiasts: the 2020 IEEE International Electron Devices Meeting, the 47th IEEE Photovoltaic Specialists Conference, and the 2020 IEEE International Physics Reliability Symposium. I would like to add that in the Regional News you can also read a report on the joint EuroSOI—ULIS 2020 Conference. Finally, among the Technical Briefs you can find the next interesting article concerning a set of reports of the International Focus Teams within the IRDS initiative. Our cycle was initiated in the July 2020 issue. We are looking forward to reading the next installment of this series.

The Upcoming Technical Meetings section announces four important conferences, namely 5th IEEE Electron Devices Technology and Manufacturing (EDTM) Conference 2021, IEEE Photovoltaics Specialists Conference 2021, 13th International Memory Workshop (IMW), and Latin American Electron Devices Conference (LAEDC) 2021.

The Regional News section brings as always articles reporting daily work of the Society Chapters. Many events were held virtually. However, in spite of the pandemic, there were also in-person meetings organized with precautionary measures. In the Chapter News you can find an interesting report on DIPED-2000 with a memory talk devoted to Prof. Voitovich, who passed away this year, and an encouraging article promoting the EDS Student Branch Chapter Instituto Tecnológico de Costa Rica, recipient of the 2020 IEEE EDS Student Branch Chapter of the Year Award. The latter note together with a story in the Young Professionals about a way of R&D in microelectronics in India may be inspiring and instructive for the ED communities on a global scale.

I am happy to announce that a new member joined the Newsletter Editorial Team, which is complete now. **Dr. Stewart Smith** has been appointed as the Regional Editor for Region 8, United Kingdom, Middle East & Africa. **Dr. Smith** is with School of Engineering of the University of Edinburgh, Scotland, U.K. Stewart, it is my great pleasure to welcome you, and wish fruitful work for the EDS Newsletter.

Stewart Smith

At this point I would like to express our gratitude to the outgoing Regional Editor: Jonathan Terry, for his dedication for the Newsletter and excellent job beyond the end of his regular 2nd term. Jonathan, all the best to you !

Finally, I would like to express my thanks to all the Authors of articles in this issue, to the Regional Editors and all the members of the Editorial Team.

Dear Readers, if you have any suggestions, comments regarding the Newsletter contents, please do not hesitate to contact me. I will be very glad to receive your feedback. Please, accept the warmest wishes from our Team for the Year 2021.

Sincerely,
Daniel Tomaszewski

Congratulations to Dr. Robert W. Dutton 2020 IEEE EDS Celebrated Member

Dr. Robert W. Dutton

To honor and recognize esteemed IEEE Electron Devices Society alumni, EDS created the Celebrated Member Program. Those of us in EDS can take pride in the accomplishments of these Celebrated Members and draw from the inspiration to advance our field and to achieve more, because it is not only their work but ours as well, that can help transform the world around us.

Recently, Dr. Dutton was presented with the EDS Celebrated Member crystal during the 2020 IEEE Electron Devices Meeting (IEDM) virtual event.

For a complete bio for Dr. Dutton, please visit the EDS Celebrated Member gallery, at https://eds.ieee.org/members/celebrated-members.

EDS Members Named Recipients of 2021 IEEE Technical Field Awards


Fernando Guarin
EDS Awards Chair

Hideaki Aochi, Ryota Katsumata, and Masaru Kito's revolutionary BiCS concept has become the standard for realizing high-density and fast three-dimensional (3D) flash memory to meet the needs of the powerful personal devices of today and the future. To overcome the scalability and complexity issues of early 3D flash memory concepts, the team created the new three-dimensional flash memory by punch and plug method, which features a multi stacked memory array with fewer critical lithography steps and charge-trapping cells for high-density yet cost-effective scalable memory. Their new concept has been widely used in solid-state drive storage systems for smartphones, PCs, and high-performance computers. With the capability for greater than a terabyte density, the team's innovative 3D flash memory can also replace hard disk drives, with the benefits of no moving parts, smaller footprint, and lower power consumption.

IEEE Andrew S. Grove Award

For pioneering and sustained contributions to high-density, three-dimensional flash memory


Hideaki Aochi

An IEEE Senior Member, Hideaki Aochi is a senior expert with the Institute of Memory Technology Research and Development at KIOXIA Corporation, Kanagawa, Japan.

An IEEE Senior Member, Ryota Katsumata is a deputy general manager with the Advanced Memory Development Center at KIOXIA Corporation, Mie, Japan.

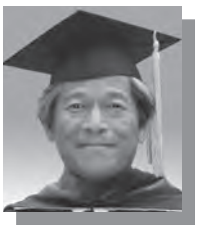

Ryota Katsumata


Masaru Kito

An IEEE Member, Masaru Kito is a group manager with the Advanced Memory Development Center at KIOXIA Corporation, Mie, Japan.

IEEE Electronics Packaging Technology Award

For contributions to new silver alloys, new bonding methods, flip-chip interconnect, and education for electronics packaging


Chin C. Lee

Chin C. Lee's innovative bonding methods and materials and new packaging technologies have been integral to developing high-temperature and high-power electronics. His work on silver wire bond reliability resulted in a wider process window, lower cost, and higher yield in packaging components. He also discovered that silver alloy is anti-tarnishing, which has had enormous economic and technical impact for applications including optics, astronomy telescopes, and LED packaging. His fluxless soldering technology has enabled numerous bonding designs and is critical to packaging electronics for applications where oxidation effects from solder materials can be problematic. Lee also developed solid-state flip-chip interconnects and formulated quantum bonding theory. He established a materials and manufacturing technology graduate program in 2007 at the University of California, Irvine, which was one of a few such programs at that time.

An IEEE Life Fellow, Lee is a professor (retired) with the University of California, Irvine, California, USA.

IEEE Cledo Brunetti Award

For leadership in and contributions to InGaAs- and GaN-based field-effect transistor technology


Jesús del Alamo

A pioneer in driving III-V semiconductor research since its early days, Jesús del Alamo has played a foundational role in establishing the viability of indium gallium arsenide (InGaAs) and gallium nitride (GaN) transistors for high-frequency communication, electrical power management and digital logic applications. With InGaAs-based materials, his research group has pursued nanoscale high-electron mobility transistors (HEMTs) and metal-oxide-field-effect transistors (MOSFETs) for Terahertz applications and achieved record performance in many dimensions. In the GaN heterostructure system, his research has focused on achieving fundamental understanding of electrical, environmental, and thermal reliability of HEMTs for radio-frequency and power electronics applications. Transistors based on del Alamo's innovations have found use in applications ranging from smartphones to fiber-optic systems to wireless networks.

An IEEE Fellow, Jesús del Alamo is the Donner Professor and professor of electrical engineering with the Massachusetts Institute of Technology, Cambridge, Massachusetts, USA.

Fernando Guarin
EDS Awards Chair
GlobalFoundries

IN MEMORY OF PROF. JAMES D. MEINDL

By Krishna Saraswat

James Donald Meindl, a towering figure from the earliest days of integrated circuitry, died on June 7, 2020 at his home in Greensboro, Georgia. He was 87.

Meindl was a great visionary, truly one of the icons of the silicon era, who saw early on the potential of integrated circuitry and who swayed the semiconductor industry in new directions for decades.

Meindl was born on April 20, 1933 in Pittsburgh, Pennsylvania. He received his BS, MS and PhD degrees in electrical engineering from Carnegie-Mellon University in 1955, 1956, and 1958 respectively.

From 1965 to 1967, he was founding director of the Integrated Electronics Division of the U.S. Army Electronics Laboratories in Fort Monmouth, New Jersey.

In 1967, he joined Stanford University as John M. Fluke Professor of Electrical Engineering and founded the Integrated Circuits Laboratory. In 1987 he co-founded the Center for Integrated Systems (CIS), before becoming vice provost of research. While at CIS, Meindl was noted as an early champion of another Silicon Valley innovation: the university-industry partnership. He helped forge lasting relationships between Stanford and notable semiconductor companies, like Intel, Advanced Micro Devices, IBM, and HP. At Stanford, Meindl developed low-power ICs and sensors for a portable reading aid for the blind, miniature wireless radio-telemetry systems for biomedical research, and noninvasive ultrasonic imaging and blood-flow measurement tools that paved the way for medical systems that are widely used today. Later on, anticipating that power consumption, not speed or size, would become the major limiting factor on future chip performance, Meindl became a proponent of low-power electronics, which prized energy efficiency above all. In this regard, he was decades ahead of the industry.

Prof. James D. Meindl (1933–2020)

In 1986, Meindl became provost of Rensselaer Polytechnic Institute. In 1993, he moved to Georgia Tech, where he was director of the Joseph M. Pettit Microelectronics Research Center and the Marcus Nanotechnology Research Center and Pettit Chair Professor of Microelectronics. He was founding director of the multi-institutional, multidisciplinary Interconnect Focus Center and led a team of more than 60 researchers from Georgia Tech, Stanford, MIT, RPI, and others. He retired from Georgia Tech in 2013.

As much as Meindl was known as a visionary engineer, however, he was regarded more so as a master of human potential—particularly, in his students. He mentored 90 Ph.D. candidates during his almost-five-decade academic career at Stanford, RPI, and Georgia Tech. That intellectual diaspora has gone on to have profound influence everywhere from the semiconductor industry to university research and administration.

Meindl authored 4 books, and more than 600 technical papers, and he was granted 23 patents. He served as the founding editor of the *IEEE Journal of Solid State Circuits*. He was likewise frequently recognized with industry awards and accolades. In addition to the 2006 IEEE Medal of Honor, he was elected to membership in the National Academy of Engineering and the American Academy of Arts and Sciences. He was a Fellow of the American Association for the Advancement of Science and an IEEE Life Fellow.

Throughout his career, he was a sought-after advisor and board member for many companies, including IBM, Intel, Hewlett Packard. His leadership and advisory roles in government and industry organizations included work with the Semiconductor Industry Association and the National Science Foundation's National Nanotechnology Infrastructure Network.

James D. Meindl is survived by his wife Frederica Meindl of Greensboro, Georgia; son Peter Meindl; daughter Candace Fleming; brother Edward Meindl and several grandchildren.

Announcement of the 2020 EDS Undergraduate Student Scholarship Winners

The Electron Devices Society Undergraduate Student Scholarship Program was designed to promote, recognize, and support undergraduate level study and hands-on experience within the Electron Devices Society's field of interest.

EDS proudly announces the winners of the 2020 EDS Undergraduate Student Scholarships.

Yanghao Wang is a senior student majoring in microelectronics at the school of Electronics Engineering and Computer Science, Peking University, China and is a student member of the IEEE Electron Devices Society. He entered Peking University in 2017 after graduating from Shaoxing No.1 high school and passed a series of microelectronic professional courses with excellent grades in college. He has been participating in academic research since the summer of 2018 and his advisors are Yuchao Yang and Ru Huang. His research interests focus on novel memristive devices for neuromorphic computing: 1) Exploiting computing superiorities of electron synapses and neurons with spatio-temporal dynamics. 2) Constructing biologically plausible memory models and circuit architectures with low power consumption. 3) Designing neuromorphic chips with new devices and new computing principles which can support advanced but unsuitable for current hardware brain-inspired algorithms. Now he is a member of the national key research and development project dealing with nonvolatile memristive devices for logic. He also had a summer research internship in Westlake University, China, where he explored the potential of high precision 3D printing technology to manufacture electronic synapses and neurons with more complex morphology and structure. Yanghao Wang took part in the 2018 national undergraduate physics competition and won the first prize. He won the Peking University Academic Excellence Award in 2019. Besides, he won the prestigious IEEE Electron Devices Society undergraduate scholarship as a recognition of his academic experience in 2020. Yanghao Wang has published four papers on Nature Communications, Science Advances, Advanced Intelligent Systems and Chinese Science Bulletin until now. His contribution is to design and simulate brain-inspired algorithms to resolve some specific and meaningful problems utilizing actual electronic devices' intrinsic dynamics or non-ideality. His first-authored work in Advanced Intelligent Systems was selected in Editor's Choice and further promoted on Advanced Science News as a highlight, where he first proposed an implementation method of biologically plausible working memory based on neuromorphic devices. In a co-authored paper published on Nature Communications and Science Advances, he respectively utilized the characteristics of nonlinear neuron devices to construct large-scale spike synchronization detection applications and nonlinear synaptic devices to construct transient chaotic neural networks for combinatorial optimization problems. After completing his B.A. in 2021, Yanghao Wang will continue to pursue his Ph.D. degree under the guidance of Ru Huang in Peking University, China.

Azwar Abdulsalam is a final year student currently pursuing his Bachelors in Electronics and Electrical Communication from the Indian Institute of Technology Kharagpur. Prior to joining IIT Kharagpur he completed his schooling from Our Own English High School, Sharjah in the United Arab Emirates. Upon completing his high school studies he gave the JEE advanced examination in which he scored in the top 99.5 percentile among approximately 200,000 candidates which helped him secure a seat in the Electronics and Electrical Communication Engineering department of IIT Kharagpur. Throughout Azwar's high school years he loved to study physics, especially topics of electricity and magnetism. This was the primary reason why he chose to pursue his undergraduate studies in Electronics. Azwar's present research interests include simulation and modeling of GaN HEMTs for power application. He began his research work under prof. Gourab Dutta of IIT Kharagpur in his sophomore year working on the analytical modeling of threshold voltage of p-GaN HEMTs. pGaN HEMTs are currently emerging as a promising E-mode GaN HEMT with technological giants like Samsung and Panasonics having already begun production of commercial p-GaN HEMTs. His work on the analytical model of threshold voltage was accepted for publication in the journal semiconductor science and technology. Azwar also worked on a TCAD based simulation study of the threshold voltage of an E-mode AlGaN/AlGaN HEMT which he then presented as a poster at the XXth International Workshop on the physics of Semiconductor Devices held at Kolkota, India. After concluding his work on the threshold voltage of E-mode GaN HEMTs he began his work on the analytical modeling of 2-DEG charge density and gate capacitance of p-GaN HEMTs. Recent works have indicated the advantages of using p-GaN HEMT as an on-chip capacitor thus making this work particularly

important. This work was then accepted for publication in the IEEE Transactions on Electron Devices. In the summer of 2020 Azwar was involved in a remote project at the POWERlabs in EPFL headed by prof. Elison Matioli. Here he worked for about six months on a TCAD simulation project on Tri-gate HEMTs. Currently he is working on his graduate application to pursue his passion of research on semiconductor devices and hopes to make a significant contribution to the field.

Samar K Saha
EDS Undergraduate Student Scholarship Committee Chair

Announcement of the 2020 EDS Masters Student Fellowship Winners

The Electron Devices Society Masters Student Fellowship Program was designed to promote, recognize, and support Masters level study and research within the Electron Devices Society's field of interest.

EDS proudly announces the winners of the 2020 EDS Masters Student Fellowship

Hong-Yi Tu was born in Tainan, Taiwan, in 1997. He received his B.S. degree in materials and optoelectronic science from National Sun Yat-Sen University, Taiwan, in 2020. He is currently in the five-year bachelor's and Master's degree program pursuing the M.S. degree at National Sun Yat-Sen University, supervised by Prof. Ting-Chang Chang and Prof. Tsung-Ming Tsai. His research interests include low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs), amorphous metal oxide TFTs, flexible TFT technology, and high electron mobility transistors (HEMTs). His current research focuses on the reliability issues and optimization of reliability in LTPS TFT and metal oxide TFT. Hong-Yi Tu has published two scientific papers as a primary author on IEEE Electron Device Letters and Journal of Physics D: Applied Physics in his junior year and senior year, respectively. He has proposed degradation mechanisms for LTPS TFTs under negative bias temperature instability of the devices with different grain size and proposed degradation mechanisms of hump formation with hysteresis effect after the devices operated under high positive bias. To date, he has published 2 articles as primary author and 10 articles as co-author. Apart from academic publication, he has also participated in several industry-academic cooperative research projects mainly solving device performance and reliability issues. In addition, he wins the "Student Engineering Paper Contest" held by Chinese Institute of Engineers (CIE) and wins the 2018, 2019 and 2020 "College of Engineering Project" in his college for his project poster presentation. Furthermore, he is one of the recipients of the "Undergraduate Student Research Scholarship" from both the Ministry of Science and Technology (MOST), Taiwan and the National Sun Yat-Sen University. He also gets the "Academic Excellence Award" in his department.

Prasanna Venkatesan

Prasanna Venkatesan received his B.Tech degree in Electrical Engineering from Indian Institute of Technology (IIT) Palakkad in 2019 with the Department Gold Medal. During his B.Tech, Prasanna was selected to the prestigious S. N. Bose Scholars Program in 2018. He is currently a second year PhD student in Dr. Asif IslamKhan's lab at Georgia Institute of Technology. Prasanna's interests lie at the intersection of electrical engineering, material science and quantum physics. The sheer curiosity about how things work and a deep desire to contribute to the advancement of technology drive Prasanna to learn every day. The goal of Prasanna's research is to push the limits of computing technology by exploiting the intricacies in fundamental science and understand the interesting physics of functional materials like ferroelectrics and antiferroelectrics. He plans on joining academia after completing his PhD.

Subramanian S. Iyer
EDS Student Fellowship Committee Chair

Announcement of the 2020 EDS PhD Student Fellowship Winners

The Electron Devices Society PhD Student Fellowship Program was designed to promote, recognize, and support PhD level study and research within the Electron Devices Society's field of interest.

EDS proudly announces three EDS PhD Student Fellowship winners for 2020: **Wangyong Chen**—Peking University (China); **Chris Allemang**—University of Michigan (USA); **Nicolas Wainstein**—Technion—Israel Institute of Technology (Taiwan). Brief biographies of the recipients appear below. Detailed articles about each PhD Student Fellowship winners and their work will appear in forthcoming issues of the EDS Newsletter.

Christopher R. Allemang is a Ph.D. candidate studying electrical and computer engineering in Professor Becky Peterson's group at the University of Michigan. Prior to coming to the University of Michigan, Chris received a Bachelor of Science in electrical engineering from the University of South Florida where he was an undergraduate researcher and Chair of the IEEE Student Branch. His research interests include microfabrication for scalable manufacturing of thin-film electronics for back end of line 3D monolithic integration on silicon CMOS for "More than Moore" technologies and customizable manufacturing of thin-film electronics. His work spans deposition and characterization of oxide semiconductor materials and devices, including atomic-layer deposition of multi-component semiconductor materials. The work Chris has performed with atomic layer deposition of zinc-tin-oxide semiconductors and aluminium oxide passivation layers have contributed to record high-performance zinc-tin-oxide thin-film transistors with process temperatures compatible with flexible electronics and back end of line 3D monolithic integration. Outside of the lab, Chris has been an active member of the University of Michigan College of Engineering's community by serving on the Lurie Nanofabrication Lab's User Committee, the college's Diversity, Equity, and Inclusion Student Advisory Board, and the college's Curriculum Committee. Chris's goals in participating in these activities were to promote student camaraderie and to create a more inclusive place for all students to live, learn, and grow. To foster STEM in underrepresented groups, he has assisted with Electrify-Sense It Summer Camps where high school students work on small team projects focused on programming, microcontrollers, and wireless sensing. During the COVID-19 pandemic, Chris has enjoyed going outside for walks with his dog and playing virtual board games with his friends. When not in a pandemic, he enjoys playing flag football in a Detroit LGBT league. The league's travel team Chris plays on won first place in their division at Chicago's 2019 Pride Bowl. He also serves as a moderator for an online automotive forum and is active in politics by volunteering for various campaigns.

Nicolás Wainstein is a Ph.D. student at the Andrew and Erna Viterbi Faculty of Electrical Engineering, Technion—Israel Institute of Technology, Haifa, Israel since 2015. He received the degree in electrical engineering (5-year program) from the Universidad de la República, Montevideo, Uruguay, in 2014. His research focuses on reconfigurable radiofrequency circuits using high-performance switches based on emerging memory technologies, such as phage-change memory (PCM), resistive RAM (ReRAM) and conductive-bridge RAM (CBRAM). Currently, he is working on the development, fabrication, and modeling of high-performance PCM RF switches as well as circuit design and fabrication of reconfigurable RF front-end circuits based on these devices. A summary of his findings on this topic was recently published in the Proceedings of the IEEE. He succeeded to publish more than seven articles in high-impact factor journals like IEEE TCAS I, IEEE T-NANO, Nature Electronics, and IEEE T-ED. He also has more than six conference contributions including IEEE DRC (late news), MRS, IEEE ISCAS, and IEEE ISVLSI. Mr. Wainstein was a recipient of the 2020 Yablonovitch Research Prize, the 2020 RBNI Prize for Excellence in Nanoscience and Nanotechnology, the 2020 RBNI Scholarship, the 2019 Jury Award for Outstanding Students, and the Excellence Scholarship from the Andrew and Erna Viterbi Faculty of Electrical Engineering, Technion—Israel Institute of Technology, in 2018, 2019, and 2020. Teaching has also played an important role in his career; being involved in teaching activities since his B.Sc. in Uruguay. He was a TA in Physics and EE courses at the EE faculty, Universidad de la República. At the Technion, he is a TA in several courses, such as Introduction to VLSI and Advanced Architectures and Circuits using Memristors. He was also a TA of the Advanced Analog Integrated Circuit Design course, given by Prof. Willy Sansen (KU Leuven). In his free time, he enjoys running, playing football, going to the beach, and traveling.

Wangyong Chen (IEEE Student Member, EDS Member, and Young Professionals) received the B.S. degree in Electronics Science and Technology from Hunan University, Changsha, China, in 2016. He is currently pursuing the Ph.D. degree in Microelectronics and Solid State Electronics with the Institute of Microelectronics, Peking University, Beijing, China. His current research interests include multi-scale reliability modeling and simulation from devices to circuits as well as experimental characterization, including reliability-aware device-circuit co-design, self-heating characterization.

He developed the trap dynamics based 3D Kinetic Monte Carlo simulator to capture the statistical charge distributions in the multilayer gate dielectric under arbitrary stress conditions in the presence of time-zero variations. The simulator provides a powerful tool for comprehensive reliability evaluation at the advanced technology node and traps impact identification over the entire bias space. Within the Ph.D. study, he did series of works on self-heating effect in advanced nanoscale devices ranging from experimental characterization to modeling and simulation, where an analytical model based on the multi-stage thermal network to effectively address the self- and mutual-heating in the scaled device was developed and a novel self-heating characterization method using the shared intrinsic series resistance was proposed. He also proposed an efficient variability- and reliability- aware device and circuit co-design methodology to predict the time-dependent delay degradation and potential critical paths in the digital circuits coupled with self-heating effect at arbitrary operating conditions.

He has published 28 technical papers and owned 3 patents during the doctoral study period, including conference and journal papers on the IEEE IEDM, EDL, T-ED and T-NANO. He received the IEEE IPFA Best Paper Award in 2018, and he was invited to deliver a report at the ESREF conference in 2018. He was selected as the Best Paper Award in the Microelectronics Forum of China in 2018. He won the title of outstanding graduate of Hunan Province and Hunan University in 2016. He was awarded the National Scholarship in China 5 times from 2013 to 2020. He won the Headmaster's Fellowship in 2019 which is the top honor prize for the graduate student in Peking University, and he was selected as Merit Student and Academic Innovation Award from Peking University for two consecutive years. He serves as the active reviewer for IEEE T-ED, EDL and J-EDS, etc.

Subramanian S. Iyer
EDS Student Fellowship
Committee Chair

2020 EDS Chapter of the Year Award Winners

Murty Polavarapu
EDS Vice-President
of Regions/Chapters

The EDS Chapter of the Year Award is presented annually to recognize chapters for the quality and quantity of the activities and programs implemented during the prior July–June period. EDS recently revised our Chapter of the Year Award to award one non-student chapter and one student chapter in any geographic location.

The 2020 EDS Chapter of the Year Award winners:

2020 Chapter of the Year Award: IEEE ED Uttar Pradesh Kanpur Chapter

2020 Student Branch Chapter of the Year Award: IEEE ED/RFID/BIO Costa Rica Institute of Technology Student Branch Chapter

Murty Polavarapu
EDS Vice-President of
Regions/Chapters

Call for Nominations – EDS Student Fellowships for 2021

The IEEE Electron Devices Society invites nominations for the 2021 PhD, Masters and Undergraduate Student Fellowships. These annual awards are given to promote, recognize, and support graduate, masters, and undergraduate level study and research within the EDS field of interest. For both Masters and PhD, it is expected that at least one fellowship will be awarded to a student in each of the following geographical regions: Americas, Europe/Middle East/Africa, and Asia/Pacific. For the Undergraduate, it is expected that at least one fellowship to each eligible student in each of the IEEE geographical Regions 8, 9, and 10 and two fellowships in Regions 1-7 not exceeding one from Region 7.

Please visit the EDS website links below to access information about these Fellowships.

EDS Masters Student Fellowship
Prize: US $2,000 and an award plaque
Submission Deadline: May 15, 2021

EDS PhD Student Fellowship
Prize: US $5,000 and travel funds to attend the IEDM for presentation of an award plaque
Submission Deadline: May 15, 2021

EDS Undergraduate Student Scholarship
Prize: US $1,000 and an award plaque
Submission Deadline: May 15, 2021

Please help to promote the EDS Student Fellowships by distributing this information to your colleagues and students. If you have any questions or need further information, please do not hesitate to contact Stacy Lehotzky by email at s.lehotzky@ieee.org. Thank you!

India's Rise in Nanoelectronics Research

Udayan Ganguly, Sandip Lashkare, and Swaroop Ganguly, IIT Bombay

Witnessing a Quiet Evolution

As semiconductor innovations power the digital age, India has aspired to contribute to nanoelectronics. Towards this, India pushed a strong nanoelectronics program starting in 2006. Our study shows that recently India has been significantly contributing to Electron Devices Society related publications. This evolution has been quiet, largely unnoticed in the humdrum of academic and research life. This paper presents the development of the Indian nanoelectronics R&D ecosystem from nothing to global competitiveness. The lessons from this shared experience will help India and other countries who aspire to set sail for similar R&D adventure, to develop a more grounded, and robust policy and implementation towards an ambitious future.

A Snapshot from the Past

In 2004, the industry was pushing transistor scaling to high performance, faster & denser integrated circuits manufactured at Intel, AMD, and other leading semiconductor companies. In academia, Cornell and Stanford nanofabrication facilities were driving nanoscience and technology—pushing cutting-edge nanoscale physics from carbon nanotube and quantum dot to the technology of deep-sub-micron CMOS. Indian students would naturally evolve into contributors in international academia, and the semiconductor industry with rewarding careers. Yet, many dreamed to pursue a career in nanoelectronics research in India. However, semiconductor research was not at a similar intensity there. Essentially, engineering institutes in India barely had microfabrication facilities.

At the time of graduation, some students would embark on a pilgrimage to Indian research-centric institutes to get the "lie of the land"—a core instinct for experimentalists. The news was that IISc and IIT Bombay had proposed two Nanofabrication Facilities—one at each location. The effort was being led by the Office of Principal Scientific Advisor through the Ministry of Electronics and IT (MeitY). It was a big relief. Yet, there were questions. Will academia be able to develop the Nanofabs? Will new faculty be able to develop a globally competitive R&D program around these new Nanofabs? Only time could tell…

Recent Significant Contributions

Fast-forward to 2020, when an IEEE EDS journal annual performance report analyzed its contributors. In a corner of the report, there was a strange little graph. It showed that India with 40 papers was ranked 8th in the contribution to Electron Device Letters (EDL) by countries, whereas the IIT System with 34 papers was ranked 9th among organizations (Fig. 1a,b). This was curious. In the whirlpool of research, funding, teaching, and fighting administrative fires, most academics would have no bandwidth left to contemplate the "overarching" state of Indian R&D—except in anecdotes. But, this nugget had to be investigated.

Among many questions, the dominant one was whether EDL was an anomaly. So, we looked up the *IEEE Transactions on Electron Devices* (*TED*) performance. It was a further surprise. The IIT system was ranked 1st in the contribution by organizations and India was ranked 3rd (Fig. 1c,d). These were compelling indicators. Both EDL and TED are considered the most exclusive venues to publish electron device-related research. India was doing well in both.

A Trajectory of Strong Growth

The next question was—how long has this been going on? A comparative study of the University of California (UC) System, Chinese Academy of Science (CAS), National Chiao Tung University (NCTU) Taiwan, and the Indian Institute of Technology (IIT) System revealed the trajectories (Fig. 2). Unlike UC, CAS, NCTU, which have been publishing regularly, the IIT System had negligible publications before 2011. Since 2011/2012, the IIT system has accelerated publication in TED as well as in EDL. The publication in TED has overtaken other university systems recently and was ranked 1st in 2019. Similarly, the publication in IEEE EDL has reached a level comparable to other systems. Starting from 2015/2016 a saturation of the IIT publication rate has been observed. Citations per paper were comparable to the journal average—slightly better than NCTU and CAS, which are similarly aged institutions, but worse than UC, which is an older player (Fig. 2).

While India had significant achievements even as early as 2005 in basic science ranking in SCOPUS etc. [1], the growth in nanoelectronics engineering research from negligible contributions before 2011 to high intensity by 2018 is a significant success of the program.

Resolving Growth

As the growth trajectory is apparent, the question was - what are the thrusters driving the change? We needed

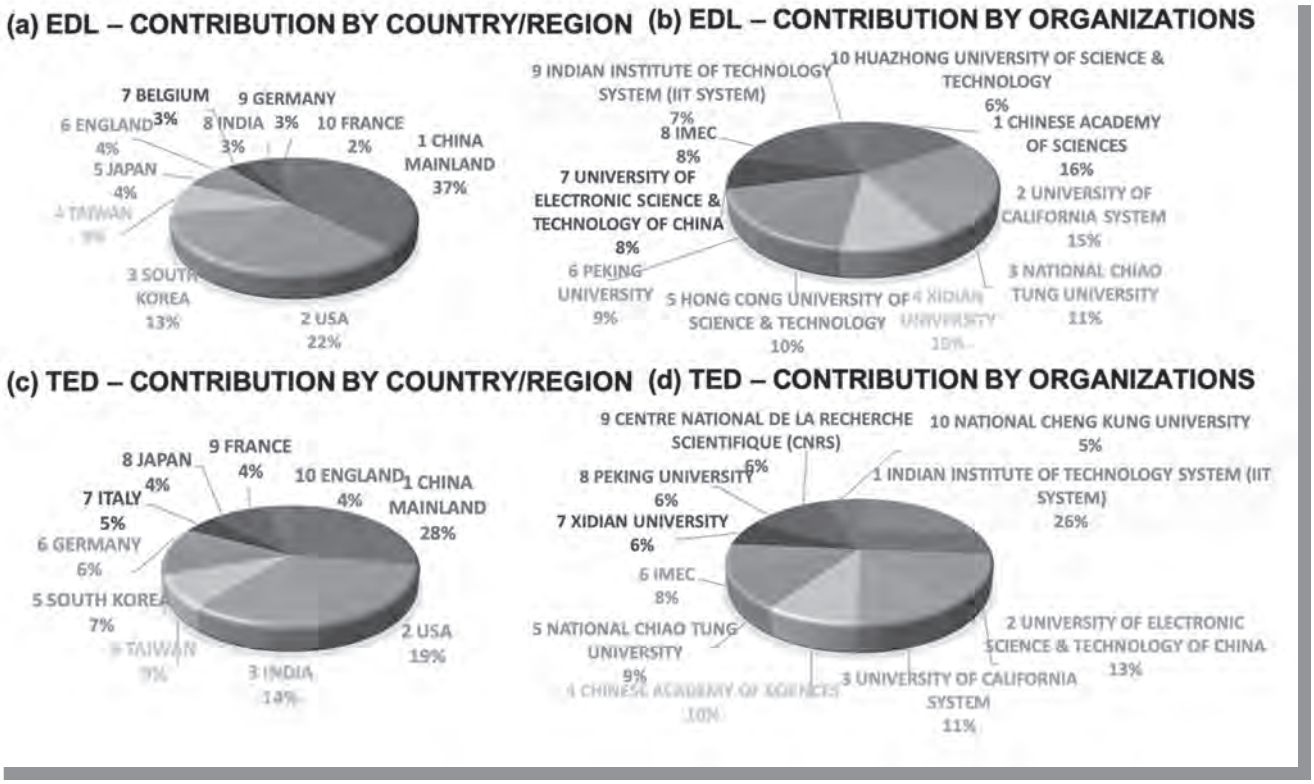


Fig. 1. India and the IIT system records among top 10 performances in EDL and TED in 2019 (pie charts limited to the top 10 contributors)

to resolve by institutions, approach (experiment vs modeling), and global collaborations. We chose publications and citations per article as metrics of success—with the sense that one could always follow up with a more detailed study. Lastly, what publications will give a cogent picture? We chose three of them in the domain of electron devices to study the progression from detailed, long-form studies (i.e. TED) to novel and newsworthy (i.e. EDL). To complete the series, we also looked at the International Electron Device Meeting (IEDM). IEDM is the flagship conference where industry & academia showcase the latest and greatest technological development of industrial impact. We considered papers published between the year 2000–2020. While this list is not exhaustive, we believe that it shows representative trends and questions which may motivate towards a more specific and exhaustive study.

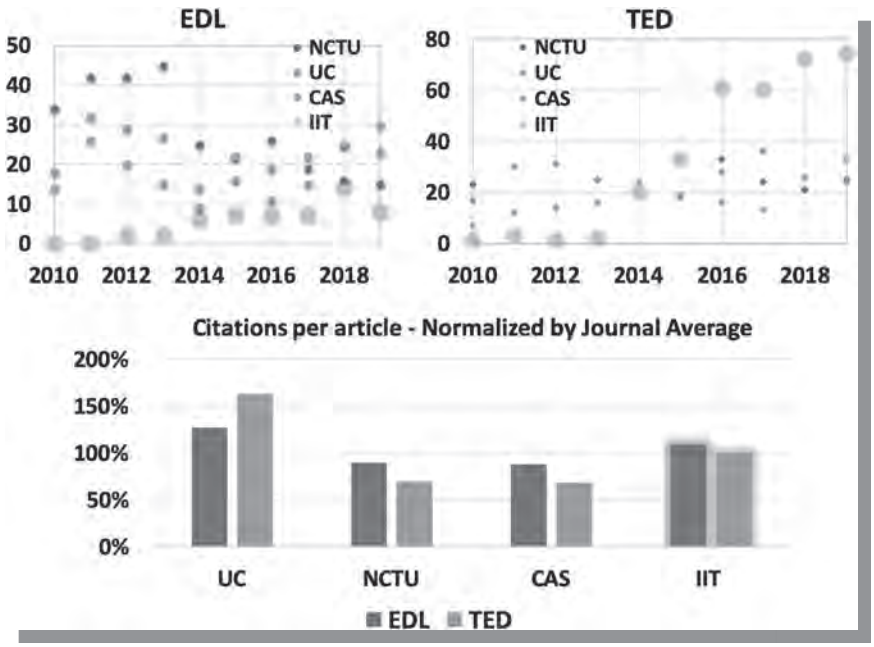


Fig. 2. A timeline of IIT publications in EDL and TED (Based on data from Web of Science database 2010–2020)

Institutions of Success

The IITs and IISc have the reputation of being top engineering education institutes [2]. IISc is a postgraduate oriented institute while IITs are undergraduate oriented, although recently evolving towards postgraduate research. The old IITs (Kharagpur, Bombay, Madras, Delhi, and Kanpur) established in the 1950s have been transformative for the global technology ecosystem. To replicate their success, various new IITs were created

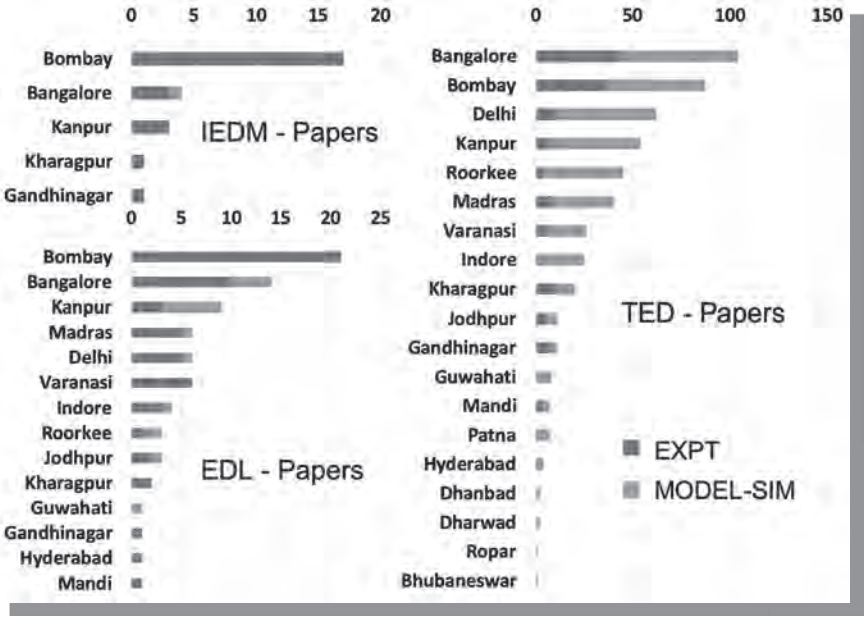


Fig. 3. Frequency of publications by IITs and IISc in 2000–2020. (The publication number in figure is slightly higher than the actual number as mentioned in the text above. This is due to some of the papers having multiple IITs collaboration. In such papers, every collaborated IIT has been given a separate count.)

and some older engineering schools like Roorkee and Banaras Hindu University (Varanasi), were brought into the IIT system. Publication activity of these institutes in the period 2000–2020 is shown in Fig. 3. IIT Bombay and IISc Bangalore are the top contributors. They have the state-of-the art experimental facilities. 13 IITs and IISc published 68 papers in EDL, 17 IITs and IISc published 473 papers in TED. A smaller number of publications in EDL by few IITs can be directly related to lacking state-of-the art processing facilities. Besides, 4 IITs and IISc published 26 papers at IEDM, which is the most selective conference.

Newer IITs like Indore, Guwahati, Jodhpur, and Gandhinagar, to name a few, have also started contributing. Furthermore, older institutions but newer entrants to the IIT system like Roorkee and Varanasi have been also productive. This overall performance is encouraging.

Intense Experiments & Modeling

We found that 131 papers published in TED (28%) were experimental and 342 papers (72%) were based on modeling and simulations. So, India contributes strongly to physics-based device modeling. Furthermore, 54 papers published in EDL (79%) and as much as 96% of the papers presented at IEDM were based on experimental demonstrations. The average citations per paper are about similar, approx. 10.5 for both IEDM and EDL articles and 8.43 for TED papers. It appears that an experimental demonstration improves newsworthiness and impact of the published paper.

International Collaborations

An exchange of knowledge with international partners plays a significant role in the research, and we dare to say is a necessary condition for successful works in micro- and nanoelectronics, reported at the top level conferences and journals, which are considered in this analysis. Among the affiliations of the international teams cooperating with researchers from the IITs and IISc in India the top 3 countries are the USA, Germany, and Singapore (Fig. 4). This graph also indicates opportunities to strengthen ties with countries like Belgium, Taiwan, Brazil, Japan, and South Korea. Such a network of

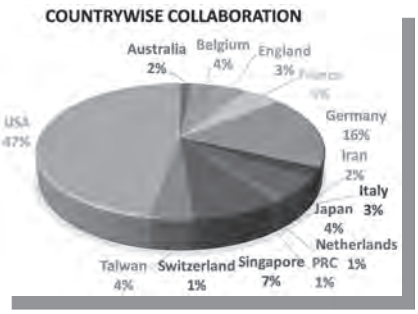


Fig. 4. The collaboration of Indian institutes with researchers from other countries.

collaboration is critical to amplifying research contribution further.

Inspiring the Path Forward

Research on electron devices in India has unfolded before our eyes over the past 15 years. This is related to the key policy and the implementation of the shared Centers of Excellence in Nanoelectronics (CENs) as rallying points for talented researchers who grow up across the country thanks to the distributed project funding. Such a successful policy and implementation should inspire a scale-up of the Indian ecosystem to contribute to the urgent national and global needs of an innovation-driven ecosystem. We believe that the aspect of the history of R&D in India presented in our article will help and inspire researchers in other countries to grow the international network of research in electron devices—that is central to the concept of a borderless Electron Devices Society.

Notes & Acknowledgements

This is a modified excerpt from a detailed study available on arXiv (arXiv:2011.11251). The authors acknowledge Prof. Jesus del Alamo, MIT, Sunita Verma, Sangeeta Semwal, and Nishit Gupta from MeitY, Milind Kulkarni from DST, and Prof. Juzer Vasi, IIT Bombay.

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IEEE Young Professionals Germany at Robert Bosch Semiconductor Headquarters

by Mike Schwarz

The IEEE Young Professionals Germany ExCom organized in cooperation with the Robert Bosch GmbH a virtual company visit on September 28, at the semiconductor headquarters of Bosch, Germany.

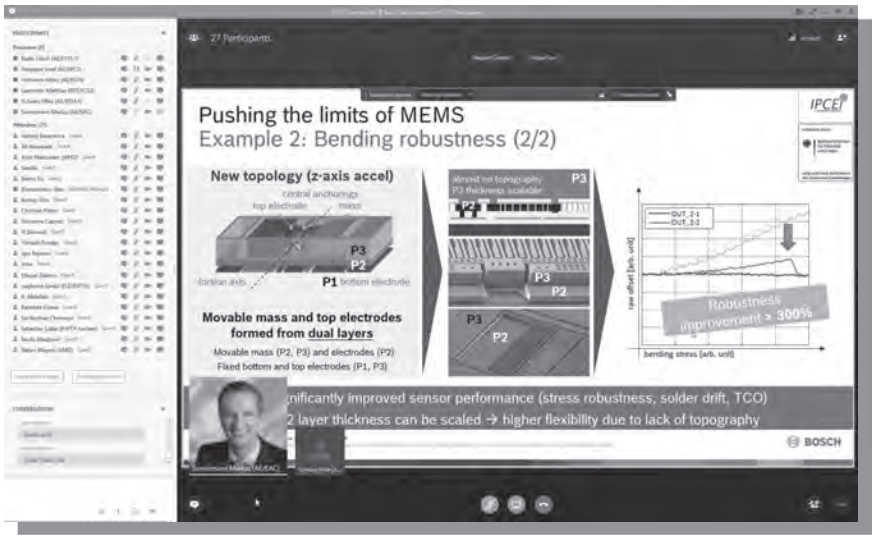
Unfortunately, the worldwide pandemic situation made an onsite visit not possible. Therefore, all the registered participants agreed to make this virtual visit and event happen. From the 30 exclusive slots, 23 students and young professionals attended the virtual event. On top 14 participants from Bosch semiconductor headquarter, i.e. top level management, chief experts and human resources completed a great event.

The one-day event started at 9:15 and went until 16:00. In the morning Mirko Hofmann, director of the MEMS design house had a welcome speech to the attendees and guided together with Mike Schwarz through the program of the day.

The first talk was delivered by Armin Scharping and was entitled "Site presentation and manufacturing area". The talk gave some insights of the various possibilities of manufacturing available in Reutlingen and in future also in Dresden´s 300 mm fab. An impressive video presenting the clean room facilities closed the talk.

Afterwards, Ali Aboosaidi from the IEEE YP Germany AG gave an overview of the activities of the YP in Germany. Organizing events and focusing on exchange/ networking with other YP groups.

The event continued with more insight by Frederik Schrey from the integrated circuit domain of Bosch who gave a talk "ASICs and Semiconductor Technologies for Bosch Systems". Here, Mr. Schrey concentrated on a portfolio overview and the future possibilities with the 300 mm fab in Dresden.



Vice President Dr. Markus Sonnemann presenting "MEMS—enabling technology for future mobility solutions pushing the limits of MEMS"

After the overview Sebastian Strache continued with "Bosch Power Semiconductors and Modules". Mr. Strache introduced the power semiconductors and SiC for volume production. He also highlighted that ongoing research is fulfilled by the Corporate Research Department. A few questions came up as examples. Here, it was emphasized that OEMs use Power Modules, i.e. inverters from Bosch for electric cars.

The day continued with a talk of Markus Sonnemann, Vice President and Head of the predevelopment of MEMS, followed with the title "MEMS—enabling technology for future mobility solutions pushing the limits of MEMS". Here, Mr. Sonnemann gave a lot of examples of sensor improvements by technology and the success of predevelopment.

The morning session ended with presentations and experiences of the human resources director Florian Schueller and Ulrich Baehr, a former Bosch PhD student. Both shared insights of their Bosch career and offered also entry opportunities. Here, a lot of Q&A made an interesting exchange between employees and students/young professionals.

The afternoon session started with a talk entitled "MEMS Technology", given by chief expert Heiko Stahl. Mr. Stahl offered various technology examples and insight and processes which enabled different applications which are state-of-the art today. Furthermore, he concentrated on the needs, where are the hidden aspects and needs to enable MEMS for mass production.

It was followed by a session of workshops and presentations with possible job advertisements.

Here, Tobias Hanke from the wafer level test development gave an overview of the custom development for MEMS technology in the talk "MEMS wafer test". Various examples were shown, which emphasized that MEMS were non-standard in various domains and showed how to tackle test equipment and test conditions.

Afterwards, Mirko Hofmann, director of the MEMS design house, gave a talk entitled "MEMS Design

House—Design & Simulation". Mr. Hofmann concentrated on the principal transducer design and optimization. He highlighted the challenges of tolerances, cross coupling and environmental influences caused by the impact of packaging, which need to be considered during the design phases prior to the mass production.

Ronald Gampp, the director of the packaging department gave a talk "MEMS Packaging". He gave more insights on the main concern of mechanical stress induced on the MEMS element, which itself is mechanical. He gave some examples, i.e. on laser dicing and automized pick up tools, to overcome these challenges.

After the various insights in technology, Matthias Laemmlin from Bosch Sensortec gave a talk on "MEMS Sensors for Consumer Electronics". Mr. Laemmlin showed the new solutions of smart sensors, including embedded algorithms for artificial intelligence for sensors. Furthermore, he gave an overview on applications of sensors nowadays.

Finally, Josef Goeppert, director of power semiconductor and modules department, offered more insights in power electronics and electrical drives which can vary from a few kilowatts up to several megawatts. Also, he concentrated on the SiC development in Reutlingen and showed finally an impressive video of overload failures during testing and how to actively handle short circuit overload.

The event ended with some final conclusion and thanks to all participants and presenters for their active contributions and questions during the day.

IEEE Ukraine Section (West) MTT/ED/AP/EP/SSC Joint Chapter DIPED-2020 Seminar/Workshop Dedicated to the Memory of Prof. Nikolai Voitovich

by Mykhaylo Andriychuk

On September 15–18, 2020, the 2020 IEEE XXVth International Seminar/Workshop on Direct and Inverse Problems of Electromagnetic and Acoustic Wave Theory (DIPED-2020) took place in Tbilisi, Georgia. The event was co-organized by the IEEE MTT/ED/AP Georgia Chapter, Tbilisi State University, Ukraine Section (West) MTT/ED/AP/EP/SSC Joint Chapter, and Pidstryhach Institute for Applied Problems of Mechanics and Mathematics, NASU, with the support of the IEEE Electron Devices, Microwave Theory & Techniques, and Antennas & Propagation Societies as the technical co-sponsors. The DIPED-2020 was dedicated to the memory of Prof. Nikolai N. Voitovich, the founder of the first IEEE EDS Chapter in Ukraine and co-organizer of the DIPED Seminar/Workshop series. This year's technical program consisted of 32 papers submitted by scientists from Georgia, Germany, Greece, Israel, Turkey, Russia, USA, and Ukraine, and covered the following sections: Diffraction and Scattering, Propagation in Complex Media, Numerical and Optimization Techniques, Antenna Design, Fabrication and Testing, Acoustics.

Prof. Nikolai Voitovich (1940–2020)

At the Opening Ceremony, Dr. Mykhaylo Andriychuk, Program Committee Secretary, presented the memory talk about the life stages and scientific achievements of Prof. Voitovich, a famous scientist in the area of electromagnetic field propagation and antenna theory, and a multitalented respected person who passed away this year at the age of 80.

Nikolai Voitovich graduated from Lviv State University in 1961 with Master Degree in Computational Mathematics, earned his Ph.D. in Radio Physics from the Institute of Radio Engineering and Electronics (IRE), Moscow, Russia, in 1968, and received his D.Sc. in Radio Physics from Kharkiv State University in 1982. His D.Sc. work "Investigation of high-quality resonators and dielectric waveguides by means of generalized eigenvalue problems" was considerable contribution to the well-known generalized method of eigen-oscillations (GMEO), which is successfully applied to solving the series of internal and external problems of Electrodynamics.

Prof. Voitovich contributed significantly to international scientific cooperation. Thus, starting in 1982, the scientific forum in the field of high frequency Electrodynamics with participants from Georgia, Poland, Russia, and Ukraine, was originated. Due to his enthusiasm, the forum took the title "Direct and Inverse Problems of Electromagnetic and Acoustic Wave Theory (DIPED)" and became the annual IEEE International Seminar/Workshop afterwards. In 1995, owing to the IEEE initiative for involving scientists of Eastern Europe and the Former Soviet Union (FSU) countries in the worldwide scientific community, as well as due to the efforts of Prof. Voitovich, the IEEE West Ukraine Joint Chapter was established. It was one of the first IEEE Chapters in Ukraine and in the FSU countries. Initially, the Chapter joined the IEEE Electron Devices and Microwave Theory & Techniques Societies, and one year later the IEEE Antennas & Propagation Society. The next development of the Chapter was joining the IEEE CPMT (now Electronic Packaging) and SSC Societies in 1997 and 1999, respectively. The first years of the West Ukraine Chapter with Prof. Voitovich as a Chapter Chair were filled with fruitful and impressive work. In 2000, Chapter won the IEEE CPMT 1999 Chapter of the Year Award being one of the first among the IEEE Chapters from Eastern Europe and FSU countries earning such a recognition. That boosted further development of the Chapter's activity and its improvement both scientifically and technically, especially in the areas related to the parent IEEE Societies. So the next awards were not long in coming. In 2001, the Chapter was recognized by the 2001 IEEE Region 8 Chapter of the Year; in the second decade of 2000s, the Chapter won the IEEE Antennas and Propagation Society 2017 Outstanding Chapter Award, IEEE Electron Devices 2017 Region 8 Chapter of the Year Award, and IEEE Microwave Theory and Techniques Society 2017 MTT-S Outstanding Chapter Award. And it is impossible to overestimate the role, efforts, and

eagerness of Prof. Voitovich, permanent honorary Chapter Chairman, which always were crucial factors in winning the above mentioned awards. The cooperation with the IEEE helped to renew the DIPED and make it the annual Seminar/Workshop as a joint event of both the MTT/ED/AP/EP/SSC West Ukraine and MTT/ED/AP/EMC Georgian Chapters since 1995. In 1997, the DIPED became an IEEE event, technically co-sponsored by AP, ED, and MTT Societies, that enabled the inclusion of DIPED Proceedings into the IEEE Xplore Digital Library. The credit for successfully holding all DIPEDs is owed largely to enthusiasm, organization efforts, and permanent care of Prof. Voitovich.

Dr. Tamar Nozadze, Organizing Committee Secretary, serving the DIPED-2020 online sessions

The scientific results of Prof. Voitovich are very impressive. He is the author of 9 monographs, more than 190 papers in the international scientific journals and conference proceedings. His research works gained recognition worldwide. In 1989, Prof. Voitovich together with his teacher, Prof. Katsenelenbaum and other authors of the GMEO, were recognized by the Ukrainian State Award in the Area of Science and Technique for the series of scientific papers "The Theory of Resonant Scattering and its Application in Radiophysics." The memory paper of Prof. Voitovich prepared by his Georgian friends and followers from Ukraine was included into the DIPED-2020 Proceedings. The scientific results of his research over the last year's period were presented in two research papers of the above Proceedings. Thus, improving the Chapter activity and carrying on the traditions of the DIPED Seminar/Workshop will be a good remembrance of Prof. Voitovich who was the founder of these both projects.

This year, the DIPED Seminar/Workshop was arranged online. Prof. Revaz Zaridze, Organizing Committee Chairman, Dr. Tamar Nozadze, Organizing Committee Secretary, Dr. Tamar Gogua, responsible person of the Tbilisi State University, and whole team of our Georgian colleagues did their best to make the DIPED-2020 successful.

~Kateryna Arkhypova, Editor

TEC Costa Rica Recipient of the 2020 IEEE Electron Devices Society Student Branch Chapter of the Year Award

IEEE EDS Student Branch Chapter Instituto Tecnológico de Costa Rica

* Esteban Arias-Méndez, Chapter Advisor and Student Branch Counselor
* Danny Xie-Li, Chapter Chair and Student Branch Chair

From Latin America, in Central America, Nicaragua to the north and Panama to the south, surrounded to the east by the Caribbean Sea and to the west by the Pacific Ocean there is located **Costa Rica**, the country of ¡*Pura Vida*! and *Gallo Pinto*, famous for its beaches, volcanos, biodiversity, and culture. With a population of just 5 million people in 51 000 km^2.

The IEEE EDS Student Branch Chapter from Instituto Tecnológico de Costa Rica (Costa Rica Institute of Technology) or TEC Costa Rica, was founded in January, 2020 by 10 students, some of them with previous IEEE volunteering experience and some new.

There was a lot of work to do ahead. As a new chapter, we didn't have a web page, social media, where we could spread the news of the activities, and logo that represented us. So we set a starting rock of the chapter. We planned some activities at the university to start as the chapter. In the last week of February 2020, we were invited to the LAEDC Costa Rica conference, where we had the opportunity to meet many people from different parts of the world, some people from a

local industry, and distinguished people in the field. Later, we invited some of them to share their knowledge with the students within our own activities. As time went by, the pandemic hit our country. That time we had to cancel all the activities we had organized because most of them were face-to-face activities, like workshops.

Face-to-Face to Virtual

As a result of the COVID-19 pandemic, the activities could not be tours or lectures and face-to-face workshops, among others. We had to **innovate** and bring everything to virtuality. We restarted with the talk: "*You at home and your mental health with you,*" from the Department of Guidance and Psychology, as a way to reconnect with members and the TEC community in the middle of times of uncertainty.

In the end, the virtuality became an advantage, because it allowed us to invite distinguished national and international speakers, which would not be possible in person, not counting a large number of international attendees. Talks like: "An Introduction to Open Source Hardware Development Leveraging Open Source Software Workflows," "Cybersickness," "Design Thinking"; participation in the IEEE UN SDG week organized by the Student Branch at TEC Costa Rica and even a programming competition called "Electron CodeWars" was organized by the chapter members.

Be a Volunteer, a Way to Build a Better Tomorrow

We like to welcome EDS and IEEE members in our activities as well as people from the community interested in them. The synergy that this generates can achieve a great impact in the world that can last forever. This is a motivation for the members to keep going. If you want to change the world you need to put one step in the road.

Some Recommendations, from Our Chapter to Yours

We like to have constant communication with chapter members and the community through our Telegram group chat and social networks on Facebook and Instagram. Nowadays, chat apps and social networks are central to good communication. For the coronavirus outbreak, these channels were the key for us to easily and quickly move to virtual events.

Members development should be the goal of the chapter, and, to achieve that, you need good communication channels with them. We encourage volunteers to organize and develop their own ideas and activities, so they can learn by doing, which can improve them academically and professionally in the near future. If you want to succeed with activities, it's good to have a person in charge and provide support and follow up on time.

Social activities such as virtual board games are spaces where people can have the opportunity to destress and to meet new friends. In other words, make social distance a social approach in this virtual age.

Work with other student branches and student chapters around the

Some EDS Student Branch Chapter members, TEC Costa Rica

world to have the opportunity to collaborate and meet their culture and way of thinking, is relevant for the growth of the person's thinking for all the society members.

We believe that one of the main benefits you get as a member is the possibility to get in contact with people from all over the world, like right now. And the chapters have to serve as connection points, as it provides extra value for members.

COVID-19 has affected our regular activities worldwide, but also it has been a trigger to get in touch with people everywhere, and both share, and be a part of activities in other countries.

Our main interest is to promote science, technology, and research. There are many talented young people at TEC and we seek to harness all that knowledge to benefit the country.

We face a difficult time this year. The pandemic hit us in different ways. Somehow and somewhat you can start to think that it is the end of everything, but we should take the pandemic as a challenge, that could make us stronger to face the future.

Stay tuned to our social media, the best is yet to come. Warm greetings from Costa Rica, ¡Pura Vida!

EDS Student Branch Chapter Board of Directors 2020

- Chair: Danny Xie-Li
- Vice chair: Alejandro Díaz-Pereira
- Fiscal: Fabián Montero-Villalobos
- Secretary: David Azofeifa-Herrera
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Social Media

- Facebook: https://www.facebook.com/EDSTECCR
- Instagram: https://www.instagram.com/eds.ieee.tec/

Contact

* Esteban Arias-Méndez, *Advisor*, email: earias@ic-itcr.ac.cr
* Danny Xie-Li, *Chair*. email: dnnxl@ieee.org

EDS Cares: Face Mask Loop Extender and Face Shield for SMK 18 Shah Alam Muslimah Student and teachers

Dr. Maizatul Zolkapli and Dr. Ahmad Sabirin Zoolfakar from Universiti Teknologi MARA (UiTM) organized a community program in conjunction with the reopening of school sessions throughout Malaysia after the conditional movement control order (CMCO). Concerned about the students' wellbeing, especially the female students who wear hijab, the pair together with the staff of Electrical Engineering Faculty of UiTM utilized their expertise and facilities of available 3D printers to produce face mask loop extenders and face shield brackets. It becomes easier for female students and teachers to put masks on the faces and at the same time comply with the guidelines set by the Ministry of Education Malaysia. All the 560 pieces of face mask loop extenders and 120 pieces of face shields were handed over to Tuan Haji Kamali bin Murid, Principal of Sekolah Menengah Kebangsaan Seksyen 18 Shah Alam for the use by students and teachers.

EDS members volunteering during the COVID-19 pandemic

Regional News

Europe, Middle East & Africa (Region 8)

ED Poland Distinguished Lecturer Mini-Colloquium

—by Krzysztof Górecki

A virtual EDS Distinguished Lecturer (DL) Mini-Colloquium "Semiconductor-based sensors—technology, modeling, applications" was held on June 27, 2020. It was organized by the ED Poland Chapter with technical support by the Lodz University of Technology. The meeting consisted of five lectures and was attended by more than twenty researchers and Ph.D. students.

The lecture "Ultralow Power, High-Resolution Sensor Interfaces" was given by Prof. Arokia Nathan (DL) from Cambridge Touch Technologies, UK. Prof. Nathan addressed the design and operational requirements of vacuum deposited and printed thin film transistors for wearable applications in which low power and high signal resolution are critical requirements, especially for detection of physiological signals.

The talk "Sensor Design—From Prototype to Series" was delivered by Dr. Mike Schwarz from Robert Bosch GmbH, Germany. The speaker presented a flow and methodology of integration of all the sensor perspectives, from prototyping to series production. He discussed examples of typical Sensor/MEMS designs including various mechanical and electronic constraints.

The lecture "Compact Modeling and Parameter Extraction for Oxide and Organic Thin Film Transistors (TFTs) from 150K to 350K" was given by Prof. Benjamin Iñíguez (DL) from Universitat Rovira i Virgili, Spain. He made a review of the physics and of DC, AC and noise modeling of Organic and Oxide Thin-Film Transistors (TFTs). He discussed direct methods to extract model parameters in the temperature range from 150K to 350K.

The talk "Nanometrology using MEMS/NEMS devices" was delivered by Prof. Teodor Gotszalk from Wroclaw University of Technology, Poland. The speaker presented numerous examples of solutions developed mainly by his team for atomic force microscopy, scanning thermal microscopy, photonics and related disciplines.

The lecture "Phase change electro-optical devices for space applications" was delivered by Prof. Mina Rais-Zadeh (DL) from NASA Jet Propulsion Lab., California Institute of Techn., USA. The speaker shared her expertise in the area of phase change materials for photonics and RF applications. She presented advanced concepts of GeTe application for realization of electro-optical devices with application in Space.

~Marcin Janicki, Editor

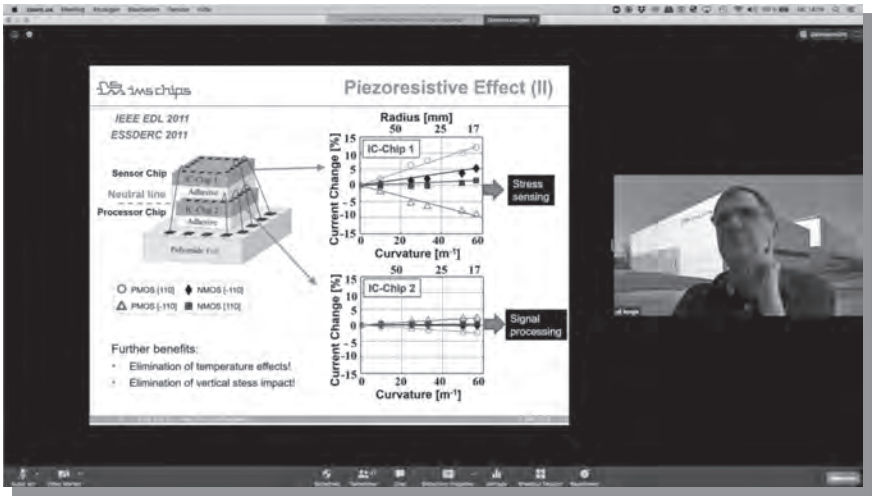
Germany Chapter Presents IEEE EDS Mini-Colloquium on "Non-Conventional Devices and Technologies"

—by Mike Schwarz

The 2020 IEEE ED Germany Chapter MQ "Non-conventional Devices and Technologies" was held from September 30th to October 1st, 2020. It was organized jointly with the Spring MOS-AK Workshop and the Symposium on Schottky Barrier MOS (SB-MOS) devices (see the separate article). The MQ was attended by 71 participants, with 23 IEEE participants and 48 guests. Prof. Mike Schwarz opened the Minicolloquium as the ED Germany Chapter chair.

The first lecture was given by Prof. Benjamin Iniguez from Universitat Rovira i Virgili on the topic "Analysis and modeling of OTFTs and IGZO TFTs from 150 to 350K". Prof. Iniguez reviewed recent results regarding the modeling of OTFTs and IGZO TFTs and their benchmarking with measurements. Different aspects of the metal-insulator-semiconductor structure, facile manufacturing, compatibility with flexible substrates were discussed. A comparison of carrier mobilities in OTFTs and IGZO TFTs was also discussed.

Prof. Joachim Burghartz from IMS Chips gave a lecture "Ultra-Thin Si Chips—A New Paradigm in Silicon Technology". He broadly discussed



Prof. Joachim Burghartz during the lecture "Ultra-Thin Si Chips—A New Paradigm in Silicon Technology."

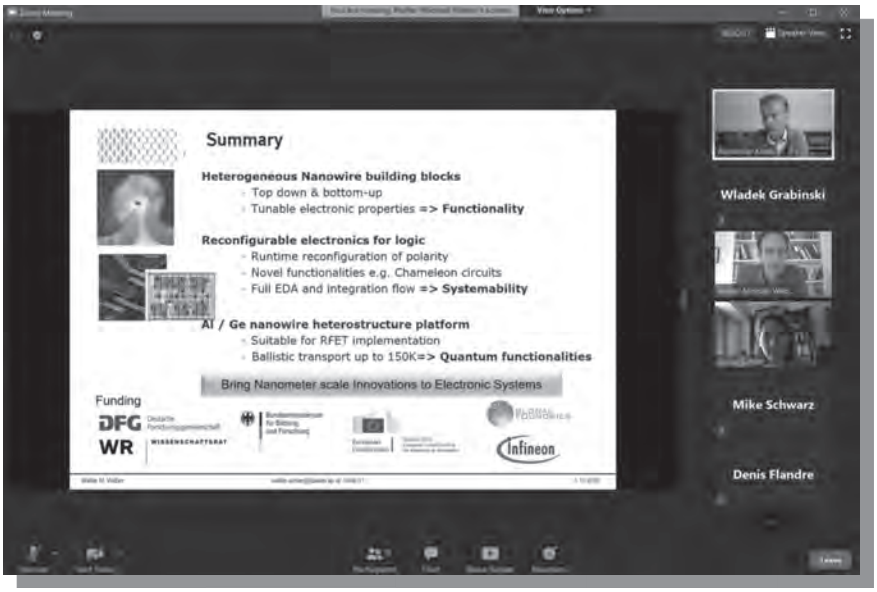
the advantages and challenges of ultra-thin silicon chips. Special focus was given to the piezoresistive effect and its benefits for eliminating temperature effects and vertical stress impact.

Dr. Wladek Grabinski from MOS-AK presented a talk "FOSS TCAD/EDA Tools for Advanced Compact Modeling." He gave an overview of existing open source tools for process- and device simulation including SPICE-family tools, and mechanical FEM simulators.

Next Dr. Frank Schwierz from TU Ilmenau gave a very detailed lecture "2D Electronics—Opportunities and Challenges." After an introduction of 2D materials, including a discussion of bandgaps of different 2D semiconducting materials, a comparison of their effective masses and the effects of direct source to drain tunneling and its suppression were discussed.

The final lecture was given by Prof. Tibor Grasser from TU Vienna on "Stability and Reliability of 2D Transistors". Prof. Grasser addressed material properties, discussed the typical defects, oxygen vacancies, and their impact on the charging behavior. Finally, effects such as the impact of charge defects were discussed.

A huge "Thank you" to all the participants and lecturers.



Discussion after the talk by Prof. Walter Weber

Joint Spring MOS-AK Workshop and Symposium on Schottky Barrier MOS (SB-MOS) Devices with IEEE EDS Mini-Colloquium on "Non-Conventional Devices and Technologies"

—by Mike Schwarz

The Joint Spring MOS-AK Workshop and Symposium on Schottky Barrier MOS (SB-MOS) devices with IEEE EDS Mini-Colloquium on "Non-conventional Devices and Technologies" was held from September 29 to October 1, 2020. While it was initially planned for spring at THM—University of Applied Sciences in Giessen (Germany), it was shifted to the early autumn due to the COVID-19 pandemic. However, finally the local organizers of NanoP—Competence Center for Nanotechnology and Photonics of THM decided to move it to Zoom and perform it virtually. It was sponsored by THM, the EDS Germany Chapter, the IEEE Young Professionals Germany Affinity Group, and the AdMOS company. The event was attended by 69 IEEE members and 115 non IEEE members (guests) from 25 countries during the three days.

The event started with the MOS-AK workshop. It was opened by Dr. Wladek Grabinski and Prof. Alexander Kloes. The first presentation was given by Dr. Markus Mohr from Ulm University and entitled "Fabrication and Application of Nanocrystalline Diamond Thin Films and Hybrid Diamond-Silicon Sensor Applications".

After a short coffee break the event continued with a talk by Aristeidis Nikolaou from THM on the topic "Statistical circuit analysis by NOVA (Noise Based Variability Approach)". It was followed by an overview presentation by Prof. Alexander Kloes entitled "Approaches for analytical (compact) modeling of tunneling current in MOS transistors".

The afternoon session was opened by Mahimna Dwivedi from AdMOS who presented a collaborative work with IMS Chips "Modeling of GaN HEMTs on Silicon Substrate". Then Lixi Yan from University of Stuttgart presented a work "Adopting the Industry-standard CMOS Models for Si Vertical Power MOSFETs".

The first day was closed after a coffee break by a talk "Overview of Gnucap, the GNU Circuit Analysis Package" presented by Al Davis from Gnucap Team (USA) and by Axel Fischer from SweepMe! team (Germany) with a talk "SweepMe!—a modular, flexible, and versatile software platform for device characterization".

The second day continued with the MOS-AK and a talk "Injection Barrier Modification by Organic Monolayers" by Dr. Alrun Hauke from Philipps-Universität Marburg. It was followed by a presentation "Quantitative Investigation of the Interplay between Intrinsic Transistor Noise and Circuit Nonlinearities" given by Leopold Van Brandt (UC Louvain).

The MOS-AK was closed by the talks of Dr. Ghader Darbandy and Dr. Mike Schwarz. Dr. Darbandy presented the work "Emerging Devices: RFET and OPBT". Dr. Schwarz discussed methodologies for high volume productions in a lecture "Simulation and Modeling of Semiconductor

Devices in MEMS". The MOS-AK was finally attended by 73 participants.

After the lunch, Dr. Schwarz opened as German Chapter chair the IEEE MQ "Non-conventional Devices and Technologies" (see a separate detailed article).

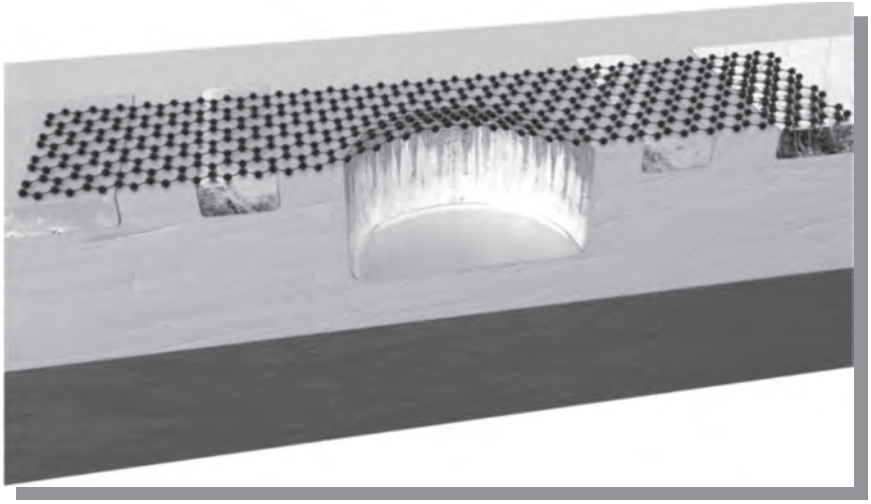
After the Mini-Colloquium, the 4th Symposium on Schottky Barrier MOS Devices was opened with some historical remarks by Prof. Mike Schwarz and Dr. Laurie Calvet. Then they introduced the first speaker Dr. Zhenxing Wang from AMO GmbH. Dr. Wang gave a talk "Metal-Insulator-Graphene RF Diodes: From Devices to Integrated Circuits". Afterwards, Dr. Laurie Calvet from Universite Saclay Paris presented a talk "Schottky barrier devices for neuromorphic computing".

After a coffee break Prof. Walter Weber from TU Vienna gave some insights on heterostructures during the presentation entitled "Nanowire metal-semiconductor heterostructures for functionality enhancement and quantum transport". Finally, Dr. Hans Kleemann from TU Dresden presented a lecture "Schottky-type Contacts in Ultra-Short Channel Organic Semiconductor Devices for GHz-Operation". The Symposium on SBMOS was attended by 40 participants.

Finally, the organizers Prof. Alexander Kloes, Dr. Wladek Grabinski, Dr. Laurie Calvet, and Prof. Mike Schwarz thanked all presenters and participants for this fantastic event. All of you made it happen!

Nanoelectromechanical Sensors Made of 2D Materials—an Overview

—by Frederica Haupt and Mike Schwarz



Schematic representation of a pressure sensor based on a suspended graphene membrane (Image: S. Wagner @ AMOGmbH)

Max Lemme with collaborators published recently in the magazine RESEARCH an overview article on nanoelectromechanical (NEMS) sensors based on floating two-dimensional (2D) materials. RESEARCH is a multidisciplinary open access journal that was launched in 2018 as the first journal in the Science Partner Journal (SPJ) program. The paper is an "Invited Paper" for a special edition entitled "Progress and challenges in emerging 2D nanomaterials preparation, processing and device integration" with the aim of developing the area of 2D materials for sensor applications and integrating them into conventional semiconductor technology to contribute.

"I believe that NEMS sensors based on 2D materials will make a significant contribution to meeting the demand for integrated, high-performance sensors that result from applications such as the Internet of Things (IoT) and autonomous mobility," said Lemme. The report summarizes extensive studies that have successfully demonstrated the feasibility of using membranes made of 2D materials in pressure sensors, microphones, mass and gas sensors, explains different sensor concepts and gives an overview of the relevant material properties, production methods and functional principles of the devices.

"Two-dimensional materials are ideal for sensors," says Lemme, "because they allow free-standing structures to be realized that are only a few atoms thick. This ultimate thinness can be a decisive advantage with nanoelectromechanical sensors, since the performance is often crucially dependent on the thickness of the suspended component. In addition, many 2D materials have unique electrical, mechanical and optical properties that can be used for completely new concepts of sensor devices."

The report contains contributions from RWTH Aachen, AMO GmbH, the University of the Bundeswehr in Munich, the KTH Royal Institute of Technology, TU Delft, Infineon and the Kavli Institute of Nanoscience. Different readout and integration methods of different sensors based on the 2D materials are discussed here, and they offer comparisons with the state of the art to demonstrate both challenges and opportunities of the nanoelectromechanical sensors based on the 2D materials.

"Sensor devices based on floating 2D materials are almost always smaller than their conventional counterparts, have improved performance and sometimes even completely new functionalities," says Peter G. Steeneken, head of work package 6 (sensors) in the Graphene flagship and the co-author of the contribution. "However, there are still enormous challenges to show that NEMS sensors based on 2D materials can outperform conventional devices in all

important aspects—for example in establishing profitable manufacturing options. The graphene flagship represents the ideal platform to address these challenges as it encourages collaboration between leading global groups to achieve a number of clearly defined goals. This paper is an example of how we can do more by bringing together complementary expertise."

6th Joint EuroSOI—ULIS 2020 Conference

—by Bogdan Cretu and Mike Schwarz

The 6th joint EuroSOI—ULIS 2020 Conference was held from September 1st–30th. Because of COVID-19 situation, the EuroSOI-ULIS 2020, initially planned to be held at Caen (Normandy, France), became a virtual conference. The next 2021 edition will be at Caen (Normandy, France) on September 1st–September 3rd, and the EuroSOI-ULIS 2022 will take place at Udine (Italy).

Each year this international conference brings each year together more than 100 expert researchers in semiconductor technologies. This year 75 participants from 4 continents (Europe (50 from 11 countries), Asia (10 from 4 countries), South and North America (12 from Brazil and 2 from USA), Australia (1)) attended the conference.

The 2020 edition included 4 plenary talks and 53 regular contributions: 34 "oral" and 19 "poster" presentations.

Pre Recorded videos/commented slides of each paper (oral or poster) presentations were available in the respective thematic channels. Discussions took place on the general or thematic channel (recommended) or as direct conversations with the presenters/authors of the papers presented at EuroSOI-ULIS 2020.

A live presentation was arranged only for the first plenary talk of Cezar Zota (IBM, Zurich, Switzerland). Prerecorded video presentations of the plenary talks were proposed by Prof. Eddy Simoen (imec, Leuven, Belgium), Prof. Jung-Hee Lee (Kyungpook National University, South Korea) and Prof. Mark Lundstrom (Purdue University, Indiana, USA). The participants could see the presentations in advance, and during the provided time slots only the key points of the different presentations were reminded for discussion/exchanges to take place.

The first plenary talk of EuroSOI—ULIS entitled "Novel Electron Devices for the Quantum Era" was delivered by Dr. Cezar Zota from IBM Zurich. Dr. Zota gave a great talk to 33 attendees during the live session. He introduced the participants into the Quantum computing topic at IBM. He discussed various types of quantum computing: Quantum Annealing, Approximate NISQ-Computing, and Fault-tolerant Universal QC. Inside of an IBM Q quantum computing system (see Figure) were discussed for various temperature regimes. Discussions on quantum volume (calculation score) took place, where the error rate stands as a dominating issue in combination with the number of qubits.

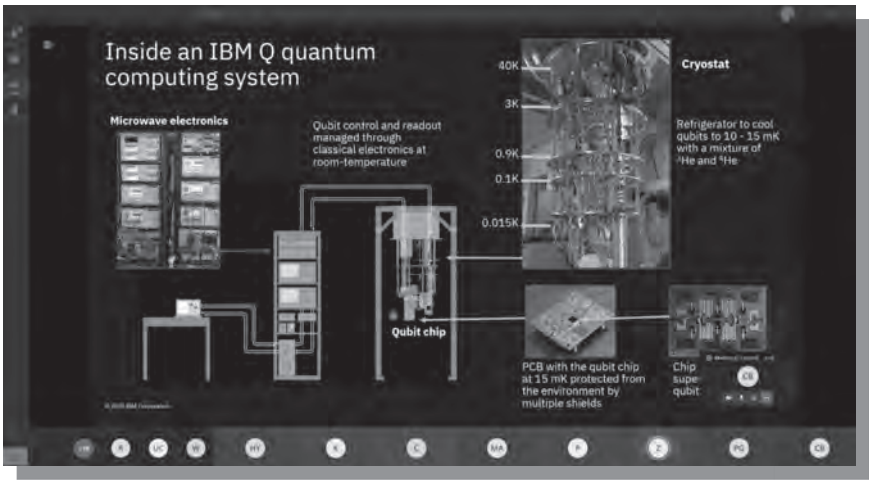
Afterwards, operation, control and scalability were discussed. Topics such as Quantum Gates, IBM qubits by Josephson qubits/junctions and oscillators were highlighted. Additionally, the talk emphasized the typical architectures. Here, the focus was especially set to electron devices for different temperature regimes. Generally, electronics in the cryogenic regime is demanded, e.g. logic controllers, signal generators, ADCs, LNAs, etc. Furthermore, III-V materials for cryogenic electronics were discussed.

Finally, novel cryogenic devices and materials were introduced. Here, important parameters such as the transconductance in the cryogenic regime and self heating were in the focus. Especially, the self heating at the cryo regime is responsible almost in 50% for the on-chip temperature.

The second plenary talk of EuroSOI—ULIS entitled "Horizontal, stacked or vertical silicon nanowires: does it matter from a low-frequency noise perspective?" was delivered by Prof. Eddy Simoen from IMEC.

Prof. Simoen held a *Question and Answer* session to 20 attendees during a live session of his recorded talk. In this very interesting talk, Prof Eddy Simoen firstly reminded the audience the basics of 1/f noise and its mechanisms. He showed that the device scaling leads to an increase of the device-to-device 1/f noise dispersion, while the average value could remain the same.

A relationship between the 1/f noise and the device architecture, i.e. horizontal NW FETs on SOI, stacked NW FETs and vertical NW FETs was



Plenary talk "Novel Electron Devices for the Quantum Era" was held in MS Teams by Dr. Cezar Zota from IBM Zurich

discussed. It was pointed out that the mechanism responsible for the 1/f noise is the carrier trapping/detrapping (carrier number fluctuations) in the horizontal NW FETs on SOI and stacked NW FETs, while in the vertical NW FETs the mobility fluctuations prevail. Ways to optimize the 1/f noise level in horizontal NW FETs on SOI were debated, however, it was pointed out that the stacked NW FETs present one decade lower noise than horizontal NW FETs on SOI substrates. Even if the 1/f mechanism is different in the vertical nanowire FETs, the advantage of this architecture from the noise point of view is that it presents a decade lower surface normalized 1/f noise than the stacked NW FETs.

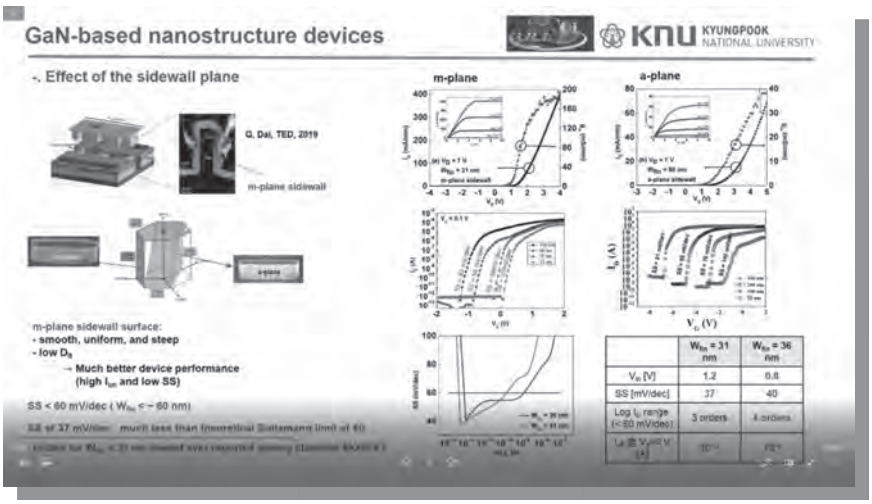
The third plenary talk "Fabrication and characterization of GaN-based nanostructure field-effect transistors (FETs)" was given by Prof. Jung-Hee Lee (Kyungpook National University, South Korea).

Prof. Lee reminded the importance of III-V based devices for RF and power application, and the critical issues of this III-V technology, e.g. trapping effects leading to a decrease of the output current, and possible ways to improve the device performance. It was argued that the GaN-based FinFETs or NW FETs show a suppression of a buffer trapping and reduction of an off-state leakage current, and present fast switching characteristics.

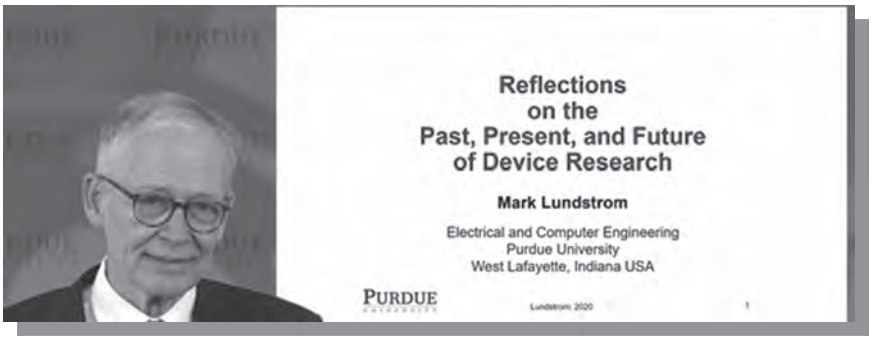
The fabrication steps and performances of AlGaN/GaN-based FinFETs and GAA GaN vertical nanowire MOSFETs were presented in detail. It was pointed out that using the concept of channel width modulation and simultaneous turn-on, fast switching characteristics with subthreshold swing below the theoretical limit for diffusive transport (60 mV/dec) may be achieved in AlGaN/GaN-based FinFETs. It was highlighted that the device simulation with a multi-level trap model and a self-heating effect reproduces the transfer characteristics of the GAA GaN vertical nanowire MOSFETs. Due to a very good electrostatic control, low drain saturation voltage, low threshold voltage and good subthreshold characteristics with high I_{on}/I_{off} ratio, these devices are promising for low voltage logic applications.

The fourth plenary talk entitled "Reflections on the Past, Present, and

Prof. Eddy Simoen answering questions during his plenary session on "Horizontal, stacked or vertical silicon nanowires: does it matter from a low-frequency noise perspective?"



Plenary talk "Novel Fabrication and characterization of GaN-based nanostructure field-effect transistors (FETs)" was held in MS Teams by Prof. Jung-Hee Lee from Kyungpook National University



Plenary talk "Reflections on the Past, Present, and Future of Device Research" was held in MS Teams by Prof. Mark Lundstrom from Purdue University

Future of Device Research" was given by Prof. Mark Lundstrom (Purdue University, Indiana, USA).

In the visionary presentation, Prof. Lundstrom reminded the past and recent evolution of devices and pointed out the essential physics of transistors and the transport theory for the 21st Century.

In a very pedagogic way, Prof. Lundstrom explained the electron transport, the current flow in a nano device, the "Fermi window," the operation at 0K, and the quantized conductance. He elaborated on the transport equation in bulk semiconductor, and in the nano-scale to the macro-scale devices.

Several open questions: "Is there a new device that will invent its own applications?", "How do we prepare students and working engineers to succeed in the 21st Century physical electronics?" animated the wonderful discussion. The key problematics and concepts of single-electron devices were debated.

Virtual Mini-Colloquium (MQ) on Photonics and Photovoltaics

—by Benjamin Iniguez and Mike Schwarz

A Virtual Mini-Colloquium (MQ) on Photonics and Photovoltaics was organized by the ED Spain Chapter, in collaboration with the Department of Electronic, Electrical and Automatic Control Engineering of the Universitat Rovira i Virgili (URV, Tarragona, Spain). It took place on July 31, 2020.

The Chair of this MQ was Prof. Benjamin Iñiguez, Full Professor at URV and Chair of the ED Spain Chapter.

The MQ included three talks given by EDS Distinguished Lecturers, addressing different issues related to Photonics and Photovoltaics. Prof. Ioannis Kymissis, Columbia University (NY, USA) targeted "LED and OLED Devices for Biomedical Optics". Prof. Angèle Reinders (Technical University of Eindhoven, The Netherlands) conducted a lecture entitled "Design-Driven Research on Solar Powered Mobility." Finally, Prof. Magali Estrada (CINVESTAV, Mexico) talked about "Fundamentals of bulk heterojunction organic solar cells: An overview of main parameters, state of the art and strategies for improvement."

~ Mike Schwarz, Editor

Asia & Pacific (Region 10)

ED Taipei Chapter

—by Steve Chung

A Post-Conference Review of 2020 SNW and 2020 VLSI

The ED Taipei Chapter together with the EDS NCTU Student Chapter held a one–day workshop on July 10th, giving post-conference reviews of the virtual 2020 IEEE Silicon Nanoelectronics Workshop (SNW) and the 2020 Symposium on VLSI Technology (VLSI). The SNW was initially scheduled from June 12–13 and was available in a virtual format from June 12–21. VLSI was scheduled from June 10–14 while the virtual meeting was available until the end of August. All presentations were available in pre-recorded videos, with live Q&A sessions provided for speakers and authors. In order to promote both activities, the chapter asked experts who participated in both conferences to present several major research of interest topics for the conferences. Six topics were presented:

1) AI and Memory (T. H. Hou),
2) 3D Packaging and Heterogeneous Integration,
3) Advanced CMOS Manufacturing,
4) Quantum Computing for Electrical Engineers (P. W. Li),
5) Ferroelectric FETs and 2D Materials Devices (C. J. Su),
6) Selected Papers from SNW (K. S. Chang-Liao).

Three of the six speakers were Distinguished Lecturers (Profs. P. W. L, H. C. Lin, and K. S. Chang-Liao). The program began with Prof. Steve Chung giving a brief status of both the SNW and VLSI, and providing an overview

Attendees of the workshop

ED Taipei Workshop on July 10th; Chair and speakers: Steve Chung, P. W. Li, K. S. Chang-Liao, T. S. Chao, B. Y. Tsui, T. H. Hou

of the major events of the IEEE Electron Devices Society. He encouraged students to join IEEE and EDS, and instructed them on how to be good writers and presenters in the VLSI. In this workshop, the organizer also invited major IC company leaders to have extensive discussions with professors and students. This talk was attended by more than 130 professors, and graduate students, and by leaders from Science Park semiconductor companies.

VLSI-TSA conference, August 13th: Keynote Q&A (speaker: Mark Ritter-IBM) and audience

2020 VLSI-TSA and VLSI-DAT Symposia

Since 1983, the VLSI-TSA and VLSI-DAT symposia are among the major and premier events on VLSI technology in the region and worldwide. The 2020 VLSI-TSA and VLSI-DAT (https://expo.itri.org.tw/2020vlsitsa) were held on August 10–13, 2020. Considering the COVID-19 pandemic worldwide, i.e., travel restrictions, this meeting was held in a hybrid form. An onsite physical meeting was organized on August 10–13 for all the local participants, while pre-recorded presentations were arranged as a video presentation available on-demand for one-month (August 14-Sept. 13) to all the audience. A majority of the ED Taipei Chapter members were involved in the organization of the conference. Prof. Steve Chung served as the Technical Program Chair of TSA, responsible for all the virtual program presentation and the on-site meeting. Both TSA and DAT symposia are sponsored by the IEEE EDS, CAS, and SSCS. The symposia attracted over 840 attendees worldwide in the technical sessions and more than 350 in a series of short courses, in which around 57% were from the industry and 43% from the universities. It was truly a very successful conference, which benefited from the well-controlled environment in Taiwan, which was nearly immune to the coronavirus. For your information, next year the conference is scheduled to be held April 19–22, 2021, in Hsinchu. Papers can be submitted online: https://expo.itri.org.tw/2021vlsitsa/Submission. The paper submission deadline is November 9, 2020. For further information, please contact Miss Caroline Huang, vlsitsa@itri.org.tw.

IEEE EDS Distinguished Lecture—ED/SSC Nanjing Chapter

—by Weifung Sun

The EDS/SSCS Nanjing Chapter co-hosted on July 21, 2020, a webinar by Prof. Merlyne De Souza, a Full Professor in Electronics at The University of Sheffield (UK) and Distinguished Lecturer of the IEEE Electron Devices Society. The title of her webinar, "From CMOS to neuromorphic computing, with a peek into the future," was selected as this research direction has been chosen to be one of the top 10 priorities by local and national Chinese governments.

At the heart of the electronics revolution, lies a four-terminal transistor: the humble Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET). Combining p and n type MOSFETs forms the basic unit of complementary logic that inverts a signal from '1' to '0' and vice versa. Scaling of this transistor according to Moore's law has had a transformative effect on society, giving us products from computers, laptops to smart phones, that have made life virtually unrecognizable with regards the one 50 years ago. This talk was focused on the physics of operation of the MOSFET leading towards present day challenges of sub-threshold operation. Combining memory with CMOS presents one possible pathway for massively parallel and highly energy efficient neuromorphic computing systems of the future.

The webinar was successful with more than one hundred scholars and students attending from all around the world.

IEEE EDS Invited Lecture—ED Tainan Chapter

—by Wen-Kuan Yeh

The ED Tainan Chapter held an invited presentation at Tainan, Taiwan, September 24, 2020. Prof. Kuan-Neng Chen (IEEE Fellow, Distinguished Professor, Department of Electronics Engineering, National Chiao Tung University) gave a talk "3D Integration, Advanced Package, and Heterogeneous Integration" at National Cheng-Kung University. This talk focused on the advanced package technology including Interposer, CoWoS, and InFO for related applications. About 60 attendees and several professors of universities from south Taiwan attended to meet Prof. Chen.

Prof. Kuan-Neng Chen with members of the ED Tainan Chapter on September 24, 2020

IEEE EDS Invited Lecture—ED Xi'an Chapter

—by Ranran Zhao

On September 29, 2020, the ED Xi'an Chapter held an invited presentation at Xidian University, Xi'an, China. Dr. Eric Liao, the general manager of Payton Technology, presented his chip research story. Dr. Liao demonstrated the key and new technologies of Payton Technology Company. He also introduced to the students the allocation and application of memory chips, the design and production of packages, and the future development direction of related technologies. Eric Liao actively and warmly asked questions and interacted with the students, who responded positively and shared their own feedback.

The Report Session of EDTM-2020—ED Japan Joint Chapter

—by Toshiro Hiramoto and Masaharu Kobayashi

On July 27, 2020, the report session of IEEE EDS 4th Electron Devices Technology and Manufacturing (EDTM) Conference 2020 (http://ewh.ieee.org/conf/edtm/2020/) was organized. This year the conference was formatted as a full virtual event. Dr. Kazunari Ishimaru, International Advisory Committee of EDTM-2020, reported on conference activities and Dr. Shuji Ikeda explained plans for the EDTM in 2021.

At the report session, subcommittee members reported the trends of their respective technical sessions:

- Subcommittee on Si Devices, Dr. Masumi Saitoh (Kioxia).
- Subcommittee on Process, Dr. Anupam Mitra (Kioxia).
- Subcommittee on Modeling, Prof. Risho Koh (Renesas Electronics).

The program and announcement of this report session are posted on the EDS Japan Joint Chapter's webpage: https://www.ieee-jp.org/section/tokyo/chapter/ED-15/2020/Home/EDTM2020_ReportSession_en.pdf.

The next EDTM (IEEE EDTM-2021), is planned as an in-person/on-site event in Chengdu, China, on March 9–12, 2021. (https://ewh.ieee.org/conf/edtm/2021/index.html)

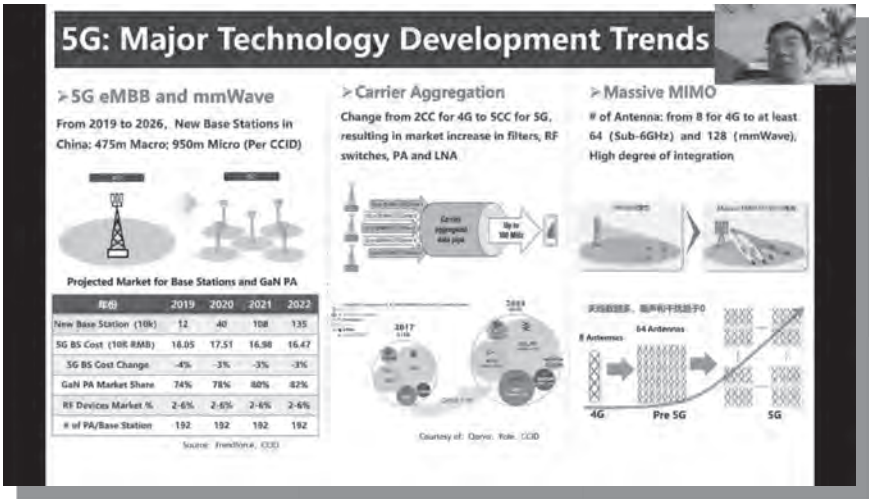
Dr. Eric Liao presenting at the ED Xi'an Chapter on September 29, 2020

The Electron Devices and Solid-State Circuits Online Seminar Series ED/SSC Hong Kong Joint Chapter

—by Qiming Shao

On April 9, 2020, the first Electron Devices and Solid-State Circuits (EDSSC) Online Seminar Series was held online via the Zoom platform. The EDSSC Online Seminar Series is a new series of seminar talks hosted by the IEEE ED/SSC Hong Kong Joint Chapter. The seminars are normally co-organized by one of the local institutions in Hong Kong, such as the Hong Kong University of Science and Technology (HKUST), University of Hong Kong (HKU), etc. Due to the pandemic, the originally scheduled EDSSC 2020 in Hong Kong was canceled. The EDSSC Online Seminar Series was initiated to continue to disseminate research frontiers and knowledge to local and nearby students.

Until now, seven EDSSC seminars were held and a few seminars are scheduled for the near future. The topics covered 5G, neuromorphic computing, emerging memory, bioelectronics, etc. Among the invited speakers there were well-established researchers (e.g., IEEE Fellow Prof. Philip H.-S. Wong from Stanford University), newly graduated PhDs (e.g., Dr. Xiang Li from Stanford University), or excellent PhD candidates (e.g., Mr. Jiahao Han from Massachusetts Institute of Technology). On average, there were roughly 50 enrollments for each seminar. On July 9, 2020, Prof. Tianling Ren gave an IEEE Distinguished Lecture on "Flexible electronic devices for physiological signal monitoring." The students exhibited their interest in EDSSC-related topics, asked questions, and provided



A screenshot from EDSSC seminar (via Zoom) by Dr. Yong-Hui Fan of the Innovation Center of Advanced Devices for Future Communication, Shenzhen, China, titled "Technology Trend and Market Opportunity of 5G Industry in China"

positive feedback on these seminars. To facilitate knowledge sharing, presentations were uploaded to YouTube, (https://www.youtube.com/channel/UCI58hLw3fM2T14VL3Naq4Hw), and Bilibili (https://space.bilibili.com/581518520). More information about the ED/SSC Online Seminar Series can be found on our newly launched ED/SSC Hong Kong Chapter website: https://r10.ieee.org/hk-edssc/seminars/.

~Ming Liu, Editor

ED Malaysia Kuala Lumpur Chapter

—by Maizatul Zolkapli, Ahmad Sabirin Zoolfakar, Haslina Jaafar, Nurul Ezaila Alias, Norazreen Abd Aziz and Aliza Aini Md Ralib

IEEE EDS Malaysia Virtual Distinguished Lecture 2020

IEEE Electron Devices Society (EDS) Malaysia Chapter successfully organized the first virtual distinguished lecture (VDL) on July 27, 2020. Two EDS distinguished lecturers, Prof. Xing Zhou from Nanyang Technological University, Singapore and Prof. Gananath Dash from Sambalpur University, India were invited by the Chapter. Prof. Xing Zhou delivered a talk "Monolithic Co-integration of III-V Materials into Foundry Si-CMOS in a Single Chip for Novel Integrated Circuits" whilst Prof. Gananath gave the lecture entitled "Influence of Structural and Operating Parameters on the Performance Characteristics of Graphene Nanoribbon Field Effect Transistors (GNRFETs)". 66 local and international participants attended this 2-hour webinar which was conducted via Cisco Webex online platform. The participants enjoyed the lectures and a short discussion wrapped up the session. Both presentations were also recorded and the link can be accessed via the EDS Malaysia Section Chapter website.

The 14th IEEE-International Conference on Semiconductor Electronics (ICSE 2020) and Appreciation Meeting

The 2020 IEEE International Conference on Semiconductor Electronics (ICSE2020) was successfully held from July 28–29 2020. This was the 14th conference in the ICSE series which started in 1992 to gather semiconductor micro- and nanoelectronics researchers from academia and industry.

In the light of COVID-19 Pandemic, this year's 2020 IEEE ICSE was the first ever virtual ICSE conference organized through WebEx Platform. The conference was organized by the IEEE Electron Devices Society Malaysia Section Chapter. The conference was chaired by IEEE EDS Malaysia Chapter Chair; Prof. Ir. Dr. Norhayati Soin. Themed "At the Edge of Nanotechnology", 48 papers covering topics such as device modelling, simulation and design; device physics and characterization; nanoelectronics and processes; VLSI design; electronics materials and device fabrication; optoelectronics and photonics technology; electronics materials and device fabrication; MEMS/NEMS and lastly emerging technologies & simulations were presented at the conference. The authors were from various countries including Malaysia, India,

Prof. Xing Zhou from Nanyang Technological University, Singapore and Prof. Gananath Dash from Sambalpur University, India

China, Germany, United Arab Emirates, Nigeria, Bangladesh, Saudi Arabia, Iraq, Taiwan, USA, Japan, United Kingdom and Indonesia.

The conference was honoured to have 3 esteemed keynote speakers joining this year's conference. Professor Dr. Zhigang Ji from Shanghai Jiaotong University, China gave a lecture "Reliability in advanced logic devices and emerging memories—From deterministic to Stochastic". Professor Dr. Gananath Dash from Sambalpur University, India had a presentation "An Iterative Simulation Method for the Current Voltage Characteristics of Graphene Field Effect Transistors" Professor Dr. Nizar Hamidon from Universiti Putra, Malaysia delivered a talk "Nano In Sensor Technology".

The conference achieved its main objective of bringing together researchers from industry and academia to gather and explore various issues and trends in the field of semiconductor electronics. Results of the best paper/best presenter awards are as follows:

1. Best Paper Award

Title of Paper: A comparative study on the performance of 1S-1R and Complementary resistive switching models

Authors: Arya Lekshmi Jagath & Nandha Kumar Thulasiraman from University of Nottingham Malaysia Campus

2. Best Student Presenter Award

Title of Paper: Numerical Modelling of MoS2/h-BN/graphene photodetector for self-powering application

Presenter: Umahwathy Sundararaju from Universiti Kebangsaan Malaysia

The IEEE EDS and ICSE2020 appreciation and retreat meeting was held from 19–20 September 2020 at Concorde Hotel Shah Alam. The ceremony was held as a token of appreciation to all the Conference Committee members who had worked so hard in ensuring the success of the 2020 IEEE International Conference on Semiconductor Electronics (ICSE) which was held on July 28–29, 2020. In conjunction with the retreat, the IEEE EDS Committee Meeting no. 8 and ICSE2020 meeting no. 12 were held. This was the first time for EDS to conduct such an event, to which all the past chairs were also invited. During the meeting, the Conference and Chapter Chair presented the appreciation certificates to all the ICSE2020 Committee members. Prof. Dato' Dr. Burhanuddin Yeop Majlis, the advisor of EDS Malaysia was given the honour to make a short speech during the opening of the ceremony.

Members of EDS during the EDS and ICSE2020 appreciation ceremony

2020 IEEE EDS Malaysia Chapter Final Year Project Award

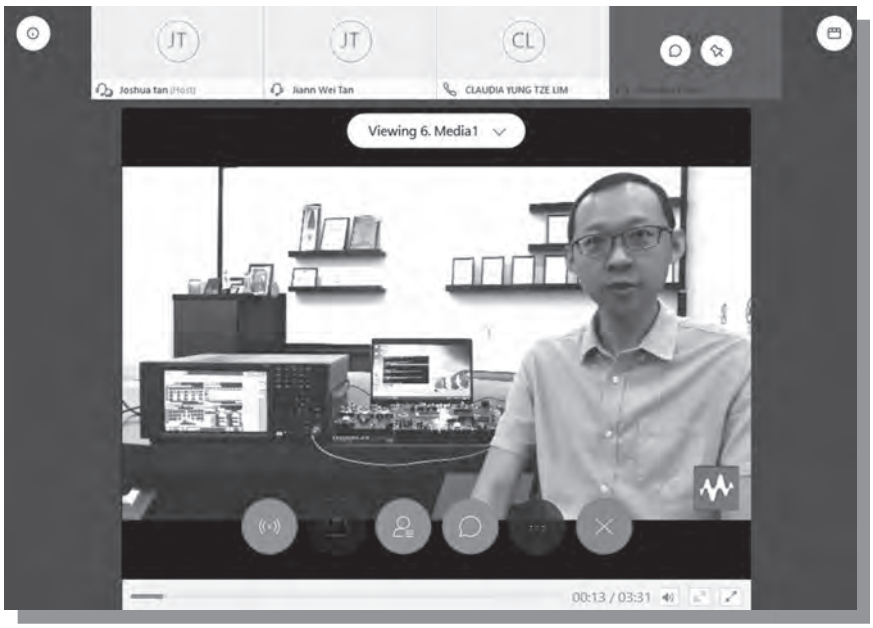
IEEE EDS Malaysia Chapter sponsored six awards for 2020 Final Year Project (FYP) Award organized by several universities in Malaysia. The awards are to encourage FYP projects related to VLSI, MEMS/NEMS etc. and to acknowledge student's work in these areas.

The winners are as below. Congratulations to all the award recipients!

No	University	Award Winner	Title
1	Universiti Malaya (UM)	Tan Jia Pei	Design, Simulation and Construction of Interface circuit for biosensors
2	Universiti Kebangsaan Malaysia (UKM)	Goh Hui Ying	Shape optimization of Piezoelectric Transducer for Vibrating Mesh Nebulizer
3	Universiti Islam Antarabangsa Malaysia (UIAM)	Dilruba Ruhksana	Development of a 2D Stretchable Strain Sensor for Facial Expressions
4	Universiti Teknologi Mara (UITM)	Nor Farahanim bt Nordin	Sol Gel coated optical fibre as a pH sensor
5	Universiti Sains Islam Malaysia (USIM)	Haikal Iqmal bin Hamdan	Electrochemical detection of tributryin using graphene oxide functionalized screen printed electrode as fat content measurement
6	Universiti Putra Malaysia (UPM)	Azman Babah	Carbon Nanotube Strain Sensor for Human Motion Detection

FYP EDS Award winner from Universiti Sains Islam Malaysia: Haikal Iqmal bin Hamdan

The participants of 2nd EDS Lecture Series at Universiti Putra Malaysia



Overview by Keysight Technologies personnel

EDS Malaysia 2nd Lecture Series 2020 and ITMA UPM visit

The second lecture series was held on September 22, 2020 at Universiti Putra Malaysia (UPM). About 30 attendees, including EDS members and students enjoyed the talk given by Assoc. Prof. Dr. Nafararizal Nayan from Universiti Tun Hussein Onn. He talked about the magnetron sputtering technique for versatile thin film deposition. On the same day, after the talk, 12 EDS members visited the Institute of Advanced Technology, Universiti Putra Malaysia. The Institute Director, Prof. Dr. Mohd. Nizar b. Hamidon welcomed us by giving an overview of the facilities and services that were available in the institute. We visited the functional devices laboratory, analysis laboratory and the characterization laboratory.

EDS UKM Student Branch Chapter

by Norazreen Abd Aziz

A Keysight Webinar 2020 was co-organized on June 10, 2020 by IEEE Electron Devices Society (EDS) UKM Student Branch Chapter in collaboration with Keysight Technologies. The session started with an overview of Keysight Technologies offer and staff. Next, graduates and internship opportunities were presented. Then, a real World IoT & 5G signal testing, and emotional intelligence exploration issues were introduced. Participants of the sessions were also shown the virtual laboratory presentation on 5G/IoT signal testing using CXA series products. More than 30 Electrical and Electronic Engineering students attended this program and benefited tremendously from the webinar.

~P Susthitha Menon, Editor

ED NIT Silchar Student Branch Chapter

—by T. R. Lenka

The ED NIT Silchar Student Branch Chapter organized a virtual DL Talk "GaN-HEMT based front end Transceiver for 5G Communication Technology" by Prof. Ajit Kumar Panda. The lecture was held on June 27, 2020 at the Department of Electronics and Communication Engineering, National Institute of Technology Silchar, Assam, India. The talk was attended by 31 participants, both IEEE members and non-members, including the faculty, the UG/PG/PhD scholars of the Department, and outside institution members.

On July 31, 2020, a virtual DL Talk "Challenges and Directions for Nanoelectronics to Nanotechnology" by Prof. Durga Misra, New Jersey Institute of Technology (NJIT), Newark was organized at the Department of ECE, NIST Assam, India. In this talk, some of the very recent developments and trends in a nano-scale device design and state-of-the-art fabrication of the next generation electronic devices and Internet of Things (IoT) devices were presented. The talk was attended by around 90 participants comprising the IEEE EDS members and non-members, including the faculty, the UG/PG/PhD scholars of the Department, and members of other institutions in India and abroad.

The Chapter in association with the Department of ECE, NIST Silchar, Assam, India and with the Institute Innovation Cell, NIT Silchar conducted a Five Days Online National Workshop "Recent Trends in Innovative CMOS-MEMS Technologies and applications: Hands on Learning", The Workshop was held from Sept 11–15, 2020 under funding from Technical Education Quality Improvement Programme, Phase III (TEQIP-III). Twelve invited speakers from India as well as from abroad delivered lectures in the workshop. The workshop was attended by around 100 participants comprising the IEEE EDS members and non-members, including the faculty, the UG/PG/PhD scholars of the ECE Dept. of NIT Silchar, and members of other institutions from India and abroad. The workshop was coordinated by Dr. Koushik Guha, Dr. Kavicharan, and Dr. Bijit Choudhury of the Dept of ECE, NIT Silchar along with Prof. F. A. Talukdar (Branch Counselor) and Dr. T. R. Lenka (Faculty Advisor).

ED Uttar Pradesh Section Chapter, ED15 Kanpur

—by Amit Verma

The ED Kanpur Chapter organized two online distinguished lectures, one by Prof. Mansun Chan, (Dept. of ECE, Hong Kong University of Science & Technology, Hong Kong) on August 12, 2020 and another by Dr. Simon Deleonibus (Chief Scientist of Research (Retired), CEA-LETI, France) on August 26, 2020. Prof. Chan presented a talk entitled "Memory Modeling for Neuromorphic Computing" highlighting the simulation infrastructure required for neuromorphic computing and the approach to develop memory models that can handle temporal variations of signals in neurons according to the in-coming signals and data. In the second distinguished lecture, Dr. Deleonibus presented the talk "New routes and paradigms in Device Engineering for Nanoelectronics and Nanosystems" emphasizing on energy and variability efficiency as being the major concerns and opportunities for future nanoelectronics development. The lectures were attended by more than 30 people including students and faculty, more than half of which were IEEE members.

ED Nepal Chapter

—by Bhadra Pokharel

The IEEE EDS Nepal Chapter organized a virtual Distinguished Lecture by EDS DL Prof. Dr. Ajit Kumar Panda, National Institute of Science and Technology, Berhampur, Odisha, India. The title of the presentation was "**GaN-HEMT based front-end Transceiver for 5G Communication Technology.**" The talk available online was held in Kathmandu on May 30, 2020. It was attended by 21 people. Among them there were 14 IEEE members and 7 students and faculty members.

ED MSIT Student Branch Chapter Report

—by Manash Chanda

The Chapter organized the 2020 IEEE VLSI Device, Circuit and System Conference (VLSI-DCS), which was held on July 18–19, 2020. More than 100 papers were presented apart from 20 Plenary and Keynote speakers and more than 100 oral/poster presentations.

The Chapter in association with the Department of ECE, Meghnad Saha Institute of Technology (MSIT), Kolkata organized a Technical Talk Program by Mr. Sankalp Jain, SoC Implementation Engineer, Apple, Austin, USA. The event was held on September 15, 2020. About 105 participants were present, out of which 35 were IEEE members. Moreover, Prof. Sudeb Dasgupta delivered on August 22, 2020 an illuminating talk on low power integrated circuit design. About 96 participants attended the session. Among them there were 54 IEEE members and 65 non-IEEE members. All the participants gained many benefits from the lecture.

ED Netaji Subhash Engineering College Student Branch Chapter

—by Saheli Sarkhel

The chapter and the Department of Electronics and Communication Engineering, in association with IEEE EDS Kolkata Chapter, organized a two-day webinar "4G and 5G Security-Opportunities and Challenges", which was held from September 26–27, 2020. The webinar was led by Dr. Ashutosh Dutta, who was an IEEE fellow, a senior scientist and

5G Chief Strategist at Johns Hopkins University, USA. The virtual meeting was attended by 60 students and faculty members.

ED Kalyani Government Engineering College Student Branch Chapter

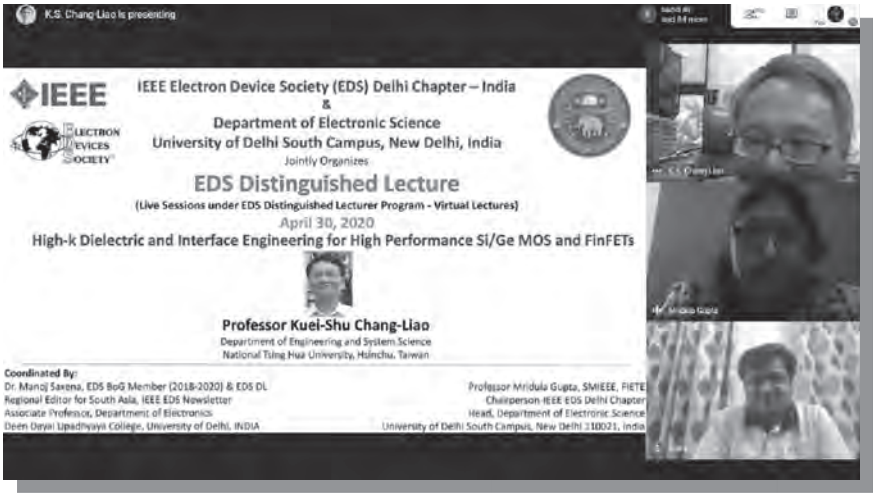
—by Angsuman Sarkar

The IEEE ED Kalyani Government Engineering College Student Branch Chapter organized a series of technical lectures. On June 29, 2020 Dr. Soumya Pandit, Assistant Professor in the Institute Of Radiophysics & Electronics, University of Calcutta delivered a talk "Integrated Circuit Amplifier." The lecture was given online using the WebEx platform. 57 participants attended virtually this event. Next, a Technical Lecture by Dr. Bhaskar Gupta, Professor in Jadavpur University, Kolkata, entitled "An Introduction to RF-MEMS Technology" was given on June 30, 2020. The talk, given in the online mode using the Webex platform, was attended by 72 participants. The chapter organized also the EDS DL talk by Prof. Paul Berger from Ohio State University, USA, who is also with Tampere University, Finland as a Fulbright-Nokia Distinguished Chair. The Lecture entitled "Fully Printable and Autonomously Powered Electronic Nodes for the Internet of Everything," was held on July 16, 2020 in the online mode using the WebEx platform. The virtual meeting was interactive and very useful for all the participants. A total of 70 participants attended this event.

ED Delhi Chapter Activities

—by Mridula Gupta and Harsupreet Kaur

The chapter organized a series of online DL talks under "EDS Distinguished Lecturer Program—Virtual Lectures" program so that IEEE EDS members could benefit from the expert talks in a time when it is not possible to organize in-person talks due to the ongoing crisis. During this period 14 DL talks were organized and these talks provided a wide exposure to participants about various emerging areas. All DL talks were jointly organized by IEEE EDS Delhi Chapter and Department of Electronic Science, University of Delhi South Campus.



Prof. Chang-Liao, Prof. Mridula Gupta (Chairperson of EDS Delhi Chapter) and Dr. Manoj Saxena

The first in the series was the IEEE Distinguished Lecture "High-k Dielectric and Interface Engineering for High Performance Si/Ge MOS and FinFETs" by Professor Kuei-Shu Chang-Liao, National Tsing Hua University, Taiwan, held on April 30, 2020. The talk focused on various aspects of High-k dielectric engineering and engineering of interfaces and buffer layers in various advanced devices to improve the device performance.

Dr. Yang Chai from the Hong Kong Polytechnic University delivered on May 1, 2020 a Distinguished Lecture on the topic "Two-dimensional Layered Materials for Nanoelectronics". The speaker emphasized that two-dimensional layered semiconductors possess ultrathin body, atomic scale smoothness, dangling bond-free surface, reasonable good mobility, and sizable bandgap, which enables promising applications in nanoelectronics.

The DL entitled "Introducing two-dimensional layered dielectrics in solid-state microelectronic devices" was given on May 5, 2020 by Prof. Mario Lanza from Soochow University, China. Prof. Lanza gave an in-depth lecture about two-dimensional (2D) layered materials.

On May 6, 2020, a DL "Field Effect Transistors: From MOSFET to Tunnel-FET" was delivered by Prof. Dr. Joao Antonio Martino, University of Sao Paulo, Brasil. The speaker gave an overview of the main progress steps of FET evolution over the last few decades.

Prof. Marcelo Antonio Pavanello, University Center of FEI, Brasil, delivered on May 8, 2020 a DL on the topic "Junctionless Nanowire Transistors: Electrical Characteristics and Compact Modeling". Prof. Pavanello discussed the emerging devices with particular emphasis on junctionless devices.

The next two DLs were organized on May 11 and May 12, 2020. First, Prof. Maria Merlyne De Souza, The University of Sheffield, UK, gave a lecture "From CMOS to Neuromorphic Computing-A peek into the future". Prof. De Souza discussed that combining memory with CMOS presents one possible pathway for massively parallel and highly energy efficient neuromorphic computing systems of the future. Next, Prof. Mina Rais-Zadeh, NASA Jet Propulsion Laboratory, USA, gave a lecture "Phase Change electro-optical devices for

space applications". She emphasized in particular features of germanium telluride (GeTe) that undergoes significant change in refractive index, which can be used for implementing optical switch, modulator, and diffraction gratings.

The DL by Prof. Michael S. Shur, Rensselaer Polytechnic Institute, USA, on the topic "State-of-the-Art Silicon Very Large Scale Integrated Circuits: Industrial Face of Nanotechnology", was delivered on May 15, 2020. Prof. Shur talked about the advent of quantum dots and the tremendous evolution of CMOS devices.

On May 16, 2020, Prof. Arokia Nathan, Cambridge Touch Technologies, UK, delivered a DL "Transparent and Flexible Large Area Electronics". Prof. Nathan gave a detailed overview about how amorphous semiconductors have opened a new realm of applications whereby a transparency and a mechanical flexibility associated with low-temperature processing on flexible substrates are important requirements.

The DL "Trends and challenges in Nanoelectronics for the next decade" was delivered on May 20, 2020 by Dr. Elena Gnani, University of Bologna, Italy. Dr. Gnani talked about the impact of nanoelectronic devices and in particular, how in the last decade nanoelectronic devices have been a driving force for societal applications and for a green sustainable world.

On May 22, 2020, a DL "Accelerating commercialization of SiC power electronics" was delivered by Dr. Victor Veliadis, North Carolina State University, US. Dr Veliadis gave an overview of silicon carbide power devices. Emphasis was placed on high impact application opportunities where SiC devices are expected to displace their incumbent Si counterparts.

The next DL "Advanced III-N Devices for 5G and Beyond" was delivered on May 27, 2020 by Prof. Patrick Fay, University of Notre Dame, US. The main message was that to obtain the low latency and high bandwidths required on a mobile platform, devices offering millimeter-wave performance with low power consumption while simultaneously delivering low noise figure, high linearity, and the ability to be integrated into complex systems in compact form factors are essential.

On May 31, 2020, Prof. Benjamin Iñiguez from Universitat Rovira i Virgili, Spain, delivered a DL "Compact Modeling and Parameter Extraction for Oxide and Organic Thin Film Transistors (TFTs)". Prof. Iñiguez discussed the recent advances in Organic Thin Film Transistors and presented various compact models.

The last DL in the series, entitled "FOSS TCAD/EDA tools for Compact/SPICE Modeling" was delivered on June 03, 2020 by Dr. Wladek Grabinski, MOS-AK Association. Dr. Grabinski presented an overview of various open source software tools used for TCAD/SPICE simulation and discussed the recent advances.

All the DLs reported above were insightful and comprehensive. They were very well received. Each DL had more than 100 attendees: students, faculty members and participants from across the world. Besides the DLs mentioned above, the Chapter co-organized the following two events.

An Online Summer School on Advances in Signal Processing and Machine Learning was jointly organized by MHRD-Institution Innovation Council, DDUC Chapter, Deen Dayal Upadhyaya College, University of Delhi (under the aegis of DBT Star College Program), Department of Electronic Science, University of Delhi and National Academy of Sciences India (NASI)—Delhi Chapter from July 20, 2020 to July 25, 2020. The Summer School was supported by the IEEE Electron Devices Society (EDS), Delhi Chapter. More than 400 students, researchers and faculty members attended the Summer School. On July 23, 2020, a special public webinar was organized on the topic "When to trust a self-driving car…" by Prof. Marta Kwiatkowska, FRS, Associate Head of MPLS Division, Fellow of Trinity College Department of Computer Science University of Oxford. On July 24, 2020, a special public evening webinar on the topic "A Reinforcement Learning Framework for Mobile Relay Beamforming" was held by Professor Athina Petropulu, President-Elect, IEEE Signal Processing Society (2020–2021), Distinguished Professor, Department of Electrical & Computer Engineering, Rutgers, The State University of New Jersey.

The 7th International conference on Microelectronics, Circuits and Systems (MICRO 2020) was jointly organized by Applied Computer Technology, Kolkata, India and Delhi Technological University during July 25–26, 2020. The conference in the virtual mode was supported by IEEE EDS Delhi Chapter. The conference was attended by more than 100 participants. Prof. Shinichi Takagi, Department of Electrical Engineering Graduate School of Engineering, The University of Tokyo, Japan delivered the keynote address. Various other renowned speakers such as Prof. Jerzy Szymanski, Electrical Engineering and Informatics, Kazimierz Pulaski University of Technology and Humanities, Poland, Dr. Jacopo Iannacci, Centre for Materials and Microsystems (CMM), Fondazione Bruno Kessler (FBK), Trento, Italy, Dr. Mohd Faizul Bin Mohd Sabri, Associate Professor, Department of Mechanical Engineering, University of Malaya, Malaysia also delivered invited talks. Over 50 papers were presented during the online conference.

~Manoj Saxena, Editor

EDS MEETINGS CALENDAR

The complete EDS Calendar can be found at our web site: http://eds.ieee.org. Please visit.

2021 15th European Microwave Integrated Circuits Conference (EuMIC)	12 Jan – 14 Jan 2021	Utrecht, Netherlands
2021 5th IEEE Electron Devices Technology & Manufacturing Conference (EDTM)	09 Mar – 12 Mar 2021	Chengdu, China
2021 IEEE International Reliability Physics Symposium (IRPS)	21 Mar – 25 Mar 2021	Virtual Event
2021 22nd International Symposium on Quality Electronic Design (ISQED)	07 April – 08 April 2021	Santa Clara, CA USA
2021 IEEE 34th International Conference on Microelectronic Test Structures (ICMTS)	12 April – 15 April 2021	Cleveland, OH USA
2021 IEEE Latin America Electron Devices Conference (LAEDC)	18 April – 20 April 2021	Virtual Event
2021 32nd Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC)	02 May – 05 May 2021	DC, WA USA
2021 International Siberian Conference on Control and Communications (SIBCON)	12 May – 14 May 2021	Kazan, Russia
2021 IEEE International Memory Workshop (IMW)	15 May – 18 May 2021	Dresden, Germany
2021 33rd International Symposium on Power Semiconductor Devices and ICs (ISPSD)	29 May – 02 June 2021	Nagoya, Japan
2021 Silicon Nanoelectronics Workshop (SNW)	12 June – 13 June 2021	Kyoto, Japan

2021 Symposium on VLSI Technology	13 June – 16 June 2021	Kyoto, Japan
2021 IEEE 48th Photovoltaic Specialists Conference (PVSC)	19 June – 24 June 2021	Fort Lauderdale, FL USA
2021 International EOS/ESD Symposium on Design and System (IEDS)	23 June – 25 June 2021	Chengdu, SICHUAN, China
2021 IEEE International Interconnect Technology Conference (IITC)	05 July – 08 July 2021	Kyoto, Japan
2021 9th International Symposium on Next Generation Electronics (ISNE)	10 July - 12 July 2021	Changsha, China
2021 IEEE International Flexible Electronics Technology Conference (IFETC)	07 Aug – 10 Aug 2021	Columbus, OH USA
2021 35th Symposium on Microelectronics Technology and Devices (SBMicro)	22 Aug – 26 Aug 2021	Campinas, Brazil
2021 16th European Microwave Integrated Circuits Conference (EuMIC)	10 Oct – 11 Oct 2021	London, United Kingdom
2021 IEEE/ACM International Conference On Computer Aided Design (ICCAD)	31 Oct – 03 Nov 2021	Munich, Germany
2021 IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)	06 Nov – 08 Nov 2021	Redondo Beach, CA USA
2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)	04 Dec – 10 Dec 2021	Monterey, CA USA

Call for Papers
for a Special Issue of
IEEE Transactions on Electron Devices
on
"New simulation methodologies for next-generation TCAD tools"

Technology Computer Aided Design is used to simulate semiconductor processes and devices, a field which has become increasingly complex and heterogeneous. Processing of integrated circuits requires nowadays over 400 process steps, and the resultant devices often have a complicated 3D structure and contain various materials. The full device behavior can only be understood by considering effects on all length scales from atomistic (interfaces, defects etc.) over nanometric (quantum confinement, non-bulk properties etc.) to full chip dimensions (strain, heat transport etc.), and time scales from femtoseconds to seconds. Voltages, currents and charges have been scaled to such low levels that electronic noise, statistical effects and process variations have a strong impact. Devices based on new materials (e.g. 2D crystals) and physical principles (ferroelectrics, magnetic materials, qubits etc.) challenge standard TCAD approaches. While the simulation methods developed by the physics community can describe the basic device behavior, they often lack important simulation capabilities like, for example, transient simulations or integration with other TCAD tools and are too slow for daily use. Due to the complexity of semiconductor technology, it becomes more and more difficult to assess the impact of a change in processing or device structure on circuit performance by looking at a single aspect of an isolated device under idealized conditions. Instead a TCAD tool chain is required that can handle realistic device structures embedded in a chip environment. New methodologies are required for all aspects of TCAD to ensure an efficient tool chain covering from atomistic effects to circuit behavior based on flexible simulation models that can handle new materials, device principles and the ensuing large-scale simulations.

This Special Issue of the IEEE Transactions on Electron Devices will feature the most recent developments and the state of the art in the field of TCAD for processing and for device behavior with a focus on new methodologies that improve the tool chain. Papers must be new and present original material that has not been copyrighted, published or accepted for publications in any other archival publications, that is not currently being considered for publications elsewhere, and that will not be submitted elsewhere while under considerations by the Transactions on Electron Devices.

Topics of interest include, but are not limited to:

- Artificial Intelligence applied to TCAD
- TCAD device models for
  - o new materials (2D materials, oxides, organic semiconductors, oxide semiconductors, nanowire devices etc.)
  - o new device types (magnetic devices, memristors, spintronics, qubits, sensors etc.)
  - o physical effects (ferroelectric dielectrics, thermal transport at nanoscale, atomistic simulation etc.)
  - o simulation conditions that push the limits of standard TCAD: ballistic transport, THz frequencies, cryogenic conditions, device degradation, electromagnetic and plasma waves in active devices, transient simulations, noise and fluctuations, microscopic simulation of large power devices
- Process simulation
  - o Atomistic process simulation to generate structures for atomistic device simulations (including both interconnects and transistors)
  - o Gate stack modeling including dipole diffusion
  - o Stress simulation for nanosheet and forksheet devices and stress simulations including layout effects
  - o Topological simulation
  - o Equipment simulation
- New methods for the TCAD tool chain
  - o Self-consistent integration of simulation models into the hierarchy
  - o Device-circuit interaction
  - o Multi-physics and multi-scale integration
  - o Efficient use of the data produced along the chain
  - o Workflow improvements
  - o Methods that improve the turn-around-time for TCAD simulations

Submission instructions: Manuscripts should be submitted in a double column format using an IEEE style file. Please visit the following link to download the templates: http://www.ieee.org/publications_standards/publications/authors/author_templates.html
In your cover letter, please indicate that your submission is for this special issue.

Submission deadline: February 28, 2021 **Publication date: November 2021**

Guest Editors:

1. Prof. Fabrizio Bonani, Politecnico di Torino, Italy
2. Dr. Stephen Cea, Intel Corp., USA
3. Prof. Elena Gnani, University of Bologna, Italy
4. Prof. Sung-Min Hong, GIST, Republic of Korea
5. Dr. Seonghoon Jin, Samsung, USA
6. Prof. Christoph Jungemann, RWTH Aachen, Germany
7. Prof. Xiaoyan Liu, Peking University, China
8. Dr. Victor Moroz, Synopsys, USA
9. Dr. Anne Verhulst, imec, Belgium

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