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Edited by Daniel Tomaszewski, EDS Newsletter Editor-in-Chief, and Manoj Saxena, EDS Newsletter Associate Editor-in-Chief

The annual IEEE IEDM conference (www.ieee-IEDM.org), sponsored by the IEEE Electron Devices Society, is the world's largest, most influential forum for the unveiling of breakthroughs in transistors and related micro/nanoelectronics devices. At IEDM each year, the world's best scientists and engineers in nano/microelectronics gather to participate in a technical program.

The 67th IEEE IEDM was scheduled for 11–15 December 2021 at the Hilton San Francisco Union Square Hotel. The main theme of the 67th annual IEEE IEDM was "*Devices for a New Era of Electronics: From 2D Materials to 3D Architectures*." The Conference was held in-person with online access to recorded content afterward.

"This year the IEEE IEDM conference features a rich collection of presentations on topics that are on everyone's minds. Among them are the advent of 2D materials, the growing number and diversity of 3D architectural concepts, the rise of system/technology co-optimization, and the possible end of Moore's Law. Breakthroughs in these and other areas will be presented and discussed, and ultimately will help the industry and society as a whole move forward," said Meng-Fan (Marvin) Chang, IEDM 2021 Publicity Chair, IEEE Fellow, Distinguished Professor of Electrical Engineering at National

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Your Comments Solicited

Your comments are most welcome. Please write directly to the Editor-in-Chief of the Newsletter at daniel.tomaszewski@imif.lukasiewicz.gov.pl

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Issue	Due Date
October	July 1st
January	October 1st
April	January 1st
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A Review of the 67th IEEE International Electron Devices Meeting

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Tsing Hua University, and Director of Corporate Research at TSMC. "New, fast-growing electronics applications often require novel semiconductor solutions," said Srabanti Chowdhury, IEDM 2021 Publicity Vice Chair and Associate Professor of Electrical Engineering at Stanford University. "With 3D technologies offering many intriguing ways to get around scaling issues, they open up new and exciting possibilities for highly integrated systems with far greater capabilities," she added.

When organizing the Conference, great emphasis was placed on educational opportunities. "As the COVID-19 pandemic has demonstrated, the world is becoming increasingly reliant on electronic technologies. The good news is that the IEDM Tutorials and Short Courses will provide attendees with the invaluable knowledge and information needed to advance the state-of-the-art in critical areas of the field," said Meng-Fan (Marvin) Chang. "The opportunity to engage with the world's technical leaders in these highly specialized areas is one of the hallmarks of the IEDM conference," he added. "The IEDM Tutorials and Short Courses represent a great opportunity to explore evolving areas of the field, with topics that include novel materials and device types; advances in process and packaging technologies; new design approaches; and much more," said Srabanti Chowdhury.

Except for the Tutorials and Short Courses, the Conference technical program included plenary and regular talks, the evening panel, focus sessions, a supplier exhibit, IEEE EDS award presentations and other events highlighting leading work in more areas of the field than any other conference. The events of the 67th IEDM are briefly reported below.

Tutorials

The five-day Conference program started on 11 December 2021 with six tutorials. The 90-minute Saturday tutorial sessions on emerging technologies have become a popular and growing part of the IEEE IEDM. They are presented by experts in the field to bridge the gap between textbook-level knowledge and leading-edge current research, and to introduce attendees to new fields of interest. The following tutorials were held during the time-frame of the 67th IEDM:

- *Beyond the FinFET Era: Challenges and Opportunities for CMOS Technology*; Kai Zhao (IBM) presented some of the recent advancements in nanosheet technology which make it the best candidate beyond FinFETs. K. Zhao reviewed the latest research directions for device architectural options beyond nanosheet and the corresponding challenges and opportunities.
- *TCAD-Based DTCO and STCO*; Asen Asenov (Glasgow University) introduced the key concepts of Design-Technology Co-Optimization (DTCO) and System-Technology Co-Optimization (STCO) and the corresponding DTCO/STCO tools and flows originally developed by Gold Standard Simulations (GSS) and now marketed by Synopsys after the acquisition of GSS in 2016. The concepts were illustrated with examples including both FinFET and PDSOI technologies. A. Asenov described how the DTCO and STCO can be used to make critical decisions regarding future technology generations.
- *6G Technology Challenges from Devices to Wireless Systems*; Aarno Pärssinen (Oulu University) addressed many aspects of implementation of radio systems for anticipated 6G requirements. Principles of wireless communications systems were analyzed against link capacity and range. The challenges of RF transceivers with regard to circuit and device aspects were explored. A. Pärssinen provided insight into the challenges of present and future technologies at different hierarchies and considered the trade-offs of next-generation communication.
- *Selective and Atomic-Scale Processes for Advanced Semiconductor Manufacturing*; Robert Clark (Tokyo Electron) reviewed the post-Dennard-style trends in device scaling. He outlined forces driving 3D integration and the effect of these changes on manufacturing technologies. Multi-patterning and atomic scale processes (ALD, ALS) used for 10nm and beyond manufacturing were introduced. Selective processing including ASD was explained. This emerging technology enables new device nodes and integration schemes. Finally, a view of how IC manufacturing will continue to evolve through 3D monolithic and heterogeneous integration was presented.
- *Machine Learning for Semiconductor Device and Circuit Modeling*; Elyse Rosenbaum (University of Illinois, Urbana-Champaign) focused on Machine Learning (ML) models that are especially suitable for device and circuit modeling. She reviewed prior works that applied ML to parameter extraction, TCAD, device modeling or circuit modeling.
- *GaN Power Device Technology and Reliability*; Dong Seup Lee

(Texas Instruments) introduced a broad overview of GaN power device technology. Basics of GaN, including polarization, device structure, and fabrication process were covered. Various reliability were reviewed, starting from intrinsic device level to real applications. The tutorial concluded with a discussion of the recent progress and future of GaN technology.

Short Courses

The IEDM program was continued with two short courses held on Sunday, 12 December 2021. In contrast to the tutorials, the full-day short courses are focused on a single technical topic. They offer the opportunity to learn about important areas and developments, and to network with global experts. The following two short courses were held during the time-frame of the 67th IEDM:

- **Future Scaling and Integration Technology,** organized by Dechao Guo (IBM Research) with the following presentations:
  - *Processes and Materials Engineering Innovations for Advanced Logic Transistor Scaling*; Benjamin Colombeau (Applied Materials) discussed process technology and materials engineering approaches used to extend FinFET scaling more specifically for critical FEOL modules (channel, junction, gate and contact). He discussed benefits and challenges of GAA Nanosheet architecture for the forthcoming generation of advanced CMOS. He also highlighted how novel co-optimized processes and materials innovations play a critical role to address integration and device performance challenges.
  - *Interconnect Resistivity: New Materials*; Daniel Gall (Rensselaer Polytechnic Institute) presented recent research results focusing on new materials for high-conductivity narrow interconnects that outperform Cu. The speaker discussed metals with a small mean free path of electrons to render their scattering at surfaces and grain boundaries negligible, 2D materials as new liner/barrier layers which maximize the conductor cross-sectional area and facilitate specular surface scattering, and topological metals with protected surface states that suppress electron scattering.
  - *Metrology and Material Characterization for the Era of 3D Logic and Memory*; Roy Koret (Nova Ltd.) presented metrology platforms that have matured during the 2D integration era. The course covered among other topics, a use of Critical Dimension Scanning Electron Microscopy (CDSEM), Transmission Electron Microscopy (TEM), X-ray Photoelectron Spectroscopy (XPS), X-ray Fluorescence (XRF), Atomic Force Microscopy (AFM), Optical Scatterometry (OCD), and a use of hybrid approach and Machine Learning in high volume manufacturing.
  - *Beyond FinFET Devices: GAA, CFET, 2D Material FET*; Chung-Hsun Lin (Intel) presented the status of Beyond FinFET solutions, their engineering opportunities and challenges for high volume manufacturing. He discussed GAA transistors, complementary FETs (CFETs), and atomic channel FETs with 2D materials. The GAA transistor is the most pragmatic architecture in the near term to enable incremental Contacted Poly Pitch and gate length scaling. CFET enables additional cell area scaling and heterogeneous integration for high mobility channel enablement. 2D material FET provides the ultimate gate length scaling with high mobility channel capability.
  - *Heterogenous Integration Using Chiplets & Advanced Packaging*; Madhavan Swaminathan (Georgia Tech) addressed among others advanced packaging platforms available for 2.5D and 3D integration, technologies available today and emerging ones, and an effect of the heterogeneity on signal integrity and power delivery. The presenter compared the technologies along with details on construction, line dimensions, form factor, bandwidth density, data rate, power delivery metrics, thermal management solutions, and system integration potential. Details on emerging technologies such as glass interposer were also presented.
  - *Design-Technology Co-Optimization/System-Technology Co-Optimization*; Victor Moroz (Synopsys) discussed DTCO and STCO methodologies applied to advanced CMOS logic and SRAM to explore and quantify different innovations in design and technology. The DTCO analysis was applied to (i) CMOS operating at cryogenic temperatures and (ii) the role of transistor variability as the driving force behind industry transitions from planar MOSFET to FinFET to GAA technologies. The STCO analysis was applied to 3D heterogeneous integration requiring resolving interrelated electrical, thermal, stress, and power delivery challenges.
- **Emerging Technologies for Low-Power Edge Computing,** organized by Huaqiang Wu (Tsinghua University) and John Paul Strachan, (Forschungszentrum Jülich) with presentations:
  - *Mobile NPUs for Intelligent Human/Computer Interaction*;

Hoi-Jun Yoo (KAIST) made a review of the status of AI and Deep Neural Network (DNN) SoCs from the viewpoint of mobile and edge AIs. The optimization methods for mobile DNN accelerators which target low power consumption and high performance, were explained at both hardware-level and software-level. Moreover, he introduced 6 lessons learned from over 10 years of NPU design experiences. These lessons explained the advantages and trade-offs of the state-of-the-art techniques for not only inference processors but also mobile training processors. He showed the past, current, and future of the mobile NPU designs with the lessons and examples of implemented chips for various human-computer-interaction (HCI) applications such as emotion recognition, object tracking, GAN, DRL, and others.

- *Brain-Inspired Strategies for Optimizing the Design of Neuromorphic Sensory-Processing Systems*; Giacomo Indiveri (University of Zurich) presented neuromorphic electronic circuits that directly emulate the physics of computation used by biological neural processing systems, and brain-inspired signal processing strategies to build beyond von Neumann ultra-low power computing technologies for real-world sensory-processing edge-computing applications.
- *Memory-Based AI & Data Analytics Solutions*; Euicheol Lim (SK Hynix) showed in his talk the demand of near data processing. With solution examples the speaker explained what architecture for near data processing is feasible. The analog computing in memory that processes data and processing in analog cell arrays were introduced as extreme examples of near data processing.
- *Material Strategies for Memristor-Based AI Hardware and their Heterointegration*; Jeehwan Kim (MIT) presented a material strategy to precisely confine the conducting paths in memristors. It allows the operation of 1R-based crossbar arrays with great programmability. By embedding such a crossbar array into the edge of a heterogeneously integrated chip, reconfigurable heterochips with stackability were demonstrated. They featured (i) memristor crossbar arrays for non-von Neumann computing and (ii) optical communication between chips via integrated LEDs and photodiodes. An outlook of some recent reconfigurable heterogeneous integration schemes for future electronics was made.
- *RRAM Devices for Data Storage and In-Memory Computing*; Wei Lu (University of Michigan) discussed in-memory computing (IMC) systems based on an emerging device —resistive-random access memory (RRAM). Approaches towards a scalable IMC system were introduced to address device nonidealities and accommodate practical AI models.
- *Practical Implementation of Wireless Power Transfer*; Hubregt Visser (Imec) discussed different building blocks of a receiver for ultra-low power level long-distance wireless power transfer (WPT) i.e., antenna, rectifier, boost converter and load. For this, the design steps of a couple of practical, remotely powered applications like an electric clock, a temperature sensor with display and a wireless temperature and humidity sensor were presented.

Plenary Session

The first point of the IEDM program on Monday, 13 December 2021 was a plenary session. Three plenary talks were delivered, namely:

- *The Smallest Engine Transforming Our Future: Our Journey Into Eternity Has Only Begun* by Kinam Kim, Vice Chairman & CEO, Samsung Electronics Device Solutions Division,
- *Creating the Future: Augmented Reality, the Next Human-Machine Interface* by Michael Abrash, Chief Scientist, Facebook Reality Labs,
- *Quantum Computing Technology* by Heike Riel, Head of Science & Technology, IBM Research and IBM Fellow.

The plenary session was followed by a number of regular sessions, focus sessions, an Evening Panel and a Career Luncheon. The most newsworthy sessions and papers are briefly presented below.

Focus Sessions

Five Focus Sessions on key emerging technologies covered a range of topics addressing the gaps, challenges and opportunities for new approaches and technologies, including system-level issues and requirements; benchmarks of current technologies; and R&D directions for the new materials, devices, circuits, and modeling/manufacturing/testing approaches needed:

- Focus Session on Advanced Logic Technology—**Stacking of Devices, Circuits, Chips: Design, Fabrication and Metrology Challenges and Opportunities** (Session #3, 13 December 2021)

3D stacking from the device to the package level is a growing trend that will enable the industry to move to larger, more densely integrated circuits and systems. It will benefit greatly from the ability to integrate

heterogeneous technologies into one solution (e.g., CFETs, quantum technologies etc.), along with new approaches to inspection and metrology. These issues were addressed in the following talks:

- *CFET Design Options, Challenges, and Opportunities for 3D Integration*, L. Liebmann, TEL Technology Center America
- *3D Sequential Integration: Applications and Associated Key Enabling Modules (Design & Technology)*, P. Batude et al, CEA-Leti/STMicroelectronics/SOITEC/Universite Grenoble Alpes/Universite Savoie Mont Blanc
- *Inspection and Metrology Challenges for 3nm Node Devices and Beyond*, T. Shohjoh et al, Hitachi/Imec
- *Heterogeneous Integration Enabled by State-of-the-Art 3DIC and CMOS Technologies: Design, Cost, and Modeling*, X.-W. Lin et al, Synopsys/IC Knowledge
- *Design for 3D Stacked Circuits*, P. Franzon et al, North Carolina State University
- *3D SoC Integration, Beyond 2.5D Chiplets*, E. Beyne et al, Imec
- *Foundry Perspectives on 2.5D/3D Integration and Roadmap*, Douglas C. H. Yu et al, TSMC

- Focus Session on Emerging Device and Compute Technology—**Device Technology for Quantum Computing** (Session #14, 14 December 2021)

This Session explored R&D directions concerning new materials, devices, circuits, manufacturing and packaging approaches for Quantum Computing. The following talks concerning these topics were delivered:

- *Si MOS and Si/SiGe Quantum Well Spin Qubit Platforms for Scalable Quantum Computing*, R. Pillarisetty et al, Intel/TU Delft
- *Material and Integration Challenges for Large-Scale Si Quantum Computing*, M. Vinet et al, CEA-Leti/ CNRS Neel Institute/CEA IRIG/Universite Grenoble Alpes
- *High-Fidelity Two and Three Spin Operations in Si with Triple Quantum Dots*, S. Tarucha, RIKEN Center for Quantum Computing
- *Silicon-Based Quantum Computing: High-Density, High-Temperature Qubits*, A. Dzurak, University of New South Wales
- *3D Integration Technology for Quantum Computer Based on Diamond Spin Qubits*, R. Ishihara et al, Delft University/Fujitsu
- *Quantum Photonics with SnV Centers in Diamond*, S. Aghaeimeibodi et al, Stanford University
- *Packaging and Integration Challenges in a Superconducting-Qubit-Based Quantum Computer*, M. Giustina, Google

- Focus Session on Memory Technology/Advanced Logic Technology—**STCO for Memory-Centric Computing and 3D Integration** (Session #25, 15 December 2021)

As integrated circuits became more powerful and offered more functionality, the line started to blur between where a device ended and where a circuit began. A need was seen to design devices and circuits synergistically, a move called design-technology co-optimization (DTCO). Now, taking the idea of synergistic design a step further, system-technology co-optimization (STCO) is a growing trend. The approach encompasses leading-edge 3D concepts and heterogeneous technologies, and it is essential to enable new ways of computing, and to optimize the performance of new computing systems. One example is computing-in-memory (CIM) for artificial intelligence (AI)-based applications. Where and how data is stored in a CIM architecture is critical to its performance. The presentations below were about these matters:

- *Human-Centric Computing*, J. M. Rabaey, University of California at Berkeley/Imec
- *In-Memory Computing with Associative Memories: A Cross-Layer Perspective*, X. Sharon Hu et al, University of Notre Dame/Rochester institute of Technology/Zhejiang University
- *Monolithic 3D Compute-in-Memory Accelerator with BEOL Transistor-Based Reconfigurable Interconnect*, Y. Luo, Georgia Institute of Technology/University of Notre Dame
- *The Future of Hardware Technologies for Computing: N3XT 3D MOSAIC, Illusion Scaleup, Co-Design*, R.M. Radway et al, Stanford University/Facebook
- *Enabling RRAM-Based Brain-Inspired Computation by Co-Design of Device, Circuit, and System*, C. Dou et al, Chinese Academy of Sciences/Fudan University
- *Co-Design In High-Performance Computing Systems*, J. Moreno et al, IBM
- *Mm-Wave Automotive Radar: From Evolution to Revolution*, K. Doris, NXP Semiconductors

- Focus Session on Sensors, MEMS, and Bioelectronics/Optoelectronics, Displays, and Imaging Systems—**Technologies for AR/VR and Intelligent Sensors** (Session #35, 15 December 2021)

AI and new architectures make possible new types of sensors for a growing number of use cases. They were discussed in the talks listed below:

- *Integrating Taste Technology with Audiovisual Media*, H. Miyashita, Meiji University
- *A Miniature Electronic Nose for Breath Analysis*, Z. Li et al, National Tsing Hua University/Taiwan Semiconductor Research Institute/ITRI/Enosim Bio-tech

- *Computational Imaging with Vision Sensors Embedding In-Pixel Processing*, J.N.P. Martel et al, Stanford
- *AI SoCs for AR/VR User-Interaction*, J. Ryu et al, KAIST
- *AR Glasses: Fatigue-Free Optical Engines and Energy-Efficient SLAM Sensors*, H.-S. Lee et al, Samsung

- Focus Session on Emerging Device and Compute Technology/ Optoelectronics, Displays, and Imaging Systems—**Topological Materials, Devices and Systems** (Session #38, 15 December 2021)

Topological materials, where the surface is conducting but the bulk portion of the material is an insulator, are being investigated for their potential to enable ultra-small devices. This very promising theme was discussed in:

- *Spin-Charge Interconversion in Topological Insulators and Topological Semimetals for Spin-Orbit Torque Devices*, N. Samarth et al, Pennsylvania State University
- *Proposal for a Negative Capacitance Topological Quantum Field-Effect Transistor*, M.S. Fuhrer et al, ARC Centre of Excellence in Future Low-Energy Electronics Technologies/Monash University/University of New South Wales/ University of Wollongong/RMIT University
- *Essential Design Criteria for Topological Electronics and Spintronics*, G. J. de Coster et al, Army Research Laboratory/ University of Illinois at Urbana-Champaign
- *Topological Semimetals for Electronic Devices*, A. Rashidi, et al, University of California at Santa Barbara
- *Semiconductor Topological Nanophotonics*, Y. Ota et al, Keio University/University of Tokyo
- *Symmetry-Enabled New Microlasers*, L. Feng et al, University of Pennsylvania

Regular Sessions

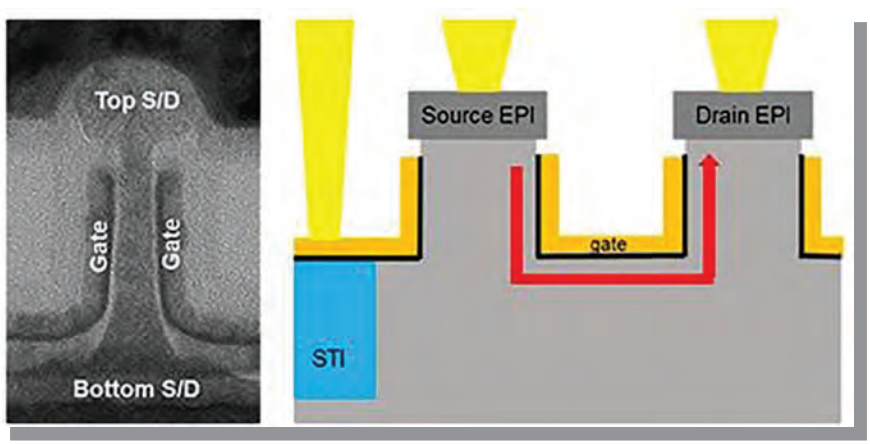
Among the papers presented during the regular sessions held from 13–15 December, a few general tracks may be distinguished. These tracks are briefly characterized below. Noteworthy papers are briefly presented.

A. CMOS Technology: New Ways to Advance Moore's Law

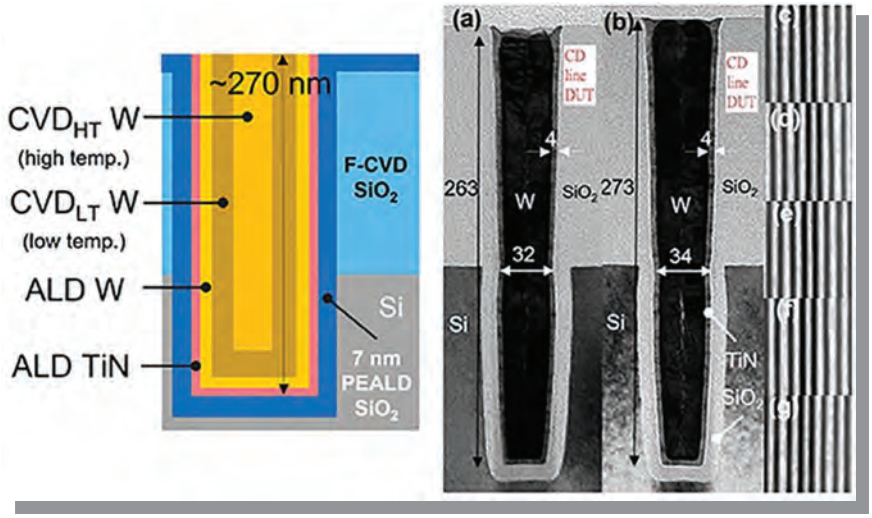
3D at the Device Level: CMOS transistors are built in a lateral, or horizontal, fashion, and countless advances over decades have shrunk their dimensions so that billions of them can now be put on a chip, in accordance with the predictions of Moore's Law. But shrinking transistors further in order to boost chip performance and add new features is difficult and costly. Would orienting them vertically instead of horizontally save space and make it easier to extend the life of Moore's Law?

Inspired by trench-based DRAM vertical access transistors, a team from IBM and Samsung described in Paper #26.1, how they turned transistor architecture on its side, with CMOS devices built using so-called Vertical-Transport Nanosheets (VTFETs) on bulk silicon and with a 45nm gate pitch. The vertical devices offer the opportunity for continued scaling because gate length and spacer size—two key elements which determine gate pitch (the distance between transistors)—can be optimized in ways that aren't possible horizontally. Also, the VTFET devices promise to deliver outstanding operating voltage and drive current as a result of reduced electrostatic and parasitic losses (SS = 69/68 mV/dec and DIBL= <30 mV). To validate the concept, the researchers used the VTFETs to make functional ring oscillators (test circuits), which demonstrated ~50% reduction in capacitance vs. a lateral design reference.

Exploring Buried Power Rails: Interconnect is the term for the layers of wiring which connect everything on a chip. There are many interconnect layers in today's most advanced chips, resulting in many interconnections which take up space and introduce undesirable electrical effects like resistance and capacitance. One possible way to continue scaling is to reconfigure the interconnect so that it takes up less space. In current designs, the top interconnect layer is what routes power to a chips' transistors. If this "power rail" could be built closer to them—in the substrate right beneath them—then the interconnect stack could be reduced in height, the number of interconnections could be reduced, and smaller chip architectures would result. But it isn't clear which metals a buried power rail



Paper #26.1, "Vertical-Transport Nanosheet Technology for CMOS Scaling beyond Lateral-Transport Devices," *H. Jagannathan et al, IBM/Samsung: left - a cross-sectional TEM of a VTFET nanosheet transistor (the source can be located at either the top or bottom for design flexibility), right - a schematic of an I/O device FET co-integrated with the VTFET*

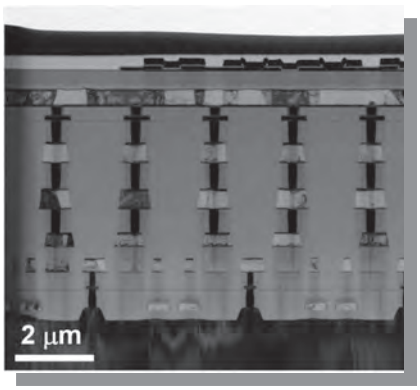


Paper #22.5, "Buried Power Rail Metal Exploration Towards the 1nm Node," *A. Gupta et al, Imec/ASM International: left—illustration of the tungsten (W) metallization stack (with a TiN liner used as an adhesion layer); right—the TEMs across the BPR line in (a) and (b) show the stack for on different wafers, and (c–g) shows void-free fill of lines for five different wafers*

(BPR) should be made from in order to address electrical performance, and for manufacturability. In Paper #22.5, a team from Imec and ASM International discussed their experiments evaluating different metals both for the BPR itself and also for the low-resistance contacts needed between the BPR and the through-silicon-vias that run through a chip's different layers. They said that for future 3 nm transistors, a tungsten BPR optimizes line and contact resistance, and for 1 nm and 2 nm devices, molybdenum (Mo) appears better for the BPR and ruthenium (Ru) for the via contacts.

2D Materials Compatible With 300mm Production: Transition metal dichalcogenides (TMDs) are 2D materials with semiconducting properties. They are promising for use as the channel in highly scaled devices because they are <1 nm thick. However, much work is needed to understand the electron mobilities of various TMDs, the electrical resistance which metallic contacts impose on them, and other key aspects. In Paper #7.1 "Advancing 2D Monolayer CMOS Through Contact, Channel and Interface Engineering," K.P. O'Brien/C. J. Dorow et al, Intel, the researchers reported fabrication and extensive studies of four TMD films: MoS_2, WS_2, WSe_2 and $MoSe_2$. The films demonstrated impressive performance, but most noteworthy is that all were grown at the 300mm scale in BEOL-type environments at process temperatures from 300 °C to 1,000 °C, meaning they are compatible with current mass-production methods.

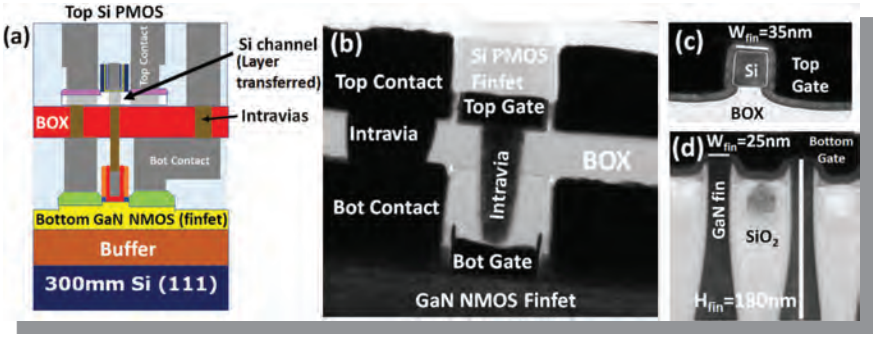
Monolithic 3D Logic/Memory Integration for Machine Learning: As scaling becomes more difficult and expensive, the monolithic 3D integration of logic and memory is increasingly seen as a way to increase integration density, enrich the functionality and boost the performance of a single chip. A team of researchers from Tsinghua University and the Chinese Academy of Sciences described in Paper #21.5 their works on building a monolithic 3D device that combines 1) silicon CMOS logic; 2) a $HfAlO_x$ resistive-RAM (RRAM)-based computing-in-memory (CIM) layer; and 3) a complex ternary content-addressable memory (TCAM) layer. The device is intended for one-shot learning, which is a training technique for machine-learning applications. In one-shot tests using a standard data set, the device demonstrated a GPU-equivalent accuracy of up to 97.8% but with far lower energy consumption.



Paper #21.5, "Monolithic 3D Integration of Logic, Memory and Computing-In-Memory for One-Shot Learning," *Y. Li et al, Tsinghua University/Chinese Academy of Sciences: a cross-sectional TEM image of the 3D integrated chip*

GaN Meets Moore's Law: Gallium nitride (GaN) is a promising material for RF/mmWave and power applications, given its ability to operate at higher voltages and frequencies than silicon, and with lower losses. If GaN technology could be integrated effectively with CMOS technology and built using mainstream silicon CMOS tools and fabrication processes, then high-performance, energy-efficient and low-cost solutions could be created for next-generation PC/mobile devices, data centers, automotive radar, communication networks and other applications.

Intel researchers described in Paper #11.1 a highly scaled, high-performance, enhancement-mode high-k GaN-on-Si NMOS FinFET built on a 300 mm Si platform and integrated with Si PMOS FinFET technology. The heterogeneous device was made possible by a layer-transfer technique Intel first described at the 2019 IEEE IEDM that enables GaN NMOS and Si PMOS devices to be fabricated in parallel. The NMOS GaN FinFET features the narrowest GaN fin to date (width = 25 nm), an ultra-short gate length (30 nm), and is integrated with a Si PMOS FinFET having a fin width = 35 nm. The device achieved many industry firsts and records for GaN-on-Si, including a record f_T/f_{MAX} of 300/400 GHz and record transconductance (GM>2100



*Paper #11.1, "*Advanced Scaling of Enhancement-Mode High-K Gallium Nitride-on-300 mm-Si(111) Transistor and 3D Layer Transfer GaN-Silicon FinFET CMOS Integration,*" H.W. Then et al, Intel: (a) a schematic of the 3D-stacked GaN-Si CMOS inverter; TEMs: (b) of the fabricated 3D layer-transfer stacked inverter, comprising a bottom GaN E-mode high-k NMOS FinFET transistor and a top Si PMOS FinFET transistor; (c) of the 35 nm-wide Si fin as the top PMOS channel; (d) of the 25nm-wide GaN fin as the bottom NMOS channel—this is the narrowest GaN fin with the highest aspect ratio (Hf_{in}/Wf_{in} = 7) ever demonstrated in literature*

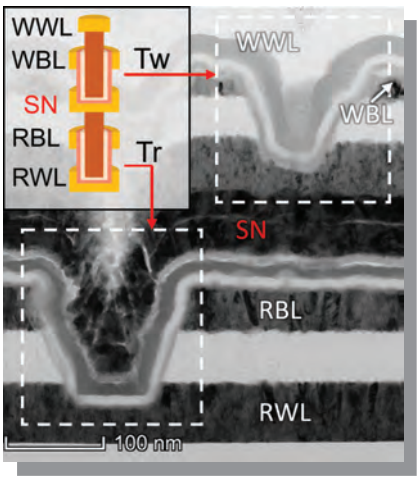
μS/μm) with the industry's thinnest T_{OXE} (14.8Å), among others. It is the first true enhancement-mode (i.e., "normally off") GaN transistor with I_{OFF} <25 pA/μm (up to V_D = 30 V). The researchers demonstrated the technology by building a low-loss inverter with it. They said that going forward, GaN FinFET architectures and 3D layer-transfer technologies will play a significant role in GaN device scaling and in the ability to integrate more functionalities like CMOS with GaN technology.

B. Memory Technology

Significant Improvements in DRAM Reliability: Samsung researchers presented in the comprehensive Paper #6.6, "*Reliability Characterization for Advanced DRAM using HK/MG + EUV Process Technology*," S. Lee et al, Samsung, demonstrating dramatic improvements in DRAM reliability at the 17 nm-to-15 nm technology nodes vs. the 18 nm node. This was achieved by transitioning to EUV for critical layers instead of using ArF immersion lithography; adopting HK/MG process technology for DRAM; and optimizing the gate dielectric breakdown of the buried access transistor (BCAT). A direct comparison of the breakdown voltage (V_{bd}) of test structures with EUV vs. immersion ArF demonstrated a clear improvement in low failure fractions for shorting nearest metal lines of the cell transistor, and a significant improvement in M0-to-metal contact process margin. High Temperature Operation Life (HTOL) testing exhibited a 2.2x reduction in failure rates for the 17 nm and 15 nm nodes. In order to confirm the success of their reliability improvements, the researchers tracked hundreds of thousands of DIMMs over one year of use, yielding a low cumulative failure of ~100 ppm, a value consistent with their accelerated tests.

FeRAM with Record Performance for Embedded Memory: Hafnium-based ferroelectric RAM (FeRAM) stores memory bits in FE or AFE (antiferroelectric) capacitors by polarizing them electrically, versus storing bits in traditional capacitors as electrical charge, as DRAM memory does. FeRAM technology is promising as an embedded memory technology because it is highly scalable, high-speed, low-voltage and CMOS-compatible, and doesn't require the use of low-leakage transistors as DRAM-based embedded memory does. Intel researchers described in Paper #33.2 how they built FeRAM with deep-trench AFE capacitors that showed industry-leading performance (read/write speed of ~2 ns) and reliability (endurance >10^{12} cycles), with high levels of uniformity at the 300 mm wafer scale.

A Path to Ultra-High Density DRAM: As scaling of traditional DRAM memory is increasingly challenged, new alternatives are being sought. A team from the Chinese Academy of Sciences and Huawei described in Paper #10.5 novel vertical channel-all-around IGZO FETs with the potential to move beyond the



*Paper #10.5, "*Novel Vertical Channel-All-Around(CAA) IGZO FETs for 2T0C DRAM with High Density beyond $4F^2$ by Monolithic Stacking,*" X, Duan/K. Huang et al, Chinese Academy of Sciences/Huawei: a TEM image of the vertically stacked $4F^2$ 2T0C bit cell; the inset shows a schematic of the proposed $4F^2$ 2T0C bit-cell, vertically connected to a read transistor's gate*

	Material	Structure	Speed (ns)	Voltage (V)	Size (μm^2)	Variation	Endurance
This work	AFE HZO	3D	2	-1.6/1.2	0.008	4σ	10^{12} at 85C
Ref. [7]	FE HZO	Planar	30	-4/4	0.1	No data	10^{11} at RT
Ref. [8]	FE HZO	Planar	14	-2.5/2.5	1	6σ	10^{9} at RT

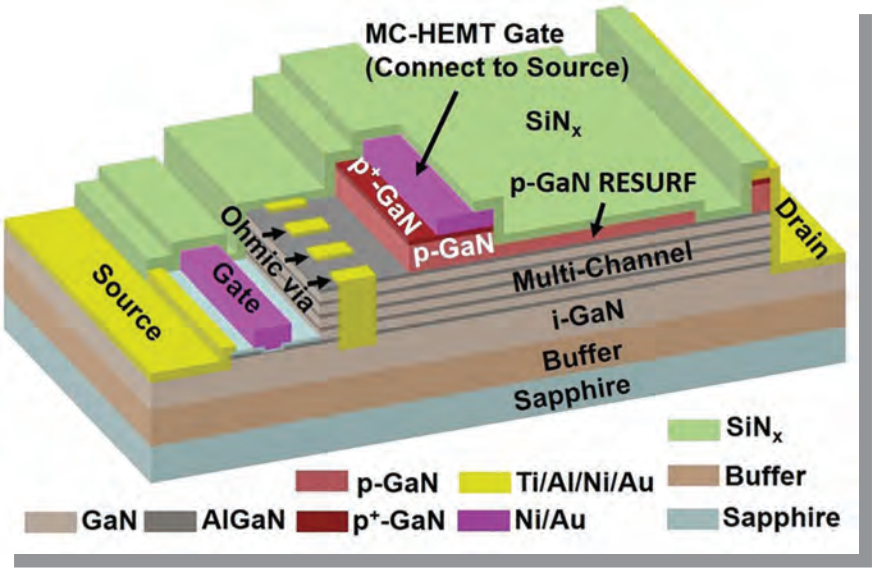
*Paper #33.2, "*FeRAM using Anti-ferroelectric Capacitors for High-speed and High-density Embedded Memory,*" S. -C. Chang et al, Intel: a table benchmarking the FeRAM described in this paper with results previously reported for FeRAM devices with FE capacitors; it shows that FeRAM with scaled AFE HZO capacitors enables faster read/write operations with a lower voltage swing*

traditional 4F² DRAM memory cell size limit. The 4F² 2T0C bit-cell device (2 transistors, no capacitors—charge is stored in the gate) has a gate electrode surrounded by a gate insulator and an IGZO channel. Its source/drain electrodes are vertically separated by an insulator layer, forming a metal/insulator/metal structure. The device demonstrated low off-current (~1.8×10^{-17} A/μm) and long retention times (300s). The possibility to stack multiple bit cells monolithically suggests it could become a higher-density alternative to conventional 1T1C DRAM.

C. Power Devices

Toward a Better Understanding of SiC: Progress in silicon-carbide (SiC) material and device technologies has enabled mass production of 600–3,300 V SiC power MOSFETs and Schottky barrier diodes, which have led to substantial energy savings in various electric systems such as power supplies, photovoltaic inverters, air conditioners, electric vehicles, and railcars. Despite this progress, our basic understanding of the material properties and device physics of SiC is still somewhat lacking, making it difficult to develop guiding principles for designing SiC power devices. Also, the oxide/SiC interface remains extremely defect-rich, limiting the performance and reliability of SiC power MOSFETs. Researchers from Kyoto and Osaka Universities described in Paper #36.1 "*Physics and Innovative Technologies in SiC Power Devices*," T. Kimoto et al, Kyoto University/Osaka University, several new insights and understandings in SiC power semiconductor technology, and presented a way to improve the SiC MOS interface for higher electron mobility through the use of a new process for gate-oxide formation.

GaN at Up to 10 kV: A Virginia Tech-led team described in Paper #5.5, a new power device concept they call a Multi-Channel Monolithic-Cascode high-electron-mobility transistor (MC²-HEMT). Made from AlGaN/GaN, the device monolithically integrates a low-voltage, enhancement-mode HEMT based on a single two-dimensional electron-gas (2DEG) channel, with a high-voltage, depletion-mode HEMT based on a stacked 2DEG multi-channel. It operates at a 10 kV breakdown voltage and has a specific on-resistance ~2.5x smaller than SiC's.



Paper #5.5, "Multi-Channel Monolithic-Cascode HEMT (MC2-HEMT): A New GaN Power Switch up to 10 kV," *M. Xiao et al, Virginia Polytechnic Institute/University of Southern California/Cambridge University/Enkris Semiconductors/Qorvo: a 3-D schematic of the AlGaN/GaN MC2-HEMT fabricated in this work. The SiNx passivation layer is partially removed to show the internal structure*

D. Advances in Imaging

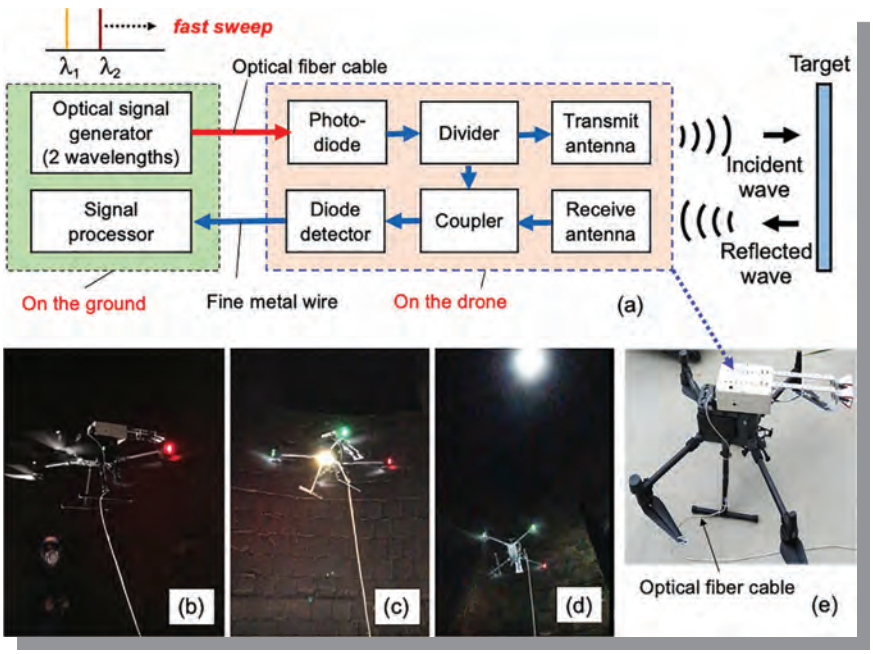
Record Quantum Efficiency for NIR/SWIR Sensors: In Paper #23.4, STMicroelectronics researchers reported a 1.62 μm pixel-pitch global shutter sensor for imaging in the near-infrared (NIR) and shortwave infrared (SWIR) regions of the light spectrum. The sensor demonstrated record optical performance: an unprecedented quantum efficiency of >50% and a shutter efficiency of >99.94%. The breakthrough was made possible by use of a novel colloidal PbS quantum dot thin-film technology. The devices were fabricated on a 300 mm manufacturing toolset.

Paper #23.4, "1.62µm Global Shutter Quantum Dot Image Sensor Optimized for Near and Shortwave Infrared," *J.S. Steckel et al, STMicroelectronics: an outdoor image taken with the 940 nm NIR QF sensor (left) and with a high-end smartphone camera (right). The NIR image shows a significant difference in contrast, and the ability to clearly identify the black electrical wires hidden in the tree leaves, vs. the visible light image*

3D Backside-Illuminated SPAD Imager Sensors: Unlike the CMOS image sensors found in smartphones, which measure the amount of light reaching a sensor's pixels in a given timeframe, single photon avalanche diode (SPAD) image sensors detect each photon that reaches the pixel. Each photon is converted into an electric charge, and the electrons that result are eventually multiplied in avalanche fashion until they form an output signal. SPAD image sensors hold great promise for high-performance, low-light imaging applications, for depth sensing, and for fully digital system architectures. However, until now their performance has been limited by tradeoffs in pixel detection efficiency vs. pixel size, and by poor signal-to-noise ratios. Recently a charge-focusing approach was proposed to overcome these issues, but until now it has not been implemented. In late-news Paper #20.2, "*3.2 Megapixel 3D-Stacked Charge Focusing SPAD for Low-Light Imaging and Depth Sensing*," K. Morimoto/J. Iwata et al, Canon, the researchers discussed how they did so, with the industry's first 3D-stacked backside-illuminated (BSI) charge-focusing SPADs. The devices featured the largest array size ever reported for a SPAD image sensor (3.2 megapixels) and demonstrated a photon detection efficiency of 24.4%, and timing jitter below 100ps at 940 nm.

E. High-Frequency Electronics

Photonics Gives a Boost to mmW and THz Electronics: In coming years high-frequency electronics will be in the spotlight, as applications like 5G/6G communications strive to make use of ever-higher frequency bands (>100 GHz), and as fiber-optic and radio networks converge, making possible technologies like integrated radar/digital communications systems operating at 200–300 GHz. With an eye toward this future, researchers from Osaka University described in Paper #11.5 how they efficiently combined digital electronics with telecom-based photonic techniques for the generation/detection of millimeter-wave (mmW) and terahertz (THz) waves, to boost overall system performance. They conducted three different demonstrations to validate their approach: 1) a 15 Gb/s wireless link with optical fiber input @ 600 GHz; 2) real-time transmission of uncompressed 8-K UHD video at 48 Gb/s; and 3) a drone-mounted broadband mmW radar operating at 4 GHz–40 GHz.

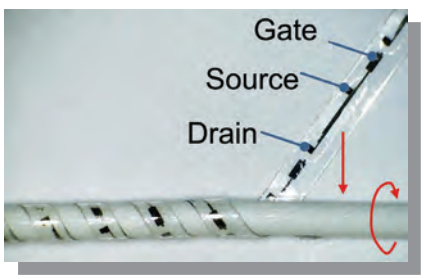


Paper #11.5, "Enabling Device Technologies for Photonics-Assisted Millimeter and Terahertz Wave Applications," *T. Nagatsuma et al, Osaka Univ.: (a) A block diagram of the ultra-broadband mmW radar mounted on a drone, (b-d) Photos of the drone flying in a chimney to inspect a wall, (e) Photo of the mmW radar mounted on a drone*

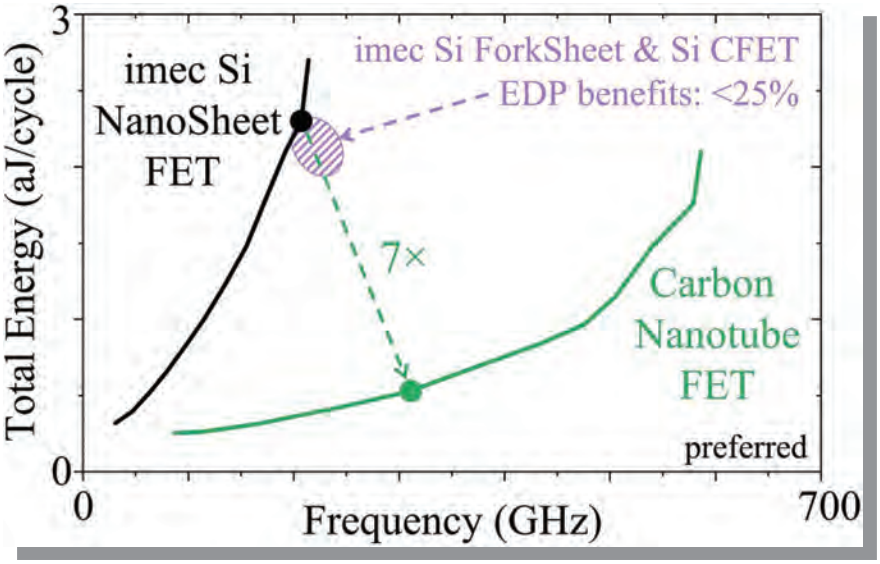
F. Noteworthy Papers on Diverse Topics

A Stretchable Amplifier for Smart Textiles: A research team from Tsinghua University/Chinese Academy of Sciences/Cambridge University will described in Paper #16.4 stretchable all-inkjet-printed organic thin-film transistors and in-situ amplification circuits integrated in a strip-helix architecture. The organic devices are fabricated on plastic strips that are fashioned into a helix, which is then coiled around a stretchable fiber to be weaved or knitted into smart textiles. The helix-fiber design outperforms current state-of-the-art intrinsically stretchable devices, with ultralow power consumption of 681 pW, high subthreshold transconductance efficiency, and a high voltage gain of 214 V/V. The transistors and amplifier circuits demonstrated no significant changes in electrical performance up to a 50% extrinsic stretch.

Tailoring Ferroelectric Properties for Logic & Memory: Ferroelectric hafnium oxide, or hafnia, films are promising for advanced logic and memory devices because they are ultra-scalable, robust, CMOS-compatible and enable low-power designs. Their ferroelectric (FE) performance



Paper #16.4, "High Stretchability Ultralow-Power All-Printed Thin-Film Transistor Amplifier on Strip-Helix-Fiber," *C. Jiang et al, Tsinghua University/Chinese Academy of Sciences/Cambridge University: a photo of the strip-helix-fiber OTFTs under coiling; red arrows indicate the directions that the strip and fiber move, respectively*



*Paper #27.3, "*Extended Scale Length Theory Targeting Low-Dimensional FETs for Carbon Nanotube FET Digital Logic Design-Technology Co-optimization,*" C. Gilardi et al, Stanford University/Imec: pareto curves for energy vs. frequency for 15-stage inverter-based ring oscillators used in DTCO explorations*

is dependent on their surface properties, and by modifying those properties (i.e., by functionalizing them) a film's performance may be tailored to a specific application. However, there isn't yet an atomic-level understanding of the relationship between a given surface functionalization and ferroelectric performance; most attempts to engineer FE performance by altering a hafnia film's surface characteristics have been laborious trial-and-error efforts. In Paper #15.1 "*Surface-Functionalized Hafnia with Bespoke Ferroelectric Properties for Memory and Logic Applications*," D.-H. Choe et al, Samsung, the researchers described the development of an automated algorithm for searching thermodynamically stable geometries of surface-functionalized FE H_fO_2. They used it to systematically investigate the surface functionalities of eight different hafnia crystal orientations, and how they impacted FE performance. They said, the technique is extendable to other oxide surfaces and functional groups, and will lead to precise control of hafnia's FE properties for use in future devices.

DTCO for Carbon Nanotube FETs: A Stanford/Imec team detailed in Paper #27.3 a design-technology co-optimization (DTCO) study on carbon nanotube FETs (CNFETs). At the device level, a new extended-scale-length theory that is crucial for low-dimensional FETs was developed, as well as a new CNFET leakage current compact model which includes inelastic band-to-band tunneling. Facilitated by these models, the team performed an in-depth DTCO analysis, which will enable CNFET technology to achieve a large energy delay product (EDP) benefit (a figure of merit for energy efficiency) versus advanced silicon technologies such as nano/forksheets and complementary FETs (CFETs) at the 2 nm node.

Luncheon—Tuesday, 14 December

Two eminent experts took part in the career-focused luncheon featuring industry and scientific leaders talking about their personal experiences in the context of career growth. The speakers were:

- Sophie Vandebroek, Founder & Owner, Strategic Vision Ventures LLC.

  Dr. Vandebroek is a seasoned executive with extensive C-level experience at IBM, Xerox and UTC, and has served on public and private company boards since 2008. She is an expert in the creation and application of technologies that drive growth, and in the governance of inclusive and innovative global organizations. Dr. Vandebroek was previously VP of Emerging Technology Partnerships for IBM; Chief Operating Officer of IBM Research; CTO and Corporate Vice President at Xerox; and Board Chair of Xerox PARC, among other noteworthy roles.
- Deji Akinwande, Temple Foundation Endowed Professor at the University of Texas at Austin.

  Dr. Akinwande invented 2D memory, also known as atomristors. He has been honored with the 2018 Fulbright Specialist Award, 2017 Bessel-Humboldt Research Award, the U.S Presidential PECASE award by President Obama, the inaugural Gordon Moore Inventor Fellow award, the inaugural IEEE Nano Geim and Novoselov Graphene Prize, the IEEE "Early Career Award" in Nanotechnology, the NSF CAREER award, and several DoD Young Investigator awards, among many others.

Evening Panel Session—Tuesday evening, 14 December

A staple of the IEEE IEDM conference is the evening panel session, an interactive forum where experts give their views on important industry topics, and audience participation is encouraged to foster an open and vigorous exchange of ideas. The title of this year's evening panel was "*Is Hardware/Software Co-Design a Necessary Evil or a Symbiotic Partnership?*" The panel was moderated by Myunghee Na, Semiconductor Technologist and VP of the Revolutionary Technology Center at SK hynix, it will explore the idea of what hardware/software co-design really means in terms of technology development and the introduction of new technology.

With this short report on the Evening Panel we conclude the wrap up of the 67th IEEE International Electron Devices Meeting.

2021 IEEE International Flexible Electronics Conference (IFETC-3)

The 2021 IEEE International Flexible Electronics Conference (IFETC-3) was held virtually on 9–12 August 2021, instead of downtown Columbus, Ohio. The meeting was intended as a hybrid format, but pivoted to fully virtual. IFETC-3 offered Sunday short courses, followed by 3-days of plenary & invited talks, interspersed amongst contributed talks. A minimal number of parallel sessions was used to maximize simulcast remote viewing. Recordings, including Q&A, were posted for registrants for 30-days following the meeting.

Figure 1. The 2021 IFETC conference committee represents a diverse group of international researchers, drawing new researchers into the IEEE EDS community

Figure 2. Medical wearables, advanced biosensors and printable manufacturing were prominently displayed within a slate of Plenary speakers, who represented well our potent WiE and young investigator communities

The IFETC-3's Technical Program covered a wide range of cutting-edge developments in printed and flexible electronics. IFETC, started in Ottawa, Canada (2018), focusing upon printed and flexible hybrid and non-hybrid materials, devices and systems. It will rotate between the Americas, Asia and Europe, heading to Qingdao, PRC in 2022. IFETC aims to bring together a wide variety of stakeholders, from chemists, materials scientists, physicists, to mechanical and electrical engineers, the fabrication and manufacturing communities, as well as end-users, e.g., packaging and medical communities. IFETC is where academia meets industry, and vice versa.

Just some key highlights included:

- Short Courses: Savas Kaya (*Ohio-Univ*) presented a compelling short course, "Flextronics: A Hard Barrier for Flexible Teaching?" offering compelling ways to teach flexible electronics, which is a highly diverse subject to a wide multidisciplinary audience
- Plenary: The future of medical wearables was prominent through Azar Alizadeh (*GE Research*), who presented "Manufacturing of Low-Cost Wearable Human Health Monitoring Devices" and Anna Claudia Arias (*Berkeley*), who presented "Flexible Arrays of Printed Devices and Their Use in Wearable Medical Devices."
- Invited: OLED and flexible solar cells were extended through talks by Paul W.M. Blom (*Max-Planck Institute for Polymer Research*) with "Towards Efficient and Stable Printed Single-Layer OLEDs" and Francesca Brunetti (*University of Rome Tor Vergata Via del Politecnico*) with "From Flexible Perovskite Solar Cells to Large Area Modules: Challenges and Perspectives." Flexible displays were advanced by Michael D. McCreary (*E Ink*), who presented "Recent Advances in Flexible Electrophoretic Display Technology Including Full Color Reflective Displays." And Karl

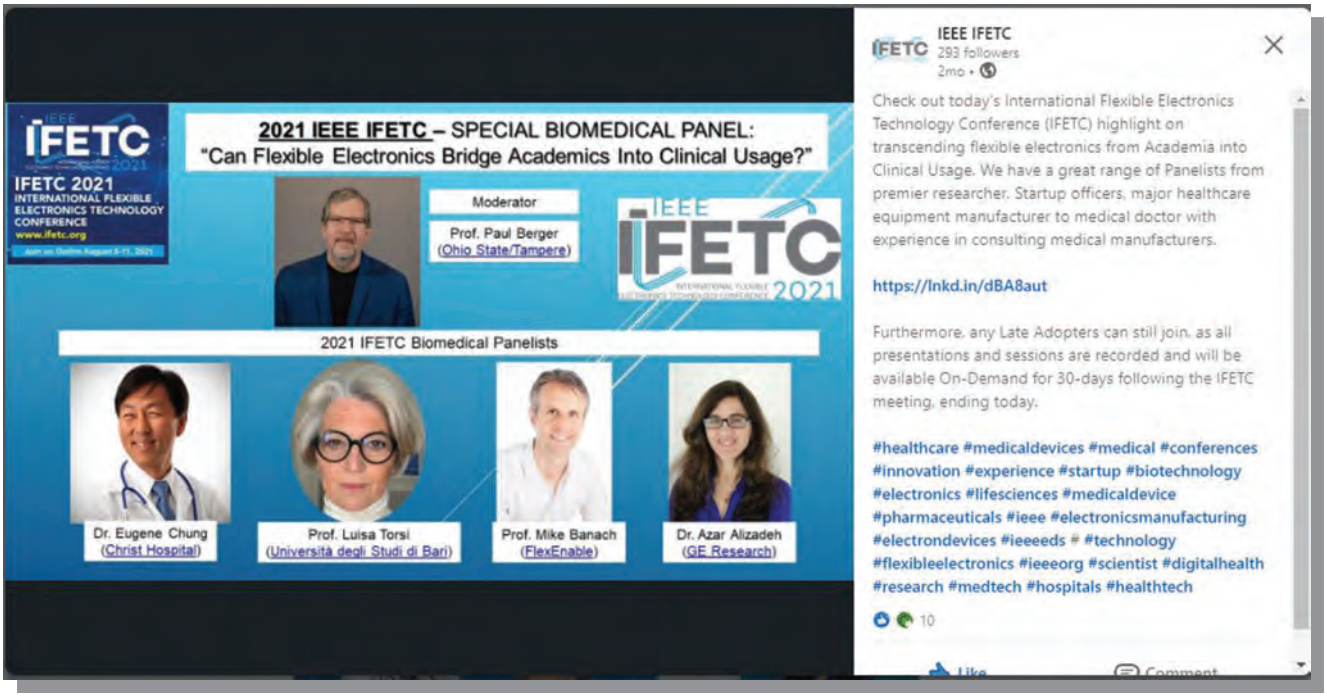


Figure 3. IFETC highlighted the transcendence of biomedical wearables from the academic research lab to the marketplace, tempered by prominent industrialists and leading medical doctors, who presented a sobering message of what is needed going forward

Leo (*Technische Universität Dresden)* reached for the flexible electronics sound barrier through "Towards GHz flexible organic electronics."

- Finally, a Special Panel was moderated by Paul Berger (*Ohio State/Tampere*) entitled "CAN FLEXIBLE ELECTRONICS BRIDGE ACADEMICS INTO CLINICAL USAGE" with key panelists Eugene Chung, MD (*Christ Hospital, Cincinnati, Ohio*), Luisa Torsi (*Universita degli Studi di Bari, Italy*), Mike Banach (*FlexEnable, Cambridge, UK*), and Azar Alizadeh (*GE Research/GE Healthcare, USA*).

And IFETC-3 transcended the usual Zoom conference, thanks to Niels Benson (*University of Duisburg—Essen*), by implementing the Gather.town platform as a gathering place for socialization and technical discussions in between sessions. I witnessed at least one proposal brainstorming session between two investigators. And looking over the Columbus, Ohio skyline at the end of each day at the sky bar, sitting next to the crackling fire with a beverage of our choosing was spectacular! Cheers!

On behalf of the Conference, International Advisory and Steering Committees, we thank contributors to IFETC-3! Special thanks to the Organic Electronics Association (OE-A) for contributions to the short courses. I am pleased to inform you that IFETC is now present also on social media, i.e. LinkedIn: https://www.linkedin.com/company/ieee-ifetc and Twitter: https://twitter.com/Ilfetc. Finally, IFETC is now branded too, with a new logo, and a dedicated webpage: www.ifetc.org for future years, like Qingdao, China in 2022.

Paul R. Berger
2021 General Chair
IEEE International Flexible Electronics Conference
https://ifetc.org

Highlights of IEEE EDTM2021

Sponsored by the IEEE Electron Devices Society (EDS), **IEEE Electron Devices Technology and Manufacturing (EDTM) Conference** is a premier conference providing a unique forum for discussions on a broad range of device/manufacturing-related topics. EDTM rotates among the hot-hubs of semiconductor manufacturing in Asia. EDTM2021 was successfully held in Chengdu, China, during 9–12 March 2021. Continuing its upward trend since EDTM was first launched in 2017, EDTM2021 was by all means another big success. The Theme for EDTM2021 was ***Intelligent Technologies for Smart and Connected Life***. Due to the pandemic, EDTM2021 was held in hybrid formats including a large onsite/in-person gathering and a virtual conference. EDTM2021 was a four-day conference comprising a one-day tutorial/short course/workshop event on 9 March, and a three-day technical program including both oral and poster sessions. On Day-1, EDTM2021 was kicked off with two parallel tutorial tracks and four concurrent short course sessions. The two tutorial series focused on "Flexible electronics + Display" and "Future Communication and Computing". The four short course sessions covered "Advanced Memories and Emerging Applications", "Quantum Computing Technologies", "Advanced Processing and Manufacturing" and "Ultra/Wide Bandgap Power Electronics". Total twelve lectures were given by globally renowned experts. The highlight on 9 March also includes the "HIR Workshop Organizing Committee" organized by the IEEE Heterogeneous Integration Roadmap Committee and featured by eighteen experts from around the globe discussing the advances, challenges and future

EDTM2021 Opening kicked-off both in-person and virtually

Participants of 5th IEEE EDTM Conference attending an in-person mode

*(From Left) Prof. Tiancun Ye (General co-Chair, 5th) and Prof. Huaqiang Wu (TPC Chair, 1st) presented the Best Student Paper Awards: First Place Award—**Nianying Wang** (3rd from left; paper: N. Wang, et al., Shanghai Inst. Microsystem and Information Technology, CAS, ShanghaiTech University, University of CAS—"Double-Deck Metal Solenoids 3D Integrated in Silicon Wafer for Kinetic Energy Harvester"); Third Place Award—**Qiumeng Wei** (2nd from left; paper: Q. Wei, et al., Inst. Microelectronics, Tsinghua University, Beijing Innovation Center for Future Chips, Tsinghua University—"Double-Deck Metal Solenoids 3D Integrated in Silicon Wafer for Kinetic Energy Harvester"); and Second Place Award—**Shunjie Yu** (4th from left; paper: S. Yu, et al., University of Science and Technology of China, Shandong University—"β-Ga2O3 Micro-Flake FET SBPD with Record Detectivity of 3.87×1017 Jones for Weak Light Detection")*

of HI technologies. EDTM2021 Technical Program started on 10 March with six Keynote Speakers talking about various hot topics, including Dr. Haijun Zhao (Co-CEO of SMIC) on "Creating Values through Innovations on Mature Nodes of Technologies of Integrated Circuits", Prof. Xiang Zhang (President, University of Hong Kong) on "How to build a camera with highest resolution: a photonics perspective", Mr. Teruo Hirayama (Executive Chief Engineer, Sony Corp.) on "The power of image sensors for innovation", Prof. Arokia Nathan (University of Cambridge) on "Thin Film Transistor Architectures for Advanced Analog Signal Processing", Prof. Ru Huang (Vice President, Peking University) on "Ferroelectric-based device: revived as a low-power technology booster for diverse applications", and Dr. Jeff Xu (Director, HiSilicon Research) on "Ubiquitous Computing Drives Future Semiconductor Technology". The Plenary was closed with a Closing Banquet Speech given by Prof. Ilesanmi Adesida (Provost, Nazabaryev University) entitled "The Development of an International Research University in the Big Steppe of Kazakhstan". EDTM2021 Technical Program core contains about 289 technical papers accepted after vigorous peer reviewing, including 172 oral (organized into 36 Sessions) and 117 interactive presentations. EDTM2021 had a total registered attendance of 800+, including 492 for the Technical Program (283 in-person and 209 virtual), 156 for Tutorials and 158 for Short Courses. EDTM2021 also featured a "Young Engineers' Networking" event and a "Women-in-Engineering Summit". EDTM2021 concluded with the Closing Banquet, a tradition of EDTM, full of Sichuan gourmet food, fun, and tears. EDTM2022 will move to Oita, Japan during 6–9 March 2022.

Albert Wang
2021 General Chair
University of California, Riverside, USA

Tianchun Ye
2021 General Co-Chair
Institute of Microelectronics, CAS, China

Huaqiang Wu
2021 Technical Program Chair
Tsinghua University, China

Subramanian Iyer
2021 Technical Program Co-Chai
University of California, Los Angeles, USA

2021 IEEE International Interconnect Technology Conference (IITC)

The International Interconnect Technology Conference (IITC), sponsored by the IEEE Electron Devices Society and co-sponsored by the Japan Society of Applied Physics, is the premier conference on interconnect technology, featuring cutting-edge research in the areas of advanced metallization and 3D integration for ULSI applications.

The 24th IITC was held on 6–9 July 2021 in a hybrid format of virtual and face-to-face meetings (Kyoto Research Park, Kyoto, Japan). Pre-recorded presentations were live-streamed and Q&A sessions were also held live.

The IITC 2021 live sessions were attended by 348 people from 14 different regions (Figure 1). Due to COVID-19, the number of guests who came to the conference room was limited (~10). The technical program included 2 plenary lectures, 12 invited lectures, 27 oral presentations, and 25 posters, presenting original and state-of-the-art research. On-demand videos were available until 31 August 2021.

Workshop Program

Prior to the technical program, a workshop entitled "Metallization Technologies and Their Applications in IoT and AI Devices" was held on 6 July, featuring seven leading experts.

M. Tsujimura (Ebara) reported on Digital and Green Transformation, which are driving the semiconductor market, and the revolution in manufacturing equipment. Experts in different technical fields discussed the most advanced key technologies for current and future applications of IoT and AI devices: 3D Flash memory by M. Tagami (KIOXIA), STT-MRAM by K. Lee (Samsung), Back-Illuminated-CIS by Y. Kagawa (Sony Semiconductor Solutions), Nano bridge Technology by M. Tada (NanoBridge Semiconductor), Reliability challenges in advanced interconnects by O. V. Pedreira (IMEC), and Si photonics by B. J. Offrein (IBM).

Technical Program

The technical program started with an opening speech by General Chair K. Ueno of Shibaura Institute of Technology, followed by the IITC2020 award ceremony.

Michel Lerme Best Paper Award was given to K. Motoyama, IBM Research for the work "Co-doped Ru liners for highly reliable Cu interconnects with selective Co cap".

LAM Research Best Student Paper Award was given to Y. Yamada, Tohoku University for the work "Thermodynamic Exploration of Co–Alloy Diffusion Barriers for Advanced Cu Interconnect".

Best Poster Award was given to T. Kuge, Tohoku University for the work "The structural origin of the minimum diffusion barrier thickness of ultra-thin TaNx".

After the ceremony, two keynotes were given by the technology leaders:

- **Prof. M. Koyanagi**, Senior Research Fellow, Tohoku University, "3D Heterogeneous Integration for Intelligent Mobile Systems";
- **Dr. G. Jeong**, Corporate EVP, Samsung Electronics, "Foundry Challenges and Opportunities Near the End of Moore's Era".

Among the topics discussed during the Conference it is worthwhile to mention "Old New" materials and process steps that were previously used in the Si front-end processes. E.g. molybdenum (Mo) was presented as the "new" contact or wiring material, and dry etching was discussed as the "new" interconnect formation method instead of the damascene process. In addition, various applications of selective deposition processes such as "old" tungsten chemical vapor deposition (W-CVD) and Self-Assembled Monolayer (SAM) were explored to overcome the scaling issues. It becomes noticeable that apart from

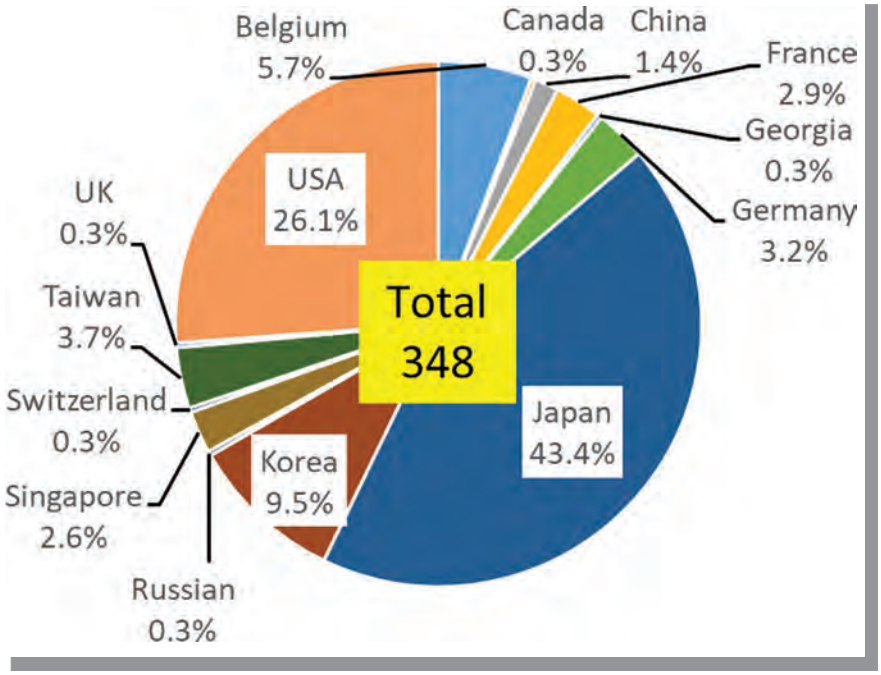


Figure 1. Percentage of participants from each country

miniaturization, the "old" approaches really work for the "new" challenges. As for the technology node, 7 nm–5 nm node process for production and <=3 nm node process for R&D were discussed. Furthermore, the potential of 3D heterogeneous integration technology to realize any future integration of circuits, devices, and systems was also discussed.

The following papers are examples of presentations that received a lot of attention from the participants:

- "Selective Barrier for Cu Interconnect Extension in 3 nm Node and Beyond", S. You, et al., Applied Materials;
- "Advanced Air Gap Formation Scheme Using Volatile Material", H. Warashina, et al., Tokyo Electron;
- "Process Integration of High Aspect Ratio Vias with a Comparison Between Co and Ru Metallizations", V.-H. Vega-Gonzalez, et al., Imec and Lam Research;
- "Advanced 5nm BEOL Integration Development for Manufacturing", J. Park, et al., Samsung;
- "Exploring W-Cu Hybrid Dual Damascene metallization for Future Nodes", M. H. van der Veen, et al., Imec and Applied Materials;
- "Selective Deposition of AlOx for Fully Aligned via in Nano Cu Interconnects", S. V. Nguyen, et al., IBM and Lam Research.

Invited Speakers

The Virtual 2021 IITC had some new activities. One of them was an

CATEGORY	TITLE	SPEAKERS
Advanced Interconnect	Advanced interconnect challenges beyond 5nm and possible solutions	Kichul Park (Samsung)
	EM performance improvements for Cu interconnects with Ru-based liner and Co cap in advanced nodes	Koichi Motoyama (IBM)
Integration/pattering	EUV patterning considerations for BEOL scaling	Nilson Felix (IBM)
	Analysis of edge placement error (EPE) at the 5 nm node and beyond	Robert Socha (ASML)
RC Scaling	On-die interconnect technologies for future technology nodes	Mauro Kobrinsky (Intel)
MOL Contacts	Contact module progress and challenges in advanced CMOS technologies	Nicolas Breil (AMAT)
Reliability	Reliability Characterization on Advanced FinFET Technology	Kihyun Choi (Samsung)
3D	Opportunities and challenges brought by 3D-sequential integration	Perrine Batude (CEA-Leti)
Memory	Enabling Ferroelectric Memories in BEOL—towards advanced neuromorphic computing architectures	David Lehninger (Fraunhofer)
	Commercialization of MRAM—Historical and Future perspective	Sumio Ikegawa (Everspin)
Novel System	Resistive memories for neuromorphic hardware	Elisa Vianello (CEA-Leti)
Beyond Cu	Intermetallic compounds for Interconnect metal beyond 3 nm node	Junichi Koike (Tohoku Univ.)

Members of on-line conference support group in Kyoto

exhibitor session from 7–9 July in between the technical sessions, where exhibitors gave presentations and virtual booth tours. The second new activity was the poster session, which consisted of five-minute presentations. Each of them was followed by an interview with the individual author in a separate virtual room to discuss the presented work with the audience. The third new activity was a networking reception where participants could converse with each other in close proximity on a virtual platform, creating an atmosphere similar to an actual social gathering.

This new format was proposed and implemented by Semiconductor Portal Inc. (Japan), the operator of this year's and 2013's IITC, and was well received. In the future, it will be necessary to run conferences in such a way that participants feel as if they were attending an actual conference. 2021 IITC was one of the great examples of this approach.

The next IITC will be held on 27–30 June, 2022 at Holiday Inn San Jose, California, USA. Looking forward to seeing you all there.

Susumu Matsumoto
Tower Partners Semiconductor

Shinichi Ogawa
AIST

Review of the 2021 IRPS

Edited by Chris Kim

The IEEE International Physics Reliability Symposium (IRPS) has been the premiere conference for engineers and scientists to present new and original work in the area of microelectronics reliability for 60 years. Drawing participants from the Americas, Europe, Asia, and all other parts of the world, IRPS seeks to understand the reliability of semiconductor devices, integrated circuits, and microelectronic systems through an improved understanding of both the physics of failure as well as the application environment.

The 2021 IRPS was held in a virtual format starting on 21 March and running until 24 March 2021—the duration of which the recorded presentations were accessible to the registrants. The virtual event was attended by almost 500 registered participants, which was 25% higher than the previous year and a record for recent years.

The highlights of the 2021 technical program include:

- 18 technical committees and 239 TPC members
- 20 technical sessions comprising 87 oral presentations, 53 poster presentations, 20 invited/focus talks, and 4 keynotes.
- 22 tutorials, 11 workshops, 3 year-in-reviews
- 10 exhibitors

The conference encompassed a wide range of topics, ranging from Circuit Reliability and Aging, Emerging Memory Reliability, ESD and Latchup, Failure Analysis, Gate/MOL Dielectrics, IC Product Reliability, Memory Reliability, Metallization/BEOL Reliability, Neuromorphic Computing Reliability, Packaging and 2.5/3D Assembly, Process Integration, Reliability Testing, RF/mmW/5G Reliability, Soft Error, System Electronics Reliability, Transistor Reliability, to Wide-Bandgap Semiconductors-GaN and SiC. The 2021 Special focus topics were Circuit Reliability and Aging (EDA Tools, Sensors, and Aging Aware Designs), Wide Bandgap Devices (with emphasis on Reliability, Availability and Serviceability (RAS), self-healing, aging aware design, design tools), Emerging Memory / Reliability issues of Neuromorphic Computing (PCM, MRAM, RRAM,

ferroelectrics), and Reliability of RF/mmW/5G Devices (CMOS, SiGe BiCMOS, SOI, GaAs, GaN).

The conference formally kicked off on 21 March 2021, with a welcome address by the General Chair Robert Kaplar, Sandia National Labs, and an overview of the technical program by the Technical Program Chair Chris Connor, Intel. Each day started with a plenary keynote by industry executives listed below.

- Day 1: Dr. Seok-Hee Lee, President and CEO of SK Hynix—Memory's Journey Towards the Future Information and Communications Technology (ICT) World
- Day 2: Dr. John Palmour, CTO of Cree / Wolfspeed—SiC MOSFET Reliability: An Overnight Success 30 Years in the Making
- Day 3: Dr. Peter Gammel, CTO of MWI at GlobalFoundries—Laying the Groundwork for 6G Communications
- Day 4: Dr. Alessandro Piovaccari, CTO of Silicon Labs—IoT End-Node Device: Built to Last (in cooperation with International Electro Static Discharge Workshop—IEW)

This year, tutorials and technical sessions were offered in parallel which gave the attendees greater flexibility to not only to listen to focused lectures from domain experts but also to learn about the latest research discoveries throughout the entire 4 day conference. Tutorials were given by instructors who are authorities in their respective reliability fields—either veteran IRPS presenters for established topics or invited specialists in emerging topics. A total of 22 tutorials were offered on topics ranging from 3D integration, 5G/mmW/RF, GaN, memory reliability, automotive, advanced interconnect, cryogenic electronics, design automation, ESD, to FinFET self-heating.

Day 1 ended with three Year-In-Review (YIR) talks, a segment always appreciated by IRPS attendees, allowing them to quickly catch up on recent developments in multiple areas. In this year's Year-in-Review (YIR) several speakers covered the past year of literature on (YIR1) FinFET versus Gate-All-Around FET Reliability, (YIR2) Considerations for Physics-Based Reliability Testing Development, and (YIR3) Industry Council on ESD Target Levels: Review of Achievements, Activities, and Initiatives.

Technical session presentations consisted of 107 Oral (of which 20 were invited) and 53 Poster papers, previously selected by 18 subcommittees. Due to the virtual nature of the conference, the papers were typically presented as prerecorded video clips which resulted in higher quality presentations. Poster presenters were allotted limited time to introduce their work and, to emulate the poster session experience, they could discuss their work with interested audience members in separate video calls. Workshops were held on Day 3 where attendees enjoyed informal discussions on specific reliability topics with the guidance of experienced moderators. As an added perk for this year's attendees, all recorded talks were available after the conference.

The IRPS subcommittees highlighted the following contributed papers:

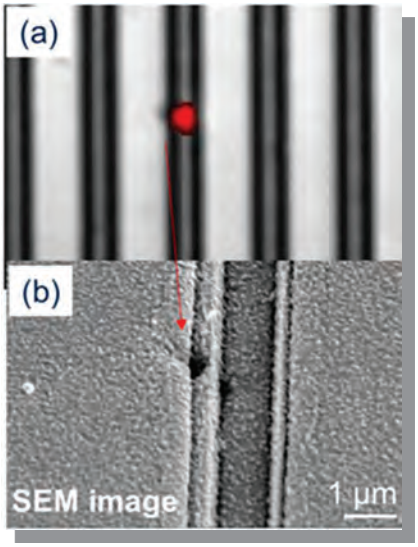
- A.G. Viey *et al.*, University Grenoble-Alpes—Study on the Difference between ID(VG) and C(VG) pBTI Shifts in GaN-on-Si E-Mode MOSc-HEMT
- J. Minguet Lopez *et al.*, Marseille Univ, INL CNRS—Elucidating 1S1R Operation to Reduce the Read Voltage Margin Variability by Stack and Programming
- T.E. Lee *et al.*, The University of Tokyo—Characterization of Slow Traps in SiGe MOS Interfaces by TiN/Y2O3 Gate Stacks
- H. Zhou *et al.*, IBM Research Division—TDDB Reliability in Gate-All-Around Nanosheet
- H. Jiang *et al.*, Samsung Electronics—Time Dependent Variability in Advanced FinFET Technology for End-of-Lifetime Reliability Prediction
- A. Lesniewska *et al.*, IMEC—Reliability of a DME Ru Semidamascene Scheme with 16 nm wide Airgaps
- W. He *et al.*, Arizona State University—Characterization and Mitigation of Relaxation Effects on Multi-level RRAM Based in-Memory Computing
- Z. Chen *et al.*, Micron Memory Japan—Reliability of Wafer-Level Ultra-Thinning Down to 3 µm using 20 nm-Node DRAMs
- G. Rzepa *et al.*, Global TCAD Solutions—Reliability and Variability-Aware DTCO Flow: Demonstration of Projections to N3 FinFET and Nanosheet Technologies
- S. Huang *et al.*, University of Illinois at Urbana-Champaign—Compact Model of ESD Diode Suitable for Sub-Nanosecond Switching Transients
- M. Wei *et al.*, Macronix International Co., Ltd, National Taiwan University—Robust Brain-Inspired Computing: On the Reliability of Spiking Neural Network using Emerging Non-Volatile Synapses
- B. Narasimham *et al.*, Broadcom Inc.—Scaling Trends in the Soft Error Rate of SRAMs from Planar to 5-nm FinFET
- Neel Chatterjee *et al.*, University of Minnesota, Intel—Machine Learning on Transistor Aging Data: Test Time Reduction and Modeling for Novel Devices
- P. Srinivasan *et al.*, GlobalFoundries—RF Reliability of SOI-Based Power Amplifier FETs for mmWave 5G Applications

After the conference, the following awards were announced:

Best Paper

Correlation Between MOSFETs Breakdown and 4HSiC Epitaxial Defects

P. Fiorenza, S. Adamo, M. S. Alessandrino, C. Bottari, B. Carbone, C. Di Martino, A. Russo, M. Saggio,



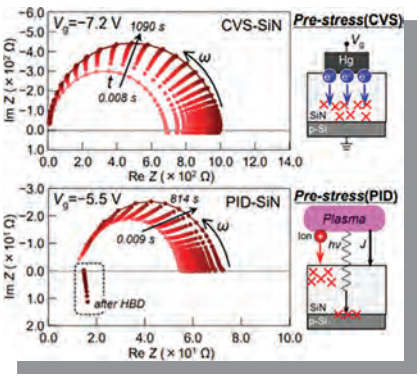
(a) Emission microscopy of the wafer level test of a defective device; (b) SEM image shows the presence of a pipe on the whole metalization

C. Venuto, E. Vitanza, E. Zanetti, F. Giannazzo and F. Roccaforte Consiglio Nazionale delle Ricerche—Istituto per la Microelettronica e Microsistemi (CNR-IMM) and ST-Microelectronics, Catania, Italy.

Best Student Paper

Evaluation Methodology for Assessment of Dielectric Degradation and Breakdown Dynamics Using Time-Dependent Impedance Spectroscopy (TDIS)

Tomohiro Kuyama, Keiichiro Urabe, Koji Eriguchi, Kyoto University, Kyoto, Japan

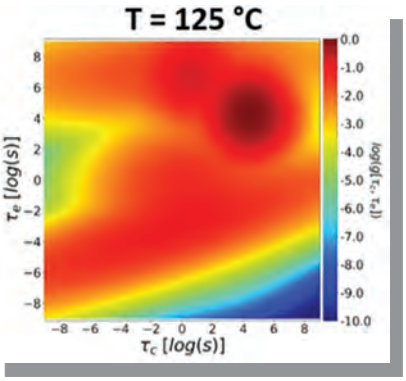


Assessment of plasma damaged SiN by TDIS: Nyquist plots of SiN after (top) electrical stress or (bottom) Ar plasma exposure

Best Posters

BTI Arbitrary Stress Patterns Characterization & Machine-Learning Optimized CET Maps Simulations

L. Gerrer, J. Cluzel, F. Gaillard, X. Garros, X. Federspiel, F. Cacho, D. Roy, and E. Vincent



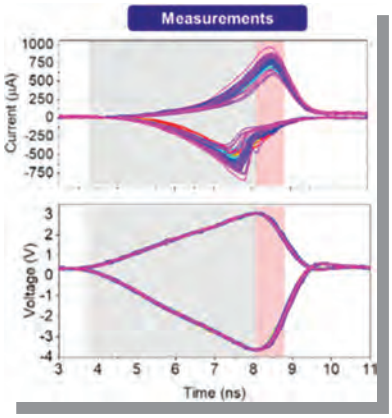
Capture/emission times (CET) map of the threshold voltage shift due to BTI for temperature 125 °C obtained using the genetic algorithm applied for the BTI model

CEA-LETI Grenoble, France and ST Microelectronics, Crolles, France

Mitigating Switching Variability in Carbon Nanotube Memristors

J. Farmer, W. Whitehead, A. Hall, D. Veksler, G. Bersuker, D. Gao, Al-Moatasem El-Sayed, T. Durrant, A. Shluger, T. Rueckes, L. Cleveland, H. Luan, R. Sen

The Aerospace Corporation, Los Angeles, CA, USA, Nanolayers Research Computing LTD, London, UK, Nantero Inc., Oburn, MA, USA

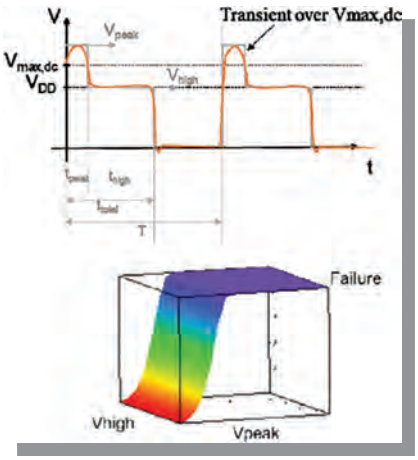


Measurements of Set and Reset currents during 5 ns repeated switching process

People's Choice

Off-state TDDB in FinFET Technology and its Implication for Safe Operating Area

M. Toledano-Luque, P. Paliwoda, M. Nour, T. Kauerauf, B. Min, G. Bossu, M. Siddabathula, T. Nigam



A standard three V-level waveform considered for the analysis (top); Failure rate for FEOL TDDB as a function of Vhigh and Vpeak with Vpeak > Vhigh at fixed tpeak and thigh

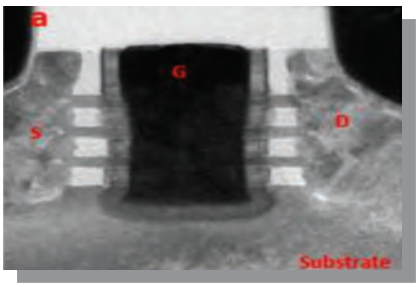
GlobalFoundries, Malta, NY, USA, Dresden, Germany, Santa Clara, CA, USA

TDDB Reliability in Gate-All-Around Nanosheet

Huimei Zhou, Miaomiao Wang, Ruqiang Bao, Tian Shen, Ernest Wu, Richard Southwick, Jingyun Zhang, Veeraraghavan Basker, Dechao Guo,

IBM, Albany, NY, USA

Next year, IRPS 2022 will return to an in person format from 27–31 March 2022, in Dallas, Texas. The latest information can be found on https://www.irps.org/.



TEM image of a stacked GAA NS transistor

Chris Kim
IRPS 2022 Publicity Chair
University of Minnesota

6th IEEE Electron Devices Technology And Manufacturing (EDTM) Conference 2022

6–9 March 2022, Oita, Japan
https://ewh.ieee.org/conf/edtm/2022/

The IEEE Electron Devices Technology and Manufacturing (EDTM) Conference 2022 is a four-day meeting to be held at Oita in Japan from 6–9 March 2022. EDTM is a premium conference sponsored by the IEEE Electron Devices Society that provides a unique forum to discuss and collaborate on a broad range of device/manufacturing—related topical areas including materials, processes, devices, packaging, modeling, reliability, and manufacturing and yield. Since its birth in 2017, EDTM has always been an excellent platform to establish contact and collaboration with the vibrating manufacturing community. In its 6th edition, EDTM will be held in Japan, with the main theme: "*Semiconductor Devices and Manufacturing Innovations for a More Sustainable World*".

Technical Sessions

The EDTM 2022 solicits papers in all types of exploratory device concepts within the following broad technical areas:

- Materials
- Process, Tools, Yield, and Manufacturing
- Semiconductor devices
- Memory technologies
- Photonics, imaging and display
- Power and energy devices
- Modeling and simulation
- Reliability
- Packaging and heterogeneous integration
- Sensor, MEMS and Bio-electronics
- Flexible and wearable electronics
- Nanotechnologies
- Disruptive technologies—Internet of things (IoT), Artificial intelligence (AI), Machine learning (ML), Neuromorphic & Quantum computing

World-class researchers in all areas will deliver invited talks. Regular submissions will be evaluated for oral and poster presentation. However, authors should indicate their preference for oral or poster presentation format when submitting their abstracts.

Publications

EDTM 2022 papers will be subjected to IEEE EDS standard review processes and IEEE conference publishing guidelines. The accepted papers presented at the meeting will be published in the EDTM 2022 Proceedings and may be available on IEEE Xplore. Besides, the authors of selected high-impact presented papers will be invited to submit their extended versions for the consideration of publication in the IEEE Journal of the Electron Devices Society (J-EDS). All such submissions must comply with J-EDS author guidelines and will be subjected to the standard IEEE and J-EDS review and publication policy.

Short Courses and Tutorials

EDTM 2022 will start with a set of short courses and tutorials on 6 March 2022. Tutorials teach selected topics from the basics to the state-of-the-art, allowing the attendees to catch up on a topic quickly. Short Courses discuss the latest research and challenges on hot and advanced topics encompassing the EDTM 2022 theme, selected from the topics of: heterogeneous integration, artificial intelligence (AI) and machine learning (ML), internet of everything (IoET), 5G+, autonomous systems, industry 4.0, future computing and quantum information processing, all enabled by electron devices.

Important Dates

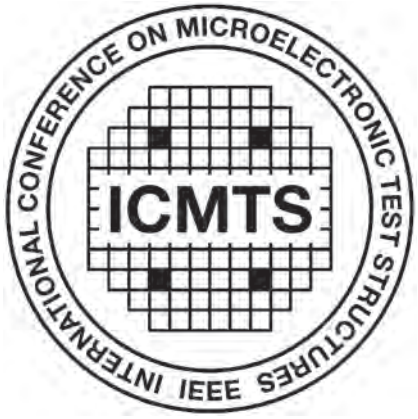
1 November 2021: Abstracts submission deadline (extended)
20 December 2021: Notification of acceptance (tentative)
11 February 2022: Early registration deadline (tentative)

COVID-19 Watch: We are closely monitoring the global infection status of COVID-19 to ensure the safety of EDTM conference participants. NOTE: The EDTM will be held as a fully virtual conference with live sessions (in-person/on-site meetings are canceled).

Masaharu Kobayashi
2022 Publicity Chair
6th IEEE EDTM Conference 2022

34th IEEE International Conference on Microelectronic Test Structures (ICMTS)

The 34th International Conference on Microelectronic Test Structures (http://icmts.net/) will be held in Cleveland, Ohio, USA, 21–24 March 2022. ICMTS is sponsored by the IEEE Electron Devices Society and is the only conference focused on the specialized requirements and methodologies related to the design, measurement, and analysis of test structures and the information they produce. As technology continues to become more complex, the ability to accurately predict how a device and/or circuit will behave is increasingly critical and difficult. For every circuit or product that operates properly, someone has designed, built, and measured one or more test structures to make sure it behaved as modeled. This conference is an opportunity for experts from all over the world to interact, to review technical results, and to debate the finer points of test structures. ICMTS authors and attendees are a mixture of academia and industry from all over the world, presenting a unique opportunity for learning and networking. The conference format provides time for one-on-one discussions with authors and other attendees, enabling a unique and inviting atmosphere.



ICMTS started as a workshop in 1979 and became a standalone conference in 1986. The location rotates between the USA, Japan, and Europe (2023 will be in Tokyo, Japan, and 2024 will be in Edinburgh, Scotland). The global pandemic caused 2020's conference to go fully virtual and 2021's conference was delayed a year. We're very excited to get back to work in 2022. Because of international travel restrictions that might still be in place in March, ICMTS 2022 will implement a hybrid model as needed. Travel restrictions over which an author has no control should not prevent him/her from presenting their solid technical work to their peers.

ICMTS starts with a full day of tutorials, organized by the 2022 Tutorial Chair, Matthew Rerecich. The topics will cover basic test structure methods as well as advanced topics. The 2022 Technical Program Chair, Chadwin Young, will oversee two and a half days of peer-reviewed, single-track technical talks. Topics will range from design to measurement to data analysis, all with a focus on the test structures that enabled the work. These commonly cover CMOS, memories, sensors, MEMS, photonics, and materials such as flexible substrates. The push toward the use of foundries, especially for advanced technology nodes, has made papers related to within-die measurements and characterization more common and interesting.

On behalf of the 2022 ICMTS Organizing Committee and the entire ICMTS Technical Program Committee, we invite you to join us in Cleveland, OH, USA, 21–24 March , 2022. It's sure to be an exciting and engaging conference!

Brad Smith
ICMTS 2022 General Chair

Chadwin Young
ICMTS 2022 Technical Program Chair

2022 IEEE International Memory Workshop (IMW)

The 14th International Memory Workshop (IMW) will be held at Taschenbergpalais Kempinski Hotel in Dresden, Germany, from 15–18 May 2022. The history of the IMW dates back to the NVSMW (Nonvolatile Semiconductor Memory Workshop) which began in 1976 and which later merged with the ICMTD (International Conference on Memory Technology and Design) to become the IMW. The IMW is sponsored by the IEEE Electron Devices Society and meets annually in May. The workshop covers all types of memory technology, is focused on advancing innovation in memory technology, and is organized in a way that provides excellent professional development and networking opportunities for attendees.

The IMW is the premier international forum for both new and seasoned technologists having diverse technical backgrounds to share and learn about the latest developments in memory technology with the global community. The scope of workshop content ranges from new memory concepts in early research to the technology drivers currently in volume production as well as emerging technologies in development. Topics include new device concepts, technology advancements, scaling and integration, circuit design and reliability, as well as emerging applications. Consistent with the increased importance of memory system architecture and integration, the workshop also includes increasing coverage of the systems in which memories are deployed and the co-evolution of memory technology along with memory systems and applications.

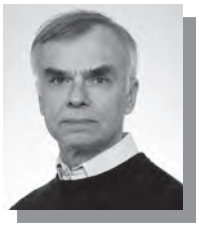
The IMW is the preeminent forum covering the latest developments, innovations, and evolving trends in the memory industry. Typical workshop attendance exceeds 250 attendees, and the technical program begins with a full day short course given by distinguished experts that provides an excellent professional development opportunity for both new and experienced technologists. The single-track technical program spans three days and also includes an evening poster session for informal technical discussion with authors as well as a panel discussion where experts discuss and debate a current hot topic. The previous workshops included invited talks from industry and research leaders. Key notes in the recent workshops were presented by Micron, Intel, Kioxia, ASML, Western Digital, IMEC, Yale Univ., Panasonic, Honda, ST Micro and NXP. Tutorial and highlights in the recent workshops included 3D NAND, DRAM, Embedded memories, Emerging memories and innovation (PCM, RRAM, MRAM, FeRAM…) for storage class memories, data centric architectures, tremendous growth of connected objects, and for neuromorphic memory, quantum computing and in-memory computing. While the last two editions of IMW were virtual events with excellent response and active participation by real time Q&A, IMW returns as an on-site event in 2022 and is currently planned to be held in Dresden. The technical program is organized to maximize networking opportunities and facilitate open information exchange among workshop contributors, committee members, and attendees. The program schedule includes ample time dedicated to social events including provided refreshment breaks, a workshop luncheon, and an evening banquet, and starting in the 2022 event, IMW is introducing a new policy of casual clothing to further promote informal discussions between participants.

On behalf of the organizing committee, I cordially invite you to participate in the IMW'2022 to continue to participate in the advancement of innovation in the rapidly evolving memory industry. For additional information, including the call for papers, key dates, abstract submission instructions, registration information, and technical program details, please visit the IMW website for the latest updates: http://www.ewh.ieee.org/soc/eds/imw/.

I look forward to seeing you in Dresden this May.

Srivardhan Gowda
2022 IMW Publicity Chair
Intel

Message from EDS Newsletter Editor-in-Chief



Daniel Tomaszewski
EDS Newsletter
Editor-in-Chief

Dear Readers, Members of the IEEE EDS Community.

Welcome to the IEEE EDS Newsletter issue January 2022. I hope that this issue brings you interesting information on a technical, organizational, societal, humanitarian activities of Electron Devices Society.

Firstly, at the beginning of 2022 we wish Ravi Todi—the President of EDS, Bin Zhao—the newly elected President-Elect, Roger Booth—the newly elected Treasurer, and MK Radhakrishnan—the Secretary, a fruitful work for the Society and an excellent collaboration with all units of the Society.

In the Society News we share with you a Message from Murty Polavarapu, EDS Vice President of Regions and Chapters. We deeply appreciate his contribution since we try to cooperate with the EDS Committee of Regions and Chapters in order to improve the visibility of the Chapters in the Newsletter. We present a summary of the EDS Board of Governors meeting, 11-12 Dec. 2021. The section also contains lists of IEEE EDS Fellows Elected 2021 and of new EDS Distinguished Lecturers. We sincerely congratulate them on the distinctions.

It is my pleasure to congratulate Prof. Tsu-Jae King Liu (UC Berkeley) who is the 2021 IEEE EDS Education Award Winner. This award is presented annually by EDS to honor an individual who has made distinguished contributions to education within the field of interest of the IEEE Electron Devices Society. We hope to publish in the next issue Prof. Liu's article on different aspects of her educational work.

I would like also to congratulate members of IEEE ED Spain Chapter which has been selected as the 2021 recipient of the IEEE EDS Chapter of the Year Award, and members and advisors of National Institute of Technology Silchar Student Branch Chapter which has been selected as the 2021 recipient of the Student Branch Chapter of the Year Award.

Coming back to the issue content, in the Technical Briefs section you will find highlights of the conferences sponsored by EDS, held in 2021: IRPS, EDTM, IITC, IFETC, IEDM (in a chronological order). These Technical events are of great importance for many EDS members.

The Upcoming Technical Meetings Section presents advertisements of the important conferences which will be held in the first half of 2022: ICMTS, EDTM, IMW. Besides, in the Regional News section you will find an advertisement of RFIC which is supported by EDS. Dates of other conferences sponsored or supported by EDS you may find in the Conference Calendar published at the end of this issue or on the website https://eds.ieee.org/conferences.

In the EDS Young Professionals and EDS Women in Engineering sections we present outstanding researchers: Dr. Qianqian Huang, 2019 IEEE EDS Early Career Award Winner, and Prof. Hui-Ying Yang, a world-renowned materials scientist.

In the Humanitarian Projects News, Chapter News, and Regional News sections we present traditionally articles on local activities carried out by the EDS chapters worldwide. I am very glad that the diversity of the chapter undertakings is more visible now. I am aware that it has partially been triggered by the pandemic. It is symptomatic that mainly the chapters in Region 10 South and South-East Asia make efforts to take such initiatives.

Dear Readers, if you have any suggestions, comments regarding the Newsletter contents, please do not hesitate to contact the editorial team. We will be very glad to receive your feedback. Interesting views will be presented with the consent of the authors, along with our replies in the Letters to Editors section.

Finally, I would like to express again my thanks to all the article Authors and to all the members of the Editorial Team. I hope that the Readers will find the issue interesting.

Sincerely,
Daniel Tomaszewski

EDS Board of Governors Meeting—December 2021

MK Radhakrishnan
EDS Secretary

EDS Board of Governors meeting in December 2021 was organized virtually due to the COVID19 pandemic and it was the fourth such virtual meeting in a row. EDS Executive Office staff provided CISCO Webex meeting support for the meetings of 3 hours each from 9.00–12.00 US Eastern time on 11 and 12 December 2021. The timing was planned to accommodate presentation schedules and to suit the convenience of Society's global representation of different time zones. Almost all elected members of the BoG and EDS Forum members attended the virtual meeting on both days.

EDS President, Ravi Todi welcomed the online attendees and informed that the meeting would have presentations by all the VPs and others scheduled in the agenda, but limited to 10 minutes each. Ravi presented the major highlights including the overall summary of the activities in 2021 and the successful culmination of the year with most of the technical activities going virtual. The Q&A was managed with questions and comments via chat box and email. All the motions were presented and the voting had to take place via email after the meeting.

Bin Zhao, EDS Treasurer, presented the financial status reporting an operating margin of $2,654K in 2020, 50% of which can be utilized for new initiatives. The budget for 2022 has been revised due to the pandemic situation with an expectation of $2,100K operating margin. Both the revenue and expenses reduction in conferences related activities affected in 2020 and 2021 due to pandemic, has been adjusted back to normal in 2022.

EDS Secretary, MK Radhakrishnan presented the Secretary's report and Newsletter report. Minutes of the mid-year BoG meeting were submitted for approval. The Newsletter is planning special sessions throughout the year of 2022 to celebrate the 75th year of transistor invention.

Kazunari Izhimaru, VP of Meetings informed that almost all the conferences were organized virtually this year. Out of the EDS financially sponsored conferences, only EDTM and IEDM are held as hybrid events. Most of the technically co-sponsored conferences were held virtually with very few in hybrid mode. Kazu also presented the vision and mission of EDS Women in Engineering group.

Navakanta Bhat, VP of Education informed the successful organization of webinars every two weeks throughout the whole year. Four summer school proposals approved have been very successfully organized by 4 chapters. A special session on career guidance has been organized. Two short courses organized through EDS Resource Center were reported to be very useful to attendees. Under the EDS education program, 14 podcasts featuring interviews with illustrious members of our community have been successfully conducted.

Joachim Burghartz, VP Publications & Products informed that all EDS journals (TED, EDL and JEDS) have an overall improvement in the number of paper submissions and Impact Factor. The acceptance rate for all three journals remains more or less the same as in the previous year. The letter of intent submitted for the EDS Magazine was processed and the phase 1 proposal is in preparation.

Murty Polavarapu, VP Regions and Chapters, reported that EDS has 224 chapters at present with 85 student branch chapters and 88 section joint chapters. All these chapters have organized 537 meetings in 2021 till the end of October, which is much more than in 2020. The virtual DL programs are getting more popular and many times global attendance based on publicity is reported. Eight new DLs are included in the DL roster. EDS Spain Chapter won the Chapter of the Year Award in the general category, whereas NIT Student Branch Chapter in Silchar, India won the Student Chapter of the Year Award.

Patrick Fay, VP for Membership informed that the EDS membership growth trends indicate not much improvement in the total member strength globally. Undergraduate student member strength is mostly concentrated in Region 10, whereas the graduate student memberships are mostly from Regions 1–6, Region 8 and 10. He emphasized the need to enhance EDS value to members to improve the overall membership.

The second day's meeting on 12 December 2021 started with the presentation by John Dallessase, VP for Technical Committees. There are 15 TCs with 129 TC members and the pandemic fatigue has resulted in a lower number of activities this year. However, the TCs supported EDS webinars and special sessions at conferences. Six TC Chairs will be retiring this year and John thanked them for their services.

Paul Berger, VP Strategic Directions, presented the EDS strategy outline to oversee future directions coordinating with IEEE Future Direction Committee and similar initiatives in sister societies. Strategic goals have been identified and approved. Strategic planning includes the existing technical fields and activities and diversion, humanitarian engineering and multidisciplinary strategic alliances. All these are planned to have measurable targets aimed at a 5 year and 20 years development plan.

Giovanni Ghione, Editor-in-Chief of TED presented the status of the journal, showing progress in paper submission and acceptance. Jesus del Alamo, Editor-in-Chief of EDL presented EDL status which shows

the cycle time for paper acceptance of EDL being one of the best in IEEE publications. Enrico Sangiorgi, Editor-in-Chief of JEDS, informed that there are 7 special issues for JEDS this year out of which 4 were published. The impact factor of all three journals has been improving every year.

Camilo Velez, YP Committee Chair, presented Young Professionals committee activities, which have been progressing. EDS visibility in Social Media platforms is very good. Among various platforms, LinkedIn seems to be the most useful to increase EDS visibility.

Tibor Grasser, 2021 IEDM General Chair presented the latest status of the first ever hybrid IEDM this year. The Tutorials and Short courses had good participation both online and on site. The conference will have both on site and online presentations.

Fernando Guarin presented the Humanitarian Activities summary. In 2021, EDS spent $129.6K on 5 projects and $410K on 22 projects from the previous years, 3% of reserve and 50% of operating budget funds. Fernando announced the EDS awards for this year. The results of the EDS Officers and BoG election held via online / email were announced. Samar Saha presented the Fellow evaluation details. There are 20 EDS members elevated to IEEE Fellows among the 2022 Class of Fellows. Patrick McCarren gave a report summarizing EDS office activities.

Ravi Todi reminded the forum about the plans to celebrate the 75th year of transistor invention in 2022. A committee with Manoj Saxena as convener will be coordinating the activities. All EDS Chapters are encouraged to participate in this and make it a success. Ravi thanked all attendees of this meeting from around the globe for their participation and support throughout the year, as well as EDS Staff for their dedicated effort in the midst of the pandemic. He adjourned the virtual meeting at 12:00 pm US Eastern Time.

MK Radhakrishnan
IEEE EDS Secretary

Message from the EDS Vice President of Regions and Chapters

Murty Polavarapu
EDS Vice President of Regions and Chapters

EDS volunteer leaders of Electron Devices Society (EDS) Chapters.

Please note that all **active** EDS Chapters (Section-based) are eligible for USD $200 annual rebate from IEEE Member and Geographic Activities (MGA). This rebate is **separate from the Chapter Subsidy** provided by EDS. Student Branch Chapters are not included in this rebate program. There will be a separate announcement forthcoming for 2022 Chapter Subsidy Requests from EDS.

For a chapter to be considered to have been active in 2021, the following requirements must be met:

1) The Chapter must have held a minimum of two (2) technical meetings in 2021. Virtual meetings do count for this purpose. These meetings must be reported using vTools at https://events.vtools.ieee.org/ **by 15 March 2022.**
2) The Chapter Officers must be reported using vTools at https://officers.vtools.ieee.org/ **by 15 March 2022.**
3) The annual financial report (via NextGen) and compliance reporting must be submitted **by 28 February 2022.** The reconciliation and compliance reporting is not applicable if your Chapter does not have its own bank account. Submit all of the Compliance Forms and the 2021 Year-end Bank Statements for Local Bank Accounts at the MGA Compliance Documents portal available at (https://mga.ieee.org/resources-operations/geographic-unit/reporting-rebates/financial). You will need to use your IEEE credentials to log into this portal and be sure to use Google Chrome or Safari (there may be issues with other browsers).

This rebate will be transferred by IEEE MGA to the parent Section of the Chapter in April/May and the Chapter will be informed. The Chapters are entitled to receive this rebate from their parent Sections as per MGA Operations Manual. Chapters are also eligible for an additional USD $75 activity bonus if they have held and reported a minimum of six technical meetings in 2021. Your parent Section may also urge you to complete the reporting by 19 February 2022 to be eligible for a 10% early reporting bonus.

If needed, please visit <https://site.ieee.org/vtools/training/> to access tutorials on how to enter the meeting reports and officer roster information. If you have questions or assistance in filing the financial and compliance reports, contact the MGA

Finance Team at finance-solutions@ieee.org.

If you need additional assistance in filing these reports, I recommend that you first contact your parent Section. If you still have unresolved issues, you can contact Stacy Lehotzky at the EDS Office (s.lehotzky@ieee.org).

Thank you for your volunteer service to IEEE and its members.

Murty Polavarapu
EDS Vice President of Regions and Chapter Space Electronics Solutions

Congratulations To The 2021 IEEE EDS Award Winners!

The IEEE Electron Devices Society is proud to announce the 2021 IEEE EDS Award Recipients. Award recipients are selected through a comprehensive nomination and evaluation process. Please join us to congratulate this year's recipients for their exceptional achievements. Visit the EDS website to learn more about this year's awardees: https://eds.ieee.org/awards/2021-ieee-eds-award-presentations

IEEE EDS Fellows Elected 2021

Since 1963, IEEE has acknowledged those individuals who have contributed to the advancement of engineering science and technology. The honor of Fellow is bestowed on the recipient who has had an extraordinary record of accomplishments in any of the IEEE fields of interest. To learn more about the IEEE Fellow Program: https://www.ieee.org/membership/fellows/index.html.

Congratulations to the fifteen EDS members elected to IEEE Grade of Fellow in 2021.

Deji Akinwande—for contributions to wafer-scale graphene synthesis and application to flexible devices

Hideaki Aochi—for contributions to three-dimensional flash memories

Benton Calhoun—for contributions to sub-threshold integrated circuits and self-powered systems

Yogesh Chauhan—for contributions to compact modeling of Si and GaN transistors

Vasilis Fthenakis—for contributions to photovoltaics technology

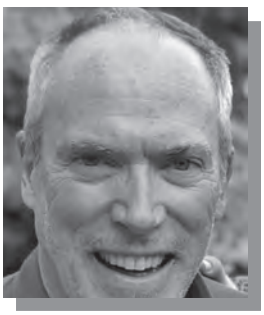
Robert Henderson—for contributions to solid-state single photon imaging

Ali Keshavarzi—for contributions to low-power circuits and devices in scaled CMOS technologies

Chang-Jin "CJ" Kim—for research of surface-tension-based microelectromechanical systems

Gourab Majumdar—for contribution to power semiconductor devices and intelligent power module

Jon Ohta—for contributions to CMOS image sensors and devices for biomedical applications



Bryan Root—for leadership in improving semiconductor reliability test methods

Ashwin Seshia—for contributions to resonant-based inertial and mode-localized sensors

Tetsuya Suemitsu—for contributions to high-frequency high-electron-mobility transistors

Takatoshi Tsujimura—for contributions to the development of organic-light-emitting diode systems

Yifeng Wu—for contributions to Gallium Nitride microwave and power conversion devices

Shinji Yuasa—for contributions to MgO-based magnetic tunnel junctions

New EDS Distinguished Lecturers Announced

Our Society is pleased to welcome eight new Distinguished Lecturers (DLs) this year to help bring talks on leading edge topics to our Chapters. The additions to our DL roster reflect technical, geographic and gender diversity. Please see below for a listing of the new DLs. Chapter Chairs are encouraged to reach out to the DLs directly to extend invitations for lectures at Chapter meetings. Funding is available from EDS. In-person talks are now possible subject to local restrictions and the latest IEEE Travel Policy for volunteers. For more information on the DL program, please visit https://eds.ieee.org/education/distinguished-lecturer-mini-colloquia-program.

Nowshad Amin
Universiti Tenaga Nasional, Malaysia
Energy Harvesting / Storage

Francesca Iacopi
University of Technology, Sydney, Australia
Heterogenous Integration

Huaqiang Wu
Tsinghua University, China
Neuromorphic/Brain Inspired Computing

Ann Concannon
Texas Instruments, USA
Heterogenous Integration

Jaydeep Kulkarni
University of Texas at Austin, USA
In-Memory Computing

Shimeng Yu
Georgia Institute of Technology, USA
Neuromorphic/Brain Inspired Computing

Nazek El-Atab
King Abdullah University of Science and Technology, Thuwal, Saudi Arabia
Energy Harvesting / Storage

Felix Palumbo
Unidad de Investigación, Buenos Aires, Argentina
Next Generation RF

Murty Polavarapu
EDS VP of Regions and Chapters

Call for Nominations—EDS Student Fellowships for 2022

The IEEE Electron Devices Society invites nominations for the 2022 PhD, Masters and Undergraduate Student Fellowships. These annual awards are given to promote, recognize, and support graduate, masters, and undergraduate level study and research within the EDS field of interest.

Please help to promote the EDS Student Fellowships by distributing this information to your colleagues and students. If you have any questions or need further information, please do not hesitate to contact Stacy Lehotzky by email at s.lehotzky@ieee.org. Thank you!

For access to more information and applications: https://eds.ieee.org/education/student-fellowships

EDS Masters Student Fellowship

Prize: US $2,000 and an award plaque

Submission Deadline: May 15, 2022

EDS PhD Student Fellowship

Prize: US $5,000 and travel funds to attend the IEDM for presentation of an award plaque

Submission Deadline: May 15, 2022

For both Masters and PhD, it is expected that at least one fellowship will be awarded to a student in each of the following geographical regions: Americas, Europe/Middle East/Africa, and Asia/Pacific.

EDS Undergraduate Student Scholarship

Prize: US $1,000 and an award plaque

Submission Deadline: May 15, 2022

For the Undergraduate, it is expected that at least one fellowship to each eligible student in each of the IEEE geographical Regions 8, 9, and 10 and two fellowships in Regions 1–7 not exceeding one from Region 7.

EDS Podcasts Available to Everyone!

Join us as we host interviews with some of the most successful members of our Society sharing their lives and careers. Their insight and wisdom inspire those in the engineering field. Stay tuned to our social media channels and website for future announcements on new podcast releases.

Dr. Qianqian Huang: 2019 IEEE EDS Early Career Award Winner

Key Laboratory of Microelectronic Devices and Circuits (MOE), Institute of Microelectronics, and National Key Laboratory of Science and Technology on Micro/Nano Fabrication, Peking University, Beijing, China

What was the specific temptation, if any, which made you join EDS which is the largest professional organization in the globe, at first?

Since my research area is in the field of electron devices, I take it for granted that I join the IEEE Electron Devices Society which is the largest and also the best professional organization in the field of Electron Device. I benefited a lot when I first attended IEDM, which is the EDS flagship conference, ten years ago. It has become a habit for me to attend the IEDM conference every year since then. Electron Devices Society provides a wonderful platform for members for sharing, exchanging and discussing their viewpoints or technical progress, accessing the most advanced expert knowledge and helping promote technology innovation at the cutting edge.

You won the prestigious EDS Early Career Award, an honor most of the young professionals aspire to. How do you consider this recognition and what are your plans to further develop your research career ?

I feel highly honored and humbled to receive the EDS Early Career Award. The award is a strong recognition of my past work and will greatly support and promote my career development in the future. During the past ten years, my research work is mainly focused on the design and realization of advanced ultralow-power devices for logic and neuromorphic applications, in particular tunnel devices and ferroelectric devices. I will continue the fundamental research of electron devices and further devote

myself to study, design and implement extremely low-power chips.

As a Young Professional, how do you position your interest in your own field with the activities and services you perform as an EDS member/ volunteer?

As a young professional, I've actively contributed to the electron device community by presenting my research work in many international conferences and seminars as an invited speaker, and serving as a reviewer for a number of EDS journals, including EDL, TED, J-EDS, etc. Most of the activities and services I perform are related to my research interest and provide more opportunities for networking with distinguished researchers in my field.

What are your thoughts about EDS membership and its paybacks? Whether the EDS membership benefited you at any time in your career growth?. If so, how?

The EDS membership has benefited me a lot ever since I was a PhD student. When I was a student member I participated in various lectures and seminars held by IEEE ED Peking University Student Branch Chapter. I got many chances to directly communicate with distinguished professors from whom I obtained valuable suggestions and experience not only on research work but also on career development. As a PI now, the EDS membership further promotes my career growth comprehensively and offers me a platform full of opportunities.

As a YP, how do you consider the ED Society as a whole and what are the changes or developments you would like to see in evolving this professional body as a group devoted to humanity and its causes?

The ED Society has already performed very well in the field of electron devices as a whole. Recently, I am helping establish EDS Women in Engineering to encourage and support WIE activities as a volunteer. We find that few EDS conferences hold WIE events and sometimes speakers are hard to find. I think it is a very meaningful work to discuss and take some effective actions to encourage or promote WIE activities, which will make the ED Society a better community in turn.

What are your suggestions and recommendations for those young professionals who may aspire to join EDS?

There is no doubt that joining EDS is a quite wise decision for the young

professionals in the electron device field.

As an EDS Young Professional and a young researcher in the field, how do you consider the prospects of scientific research in this field for the progress of Humanity as a whole?

Electron devices are the fundamentals of integrated circuits which have profoundly changed human society for decades. With the fast development of integrated circuits, more severe, uncertain but exciting challenges are encountered in the research of electron devices. I believe that under the support, help and promotion of EDS, the device communities will promptly find new directions and solutions and continuously provide solid scientific support for the progress of humanity.

Qianqian Huang is currently an assistant professor at Peking University (PKU). She received her PhD. from the Institute of Microelectronics, PKU in 2015, and B.Sc. from the School of Electronic Engineering and Computer Science, PKU in 2010. Her research interests are in the area of emerging ultralow-power device technology for logic applications and neuromorphic computing, focusing on tunnel FET, negative capacitance FET and ferroelectric FET, and FET variability, reliability and noise. She has authored/co-authored more than 70 technical papers in international journals and conferences, including 10 IEDM and VLSI papers (6 papers as the first author, 3 papers as the corresponding author, 7 times as the presenter). She has more than 50 authorized patents. Her honors include the Xplorer Prize (2020), Qiu Shi Outstanding Young Scholar Award (2020), IEEE Electron Devices Society Early Career Award (2019), the Forbes 30 under 30 in Science in China (2019), National Science Foundation of China for Excellent Young Scientists (2018), Young Talents of the L'Oréal-UNESCO For Women in Science Award in China (2017), etc. She is currently a member of IEEE Electron Devices Society VLSI Technology & Circuits Committee and a member of the Board of Governors of the Women Scientist Association of CIE.

Dr. Harshit Agarwal: 2020 IEEE EDS Early Career Award Winner

Assistant Professor, Department of Electrical Engineering, IIT J-Indian Institute of Technology Jodhpur, India

What was the specific temptation, if any, which made you join EDS which is the largest professional organization in the globe, at first?

My deep interest in the field of EDS forced me to join EDS, and I am glad that I joined EDS. IEEE EDS is an excellent platform for knowledge sharing, meeting new peoples and gaining insight into emerging technologies. This enables you to contribute meaningfully towards the development of future technologies.

You won the prestigious EDS Early Career Award, an honor most of the young professionals aspire. How do you consider this recognition and what are your plans to further develop your research career?

This is a proud moment. I thank EDS for creating a mechanism to encourage young professionals like us.

I wish to continue my contribution in the field of semiconductor devices and applications.

As a Young Professional, how do you position your interest in your own field with the activities and services you perform as an EDS member/volunteer?

My interest lies in semiconductor device design and modeling for applications like IoT, quantum computing, machine learning etc. Since this is in-line with the broader EDS field of interests, it helped me in my role as EDS volunteer and member. For instance, I am an active reviewer of the EDS journals (featured consecutively three times in the list of golden reviewers of EDL and TED) and a member of IEEE Electron Devices Society Compact Modeling Committee.

What are your thoughts about the EDS membership and its paybacks? Whether the EDS membership benefited you at any time in your career growth? If so, how?

EDS is one of the largest professional organizations. Its membership

is really helpful as it brings academia and industry experts on the same platform, facilitates candid discussions and easy flow of knowledge. This is a healthy culture, which benefits not one but all.

As a young professional, how do you consider the ED Society as a whole and what are the changes or developments you would like to see in evolving this professional body as a group devoted to humanity and its causes?

In my view, EDS is doing a great job. I found periodic webinars to be very useful. When it comes to knowledge, more is always better. Therefore, it will be nice to have even more tutorials/workshops/short courses on recent and emerging areas.

What are your suggestions and recommendations for those young professionals who may aspire to join EDS?

I strongly encourage all the young professionals working in the EDS field of interest to join the society. I am sure that they will never get disappointed.

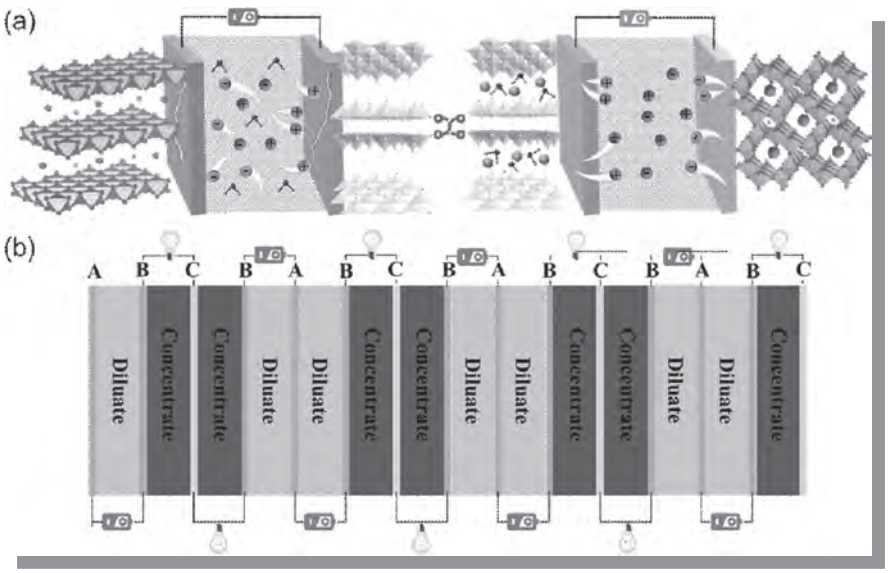
As an EDS Young Professional and a young researcher in the field, how do you consider the prospects of scientific research in this field for the progress of Humanity as a whole?

ED is a very mesmerizing field. Technologies that were unthinkable or were part of fascinating sci-fi films 2-3 decades back are now a reality. If we take a pause and introspect, we will find a huge contribution of electronic devices. In fact, they are so deeply diffused in every aspect of our lives that we sometimes take them for granted. I have no doubts in my mind that scientific research in this field will continue to fuel the further development of technologies that will improve quality of life while preserving the environment.

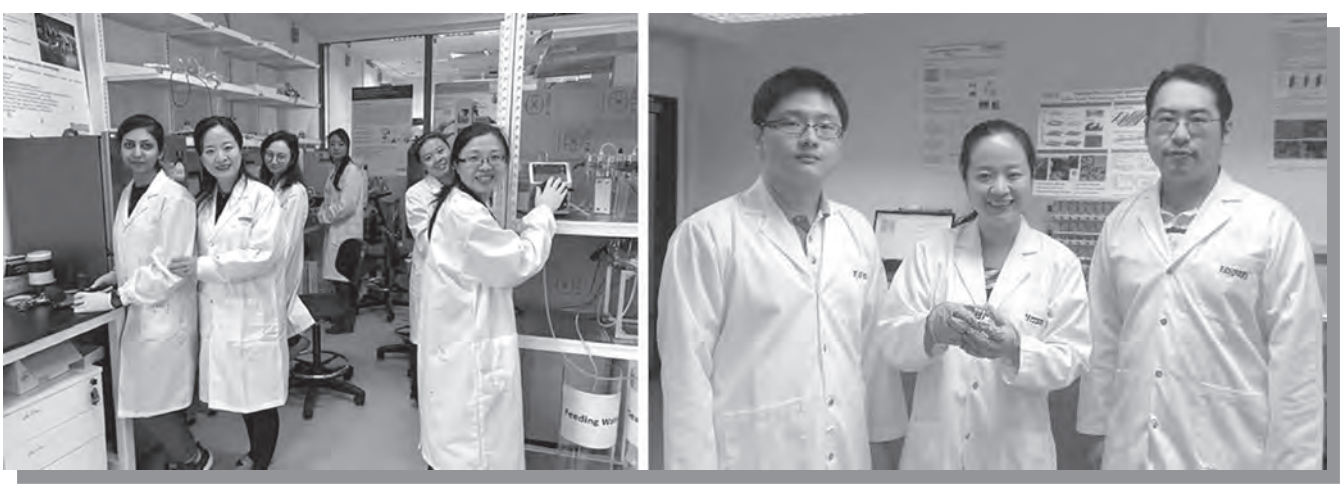
Dr. Harshit Agarwal is Assistant Professor at the Dept. of Electrical Engineering, Indian Institute of Technology (IIT), Jodhpur, India. He received the PhD degree from IIT-Kanpur in 2017. Before joining IIT-Jodhpur, he worked with the BSIM group as post-doc fellow cum Center Manager of Berkeley Device Modeling Center, University of California, Berkeley, USA for 3 years. Dr. Agarwal is highly fascinated with Nano-electronics. His research group at IIT-Jodhpur works in compact modeling, simulation and characterization of emerging transistor and memory devices for AI, IoT and neuromorphic applications. His other research interests include steep-slope devices, advanced CMOS architecture, 2D semiconductor devices and their compact modeling. Dr. Agarwal is a member of IEEE Electron Devices Society Compact Modeling Committee, is recipient of two IEEE best paper awards and featured thrice in IEEE EDS list of golden reviewers of EDL and TED. He has published one book and more than 50 articles in journals and conferences of international repute including IEDM, EDL, TED, etc.

Hui-Ying Yang—Material Sciences in Service of Society Development

Water and energy are intimately linked to greater economic development and advancement of society as a whole. Often, we are forced into a dilemma where one is prized over the other and times when energy is the victor, society is left in thirst. The main problem with modern desalination techniques is a high cost of energy which necessitates huge capital investments in infrastructure, technology, and manpower. However, Prof. Yang, a world-renowned materials scientist, and her team have managed to disrupt this through smart nanoscale fabrication techniques which have enabled the development of low energy desalinators. Her ideas for low energy desalinators are fundamentally built on sound concepts of electrochemistry and under her leadership, her research team pioneered the cross-disciplinary development of converting battery materials for use in water desalination and treatment, achieving a revolutionary desalination battery system which can perform both functions simultaneously. By utilizing redox-active (able to undergo chemical reactions with salt ions) electrodes, seawater behaves like an electrolyte and desalination can be analogously treated as charging a battery. No one-size-fits-all solution exists to solve problems of water security and energy concurrently, but the desalination battery comes close. By developing



Desalination process based on Nanomaterials



Prof. Hui-Ying Yang with her team members in a laboratory

energy-efficient desalinators, Prof. Yang has essentially untethered the relationship between energy and water and provided resource-scarce countries with an alternative solution to their water woes. To add on, these desalinators require little infrastructure and can be designed as a distributed water network system. The crux of these desalinators lies with the nanomaterials comprising it. Her team can fabricate nanomaterials with unique selectivity towards certain ions and a cascading series of these devices can substantially alter the composition of input water to fit agricultural, medical, industrial, or domestic needs. Her most recent accomplishment was adapting a variant of an electrochemical desalinator for dialysis treatment to regenerate used dialysates for portable dialysis systems. This technology was also developed for seawater mineral mining operations and her recent work showed how lithium metal ions can be extracted with high efficiency from seawater. Her futuristic vision is to achieve complete mitigation of water and energy problems through a combination of advanced nanofabrication and electrochemistry.

She has devoted her efforts to educate the next generation of young students and to multidisciplinary collaborative projects in practical applications of energy storage and water treatment. Her creative ideas, profound knowledge and extensive experience in water research led to existing economic benefits, significant educational impacts, enormous social benefits, and many intellectual properties/publications/books. In particular, she has been the UN Women Ambassador for Young Women in Science, Technology, Engineering and Math (STEM) in Singapore since 2014. At this position she has supported female scientists in many ways and motivated young girls to excel in science.

Professor Hui-Ying Yang did her Ph.D from Nanyang Technological University, Singapore in 2007. During 2008-2010, she was Lee Kuan Yew Fellow, School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore. She was Assistant Professor from 2010-2016 at Singapore University of Technology and Design and at present she is Programme Director, Nano-electronic Engineering and Design, Singapore University of Technology and Design. She has handled more than 25 major research projects with a cumulative worth of 15 million Singapore dollars. She has received more than 20 International and National Awards including SUTD Research Excellence Award, Singapore University of Technology and Design (2021); Fellow of Royal Society of Chemistry, UK (2020); IPS Nanotechnology Medal (Outstanding Nanotechnology Physics Research), Institute of Physics Singapore (2018); Outstanding Young Manufacturing Engineer Award, Society of Manufacturing Engineers (SME), USA (2014). Yang has published more than 270 peer-reviewed articles in many prestigious international journals, such as Nature Communications, Nano letters, ACS Nano, Advanced Materials and so on. From Google Scholar, her work has been cited over 12000 times. Her H-index is 61. She also has given 50+ invited talks and 100+ conference presentations. Yang is Singapore's all-time 32nd most prolific researcher for materials science publications in top international journals. Among Singapore's all-time top 40, her category normalized citation impact (CNCI) ranks 19th. She is among the youngest in the top 40 list.

Chapter News

IEEE EDS Malaysia COVID-19 Awareness Program

By Nurul Ezaila Alias, Nafarizal Nayan and Maizatul Zolkapli

The ED Malaysia Chapter conducted in July 2021 an online COVID-19 Awareness program. The sharing session was moderated by Dr. Nurul Ezaila Alias from Universiti Teknologi Malaysia (UTM). The panel speakers were Dr. Sakinah Binti Kamarul Bahrin from Klinik Anda, two COVID-19 survivors, Dr. Hazliza Hassan from Universiti Tun Hussein Onn Malaysia (UTHM), and Ir. Ts. Dr. Maizatul Zolkapli from Universiti Teknologi MARA (UiTM). The program received an overwhelming attendance of 120 participants from all over the country.

Panelists for the IEEE EDS Malaysia COVID-19 Awareness Program

Bridging Digital Inequalities Amongst the Urban Poor Communities in Malaysia

By Maizatul Zolkapli

A project titled "Bridging Digital Inequalities Amongst the Urban Poor Communities in Malaysia" led by IEEE EDS Malaysia member Dr. Maizatul Zolkapli, with two other members Assoc. Prof. Dr. Ahmad Sabirin Zoolfakar and Dr. Aliza 'Aini Md Ralib received a US $5,000.00 fund from IEEE HAC/SIGHT. This project aims to equip selected urban poor category families from Sekolah Menengah Kebangsaan Seksyen 18, Shah Alam, with digital application devices and skills to ensure that these students can participate in online learning in preparation for the March 2022 exams for Malaysian Certificate of Education. In total, 21 units of Samsung Galaxy A7Tab were donated to the school on 15 September 2021. Besides that, the students were also provided with a STEM kit to be used during the online STEM workshop. During the workshop, the students will be guided and trained by mentors from International Islamic University Malaysia to use the devices and related applications. Training modules, step-by-step manuals and handouts will be developed by the team to assist the students in their digital learning experience. This program corresponds to IEEE's effort in mobilizing member grassroots' humanitarian activity for sustainable development projects that address local challenges of the COVID-19 situation in the members' communities.

Dr. Maizatul Zolkapli handed over 21 units of Samsung Galaxy A7 Tablet to the school principal of Sekolah Menengah Kebangsaan Seksyen 18 Shah Alam

STEM Outreach: Let's Code with Microbit

By Aliza 'Aini Md Ralib and Rosminazuin Ab Rahim

In the spirit of promoting the advancements of technology to the students, Fun with STEM (Let's Code with Microbit) was an educational and community service event organized by IEEE EDS Malaysia Chapter in collaboration with Perintis Youth International Islamic University Malaysia (IIUM) Chapter. The online program was sponsored by IEEE Region 10 Educational Activities Fund under local initiatives and IIUM MYSTEM Ambassador. The event was aimed to cultivate the Sekolah Berasrama Penuh Integrasi Gombak students' interest in STEM and robotics through Microbit Workshops.

The Microbit kits that were given to the students

Twenty Microbit kits were delivered to the participants. The modules were designed by referring to IEEE resources such as TryEngineering. The engagement of IEEE EDS members with the local community was cultivated through this program.

ED Malaysia Chapter Research Grant Writing Workshop and Membership Drive

By Norhayati Soin and Maizatul Zolkapli

The ED Malaysia Chapter organized a membership drive program in conjunction with the online workshop on Research Grant Writing. The workshop which was held on 8 September 2021 by Prof. Dr. Norhayati Soin focuses on training of lecturers on preparing international and local research grant proposals. Prof. Norhayati started off with sharing the tips and tricks in writing proposals and later followed by the actual proposal writing by the participants. Participants get the opportunity to revise their proposal with the trainer towards the end of the session. The event was hosted by the Faculty of Health Science, Universiti Kebangsaan Malaysia (UKM). During the discourse, the speaker introduced the IEEE Electron Devices Society to the participants. Many were interested to get to know more about IEEE and EDS.

~Sharma Rao Balakrishnan, Editor

Regional News

North America (Regions 1–7)

DRC 80th Device Research Conference

For eight decades, the Device Research Conference (DRC) has brought together leading scientists, researchers, and students to share their latest discoveries in device science, technology, and modeling. Notably, many of the first public disclosures of key device technologies were made at the DRC. **This year marks the 80th anniversary of the DRC—the longest running device research meeting in the world.** The high-caliber technical sessions will be highlighted by plenary talks and invited talks by international research pioneers and leaders behind modern electronic technology. Dates and Location: 26–29 June 2022, The Ohio State University, Columbus, Ohio. Learn more at www.mrs.org/drc-2022.

~ Michael Adachi, Editor

Latin America (Region 9)

Centro Universitario FEI ED Student Branch Chapter—EDS (Virtual) Brazil Mini-Colloquium and 35th Symposium on Microelectronics Technology and Devices—SBMicro2021

—by Marcelo Antonio Pavanello, Michelly de Souza and Flavio Enrico Bergamaschi

On 23 August, the Centro Universitario FEI ED Student Branch Chapter organized the 2021 EDS (Virtual) Brazil Mini-Colloquium. It is an annual event that precedes the Symposium on Microelectronics Technology and Devices. This year the Mini-Collolloquium consisted of 5 presentations, including 4 given by IEEE EDS Distinguished Lecturers, covering state-of-the-art topics in micro/nanoelectronics, including modeling of nanosheets, heterogeneous integration, neuromorphic computing, quantum computing, and 2D materials:

- Dr. Yogesh Chauhan, from IIT Kanpur, India, "*Modeling and Simulation of FinFET and Nanosheet Transistors for Advanced Technology Nodes*";
- Dr. Mario Lanza, from KAUST, Saudi Arabia, "*Hexagonal boron nitride based electronic devices and circuits: status and prospects*";
- Dr. Merlyne De Souza, from University of Sheffield, UK, "*From CMOS to Neuromorphic Computing, with a peek into the future*";
- Dr. Robert Bogdan Staszewski and Dr. Elena Blokhina, from University College Dublin, Ireland, "*Quantum Computing in Nanoscale CMOS using Position-Based Charge Qubits*"
- Dr. Mukta Farooq, from IBM Research, USA, "*Heterogeneous Integration for AI Architectures*".

Because of the outbreak restrictions, the Mini-Colloquium was held virtually. Also, it was broadcasted live via Brazilian Microelectronics Society social media to broaden the audience. Every presentation of the Min-Colloquium received more than 60 participants, from undergraduate and graduate students as well as professors and researchers, mainly Brazilians. Also, several unregistered people from several countries attended the Mini-Colloquium via social media.

Immediately after the Mini-Colloquium, from 24–27 August 2021, the 35th Symposium on Microelectronics Technology and Devices (SBMicro 2021) was held virtually as well. SBMicro is the largest conference in Latin America in the field of micro/nanoelectronics, covering topics such as fabrication technology, sensors, modeling, device characterization and photonics. This year, 32 papers were selected by the program committee to be presented orally. Four invited presentations were also delivered during the Symposium: Dr. Meng Tao (Arizona State University), Dr. Muhammad Mustafa Hussain (University of California), Dr. Robert Clark (TEL Technology Center America), and Dr. Valeriya Kilchytska (UCLouvain). About 350 people registered for the conference this year. The conference was technically cosponsored by the IEEE EDS and its proceedings are available in the IEEE Xplore Digital Library.

~ Paula Agopian, Editor

Europe, Middle East & Africa (Region 8)

2021 International Conference on Microelectronics (MIEL)

—by Danijel Danković and Vojkan Davidović

The 32nd International Conference on Microelectronics (MIEL 2021) was held virtually on 12–14 September 2021. The conference was organized by the Faculty of Electronic Engineering, University of Niš and the IEEE

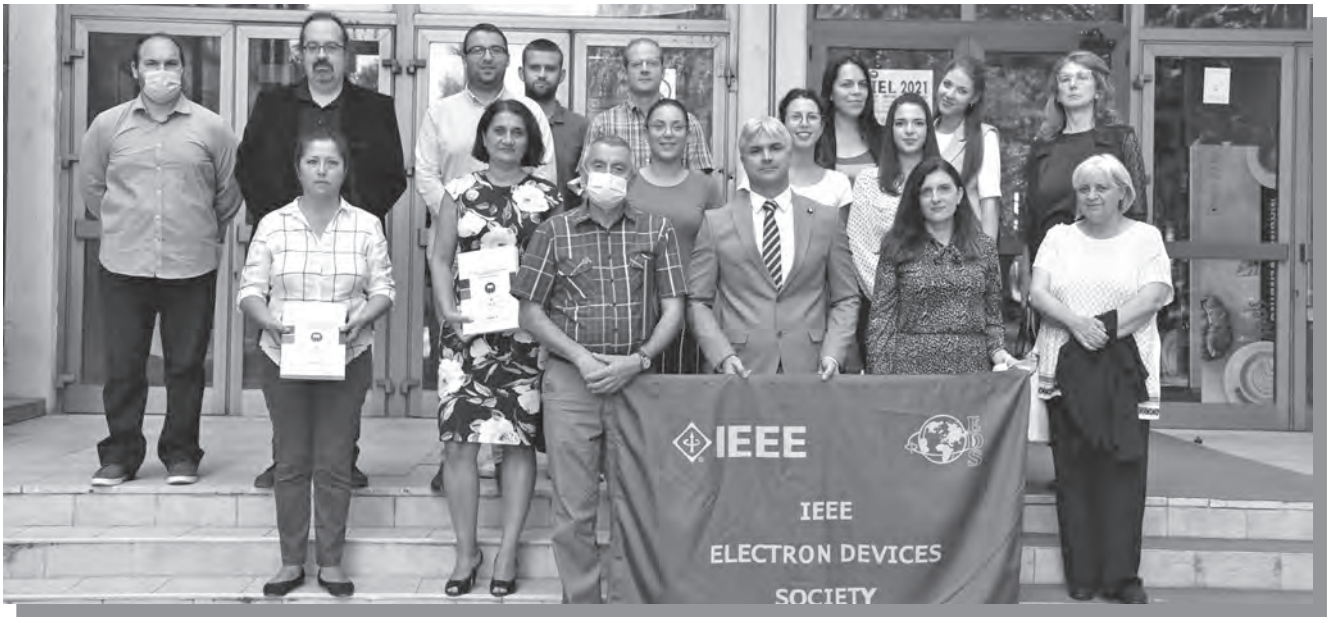
Serbia and Montenegro Section—ED/SSC Chapter in cooperation with the Serbian Academy of Sciences and Arts—Branch in Niš, under the co-sponsorship of the IEEE EDS, and under the auspices of Serbian Ministry of Education, Science, and Technological Development and of Serbian Society for Electronics, Telecommunications, Computing, Automatics and Nuclear engineering (ETRAN). The Conference was co-chaired by Prof. Danijel Danković and Prof. Vojkan Davidović. Due to the unprecedented health, travel and social distance restrictions imposed in Serbia and all over the world, as a result of the COVID-19 pandemic, all participants were invited to join a "Virtual MIEL 2021" digital platform.

The Mini-Colloquium on "Nanoelectronics and nanodevices" (http://miel.elfak.ni.ac.rs/uploads/ConferenceProgramme.pdf), was held on 12 September and attracted a lot of interest of both domestic and foreign participants. In this session 6 papers were presented. It was an excellent introduction to the main technical program of MIEL Conference, which consisted of Plenary Session and four regular Sessions: Device Physics and Characterization, Device Technology and Characterization, Circuit and System Design and Testing, and Devices and Systems in Radiation Environment. The participants, 71 domestic and 175 foreign, came from 26 different countries. The total of 15 keynote invited papers and 76 regular contributions were presented. The conference proceedings (401 pages) were published through the IEEE Conference Publication Program and are available on IEEE Xplore.

The keynote invited speakers were: R. Singh (Clemson University, SC, USA), M. Spasenović (University of Belgrade, Serbia), L. Filipovic (Universitat Wien, Austria), A. Y. Nikiforov (NRNU MEPhI, Russia), M. Krstić (IHP—Leibniz Institut für innovative Mikroelektronik, Frankfurt, Germany), D. Danković (University of Niš, Serbia) and A. Jaksic (Tyndall National Institute, Ireland).

Based on evaluation of the quality of the papers and presentations, four Best Paper Awards were presented. The Best Paper Award was given to E. Bender and J. B. Bernstein (Ariel University, Israel) for the paper "Self-heating Effects Measured in Fully Packaged FinFET Devices". The Best Paper Award in Special Session "Devices and Systems in Radiation Environment" was given to S. Simoglou, C. Georgakidis, I. Lilitsis, C. Sotiriou, M. Andjelkovic, and M. Krstic (University of Thessaly, Greece and University of Potsdam, Germany) for the paper "Single Event Transients Generation and Propagation Flow using Commercial EDA Tools". The Best Student Paper Award went to A. Kovačević, M. Potrebić, and D. Tošić (University of Belgrade, Serbia) for the paper "Sensitivity Analysis of Possible THz Virus Detection Using Quad-Band Metamaterial Sensor". In addition, *FACTA UNIVERSITATIS, Series Electronics and Energetics* Journal awarded the paper "Hot Carrier Degradation in Triple-RESURF LDMOS with Trenched-Gate" by A. Houadef and B. Djezzar (University of Boumerdés (UMBB), Algeria and Centre de Développement des Technologies Avancées (CDTA), Algeria).

This year's Conference was organized in the honor of the academician Ninoslav Stojadinovic´, who passed away from the COVID-19 virus. He was the former EDS/SSC Chapter Chair, the chairman of numerous conferences, editor of many scientific journals, well



Live attendees of the event "MIEL 2021 dedicated to the academician Ninoslav Stojadinović" with both Conference Chairs standing in the front row: Prof. Vojkan Davidović (left) and Prof. Danijel Danković (right)

known and respected professor, colleague, and a friend of many people around the World. His contribution to this Conference, and many others, will not be forgotten. On Monday, 13 September at 1 PM, at the Faculty of Electronic Engineering, in the presence of his closest associates, a seminar entitled "MIEL 2021 dedicated to academician Ninoslav Stojadinovic´", was held live (https://www.youtube.com/watch?v=tpQxhkhBU10). In honor of Professor Stojadinovic´, a documentary film about his life and work was shown during the event for the first time (now available on https://www.youtube.com/watch?v=Y9zHeTj3zV4&t=12s). The MIEL participants had the opportunity to watch this video as well.

Due to the fact that the Conference was held online, the traditional hospitality accompanying the MIEL editions could not be shown. This special charm adds to very positive impressions the participants bring from the conference and is one of the reasons why one rarely attends MIEL just once. One who comes will almost certainly come again. The hope remains that the next IEEE 33rd International Conference on Microelectronics will be held live and that the Faculty of Electronic Engineering will be in position to welcome old and new friends at MIEL 2023.

Report on the IEEE EDS Mini-Colloquium on Nanoelectronics and Nanodevices, Niš, Serbia

—by Danijel Danković and Vojkan Davidović

The IEEE EDS sponsored the Mini-Colloquium "Nanoelectronics and Nanodevices" (MQ) which was held on Sunday, 12 September, on a "Virtual MIEL 2021" digital platform. This MQ was organized in conjunction with 32nd International Conference on Microelectronics—MIEL 2021, giving great opportunity to foreign participants to be updated with novelties in this modern scientific field. Detailed information on the EDS MQ can be found at, http://miel.elfak.ni.ac.rs/uploads/Conference Programme.pdf.

The event began with a welcome and opening address by Danijel Danković and Vojkan Davidović, followed with six presentations given by leading experts in the field, including IEEE EDS Distinguished Lecturers:

- "Past and future of micro-/nano-electronics" (Hiroshi Iwai, *National Yang Ming Chiao Tung University, Hsinchu, Taiwan*),
- "On the CMOS Device Downsizing, More Moore, More than Moore, and More-than-Moore for More Moore" (Hei Wong, *City University of Hong Kong, Hong Kong*),
- "Silicon Based Quantum Computers" (Shunri Oda, *Tokyo Institute of Technology, Japan*),
- "Multi-Dimensional Integrated Circuit (MD-IC): Enhancing Functionality In Multi-Faceted Way For Standalone Internet of Things (IoT) Devices" (Muhammad Mustafa Hussain, *KAUST, Saudi Arabia*),
- "Physical and Technological Limitations of NanoCMOS Devices to the End of the Roadmap and Beyond" (Simon Deleonibus, *CEA/LETI, France*), and

"Oxide Thin Film Transistors and Device Circuit Interactions" (Arokia Nathan, *Cambridge Touch Technologies, UK*).

The audience of about 130 people received the MQ very well, in terms of organization, technical quality of the contributions, and opportunities for discussion. The virtual interaction between the lecturers and the audience was very lively, and interest in the presented research was very high. A confirmation of the interest is the number of views of lecture recordings. The viewers were mainly MIEL 2021 Conference participants, but also local students, professors, and colleagues from all over the World.

The 15th International Seminar on Power Semiconductors (ISPS 2021)

—by Vítězslav Benda

The 15th ISPS was held in Prague, 26–27 August 2021. This conference provides a forum for technical discussion in the area of power semiconductor devices and their applications. It is a small conference with the special flair of an atmosphere of searching for deeper insight and intensive discussion. According to the current COVID situation, this year ISPS was organised in a hybrid form (25 participants attended in person, 10 participants attended online). The Conference was organised by IET Czech Network in co-operation with the IEEE Czechoslovakia Section, and was co-sponsored by the Faculty of Electrical Engineering, Department of Electrotechnology, Czech Technical University in Prague (CTU). Prof. Vítězslav Benda from CTU was the Conference chairman. Prof. Gerhard Wachutka from Technical University of Munich was the chairman of the International Program Committee. The Conference co-chairmen were Prof. Nando Kaminski, University of

The 15th ISPS attendees during a session

Bremen, Prof. Josef Lutz, Chemnitz University of Technology, and Prof. Sankara N. Ekkanath Madathil, University of Sheffield.

Papers oriented on current problems in the field of power semiconductors were presented in the following sessions: "Robustness, Ruggedness and Efficiency", "Degradation and Defects in Wide-Gap Power Devices", "Packaging and Integration", "Integration of Power Devices", and "Measurement and Testing Techniques". The opening invited lectures were given by H.-J. Shulze et al. from Infineon: "Important Criteria for the Short-Circuit Capability of IGBTs", and Shiori Idaka from Mitsubishi Electric Corporation, Tokyo, Japan: "New Packaging Concepts: Bridging Devices and Applications". Papers presented at the ISPS 2021 are available online on the website https://technology.fel.cvut.cz/en/isps/previous_years/isps21proceedings/isps-2021-contents-of-proceedings/. All participants appreciated both the scientific level and the social program of the Conference.

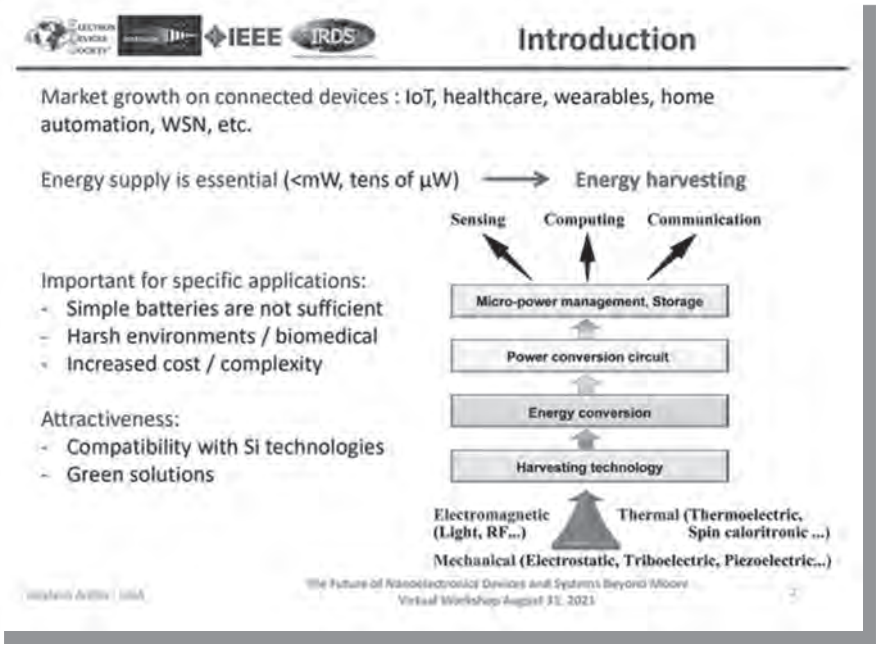
The 16th ISPS is scheduled to take place at the end of August 2023.

~Marcin Janicki, Editor

The Future of Nanoelectronics Devices and Systems Beyond Moore Workshop

—by Pascale Caulier and Francis Balestra

The Future of Nanoelectronics Devices and Systems Beyond Moore Virtual Workshop, supported by IEEE EDS, was held on 31 August 2021 and was devoted to the update of the European contribution to the IRDS Roadmap in the field of **More than Moore, Beyond CMOS and Emerging Materials**. The main challenges, most promising technologies, needed research efforts and possible applications were presented in the following sessions by renowned EU experts.



Introduction of the European and International Roadmaps

Francis Balestra—CNRS-G_INP, Director of the SINANO Institute, Chair of EDS France, gave in the introduction some information on the European and International Roadmaps.

The first session on **Beyond CMOS and Emerging Materials** included four presentations: ***Trends in Beyond CMOS*** (by Clivia Sotomayor -Torres—ICN2 and Jouni Ahopelto—VTT), ***2D semi-metal to semiconductor transition devices and/or doping of 2D materials*** (by Farzan Gity—Tyndall), ***GeSn/Ge vertical nanowire GAA FETs*** (by Qing-Tai Zhao—FZJ) and ***Flexible electronics with 2D materials*** (by Zhenxing Wang—AMO GmbH).

The second session covering the topic **New IRDS More than Moore Roadmap**, launched last year with a White Paper, was presented by Mart Graef—TU Delft, Chair of this IRDS new International Focus Team. He introduced the content of the More than Moore Roadmap, highlighted the upcoming steps and introduced 4 sub-chapters:

Energy Harvesting for Autonomous Systems sub-chapter, chaired by Gustavo Ardila (UGA) who presented the summary of the IRDS Energy Harvesting for Autonomous Systems White Paper and introduced 2 complementary talks on ***Energy sustainability problems of IoT***

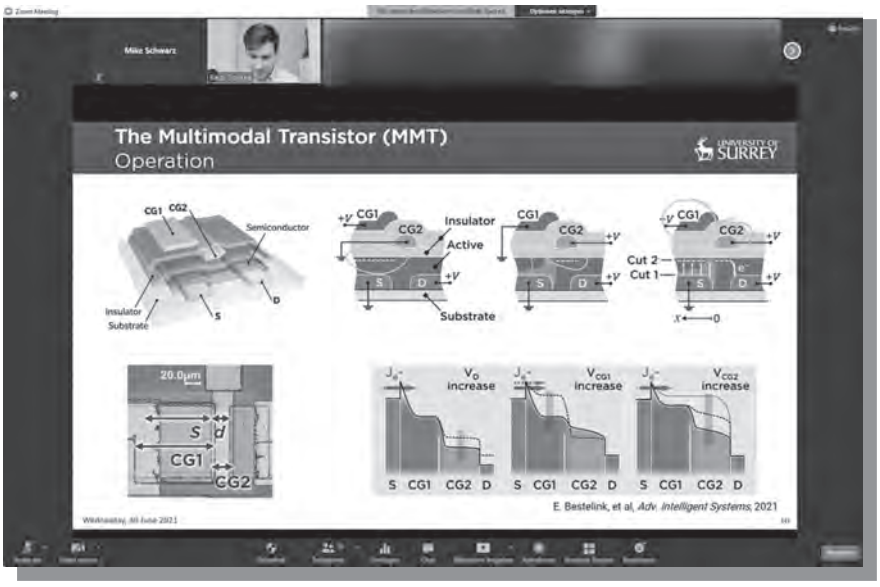
networks (by Maciej Haras—CEZAMAT) and ***Contribution of triboelectricity for kinetic energy harvesting using electrostatic transduction*** (by Philippe BASSET—ESIEE).

Smart Sensors, chaired by Alan O'Riordan (Tyndall) who presented the summary of the IRDS Smart Sensors White Paper and then 3 complementary talks on ***Sensing at the Edge: Challenges and Opportunities*** (by Adrian Ionescu—EPFL), ***Smart Sensors and Systems for environment and human exposure monitoring*** (by Carmen Moldovan—IMT) and ***Micro and nanotransducers for the Internet of Things*** (by Cosmin Roman—ETHZ).

Smart Energy, chaired by Gaudenzio Meneghesso (UniPD) who presented the summary of the IRDS Smart Energy White Paper and 2 complementary talks on ***Materials and substrates for future power devices*** (by Joff Derluyn—Soitec BU EpiGaN) and ***Smart power devices based on Wide Bandgap semiconductors*** (by Mikael Östling– KTH).

Flexible/Wearable Electronics Roadmap, chaired by **Benjamin Iñiguez (URV)** who presented the Summary of the IRDS Flexible/Wearable Electronics White Paper and then 2 complementary talks on ***Schottky barrier and organic devices for neuromorphic circuits*** (by Laurie Calvet—CNRS—Université Paris Saclay) and ***New strategies for sustainable electronics*** (by Elvira Fortunato—UNL).

All presentations are available on the SINANO Institute website: http://www.sinano.eu/the-future-of-nanoelectronics-devices-and-systems-beyond-moore-workshop/.



Prof. Radu Sporea introducing the operation principle of MMT

Joint Graduated Students Meeting at URV and 5th Symposium on Schottky Barrier MOS (SB-MOS) Devices

—by Mike Schwarz and Benjamin Iniguez

The Graduated Students Meeting on Electronic Engineering at the Department of Electronic, Electrical and Automatic Control Engineering of the University Rovira i Virgili (URV) and 5th Symposium on Schottky Barrier MOS (SB-MOS) Devices were held from 30 June to 2 July 2021. This was the first joint R&D event between the URV and Symposium of SB-MOS Devices organized by the Department of Electronic, Electrical and Automatic Control Engineering of the University Rovira i Virgili (Tarragona, Spain) and the EDS Spain and Germany Chapters (chaired by Profs. Benjamin Iñiguez and Mike Schwarz, respectively). The Graduate Students Meeting on Electronic Engineering was chaired by Prof. Josep Ferré-Borrull (URV).

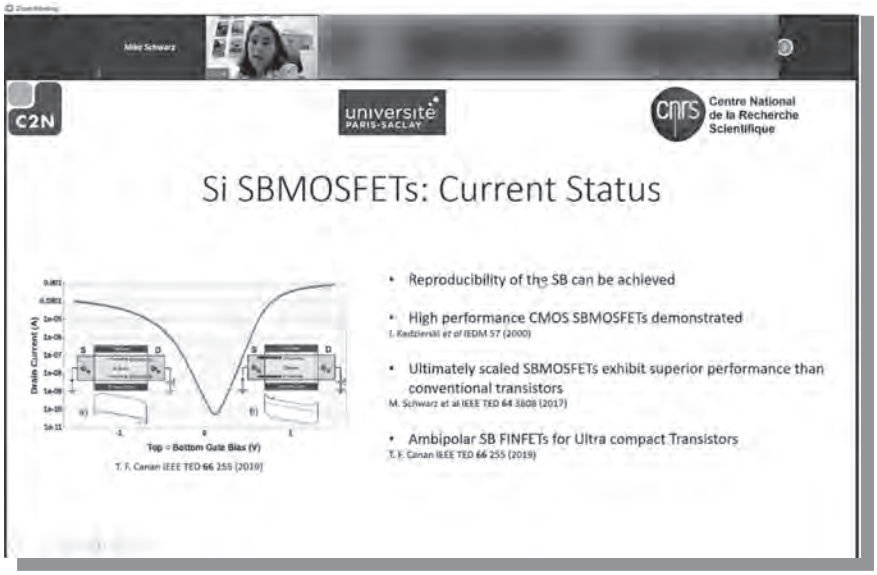
In its time frame three distinguished lectures were also given (see additional reports in Regional News). One by Prof. Gana Nath Dash from Sambalpur University on **"Tunneling Graphene FET"**, one by Prof. M.K. Radhakrishnan from NanoRel, Singapore on **"Revisiting a Birth which Impacted Humanity in Seven Decades"**, and one by Prof. Adam Skorek from the Universitédu Québec à Trois Rivières, Canada, on **"Biofields and bioelectronics on Human-Machine interfaces"**.

Due to the still ongoing COVID-19 pandemic the event was organized virtually via the Zoom and MS Teams Platforms. All presentations were given live in this virtual format. The event was sponsored by URV, THM, the EDS Spain and Germany Chapter. The event was attended by approximately 100 participants during the three days.

The event began with a distinguished lecture by Prof. Gana Nath Dash. Afterwards, the Symposium on Schottky Barrier Devices was opened with a short "celebration" of the 5th birthday.

The first presentation entitled "Germanium nanosheet and nanowire transistor technologies for beyond CMOS applications" was given by Prof. Walter Weber from Vienna University. He focused on Al/Ge/Al Transistors with negative differential resistance (NDR) characteristics, Ge based Reconfigurable Nanowire Transistors and on NDR Mode Reconfigurable Transistors. Prof. Weber discussed broadly various results.

The next talk was given by Prof. Radu Sporea from University of Surrey on the topic "Evolving contact-controlled thin-film transistors". He started with some premise and introduced the multimodal transistor (MMT) with its physical background and functionality. Afterwards, he showed various potential applications e.g. analog memory, digital to analog converters, and many more.



Dr. Laurie Calvet offers the current status of Silicon Schottky Barrier MOSFETs

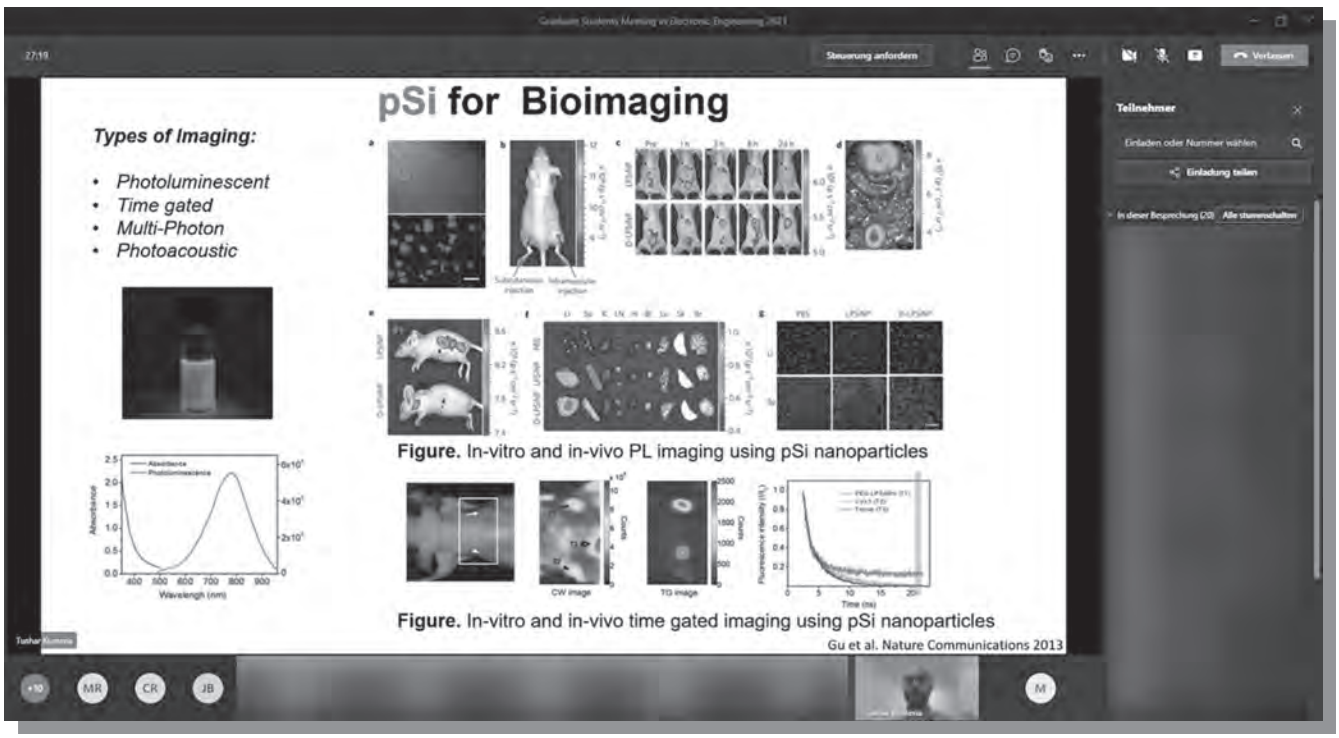
After a coffee break, the session was continued by a presentation from PhD candidate Christian Römer from THM University of Applied Sciences. He presented a collaborative work with namLAB Dresden "Compact Modeling of Dually-Gated Reconfigurable Field-Effect Transistors". He was showing the evolution of a compact modeling approach for dual-gated Reconfigurable Field-Effect Transistors to a closed-form and physics-based DC compact model with the latest results and comparisons with experimental data.

The first day was closed by Dr. Laurie Calvet with a talk on "The Schottky barrier transistor in all its forms". She offered an introduction into the basic principles and a wrap up of the history. Afterwards, Dr. Calvet presented the state of the art and discussed the Schottky barrier transistors in all their forms.

The second day continued with the Graduated Students Meeting opened by Prof. Jose Ferre Borrul from URV. The first presentation was a DL by Prof. M.K. Radhakrishnan from NanoRel, Singapore. Prof. Radhakrishnan gave an outstanding review on the last 115 years of device evolution and offered historical photos and documents.

After a short break Dr. Pierrick Clément from EPFL presented a talk on "Integration of nano-engineered carbon nanotube hybrids on MEMS for (bio)sensing application". Interesting discussions on carbon nanotubes vs. graphene sheets followed.

The last talk of the second day was given by Prof. Adam Skorek from Université Québec on "Biofields and bioelectronics in Human-Machine interfaces". It was a very interesting presentation from a worldwide perspective of some modern research works with their results impacts, and completed



Prof. Tushar Kumeria offering the properties of porous silicon *for bioimaging*

by the lecturer's experiences and guidelines for the future. Some practical examples were explained, stimulating the audience to various scientific as well R&D activities in this promising area. Besides, Prof. Skorek made an additional presentation about the benefits of becoming a Student Member of IEEE, and in particular EDS.

The third day began with an excellent talk by Prof. Tushar Kumeria from University of New South Wales, Australia on "Porous nanomaterials for biomedical applications". He gave details and many applications on photoacoustic properties of porous silicon particles for bioimaging.

After the presentation, a session for PhD candidates followed. The first work was presented by Sara Martínez de Cripán from URV on "Machine learning-based retention time prediction of trimethylsilyl derivatives of metabolites". The investigations offered the limitation of the machine learning (ML) algorithms by the limited amount of available data.

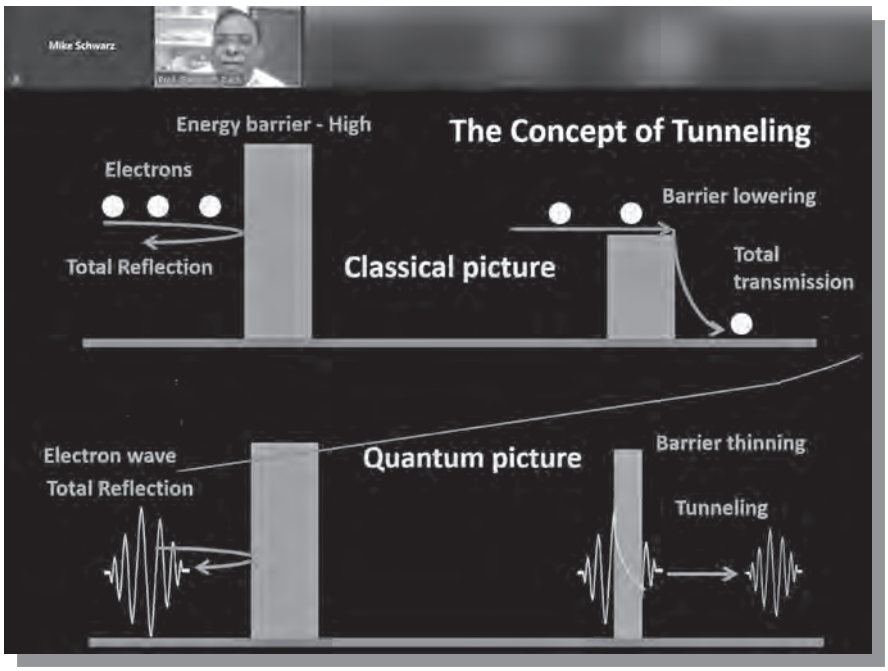
The presentations continued with a talk entitled "Optical Platform to Analyze a Model Drug-Loading and Releasing Profile Based on Nanoporous Anodic Alumina Gradient Index Filters" by Pankaj Kapruwan from URV. The session was finalized by Xavier Genaro from URV with a presentation on "Contribution to the Development of a Multifrequency Energy Distribution System for Battery Charging in Electric Vehicles".

After a break the final talk of the GSM was delivered by Prof. Christoph Bookmeyer entitled "Post-ionization techniques in MALDI mass spectrometry imaging".

Gana Nath Dash—Distinguished Lecture on Tunneling Graphene FET

—by Mike Schwarz

The distinguished lecture on **"Tunneling Graphene FET"** was held in the timeframe of the virtual joint event of the Symposium on Schottky Barrier devices and the Graduated Students Meeting on Electronic Engineering at the Department of Electronic, Electrical and Automatic Control Engineering of the University Rovira i Virgili (URV), Tarragona, Spain on 30 June 2021. It was organized by the EDS Spain and Germany Chapters and co-sponsored by the NanoP from THM—University of Applied Sciences and URV. The DL was attended by 15 IEEE participants, as well as other non-IEEE members.



Prof. Gana Nath Dash introducing the tunneling concept

The distinguished lecture of Prof. Dash from Sambalpur University gave an overview and introduction to Moore's law and technology revolution as well as the principle of CMOS scaling and the resulting issues. Afterwards, he introduced the mechanism of tunneling and its effect on operation of devices (FETs). The emergence of graphene with its relevant properties was followed by development of graphene-based devices. Prof. Dash continued with Tunneling Graphene FETs and introduced the lateral tunneling and the vertical tunneling architectures. The DL was concluded with addressing the Graphene Nanoribbon Tunneling FETs (GNRTFETs).

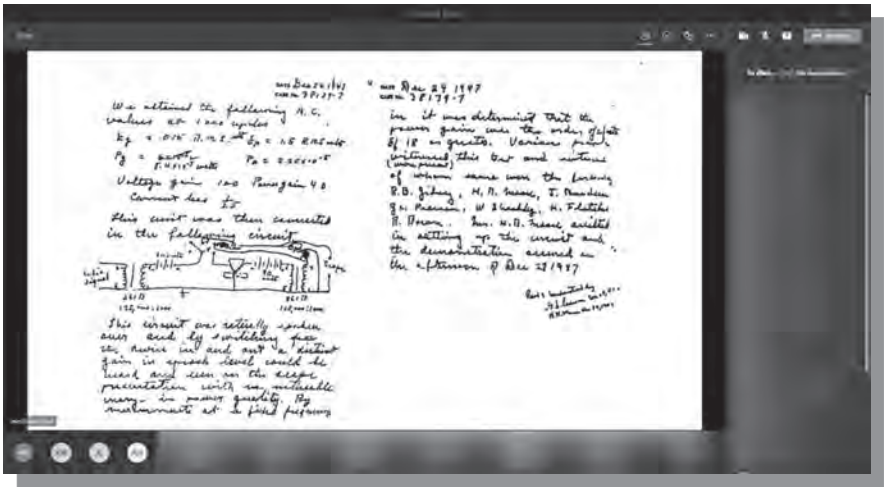
M.K. Radhakrishnan Distinguished Lecture on "Revisiting a Birth which Impacted Humanity in Seven Decades"

—by Mike Schwarz

The distinguished lecture on **"Revisiting a Birth which Impacted Humanity in Seven Decades"** was held on 1 July 2021. The event was organized jointly by the EDS Spain and Germany Chapters and co-sponsored by the NanoP from THM—University of Applied Sciences, Mittelhessen, Germany, and by URV. Among the attendees of the DL there were 20 IEEE members.

Prof. Radhakrishnan from NanoRel, Singapore, serves currently as the EDS Secretary. He gave an outstanding review on the last 115 years of the electronic device evolution and offered historical photos and documents that many of the participants have never seen.

Prof. Radhakrishnan guided the participants from the device evolution story towards veracity in device progression including reliability and its challenges. Afterwards, he concluded his talk with thoughts on the impact of technology on society and



Prof. Radhakrishnan showing the notes of Shockley, Brattain, Bardeen, and others from 1947

humanity. Topics such as transistors and neurons—a number game as well as advancements in society and human interactions were discussed.

Virtual EDS Mini-Colloquium on TFT for Emerging Technologies

—by Benjamin Iniguez

A Virtual EDS Mini-Colloquium (MQ) on TFT for Emerging Technologies was held on 2 September 2021. It was organized jointly by the ED Spain Chapter and the ED United Kingdom & Republic of Ireland Chapter. The Chair of this MQ was Prof. Benjamin Iñiguez (University Rovira I Virgili, Tarragona, Spain). Prof. Arokia Nathan (Darwin College, University of Cambridge, UK) was the Co-Chair of this event.

This Mini-Colloquium was a satellite event of the 12th CAD TFT Workshop (3 September 2021), organized by the University of Cambridge, Silvaco Europe Ltd. (UK) and the ED United Kingdom & Republic of Ireland Chapter.

The Mini-Colloquium on TFT for Emerging Technologies included 13 virtual talks, with five of them conducted by EDS Distinguished Lecturers.

Several topics related to the physics, technology, characterization, modeling and applications of different types of TFTs were addressed by the speakers.

Dr. Takayuki Ikeda (SEL Co., Japan) talked about "Circuit design with crystalline oxide semiconductors". Prof. Yanli Pei (Sun Yat-Sen University, Guangzhou, China) made a presentation about a "Biosensor based on In_2O_3 thin film transistors". Prof. Kai Wang (Sun Yat-Sen University, Guangzhou, China) targeted "IGZO TFT-based Addressing and Readout Circuits for Hybrid LAE-CMOS Interfacing". Prof. H. Ma (Chinese Academy of Sciences, Suzhou, China) gave a talk entitled "Active matrix digital microfluidics chip with diversified pixel designs".

Prof. Paul R. Berger, (Ohio State University, USA and Tampere University, Finland) gave a talk as EDS Distinguished Lecturer about "Fully Printed Flexible Electronics: Low Voltage TFTs and Novel NDR devices". Prof. Luisa Petti (Free University of Bozen-Bolzano, Italy) conducted a lecture on "Flexible Amorphous Oxide Thin-Film Transistors for Analog Circuits and Systems". Prof. Benjamin Iñiguez (University Rovira I Virgili, Spain), as EDS Distinguished Lecturer, targeted "Compact DC and AC a-Si:H TFT modeling including parasitic capacitances".

After a break, Prof. Arokia Nathan (Darwin College, University of Cambridge, UK), as EDS Distinguished Lecturer, gave a talk about "Thin Film Transistor Architectures for Advanced Signal Processing". Prof. Ravinder Dahiya (University of Glasgow, UK) made a presentation on "Soft Electronic Skin for Robotics". Prof. John Kymissis (Columbia University, NY, USA), as EDS Distinguished Lecturer, addressed "The impact of contact selection on performance in organic FETs". Prof. Sanjiv Sambandan (University of Cambridge, UK) talked about "Self-Healing of Thin Film Transistor Circuits". Prof. Jerzy Kanicki (University of Michigan, USA) conducted a lecture about "Electrical Instabilities of Amorphous Metal Oxide Semiconductors." Finally, Dr. Samar Saha, as EDS Distinguished Lecturer, targeted "Thin Film Transistors for Ubiquitous Flexible Electronics".

International Conference on IC Design and Technology 2021

—by Wenke Weinreich and Mike Schwarz

Today, the mutual optimization of design and technology provides a key advantage in the highly competitive semiconductor market. Traditionally, when developing integrated circuits (IC), their design and technology were considered and developed separately. Looking to the future, this is no longer appropriate.

For the 18th time, the "International Conference on IC Design and Technology (ICICDT)" provided a forum for engineers, researchers, graduate students and professors to cross the boundary between design and technology. It provides an important international platform for interaction and collaboration of IC design and technology and is sponsored by the Institute of Electrical and Electronics Engineers (IEEE).

The organizer of last year's ICICDT, which for the first time was held in a virtual format from 15–17 September 2021, was the Fraunhofer Institute for Photonic Microsystems IPMS in Dresden, Germany. "We are proud to have hosted this year's ICICDT," says Fraunhofer IPMS deputy director

and conference co-chair Dr. Wenke Weinreich. "Even though we were unable to welcome the total of around 90 international guests in person due to the pandemic situation, exciting lectures and workshops awaited the participants, offering plenty of room for interaction and exchange."

The one-day tutorial program on plasma-induced damage, GaN power devices, neuromorphic computing for edge AI, and large-scale silicon photonic MEMS switches was followed by two days of technical presentations and workshops. An entertaining social program accompanied the conference, including a virtual city tour around Dresden. Keynotes were presented by Dr. Abu Sebastian from IBM Research (Zurich, Switzerland) entitled "In-memory computing: The next frontier in deep learning acceleration?", by Dr. Chidi Chidambaram from Qualcomm (Albany, New York, US) on "Semiconductor challenges in realizing the full benefit of 5G mm wave and extending the roadmap into 6G", by Dr. Mirko Sanzaro from Toshiba Europe/Cambridge Research Laboratory (UK) on "A photonic integrated quantum communication system", and by Dr. Alvin Leng Sun Loke from NXP Semiconductors (San Diego, California, US) on the topic of "Driving Automotive ICs into Advanced CMOS".

Besides four tutorial were given by Andreas Martin (Infineon Technologies AG, Germany) on "Plasma-induced damage (Process and device design)", Dr. Matteo Meneghini (University of Padova, Italy) on "GaN power devices: from technology to reliability challenges", Dr. Thomas Kämpfe (Fraunhofer IPMS, Germany) on "Neuromorphic Computing for Edge AI" and by Prof. Ming Wu (Berkeley University, USA) on "Large-Scale Silicon Photonic MEMS Switches".

The next ICICDT will be held in 2023.

~ Mike Schwarz, Editor

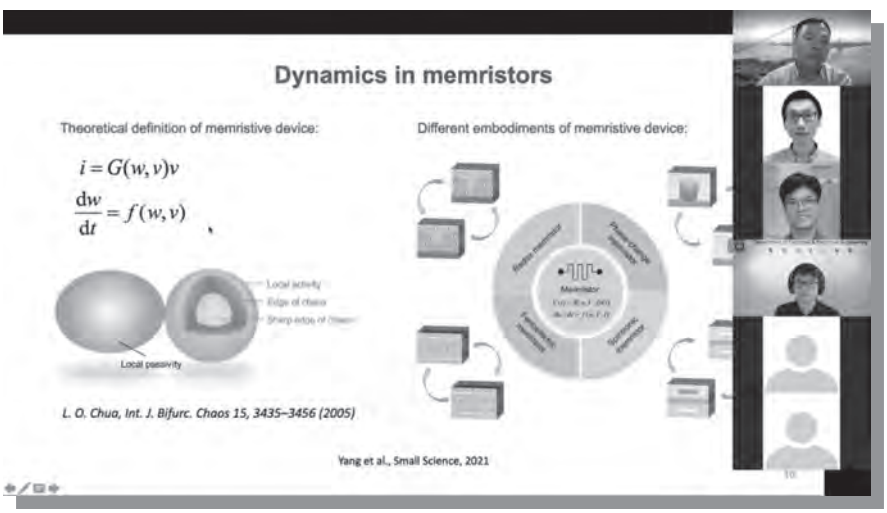
Asia & Pacific (Region 10)

ED/SSC Hong Kong Chapter

—by Qiming Shao

On 3–5 August 2021, the IEEE Hong Kong Joint Chapter of Electron Devices and Solid-State Circuits (ED/SSC) co-organized the "Microelectronics Technology Forum: Capturing the Emerging Technologies and Business Opportunities". This is a hybrid forum mainly organized by the newly established Semiconductor Nanotechnology Alliance. The leading experts in the microelectronics industry and academia shared their visions and insights about global trends, business opportunities of emerging technologies, and critical research infrastructure. Dr. Anthony Yen, Vice President and Head of Technology Development Center, ASML, gave a keynote speech titled "EUV Lithography—Road to HVM, Today's Status, and What's Next." Prof. Hon Ki Tsang and Prof. Din Ping Tsai shared their visions on the commercialization of silicon photonics and meta-devices. Prof. Philip Wong from Stanford University presented how flexibility at scale accelerates lab-to-fab transition. During the forum, the experts and attendants discussed the future of microelectronics. As a result, the Semiconductor Nanotechnology Alliance will soon release a white paper about microelectronics. Many chapter members are contributing to this undertaking.

On 27 August 2021, the IEEE Hong Kong Joint Chapter of Electron Devices and Solid-State Circuits (ED/SSC), in association with the Department of Electrical and Electronic Engineering, University of Hong Kong, organized a webinar given by Prof. Yuchao Yang, Professor, and Director of Center for Brain-Inspired Chips, Peking University. The title of his talk is "Memristive Dynamics Based Hardware Primitives for Efficient Computing." Prof. Yang gave a comprehensive overview of non-von Neumann architectures based on emerging memristive devices, such as RRAM, MRAM, PCM, etc. He showed a few examples to illustrate how to leverage analog nature, intrinsic spatiotemporal dynamics, and uncertainty to perform AI and neuromorphic computing. In total, 140 participants, including 47 IEEE members/student members, attended the webinar. The participants and speaker got involved in the talk very much, through many questions and answers. Readers can find more information about this seminar on the IEEE HK ED/SSC Chapter website: https://r10.ieee.org/hk-edssc/.



Webinar by Prof. Yuchao YANG (top right)

ED Kansai Chapter

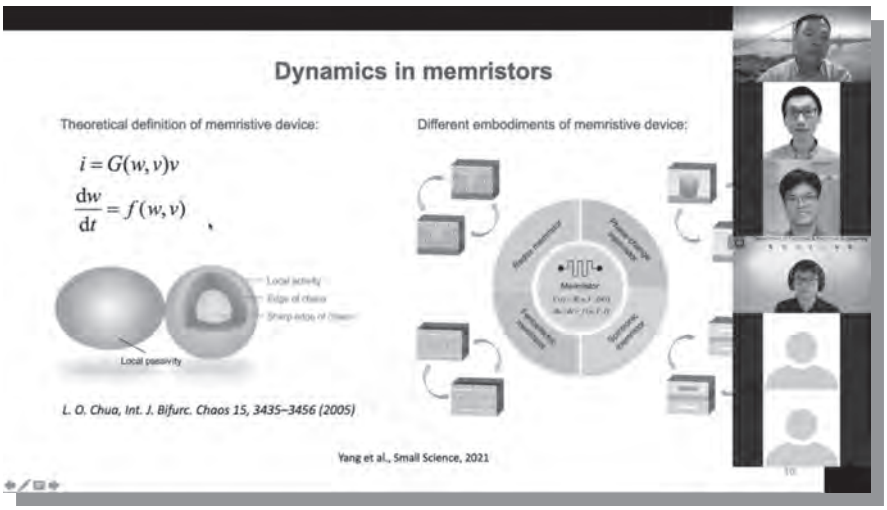
—by Yuichi Ando

A technical online meeting of ED Kansai Chapter was held on 21 June 2021. Dr. Hirobumi Watanabe, ED Kansai Chair, gave a talk to students entitled: "Lecture for graduate students". The meeting had a total 59 attendees, including 3 EDS members, enjoying the interesting presentation.

On 28 July 2021, the ED Kansai Chapter hosted a round-table meeting, discussing widely technical, industrial, educational, and business interests/concerns. The meeting organizers invited two speakers. Mr. Atsushi Takahashi of Nagase & Co. Ltd. gave a talk on "Market Trend of Fan-Out Panel Level Package". Mr. Makoto Watanabe of Silvaco Japan gave a speech on "The Reality of TCAD Utilization in FPD Development". We had 15 EDS members enjoying these discussions.

The VLSI Symposium Report Meeting was held on 30 July 2021. This meeting was a joint event with SSCS Japan Chapter, SSC Kansai Chapter, and ED Japan Chapter. A total of 19 papers on a wide range of topics such as electronic devices and circuits were presented. There were 147 attendees, including 118 IEEE members enjoying these lectures.

The ED Kansai Chapter has two upcoming events. Both Chapter General Assembly Meeting and Technical Lecture meeting will be held in the middle of January 2022.



The roundtable meeting on July 28, 2021. Mr. Atsushi Takahashi of Nagase & Co. Ltd. talked about "Market Trend of Fan-Out Panel Level Package"

The roundtable meeting on 28 July 2021. Mr. Atsushi Takahashi of Nagase & Co. Ltd. talked about "Market Trend of Fan-Out Panel Level Package"

The invited webinar "Beyond CMOS: Novel Materials, Emerging Memory and Applications" by Prof. Ying-Chen "Daphne" Chen

ED NCTU Student Branch Chapter

—by Ming-Chun Hong

An invited webinar organized by ED NCTU Student Branch Chapter was held on 30 July 2021. Prof. Ying-Chen "Daphne" Chen from Northern Arizona University was invited to share the experience in her academic career and current research focuses. In the speech entitled "Beyond CMOS: Novel Materials, Emerging

Memory and Applications". Prof. Chen firstly talked about her motivation for pursuing an academic career. Then during the research focus part, four important research topics were covered: emerging memory and its applications, active matter, flexible electronics, and the new possibility of fabrication in outer space. At the end of the talk, Prof. Chen encouraged future researchers: "Be passionate, be curious, be strong". Her personal experience sharing motivated our young students greatly.

~Alex Hou, Editor

Delhi Section ED Chapter

—by Harsupreet Kaur

The Chapter in association with the Department of Electronic Science and University of Delhi South Campus jointly organised a webinar on "PCB Manufacturing and Assembly" which was held on 7 September 2021. The inaugural talk on the topic "Electronics Manufacturing—Trends and Developments" was delivered by Mr. Vinit Verma, Director, PROSEM Technology India Pvt. Ltd. The speaker discussed the various aspects related to PCB technology and evolution of the trend over the years. The prospects and challenges related to PCB manufacturing in India were highlighted. The next talk on "An Introduction to PCB Manufacturing and Assembly" was delivered by Dr. Hema Mehta Kapoor, Director, HMPCB Solutions. The technical steps of PCB Manufacturing and Assembly were explained in detail. This was followed by a talk on the topic "Process Flow and Virtual Tour of PCB and PCBA Unit" by Ms. Monika Bansal, Director, HMPCB Solutions. The speaker explained various processes in detail and presented videos of some practical case studies. The talks were attended by more than 75 participants.

The Chapter in association with Shaheed Rajguru College of Applied Sciences for Women, University of Delhi organized on 15 September 2021, a Distinguished Lecture on the topic, "Near-/in-sensor computing for neuromorphic machine vision" by Dr. Yang Chai, the Hong Kong Polytechnic University. The talk focused on integrated sensor/computing systems and the use of advanced integration technologies with new computing algorithms for implementing various low-level and high-level processing functions. The talk was attended by more than 70 participants. In addition to this, the chapter organized on 24–25 September a two-day online lecture series on "Fundamentals and Applications of Technology Driven Sensors". The first talk was delivered by Dr. Saakshi Dhanekar, Department of Electrical Engineering, IIT Jodhpur, on "The Development and Applications of Nano-Sensors". The talk focused on the development of nanosensors, the trends and challenges that lie ahead. The next talk was by Prof. Mahesh Kumar, Department of Electrical Engineering, IIT Jodhpur, on "AlGaN/GaN HEMT based Heavy Metal Ion Sensors for Smart Water Quality Monitoring". The last talk of the webinar was on the topic "Silicon detectors in High Energy Physics Experiments: Challenges and the Use of New Technologies" by Prof. Ashutosh Bhardwaj, Department of Physics and Astrophysics, University of Delhi, India. The talks were attended by more than 90 participants.

Madras Section ED Coimbatore Chapter

—by J. Charles Pravin

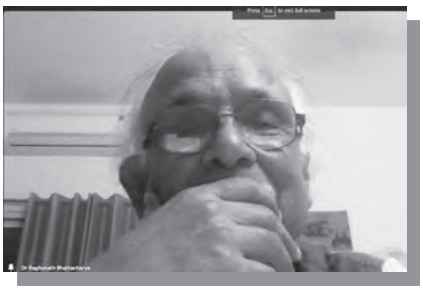
The Chapter along with the Department of Electronics and Communication Engineering College of Karunya Institute of Technology and Sciences organized on 27 July 2021 an online Distinguished Lecture, titled "GaN-on-Si Technology for Power, RF & Specials". The speaker was Prof. Joachin N. Burghartz, Director and Chairman of the Board at Instituts für Mikroelektronik Stuttgart (IMS), Germany. Dr. D. Nirmal, chairperson of ED Coimbatore Chapter welcomed the speaker and introduced the audience to the various challenges in high power devices. Prof. Burghartz discussed the key benefits of GaN-on-Si devices and its recent RF applications. He explained in detail about the technologies, testing, packaging and assembly of GaN-on-Si devices. Around 57 participants from various engineering colleges across India and abroad were enlightened by the lecture. The participants actively participated in the interactive session after the lecture and got insightful perceptions towards research problems on high power semiconductor devices.

Meghnad Saha Institute of Technology ED Student Branch Chapter

—by Adrija Mukherjee

The Chapter in association with the Student Branch and the Department of Electronics and Communication Engineering, Meghnad Saha Institute of Technology organized an Alumni Talk Program by the alumnus Mr. Dipanjan Sen. The online talk was held on 3 July 2021 and the topic was "Journey from MSIT to Penn State University". Prof. Swarnil Roy and Prof. Sharmi Ganguly, who are faculty members of the Department, coordinated the entire session. About 94 participants were present during the session. It was an extremely important talk during which the students could obtain information on how to prepare in the research and academic field at home and abroad for their future professional career.

Further, the Chapter in association with CARREST and Research & Development Cell, Meghnad Saha Institute of Technology, Research & Development Cell, Netaji Subhash Engineering College organized on 12 July 2021 a technical talk program on "My Scientific Journey for Last Half a Century" by Prof. (Dr.) Raghunath Battacharya. Dr. Bhattacharya is



Virtual mode of presentation by Prof. Dr. Raghunath Bhattacharya

currently the Advisor at DST-IIEST Solar PV Hub which is a joint initiative by Department of Science & Technology (DST), Government of India, and Centre of Excellence for Green Energy and Sensor Systems (CEGESS), Indian Institute of Engineering Science and Technology (IIEST), Shibpur. More than 60 participants (12 IEEE Members) were present during the session. Faculty members like Prof. Ankur Ganguly, Principal at MSIT and the counselor of the Student Branch, and Prof. Utpal Ganguly also gave introductory speeches. Prof. Amal Kumar Ghosh vividly described the various topics related to the R&D Cell. The talk ended with "Vote of Thanks" by the Chapter advisor, Dr. Manash Chanda.

The Chapter in association organised on 14–15 July 2021 a 2-day Workshop on "Semiconductor Device Modeling & Simulation" chaired by Mr. Dipanjan Sen. Fifty-four participants (incl. 16 IEEE student members) were present during the Workshop. The students learnt about the importance of using TCAD tools. Hands-on training on device modeling and simulations was provided to all the students.

An online "Membership Awareness Program" was organized on 1 August 2021. Dr. Manash Chanda, the advisor of the ED Student Branch Chapter and Dr. Chandi Pani, the advisor of the COMSOC Student Branch Chapter conducted the session. About 42 participants were present. They were highly benefited from the session. As an outcome of this program, twelve students from the first year took the membership of the ED Chapter.

Uttar Pradesh Section, ED Kanpur Chapter

—by Subham Sahay

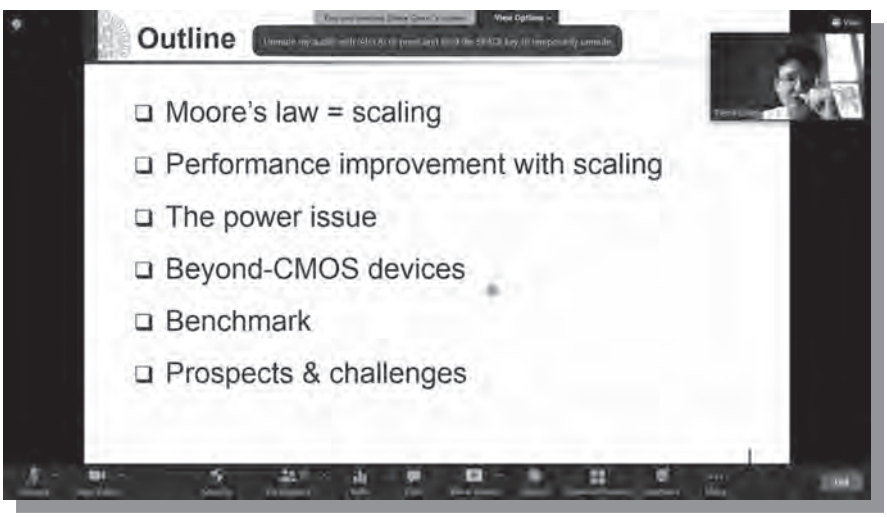
The Chapter organized a Distinguished Lecture by Prof. Elena Gnani, Department of Electrical, Electronic, and Information Engineering "Guglielmo Marconi", University of Bologna, Italy, on the topic "Trends and challenges in Nanoelectronics for the next decade". Apart from this, Dr. Sumit Mandal, Electrical Engineering, University of Wisconsin-Madison, conducted a seminar on "Network-on-Chip (NoC) Performance Analysis and Optimization for Deep Learning Applications". The seminar was organized to boost the knowledge and introduce the Chapter members to NOC design and Deep Learning.

National Institute of Technology-Silchar, ED Student Branch Chapter

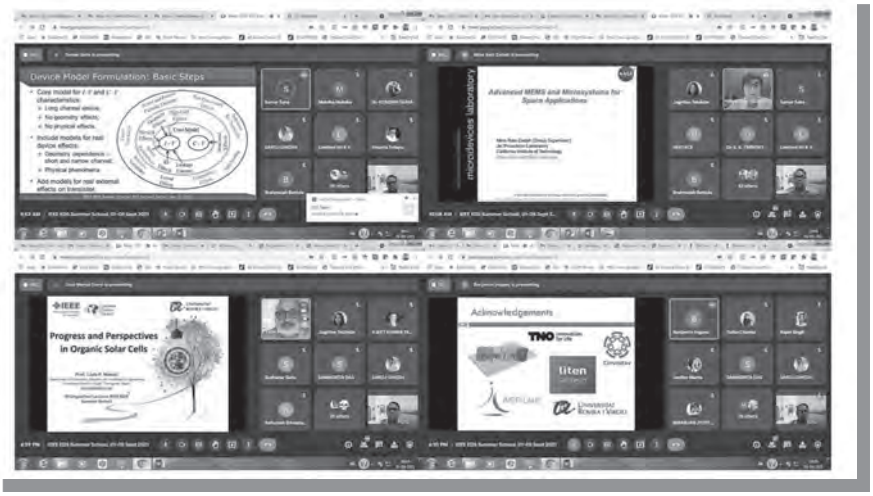
—by T.R. Lenka

The Chapter in association with the Nanotechnology Council Chapter of Kolkata Section and the Department of Electronics and Communication Engineering, National Institute of Technology (NIT) Silchar, organized from 26–30 July 2021 an international workshop on "Optimization and Intelligence in Electronics Engineering" which was held in a virtual mode. On 12 June 2021 the Chapter organized a Distinguished Lecture by Prof. Elena Gnani, University of Bologna, Italy. The topic of the virtual DL was "Tunnel FETs: Device Physics and Realizations." Another Distinguished Lecture was delivered on 4 August 2021 by Prof. Anisul Haque of East West University Bangladesh. The title of the on-line talk was "Bifacial Photovoltaics." Another DL on "High Performance Quantum Computing in Nanoelectronics" was delivered by Prof. Adam W. Skorek of the University of Quebec, Canada. The Lecture was held in virtual mode on 26 August 2021. The Chapter also organized a five-day Faculty development program on "Recent Trends in Bio-MEMS and Medical Microdevices: From Device to Application". From 1–5 September 2021 the Chapter organized a Summer School funded by the IEEE Electron Devices Society. The Summer School was held virtually, with 20 Distinguished Lectures delivered by:

- Prof. Samar Saha, of Santa Clara University, USA delivered the talk on "Physics of Microelectronic Device Models for VLSI Circuit Design".
- Prof. Mina Rais-Zadeh, of the University of Michigan, USA



On-line presentation by Prof. Elena Gnani



DLs by Prof. Samar Saha, Prof. Mina Rais-Zadeh, Prof. Lluis F. Marsal and Prof. Benjamin Iniguez delivered on 1 September 2021

presented a talk on "Advanced MEMS and Microsystems for NASA application".

- Prof. Lluis F. Marsal of the Universitat Rovira Virgili, Spain presented the talk titled "Progress and Perspectives in Organic Solar-Cells".
- Prof. Benjamin Iniguez gave the talk "Identification and modelling of low-frequency noise sources in Organic and IGZO TFTs".

Other Distinguished Lecturers were:

- Prof. Victor Veliadis of the North Carolina State University, USA,
- Prof. Lan Fu of Australian National University, Australia,
- Prof. Tibor Grasser of Technische Universität Wien, Austria,
- Prof. Durga Misra of New Jersey Institute of Technology, USA,
- Dr. Andreas Kerber of Intel, USA,
- Prof. Ajit K. Panda of National Inst. of Science & Technology, India,
- Prof. Arokia Nathan of the University of Cambridge, UK,
- Prof. Michael Shur from Rensselaer Polytechnic Institute, USA, and others.

This School was attended by 80 participants comprising EDS members and non-members, including foreign participants. The organization of the EDS Summer School was a great success.

~ Soumya Pandit, Editor

Let's Talk: Semiconductor Fabrication

—by Sharifah Fatmadiana Wan Muhammad Hatta and Maizatul Zolkapli

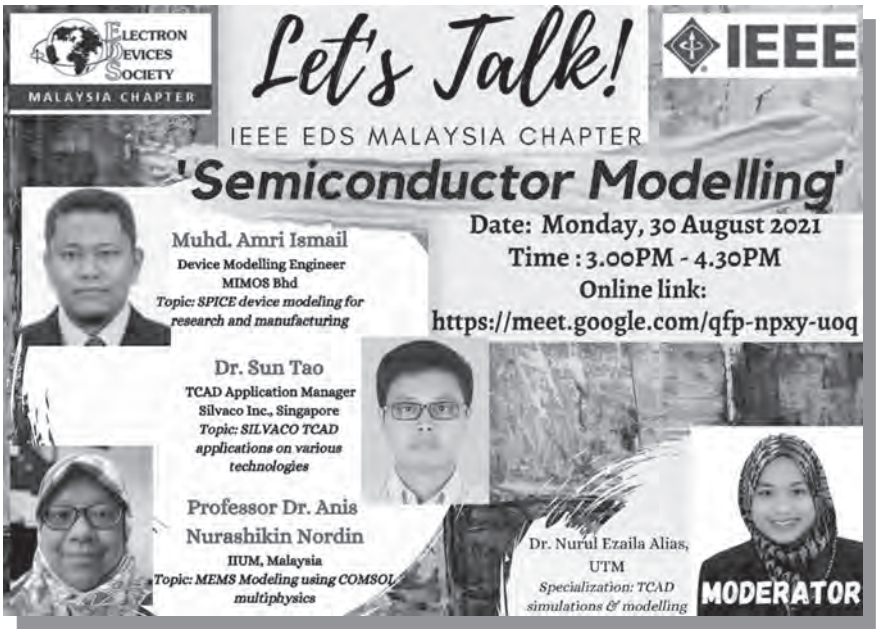
On 6 July 2021 the ED Malaysia Chapter conducted an online forum series called 'Let's Talk'. The forum was focused on the topic "Semiconductor Fabrication and Processes". The following invited speakers participated in the discussion panel: Prof. Ts. Ir. Dr. Abdul Manaf Hashim from Malaysia-Japan International Institute of Technology (MJIIT) on 'Electron and Ion Beam Facilities for Micro-Nanostructure Formation and Device Fabrication', Assoc. Prof. Ts. Dr. Muhammad Mahyiddin Ramli from Universiti Malaysia Perlis (UniMAP) and Ir. Dr. Hazian Mamat from MIMOS on 'Defects in Semiconductor Process'. The forum was moderated by Dr. Suhana Mohamed Sultan from UTM. The event was started with a IEEE membership drive briefing by the Chair of ED Malaysia Chapter, Assoc. Prof. Ir. Ts. Dr. Ahmad Sabirin Zoolfakar. Then the speakers presented their 20 mins talks. The forum concluded with a 15 mins session of Q&A with the audience. The forum attracted more than 60 audiences and received positive feedback from all the participants.

Let's Talk: Semiconductor Modelling

—by Sharifah Fatmadiana Wan Muhammad Hatta and Maizatul Zolkapli

On 30 August 2021 the ED Malaysia Chapter conducted another forum series of 'Let's Talk'. During

Panelists of Let's Talk: Semiconductor Fabrication



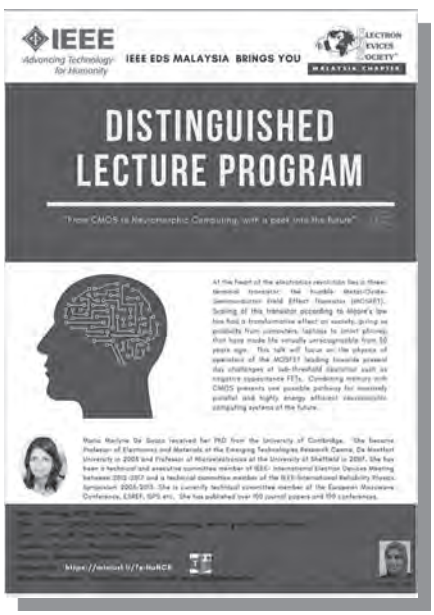
Panelists for Let's Talk: Semiconductor Modelling

this forum the invited speakers discussed the topic "Semiconductor Device Modelling". Prof. Dr. Nurashikin Nordin from International Islamic University Malaysia (IIUM) presented on "Modeling MEMS devices using CST and COMSOL." Dr. Sun Tao from Silvaco Inc. made a presentation on "Silvaco TCAD applications in various technologies." Mr. Muhd Amri Ismail presented the topic "SPICE device modelling for research and manufacturing". The forum was moderated by Dr. Nurul Ezaila Alias from Universiti Teknologi Malaysia (UTM). After the panelists had presented their 20 minute talks the forum was concluded with a 15 minute Q&A session with the audience. The forum attracted more than 100 attendees from countries worldwide and received positive feedback from all the participants.

Virtual Distinguished Lecture: From CMOS to Neuromorphic Computing, With a Peek Into the Future

—by Maizatul Zolkapli & Suhana Mohamed Sultan

The EDS Malaysia Chapter successfully organized on 4 August 2021 the first virtual distinguished lecture (VDL). Prof. Merlyne De Souza from University of Sheffield, UK, was invited to give the lecture "From CMOS to neuromorphic computing, with a peek into the future". At the heart of the electronics revolution lies a three-terminal transistor: the humble Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET).



Distinguished lecture by Professor Merlyne De Souza

Scaling of this transistor according to Moore's law has had a transformative effect on society, giving us products from computers, laptops to smart phones, that have made life virtually unrecognizable from 50 years ago. Professor Souza began her talk with the physics of operation of the MOSFET leading towards present day challenges of subthreshold operation such as negative capacitance FETs. She then talked about combining memory with CMOS which presents one possible pathway for massively parallel and highly energy efficient neuromorphic computing systems of the future. The VDL was moderated by Dr. Suhana Binti Mohamed Sultan from Universiti Teknologi Malaysia (UTM). A total of 40 participants from both local and international attended the lecture. The lecture was recorded, and the link can be accessed via this link: https://www.youtube.com/watch?v=R7Do2UwtuWU.

Virtual Distinguished Lecture: Acousto Optic Devices for Space Applications

—by Maizatul Zolkapli, Nurul Ezaila Alias, and Hazian Mamat

On 27 August 2021, the ED Malaysia Chapter successfully organized the second virtual distinguished lecture (VDL). Dr. Mina Rais-Zadeh from Jet Propulsion Laboratory, California Institute of Technology, was invited to deliver a lecture on "Acousto Optic Device for Space Applications". Dr Mina started off with an overview of the research domains under investigation by JPL. She then talked about the unique criterias of space and mission concepts to hot planets particularly venus. The potential instruments for the mission to Venus and their science goal and capabilities were also shared. Besides from the VDL, Dr. Hazian from MIMOS Berhad introduced ED Malaysia Chapter. The session was moderated by Dr. Nurul Ezaila Alias from Universiti Teknologi Malaysia (UTM).

Distinguished lecture by Dr. Mina Rais-Zadeh

Forty participants from both local and foreign communities attended the lecture. The lecture was also recorded, and it can be accessed via this link: https://www.youtube.com/watch?v=Rg-MQdUNXMM

13th 2021 IEEE Regional Symposium on Micro and Nanoelectronics (RSM)

—by Maizatul Zolkapli

The 2021 IEEE Regional Symposium on Micro and Nanoelectronics (RSM) was successfully held from 2–4 August 2021 by the ED Malaysia Chapter. This is the 13th installment in the RSM series which has been conducted since 2007 to convene semiconductor micro and nanoelectronics researchers from academia and industry. Due to COVID-19 pandemic, the conference was held virtually on the WebEx Platform. The conference was chaired by ED Malaysia Chapter Chair, Assoc. Prof. Ir. Ts. Dr. Ahmad Sabirin Zoolfakar. In total, 45 publications that covered various topics in micro and nanoelectronics were accepted. The conference was honoured to have 3 esteemed keynote speakers in this conference: Professor Dr. Muhammad Mustafa Hussain from University California at Berkeley, USA, who spoke on Democratized Wearable Electronics Using DIY Assembly of Paper and High Performance CMOS Electronics, Ir. Ts. Bernard from Appscard Group AS (Security in Semiconductor Manufacturing) and Prof Ir. Dr. Norhayatin Soin from Universiti Malaya (Printed Flexible and Stretchable Electronics Toward Wearable Sensing Devices).

~Sharma Rao Balakrishnan, Editor

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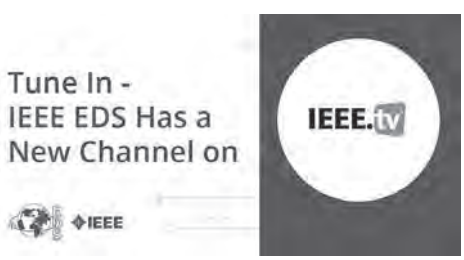

EDS MEETINGS CALENDAR

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2022 16th European Microwave Integrated Circuits Conference (EuMIC)	13 Feb -18 Feb 2022	London, United Kingdom
2022 6th IEEE Electron Devices Technology & Manufacturing Conference (EDTM)	06 Mar – 09 Mar 2022	Oita, Japan
2022 IEEE 34th International Conference on Microelectronic Test Structures (ICMTS)	20 Mar – 23 Mar 2022	Cleveland, OH
2022 IEEE International Reliability Physics Symposium (IRPS)	27 Mar – 31 Mar 2022	Dallas, Texas
2022 International Symposium on VLSI Design, Automation and Test (VLSI-DAT)	18 April – 21 April 2022	Hsinchu, Taiwan
2022 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA)	18 April – 21 April 2022	Hsinchu City, Taiwan
2022 23rd International Vacuum Electronics Conference (IVEC)	25 April – 28 April 2022	Monterey, CA
2022 IEEE Latin American Electron Devices Conference (LAEDC)	27 April – 29 April 2022	Mexico
2022 33rd Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC)	02 May – 05 May 2022	Saratoga Springs, NY
2022 IEEE International Memory Workshop (IMW)	15 May – 18 May 2022	Germany
2022 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EuroSOI-ULIS)	18 May – 20 May 2022	Udine, Italy

2022 34th IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD)	22 May – 26 May 2022	Vancouver, BC, Canada
2022 IEEE Symposium on VLSI Technology & Circuits	13 June – 17 June 2022	Honolulu, HI
2022 IEEE International Interconnect Technology Conference (IITC)	27 June – 30 June 2022	CA, USA
2022 17th European Microwave Integrated Circuits Conference (EuMIC)	26 Sept – 27 Sept 2022	Milan, Italy
2022 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)	16 Oct – 20 Oct 2022	Phoenix, AZ
2022 International Electron Devices Meeting (IEDM)	02 Dec – 08 Dec 2022	San Francisco, CA
2022 IEEE 50th Semiconductor Interface Specialists Conference (SISC)	08 Dec – 10 Dec 2022	San Diego, CA

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EDS Vision, Mission and Field of Interest Statements

Vision Statement
Promoting excellence in the field of electron devices for the benefit of humanity.

Mission Statement
To foster professional growth of its members by satisfying their needs for easy access to and exchange of technical information, publishing, education, and technical recognition and enhancing public visibility in the field of Electron Devices.

EDS Field of Interest
The EDS field-of-interest includes all electron and ion based devices, in their classical or quantum states, using environments and materials in their lowest to highest conducting phase, in simple or engineered assembly, interacting with and delivering photo-electronic, electro-magnetic, electromechanical, electro-thermal, and bio-electronic signals. The Society sponsors and reports on education, research, development and manufacturing aspects and is involved in science, theory, engineering, experimentation, simulation, modeling, design, fabrication, interconnection, reliability of such devices and their applications.