IEEE

ELECTRON DEVICES SOCIETY

IEEE ELECTRON DEVICES SOCIETY

JULY 2004 VOL. 11, NO. 3 ISSN:1074 1879 EDITOR-IN-CHIEF: NINOSLAV D. STOJADINOVIC

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YOUR COMMENTS SOLICITED

Your comments are most welcome. Please write directly to the Editor-in-Chief of the Newsletter at nstojadinovic@elfak.ni.ac.yu

2004 IEEE INTERNATIONAL SOI CONFERENCE (SOI)

The 30th Annual IEEE International SOI Conference, the premier conference dedicated to current trends in Silicon-on-Insulator technology, will be held October 4 – 7, 2004 at the Francis Marion Hotel, Charleston, South Carolina. A one-day Tutorial Short Course will precede the conference on Monday, 4 October.

The SOI conference was established with the support of IEEE to provide a forum for open discussion in all areas of silicon-on-insulator technologies and their applications. Ever increasing demand and modifications in this technology bring the industry together to discuss new accomplishments and gains. Original papers presenting new developments in the industry will be presented at the conference.

The 2004 SOI International Conference will begin with a half-day plenary session followed by two days of oral sessions, a poster session and a late news session. A Best Paper Award will be presented at the closing on Thursday. Session topics will focus on basic materials research, device research, circuit development (special and improved) and applications and uses. Rump sessions will be held on Wednesday evening, October 6. These sessions encourage attendees to share their opinions and expertise on the chosen topics of discussion.

Additionally, a materials and equipment exhibition relating to SOI technology will be held concurrently with the conference. Participants will have the opportunity to visit the exhibit area to see what's new in SOI. Overall, the 2004 SOI International Conference offers attendees a broad spectrum of information, opportunities for discussion with one's peers, and is a must for engineers with direct involvement or partial involvement in SOI.

The 2004 SOI Conference seeks papers on a wide range of SOI technology including:

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(Elected for a three-year term (maximum two terms) with 'full' voting privileges)

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CONTRIBUTIONS WELCOME

Readers are encouraged to submit news items concerning the Society and its members. Please send your ideas/articles directly to either the Editor-in-Chief or appropriate Editor. The e-mail addresses of these individuals are listed on this page. Whenever possible, e-mail is the preferred form of submission.

Newsletter Deadlines

Issue	Due Date
January	October 1st
April	January 1st
July	April 1st
October	July 1st

IEEE Electron Devices Society Newsletter (ISSN 1074 1879) is published quarterly by the Electron Devices Society of the Institute of Electrical and Electronics Engineers, Inc. Headquarters: 3 Park Avenue, 17th Floor, New York, NY 10016-5997. Printed in the U.S.A. One dollar ($1.00) per member per year is included in the Society fee for each member of the Electron Devices Society. Periodicals postage paid at New York, NY and at additional mailing offices. **Postmaster:** Send address changes to IEEE Electron Devices Society Newsletter, IEEE, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331.

Message from the EDS President


Hiroshi Iwai

As the first President elected from a region outside the U.S., it is a great honor and privilege to serve as the President of the Electron Devices Society. My term is starting at a time when the globalization activities of the Society are extremely intense and also when the financial situation of the Society has started to recover, thanks to the great effort of the Society members.

The importance of Electron Devices for the world is increasing more than ever, as it has played an indispensable role for providing us with intelligent services through the recent tremendous progress made by Electron Devices, including the internet, cellular phones, digital electronic appliances, video game machines, GPS navigations and industrial and entertainment robots. In the near future, Electron Devices are expected to contribute more significantly by substituting some of our intelligent labors with a human's sensitivity and machine accuracy. For example, automatic simultaneous interpretation, automatic elderly care, and automatic surgery operations could be realized in 20 years. We are proud that our Society is participating in such important activities in such an exciting period, and we wish to contribute to the progress of Electron Devices as much as we can.

At the February IEEE TAB Meeting series, we held the second EDS strategic planning meeting to discuss how the Society can better serve the current members and attract future potential members. In order for EDS to be more flexible in its ability to respond quickly to technical shifts in the community and to allow the technical committees to have more leverage in influencing the Society's directions, we will make the Technical and Meetings committees create concrete action items and discuss them at the coming 2004 May AdCom Meeting series. Although there are an enormous number of industrial people in the world participating in Electron Devices development, manufacturing, and application, only a small portion of these individuals are members of the Society. To promote the participation of industrial people, the Industrial Relations Adhoc Committee was founded and is working on a plan of action. Education is another important role of the Society, and the Distinguished Lecturer (DL) Program is one of the most attractive programs for the members. We are planning to enhance the DL Program by significantly increasing the number of lecturers, increasing the DL budget and having a strong collaboration between the Educational Activities and the Regions/Chapters committees. The number of Electron Devices engineers and scientists are increasing very rapidly in the non-US Regions such as Asia. In order to take advantage of the opportunity, the Regions/Chapters and the Membership committees will work together to promote membership.

We are planning to make EDS membership more useful and attractive to the members. It is planned that an archival DVD set, which will include all issues and years of Transactions on Electron Devices (T-ED), and Electron Device Letters (EDL), and all published digests of the International Electron Devices Meeting (IEDM), will be made available to our members in December at the IEDM for a very reasonable price. EDS plans to work closely with its flagship conference, the IEDM, to encourage and increase the student and industry participation for both the IEDM and EDS. We recognize that all the activities of the Society are accomplished by the devotion of the volunteers of the Society; and as a result, EDS plans to increase the number of certificates of appreciation it issues to its contributors. These proposals will be further discussed at the May 2004 EDS AdCom Series and we will establish a schedule for implementation.

I will report back to the membership on the progress of the Society goals in future communications. I would like to encourage you all to think about ways that we can enhance these programs and let me know how the Society can better serve you each individually.

Hiroshi Iwai
EDS President
Tokyo Institute of Technology
Yokohama, Japan

Message from the Editor-in-Chief

After six years of distinguished service, Prof. Christian Zardini has departed from the Editorial Board this year. I am taking this opportunity to thank Christian for his dedicated service to the Newsletter as a Region 8 Editor. Replacing Prof. Zardini is Dr. Cora Salm from the University of Twente, The Netherlands, whose biography follows. Cora has a lot of experience in EDS related activities, and it is my pleasure to welcome her as the new Region 8 Newsletter Editor for Western Europe.


Cora Salm

Cora Salm received M.Sc. degree in applied physics in 1993, and Ph.D. degree in electrical engineering in 1997, both from the University of Twente. She is currently an Assistant Professor at the MESA Research Institute, University of Twente. Her past research interests include electrical characterization of deep-submicron MOS devices, integration of poly-SiGe in existing process flow, and polycrystalline GeSi for advanced CMOS technologies. Her recent research mainly focuses on reliability issues of advanced semiconductor devices, such as gate-dielectric integrity, stresses in metallization films, and electrostatic discharge. Dr. Salm is a Member of IEEE and a reviewer for *IEEE Electron Device Letters.*

Ninoslav D. Stojadinovic
EDS Newsletter Editor-in-Chief
University of Nis
Sertbia and Montengro

Upcoming Technical Meetings

2004 IEEE Non-Volatile Semiconductor Memory Workshop (NVSMW)

The 2004 IEEE Non-Volatile Semiconductor Memory Workshop (NVSMW) will be held August 22 - 26, 2004 in Monterey, California. The IEEE Electron Devices Society sponsors the workshop. NVSMW is a unique forum for both specialists in all aspects of nonvolatile memory microelectronics and novices wanting to gain a broader understanding of the field. Attendees represent professional and academic researchers involved with semiconductor non-volatile memory development and production along with end users of memory products. Principal topics for discussion at NVSMW are: device physics; silicon processing; product testing; new technologies, including multi-level-cell approaches; programmable logic; memory cell design; integrated circuits; solid state disks and memory cards; memory reliability; and new applications.

An important goal of NVSMW is to provide an informal environment to encourage discussions among participants and lively interactions. There will be morning and afternoon technical sessions, along with a lively evening panel discussion on a hot topic in the nonvolatile memory field. Technical interaction among presenters and attendees is encouraged through question and answer sessions and allotting ample time after the formal paper presentations for further in-depth discussions. Organized breaks, including snacks and the workshop dinner and lunch are provided as opportunities to meet and exchange ideas with colleagues. Breakfasts are also provided. The morning and afternoon technical sessions are organized in a manner to provide ample time for the informal exchange and to enjoy the beauty of the Monterey peninsula region of California.

This year will be the 20th meeting of NVSMW. The workshop is held every 18 months, alternating between February and August. The February meeting is usually held the week after ISSCC. The 2004 meeting will be held in the fourth week of August. Early workshops alternated between Monterey, California for the February meeting and Vail, Colorado for the August meeting. The Vail venue was dropped a number of years ago, to facilitate attendance and travel from the nearby Silicon Valley. For many years, the attendance for the workshop was around 100. In recent years, however, the attendance has grown considerably, reflecting the large growth in the Non-volatile memory market, particularly flash memory and embedded memory on logic cores, with the attendance at the last several workshops being well in excess of 200. In order to maintain the workshop atmosphere of the forum, the maximum attendance is limited to 300. Therefore, advance registration is highly recommended. A wide international community attends NVSMW from North America, Europe, Japan and other Asian countries. The past several workshops have had featured sessions to address the growth of segments of the memory market.

The last workshop, in 2003, featured the keynote speech presented by Dr. Herman Maes of IMEC, on Silicon Scaling and Its Consequences for Memory Technology. There were two invited papers. One of the invited papers by Al Fazio of Intel discussed the Technology and Applications related to 0.13um Logic + Flash. Another invited paper by Dr. Josef Willer of Ingentix discussed recent developments of Nitride-Storage Memories. A third invited paper, presented by Radu Andrei of Web feet Research, discussed a competitive assessment of Advanced Nonvolatile technologies, as compared to conventional Floating Gate NVM technologies. There was a panel discussion, moderated by Alan Niebel of Web feet Research, which examined packaging and test developments for System-In-Package Technologies. In addition, there were paper sessions on Design and Applications of NVM, Nitride Storage technologies, Reliability, Integration & Characterization of NVM, and Alternative Memory technologies.

For this year's workshop, the deadline for submitting abstracts to the Technical Chairman was April 26, 2004. Proceedings consisting of bound copies of all abstracts will be handed out to attendees at the conference, along with a list of attendees and their phone numbers and e-mail addresses to allow future contact of workshop colleagues. It is anticipated that the format of the 2004 workshop will be similar to that of the past years, with an expected 30-40 technical paper presentations. The last workshop consisted of six technical sessions over a three-day period. The workshop opened with a Sunday evening registration reception, consisting of drinks and hors d'oeuvres. Breakfast opened each day, while a work-

shop reception dinner and evening panel discussion closed out Tuesday evening. The workshop formally closed on Wednesday afternoon. Breakfast was also provided on Thursday morning, for those remaining in the Monterey area.

The 2004 NVSMW will be held at the Hyatt Regency in Monterey, California. The hotel is conveniently situated in the Monterey peninsula and allows fast access to many sights. Among favorite destinations are: the famous Fisherman's Wharf, Cannery Row, The Monterey Bay Aquarium, 17-Mile Drive, nearby Carmel and the many tranquil sights of natural beauty of the Monterey coastline and the fine dining experiences of the area. The Hyatt Regency is located at: One Old Golf Course Road, Monterey, California. The hotel can be reached by TEL: (831) 372-1234.

For registration information and general inquiries about NVSMW, please contact any of the workshop chairmen. General Chairman: Kelly Baker, Motorola, Inc., Mail Drop OE341, 6501 William Cannon Dr. West, Austin, TX 78735, USA, Phone: (512)-895-8335, Fax: (512)-895-8605, E-mail: kelly.baker@motorola.com; Technical Chairman: Andrei Mihnea, M/S 306, Micron Technology, Inc., 8000 S. Federal Way, P.O. Box 6, Boise, ID 83707, Phone: (208) 363-1330, FAX: (208) 363-2919, E-mail: amihnea@micron.com. Finance Chairman: Dr. Stephen Keeney, M/S RN3-01, Intel, 2200 Mission College Blvd., Santa Clara, CA 95054, USA, Phone: 408-765-0128, Fax: 408-765-5775, E-mail: stephen.n.keeney@intel.com.

You can also visit the NVSMW web site for up-to-date information at: http://ewh.ieee.org/soc/eds/nvsmw

Kelly Baker
NVSMW General Chair
Motorola, Inc.
Austin, TX, USA

2004 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)

Wireless communications is a burgeoning market area and a major driver behind the semiconductor industry, and SiGe BiCMOS and III-V technologies have emerged as the manufacturing processes of choice for many wireless ICs. If you work or are interested in this exciting area, then the 2004 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (IEEE BCTM) is a conference you want to attend. The 2004 IEEE BCTM will be held at the Le Centre Sheraton Hotel in Montreal, Quebec, Canada from 12 to 15, September 2004.

IEEE BCTM has historically been held in Minneapolis, MN. However, due to popular demand, the conference is now on the road, which started in 2002 in Monterey, CA, in 2003, in Toulouse, France, and back to North America in 2004. Historically, Canada has been a stronghold of bipolar research and development, in manufacturing technologies and circuits, both in industry and academic institutions.

Montreal is one of the world's most dynamic metropolises, characterized by its distinctive "joie de vivre", entertainment, recreation, and gastronomy. Boasting a rich history, Montreal is unique in North America for its special blend of urban modernism and discreet charm inspired by the cultural distinctiveness of Quebec.

The technical program for IEEE BCTM consists of one day of short courses given by noted experts, followed by two days of invited and contributed technical presentations in the areas of RF, device physics, process technology, modeling, analog, and power devices. In addition, a special session will be held on emerging technologies. A workshop on Compact Modeling will be held the day following the conference. There will be exhibits from vendors with products of interest to those working in the bipolar/BiCMOS area. To complement the technical conference, there will be an exciting social program in the heart of Montreal.

For registration and other information, please visit the IEEE BCTM home page: http://www.ieee-bctm.org

We hope you will join the IEEE BCTM World Tour. See you in Montreal!

Ross Teggatz
BCTM General Chair
Texas Instruments
Dallas, TX, USA

2004 IEEE International SOI Conférence (SOI)

(continued from page 1)

- SOI material science/modification, material characterization, and manufacture
- SOI device Physics and modeling
- SOI circuit applications (high-performance microprocessors, srams, asic, low power, high-voltage, rf, analog, Mixed mode, etc.)
- Double Gate/Vertical Channel Structures; Other Novel Structures
- Strained Si-Ge structures
- New SOI structures, Circuits, and applications (3d integration, displays, microactuators - MEMS, microsensors, Drop-in RAMS, etc.)
- SOI reliability issues (hot-carrier effects, radiation effects, high-temperature effects, etc.)
- Manufacturability and process integration of SOI devices and circuits
- Alternate silicon-on-insulator material.

Abstracts for the 2004 SOI Conference were due no later than May 7, 2004 to: BACM, by e-mail ONLY to SOIPaper@bacminc.com in PDF format. Late newspapers with exceptional merit will be considered for the Late News session if submitted on or before August 15, 2004.

Once again, the popular One-Day Tutorial Short Course will be offered preceding the 2004 SOI International Conference. Tutorial Short Course instructors have many years of experience in the field of silicon-on-insulator technology. The course is intended to educate attendees in detail about current trends and issues in the SOI industry. The 2004 SOI Tutorial Short Course will focus on future trends in SOI technologies including such topics as novel SOI devices and strained silicon on insulator. Participants will receive copies of all visual presentations.

The SOI Conference is held annually throughout the United States. An advisory board and a technical committee, comprised of members from the society throughout the world, guide the conference. The 2004 advisory board members are Dimitris Ioannou (George Mason U), Harold Hovel (IBM), Mike Liu (Honeywell), and Ted Houston (TI). The 2004 conference is organized by: General Chair, Mike Mendicino (Motorola), Technical Program Chair, James Burns (MIT/Lincoln Lab); Local Arrangements Chair, Christophe Tretz (IBM E&TS); Treasurer and Registration Chair, Toshiro Hiramoto (University of Tokyo); Rump and Poster Chair, Mario Pelella (AMD); and Short Course Chair, Pierre Fazan (LEG/EPFL); and technical committee members, Richard Brown (U. Michigan), Jean-Pierre Colinge (UC Davis), Paul Fechner (Honeywell), Samuel Fung (TSMC), Keith Jenkins (IBM Research), William Jenkins (NRL), Shigeru Kawanaka (Toshiba), James Kuo (National Taiwan Univ.), Hector Sanchez (Motorola), Sunit Tyagi (Intel), Rene Zingg (Phillips), Gerry Neudeck (Purdue), Atsushi Ogura (NEC), and Carlos Mazure (SOITEC).

Charleston has made many changes through the last 300 years and presents many faces to the visitor of today. There was the Charles Towne of the 18th century, a wealthy growing city, Charleston of the 19th century during the rise and fall of Southern aristocracy before the American Civil War and the upheaval after the war ended. Like no other city, Charleston has been described, as a "living museum", since parts of the city appear frozen in time.

Despite its emphasis on preservation, Charleston is also a modern city that nurtures theater, dance, music, and visual arts. There is fishing, golf and tennis, beautiful beaches, and island getaways, and a virtual plethora of restaurants & bistros featuring traditional as well as modern adaptations of "Southern food". Charleston is also a gracious 300 year old port city and living historical site that pays homage to its past, celebrates its present and moves gracefully into the future.

Opened in 1924, The Francis Marion Hotel is the largest and grandest in the Carolinas. Rising 12 stories above the historic district, many of the Hotel's guestrooms offer spectacular views of Charleston's church steeples, antebellum mansions and famous harbor. Located downtown on historic Marion Square, the magnificent gardens, house museums, antique shops, local boutiques, restaurants and nightlife that make Charleston unique, are all an easy walk from our conference hotel.

You may contact the 2004 IEEE International SOI Conference for additional information as follows: c/o BACM, 520 Washington Blvd., #350, Marina del Rey, CA 90292, Tel: 310-305-7885; Fax: 310-305-1038; Email: bacm@attbi.com or the SOI Conference website at http://www.soiconference.org.

Michael Liu
SOI General Chair
Honeywell SSED
Plymouth, MN, USA

2004 IEEE International Integrated Reliability Workshop (IRW)

The Integrated Reliability Workshop focuses on ensuring semiconductor reliability through component fabrication, design, characterization, and analysis tools, as well as identification of root cause defects and physical mechanisms responsible for reliability problems. It provides a unique environment for understanding, developing, and sharing reliability technology for present and future semiconductor applications.

Last year's 2003 IRW discussed all aspects of technology reliability and many aspects of product reliability in an informal workshop atmosphere through platform paper presentations, in-depth tutorials, poster sessions, early evening workshops, and the very popular late evening special interest groups. CMOS and BIPOLAR device reliability was discussed both in bulk and SOI. In the ever-challenging quest to shrink gate dielectric thicknesses, both conventional SiO2 and high-K dielectric gates were contrasted. A high-K tutorial as well as a discussion group on this topic ensures it again will be hot in 2004. CMOS device topics included both negative and positive bias temperature instabilities (NBTI, PBTI). An entire session was devoted to BIPOLAR issues which included state of the art band gap engineered Si-Ge BiCMOS. Interconnect fuse and MIMCAP issues were also covered in the course of the papers. Non-contact measurement techniques were presented in a tutorial and discussed further by additional authors in the course of the paper presentations. Two other tutorials included a comprehensive discussion of fast wafer level monitoring for product wafers in manufacturing and a forward looking tutorial giving an update on the status of Magnetic RAMs and their reliability issues.

In 2004 IRW plans to build upon last year's success.

Our Keynote speaker is already chosen, and he will both inspire and challenge us with his opening address. Here is the information about this talk:

Keynote Speaker: Timothy Forhan, Senior VP Corporate Reliability, AMI Semiconductor.

"Managing Tomorrow's Reliability Risks Today"

"In today's world, semiconductor ICs control mission critical functions in airplanes and pacemakers to nuclear reactors and ABS brakes. Big customers use multiple millions of a single part number and easily differentiate 3-ppm performance from .7ppm performance. So, the importance of quality and reliability in our products has never been higher… I hope to share some of our thinking, strategy and results in this area and hopefully set the stage for a healthy exchange on managing tomorrow's risks today. "

In addition, we have planned an exciting venue of Tutorials. They are:

- Gate Dielectric Reliability
- Device Reliability
- Interconnect Reliability
- Negative Bias Temperature Instability (NBTI)
- Cu-Metallization Reliability
- Product Reliability

The deadline for abstract submissions was June 18, 2004 and the Technical Program Chair is Rolf-Peter Vollertsen, Rolf.Vollertsen@infineon. com. The categories for the papers for this year's platform and poster presentations submissions are:

- Wafer level reliability tests and test approaches
- Identification of new reliability effects & characterization
- Reliability models and simulations
- Reliability test structures
- Customer product relia bility requirements/ manufacturer reliability tasks
- Designing-in reliability (circuits, processes, products)

For the interested reader, or first-time participant, please go to the IRW website and download the full call for papers: http://www.irps/irw

Finally, a brief checklist for your consideration and investigating IRW 2004 further:

When: October 18-21 2004

Where: Stanford Sierra Camp, South Lake Tahoe, CA

Technical Program Chair: Rolf-Peter Vollertsen, Infineon Technologies, Rolf.Vollertsen@infineon.com

Abstract submission deadline: June 18,2004

General Chair: Al Strong, IBM Technology Reliability astrong@us.ibm.com

Web Site: http://www.irps.org

Whether you are interested in presenting a paper, or interested in sharpening your skills through the wonderful interaction that takes place at IRW, we are looking forward to meeting you at the conference!

Alvin Strong
IRW General Chair
IBM Technology Reliability
Essex Junction, VT, USA

Society News

Announcement of Newly Elected AdCom Members

On December 7, 2003, the EDS AdCom held its annual election of officers and members-at-large. The following are the results of the election and brief biographies of the individuals elected.

I. OFFICERS

The following individuals were elected as officers beginning 1/1/2004:

HIROSHI IWAI (President, with a two-year term) is a professor of Frontier Collaborative Research Center, Tokyo Institute of Technology (TIT). Before joining TIT, he worked at Toshiba Corporation for 26 years, having developed advanced Si device technologies. He was also a visiting scholar at Stanford in 1983 and 84. He received the B.E. and Ph.D. degrees in electrical engineering from the University of Tokyo, Japan in 1972 and 1992, respectively.

He is currently the EDS Regions/Chapters Committee Chair. He has served for many years with IEEE/EDS, as an Elected AdCom member, an editor of the EDS Newsletter, and the chair of a number of EDS conferences.

ILESANMI ADESIDA (President-Elect, with a two-year term) received his Ph.D. in electrical engineering from the University of California, Berkeley, in 1979. From 1979 to 1984, he worked in at Cornell University. He was the Head of the Electrical Engineering Department at Tafawa Balewa University, Bauchi, Nigeria, from 1985 to 1987. In 1987, he joined the University of Illinois at Urbana-Champaign, where he is currently the Donald Biggar Willet Professor of Engineering and the Director of the Micro and Nanotechnology Laboratory. He was on the EDS Administrative Committee and Chaired the EDS Education Activities Committee. He has served on the organizing committees of various international conferences and served as an Associate Editor of the Journal of Electronic Materials. He was awarded the Oakley-Kunde Award for Excellence in Undergraduate Education in 1994, named a University Scholar in 1997, and became an Associate Member of the Center for Advanced Study at the University of Illinois in 1999. He is a Fellow of IEEE and AAAS.

PAUL K.L. YU (Treasurer, with a one-year term) received his Ph.D. from the California Institute of Technology in 1983. That same year, he joined the faculty of the Department of Electrical and Computer Engineering at the University of California at San Diego (UCSD) where he has been a professor since 1993. At UCSD, he conducts research in materials and device for fiber optics and optoelectronics applications. He is a Senior Member of IEEE, a Distinguished Lecturer of the EDS and a member of OSA. Currently, his research focus is in solving problems for microwave photonics systems. He has published more than 100 papers in the area of photonics.

JOHN K. LOWELL (Secretary, with a one-year term) received the Ph.D. degree in Applied Physics from the University of London. He has held technical and managerial assignments for United Technologies, Northern Telecom, Mostek, Texas Instruments, British Telecom/Dupont, AMD, Applied Materials, Oracle and most recently PDF Solutions. He has also been a Professor at Texas Tech University and in the University of Texas system, and held Consulting Professorships at other universities in addition to being a Visiting Scholar at the NSF Center for the Synthesis, Growth and Characterization of Electronic Materials at the University of Texas at Austin.

Dr. Lowell is a Senior Member of the IEEE, a Distinguished Lecturer of the EDS and has held AdCom-level positions previously within the LEO and CAS societies. For fifteen years, he was also the Associate Editor-in-Chief of the IEEE Division I *Circuits & Devices Magazine*, and was its Guest Editor twice.

II. ADCOM MEMBERS-AT-LARGE

A total of seven persons were elected to three-year terms (2004-2006) as members-at-large of the EDS AdCom. Three of the seven individuals were re-elected for a second term, while the other four were first-time electees. The backgrounds of the electees span a wide range of professional and technical interests.

A. SECOND TERM ELECTEES:

TOSHIRO HIRAMOTO received B.S., M.S., and Ph.D degrees in electronic engineering from the University of Tokyo in 1984, 1986, and 1989, respectively. In 1989, he joined the Device Development Center, Hitachi Ltd., Ome, Japan, where he was engaged in the device and circuit design of ultra-fast BiCMOS SRAMs. In 1994, he joined the Institute of Industrial Science, University of Tokyo, Japan, where he has been a Professor since 2002. His research interests include low power and low voltage design of advanced CMOS devices, SOI MOSFETs, device/circuit cooperation scheme for low power VLSI, quantum effects in nano-scale MOSFETs, and silicon single electron transistors. He served as the General Chair of Silicon Nanoelectronics Workshop in 2003, and the Program Chair in 1997, 1999, and 2001.

LEDA LUNARDI holds a Ph.D. in electrical engineering from Cornell University. From 1985 to 2000, she was with AT&T Bell Labs, in New Jersey, where her research was in high-speed devices for light wave systems. From 2000-2003, she was with JDS Uniphase.

Since 2003, she has been a professor at the Department of Electrical and Computer Engineering, North Carolina State University, Raleigh with research interests in nanotechnology and photonic devices for communication systems.

Dr. Lunardi is an IEEE Fellow and co-recipient of the 2000 LEOS Engineering Achievement Award She has published over 90 refereed papers and conference talks. Presently, she is the editor of Optoelectronic Devices for *IEEE Transactions on Electron Devices*.

HON-SUM PHILIP WONG received the Ph.D. degree in electrical engineering from Lehigh University, Pennsylvania, in 1988. He joined the IBM Thomas J. Watson Research Center, Yorktown Heights, New York, in 1988, as a Research Staff Member. He is now Senior Manager of the Nanoscale Materials, Processes, and Devices Department. He has the responsibility of shaping and implementing IBM's strategy on nanoscale science and technology. Prior to this appointment, he was Senior Manager of the Exploratory Devices and Integration Technology Department. His department was responsible for defining and executing IBM's exploratory devices and technology roadmap for silicon technology

He has worked on CCD's, CMOS image sensors, device modeling, double-gate FET, strained Si CMOS, ultrathin body SOI, device applications of wafer bonding, and most recently, Ge FET, and carbon nanotube FET.

He is a Fellow of the IEEE and has served on both the IEDM committee and ISSCC Program committee since 1998. He is a member of the Emerging Research Devices Working Group of the International Technology Roadmap for Semiconductors (ITRS).

B. FIRST-TIME ELECTEES:

STEVE S. CHUNG received his Ph.D. degree from the University of Illinois at Urbana-Champaign, in Electrical Engineering in 1985.

He is currently a Professor and Chairman of EECS Undergraduate Honors Program and also a Professor with the Electronics Engineering Department at the National Chiao Tung University. In the Fall Quarter of 2001, he was a Research Visiting Scholar with Stanford University. His current research areas include CMOS devices; flash memory, and reliability characterization and modeling; and nanoelectronics in bio applications. He has published more than 130 journal articles and conference papers, one undergraduate textbook, and holds more than 15 US and ROC patents.

Dr. Chung is a Senior member of IEEE, DL of EDS, Editor of EDL and the Chair of the ED Taipei Chapter. He has served on the committees of major conferences, e.g., VLSI Technology, IEDM, IRPS, etc. He has also been the Technical Program Chair of the 2004 IPFA and EDMS. His chapter was awarded the 2002 EDS Chapter of the Year Award and he received the Outstanding Research Award from the National Science Council, Taiwan several times. He was also granted Distinguished EE Professor and Engineering Professor by the Engineering Societies of Taiwan.

MARK S. LUNDSTROM is the Don and Carol Scifres Distinguished Professor of Electrical and Computer Engineering at Purdue University. He received his B.E.E. and M.S.E.E. degrees from the University of Minnesota and then worked for Hewlett-Packard on integrated circuit processes. After completing his Ph.D. on photovoltaics at Purdue, he joined the faculty in Electrical Engineering in 1980. His teaching and research currently center on the physics technology, and simulation of electronic devices. Lundstrom is the founding director of the NSF funded Network for Computational Nanotechnology. He is an IEEE Fellow and a co-recipient of the 2002 Cledo Brunetti Award for his work on nanoscale electronics.

ALBERT WANG received his B. Eng. and PhD degrees in EE from Tsinghua University, China and State University of New York at Buffalo in 1985 and 1996, respectively. He was with National Semiconductor until 1998 when he joined the Faculty of ECE of Illinois Institute of Technology, where he is an Associate Professor and directs the Integrated Electronics Laboratory. His research interests center on analog/mixed-signal/RF ICs, on-chip ESD protection, IC CAD and modeling, SoCs and semiconductor devices, etc. He received the NSF CAREER Award in 2002. He is the author of one book and more than seventy papers, and holds several U.S. patents. He is an Editor for the *IEEE Electron Device Letters*, an Associate Editor for the *IEEE Transactions on Circuits and Systems I*. He is an IEEE Distinguished Lecturer for the Electron Devices Society and the Solid-State Circuits Society.

XING ZHOU received his B.E. degree in electrical engineering from Tsinghua University in 1983, M.S. and Ph.D. degrees in electrical engineering from the University of Rochester in 1987 and 1990, respectively. He is currently an Associate Professor in the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore. His past research interests include Monte Carlo simulation of photo carrier transport and ultra fast phenomena as well as mixed-mode circuit simulation and CAD tool development. His recent research mainly focuses on nanoscale CMOS technology and device compact modeling. He is a Senior Member of the IEEE, a member of the EDS Compact Modeling and Regions/Chapters committees, an EDS Newsletter Editor for Region 10, and an EDS Distinguished Lecturer.

EDS Administrative Committee Election Process

The Members-at-Large (MAL) of the EDS AdCom are elected for staggered three-year terms, with a maximum of two consecutive terms. The 1993 Constitution and Bylaws changes mandated increasing the number of elected MAL from 18 to 22, and required that there be at least two members from both IEEE Region 8 (Europe, Middle East & Africa) and Region 10 (Asia & Pacific). In 2003, EDS made changes to its Constitution and Bylaws to require that at least one elected AdCom member is a Graduate of the Last Decade (GOLD member). A GOLD member is defined by IEEE as a member who graduated with his/her first professional degree within the last ten years. It is also required that there be at least 1.5 candidates for each opening. From 2001 to 2003, seven, eight and seven positions were filled, respectively. In 2004, seven positions will be filled.

The election procedure begins with the announcement and Call For Nominations in the EDS Newsletter. The slate of nominees is developed by the EDS Nominations Committee and includes the non-Committee and self-nominations received. Nominees are asked to submit a two-page biographical resume in a standard format. Nominations are closed on 15 October, and the biographical resumes are distributed to the 'full' voting members of AdCom prior to the December AdCom meeting. The election is then held after the conclusion of the meeting. The nominees do not need to attend the AdCom Meeting/Election to run. On the other hand, if you are elected, you are expected to attend the two AdCom meetings a year. In general, the travel and accommodation costs to attend these meetings are borne by the elected member.

A continuing flow of new AdCom members who are interested in working for the improvement of the Society and its related technical areas is essential for the continued development of EDS and the field of electron devices. Those interested in the field, the Society, and its operations are encouraged to attend AdCom meetings, become involved in Society activities, and consider running for election to AdCom.

Steven J. Hillenius
EDS Nominations & Elections Chair
Agere Systems
Allentown, PA, USA

Call For Nominations - EDS AdCom

The Electron Devices Society of the IEEE invites the submission of nominations for election to its Administrative Committee (AdCom). Presently, the AdCom meets twice per year and is composed of 22 members. Seven members will be elected this year for a term of three years, and a maximum of two consecutive terms is allowed. In 2004, the election will be held after the AdCom meeting on Sunday, 12 December. Electees begin their term in office on 1 January 2005. For your information, the nominees do not need to attend the AdCom Meeting/Election to run.

Nominees are being sought to fill the slate of candidates. Nominees may be self-nominated, or may be nominated by another person; in the latter case, the nominee must have been contacted and have agreed to serve if elected. Any member of EDS in good standing is eligible to be nominated. As another condition for nomination and election, a nominee is expected to attend the two annual AdCom meetings. In general, the travel and accommodation costs to attend these meetings are borne by the elected member.

In 2003, EDS made changes to its Constitution and Bylaws to require that at least one elected AdCom member is a Graduate of the Last Decade (GOLD member). A GOLD member is defined by IEEE as a member who graduated with his/her first professional degree within the last ten years. We encourage and are looking forward to receiving nominations from EDS members in this category.

Please send your nominee's name, address, and supporting information to the EDS Executive Office Administrator, Laura J. Riello, IEEE, 445 Hoes Lane, Piscataway, NJ 08854, Fax: 732-235-1626, E-Mail: l.riello@ieee.org in time to be received by the deadline of 15 October 2004. It is very desirable that submissions include a biographical summary in a standard two-page format. The EDS Executive Office can provide you with an example of the format. If you have any questions regarding the nomination requirements or process, feel free to contact the Nominations and Elections Chair, Steven J. Hillenius (s.hillenius@ieee.org).

Call for EDS Chapter Subsidies for 2005

The deadline for EDS chapters to request a subsidy for 2005 is 1 September 2004. For 2004, the EDS AdCom awarded funding to 52 chapters, with most amounts primarily ranging from US$250 to US$1,000. In June, Chapter Chairs were sent an e-mail notifying them of the current funding cycle and providing them with a list of guidelines. In general, activities which are considered fundable include, but are not limited to, membership promotion travel allowances for invited speakers to chapter events, and support for student activities at local institutions. Subsidy requests should be sent via e-mail, fax or mail to the EDS Administrator, Laura J. Riello, IEEE, EDS Executive Office, 445 Hoes Lane, Piscataway, NJ 08854, l.riello@ieee.org or fax 732 235 1626. Prior to the submission of the subsidy request, the Chapter Chair must submit a chapter activity report to its respective SRC Chair and Laura Riello of the EDS Executive Office by July 1. This report should include a general summary of chapter activities (one to two pages) for the prior July 1st - June 30th period. You must also attach a copy of the activity report to your chapter subsidy request. Final decisions concerning subsidies will be made by the EDS SRC Chairs/Vice Chairs in early November. Subsidy checks will be issued by late January.

EDS Standing Committee Reports – Regions/Chapters & Membership

EDS Regions/Chapters Committee Report

- by Cor L. Claeys, EDS Vice President of Regions/Chapters

Cor L. Claeys

The EDS Regions/Chapters Committee (RCC) has been very active and successful during the last year. In the last 6 months of 2003, new ED chapters were formed in Eastern North Carolina, Orange County, Calcutta, and a Student Chapter in Louvain-La-neuve, Belgium, bringing the total to 109 chapters. For the moment the formation of an additional 15 chapters is under discussion and progressing well. This clearly indicates the strong interest and need for ED chapters. The quality of the chapter activities organized by the chapters is monitored and triggered by the Chapter of the Year Award. In 2003 there was a tough competition for the award with the ED Boise Chapter being the winner.

The re-organization of the RCC into 5 subcommittees (North America East, North America West, Europe-Africa-Middle East, Latin America, and Asia-Pacific) has turned out to work efficiently and has strongly increased the interactions between the Chapters and the Society. Beginning this year, several additional Vice-Chairs of these subcommittees have been appointed. Region 9 is starting with a new initiative, called the Outstanding Student Paper Award, whereby an award will be given to a regional student who authored or co-authored during the previous year a paper or conference manuscript in an IEEE Journal or Proceedings Volume. Depending on the success of this initiative, it may be extended to other regions as well.

Regional chapter meetings have been organized in Region 9 (Sao Paulo, September) and Region 2 (Washington DC, December). In May, a Region 8 meeting was held in conjunction with the Ed AdCom meeting in Madrid, Spain. The organization of mini colloquia, in which 5 to 10 Distinguished Lecturers are participating, is a very successful formula attracting many attendees. The most recent ones were organized in Sao Paulo (September 2003, Seoul (September 2003), Singapore (October 2003) and Bombay (October 2003), and in May in Madrid, Spain. More and more chapters are also making use of the Distinguished Lecturer Program.

The near future strategic activities will be focusing on issues related to:

- Increasing the number of chapters and Student chapters in Latin America.
- Special actions to promote the formation of new chapters in India and China, both which have a very strong potential in ITC and are growing fast. Attention will have to be given to local circumstances.
- Extending in some Regions, the number of local Distinguished Lecturers.
- Further intensifying interaction between the chapters and the Society, whereby the role of Chapter Partners is very important

Activities and Future Plans of the EDS Membership Committee

-by James B. Kuo, EDS Vice President of Membership

James B. Kuo

EDS membership has been quickly becoming globalized these days. From the 2003 EDS membership statistics, the US (Region 1-6) has 57.6% of the total membership, Asia and the Pacific Region (Region 10) has 20.6% and Europe, Middle East & Africa (Region 8) has 18.3%. According to the statistics in the recent years, non-US membership becomes more and more important. Nowadays the worldwide semiconductor industry is reconfiguring its territory at a quick pace. In compliance with the EDS strategic planning position statement to ensure EDS activities reflect the current and the future global trends, the EDS Membership Committee has been working to create new strategies in membership promotion. In addition to on-site membership promotion at important conferences and various other promotional events held over the years, EDS membership promotion has been successful from other programs such as the Senior Membership Program (SMP) and the Membership Fee Subsidy Program (MFSP). Among the 38 societies of IEEE, EDS has the most successful SMP program for the past two years. At the last AdCom meeting, an improved SMP program has been approved for further success in membership retention at EDS. Also the first-year Partial Membership Fee Subsidy Program (PMFSP), which is derived from MFSP, has also been approved for attracting potential members. To further increase EDS membership, promoting new chapters in the under-served regions, especially in China and India, is another major strategy. In conjunction with the Regions/Chapters and Education committees, via frequent, short visits to major universities coordinated through the Distinguished Lecturers Program, we hope to develop new chapters in the under-served regions. In China, in addition to the current Beijing and Shanghai chapters, EDS is currently in the process of forming chapters in Xi'an and Nanjing, to better reflect the booming semiconductor industry and research activities there. A similar situation exists in India. EDS membership promotion is every member's business. We encourage every one of you to get involved.

EDS Technical Committee Reports – Photovoltaic Devices & VLSI Technology & Circuits

EDS Photovoltaic Devices Technical Committee Report

-by Dennis J. Flood, EDS Photovoltaic Devices Chair

Dennis J. Flood

The Photovoltaic Devices Technical Committee's (PVDTC)'s primary responsibility is to keep the EDS apprised of the latest worldwide results in photovoltaic device and system research and development, and the status of world markets and applications. The Committee will provide the EDS with highlights from each major conference and will track emerging technologies reported in the peer-reviewed literature. The Committee's membership represents each major geographical region with a significant level of activity in both R&D programs and commercialization efforts. At present, those regions are North America, Europe, Japan/Asia and Australia/South Pacific.

Reports to the EDS will come in the form of short white papers (one to three pages) that will be made available to IEEE members via direct request to the PVDTC, pending IEEE/EDS approval. The first such white paper will be issued following the European Photovoltaic Solar Energy Conference and Exhibition, held in Paris, France, June 7-11, 2004. (For those interested in more information on the European Conference, which is now the largest in the world, please go to http://www.photovoltaic-conference.com/ for further information). Information on the next IEEE Photovoltaic Specialists Conference, to be held in Orlando, Florida Jan. 3-8, 2005, will soon be available via the web.

Current PVDTC members and the areas each represents are: North America: Dennis Flood dflood140@oberlin.net); John Meakin (meakin@ME.UDel.Edu); David Carlson (dave.carlson@bp.com); Nicola Pearsall (nicola.pearsall@unn.ac.uk) and one other to be named; Japan/Asia: Masafumi Yamaguchi (masafumi@toyotati.ac.jp) and Kosuke Kurokawa (kurochan@ cc.tuat.ac.jp); and Australia/South Pacific: Martin Green (m.green@ unsw.edu.au).

EDS VLSI Technology & Circuits Technical Committee Report

-by Bin Zhao, EDS VLSI Technology & Circuits Chair

Bin Zhao

Six new members joined the VLSI Technology and Circuits Technical Committee at the beginning of 2004. The committee now has 17 members representing a very wide spectrum of technical expertise in VLSI devices, technology, and circuits. The present members are: Ilesanmi Adesida (University of Illinois), Joe Brewer (University of Florida), Steve Chung (National Chiao Tung University), Jamal Deen (McMaster University), James Hutchby (SRC), Shuji Ikeda (Trecenti Technologies), Jason Jenq (UMC), Mark Law (University of Florida), Kwyro Lee (KAIST), Yanhe Li (Tsinghua University), Huiling Shang (IBM), Roland Thewes (Infineon), Akira Toriumi (University of Tokyo), Albert Wang (Illinois Institute of Technology), Jeffery Welser (IBM), Reinout Woltjer (Philips), and Bin Zhao (Skyworks) - Chair.

Since its formation in 1998, the VLSI Committee has chartered its missions to identify new technical trends, to help foster new technical concepts, and to serve the emerging needs of the Electron Devices and Solid-State Circuits communities in VLSI. The committee achieves these missions by initiating topical workshops, proposing special journal issues to cover important VLSI topics, organizing or supporting panel sessions, special sessions, and short courses at major conferences. Recent work accomplished by the committee and its members includes:

- The International Workshop on Future Information Processing Technologies held in Nov. 2003.
- Chaired the section of "Emerging Research Devices" in the International Technology Roadmap for Semiconductors (ITRS) – released in Dec. 2003.
- Co-chaired the section of "RF and Analog/Mixed-Signal IC Technologies for Wireless Communications" in the ITRS Roadmap – released in Dec. 2003.
- A special issue on "Integrated Circuit Technologies for RF Circuit Applications" of Transactions on Electron Devices has been approved – it will be published in March 2005.
- Workshop on Compact Modeling held in March 2004 at the 7th International Conference on Modeling and Simulation of Microsystems.
- Emerging Memory Workshop held at Stresa, Italy in April 2004.

In 2004, the committee continues its tradition to help the IEDM by providing suggestions and support for the Evening Panel Sessions and the Emerging Technologies Session. We continue to work with ITRS Technical Working Groups in "Emerging Research Devices/Materials" and "RF and Analog/Mixed-Signal IC Technologies for Wireless Communications" for the ITRS 2004 update. The committee's other on-going activities include: organizing the International Workshop on VLSI Technologies and Circuits for RF Applications, Aug. 2004; organizing a short course and a panel session at the International Conference on Solid-State and Integrated-Circuit Technology, Oct. 2004; organizing several special journal issues on "Non-Classical CMOS Devices and Technologies: Extending the Roadmap," "Advanced Non-Volatile Memory Technologies for Embedded Applications," "Heterogeneous Integration of Dissimilar Technologies," "Information Processing Technology and Circuit Architectures beyond CMOS," etc.

Looking forward, the VLSI Committee will continue to focus on identifying emerging trends in VLSI devices and technologies, enhancing the bridge between VLSI technologies and circuits, and promoting VLSI technical activities globally. If you have ideas and suggestions for the VLSI Committee to better serve your interests and needs, please contact us. For more information on the committee and our activities, please visit our website: http://www.ieee.org/society/eds/technical_committees/vlsi.

Compound Semiconductor Roadmap Embedded in the 2003 International Technology Roadmap for Semiconductors

The purpose of this article is to give the EDS community a few highlights on compound semiconductors from the perspective of the 2003 International Technology Roadmap for Semiconductors (ITRS). This article mentions briefly only a portion of the work done by the ITRS Technical Working Group on RF and Analog-Mixed Signal (AMS) Technologies for Wireless Communications.

A technology roadmap for RF and AMS applications of compound semiconductors now exists in the 2003 ITRS. Past ITRS roadmaps focused on mainstream CMOS and BiCMOS processes and applications. For the first time, the current 2003 ITRS Roadmap includes III-V compound semiconductors in the context of CMOS technology nodes. To locate this part of the 2003 ITRS, please browse to http://public.itrs.net/Files/2003ITRS/Home2003.htm and then click on the RF and AMS Technologies for Wireless Communications Chapter. This Chapter addresses the intersection of Si based technologies and III-V compound semiconductor based technologies. It presents technical challenges and requirements that RF and AMS technologies must meet for successful deployment in wireless applications that span the frequency range from 0.8 GHz to 100 GHz. Such applications include such cellular phone transceivers, cellular base station amplifiers, wideband local area networks, automotive radar, all weather landing, and the like.

Wireless applications have grown quickly to become significant markets for semiconductor device manufacturers. The 2003 ITRS now recognizes wireless applications enabled by RF and AMS devices and circuits as a separate new system and technology driver. In contrast to the other three ITRS drivers, which are the DRAM, MPU, and ASIC, the correlation between feature size and device performance is weaker for RF and analog devices. Gordon Moore's first law [1] is used to assess the density of mainstream CMOS based devices and is only one among many competing ways to assess the performance of RF and AMS devices. Instead, RF and analog devices must meet many other performance specifications and parameters that do not scale in the same manner as CMOS device metrics scale.

The most important drivers for wireless communications systems are cost, time to market, available frequency bands, power consumption, functionality, size of mobile units, very high volumes of product, appropriate performance requirements, and standards and protocols. Standards and protocols often affect advances in RF and AMS technologies much more than they affect advances in many of the other CMOS technologies. They influence considerably parameters such as operating frequency, channel bandwidth, and acceptable transmit power. Such standards and protocols impact overall system performance and include regulations from various governments that determine frequency availability, systems compatibility, and market shares.

The technology requirements for meeting the demands of wireless systems are manifold, often conflicting and very different from digital requirements. Thus, we see often today in wireless systems a combination of specialized RF and analog technologies such as Si CMOS, SiGe, Si BiCMOS, Si LDMOS, GaAs MESFET, GaAs PHEMT, GaAs HBT, InP HEMT, and InP HBT. Integration is closely related to and to a great extent dictated by cost and performance targets. Depending on requirements either monolithic system on chip or system in package (SiP) integration may be preferred. When required, the SiP approach is especially suited to bring the specialized RF and AMS technologies together in a highly integrated, high-performance, and lower cost unit.

RF technologies often require added tolerances for the values of performance parameters because several conflicting or competing requirements must be met simultaneously. Therefore, design compromises must be made among competing performance parameters such as dynamic range, PAE, linearity, high output power, low current, and low voltage. For example, the effective bit resolution of analog-to-digital converters should be greater than what is needed for fulfilling a given communication specification in order to perform signal error correction in "real time" and to keep latency to a minimum. Increased RF performance for silicon is predominantly achieved by geometrical scaling. Increased RF performance for III-V compound semiconductors is achieved by optimizing carrier transport properties through materials and bandgap engineering.

Acronyms

AMS	analog-mixed signal
ASIC	application-specific integrated circuit
BiCMOS	bipolar-complementary metal oxide semiconductor
CMOS	complementary metal oxide semiconductor
DRAM	dynamic random-access memory
EDS	Electron Devices Society
HBT	hetero bipolar transistor
HEMT	high electron mobility transistor
LDMOS	laterally diffused metal oxide semiconductor
MESFET	metalsemiconductor transistor
MHEMT	metamorphic high electron mobility transistor
MPU	multiprocessing unit
PAE	power added efficiency
PHEMT	pseudomorphic high electron mobility transistor
RF	radio frequency

The locations of boundaries, shown schematically in Figure 1, between the kinds of RF semiconductors (e.g., Si, SiGe, GaAs, and InP) are broad, are diffuse, change with time, and depend very much on cost. The boundaries between the group IV semiconductors Si and SiGe and between SiGe and the III-V semiconductor GaAs have been moving to higher frequencies with time and for other applications the boundary between GaAs and InP is tending to shift to lower frequencies. Eventually, MHEMTs may displace both GaAs PHEMTs and InP HEMTs. The wide bandgap semiconductors, not shown in Figure 1, such as SiC and GaN will be used for infrastructure such as cellular base stations at frequencies typically above about 2 GHz. When high volumes of product are expected, silicon and more recently SiGe replace the III-Vs in those markets for which group IVs can deliver appropriate performance at low cost. In future years, carrier frequency is expected to lose its significance in defining the boundaries among technologies for some applications, because most of the RF technologies can provide very high operating frequencies. Future boundaries will be dominated more by such parameters as noise figure, output power, PAE, linearity, and cost. Two or more technologies may coexist with one another for certain applications such as cellular transceivers, modules for terminal or base station power amplifiers, and mm-wave receivers. The "future" for compound semiconductors has arrived.

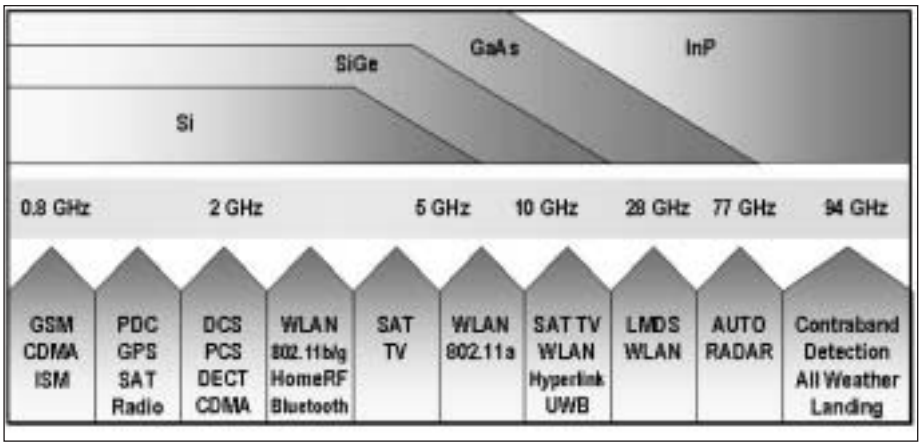

Figure 1: Application Spectrum (The format and style used here are adapted from Fig.1 in Microwave Journal of the paper by D. Barlas et al., page 22, June 1999, and are printed with permission from the Editor, Microwave Journal.)

This article is based in part on 1) the paper entitled Circuits and Device for Wireless Communications, submitted to the IEEE Circuits and Devices Magazine for publication in the June 2004 issue and 2) on the 2003 ITRS Chapter entitled RF and Analog Mixed-Signal Technologies for Wireless Communications, Semiconductor Industry Association, International Technology Roadmap for Semiconductors, 2003 edition, International SEMATECH:Austin, TX, 2003. The ITRS logo is used by permission from the Semiconductor Industry Association, The International Technology Roadmap for Semiconductors, 2003 edition. International SEMATECH:Austin, TX, 2003.

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Congratulations to the EDS Members Elected to the National Academy of Engineering (NAE)

The U.S. National Academy of Engineering (NAE) elected twenty-five IEEE members in 2004, 22 as NAE Members and 3 as NAE Foreign Associates. Three of the twenty-five members elected are EDS members. These members will be inducted into the NAE this October.

A private, nonprofit institution, the NAE has more than 2,100 peer-elected members and foreign associates-senior professionals in business, academia and government who are among the world's most accomplished engineers.

The three EDS members elected in 2004 were elected as NAE Members. They are: Fellow, Young-Kai Chen; Fellow, Paul D. Dapkus; and Member, Daniel C. Tsui.

The other nineteen IEEE members elected as NAE Members are: Fellow, Siva S. Banda; Fellow, Rodney A. Brooks; Fellow, Vernon L. Chartier; Fellow, Larry A. Coldren; Fellow, Eli Fromm; Fellow, Richard Gambino; Member, Van Jacobson; Fellow, Biing-Hwang (Fred) Juang; Senior Member, Pradman P. Kaul; Senior Member, Yoram Koren; Member, Frank T. Leighton; Fellow, Joan L. Mitchell; Member, Raymond E. Ozzie; Life Fellow, Andrew P. Sage; Fellow, Alfred Z. Spector; Senior Member, Bjarne Stroustrup; Senior Member, Ronald D. Sugar; Fellow, Vijay Vittal; and Member, Victor W. Zue.

The three IEEE members elected as a NAE Foreign Associate are: Fellow, Tatsuo Izawa; Fellow, Lennart Ljung; and Member, Pierre Perrier.

Our congratulations to all the IEEE members elected to this prestigious institution.

Jerry M. Woodall
Yale University
New Haven, CT, USA

Status Report from the 2003 EDS Graduate Student Fellowship Winners

In 2000, the IEEE approved the establishment of the Electron Devices Society Graduate Student Fellowship Program. The Program is designed to promote, recognize, and support graduate level study and research within the Electron Devices Society's Fields of Interest: which include: All aspects of the physics, engineering, theory and phenomena of electron and ion devices such as elemental and compound semiconductor devices, organic and other emerging materials based devices, quantum effect devices, optical devices, displays and imaging devices, photovoltaics, solid-state sensors and actuators, solid-state power devices, high frequency devices, micromechanics, tubes and other vacuum devices. In deference to the increasing globalization of our Society, at least one fellowship is to be awarded to students in each of three geographical regions: Americas, Europe/Mid-East/Africa, and Asia & Pacific.

In July 2003, EDS announced the winners of the 2003 Fellowships'. The two winners were: Yu-Long Jiang of Fudan University, Shanghai, China and Javier Salcedo of the University of Central Florida, Orlando, FL, USA. The winners are pursuing distinctly different research topics for their doctoral degrees. The following are brief progress reports written by the award winners.

Yu-Long Jiang

Yu-Long Jiang is a Ph.D. student in the Department of Microelectronics at the Fudan University, Shanghai, China. His supervisors are Professor Bing-Zong Li and Professor Guo-Ping Ru.

Yu-Long spent a year in Axcelis Technologies, Inc., Beverly, Massachusetts, from February 2003 to February 2004, as a visiting scholar. He collaborated with scientists from Axcelis and performed research of nickel silicide formation on a shallow junction. He continued his research in this area after returning to Fudan University.

Yu-Long published several papers since winning the IEEE EDS graduate student fellowship. A paper entitled "The reaction characteristics of ultra thin Ni film on undoped and doped Si (100)" authored by him has been accepted for publication by the *Journal of Electronic Materials*. Another paper entitled "Dopant redistribution induced by Ni silicidation at 300oC" has been published in the Proceedings of the Fourth International Workshop on Junction Technology (IWJT-2004). He gave an oral presentation in this workshop. He also helped to organize this workshop and edit the electronic proceedings, which is sponsored by the IEEE/EDS and EDS Shanghai Chapter. Besides he has submitted two papers, one to *Applied Physics Letters* to explain the electrical dependence of nickel silicide film formed at low temperature on the substrate dopant type and another one to *IEEE Electron Devices Letters* to demonstrate the improvement of nickel silicide/Si interface properties by a 2-step RTP technology. He also co-authored (second author) an invited paper on nickel silicide for the International Conference on Materials for Advanced Technologies-2003 in Singapore.

Yu-Long also paid great attention on the collaboration with semiconductor industries. The friendship between Fudan University and Axcelis Technologies, Inc. has been strengthened with Yu-Long's hard research work at the company headquarters. His joint research work with Axcelis Technologies in nickel silicide has attracted the interest of many local fabs in China. He was invited by the Semiconductor Manufacturing International (Shanghai) Corp. (SMIC) to introduce nickel silicide studies, which greatly pushed forward the research collaboration between Fudan Univeristy and SMIC for 65nm node.

Javier A. Salcedo

Javier A. Salcedo The IEEE Electron Devices Society 2003 Graduate Student Fellowship Award presented to me at IEDM in December 2003 represents a memorable personal distinction. I wish to thank the EDS for the recognition and the support this prestigious award embodies. I would like to express my gratitude as well, to my family, Simón Bolívar University (USB) and my former teachers at the USB Solid-State Electronics Laboratory, my Ph.D. advisor at the University of Central Florida (UCF), Dr. Hefner's SoC Group at NIST, and the Reliability Group at Intersil Corporation, all of whom have provided priceless guidance and support for my personal and professional development.

This EDS Award has partly supported my research work at UCF dealing with the study of novel thyristor-based electrostatic discharge (ESD) protection cells. In particular it has contributed with my projects related to design, modeling and optimization of multiple variables in the ESD protection cell and its ultimate on-chip integration. As a result, superior ESD performance and I-V characteristics not previously observed in other ESD devices have been obtained. A detailed study of the physics of these ESD cells and of the design criterion extendable to different technologies is currently under way. These novel ESD protection cells appear very promising for a wide range of advanced IC applications and result to be increasingly important for highly integrated system-on-a-chip applications, where silicon area is a critical concern. Two ESD protection systems are being currently designed and optimized with the use of thyristor-based cells calibrated within different fabrication processes for very demanding ESD stress conditions and wafer area constrains. One is for the protection of communications ICs, the other for protecting MEMS chips with embedded gas sensors. My research work has so far resulted in the filing of a patent and the submission of two conference papers.

Ilesanmi Adesida
EDS President-Elect & VP of Educational Activities
University of Illinois
Urbana, IL, USA

Stephen A. Parke
EDS Graduate Student Fellowship Chair
Boise State University
Boise, ID, USA

Congratulations to the EDS Members Recently Elected to IEEE Senior Member Grade!

Chew Hoe Ang*
Joseph Barnard
Edward Y. Chang*
Cynthia A. Colinge*
Tianhong Cui
Jody N. Defazio
Pankaj Dixit*
Maxim Ershov
Alois P. Freundorfer
Kirk S. Giboney
Toshihiko Hamasaki
Koji Hasegawa
Ahmed Hemani
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Rajendra M. Patrikar
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Marathe A. Shashishekar
Jyuo-Min Shyu
Chang-Feng Wan
James C. Weiler, Jr.
Kazuhisa Yamauchi
Jiong Zhang*

* = Individual designated EDS as nominating entity

If you have been in professional practice for 10 years, you may be eligible for Senior Membership, the highest grade of membership for which an individual can apply. New senior members receive a wood and bronze plaque and a credit certificate for up to US $25 for a new IEEE society membership. In addition, a letter will be sent to employers, recognizing this new status.

For more information on senior member status, visit http://www.ieee.org/membership/grades_cats.html#SENIORMEM To apply for senior member status, fill out an application at http://www.ieee.org/organizations/rab/md/smelev.htm.

Call for Nominations for the EDS Chapter of the Year Award

The EDS Chapter of the Year Award is given each year based on the quantity and quality of the activities and programs implemented by the chapters during the prior July 1st – June 30th period. Nominations for the award can only be made by Chapter Partners, SRC Chairs/Vice-Chairs, or self-nominated by Chapter Chairs.

The winning chapter will receive a certificate and check for $1,000 to be presented at the International Electron Devices Meeting (IEDM).

The schedule for the award process is as follows:

Action	Date
Call for Nominations E-Mailed to Chapter Chairs, Chapter Partners, SRC Chairs & SRC Vice-Chairs	6/1
Deadline for Nominations	9/15
Regions/Chapters Committee Selects Winner	Early-October
Award given to Chapter Representative at IEDM	First week of December

IEDM Short Courses on Videotape

The 2003 IEEE International Electron Devices Meeting was held this past year in Washington, DC. The two short courses that were offered at this meeting were titled, "Interconnect Scaling: From Technology to System Design" and "Silicon +: Augmented Silicon Technology". These short courses are now available on videotape to purchase through IEEE Customer Service.

Interconnect Scaling: From Technology to System Design
Presented by: Karen Maex, IMEC and KULeuven, Leuven, Belgium; Chai-Hong Jan, Intel Corp., Hillsboro, OR; Jeff Gambino, IBM, Essex Junction, VT; Eric Beyne, IMEC, Leuven, Belgium; Davide Pandini, STMicroelectronics, Agrate Brianza, Italy; Krishna Saraswat, Stanford University, Stanford, CA

Order information:
Title: **Interconnect Scaling: From Technology to System Design**
NTSC Order No. **EV6991**
NTSC ISBN: 0-7803-8221-8
PAL Order No. **EV6992**
PAL ISBN: 0-7803-8222-6
IEEE Member Price: **$380.00**
List Price: **$450.00**

Silicon +: Augmented Silicon Technology
Presented by: Tsu-Jae King, University of California, Berkeley, CA; Jerry Fossum, University of Florida, Gainesville, FL; Jean-Pierre Colinge, University of California, Davis, CA; Digh Hisamoto, Hitachi, Ltd., Tokyo, Japan; Shinichi Takagi, Toshiba Corp., Tokyo, Japan; David Harame, IBM, Essex Junction, VT

Order information:
Title: **Silicon +: Augmented Silicon Technology**
NTSC Order No. **EV6993**
NTSC ISBN: 0-7803-8223-4
PAL Order No. **EV6994**
PAL ISBN: 0-7803-8224-2
IEEE Member Price: **$380.00**
List Price: **$450.00**

Here's how to place your order for the above videos:
Telephone: (800) 678-4333 (in the USA or Canada) or (732) 981-0060
Fax: (732) 981-9667
Online: http://shop.ieee.org/store/
Email: customer.service@ieee.org

Regional and Chapter News

USA, Canada and Latin America (Regions 1-6, 7 & 9)

ED Northern Virginia/Washington

- by Hrayr Sayadian

The Northern Virginia/Washington Chapter of the Electron Devices Society held four meetings between January and March 2004.

The January 22, 2004, meeting was titled NanoBio 101, and was moderated by Dr. Nathan Swami, Director, iNanoVa. This presentation featured Dr. Anantha Krishnan, a Program Manager at the Defense Advanced Research Project Agency and Harry Dorn of Virginia Tech. Dr. Krishnan described current bioengineering multi-disciplinary programs and Dr. Dorn discussed the current status and applications of the physics/chemistry interface of carbon-based nanostructures.

Dr. Richard Claus, President of NanoSonic, and Dr. Harris Goldberg, President of InMat, described current applications of nano-coated materials and products at the February 12, 2004, meeting. Murty Polavarapu, the past chair moderated the discussion.

The March 9, 2004, nanotechnology presentation was titled NanoElectronics 101 and was moderated by Dr. Nathan Swami, Director, iNanoVa. This presentation featured Dr. Stan Williams, a Senior Hewlett-Packard Fellow and the Director of Quantum Science Research at Hewlett Packard and Dr. Lloyd Harriett, Chair of the Electrical Engineering Department at the University of Virginia. The speakers described current research in microelectronics; electron, ion, and photon beam lithography; fabrication of nano-scale structures and devices; switching; and molecular electronics.

Also, on February 10, our Chapter co-sponsored with the MTT Washington/ Northern Virginia Chapter a presentation titled "Power Amplifiers: Technology and Design Techniques" by Dr. Dale Dowson of Northrop Grumman Corporation, who described device technology and circuit design techniques suitable for 1,000 Watt internally matched power transistors at L-Band and for 200 Watts at S-Band.

The meetings on nanotechnology are cosponsored with Atlantic Nano Forum. For more information, please see http://www.ewh.ieee.org/r2/no_virginia/eds/.

2003 International Semiconductor Device Research Symposium

- by Pankaj B. Shah and Ken A. Jones

The 2003 International Semiconductor Device Research Symposium (ISDRS) was held December 10 – 12, in Washington D.C. The Army Research Laboratory, National Institute of Science and Technology, Army Research Office, IEEE, EDS, National Science Foundation, Naval Research Laboratory, and the Electronics and Computer Engineering Department of the University of Maryland sponsored it.

This biannual symposium focuses on futuristic electronic and photonic devices and the materials technology necessary to make them. Areas such as novel device concepts, advanced processing technologies, nanotechnology, wide band-gap semiconductors, MEMS materials and devices, dielectrics, magnetic materials and devices, organic and polymer optoelectronic materials and devices, ultra high frequency devices & RF effects, and high power-high temperature devices, were included. These themes were highlighted by three plenary talks – "Photonic Band gap Based Designs for Nano-Photonic Integrated Circuits" by Prof. Eli Yablonovitch (UCSB); "A New Spin on Electronics – Spintronics" by Prof. Stu Wolf (UVa and DARPA); and "Enhanced Functionality in GaN and SiC Devices by Using Novel Processing" by Prof. Steve Pearton (UFI).

Three parallel sessions were held for the two and half days of the conference with more than 250 papers presented. Oral presentation awards were given in the area of devices to Anthony De Marco from the Universi-

Ken Jones, Conference Chair, presenting the Aldert van Ziel Award to Jim Plummer.

Prof. Arora and members of the EDS Student Chapter at UNICAMP.

ty of Maryland for "Maskless Fabrication of JFETs Via Focused Ion Beams", and in the area of materials to Shawn Bradley of Ohio State University for "Dependence of Schottky Barrier Height on Electronic and Chemical Properties of Ni/AlGaN Contacts". Poster presentation awards were given in the area of devices to Dae Hyun Kim from Seoul National University for "Asymmetrically Recessed 0.13 mm In.65Ga.35As HEMT's Using Double-Deck Shaped Gate Technology", and in the area of materials to Hasina Ali of the University of Maryland for "Study of ZnO Nanocluster Formation within Styrene-Acrylic Acid and Styrene-Methacrylic Acid Diblock Copolymers on Si and SiO2 Surfaces".

The conference banquet highlight was the Aldert van der Ziel award given in honor of Professor Aldert van der Ziel for his distinguished career as an educator and scientist. This year's recipient was Dr. James D. Plummer, Dean of Engineering, Frederick Emmons Terman Professor of Engineering, and the John M. Fluke Professor of Electrical Engineering at Stanford University. Dr. Plummer was chosen because, not only has he been a world renowned pioneer in the field of silicon based electronics, but also a superb educator evidenced by his many teaching awards and his mentoring of close to 100 Ph.D. students.

Dr. Ken Jones (ARL) chaired this year's organizing committee. Other organizing committee members included Dr. Jerry Woodall (Yale University) - symposium co-Chair, Dr. Al Hefner (NIST) - Program Chair, Dr. Gerry Borsuk (NRL) - Program co-Chair, and Dr. Agis Iliadis (University of Maryland) - Publications Chair. Both Dr. Hideki Hasegawa, (Hokkaido University) - Asian Continent based Chair and Dr. Mikael Ostling (KTH Royal Institute of Technology) - European Continent based Chair, were very active in recruiting participants from overseas. Dr. Pankaj Shah (ARL) served as Local Arrangements Chair, and Dr. Tom Murphy (University of Maryland) as Student Awards and Publicity Chair.

For more details, see the conference website at http://www.ece.umd.edu/isdrs2003/.

~ Murty S. Polavarapu, Editor

Professor Hiroshi Iwai attends the ED/MTT Orange County Seminar and gives a Distinguished Lecture on "The Future of CMOS Downscaling"

ED/MTT Orange County

- by Yuhua Cheng

The ED/MTT Orange County Chapter held a seminar on February 6, 2004 at the campus of Skyworks Solutions. Prof. Hiroshi Iwai of the Tokyo Institute of Technology was invited to deliver a distinguished lecture on "the future of CMOS downscaling". Dr. Yuhua Cheng of Skyworks Solutions hosted the seminar. In his talk, Prof. Iwai reviewed the recent trend of CMOS downsizing and commented the limit of scaling while discussing the process and device design and optimization. According to Prof. Iwai, with the consideration of the requirement of the investment for the development and production of the chip increasing for every new generation, aggressive global alliance strategies between companies, including universities and government labs, will become the most important issue for the next 10 years in order to survive the downsizing race.

Prof. Iwai's talk was well received by the audience and there were around 40 attendees from universities and companies. There was a one-hour question and answer session. After the seminar, a group of people continued another half hour discussion with Prof. Iwai on both the technical contents in the presentation and the development of the Electron Devices Society.

~ Sunit Tyagi, Editor

ED South Brazil

- by Jacobus W. Swart

On March 11-12, 2004, the EDS South-Brazil Chapter and EDS Student Chapter at UNICAMP (petition submitted to IEEE for approval) organized a series of short courses at the State University of Campinas, UNICAMP, in Campinas, SP. Prof. Vijay K. Arora, from the Wilkes University (PA/EUA), gave two courses as an EDS Distinguished Lecturer. The courses were entitled: "The Role of Physical and Behavioral Sciences in Developing Strategic Technologies in Micro/Nano-Systems" and "Quantum Nanoengineering". The first course was two parts on the afternoon of March 11th and the second course lasted all day on March 12th and was divided into 4 sessions. Discussions with the participants were performed after each presentation. Prof. Arora's courses attracted 30 attendees, most of them, staff and students from the Faculty of Electrical and Computer Engineering of UNICAMP. At the beginning of the first short course, on March 11th, the new EDS Student Chapter at UNICAMP, was introduced to the participants. The group of students involved in the organization of this new chapter were very helpful in giving support to make the two short courses a success. Prof. Arora also visited the Center for Semiconductor Components, where on going research projects were presented. After his stay at UNICAMP, Prof. Arora went to the World Congress on Engineering and Technological Education (WCETE-2004) in Guarujá / Santos, Brazil, from March 14 to March 17, to present his work entitled "Engineering a Quality Global Organization: Integration of Business and Engineering Paradigms".

On March 26, 2004, the EDS South-Brazil Chapter and EDS Student Chap-

ter at UNICAMP organized a meeting to present a one-day short course. The course was held by means of the videotapes obtained from EDS Videotape Lending Library Program, entitled "Circuit Designs and Technology for RF-CMOS", presented by Dr. Asad Abidi, from the University of California, Los Angeles, USA. A total of 16 people participated in the course, most of them from the State University of Campinas and some from nearby institutes. Dr. Everson Martins, from the Paulista State University, at Guaratinguetá, Brazil, was invited to hold discussions with the participants after the presentation of each of the four videotapes. Dr. Martins has experience in MMIC design and did his PhD on design of mixers on GaAs pHEMT technology. These discussions with the participants helped to answer some of the doubts of the participants and to give some complementary explanation to some of the topics presented on the tapes.

For additional information, contact Professor Jacobus W. Swart at jacobus@led.unicamp.br.

~ Adelmo Ortiz-Conde, Editor

EUROPE, MIDDLE EAST & AFRICA (REGION 8)

MTT/ED/AP/CPMT Nizhny Novgorod

- by Yuri I. Belov

The main activities of the ED/MTT/AP/CPMT/SSCS Nizhny Novgorod Chapter during last year are indicated here:

1) The XIII Industrial branch coordinating seminar 'The SHF–EHF engineering' (Aug. 27 – 29, 2003). Sixty-five contributions were presented at the seminar, 98 participants attended the event and the seminar topics were:
   - Powerful tubes and systems of use it
   - Solid State devices and assembles
   - Semiconductors and super pure materials for SHF-EHF engineering
   - Radio systems
2) The interregional seminar 'A precise processing of dielectric materials' (Sept. 16-17, 2003).
3) Nizhny Novgorod Chapter technical meeting (Nov. 14, 2003) with topics:
   - Probe microscopy at Nizhny Novgorod
   - Nanostructured semiconductors and dielectric materials
   - Ion beam modifications of Solids
   - Bulk nanostructure metal materials
   - Er-doped optical active phosphate films

MTT/ED/AP/CPMT Saratov-Penza

- by Nikita M. Ryskin

The School "Nonlinear Days in Saratov" was held in the "Volzhskie Dali" Hotel, in a picturesque place on the bank of the Volga River near Saratov, Russia October 8-13, 2003. The Saratov State University (SSU), Saratov Branch of the Institute of Radio Engineering and Electronics of Russian Academy of Sciences (SBIRE) have organized such schools each year since 1998, and the AP/EDS/MTT/CPMT Saratov-Penza Joint Chapter members play an active role in the organizing of the Schools. Namely, Prof. Dmitry I. Trubetskov who was the Conference Chair and Prof. Yurij I. Levin, Prof. Yurij P. Sharaevsky and Dr. Nikita M. Ryskin were the Organizing committee members.

The main goal of the Schools is twofold. First, it is intended to attract talented pre-college students to continue education in the field of physics and electronic engineering. Second, the Schools provide a good chance for undergraduate and postgraduate students to present results of their own research.

This year 54 oral and 26 poster papers were presented. More than 50 postgraduate, undergraduate and pre-college students from Saratov, Moscow, Nizhny Novgorod and Petropavlovsk–Kamchatsky, a city on the Far East, and more than 7000 km far from Saratov, participated in the School and presented the results of their own research. Sixteen lectures were devoted to different aspects of nonlinear science and its application in engineering have been presented by such known scientists as Prof. D.I. Trubetskov (SSU), Prof. V.S. Anischenko (SSU), Prof. S.P. Kuznetsov (SBIRE), Prof. Yu.A. Danilov (Moscow), Prof. A.P. Sergeev (Nizhny Novgorod), Prof. W. Ebeling (Berlin). The topics of the lectures were: 'Generation of femtosecond and attosecond pulses', 'Communications using chaos', 'Waves in anisotropic media', etc. The volume of the Proceedings was published shortly after the School. A competition in physics for pre-college students was held as well.

Prof. Werner Ebeling (Humboldt University, Berlin) is delivering a lecture "Self-Organization in Open Systems"

The 8th Chapter Workshop "CAD and Numerical Methods in Applied Electrodynamics and Electronics" was held in SSU on Nov. 25, 2003. The Chairman was Prof. Michael V. Davidovich. There were 11 presentations and more then 20 attendees, including 7 IEEE Members.

AP/ED/MTT/COM/EMC Tomsk

- by Eugeny D. Golovin

The Tomsk joint Chapter has expanded cooperation with foreign organizations. Two years ago EDS proposed the Regional Chapter Coordination Program. Professor Kwyro Lee, Director of KAIST in Daejeon, South Korea, has become our partner. Now our cooperation is not limited only in Tomsk and Novosibirsk Chapters, but has the framework of the Siberia Section.

In November, we had the opportunity to visit our partner, when we attended the 2003 Asia-Pacific Microwave Conference. The past Chapter Chair, Oleg Stoukatch, was a participant at the conference. APMC is the premier conference on microwave and electron devices in Region 10.

The Chapter Chairs Meeting of Region 10 was traditionally held in conjunction with APMC. It was very

Prof. Kwyro Lee, Past Chapter Chair Assoc. Prof. Oleg Stoukatch, and Kyu-done Choi

interesting to participate at the meeting and to compare it with a Region 8 Chapters Meeting. The Region 10 meeting was very short, unlike the chapter meetings held in Region 8 in conjunction with the European Microwave Week. Nevertheless, we were happy we had the opportunity of meeting our friendly colleagues from other chapters. Many thanks to professor S. -W. Yun for the invitation and professionalism in the organization of the event.

The meeting with professor K. Lee in KAIST was very productive and useful. Many questions, concerning not only IEEE, but also technical cooperation between laboratories of our universities were discussed. We thank Prof. Lee for his hospitality and assistance in travel. No doubt that EDS partnership is a useful program and will be useful in the future.

~ Alexander V. Gridchin, Editor

ED Israel

- Prof. Gady Golan, Chapter Chair

On Wednesday, January 28, 2004, at the Holon Inst. of Technology (HAIT) - Holon. Subject of meeting: "Mirror Alignment in Space Telescopes", By Dr. Rami Finkler,

Abstract: Telescopes with refractive elements were introduced by Newton in the middle of the 17th century. The first Cassegrain telescope consisting of two aspherical reflectors was introduced in 1672. This classical design has been used with some minor modifications, such as the Ritchey-Chretien Cassegrain, where the primary parabola is substituted by a hyperbola. It is the basic design of the Hubble Space Telescope. The basics of this telescope will be reviewed, and the principles used in polishing and testing the mirrors will be described. The alignment of the secondary mirror relative to the primary mirror is carried out under classical and lengthy procedures. An innovative method, which increased drastically the efficiency of the telescope alignment, was suggested. This method is based on an interferometric mapping of each reflector, and on a novel ptimization algorithm. This method was added as the "Alignment Tool" to the leading lens design package, Code V(r), by Optical Research Associates (ORA(r)) from California in 1990, and was successfully practiced at El-Op Ltd. in Israel.

About the author: Rami Finkler (Ph.D.) Rami Finkler has an extensive industrial track record in optical R&D, in the fields of: lens and optical system design, CAD tools for optics and opto-mechanics, testing and alignment methods and multidisciplinary systems. He holds B.Sc degrees from Tel Aviv University (Applied Math & Physics) and the Polytechnic of Central London (Photographic Science and Technology), M.Sc. and Ph.D. in Physics from Imperial College, University of London (Applied Optics Group). Dr. Finkler is active in societies of Optical Engineering and plays an active role in enhancing the dialog between academia and industry.

Chairmen of the meeting: Prof. Gady Golan - 50 people, students and academic staff, attended the meeting at HAIT.

On Wednesday, March 3, 2004, at the Holon Inst. of Technology (HAIT) - Holon.

Subject of meeting: "New methods for assessing arterial stenosis and arterial elasticity based on high frequency components of pressure and flow waves", By Dr. Zehava Blechman,

Abstract: Arterial stenosis, particularly coronary stenosis, is one of the main causes of morbidity and mortality in the western world. Aim: Qualitative and quantitative characterization of arterial stenosis using physical hemodynamic variables, by analysis of pressure and flow waves.

Methods: In-vitro and in-vivo pressure measurements were performed in different tubes and in femoral arteries of anesthetized dogs. The pressure waves were recorded at several degrees of stenosis and at different distances proximal to the stenosis, and were analyzed by Power Spectral analysis of incident and reflected pressure waves. Polynomials of pressure components were fitted for the different stages. The compliance was calculated based on elasticity measurements. Results: Similar phenomena, in both in-vitro and in-vivo models, were observed: 1) Gradual changes in low frequency energy of the pressure waves reflecting increasing degrees of arterial stenosis; 2) Pressure wave components at the acoustic frequency (400-2500 Hz), change gradually and are dependent on the distance from the stenosis and its severity. 3) Novel indices, based on the pressure-flow loop, were developed to detect arterial/graft stenosis. In contrast to available methods, they are independent of probe position and do not require drug administration. 4) Polynomials, based on the new indices, can quantify the changes in the stenoses severity ($R2>0.94$, $R2>0.82$ for in-vitro and in-vivo experiments, respectively). 5) In addition, the indices can be used to estimate radial compliance ($|R|>0.9$) and quantitatively characterize the elasticity of the artery. Conclusion: This multi-disciplinary study allows for better understanding of arterial function under normal and pathological conditions. Novel indices were developed enabling transcatheter quantitative evaluation of arterial stenoses and elasticity.

Chairmen of the meeting: Prof. Gady Golan - 70 people, students and academic staff, attended the meeting at HAIT.

MTT/ED/AP/LEO UK&RI

-by Terry Oxley

The Chapter would like to remind readers of two key events planned for 2004:

The IEEE High Frequency Postgraduate Student Colloquium (HFPSC). The 9th IEEE HFPSC will be held at UMIST in Manchester on Monday

and Tuesday 6-7, September 2004. Contributions are sought from post-graduate students who are working in fields relating to electromagnetism, RF, microwave, mm-wave and optical technologies. For further details, please contact the 9th HFPSC Chairman Dr Rob Sloan, E-Mail: sloan@umist.ac.uk, or visit: www.ee.umist.ac.uk/mw/.

IEEE International Symposium on Electron Devices for Microwave & Optoelectronic Applications (EDMO). The next EDMO, EDMO-2004, will take place at Gruger National Park, South Africa November 8-9, 2004. This is the 12th consecutive year EDMO has been held. For further particulars, please contact the EDMO 2004 Chairman Professor Lukas W Snyman, E-Mail: isnyman@techpta.ac.za, or visit: www.edmo-symposium.org.

CHAPTER CHAIRMAN: For further information on Chapter news, please contact the Chapter Chairman: Ali A Rezazadeh, Professor of Microwave Engineering, Dept. of Electrical Engineering and Electronics, University of Manchester Institute of Science and Technology (UMIST), P.O. Box 88, Manchester M60 1QD, UK. Tel: +44 (0)161 200 4708 (Sec.4801). E-Mail: a.rezazadeh@umist.ac.uk.

~ Gady Golan, Editor

ED Benelux

- by Hans Wallinga

The Benelux chapter organized a seminar at the University of Twente by Dr. L.K.J. Vandamme (Eindhoven University of Technology) on 16 January 2004, entitled: "1/f Noise in MOSTs: Faster is Noisier". In this seminar, Dr. Vandamme presented a historical overview of 1/f noise observed in different materials and devices. The two main models to explain 1/f-noise (mobility fluctuations and number fluctuations) were presented. Also, a new method to separate the RTS-noise observed in small MOSFETS from an underlying 1/f-noise was discussed. Twenty-five guests, mostly IEEE student members, attended the seminar.

2004 ESSDERC

- by Cor Claeys

The 34th European Solid-State Device Research Conference (ESSDERC 2004) will be held in Leuven, Belgium, September 21-23, 2004. The aim of the ESSDERC Conference is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and technologies. ESSDERC and its sister Conference ESSCIRC, which deals with solid-state circuits, are governed by a single Steering Committee. The increasing levels of integration for system-on-chip design made available by advances in silicon technology is stimulating more than ever before the need for deeper interaction amongst technologists, device experts, and circuit and system designers. Following the successful joint organization in 2002 and 2003, ESSDERC and ESSCIRC will again be jointly organized in 2004. While keeping separate Technical Program Committees, ESSDERC and ESSCIRC will share Plenary Keynote Presentations bridging both communities. Delegates registered for either Conference, are encouraged to attend any of the scheduled parallel sessions. The ESSDERC/ESSCIRC 2004 Conference Chair is Prof. Gilbert Declerck, IMEC, Belgium. This meeting is technically co-sponsored by the IEEE Electron Devices Society.

ESSDERC 2004 will continue the program trends by providing more emphasis on advanced device concepts, nanotechnologies, quantum and molecular devices, ITRS roadblocks and new process steps, (bio) sensors and displays. The main themes for ESSDERC 2004 include, but are not limited to the following:

* ITRS AVANCED DEVICES
Deep submicron scaling, device physics and performance, low-voltage CMOS devices, SOI devices, SiGe devices, low- and high-temperature operation, hot-carriers effects, gate-dielectric reliability, noise, process-induced damage, ESD, EMI, high-voltage devices, MOS controlled power devices, e.g. DMOS, IGBT, smart power devices and ICs, high-temperature operation, SiC devices, novel device concepts, low-inductance interconnects, reliability of contacts and bonds, cooling.

* ITRS ROADBLOCKS, MODULES AND PROCESS STEPS, PROCESS INTEGRATION
Advances in integration for ULSI, SOI, memories (dynamic, static, NV, novel types), bipolars, ASICs, MPU, multifunction, ICs patterning techniques, micromachining, shallow junctions, RTP, isolation and interconnects, optical interconnects, silicidation, thin dielectrics, high-k gate dielectrics, low-k interlevel dielectrics, cleaning issues, physical and structural characterization, surface preparation, module optimization, defect control, equipment issues, monitoring, metrology.

* MODELING, CHARACTERIZATION AND SIMULATION
Two- and three-dimensional modeling of processes, devices, equipment, isolations and interconnects, quantum devices, physical-device and yield models, electrical characterization techniques and parameter extraction, mixed electrical-thermal modeling and simulation.

* PHOTONICS, NANOTECHNOLOGIES, QUANTUM DEVICES AND SPIN ELECTRONICS
Single-electron devices, molecular devices, quantum dots, quantum wires, quantum gates, self-assembling structures, novel devices and principles of operation.

* SENSORS, BIOSENSORS AND DISPLAYS
CCD and CMOS imagers, radiation sensors, infrared sensors, physical sensors and actuators, micro fluidics, mTAS, biochemical sensors and actuators, array technology, active displays, display-device technologies, polycrystalline TFTs, field-emission devices, sensors and micro system packaging issues.

* POLYMER ELECTRONICS
Conducting polymers, semi-conducting polymers, flat-panel displays, polymer transistors, polymer light-emitting diodes and optoelectronic devices, giant flexible displays, polymer detectors

The ESSDERC/ESSCIRC 2004 meeting will have the following Keynote speakers
* Technology Considerations for Automotives (H. Casier, AMIS, Belgium)

Venue of the 2004 ESSDERC: Leuven, Belgium

* Organic Electronics for LED Applications (R. Friends, Cambridge University, United Kingdom)
* Low Voltage, Low Power Aspects of Data Converter Design (Q. Huang, ETH, Switzerland)
* Low Power Digital Circuit Design (T. Sakurai, University of Tokyo, Japan)
* Integrated Circuits for the Biology to Silicon Interface (R. Thewes, Infineon, Germany)
* On Ambient Intelligence, Needful Things and Process Technology (C. van de Poel, Philips Research Leuven, Belgium)

The ESSDERC 2004 Invited Speakers are:
* Optoelectronics and Photonics Integration (R. Baets, University of Ghent, Belgium)
* Novel Gate Concepts (J.P. Colinge, University of California at Davis, USA)
* Low Power Digital Circuit Design (S. Halama, Intel, USA)

In addition to the conference on Monday, September 20, there will be a tutorial on "Nanoelectronics and Emerging Devices', and on Friday, September 24 a Workshop on "System level Integration".

The Technical Program Chair is Prof. Robert Mertens, IMEC, Belgium. The Local Organizing Committee Chair is Prof. Cor Claeys, IMEC (c.claeys@ieee.org). More detailed information related to the technical program and the registration can be found at www.essderc.org.

~ Cora Salm, Editor

ASIA & PACIFIC (REGION 10)

ED/SSC Bangalore

- by Dr. Navakanta Bhat

The first event for the year 2004 was an IEEE DL by Prof. Cor Claeys, KU Leuven, Belgium. It was held on Jan. 8 and the topic of his talk was entitled "Technological Challenges of Advanced CMOS Processing and their Impact on Design Aspects". He stressed the importance of a strong connection between process technologists and designers in the deep sub-micron era.

Prof. Paul G. Jespers, KU Leuven, Belgium presented a two-day extended short course on Data Converters on Jan. 14 and 16. On the 14th, he explained the design issues in "Integrated D to A converters" while, on the 16th, he discussed "Integrated A to D converters" and "Sigma-Delta Converters". There were about 80 attendees from academia and industry. He spent time talking with the students at the Indian Institute of Science. He also visited the Texas Instruments India office and talked with the designers at TI.

The chapter received the Outstanding Chapter of the Year award (2003) from the Solid State Circuits Society, which was presented during the ISSCC 2004 in San Francisco, CA, USA on Feb. 16.

AP/ED Bombay

-by Dr. Mahesh Patil

During January-March 2004, the AP/ED Bombay Chapter organized the following activities.

The 17th International Conference on VLSI Design and the Third International Conference on Embedded Systems was jointly held in Mumbai January 7-9, 2004. The AP/ED Bombay Chapter provided local support for this event. The conference had a strong technical program, with five plenary talks, 35 invited talks, and 130 contributory talks, with a significant representation in the Electron Devices area. In addition, eight tutorials on a wide range of topics from device technology to system design were organized.

On January 12, two IEEE Distinguished Lectures were organized at IIT Bombay:

(1) "Sigma-Delta Converters" by Prof. Paul Jesspers, Catholic University, Belgium.
(2) "Techniques for very low-voltage operation of continuous-time analog CMOS circuits" by Prof. J. Ramirez-Angelo, New Mexico State University, USA. The talks were attended by graduate students and researchers and were followed by technical discussions with the speakers.

ED Calcutta

- by Banani Sen

The Chapter started its journey this year with Distinguished Lecturer (DL) talks in collaboration with CODIS 2004 organized by the ETCE Dept. of Jadavpur University (JU), Calcutta, India.

The joint organizers on "MOSFET in nanoscale" at the ETCE Dept., JU arranged a tutorial on the 8th of Jan. Two EDS Distinguished Lecturers, Prof. H. Wong of City University, Hong Kong and Prof. C.K. Sarkar of JU, shared their worthy experience with the graduate students, research scholars and faculties of different universities. Personalities associated with R&D aspects of different industries also benefited from the tutorial.

On the 9th and 10th of Jan., two more DL talks were arranged at the Park Hotel, Calcutta: (I) Prof. Cor Claeys of IMEC, Leuven, Belgium, delivered the talk on "Silicon based cryogenic electronics: from physical curiosity to quantum computing". (II) Prof. H. Wong of the City University, Hong Kong, gave a talk entitled: "On the scaling issues of ultra thin MOS gate dielectrics". Research scholars, faculties of different universities and scientists from different parts of India and abroad benefited from the talks.

ED/MTT India

- by K.S. Chari

Prof Vijay K. Arora, an EDS Distinguished Lecturer visited the Chapter and delivered a talk entitled: Quantum Engineering of Nanoelectronic Devices at DIT Delhi on 2 January 2004. The talk covered the concepts of Quantum (digital-type) over and above classical (analog-type) ones in relation to miniaturized devices where nano size can be less than or equal to the De- Broglie wavelength of an elec-

Prof. H. Wong of City University, Hong Kong and Prof. Cor Claeys of IMEC, Leuven, Belgium with Prof. C.K. Sarkar, his students and family members.

tron in Cartesian directions. The electric field driving electrons in these devices, carrier motion, limiting velocity (thermal or Fermi), Ohm's law validity and role of high-field velocity saturation in performance evaluation and characterization of nanostructures were discussed. The Role of phonon or photon on saturation velocity and degradation of diffusion coefficient were also described. The influence of quantum-mechanical and high-field effect impact on the design of opto-electronic devices and other micro-circuits was briefly presented. Over 50 participants attended the talk.

At the invitation of the Chapter, Mr. Paresh Patel, Founder and CEO, System Level Solutions (India) Pvt. Ltd., Gujrat gave a talk on "Embedded Systems Design- Hardware and Software" at DIT Delhi on 22 January 2004. Trends in Embedded Systems, Design and Synthesis, Simulation, Testing and Validation and Design sign off etc were touched on. Issues in software design flow like problem definition and specs, partitioning, simulation and debug, emulation and realizing final hardware system were covered. A low cost Embedded System Development Kit (ESDK) containing standalone board with FPGA/ Microprocessor and microcontroller cores and all associated peripherals and on-board interfaces and clock utilities etc. were demonstrated for a few typical applications of hardware design using Verilog/ VHDL/ C. Over 45 participants attended the event.

The Chapter co-sponsored an International Conference on Opto-electronics Technology (ICOT-03) held at the North Maharashtra University (NMU), Jalagaon during 12 to 14 January 2004. The event brought together international researchers, local R&D groups and academia in the field. Many oral presentations in the areas of design and analysis of optoelectronic devices, optical material fabrication and characterization, sensors, instrument application and miscellaneous studies were featured. Prof. I. Suemune, of Japan delivered a keynote address. Other leading speakers included Prof. Y. Chung, Korea; Prof. T. Arakawa of Japan; Prof. Vassilios Sarafis, and Dr. S. Lee, of Korea, etc. A total of 75 oral presentations and 25 poster papers were presented at the event attended by over 250 participants. Dr. K.S. Chari, Chapter Chair, chaired a session on opto-electronic materials held on 14 January 2004 along with Dr. A.D. Shaligram. Prof. D.K. Gautam, Head of the Dept. of Electronics, NMU, Jalagaon, coordinated the event. The conference had attracted financial support and sponsorship from several leading Government and Engineering agencies. The Chapter had instituted 6 Best Paper Awards and 3 Cultural Fete Prizes. These were given to the following winners in the respective events:

Best Paper Awards: Mr. U.K. Tripathi etal, IIT, Madras; Mr. Naveen Kumar, etal, IIT, Delhi; Mr. S.A. Gaikwad, NMU, Jalagaon; Mr. D.J. Shirale, BAM University, Aurangabad, Mr. V. K. Tomar, NMU, Jalagaon; Mr. S.S. Chauhan, CVPUAT, Pant Nagar

Cultural Prizes: Mr. Rajdeep Gautam, Mr. Harshad Deshmukh and Ms. Pooja Bhaiya etc from Jalagaon.

Mr. R. Murlidharan, Chair of the IEEE India Council, hosted a meeting of EDS and SSC, on 9 January 2004 at the Conventional Centre, Renaissance Hotel, Powai, and Mumbai coinciding with the VLSI 2004 Conference. Prof. Hiroshi Iwai, EDS President, Prof. Paul Jespers, Past Region 8 Director, and Chapter Chairs of EDS and SSC attended the meeting. Several issues related to IEEE and Society activities, including the accelerating membership, enhancing chapter and regional activities, membership upgrades, student activities, inter-society linkages and other administrative issues of concern, were discussed. Chapter chairs participated in the meeting and gave several suggestions. Chapter Chairs also chaired an industry forum session at the VLSI 2004.

The Chapter co-sponsored National Science and Engineering Technology (NASET) 2004 met at Kurukshetra University during 19-20 March 2004.

CPMT/ED/R Singapore

- by Dr. Kin Leong Pey

The Chapter organized the following ED-related technical talks during Jan-March 2004:

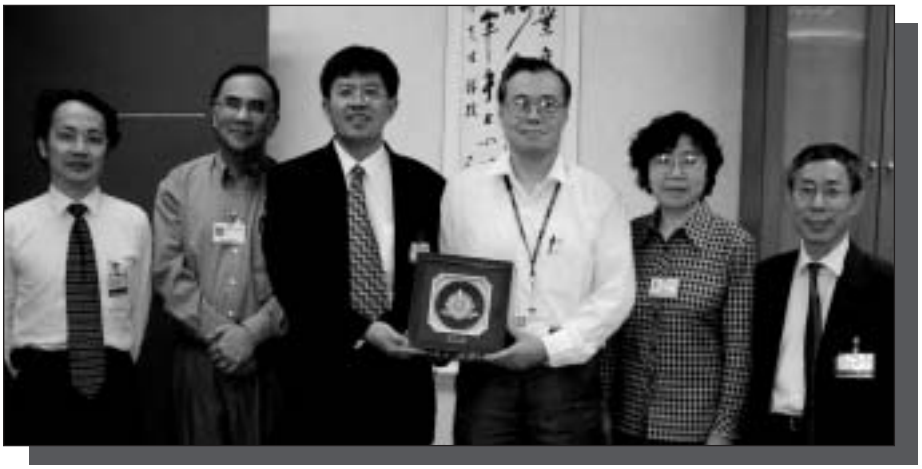
(1) On Jan. 7, Dr. Guoqiao Tao, Philips Semiconductors, The Netherlands, presented a talk on "Embedded Flash — the Philips/SSMC Approach with 2T-FN-NOR" at National University of Singapore.

(2) On Mar. 3, Professor Mark Lundstrom (IEEE Fellow and EDS AdCom member), Purdue University, gave a talk on "Transistor: from Lilienfeld to Landauer" at Nanyang Technological University (NTU), attended by more than 50 people from both university faculty/students and local industries as well as EDS members.

(3) On Mar. 17, Dr. Steven Voldman (IEEE Fellow), IBM, gave a talk on "ESD and Latchup in RF CMOS and RF BiCMOS Silicon Germanium Technology" at NTU, attended by more than 50 participants.

The Chapter already planned an EDS DL talk on April 15 by Professor C. K. Sarkar, Jadavpur University, on "Gate Oxide Degradation in MOS Devices Under High Field Stress-Breakdown Issues and the Model". An EDS DL mini-colloquium is also planned for the 3rd week of July 2004.

Prof. Lundstrom (right) received a plaque from Dr. Xing Zhou on behalf of the Chapter after delivering the technical talk to local members and participants.



IMETU delegate visit to Chartered on Feb 5, 2004. From left to right: X. Zhou (NTU), S. Chu (VP, CSM), Y. Li (Director, IMETU), S.C. Sun (Senior VP, CSM), L. Tian (IMETU), Z. Yu (Deputy Director, IMETU).

The 2004 International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA'04), jointly organized by the IEEE ED Taipei Chapter, IEEE Taipei Section, National Chiao Tung University (NCTU) and IEEE Rel/CPMT/ED Singapore Chapter, has received an overwhelming number of abstract submissions. Dr. Alastair Trigg of the Institute of Microelectronics, the General Chair of IPFA'05, is forming the Organizing Committee. It will be held in Singapore in July 2005. The Chapter has decided to hold IPFA outside Singapore in the Asia Pacific region on alternate years. IPFA was started in 1987 in Singapore, and is fully sponsored the IEEE CPMT/ED/R Singapore Chapter.

The Chapter committee member, Dr. Xing Zhou, has been elected an EDS AdCom member for a three-year term (2004-2006). He has also been appointed as an EDS Newsletter Editor for Region 10 (Australia, New Zealand & South Asia).

NTU-IMETU-Chartered Collaboration

- by X. Zhou & S.C. Sun

A delegate from the Institute of Microelectronics at Tsinghua University (IMETU) in China visited Nanyang Technological University (NTU) in Singapore February 4~6, 2004, and they signed an MOU on joint research & development in microelectronics and information engineering between the School of Electrical & Electronic Engineering at NTU and the School of Information Science & Technology at Tsinghua. The IMETU delegate visited Chartered Semiconductor Manufacturing (CSM) on February 5, and the three parties have discussed joint efforts in embarking on scalable RF device/component modeling for sub-100nm CMOS, which combines the respective expertise in active/passive compact-model development at NTU/IMETU as well as industry support in advanced mixed-signal RF CMOS technologies. Dr. Zhiping Yu gave a talk on "Quantum Mechanical Carrier Transport and Nano-scale MOS Modeling" at NTU, and another talk on "Broadband Modeling of Onchip Passive Components for RF CMOS" at Chartered. The NTU team has been funded by the Semiconductor Research Corporation on next generation compact-model development through Chartered support.

~ Xing Zhou, Editor

ED Japan

- by Hiroshi Ishiwara

The chair and secretary of the ED Japan Chapter, Dr. Naoki Yokoyama (Fujitsu Laboratories Ltd.), Chair, and Dr. Yuu Watanabe (Fujitsu Laboratories Ltd.), Secretary, retired at the termination of their 2-year term. For 2004-2005, the chapter has a new chair and its staffs: Prof. Hiroshi Ishiwara (Tokyo Institute of Technology); Chair, Dr, Yasuo Ikawa (Toshiba Corp.); Vice-Chair, Prof. Kazuo Tsutsui (Tokyo Institute of Technology); Secretary, and Dr. Shigeyoshi Watanabe (Toshiba Corp.); Treasurer. We would like to thank Drs. N. Yokoyama and Y. Watanabe for their great contribution to the ED Japan Chapter and welcome the new officers.

On January 19th, the second Japan Chapter Student Award was given to Takafumi Kamimura (Tsukuba Univ.), Hiroshi Irie (Univ. of Tokyo), Masumi Saito (Univ. of Tokyo) and Yasushi Ishikawa (Tohoku Univ.). This award was established in 2002 to encourage student members who actively contribute to the research of electron devices. The Japan Chapter selected these four students who have shown outstanding activities in the last year. They received metallic certificate plaques and a premium from the Chapter Chair at the Japan Chapter annual meeting held in Tokyo.

After the annual meeting, the briefing session for the 2003 IEDM was held to provide a summary discussion on the highlights of the 2003 IEDM. The five invited speakers delivered topics covering Integrated Circuits, CMOS Devices, CMOS Interconnects/Process, Modeling/Simulation, and Compound/Quantum Devices. This session has won popularity with a lot of the Japanese engineers who did not have a chance to attend the last IEDM to discuss the most advanced information of electron device technology. The session was very successful with 120 participants.

A Distinguished Lecturers Meeting was held on February 13th, 17th and 23rd by the Japan Chapter at the Tokyo Institute of Technology in Yokohama, Japan. Four prestigious speakers from EDS gave presentations on: "Advanced Low Leakage Interface and Reliability Measurement Techniques for Nano-CMOS Devices with Ultra-

Winners of Japan Chapter Student Award

Thin Gate Oxide Thickness Down to 1nm" by Prof. Steve S. Chung (National Chiao Tung University, IEEE ED Taipei Chapter Chair), "Electronic Nan devices research at LETI-France" by Dr. Simon Deleonibus (LETI), "New Horizon in SOI CMOS" by Prof. Sorin Cristloveanu (Institute National Polytechnique de Grenable), and "Reliability physics of ultra-thin gate oxides in MOS devices" by Prof. Enrique Miranda (Universidad de Buenos Aires, Argentina).

ED Kansai

- by Hiroyuki Sakai

The EDS Kansai Chapter held the 4th Kansai Colloquium Electron Devices Workshop at Campus Plaza Kyoto, Kyoto, Japan, on March 9, 2004. The Workshop is recognized as a traditional event of the Chapter, which offers a great opportunity for students and researchers in the Kansai area to access the up-to-date world-class researches and development. Twelve papers were accepted for presentation; seven of them concerning Si based technologies and the others covering compound semiconductor related issues. The Award Committee selected three papers for the 4th MFSK (Message From Spirited Kansai) Award. The winners of the Regular Award were Dr. Miyamoto for his paper entitled "RF Power Performance of Recessed-Gate AlGaN/GaN Heterojunction Field-Plate FETs" and Dr. Fujimori for "Design of Ferroelectric-Based Logic-in-Memory VLSI". Dr. Nakamura won the Student Award for his paper entitled "Fabrication of SiC Lateral Super Junction Diodes with Multiple Stacking p- and n-Layers". The winners will be honored with a memorial wall plaque engraving their names on it.

The 2004 general assembly meeting of the EDS Kansai Chapter followed the workshop. Dr. Daisuke Ueda, Chair of the Chapter, reported chapter activities in 2003 and presented activity plans for the year 2004. Prof. Nozawa, Chair of the International Meeting Committee, announced the coming international conference entitled "2004 International Meeting for Future Electron Devices, Kansai (2004IMFEDK)" and called for active paper submission.

The executive committee meeting was also held on the same day in the evening at the APA Hotel Kyoto. New committee members selected by officers and committee chairs were introduced. The Kansai Chapter now has 29 committee members. Next, an accounting report and activity plans were explained and a draft of the bylaws for the Chapter were discussed. The draft will be displayed on the Chapter website: http://www.edskansai.org.

Another key topic was the administration of the 2004 IMFEDK. The conference will be held at Katsura Hall of Kyoto University July 26-28. The latest progress of the keynote speakers' and tutorial instructors' selection were reported. Revision of the "Call for Paper" and rescheduling the timetable of the presentation were also discussed. The latest information will be updated on the conference website: http://www.imfedk.org.

~ Hisayo S. Momose, Editor

The Officers, Committee Chairs and Committee Members of the EDS Kansai Chapter

ED Taipei

- by Steve Chung

The ED Taipei Chapter organized two major events in this report period. On February 24, a one-day workshop called "2004 Advanced CMOS Device and Process Technology Workshop" was held at the National Chiao Tung University, Hsinchu. The purpose of this workshop was to give those industrial engineers, university faculties, and students who had not attended the last VLSI Technology Symposium and IEDM, the opportunity to learn the most recent advances in silicon-based VLSI devices and technologies. This workshop attracted more than 140 participants. The topics of the workshop included: (1) The Technology and Design for Advanced SOI-CMOS Devices (Dr. F.L. Yang); (2) High-K Gate Dielectric and Device Integration for Nanoscale CMOS Devices (Dr. H.C. Lin); (3) Reliability Issues for High-K Gate Dielectrics (Dr. Anthony Oates); and (4) SONOS Type Flash Memory

The invited speaker: Prof. T. P. Ma (left) and the Chair of ED Taipei: Prof. Steve Chung (right).

(Prof. T. Wang). These invited speakers presented the most up-to-date technologies and a review of the selected papers from the aforementioned two conferences. For each topic, tutorial materials were also included, so that the attendees may understand the fundamentals of these areas. In other words, the lectures given were similar to a short course with a recent update on the CMOS technology.

On March 15, an invited talk entitled "Pushing the Frontiers of MOS Gate Dielectrics" was given by our distinguished NAE (National Academy of Engineering) member, Prof. T.P. Ma at National Chiao Tung University, Hsinchu. Two hundred and ten participants, including engineers from Science Park and graduate students from universities, attended this talk.

Meanwhile, the Chapter is organizing the most important event in this year. The International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA) will be held, from July 5 to July 8, in a luxurious Lakeshore Hotel, close to the Science Based-Industrial Park, in Hsinchu, where the two world leading foundries TSMC and UMC, as well as many other highly developed semiconductor manufacturing and IC design companies are located. The format of the conference includes a one-day workshop, 3 days of technical paper presentation, and with concurrently held worldwide exhibitions. For more information, please visit the Conference website: http://www.ieee.org/ipfa or contact the Technical Program Chair: Prof. Steve S. Chung, National Chiao Tung University. Tel: +886-3-5731830, Fax: +886-3-5734608, Email: schung@cc.nctu.edu.tw

ED Beijing Chapter

- by Jinjun Feng

The ED Beijing Chapter has organized a number of activities since its last report. On September 9, 2003, Dr. Peter Pearce of CEDN, Geneva, Switzerland gave an invited talk on "Solid state pulse generators", which had 23 attendees. On August 6, 2003, Dr. Albert Wang of the Illinois Institute of Technology was invited to give a presentation on "IC circuit design methodology" in Tsinghua University. On September 25, 2003, Prof. N.C.Luhmann of the University of California at Davis presented a lecture on "New advance in microwave electronics" in the Beijing Vacuum Electronics Research Institute, which had 21 attendees. On November 4, 2003, Prof. Wang Yi Man of the Beijing Vacuum Electronics Research Institute was invited to deliver a lecture on "Introduction to IVESC2004. Its content and preparation" in the CIE/IEEE EDS joint meeting, which had 20 attendees. A workshop on "Trends in Microwave Tube Technology and Markets, Past and Future"was organized during December 11-13 in Beijing Vacuum Electronics Research Institute. Prof. N. C. Luhmann of University of California at Davis and Prof. George Caryotakis of Stanford University are the invited speakers.

On March 8, 2004, EDS President Prof. H. Iwai, and VP of Membership Prof. James Kuo visited the ED Beijing Chapter to discuss the establishment of two new sub-chapters (Nanjing Sub-chapter and Xi'an Subchapter) as well as the membership development in China. Prof. Fujiang Liao (Chapter Chair), Dr. Shanhong Xia (Vice Chair), Dr. Jinjun Feng (Treasure), Dr. Qiang'an Huang (Secretary), Prof. Yimen Zhang (Xiandian University, liaison representative of Northwest region of China), Dr. Baoqing Zeng (liaison representative of Southwest region) and Ms. Yang Kun (Officer of IEEE Beijing Section) attended the meeting.

The Chapter is now organizing the Fifth International Vacuum Electron Source Conference (IVESC2004) to be held in Beijing during September 6-10, 2004. The Conference Chair is Professor Fu Jiang Liao (Chapter Chair of ED Beijing). For more information please visit our Conference

Website: http://www.cie-china.org/ivesc2004, or contact Professor Fujiang Liao at bverizw@public3.bta.net.cn.

~ Hei Wong, Editor

EDS Meetings Calendar

(As of 27 April 2004)

The complete EDS Calendar can be found at our web site:
http://www.ieee.org/organizations/society/eds/meetings_calendar.xml Please visit!

July 1 - 5, 2004, T **Siberian Russian Workshop and Tutorial on Electron Devices and Materials**, Location: Novosibirsk State Technical University, Novosibirsk, Russia, Contact: Alexander Gridchin, Novosibirsk State Technical University, E-Mail: ieeensk@yandex.ru, Deadline: Not Available, www: http://www.ieee.nsk.su/edm/

July 5 - 8, 2004, T **IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits**, Location: Hsinchu, Taiwan, Contact: Jyuo- Min Shyu, Industrial Technology Research Institute, E-Mail: shyu@itri.org.tw, Deadline: 2/10/04, www: http://www.ieee.org/ipfa

July 11 - 16, 2004, @ **International Vacuum Nanoelectronics Conference**, Location: Massachusetts Institute of Technology, Cambridge, MA, USA, Contact: Tayo Akinwande, Massachusetts Institute of Technology, E-Mail: IVNC04chair@mtl.mit.edu, Deadline: 9/1/04, www: http://www-mtl.mit.edu/research/ivnc

July 12 - 16, 2004, T **European Electromagnetics Conference**, Location: University of Magdeburg, Magdeburg, Germany, Contact: Frank Gronwald, University of Magdeburg, E-Mail: magdeburg@euroem.org, Deadline: 2/29/04, www: http://www.euroem.org

July 26 - 30, 2004, T **International Conference on the Physics of Semiconductors**, Location: Northern Arizona University, Flagstaff, AZ, USA, Contact: David Seiler, National Institute of Standards & Technology, E-Mail: david.seiler@nist.gov, Deadline: 12/10/03, www: http://www.icps2004.org

July 26 - 28, 2004, T **IEEE International Meeting for Future of Electron Devices, Kansai**, Location: Katsura Hall, Kyoto, Japan, Contact: Hiroshi Nozawa, Kyoto University, E-Mail: nozawa@vega.energy.kyoto-u.ac.jp, Deadline: 4/30/04, www: http://www.imfedk.org

August 4 - 6, 2004, T **Lester Eastman Biennial Conference on High Performance Devices**, Location: Rensselaer Polytechnic Institute, Troy, NY, USA, Contact: Michael Shur, Rensselaer Polytechnic Institute, E-Mail: shurm@rpi.edu, Deadline: 5/15/04, www: http://nina.ecse.rpi.edu/shur/Eastman-Conference

August 9 - 11, 2004, T **International Symposium on Low-Power Electronics and Design**, Location: Newport Beach Marriott, Newport Beach, CA, USA, Contact: Kaushik Roy, Purdue University, E-Mail: kaushik@ecn.purdue.edu, Deadline: 2/5/04, www: http://www.islped.org

August 17 - 19, 2004, T **IEEE Conference on Nanotechnology**, Location: Audimax-TU München, Munich, Germany, Contact: Clifford Lau, Office of Naval Research, E-Mail: lauc@onr.navy.mil, Deadline: 3/5/04, www: http://www.nano.ei.tum.de/ieeenano2004/

August 18 - 21, 2004, T **International Conference on Microwave and Millimeter Wave Technology**, Location: Chinese Institute of Electronics, Beijing, China, Contact: Zheng-He Feng, Tsinghua University, E-Mail: fengzh@ee.tsinghua.edu.cn, Deadline: 4/30/04, www: http://www.cie-china.org/icmmt2004/index.htm

August 22 - 26, 2004, @ **IEEE Non-Volatile Semiconductor Memory Workshop**, Location: Hyatt Regency Monterey, Monterey, CA, USA, Contact: Kelly Baker, Motorola, Inc., E-Mail: rwvd10@email.sps.mot.com, Deadline: 4/26/04 www: http://ewh.ieee.org/soc/eds/nvsmw

August 22 - 27, 2004, T **IEEE International Conference on Molecular Beam Epitaxy**, Location: Edinburgh Conference Centre, Edinburgh, United Kingdom, Contact: Anna Low, Heriot Watt University, Riccarton Campus, E-Mail: a.e.low@hw.ac.uk, Deadline: Not Available, www: Not Available

August 23 - 27, 2004, T **International Conference on Hot-Wire (Cat-CVD) Process**, Location: Educatorium, University Center 'De Uithof', Utrecht, The Netherlands, Contact: Ruud Schropp, Utrecht University, E-Mail: schropp@phys.uu.nl, Deadline: 4/1/04, www: http://www.hwcvd.nl

September 2 - 4, 2004, @ **IEEE International Conference on Simulation of Semiconductor Processes and Devices**, Location: Forum Hotel, Munich, Germany, Contact: Gerhard Wachutka, Munich University of Technology, E-Mail: wachutka@tep.ei.tum.de, Deadline: 2/28/04, www: http://www.tep.ei.tum.de/sispad04

September 6 - 7, 2004, T **High Frequency Postgraduate Student Colloquium**, Location: Staff House, UMIST, Manchester, United Kingdom, Contact: Robin Sloan, UMIST, E-mail: sloan@umist.ac.uk, Deadline: Not Available, www: http://www.ce.umist.ac.uk/mw/news_&_events.htm

September 6 - 10, 2004, @ **International Vacuum Electron Sources Conference,** Location: Beijing International Convention Center, Beijing, China, Contact: FuJiang Liao, Beijing Vacuum Electronics Research Institute, E-Mail: bverizw@public3.bta.net.cn or liaofj@hotmail.com, Deadline: 4/15/04, www: http://www.cie-china.org/ivesc2004/index.htm

September 7 - 11, 2004, T **Symposium on Microelectronics Technology & Devices**, Location: Hotel Armacao do Porto, Porto de Galinhas, Brazil, Contact: Edval Santos, Caixa, E-Mail: edval@ee.ufpe.br, Deadline: 3/31/04, www: http://www.cin.ufpe.br/~chiponthereefs/

September 8 - 10, 2004, T **International Conference on Electrical and Electronics Engineering,** Location: Hyatt Regency, Acapulco, Mexico, Contact: Arturo Morales-Acevedo, E-Mail: amorales@gasparin.solar.cinvestav.mx, Deadline: Not Available, www: http://www.iceee.ie.cinvestav.mx

September 8 - 10, 2004, T **Conference on Electrical Engineering**, Location: Hyatt Regency, Acapulco, Mexico, Contact: Arturo Morales-Acevedo, E-Mail: amorales@gasparin.solar.cinvestav.mx, Deadline: Not Available, www: http://iceee.ie.cinvestav.mx

September 9 - 10, 2004, T **Semiconductor Manufacturing Technology Workshop**, Location: Ambassador Hotel, Hsinchu, Taiwan, Contact: Julie Wu, E-Mail: julie@tsia.org.tw, Deadline: 4/26/04, www: http://www.tsia.org.tw

September 12 - 16, 2004, T **International Symposium on Compound Semiconductors**, Location: Hoam Convention Center, Seoul National Univ, Seoul, Korea, Contact: Conf Mgt Group LEOS, IEEE, E-Mail: leosconferences@ieee.org, Deadline: Not Available, www: http://iscs-2004.snu.ac.kr

EDS Distinguished Lecturer/Chapter Partner Visits South Africa

Professor Marcel D. Profirescu visited South Africa as both the Partner of the ED/LEO South Africa Chapter and an EDS Distinguished Lecturer. He gave a presentation on Device Simulation on the Nanometer Scale at the University of Pretoria/CEFIM on 28 January where Dr. Christo Schutte of Detek/Kentron also gave a talk on Infrared Detector Technology in South Africa. There were 14 IEEE members and 23 guests in attendance. On 29 January, Professor M.D. Profirescu gave a presentation at Rand Afrikaans University/Department of Physics in Johannesburg. Professor V. Alberts of RAU also presented a talk entitled: Production of Commercially Viable Solar Modules Based on Cu (In, Ga)(Se, S) 2 Semiconductor Thin Films. 8 IEEE members and 24 guests attended the event. Both events were followed by social functions where the speakers and the attendees talked about IEEE activities and about the trends in Microelectronics in SA and worldwide. Professor M.D. Profirescu also gave talks in Cape Town on 26 January at Cape Technikon (event organized by Professor Nico Beute, IEEE SA Section) to 3 IEEE members and 22 guests, and on 27 January at Peninsula Technikon to 1 IEEE member and 14 guests. All four presentations were well received; there were questions and comments.

From left to right: Professor Monuko du Plessis, ED/LEO South Africa Chapter Chair, Professor Duncan Baker, University of Pretoria, former Region 8 News Editor, Dr. Christo Schutte, Manager Detek Pretoria, Professor Marcel D. Profirescu, EDS SRC EAM Vice Chair, ED/LEO South Africa Chapter Partner, Saurabh Sinha, University of Pretoria

Professor M.D. Profirescu also visited the University of Stellenbosch and the University of Cape Town. In these places and also in Cape Technikon and Peninsula Technikon he had talks with IEEE members and IEEE student members and initiated the formation of an EDS Student Branch Chapter in the southern part of South Africa. He has four contacts coordinated by Saurabh Sinha of the University of Pretoria and the goal is to open the EDS Student Branch Chapter with the occasion of Africon 2004 in September.

On 30 January, Professor M.D. Profirescu, together with Professor Monuko du Plessis, visited the Department of Science and Technology of South Africa and had talks to boost the bilateral S&T cooperation between South Africa and Romania. Also on 30 January, Professor M.D. Profirescu, together with Professor Duncan C. Baker of University of Pretoria, former Region 8 News Editor, visited EE Publishers (Pty) Ltd where Chris Yelland, Managing Editor presented the publishing flux for SAIEE Journals.

The visit in South Africa was successful and well organized by Professor Monuko du Plessis, ED/LEO South Africa Chapter Chair.

Marcel D. Profirescu
Technical University of Bucharest
Bucharest, Romania