IEEE
ELECTRON DEVICES SOCIETY
Newsletter

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TABLE OF CONTENTS

2006 IEEE INTERNATIONAL CONFERENCE ON THE SIMULATION OF SEMICONDUCTOR PROCESSES AND DEVICES (SISPAD)

The 11th IEEE International Conference on the Simulation of Semiconductor Processes and Devices (SISPAD 2006) will be held September 6-8, 2006, at the Monterey Plaza Hotel, Monterey, California. SISPAD is under sponsorship of the IEEE Electron Devices Society (EDS).

SISPAD provides an international forum for presenting leading edge research and development results in the area of process and device simulation. It is held annually, with the location of the conference circulating among Europe, Asia and the U.S. SISPAD is one of the longest running conferences devoted to semiconductor modeling. Prior to the 1st SISPAD in 1995, it was known as VPAD, SISDEP, and NUPAD, held in the same three regions as current day SISPAD. This year, we will have oral presentations and poster sessions on topics such as:

(continued on page 7)

IEEE

YOUR COMMENTS SOLICITED

Your comments are most welcome. Please write directly to the Editor-in-Chief of the Newsletter at nstojadinovic@elfak.ni.ac.yu

ELECTRON DEVICES SOCIETY

EDS AdCom
Elected Members-at-Large

Elected for a three-year term (maximum two terms) with 'full' voting privileges

2006	Term	2007	Term	2008	Term
S.S. Chung	(1)	J. N. Burghartz	(1)	G. Baccarani	(1)
T. Hiramoto	(2)	M. J. Chan	(1)	J. Deen	(1)
L. M. Lunardi	(2)	M. Estrada del Cueto	(2)	F. J. Garcia Sanchez	(2)
M. Lundstrom	(1)	S. Ikeda	(1)	J.B. Kuo	(1)
A. Wang	(1)	R. J. Nikolic	(1)	J.J. Liou	(2)
H.S.P. Wong	(2)	N. D. Stojadinovic	(2)	H. Shang	(1)
X. Zhou	(1)	J. J. Wesler	(1)	J. W. Swart	(1)
				S. Tyagi	(1)

NEWSLETTER EDITORIAL STAFF

CONTRIBUTIONS WELCOME

Readers are encouraged to submit news items concerning the Society and its members. Please send your ideas/articles directly to either the Editor-in-Chief or appropriate Editor. The e-mail addresses of these individuals are listed on this page. Whenever possible, e-mail is the preferred form of submission.

Newsletter Deadlines

Issue	Due Date
January	October 1st
April	January 1st
July	April 1st
October	July 1st

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EDS President's Message

Ilesanmi Adesida

It is indeed a special honor and privilege for me to serve as the President of the Electron Devices Society for the years 2006 and 2007. I take over a Society from my immediate predecessors, Hiroshi Iwai and Steven Hillenius, that is strong and ready to take on the prime challenge of delivering value to its members. I have been a volunteer in the Society for over a dozen years and have enjoyed serving in various positions. The joy emanates from being part of a community of engineers, technologists, and scientists whose daily endeavors have had tremendous impact in shaping the modern world!

Over the last year, the book "The World is Flat" by Thomas Friedman has been talked about ceaselessly; its theme is that technology has made possible access to information on a massive scale such that anybody anywhere now has the tool for competition. Of course, the computer is now regarded as the critical unit of this information technology revolution. However, we all know that the invention of the transistor is the fundamental element that has enabled the pervasiveness of technology that we encounter daily. The importance of electron devices in general continues to increase without boundary and all of its branches - microelectronics, photonics, MEMS, vacuum electronics, power electronics, and sensors have been transformed into major businesses that are critical to all spheres of human endeavors. Can we now imagine a world without internet, cellular phones, PDAs, video game systems, robots, and home entertainment systems? Of course not; and the trend is that transformation based on the contributions of electron devices will continue to bring about more intelligent systems for health, environmental, and other applications that will positively impact the daily life of almost everyone. The Electron Devices Society has existed for over 50 years, almost since the time of the invention of the transistor. We are proud that we have been part of these exciting developments and pledge to continue to fully participate in this tradition of innovation in the second half of our first century.

The information technology that we have all worked very hard to bring about also is the Achilles heel of many Societies in terms of maintaining and increasing the strength of membership. A critical question for all Societies is what is the value of membership when most of the information previously obtained by being a Society member can be obtained on-line? It is my opinion that the values derived from being a member of a Society include the interactions with colleagues in meetings to obtain knowledge first-hand, jointly promoting the intellectual activities of the field, networking among members, and mentoring future leaders of the Society, IEEE and the society at large. At several of our Executive and Administrative Committee meetings in the recent past, we have discussed strategic plans that will allow us to better serve our current members and attract new members. We will continue to work on our globalization efforts to increase EDS activities in Asia where the presence of the semiconductor industry is increasing. We have made significant efforts in establishing chapters in China, India, Korea and other countries. This will be further intensified. We will also build on the inroads that we have made in Latin America, Europe and the Middle East, with more chapters to be formed in Argentina, Brazil, Mexico, Peru, Turkey, Moldova, and elsewhere. The Regions/Chapters and Membership committees will work to promote membership in all regions. We will revitalize our Chapter Partners Program in order to assist in the formation of new chapters, rejuvenate moribund chapters, and assist existing chapters to be more effective in their activities. We will also promote affiliate membership. Special efforts are being developed to increase membership among workers in the semiconductor industry, especially in the US.

Education has always being a major activity of the Society with the Distinguished Lecturer (DL) Program being one critical element. The DL program will be streamlined and enhanced with a larger travel budget and a stronger collaboration will be promoted between the Educational Activities and the Regions/Chapters Committees. Educational workshops and mini-colloquia will be held in conjunction with chapter meetings with participation by EDS officers and DLs. We plan to develop a career guide book for students and advisors relating to EDS field of interest and associated curricula. We will participate in the IEEE Expert Now Program to offer web-based short courses. The Fellowship program will be strengthened by establishing a new Masters level Graduate Student for graduating College seniors to encourage them to go to graduate school and reward their undergraduate research. To continue to elevate education in the Society, a new EDS Award in Education will be instituted. Rapid advances in technology and how to respond to these advances and how they are communicated are subjects being considered by the Technical and Meetings Committees. They will collaborate to supervise and streamline EDS sponsored conferences.

The flagship publications, *IEEE Transactions on Electron Devices (TED) and IEEE Electron Device Letters* (EDL), of the Society have improved there turnaround time over the last five years due to the efforts of the Editors and the addition of publication personnel in the Executive Office. Coupled with electronic publishing innovations, we expect the publication cycle time for these journals to continue to be reduced notwithstanding the

(continued on page 7)

Upcoming Technical Meetings

2006 IEEE Compound Semiconductor IC Symposium (CSICS)

We cordially invite you to the 2006 IEEE Compound Semiconductor IC Symposium being held Nov. 12–15 in beautiful, historic San Antonio, Texas. The high-performance wireless and high-speed digital communications markets are thriving due to impressive strides in new materials and devices, greater integration levels, novel circuit implementations, and ever-changing systems partitions. Over the last 28 years the Compound Semiconductor IC Symposium (CSICS – formerly named the GaAs IC Symposium) has been and continues to be the preeminent international forum in which advances in semiconductor circuit and device technology are presented, debated, and discussed. The scope of the Symposium encompasses devices and circuits in GaAs, SiGe, InP, GaN, and InSb as well as sessions targeting the fields of RF CMOS and high-speed digital CMOS to provide a truly comprehensive conference. This is the ideal forum for presentation of the latest results in high-speed digital, analog, microwave/millimeter wave, mixed mode, and optoelectronic integrated circuits.

This year's 2006 CSIC symposium will be co-located with the Key Conference. The co-location is referred to as Compound Semiconductor Week and is comprised of 2 short courses and a primer course, a full 3-day technical program, and a joint technology exhibition.

The joint technology exhibition will be held on Monday and Tuesday. The technology exhibition will feature in excess of 80 companies showcasing a wide variety of products and services. The exhibition will feature informative and interesting displays with corporate representatives on hand. The list of exhibitors can be found in the CSICS advance program which will be published and distributed in late June.

The technical sessions will be held from Monday through Wednesday, Nov 12–15, 2006. The full 3-day technical session is comprised of several device technology, RF design, high-speed digital design, manufacturing and reliability, and executive management sessions.

River Walk – Paseo del Rio, San Antonio, Texas

The conference offers two short courses that will be held on Sunday, November 12, 2006. The courses are currently under development; tentatively there will be a course involving RF and high-speed CMOS and a course on GaN circuits and applications. The Symposium will also offer the popular primer course, "Basics of GaAs, InP and SiGe RFICs," which is an introductory-level class presenting a broad overview of RFIC technology. The Sunday evening course will cover materials and processes, device operation, and both analog/microwave and digital ICs.

To complement the Symposium, there are several social events. Events include the Sunday Evening CSICS Opening Reception, the Monday CS-Week Exhibition Opening Reception, the CS-Week Tuesday evening Theme Party to be held at the Rio Cibolo Ranch providing an authentic and memorable Texas experience, and the CS-Week Exhibition Luncheon on Tuesday. Additionally, a breakfast will be served on Monday, Tuesday and Wednesday.

The 2006 CSICS will be held in San Antonio, Texas, at the Marriott, Riverwalk Hotel located in downtown San Antonio. Now the eighth largest city in the United States, the city has retained its sense of history and tradition, while carefully blending in cosmopolitan progress. Close to twenty million visitors each year delight in the discovery of San Antonio's charms. Amidst the daily hubbub of the busy metropolitan downtown, sequestered 20 feet below street level, lies one of San Antonio's jewels - the Paseo del Rio. Better known as the "River Walk," these cobblestone and flagstone paths border both sides of the San Antonio River as it winds its way through the middle of the business district. The River Walk is quiet and park-like in some stretches, while other areas are full of activity with European-style sidewalk cafes and specialty shops. The River Walk stretches for approximately two-and-a-half miles from the Municipal Auditorium and Conference Center on the north end to the King William Historic District on the south. Rio San Antonio Cruises, the river's floating transportation system, provides a novel method of sightseeing and people-watching in downtown San Antonio. Groups can also dine aboard open-air cruisers as they wind their way along the scenic waterway.

High quality technical papers will be selected from worldwide submissions for oral presentation and publication in the symposium digest. The deadline for electronic receipt of abstracts was

May 15, 2006. Authors will be informed regarding the results of their submissions by June 24, 2006. For registration, paper submissions, call for papers, advance program, and further information, please visit the CSICS website at http://www.csics.org. Further questions on abstract submission may be addressed to the Symposium Technical Program Chair: Mohammad Madihian, Phone: +1 609 951 2916, Email: madihian@nec-labs.com

We hope you can attend.

Walter A. Wohlmuth
2006 CSICS Publicity Chair
RF MicroDevices
Greensboro, NC,
USA

2006 IEEE International SOI Conference (SOI)

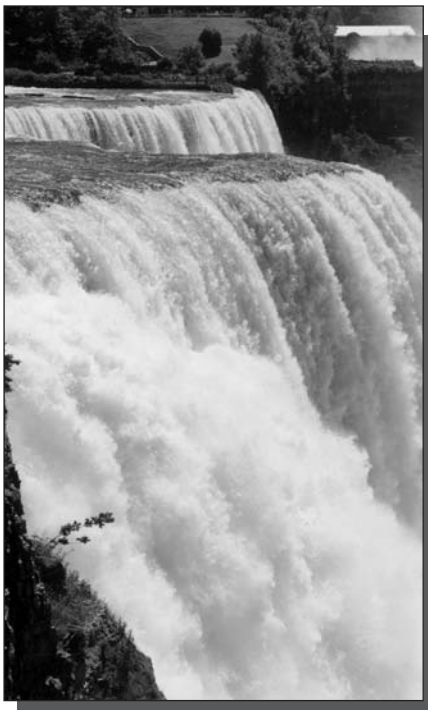
The premier conference dedicated to current trends in Silicon-on-Insulator technology, the annual IEEE International SOI Conference, will be held October 2–5, 2006, at the newly renovated Holiday Inn Select in Niagara Falls, New York. The conference will be preceded by a one-day tutorial Short Course on Monday, October 2nd.

The SOI conference was established with the support of IEEE to provide an international forum for open discussion in all areas of silicon-on-insulator technologies and their applications. Ever increasing demand and modifications in this technology bring the industry together to discuss new accomplishments and gains, plus consider new developments in the industry contained in original papers presented at the conference.

The 32nd annual IEEE International SOI Conference will begin with a half-day plenary session followed by two days of oral sessions, a poster session and a late news session. A Best Paper Award will be presented at the close of the conference on Thursday. Session topics will focus on basic materials research, device research, circuit development (special and improved) and applications and uses.

On Wednesday afternoon, participants will be free to enjoy the world's most famous waterfall – Niagara Falls, get a little work done, or just relax. An evening discussion panel session where attendees are encouraged to share their opinions and expertise on the chosen topics of discussion will round off Wednesday evening.

The 2006 SOI Conference seeks papers on a wide range of SOI technology including:



Niagara Falls. View from Goat Island, Niagara Falls State Park

- SOI material science/modification, material characterization, and manufacture
- SOI device Physics and modeling
- SOI circuit applications (high-performance microprocessors, srams, asic, low power, high-voltage, rf, analog, Mixed mode, etc.)
- Double Gate/Vertical Channel Structures; Other Novel Structures
- Strained Si-Ge structures
- New SOI structures, Circuits, and applications (optics, 3d integration, displays, microactuators - MEMS, microsensors, Drop-in RAMS, etc.)
- SOI reliability issues (hot-carrier effects, radiation effects, high-temperature effects, etc.)
- Manufacturability and process integration of SOI devices and circuits
- Alternate silicon-on-insulator material.

Abstracts for SOI 2006 Conference were due no later than May 5, 2006, to: BACM, by e-mail ONLY to SOIPaper@bacminc.com in PDF format. Late news papers with exceptional merit will be considered for the Late News session if submitted on or before August 13, 2006.

Once again, the popular One-Day Tutorial Short Course will be offered preceding the 2006 SOI International Conference. Tutorial Short Course instructors have many years of experience in the field of silicon-on-insulator technology. The course is intended to educate attendees in detail about current trends and issues in the SOI industry. The SOI 2006 Tutorial Short Course will focus on future trends in SOI technologies to enable low power electronics. Participants will receive copies of all visual presentations.

For registration forms and additional information please go to the conference web site www.soiconference.org, or contact the 2006 IEEE International SOI Conference at 520 Washington Blvd., #378, Marina del Rey, CA 90292, Tel: +1 310 305 7885; Fax: +1 310 305 1038; Email: bobbi@bacminc.com.

Christophe Tretz
2006 SOI Conference Chair
IBM
San Jose, CA, USA

2006 IEEE International Integrated Reliability Workshop (IIRW)

Stanford Sierra Camp on the shore of Fallen Leaf Lake near South Lake Tahoe, California.

The 2006 IEEE International Integrated Reliability Workshop (IIRW), sponsored by the IEEE Reliability Society and the IEEE Electron Devices Society, will be held at the Stanford Sierra Camp on the shore of Fallen Leaf Lake near South Lake Tahoe, CA, October 16-19, 2006. This workshop provides a unique forum for open and frank discussions of all areas of reliability research and technology for present and future semiconductor applications. Please visit www.iirw.org for the Call for Papers and to submit your abstract to the Technical Program Chair, Yuan Chen, JPL (yuan.chen@jpl.nasa.gov). The submission deadline is July 14, 2006. This year there will be an opportunity for expanded versions of selected manuscripts to be part of a special IIRW Proceedings Issue of *IEEE Transactions on Device and Materials Reliability* (T-DMR), scheduled for June 2007.

The IIRW is very different from a typical technical conference. From the moment you arrive, after winding slowly back to the south shore of Fallen Leaf Lake, you realize that you are taking part in something special. Attendees stay in cabins without TVs or phones, dress is casual to rustic, affiliations are downplayed, and meals are provided at the lodge dining room, family-style. Attendees of the workshop are expected to participate actively. You feel yourself drawn into technical discussions from the start. Every aspect of this conference, from the isolated location to the format of the technical program, is designed to encourage attendees to interact.

The peaceful setting, free from the distractions and annoyances of modern life, presents a terrific opportunity to get to know your colleagues, including internationally renowned experts. This is an opportunity not usually available at other conferences. Participants spend their evenings at discussion groups, poster sessions, and special interest groups (SIGs), all with refreshments provided to stimulate discussions.

This year's IIRW 2006 Keynote Topic is "Reliability Challenges: Preventing Them from Becoming Limiters to Technology Scaling" presented by Jose Antonio Maiz, Intel Fellow, Technology and Manufacturing Group Director, Logic Technology Quality & Reliability, Intel Corporation.

Another advantage of attending the IIRW are the extensive Tutorial Courses, presented by world-class experts and included at no additional cost. This year's tutorial courses cover Electromigration, Reliability in BEOL High-k, Gate Dielectrics, Negative Bias Temperature Instability (NBTI), Impact of Process Limitations on Reliability, Qualification Strategy, Sensors, and Phase Change Memory.

One unique aspect of this workshop is the opportunity for every attendee to present a poster of his or her own research. Either arrange for space when you register or bring last-minute results in your briefcase or backpack. This is a great way to share your latest results and to get world-class feedback. These poster presentations are even eligible for inclusion in the conference proceedings. The open poster sessions are but one example of the opportunities for the intense interaction that sets the IIRW apart from other conferences.

Another distinction of the IIRW is the moderated Discussion Groups that are held in the evenings. This year's Discussion Group Topics include: 1) High-k Gate Dielectrics, 2) NBTI, 3) Interconnects, and 4) Product Reliability. Lively conversation and debate among participants is promised and written summaries will be included in the workshop proceedings.

The Discussion Groups are followed by the Special Interest Group meetings (SIG). The SIGs are composed of small groups of researchers and engineers with a mutual interest who often continue their conversations and collaborations even after they leave the workshop. Every attendee has the opportunity to become part of an existing SIG or suggest a new topic and start one of their own.

Additional information about the workshop is available on the IIRW website at www.iirw.org, or by contacting John F. Conley, Jr., Sharp Laboratories of America, the 2006 IIRW General Chair (jconley@sharplabs.com). If you want to take part, please register early as space at the Stanford Sierra Camp is limited to roughly 120 attendees.

On behalf of the 2006 International Integrated Reliability Workshop Committee, I look forward to meeting you in Lake Tahoe!

George Goffman
2006 IIRW Communications Chair,
Philips
AE Nijmegen, The Netherlands

2006 IEEE International Conference on the Simulation of Semiconductor Processes and Devices (SISPAD)

(continued from page 1)

- Transport in nano-structures and structures using non-conventional materials, effects of strain on carrier transport, models of device scaling limits, quantum effects, reliability, fluctuations, and novel nano-scale devices such as QCA, SET, and molecular devices
- Continuum and atomistic approaches for process simulation, models for dopant activation and diffusion, oxidation, silicide growth, interface effects, and effects due to stress
- Equipment, topography, and lithography simulation
- Interconnect modeling and algorithms including noise and parasitic effects
- Compact device modeling for circuit simulation, including high frequency and noise modeling
- Integration of circuit, device, process simulation with applications to performance modeling of circuits
- User interfaces and visualization
- High performance computing, advanced numerical methods and algorithms, including gridding
- Simulations of new memory structures such as nanocrystal, phase change, MRAM, and devices such as microsensors, microactuators, optoelectronics devices, lasers, and flat panel displays
- Benchmarking, calibration, and verification of models and simulators

One of the unique strengths of SISPAD is its size. SISPAD attracts approximately 200 participants from around the world. The conference is the right size to allow for attendees to foster relationships and to relax among their peers. SISPAD will have invited speakers who will present new ideas about device and process physics, demonstrate applications to leading edge technologies, and show new models for compact devices.

Preceding the conference at the Monterey Plaza Hotel will be a companion workshop on Tuesday, Sept. 5, 2006, "Gate Stack and Contact Engineering for sub-30nm FETs", organized by R. Dutton, Y. Nishi, and K. Saraswat of Stanford University. This workshop is targeted at the discussion of critical issues facing scaled MOS technology with emphasis on the gate stack and contact technologies. There are many challenges both in terms of technology and device design that need to be considered. It is now generally accepted that alternative materials are needed to maintain good electrostatics and to reduce parasitic effects. This workshop will explore these issues based on experimental and modeling work of leading experts in the field.

Monterey is a picturesque slice of California culture. The Big Sur coastline, Carmel, and Pebble Beach are famous for their beauty. Any trip to Monterey should include taking in 17-mile drive, Cannery Row, and the Monterey Wine Country. Another famous site is the Monterey Bay Aquarium, where the SISPAD banquet will be held.

We cordially invite you to attend SISPAD 2006 to learn more about state-of-the-art simulation models and applications, and to bask in the culture of Monterey, California.

For further information, please visit our conference web site at http://www-tcad.stanford.edu/sispad06/, or send e-mail to sispad06@gloworm.stanford.edu or to the conference chairs.

Phil Oldiges
2006 SISPAD Conference Chair
IBM Corporation
East Fishkill, NY, USA

Kartikeya Mayaram
2006 SISPAD Technical Chair
Oregon State University
Corvallis, OR, USA

EDS President's Message

(continued from page 3)

significant increase in the number of manuscript submissions. New guidelines are being developed for editors to solicit best papers from conferences for possible publication in TED. The Publications and the Educational Activities Committees are working on the possibility of converting all International Electron Devices Meeting (IEDM) Short Courses videotapes to CD/DVD for sale to our members at reasonable price. The committees will also be working to see which other conference proceedings and short courses sponsored by EDS will be amenable to being converted to CD/DVD format for members.

The activities of the Society can only be carried out successfully through the efforts of dedicated cadre of volunteers and the staff members at the Executive Office. I implore all members to volunteer their time for the advancement of the Society. There are many benefits to be derived from volunteering both at the personal and professional levels which I will go into in the future, suffice it to say for now that your assistance is needed in making our Society all that it can be. Rapid changes are occurring around us, in our work places and homes, and we must devise ways to make them effective for our progress as a vibrant Society. I will report from time to time on the progress of our Society on these pages. I would like to encourage you all to think about ways and means to enhance our programs and our Society and let me know how the Society can better respond to your needs as individuals. Again, I emphasize that the world around us is changing; this is our chance to lead the change by serving our Society.

Society News

Congratulations to Ilesanmi Adesida, Elected to the National Academy of Engineering (NAE)

Ilesanmi Adesida

Ilesanmi Adesida, President of the Electron Devices Society and Dean of the College of Engineering, University of Illinois, Urbana-Champaign, was elected to the National Academy of Engineering for his contributions to the nanometer-scale processing of semiconductor structures and applications in high-performance electronic and optoelectronic devices. He will be inducted into this prestigious organization during its annual meeting on October 20th in Washington, DC.

Alfred U. Mac Rae
EDS Vice-President of Awards
Mac Rae Technologies
Berkeley Heights, NJ, USA

Report from the EDS Vice-President of Regions/Chapters

Cor L. Claeys

During the past year, the EDS Regions/Chapters Committee has been very active and successful in the formation of new chapters. At the end of 2005 there were in total 120 EDS chapters, which is an annual increase of 2%. Compared to December 2005, new chapters have been formed in Region 9 (Bahia Chapter in Recife, Brazil and student chapters at Universidad Cristobal Colona, Veracruz and Universidad del Sol, Cuernavaca, Mexico) and Region 10 (Chapter at Xian, China, and Chapter in Penang, Malaysia). Presently, the formation of another 20 new chapters is in progress or under discussion.

Regional Chapter meetings have been organized in Region 10 (Seoul, Korea, June 2005), Region 9 (Veracruz, Mexico, August 2005) and Regions 1-3, 7 (Washington DC, USA, December 2005). The Seoul meeting,

(continued on page 19)

EDS Electronic Materials Committee Report

Judy L. Hoyt

The Electronic Materials Committee, one of the Technical Committees of the IEEE EDS, has recently been reconstituted to reflect the growth in research and development of new materials for improving CMOS performance, and CMOS-related technologies.

The committee is chaired by Judy Hoyt (MIT), and other committee members include: Matty Caymax (IMEC), Simon Deleonibus (LETI), Eugene Fitzgerald (MIT), Tahir Ghani (Intel), Rajinder Khosla (NSF), Veena Misra (NC State), Ken Rim (IBM), Glenn Solomon (NIST), James Sturm (Princeton), Shinichi Takagi (Univ. Tokyo), Hitoshi Wakabayashi (Sony), Howard C.-H. Wang (TSMC), and Shaofeng (Scott) Yu (TI).

As is the case for most of the EDS Technical Committees, the main functions of this committee are to review requests from various conferences to receive EDS sponsorship, and to make recommendations for awards.

The members of the Electronic Materials Committee represent a range of expertise with emphasis on CMOS materials and processes, including research on global and process-induced strained Si, new channel materials for CMOS such as strained SiGe, Ge and III-V semiconductors on Si, high-K gate dielectrics and metal gates, silicides, III-V materials for FETs and CMOS device technology. There is a separate Optoelectronics Committee that is expected to cover optical applications of these materials.

The growth in volume of research in these areas has been accompanied by an increase in the number of conferences and workshops covering these topics, and part of the work of this committee is to ensure that the conferences of greatest interest to EDS members receive EDS support. The committee was chosen to have membership representation from North America, Europe and Asia.

Judy L. Hoyt
EDS Electronic Materials
Committee Chair
Massachusetts Institute of Technology
Cambridge, MA, USA

EDS VLSI Technology and Circuits Committee Report

Bin Zhao

The EDS VLSI Technology and Circuits Technical Committee now has twenty-one members with worldwide geographical representations and a very wide spectrum of technical expertise in VLSI technology, devices and circuits. The current committee members are: Ilesanmi Adesida (University of Illinois), Joe Brewer (University of Florida), Robert Chau (Intel), Steve Chung (National Chiao Tung University), Jamal Deen (McMaster University), James Hutchby (SRC), Shuji Ikeda (ATDF), Hiroshi Iwai (Tokyo Institute of Technology), Seiichiro Kawamura (AIST), Kinam Kim (Samsung), Yanhe Li (Tsinghua University), Akira Matsuzawa (Tokyo Institute of Technology), Huiling Shang (IBM), Roland Thewes (Infineon), Albert Wang (Illinois Institute of Technology), Jeffery Welser (IBM), Reinout Woltjer (Philips), Patrick Yue (Carnegie Mellon University), Peter Zeitzoff (SEMATECH), Xing Zhou (Nanyang Technological University), and Bin Zhao (Skyworks).

The committee has been focusing its activities to identifying new technical trends, fostering emerging technical concepts, and serving the needs of the Electron Devices and Solid-State Circuits communities in VLSI technology and circuits. Recent work accomplished by the committee and its members include:

- A special issue on "Integrated Circuit Technologies for RF Circuit Applications" of *IEEE Transactions on Electron Devices* published in July 2005.
- Organized a workshop "RF and Mixed-Signal SoC Design" at the 6th International Conference on ASIC, October 2005.
- Chaired the Technical Working Group of "Emerging Research Devices" for the International Technology Roadmap for Semiconductors (ITRS) – released in Dec. 2005.
- Co-Chaired the Technical Working Group of "RF and Analog/Mixed-Signal IC Technologies for Wireless Communications" for ITRS – released in Dec. 2005.
- Chaired the Technical Working Group of "Process Integration, Devices, and Structures" for ITRS – released in Dec. 2005.
- Workshop "Emerging Research Memory Devices" held at Maastricht, Netherlands in April 2006.
- A special issue on "Non-Classical Si CMOS Devices and Technologies: Extending the Roadmap" of *IEEE Transactions on Electron Devices* published in May 2006.

This year, the committee continues its tradition to help IEDM by providing suggestions and support for the Evening Panel Sessions and the Emerging Technologies Session. We continue to work with ITRS Technical Working Groups of "Emerging Research Devices," "RF and Analog/Mixed-Signal IC Technologies for Wireless Communications," and "Process Integration, Devices, and Structures" for the ITRS 2006 update. The committee has planned to organize workshops/panel sessions in several VLSI areas of growing importance and the topics include: "Emerging Technologies for RF IC Applications," "Technology Options for the 32nm Node," "Analog/RF Measurement and Characterization for Emerging Devices," and "Power Management in Devices and Circuits." The topics planned by the Committee for special journal issues include: "Advanced Non-Volatile Memory Technologies," "Heterogeneous Integration of Dissimilar Technologies," "Power Management in Devices and Circuits," and "Information Processing Technology and Circuit Architectures beyond CMOS."

The ability to implement highly complex, very-large-scale integrated circuits with the most advanced devices and process technologies is critical for modern electronic products. As such, VLSI has been and will continue to be a critical technical field for EDS. The VLSI Committee will continue to carry out its mission in serving EDS in the technical needs of VLSI and promoting VLSI technical activities globally.

Bin Zhao
EDS VLSI Technology
and Circuits Committee Chair
Skyworks Solutions
Irvine, CA, USA

Announcement of Newly Elected AdCom Members

On December 4, 2005, the EDS AdCom held its annual election of officers and members-at-large. The following are the results of the election and brief biographies of the individuals elected.

I. OFFICERS

The following individuals were elected as officers for a one-year term beginning January 1, 2006:

COR L. CLAEYS (President-Elect) received the Electrical-Mechanical Engineering and the Ph.D. degree from the KU Leuven, Belgium. In 1984 he joined IMEC as Head of Silicon Processing and is since 1990 responsible for Technology Business Development. He is also Professor at the KU Leuven. His main interests are in silicon technology, device physics, low frequency

noise, radiation effects, and defect engineering. He co-edited a book "Low Temperature Electronics" and wrote "Radiation Effects in Advanced Semiconductor Materials and Devices". He co-authored six book chapters and more than 600 technical papers. He is an Associate Editor for the Journal of the Electrochemical Society. Dr. Claeys is a Senior Member of IEEE and a Fellow of the Electrochemical Society. In 1999 he was elected as Academician and Professor of the International Information Academy. He also received the IEEE Third Millennium Medal and in 2004 the Electronics Division Award of the Electrochemical Society. He was the founder of the IEEE EDS Benelux Chapter, Chairman IEEE Benelux Section, and Vice-President EDS Regions/Chapters. Since 2001 he is an IEEE EDS Distinguished Lecturer.

JUIN J. LIOU (Treasurer) received the B.S. (honors), M.S., and Ph.D. degrees in electrical engineering from the University of Florida, Gainesville, in 1982, 1983, and 1987, respectively. He is now a Professor at the University of Central Florida, Orlando, Florida.

Dr. Liou has filed 3 patents, and has published 6 textbooks, 200 journal papers, and 150 papers (including 50 keynote/invited papers) at international conferences. He has been awarded more than $6.5 million of research contracts and grants.

Dr. Liou received UCF Distinguished Researcher Award three times (1992, 1998, 2002), UCF Research Incentive Award two times (2000, 2005), and IEEE Joseph M. Biedenbach Outstanding Engineering Educator Award in 2004 for his exemplary teaching, research, and international collaboration. His other honors include Fellow of the IEE, IEEE EDS Distinguished Lecturer, Cao Guang-Biao Endowed Professor of Zhejiang University, China, and Consultant Professor of Huazhong University of Science and Technology, China.

Dr. Liou is the IEEE EDS Treasurer, IEEE EDS Finance Committee Chair, and IEEE EDS Administrative Committee member.

JOHN K. LOWELL (Secretary) received the Ph.D. degree in Applied Physics from the University of London. He has held technical and managerial assignments for United Technologies, Northern Telecom, Mostek, Texas Instruments, British Telecom/Dupont, AMD, Applied Materials, Oracle and PDF Solutions. Presently, he is the President and Chief Consultant at Lowell Consulting in Dallas. He has also been a Professor at Texas Tech University and in the University of Texas system, and held Consulting Professorships at other universities in addition to being a Visiting Scholar at the NSF Center for the Synthesis, Growth and Characterization of Electronic Materials at the University of Texas at Austin.

Dr. Lowell is a Senior Member of the IEEE, a Distinguished Lecturer of the EDS and has held AdCom-level positions previously within the LEO and CAS societies. For fifteen years, he was also the Associate Editor-in-Chief of the IEEE Division I Circuits & Devices Magazine, and was its Guest Editor twice.

II. ADCOM MEMBERS-AT-LARGE

A total of eight persons were elected to three-year terms (2006-2008) as members-at-large of the EDS AdCom. Two of the eight individuals were re-elected for a second term, while the other six were first-time electees. The backgrounds of the electees span a wide range of professional and technical interests.

A. SECOND TERM ELECTEES:

FRANCISCO J. GARCIA SANCHEZ received his B.E.E., M.E.E. and Ph.D. degrees from the Catholic University of America, Washington, DC, in 1970, 1972, and 1976, respectively. He has been a faculty member at Simón Bolívar University, Caracas, Venezuela, where he has directed the Solid State Electronics Laboratory since 1978. He has received numerous awards for excellence in research. His research interests are in electron device modeling. He has published over 120 articles and is the co-author of a book on MOSFET modeling. He serves as reviewer for journals, has been active in editorial work, and in various international conference organization activities.

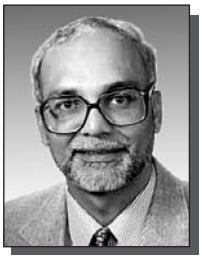
Prof. García Sánchez is a Distinguished Lecturer of the EDS, founder and past Chair of CAS/ED/PEL Venezuela Chapter, presently is a member of IEEE's Graduate and Undergraduate Teaching Awards Committee, a member of EDS Graduate Student Fellowship Subcommittee, Vice-Chair of Region 9 EDS Subcommittee for Regions & Chapters, and elected member of EDS AdCom.

JUIN J. LIOU (see Section I. of this article)

B. FIRST-TIME ELECTEES:

GIORGIO BACCARANI (G.B.) received his Dr. Ing. degree in Electrical Engineering in 1967 and his Dr. degree in Physics in 1969, both from the University of Bologna, Italy, where he is now professor of Digital Electronics. He is currently Director of the Research Center on Electronic Systems (ARCES). G.B. has devoted his research work to various aspects of Microelectronics, including processing technology, device physics and characterization, current transport in semiconductor materials and devices, sub-micron MOSFET optimization and design, numerical analysis of

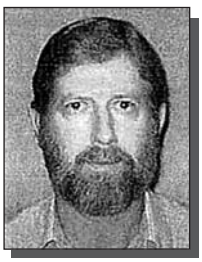
semiconductor devices. He has authored or coauthored about 180 papers, and his activity is the result of an extensive cooperation with national and European Industries, and with a number of research Institutions in Italy and abroad. He is a Fellow of the IEEE.



M. JAMAL DEEN (Fellow '03) was born in Georgetown, Guyana. He is Professor of Electrical and Computer Engineering and Senior Canada Research Chair in Information Technology, McMaster University, Canada. Dr. Deen was a Fulbright-Laspau Scholar from 1980 to 1982, and an American Vacuum Society Scholar from 1983 to 1984. He is a Distinguished Lecturer of the IEEE EDS; was awarded the 2002 Callinan Award from the Electrochemical Society and the Distinguished Researcher Award, Province of Ontario in July 2001. Dr. Deen is currently an Editor of *IEEE Transactions on Electron Devices*; Executive Editor of Fluctuations and Noise Letters; and Member of the Editorial Board of Interface and The Journal of Nanoscience and Nanotechnology. He has been elected a Fellow of the Engineering Institute of Canada (EIC), the Electrochemical Society (ECS) and the American Association for the Advancement of Science (AAAS).

JAMES B. KUO received a Ph.D. degree from Stanford University in 1985. From 1985 to1987, he was a research associate in IC Lab of Stanford. Since 1987 he has been with National Taiwan University, where he currently is a professor. Between 2000 and 2002, he has been a professor at University of Waterloo in Canada, where he was awarded the prestigious Canada Research Chair on Low-Voltage CMOS VLSI. Currently he is with SFU in Canada, on leave from NTU. His research expertise is in the field of low-voltage CMOS VLSI circuits and compact modeling of CMOS VLSI devices. He became an IEEE fellow in 1999 for contributions to modeling CMOS VLSI devices. He served as the VP of Membership for the IEEE Electron Devices Society 2004-2005. He has published 300 technical papers and authored eight textbooks on CMOS VLSI. He has graduated 80 graduate students specialized in CMOS VLSI working in leading microelectronics companies

HUILING SHANG received her Ph.D. degree in Electrical Engineering from Lehigh University, Bethlehem, Pennsylvania, in 2001. She has been working in silicon technology department at IBM T. J. Watson Research Center as research staff member since her graduation. Her current research focuses on the novel material fabrication and device structures for 32nm node and beyond. Her research interests include strained Germanium and strained Silicon Germanium channel CMOS device design and integration; transport physics in ultra thin SOI device and FinFET device technologies. She is a member of IEEE Electron Devices Society and Sigma Xi Honorary (scientific research) Society.



JACOBUS W. SWART received the B. Engineer and Dr. Engineer Degrees in 1975 and 1981 respectively, from the Polytechnic School, University of São Paulo, Brazil. Following, he worked at: K. U. Leuven, Belgium, 1982-83; CTI, Campinas, 1984; LSI-University of São Paulo, 1985-88, RTI, USA, 1991, The School of Electrical and Computer Engineering, State University of Campinas, since 1988, presently as Full Professor. Dr. Swart has published 40 papers in Journals and 150 full papers in Proceedings of Conferences. He has advised 32 Dr. and MSc. degree students. He is a Senior Member of IEEE, member of ECS, SBMicro, SBMO and SBPC and has been president of SBMicro twice, 1988-90 and 1998-2000. He is Chair of the ED South Brazil Chapter.

SUNIT TYAGI is Senior Principal Engineer with Intel Corporation, responsible for next generation microprocessor for servers and enterprise computing. He was previously responsible for process integration and transistor design till 2005. Tyagi joined Intel in 1991 and has worked on transistor design, circuit design methodology, process integration, and yield on Intel's advanced CMOS logic technologies, and led the development of transistor for 65nm logic process technology.

Tyagi is an active member of IEEE since 1980 and has served as a member of the EDS Education Committee and as Vice-Chair of the SRC for Regions 4, 5 and 6 since 1999. Tyagi was the chairman of a local student chapter in Bombay for the period of 1983 and 1984.

He got his Bachelors in Electrical Engineering from IIT, Bombay in 1984 and his M.S and Ph.D. In Electrical, Computers and Systems Engineering from Rensselaer, Troy, New York in 1987 and 1991 respectively.

Hiroshi Iwai
EDS Chair of Nominations and Elections
Tokyo Institute of Technology
Yokohama, Japan

Call For Nominations - EDS AdCom

The Electron Devices Society of the IEEE invites the submission of nominations for election to its Administrative Committee (AdCom). Presently, the AdCom meets twice per year and is composed of 22 members. Seven members will be elected this year for a term of three years, and a maximum of two consecutive terms is allowed. In 2006, the election will be held after the AdCom meeting on Sunday, 10 December. Electees begin their term in office on 1 January 2007. For your information, the nominees do not need to attend the AdCom Meeting/Election to run.

Nominees are being sought to fill the slate of candidates. Nominees may be self-nominated, or may be nominated by another person; in the latter case, the nominee must have been contacted and have agreed to serve if elected. Any member of EDS in good standing is eligible to be nominated. As another condition for nomination and election, a nominee is expected to attend the two annual AdCom meetings. In general, the travel and accommodation costs to attend these meetings are borne by the elected member.

Please send your nominee's name, address, and supporting information to the EDS Executive Office Administrator, Laura J. Riello, IEEE, 445 Hoes Lane, Piscataway, NJ 08854, Fax: 732-235-1626, E-Mail: l.riello@ieee.org in time to be received by the deadline of 15 October 2006. It is very desirable that submissions include a biographical summary in a standard two-page format. The EDS Executive Office can provide you with an example of the format. If you have any questions regarding the nomination requirements or process, feel free to contact the Nominations and Elections Chair, Hiroshi Iwai (h.iwai@ieee.org).

EDS Administrative Committee Election Process

The Members-at-Large (MAL) of the EDS AdCom are elected for staggered three-year terms, with a maximum of two consecutive terms. The 1993 Constitution and Bylaws changes mandated increasing the number of elected MAL from 18 to 22, and required that there be at least two members from both IEEE Region 8 (Europe, Middle East & Africa) and Region 10 (Asia & Pacific). In 2003, EDS made changes to its Constitution and Bylaws to require that at least one elected AdCom member is a Graduate of the Last Decade (GOLD member). A GOLD member is defined by IEEE as a member who graduated with his/her first professional degree within the last ten years. It is also required that there are at least 1.5 candidates for each opening. In 2006, seven positions will be filled.

The election procedure begins with the announcement and Call for Nominations in the EDS Newsletter. The slate of nominees is developed by the EDS Nominations Committee and includes the non-Committee and self-nominations received. Nominees are asked to submit a two-page biographical resume in a standard format. Nominations are closed on 15 October, and the biographical resumes are distributed to the 'full' voting members of AdCom prior to the December AdCom meeting. The election is then held after the conclusion of the meeting. The nominees do not need to attend the AdCom Meeting/Election to run. On the other hand, if you are elected, you are expected to attend the two AdCom meetings a year. In general, the travel and accommodation costs to attend these meetings are borne by the elected member.

A continuing flow of new AdCom members who are interested in working for the improvement of the Society and its related technical areas is essential for the continued development of EDS and the field of electron devices. Those interested in the field, the Society, and its operations are encouraged to attend AdCom meetings, become involved in Society activities, and consider running for election to AdCom.

Hiroshi Iwai
EDS Chair of Nominations and Elections
Tokyo Institute of Technology
Yokohama, Japan

EDS Delegation to China

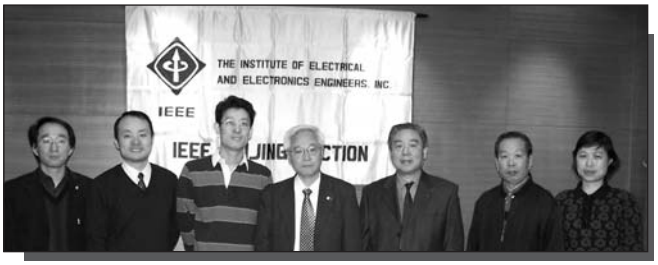


Figure1. EDS Delegation visit to Beijing, from right: Prof. Xia of Beijing Chapter, Prof. Zhou of CIE, Prof. Liao of Beijing Chapter, Prof. Iwai of EDS, Prof. Wang of EDS, Prof. Ren of Beijing Chapter and Prof. Feng of Beijing Chapter.

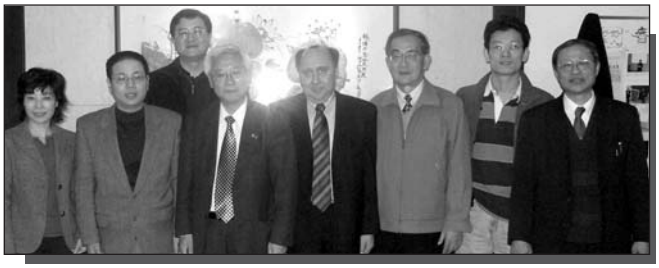


Figure 2. EDS Delegation in Shanghai, from right: Prof. Tang, Director of Microelectronics Institute of Fudan University, Prof. Wang of EDS, Prof. Li, Chair of Shanghai Chapter, Prof. Claeys of EDS, Prof. Iwai of EDS, Dr. Gao Vice Chair of Shanghai Chapter, Prof. Ru of Shanghai Chapter and Prof. Yu of Shanghai Chapter.

A mini IEEE Electron Devices Society (EDS) Delegation visited China in March 2006 with the goal to promote EDS values and presence in China, the emerging semiconductor power. The Delegation consisted of four EDS Officers including: Prof. Hiroshi Iwai of the Tokyo Institute of Technology and EDS Jr. Past President; Prof. Cor Claeys of IMEC and EDS President-Elect; Prof. Juin J. Liou of the University of Central Florida and EDS Treasurer; and Prof. Albert Wang of the Illinois Institute of Technology and EDS Vice-President of Membership. This Delegation occurred in conjunction with the 10th Workshop and IEEE EDS Mini-colloquia on Nanometer CMOS Technology (WIMNACT -10) - Nanoelectronics Workshop in China, held in three cities in March (please read the separate report in this Issue).

The Delegation visit started in Beijing on March 10th, where Prof. Iwai and Prof. Wang held a meeting with Prof. Mengqi Zhou, Secretary of the Chinese Institute of Electronics (CIE) and IEEE Beijing Section, and Prof. Fujiang Liao, Chair of the IEEE ED Beijing Chapter (Fig. 1). This meeting cleared out many logistic issues in possibly establishing new EDS chapters in other Chinese cities. The Delegation next traveled to Chengdu, a major semiconductor-rich city in China, where the Delegation visited the University of Electronics Science and Technology of China on March 13th and delivered the first DL Seminar for the 10th WIMNACT. In principle, local semiconductor professionals agreed to establish an EDS Chapter in the Chengdu area to serve the booming semiconductor community. The next stop for the Delegation was Wuhan, another Chinese city with booming microelectronics activities. The Delegation visited the Huazhong University of Science and Technology and the second DL Seminar of the 10th WIMNACT was held there on March 15th. As a result of this visit, the locals agreed in principle to set up a new EDS chapter in Wuhan. The 4th stop of the EDS Delegation was Harbin where the Delegation visited the Harbin Institute of Technology and delivered the 3rd DL Seminar for the 10th WIMNACT on March 17th. Our meeting with the local microelectronics professionals was very successful and a new EDS chapter shall be established soon to serve the Harbin region. The last stop for the Delegation was Shanghai, where the EDS delegates met with Officers of the ED Shanghai Chapter on March 20th (Fig. 2) and discussed various issues related EDS activities, including the organization work for the upcoming International Conference on Solid-State and Integrated Circuit Technology (ICSICT), a major regional conference co-sponsored by EDS to be held in October 2006 in Shanghai. In general, this EDS Delegation to China was very successful by meeting its goals to enhance EDS presence in China and to ensure EDS is part of the success of the new China Microelectronics boom.

Albert Wang
EDS Vice-President of Membership
Illinois Institute of Technology
Chicago, IL, USA

EDS Chapter Subsidies for 2007

The deadline for EDS chapters to request a subsidy for 2007 is 1 September 2006. For 2006, the EDS AdCom awarded funding to 53 chapters, with most amounts primarily ranging from US$250 to US$1,000. In June, Chapter Chairs were sent an e-mail notifying them of the current funding cycle and providing them with a list of guidelines. In general, activities which are considered fundable include, but are not limited to, membership promotion, travel allowances for invited speakers to chapter events, and support for student activities at local institutions. Subsidy requests should be sent via e-mail or fax to the EDS Administrator, Laura J. Riello, IEEE, EDS Executive Office, 445 Hoes Lane, Piscataway, NJ 08854, l.riello@ ieee.org or fax 732 235 1626. Prior to the submission of the subsidy request, the Chapter Chair must submit a chapter activity report to its respective SRC Chair and Laura Riello of the EDS Executive Office by July 1. This report should include a general summary of chapter activities (one to two pages) for the prior July 1st - June 30th period. You must also attach a copy of the activity report to your chapter subsidy request. Final decisions concerning subsidies will be made by the EDS SRC Chairs/Vice-Chairs in December. Subsidy checks will be issued by late January.

EDS Distinguished Lecturers Participate in the 10th WIMNACT - China

The 10th Workshop and IEEE EDS Mini-colloquia on NAnometer CMOS Technology (WIMNACT-10) - Nanoelectronics Workshop in China, was held in conjunction with the EDS Delegation to China in March 2006 (please refer to a separate report in this issue). The WIMNACT-10 consisted of three DL seminars held in three microelectronics-rich cities in China, i.e., Chengdu, Wuhan and Harbin. The WIMNACT-10 was jointly sponsored by the Electron Devices Society, IEEE Beijing Section and the Chinese Institute of Electronics. Four Distinguished Lecturers (DL) participated in the WIMNACT-10 including: Prof. Hiroshi Iwai of the Tokyo Institute of Technology and EDS Jr. Past President; Prof. Cor Claeys of IMEC and EDS President-Elect; Prof. Juin J. Liou of the University of Central Florida and EDS Treasurer; and Prof. Albert Wang of the Illinois Institute of Technology and EDS Vice-President of Membership. The WIMNACT-10 was composed of four DL topics: "Future CMOS Scaling and Its Manufacturing" by Prof. Iwai, "Low Frequency Noise Characterization of Advanced Semiconductor Materials and Devices" by Prof. Claeys, "Robust ESD Protection in CMOS Technology" by Prof. Liou and "RF CMOS Comes to Reality" by Prof. Wang. The first DL seminar (Fig. 1) was held at the University of Electronics Science and Technology of China (UESTC), Chengdu, on March 13th, and chaired by Prof. Jianguo Ma of the School of Electronics Engineering of UESTC. The DL seminar was well received by an audience of more than 150 of whom most were students. On March 15th, the second DL seminar (Fig. 2) was held at the Huazhong University of Science and Technology (HUST) in Wuhan, which was chaired by Prof. Xavier Zou, Chairman of the Dept. of Electronic Science and Technology of HUST. More than 200 participants of local professionals and students attended the DL seminar. The third DL seminar (Fig. 3) was held at the Harbin Institute of Technology (HIT), Harbin, on March 17th and was moderated by Prof. Zhigang Mao of the Microelectronics Center of HIT, which was also warmly received by an audience of more than 100 faculty members and students. Overall, the WIMNACT-10 was a great success in promoting EDS values and presence in China, an emerging power house in semiconductors, and the event certainly serves as a catalyst to possibly establish new EDS chapters in the three cities.

Figure 1. Seminar-1 in Chengdu: Prof. Wang of EDS (left 3), Prof. Ma of UESTC (left 5), Prof. Iwai of EDS (left 7), Prof. Claeys of EDS (left 9) and Prof. Liou of EDS (left 11).

Figure 2. Photo taken for Seminar-2 in Wuhan, from right: Prof. Zou of HUST, Prof. Wang of EDS, Prof. Liou of EDS, Prof. Iwai of EDS, Prof. Claeys of EDS, Prof. Wei Liu, Vice President of HUST and Prof. Jiang of HUST.

Figure 3. Seminar-3 in Harbin, from right: Prof. Mao of HIT, Prof. Liou of EDS, Prof. Iwai of EDS, Prof. Jiecai Han, Vice President of HIT, Prof. Claeys of EDS, Prof. Wang of EDS and Prof. Xiaohong Wang of HIT.

Albert Wang
EDS Vice-President of Membership
Illinois Institute of Technology
Chicago, IL, USA

EDS Distinguished Lecturers Visit Universities in Argentina and Peru

Dr. Hiroshi Iwai, EDS Jr. Past President, and Dr. Juin Liou, IEEE EDS Treasurer, recently took a trip to South America to promote EDS activities and establish new EDS chapters in the region. They first visited the University of Buenos Aires (UBA), in Buenos Aires, Argentina, on February 27, 2006. They met with Dr. F. Grasso, Dean of the College of Engineering, Dr. J. C. Fernandez, Director of Academics at the university and several other professors and researchers from UBA, ITBA (Inst. Tech. Buenos Aires) and UNLA (Univ. of Laplata), to introduce the IEEE EDS and discuss the possibility of establishing a new chapter in Buenos Aires. Dr. N. Lerendegui of GALIX who is the President of IEEE Argentina Section attended the meeting and promised his strong effort for this together with the people of the universities. Drs. Iwai and Liou also gave DLs on "Downscaling of CMOS and Manufacturing" and "Recent Advances in RF CMOS", respectively.

On March 1, 2006, Drs. Iwai and Liou traveled to Peru, and visited the University of San Martin in Lima, Peru. They met with Dr. Bao-Garcia, Dean of the College of Engineering, Dr. Tejada-Polo and several other professors, researchers, officers and students of the university to introduce the IEEE EDS and discuss the possibility of establishing a new chapter in Lima. They promised to make a strong effort to form the chapter and requested EDS distinguished lecturers to attend their convention, VISION 2006, to be held this October. Drs. Iwai and Liou also gave DLs on "Downscaling of CMOS and Manufacturing" and "Recent Advances in RF CMOS", respectively.

The local responses to Drs. Iwai and Liou's visits to Buenos Aires and Lima were very positive, and it is expected two new EDS chapters in these two cities will be established before the end of 2006.

- by Juin J. Liou

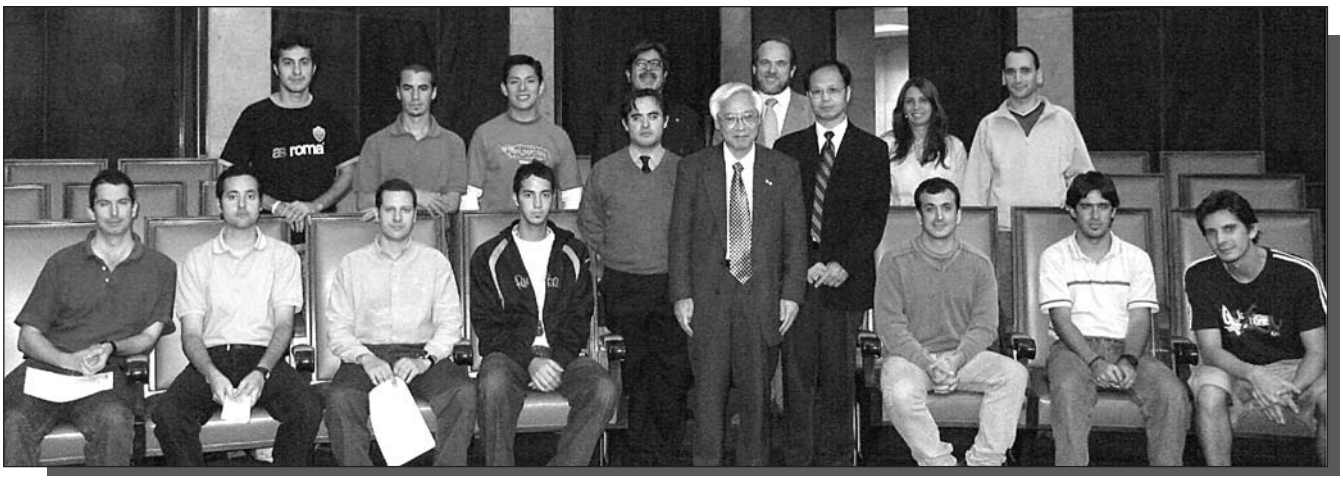


Figure 1. Dr. Hiroshi Iwai, EDS Jr. Past President and Dr. Juin Liou, EDS Treasurer (1st row, 6th & 7th from left), with attendees from the seminars held at the University of Buenos Aires, Argentina.

Figure 2. Dr. Juin Liou, EDS Treasurer and Dr. Hiroshi Iwai, EDS Jr. Past President (seated 1st row, 3th & 4th from left), with attendees from the seminars held at the University of San Martin, Lima, Peru.

William R. Cherry Award

This award is named in honor of William R. Cherry, a founder of the photovoltaic community. In the 1950's, he was instrumental in establishing solar cells as the ideal power source for space satellites and for recognizing, advocating, and nurturing the use of photovoltaic systems for terrestrial applications. The William R. Cherry Award was instituted in 1980, shortly after his death. The purpose of the award is to recognize engineers and scientists who devote a part of their professional life to the advancement of the technology of photovoltaic energy conversion.

This award is presented at each IEEE/EDS Photovoltaic Specialists Conference (PVSC). The recipient is selected by the William R. Cherry Committee composed of past PVSC conference chairpersons and past recipients of the award.

This year's winner of the Cherry Award is Antonio Luque and he was honored at the PVSC held in Waikoloa, Hawaii, May 7-12, 2006. **Antonio Luque** is presently leading the Integrated Project FULLSPECTRUM co-funded by the European Commission and involving 19 European R&D centers. The major thrust of the project is a search for novel concepts in photovoltaics.

Antonio Luque

Antonio Luque, born in Malaga, Spain, holds the degree of Dr. Engineer in Telecommunication and is also Doctor Honoris Causa of the Universities of Jaen and Carlos III of Madrid. He has been Full Professor of Electronic Technology at the Universidad Politécnica de Madrid, since 1970, where he leads the Institute of Solar Energy that he founded in 1979. His research activity is mainly devoted to the photovoltaic conversion of solar energy. He invented the bifacial cell in 1976 which is now fabricated by Isofotón, a company which he founded in 1981 and that today is in the World top ten of cell manufacturers. Subsequently Dr. Luque devoted part of his effort to the development of photovoltaic concentrators and in 1989 he wrote, with his co-workers, the first monograph devoted to photovoltaic concentration. More recently he and his co-workers have proposed the new Intermediate Band Solar Cell —a concept that might overcome the fundamental efficiency limitations of conventional single band gap solar cells. He is also active in development of improved silicon purification. He has published more than 250 scientific papers as well as several books and he holds 12 patents.

He has frequently participated in the organization of the European and World Photovoltaic conferences and was the Chairman of the 10th EC Photovoltaic Solar Energy Conference held in Lisbon in 1991.

Among other honors he has been awarded the Spanish National Prize for Technology Research in 1989 and again in 2003; the Alexander-Edmond Becquerel Prize in PV research, granted by the EC, in 1992 and the King James I Award for Environmental Research from the Crown Prince in 1999. He is a member of the Spanish Royal Academy of Engineering and a foreign member of the Russian Academy of Engineering.

John D. Meakin
Consultant
Weybridge, VT, USA

Congratulations to the EDS Members Recently Elected to IEEE Senior Member Grade!

Giovanni Anelli	David Esseni	Janice Hudgings*	Andrew Mason	Ricardo A. Reis	James Warnock
Reza Arghavani	Daniel Foty	Raymond Hueting	Hitoshi Matsuo	Santiago Silvestre*	Sai Peng Wong
Masahiro Asad	Kazuhito Furuya	Arvind Kumar*	Todd Mitchell	Theresa Mayer Stellwag	Soon Yoon
Snorre Aunet*	Geon Hahm	Jatinder Kumar	Robert Montgomery	Keeyoung Suh	Chadwon Young*
Ralf Brederlow*	Judy Hoyt*	Guifang Li	Chang Seo Park	Dina Triyoso	Shaofeng Yu
Jeffrey Bulson	W. Margaret Huang	Samjid Mannan	Jean-Pierre Raskin	Brent Wagner	Guoliang Zhou

* = Individual designated EDS as nominating entity

If you have been in professional practice for 10 years, you may be eligible for Senior Membership, the highest grade of membership for which an individual can apply. New senior members receive a wood and bronze plaque and a credit certificate for up to US $25 for a new IEEE society membership. Upon request, a letter will be sent to employers, recognizing this new status.

For more information on senior member status, visit http://www.ieee.org/membership/grades_cats.html#SENIORMEM. To apply for senior member status, fill out an application at http://www.ieee.org/organizations/rab/md/smelev.htm.

Status Report from the 2005 Graduate Student Fellowship Winners

In 2000, the IEEE approved the establishment of the Electron Devices Society Graduate Student Fellowship Program. The Program is designed to promote, recognize, and support graduate level study and research within the Electron Devices Society's Field of Interest, which includes: All aspects of the physics, engineering, theory and phenomena of electron and ion devices such as elemental and compound semiconductor devices, organic and other emerging materials based devices, quantum effect devices, optical devices, displays and imaging devices, photovoltaics, solid-state sensors and actuators, solid-state power devices, high frequency devices, micromechanics, tubes and other vacuum devices.

In deference to the increasing globalization of our Society, at least one fellowship is to be awarded to students in each of three geographical regions: Americas, Europe/Middle East/Africa, and Asia & Pacific.

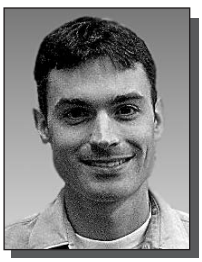
In July 2005, EDS announced the winners of the 2005 Fellowships. There were four winners: Tony Low Aik Seng of the National University of Singapore, Singapore; Sun-Jung Kim of the National University of Singapore, Singapore; Christopher J. Morris of the University of Washington, Washington, USA and Elena I. Smotrova of the National Academy of Sciences of Ukraine, Ukraine. The winners are pursuing distinctly different research topics for their doctoral degrees. The following are brief progress reports written by the award winners.

Tony Low Aik Seng

I am currently working on my Ph.D. thesis "Numerical modeling of field-effect transistor based on thin film semiconductor" (expected to submit before August 2006), while serving my appointment as a research officer in Silicon Nano-Device Laboratory, Singapore. Several new journal papers in preparation includes (1) calculation of electronic structures of thin film semiconductors using empirical pseudopotential method, (2) study of access geometry effects and spatial dependent transport mass in quantum transport through 2D waveguide, and (3) finite element analysis study of quantum transport through roughen 2D waveguide. All these new studies will hopefully shed new light on the device physics of field-effect transistor based on thin film semiconductor, especially in the quantum regime.

Sun-Jung Kim

I received my Ph.D. degree in Electrical & Computer Engineering from the National University of Singapore in December 2005. My Ph.D. research was on the high-k metal-insulator-metal (MIM) capacitors for RF/Mixed-signal IC applications. Currently I am with Samsung Semiconductor R&D Center, Korea, as a senior research engineer for sub-50nm Flash memory technology development.



Christopher J. Morris

After several initial studies on the concepts of self-assembly, I am working toward my final project of self-assembled, 3-D integrated circuits from micro fabricated building blocks. I am very close to successfully incorporating a low-melting point solder alloy into a post-CMOS fabrication process, which has been the primary challenge in the fabrication of these blocks. The solder will provide capillary forces to drive the assembly of each block, as well as permanent electrical and mechanical connections. The successful fabrication of these building blocks will enable a new 3-D circuit architecture, and open the door to heterogeneous integration on the micrometer scale.

Elena I. Smotrova

The area of my concentration is mathematical and numerical modeling of semiconductor micro cavity lasers: eigenvalue problems for the Maxwell equations specifically tailored to extract not only frequencies but also linear thresholds of the lasing modes, and development of efficient and accurate numerical algorithms for the wavelength-scale optics with the aid of integral equations. Currently I am studying the lasing of photonic molecule lasers formed by micro disks. The main outcome of this study is a possibility of the lowering of thresholds by a careful tuning of the distance between the disks. Further I plan to work on arbitrarily shaped resonators.

Paul K. L. Yu
EDS Vice-President of
Educational Activities
University of California
at San Diego
La Jolla, CA, USA

Steven A. Parke
EDS Graduate
Student Fellowship Chair
Boise State University
Boise, ID, USA

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Correction to the December 2005 AdCom Meeting Summary in the April 2006 Issue

We regret an error made in the April 2006 issue of the EDS Newsletter in the article, December 2005 AdCom Meeting Summary. The dates of some of the IEEE and EDS awards received by EDS members were incorrectly stated. The following revised chart correctly identifies the year of these awards.

2005 EDS Awards	Recipient/Affiliation
EDS J.J. Ebers	Bijan Divari (IBM)
EDS Distinguished Service Award	Cary Yang (Santa Clara University)
2006 IEEE Awards	**Recipient/Affiliation**
IEEE Medal of Honor	James Meindl (Georgia Tech)
IEEE Frederick Phillips Award	Louis Parrillo (Parrillo Consulting)
IEEE Jun-ichi Nishizawa Medal	Mitsumasa Koyanagi (Tohoku University), Kiyoo Itoh (Hitachi) and Hideo Sunami (Hiroshima University)
IEEE Andrew S. Grove Award	Chang-Gyu Hwang (Samsung)
IEEE Daniel Noble Award	Carlos A. Paz de Araujo (University of Colorado)
IEEE Cleo Brunetti Award	Susumu Namba (Nagasaki Institute of Applied Science)

EDS Member recipients of the 2006 IEEE Awards and two 2005 EDS Awards

Report from the EDS Vice-President of Regions/Chapters

(continued from page 8)

in conjunction with the EDS AdCom meeting, was preceded by the WIMNACT-7 mini-colloquium. Other mini-colloquium and technical meetings, in which 5 to 10 Distinguished Lecturers are participating, have been organized in the USA, Boise (WMED, April 2005), Singapore (WIMNACT 8, July 2005), Veracruz (August 2005), Japan (WIMNACT 9, September 2005) and Hong Kong (HKWSM December 2005). In general, the number of events organized by the different chapters has been growing and in different regions extensive use has been made of the Distinguished Lecturers program. This will ensure that the successful DL program remains attractive in the future and that the number of chapters using DL presentations will further increase.

In 2005 special effort was devoted to review and to improve the Chapter Partner program in order to optimize the support given to the chapters. The winner of the annual EDS Chapter of the Year Award went in 2005 to the Bangalore Chapter.

Much attention is also given to increase the number of chapters in select regions such as Region 9 (Latin America) and Region 10 (Asia & Pacific). These regions have a good growth potential in microelectronics and will strongly increase their EDS activities in the coming years. Therefore, in the first quarter of 2006, an EDS delegation went on a promotion tour to Argentina, Peru and China. Presently, the formation of about 10 new chapters in Region 10 is under discussion or in progress.

For 2006, Regional Chapter meetings are scheduled for Region 8 (Naples, Italy, June), and Regions 4-6 (San Francisco, USA, December). The meeting in Naples will be preceded by a mini-colloquium and combined with the EDS AdCom meeting. The Regions 4-6 Chapters Meeting will also be held in conjunction with the EDS AdCom meeting as well as the IEDM in San Francisco. In addition, IWNC-1 (Japan) and WIMNACT 10 (China: Chengdu, Wuhan and Harbin) were held this January and March, respectively.

The well being of a chapter is directly related to the membership growth and strongly driven by the organization of activities and events in response to the expectations of its members. The chapters are there for their members and their direct involvement and participation is therefore crucial. All possible input is highly appreciated and will surely be taken into account.

Cor L. Claeys
EDS Vice-President of Regions/Chapters
IMEC
Leuven, Belgium

Regional and Chapter News

USA, Canada & Latin America (Regions 1-6, 7 & 9)

ED/CPMT Orlando

- by Ravi Todi

The ED/CPMT Chapter of the Orlando Section organized a two day International Electron Devices and Materials Colloquium at the University of Central Florida, Orlando, Florida, February 24-25, 2006. The colloquium started with a welcome note from Ravi Todi, ED/CPMT Chair of the Orlando Section, followed by brief messages from the dean of college of engineering, Dr. Neal Gallagher, and EECS director Dr. Issa Batarseh. The first talk of the colloquium was given by the EDS President, Dr. Ilesanmi Adesida, on GaN and related materials, followed by a presentation from Dr. Michael Shur on "Terahertz Photonics and Electronics." Dr. Rona Belford presented an interesting seminar on strained silicon devices. Professor Stephen Park talked about the impact of flexible threshold on ultra-low power circuit design. This was followed by an hour lunch break, in which everyone had an opportunity to interact.

The post lunch session was started by EDS President-Elect, Dr. Cor Claeys, with his presentation on low frequency noise characterization of advanced semiconductor materials and devices. Professor Durga Misra discussed high-k gate dielectrics for sub 65 nm CMOS devices, followed by an interesting talk by Professor Jack Lee of UT-Austin, entitled "High-k and "Higher-k" Dielectrics." Dr. Supratik Guha, senior manager at IBM T.J. Watson Research Center, discussed materials interaction of high-k gate stack of silicon technology at nanoscale. Professor Kevin Coffey from AMPAC presented an interesting discussion on the electrical resistivity of interconnects and the classical size effect. The first day of the colloquium was concluded by Dr. Paul Agnello, manager at IBM, by presenting the integration challenges for 45 nm node and beyond.

The first session of day two was dedicated to bio-electronics, with Professor Jamal Deen discussing the applications and challenges of integrated biosensors, followed by "Bio-electronics, Nanotechnology For the Brain" presented by Professor Vikram Kapoor. Professor Francisco Garcia-Sanchez, from Venezuela, discussed the application of Lambert's W function for electron device modeling. Dr. Paul Yu, discussed high power photo diode for antenna applications. The last talk of the two-day colloquium was presented by Dr. Samar Saha from Silicon Storage Technology, Inc. The colloquium was concluded by a vote of thanks presented by Mr. Matthew Erickson, the Chair of IEEE student branch at UCF.

~ Ibrahim Abdel-Motaleb, Editor

From left to right: Standing, Stephen Parke, Paul Agnello, Jhon Shen, Vikram Kapoor, Peter Yuan, Kevin Coffey, Supratik Guha, Matthew Erickson, Jamal Deen, Jack Lee, Paul Yu, Juin Liou, Francisco Garcia Sanchez, Kalpathy Sundaram, Durga Misra. Sitting: Ravi Todi, Rona Belford, Samar Saha, Ilesanmi Adesida, Michael Shur and Cor Claeys

ED South Brazil and UNICAMP Student Branch

- by Jacobus W. Swart and Leandro T. Manera

On February 9 and 10, 2006, the ED South Brazil Chapter and ED Student Chapter at UNICAMP, organized the 2nd Workshop on Semiconductors and Micro & Nano Technology – SEMINATEC 2006, aiming to show and share results of researches developed at the universities and laboratories of the region, including a national research network called NANOFAB.

In this second edition, three invited lectures were presented. The first one was delivered by Dr. Hercules Neves, from IMEC, Belgium, entitled "Development of BioMEMS". Following, the second was given by Laurent Roussel, from FEI company, The Netherlands, entitled "Focused Ion Beam – a powerful analytical and nanofabrication tool". The third lecture entitled "Tools, methodologies and scientific issues for the modeling of advanced semiconductors devices" was delivered by IEEE EDS Distinguished Lecturer, Prof. Siegfried Selberherr, from the Technical University of Vienna, Austria. Additionally, short invited talks were given by local researchers: Prof. Fernando Galembeck and Dr. Antonio Ramirez on analytical tools at UNICAMP and at LNLS respectively; and Dr. Andre Torre, on "Micro and Nanotechnology in the agribusiness". Oral short presentations were given by research members of NANOFAB and by industry representative members. A poster session with about 50 papers was held and a best paper award was

Invited speakers Prof. Siegfried Selberherr (1st right) and Dr. Hercules Neves (3rd from right) and organizing committee members

elected. At the end, a round table on "Semiconductors – the importance for innovation and the opportunities for collaboration between university and industry" was held. More than 130 people attended the workshop. Details about the workshop, as well as a copy of the proceedings, can be found at http://www.ccs.unicamp.br/seminatec/. As a social event, a cocktail hour was organized for all participants.

ED México City

- by Rodolfo Quintero

E. Fred Schubert, Distinguished Lecturer and professor of the Rensselaer Polytechnic Institute, lectured on optoelectronics in Mexico City, on January 13, 2006. The one-day event consisted of a morning 3-hour short course "Light Emitting diodes and Solid-State Lighting", and an afternoon conference entitled "Innovations in Light Emitting Devices". The event, hosted by CINVESTAV, an important postgraduate university in Mexico, attracted an audience of 135 students and professors not only from CINVESTAV, but from other universities, one of them as far as 400 Km. from Mexico City. Our chapter thanks Prof. Schubert, the Electron Devices Society and CINVESTAV, for helping us to make this event possible.

ED Recife

- by Edval J. P. Santos

Recife is the headquarters of a new EDS Chapter, the IEEE ED Recife Chapter was formed on November 3, 2005. Elections were held in February, 2006, and the elected officials are shown in the photo. From the left: Chapter Chair, Dr. Edval J. P. Santos from the Universidade Federal de Pernambuco; Vice Chair, Dr. José Sérgio da Rocha Neto from the Universidade Federal de Campina Grande; Eng. Alexandre Branco Guerra, as the Treasurer and Eng. Khyale Santos Nascimento, as Secretary.

Professor Schubert and some of the attendees, celebrating after the lectures

Recife-Brazil-469 Years

Edval J. P. Santos

José Sérgio da Rocha Neto

Alexandre Branco Guerra

Khyale Santos

Chapter Members have presented lectures on various themes, such as: "Building a low cost supercomputer for nanoelectronics simulations" by Alexandre Branco Guerra presented at the Laboratory for Devices and Nanostructures; "AFM/STM" by Edval J. P. Santos presented at the Geology Department, "Brazilian Digital TV System: an opportunity" by Edval J. P. Santos, presented at the Laboratory for Devices and Nanostructures.

The ED Recife Chapter plans to participate in the 3rd Engineering Week, III SEENGE, at the Universidade Federal de Pernambuco, to be held from May, 31 to June 2, 2006.

~ Jacobus W. Swart, Editor

EUROPE, MIDDLE EAST & AFRICA (REGION 8)

ED/MTT/CPMT/COM/SSC Novosibirsk

- by Viatcheslav P. Shuvalov

In accordance with IEEE Bylaws, at the end of 2005, the period of authority of the Russia Siberia Section ExCom was exhausted. As a result, the Section ExCom was renewed and Dr. Sc., Prof. Andrey N. Fionov from the Siberian State University of Telecommunications and Informatics, was appointed as new Section Chair for a 2 year term. Ms. Nadezhda A. Dvurechenskaya, from Novosibirsk State Technical University (NSTU), was appointed Section Vice-Chair and Associate Prof. Dr. Alexander V. Gridchin from NSTU, was appointed as Section Treasurer/Secretary.

This year the Section is planning to organize the first Siberian Section Congress in conjunction with the 16th International Conference on Computer Graphics and Applications, GraphiCon'2006, which will be held on July 1-5, 2006, in Novosibirsk (Novosibirsk Scientific Center, Siberian Branch of Russian Academy of Sciences, http://www.graphicon.ru). This Congress is planned as the first joint administrative and scientific meeting, which will be used for attracting interest to the activities of the IEEE in Siberia.

MTT/ED/AP/CPMT Saratov-Penza Chapter

- by Nikita M. Ryskin

The XIII Saratov Winter School and Seminar in Microwave Electronics and Radio Physics was successfully held at the "Volzhskie Dali" Hotel, on the picturesque banks of the Volga River near Saratov, Russia, January 31 to February 4, 2006. Such schools have been held every third year since 1970, giving a unique opportunity for presentation and discussion of broad topics related to vacuum microwave electronics. The XIII School was organized by Saratov State University (SSU) and State Scientific and Education Centre "College" of SSU, with technical and financial co-sponsorship from the IEEE Saratov-Penza Chapter. Other financial co-sponsors included the Russian, Foundation for Basic Research, "Dynasty" Foundation and two widely known Saratov manufacturers of electron devices — FSUE "Almaz" and FSUE "Contact". Members of the Saratov-Penza IEEE Chapter played an active role in the organizing of the School: Prof. D.I. Trubetskov served as Conference Chairman, Prof. Yu.I. Levin, Prof. Yu. P. Sharaevsky and Dr. N.M. Ryskin were key members of the Local Organizing Committee responsible for the technical and social program.

The topics of the School included modern software for CAD and simulation of microwave devices, theory and experiment on vacuum microwave tubes (TWTs, BWOs, klystrons, magnetrons, etc.), vacuum microelectronics, gyrotrons, high-power vacuum and plasma microwave devices, nonlinear science and its application to microwave electronics. The core of Saratov Winter School was invited plenary lectures reviewing most actual problems of theory, simulation and technology of microwave electron devices. This year 22 plenary lectures were given by leading experts from Russian and foreign academia and industry. Among them were: Prof. S.P. Kuznetsov (Saratov) "Nonlinear dynamics of the backward-wave oscillator", Prof. A.D. Grigoriev (St. Petersburg) "Effective finite-element methods for simulation of microwave devices", Prof. Yu.P. Bliokh (Technion, Haifa, Israel) "The Pasotron: the latest achievements of theory and experiment", Dr. V.P. Tarakanov (Moscow) "The universal code KARAT for simulation of microwave devices, plasma processes, etc.", Prof. N.S. Ginzburg (Institute of Applied Physics, Nizhny Novgorod) "Free-electron masers with 2D Bragg cavities", and Prof. O. Dumbrajs (Helsinki University of Technology, Finland) "Stochastic processes in gyrotron". Also, the program included 28 oral and over 40 poster presentations given by the School's attendees. The total number of participants was nearly 100, from many regions of Russia (Moscow, St. Petersburg, Saratov, Tomsk, Nizhny Novgorod, etc.), and nearly 30 were postgraduate students, young scientists and engineers from Saratov universities, academic institutions and industrial companies.

Special issues of the Russian journals "Applied Nonlinear Dynamics" and "Radiophysics and Quantum Electronics" with selected papers presented at the conference, will be published in 2006.

The 7th International Conference on Actual Problems of Electron Devices Engineering APEDE 2006, will be held on September 20-21, 2006, at Saratov State Technical University, Saratov, Russian Federation.

The conference will be an inspiring forum for the exchange of new ideas and results. It will include a plenary session and technical sessions. Prospective authors are invited to submit their manuscripts in the following areas:

1. Microwave Electronics, including nanoelectronics;
2. Microwave Theory and Techniques;
3. Electron Devices and Instruments Application and Technology, power electronics.

The conference is co-sponsored by the IEEE ED Society, MTT/ED/AP/CPMT Saratov-Penza Chapter.

For sending application forms and papers please use the following information: Dr. Alexei Miroshnichenko, http://www.sstu.ru/sstu/win/konf/apede2006.html, phone +7 (8452) 525697, fax: +7 (8452) 527878, e-mail: alexm@sstu.ru.

You are welcome to send your papers and visit Saratov.

~ Alexander V. Gridchin, Editor

ED Israel

- by Gady Golan

On Thursday, March 2, 2006, Professor Frank Richter, Chemnitz University of Technology, Germany, delivered his seminar on "Thin film deposition by ion and plasma assisted processes including magnetron sputtering, plasma enhanced CVD and cathodic arc evaporation" to around 110 attendees at the Holon Institute of Technology (HIT), Holon, Israel. The seminar was chaired by Professor Gady Golan, ED Israel Chapter Chair.

On Thursday, March 23, 2006, Professor Jean-Francois Baggioni, Vice-President, EDA Operation ESTEREL Technologies, France, presented his

seminar on "Novel Construction Design Tools to Generate VHDL or Verilog from Graphical Presentation" to approximately 60 people at the Holon Institute of Technology (HIT), Holon, Israel.

Esterel Studio is a design environment, optimized for hardware IPs (such as DMAs, protocols, cache controllers, I/O subsystems, etc.) dedicated at capturing formal design specifications, enabling formal verification of properties very early in the design phase, and automating the production of synthesizable RTL (VHDL and Verilog), both for prototyping and production purposes. The seminar was chaired by Professor Gady Golan, ED Israel Chapter Chair.

~ Zhirun Hu, Editor

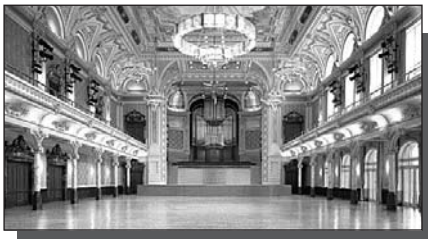
ED Sweden

- by Mikael Ostling

The IEEE ED Sweden Chapter hosted an interesting event early April. On Wednesday, April 5th, Prof. Cor Claeys, IMEC, Belgium, and the EDS President-Elect, visited the chapter and gave a highly appreciated DL lecture entitled "Defect Engineering in High-Mobility Substrates for Advanced CMOS Technologies". He was invited by KTH - Royal Institute of Technology, School of Information and Communication Technology, to act as faculty opponent for a Ph.D. dissertation the day after on April 6th. The Ph.D. student, Martin von Haartman, an IEEE student member and the recipient of the 2004 EDS Graduate Student Fellowship, presented his thesis "Low Frequency Noise Characterisation for Si and SiGe-based CMOS Transistors". The Ph.D. evaluation committee was also comprised of all IEEE Fellows: Prof. Ninoslav Stojadinovic, University of Nis, currently an Ambassador of Serbia & Montenegro to Sweden, Prof. Christer Svensson, Linköping University, and Prof. Mohammed Ismail El-Naggar, KTH.

This is the first time KTH has hosted an all IEEE Fellow Ph.D. Committee. The Ph.D. thesis supervisor was Prof. Mikael Östling, KTH and IEEE Fellow.

~ Andrzej Napieralski, Editor



Upcoming: ESREF 2006

- by Ludwig Balk

The 17th European Symposium Reliability of Electron Devices, Failure Physics and Analysis will take place at Wuppertal (Germany) from October 3- 6, 2006.

This international symposium continues to focus on recent developments and future directions in Quality and Reliability Management of materials, devices and circuits for micro-, nano-, and optoelectronics. It provides a European forum for developing all aspects of reliability management and innovative analysis techniques for present and future electronic applications.

The technical scope of the conference is:

- Quality and reliability techniques for devices and systems, reliability indicators and early detection, reliability test structures, limits to accelerated tests, screening methods and burn-in, HAST, HASS, yield/reliability relationship, field reliability, realisation of stringent Q &R requirements. Physical modeling and simulation for reliability prediction. Characterization of defects, defect models, simulation of reliability-related circuit constraints.
- Advanced Failure Analysis: Defect Detection and Analysis including electron, ion and laser beam techniques, backside techniques, scanning probe techniques, acoustic microscopy, electrical and thermal characterization, sample preparation, construction analysis, FA: case studies.
- Failure mechanisms in new materials and transistors, process-related issues, hot carriers, passivation stability, high-K gate oxides, metal migration: mechanical and thermal aspects, ESD, low-K dielectrics and Cu interconnects.
- Reliability of New Technologies, non-volatile and programmable devices, passive elements and modules, wide bandgap semiconductors, microwave and compound semiconductor devices, photonic devices: optoelectronics and lasers, SOI devices, MEMS and MOEMS, sensors and actuators, organic devices.
- Power Devices Reliability, smart-power devices, IGBT, thyristors, thermal management.
- Packaging and Assembly Reliability, bonding, solders and joints, high densities assemblies, MCM, BGA, CSP, flip-chip, connectors.

The location of the Conference is the "Historische Stadthalle" in Wuppertal, Germany, with a lot of attractive highlights in its surrounding area. It is one of the most

The first all IEEE Fellow Ph.D. Committee at KTH: From left, Prof. Mohammed Ismail El-Naggar, Prof. Christer Svensson, Prof. Cor Claeys, Dr. Martin von Haartman, Prof. Mikael Östling, Prof. Ninoslav Stojadinovic.

remarkable concert halls and conference centers in Europe

This event is organized by Prof. Ludwig Josef Balk, Bergische Universität Wuppertal, Germany. For further information, see www.esref.org or contact: esref@electronics.uni-wuppertal.de.

~ Cora Salm, Editor

ASIA & PACIFIC (REGION 10)

EDS Distinguished Lecturers Participate in the IWNC - Japan

- by Kazuo Tsutsui

For the first time, the International Workshop on Nano CMOS (IWNC), was held in Japan, at TORAY Sougou Kensyu Center, Mishima, on January 30 to February 1, 2006. The Workshop was sponsored by the IEEE ED Japan Chapter, and co-sponsored by IEEE EDS, IEEE Japan Council, Nanotechnology Researchers Network Center of Japan, Silicon Technology Division of JSAP, and Silicon Devices and Materials, Electronics Society of IEICE, Japan. The venue was located at the foot of the world famous Mt. Fuji.

The workshop covered discussions focused on the challenging Nanometer scale CMOS technology including the fields of new materials, process technology, device physics and structures, advanced analysis techniques and circuit technology. The 34 professors/experts (including 13 EDS Distinguished Lecturers) were invited to deliver the outstanding talks from Japan(18), USA(6), France(3), Italy(1), UK(1), Poland(1), Taiwan(1), China(1), India(1) and Brazil(1), Over 80 professors, students, research staffs, engineers from companies and organizations, participated in the workshop. They enjoyed substantial presentations and discussions from various fields for the future Nano-CMOS technology throughout the three day workshops.

Invited talks by the EDS distinguished lecturers in the workshop were as follows: (1) Recent Status on Nano CMOS and Future Direction (Prof. Hiroshi Iwai, Tokyo Inst. of Technology), (2) CMOS Scaling and Non-Silicon Opportunities (Prof. Yoshio Nishi, Stanford Univ.), (3) Nano CMOS Devices at the End and Beyond the Roadmap (Dr. Simon Deleonibus, CEA/LETI), (4) 32nm Technology Node Double-Gate SOI MOSFET using SiO2 Gate Stack (Prof. Enrico Sangiorgi, Univ. of Bologna), (5) Research Opportunities For Nanoscale CMOS (Prof. Philip Wong, Stanford Univ.), (6) Reliability Issues for High Performance 65nm and Beyond CMOS Technologies with Channel Mobility Enhancing Schemes (Prof. Steve Chung, Nat. Chiao Tung Univ.), (7) CMOS Technology-Based Spiral Inductors for RF Applications (Prof. Juin J. Liou, Univ. of Central Florida), (8) New Applications of Internal Photoemission to Determine Basic MOS System Parameters (Prof. Henryk M. Przewlocki, Inst. of Electron Technology), (9) Material and Interface Instabilities of High-k MOS Gate Dielectric Film (Prof. Hei Wong, City Univ. of Hong Kong), (10) Qvo Vadis Nano-CMOS (Dr. Thomas Skotnicki, STMicroelectronics), (11) Length, Width and Thickness Effects in SOI Transistors (Prof. Sorin Cristoloveanu, ENSERG), (12) Parasitics Effects in Multi Gate MOSFETs (Prof. V. Ramgopal Rao, IIT Bombey), (13) Accurate 3D Electro-Thermal Modeling for ESD Protection Structures to Nano Scale (Prof. Albert Wang, Illinois Inst. of Technology).

The following invited speakers also delivered outstanding talks; Prof. Mitsumasa Koyanagi (Tohoku Univ.), Prof. Toshiro Hiramoto (The Univ. of Tokyo), Prof. Kazuo Tsutsui (Tokyo Inst. of Technology), Prof. Hiroshi Nohira (Musashi Inst. of Technology), Prof. Kenji Kimura (Kyoto Univ.), Prof. Nobuo Tanaka (Nagoya Univ.), Dr. Junichi Tonotani (Toshiba Corp.), Dr. Tohru Mogami (NEC Corp.), Dr. Yasuo Nara (SELETE), Dr. Aya Seike (Waseda Univ.), Dr. Bunji Mizuno (UJT Lab), Prof. Gerry Lucovsky (North Carolina State Univ.), Dr. Kenji Ohmori (Nat. Inst. for Materials Science), Prof. John Robertson (Univ. of Cambridge), Prof. Kenji Shiraishi (Tsukuba Univ.), Dr. Naoto Umezawa (Nat. Inst. for Materials Science), Prof. Akitomo Tachibana (Kyoto Univ.), Prof. Jun Nakamura (Univ. of Electro-Communications), Prof. Kenji Natori (Tsukuba Univ.), Prof. Jose Camargo da Costa (Univ. de Brasilia), and Prof. Tejas Krishnamohan (Stanford Univ.).

The proceedings of the IWNC will be published in August, 2006.

ED Japan

- by Atsushi Kurobe

The officers of the ED Japan Chapter retired upon termination of their 2 year term at the end of 2005. For 2006-2007 the chapter has a new Chair and staff. They are Dr. Atsushi Kurobe (Toshiba Corp.), Chair; Prof. Mitsumasa Koyanagi (Tohoku Univ.), Vice-Chair; Dr. Hisayo S. Momose (Toshiba Corp.), Secretary; and Prof. Tetsu Tanaka, (Tohoku Univ.), Treasurer. We would like to thank the former executive officers for their great contri-

Participants of International Workshop on Nano CMOS (IWNC) held in Mishima, Japan, on Jan. 30 to Feb. 1, 2006.

The committee meeting of the ED Japan Chapter this January. From the left in the front row: Prof. Hiroshi Iwai, Partner and EDS Jr. Past President; Prof. Hiroshi Ishiwara, ex-Chair; Dr. Atsushi Kurobe, new Chair; and Prof. Yasuo Ikawa, ex-Vice Chair

bution to the ED Japan Chapter.

On January 12th, the annual meeting of the ED Japan Chapter was held in Tokyo. The new executive officers were introduced to the members. The 2005 activities and the 2006 plan of the Chapter were approved. At the meeting, the 2005 ED Japan Chapter Student Award was given to five students for their outstanding activities in the research of electron devices last year. They are Yusaku Kato (Univ. of Tokyo), Takafumi Kamimura (Osaka Univ.), Rihito Kuroda (Tohoku Univ.), Gen Tsutsui (Univ. of Tokyo) and Masaru Yamamura (Osaka Univ.). They received the metallic certificate plaques and premiums from Prof. Hiroshi Ishiwara (Tokyo Institute of Technology), the 2004-2005 Chapter Chair.

Following the annual meeting on the same day, the Briefing Session regarding the 2005 IEDM was held. Five speakers gave summary talks on the highlights of the IEDM. This session has gained widespread popularity among engineers in Japan who did not have a chance to attend the last IEDM in order to get the most advanced information on electron device technology. The session, with 80 participants, was very successful.

In addition, at the end of January, the International Workshop on Nano CMOS was held in Mishima, Japan, by the IEEE ED Japan Chapter. The successful workshop is reported apart in this issue by Prof. Kazuo Tsutsui, Chair of the Program Committee of the Workshop and the former Secretary of the ED Japan Chapter.

ED Kansai

- by Michinori Nishihara

The ED Kansai Chapter held a Technical Meeting at Osaka University, Nakanoshima Center, Osaka, Japan, on January 11, 2006. Three prestigious lecturers gave presentations on device technology trends reviewing papers presented at the 2005 International Electron Devices Meeting. The first talk on the latest Nonvolatile and other memory technology trend and Reliability was delivered by Dr. Eiichi Murakami (Renesas Technology Corporation). He described various aspects in most advanced nonvolatile memory technology which is very active and competitive thanks to portable digital audio boom in the market. He identified MONOS or SONOS structure would be a promising candidate as future nonvolatile technology. The second talk on gatestack technology was given by Dr. Masao Inoue (Renesas Technology Corporation). He covered overall technology trends of gatestack including FUSI and High-k, as well as threshold voltage adjustment technique. The last speaker was Prof. Masaaki Kuzuhara from the University of Fukui. He reviewed compound semiconductor technology concerning GaN and related materials. He also talked about the possibility of compound semiconductor as post-CMOS technology. Dr. Takashi Kuroi (Renesas Technology Corporation), chaired the meeting and the 19 participants included students and researchers from industries.

~ Kazuo Tsutsui, Editor

ED Taipei

- by Steve Chung

The ED Taipei Chapter organized two events in the first quarter of 2006. On January 4th, an invited

On January 4, 2006, Prof. T. Ohmi was invited to deliver a distinguished talk at the ED Taipei Chapter

Prof. S. L. Chuang (right) gave a DL talk on March 21, 2006, in Hsinchu. He is pictured with Prof. Steve Chung (left), the Chair of the ED Taipei Chapter

talk entitled "New Paradigm of Semiconductor Industry- Radical Reaction Based Manufacturing for System LSI " was given by Prof. Tadahiro Ohmi, Tohuku University, Japan. In this talk, Prof. Ohmi delivered subjects on: (1) the new plasma process equipment, (2) radical growth of high-quality ultra-thin nitride technologies for next generation CMOS, (3) damage free process, and (4) a target to reduce the manufacturing cost for high speed logic and mixed-mode CMOS technologies. This talk was attended by 160 participants including engineers from the Science Park and graduate students from universities. On March 21st , Prof. S.L. Chuang of the University of Illinois gave a DL talk on "Slow Light Using Semiconductor Quantum Devices." More than 50 graduate students and 10 professors attended the talk.

Meanwhile, the Chapter co-sponsored the International Symposium on VLSI Technology, Systems, and Applications (VLSI-TSA) April 24-26, in Ambassador Hotel near Science-Based Industrial Park, Hsinchu. VLSI-TSA is an IEEE EDS sponsored international conference. The Conference includes two-and-half day paper presentations and two half-day short courses on Memory and Advanced CMOS Manufacturing. Interested parties may visit the conference website at http://vlsitsa.itri.org.tw/2006. The Conference participants may also take this opportunity to visit the world's most dense semiconductor manufacturing and IC design community, Hsinchu Science-Based Industrial Park.

~ Hei Wong, Editor

ED/SSC Bangalore

- by P. R. Suresh

The following events occurred during the first quarter of 2006:

The technical events organized by the chapter continue to gain popularity with a significant increase in the number of attendees. The average attendance for the events was about 60, with a peak attendance of 80 at one event. The following is a brief description of the events conducted by the joint chapter for the first quarter of this year.

The first event was a seminar by Dr. Nagaraj NS, Texas Instruments, Dallas, on 10 January and the topic was "Interconnect Scaling Trends and Impact on SoC Designs". In his talk, Dr. Nagaraj reviewed fresh perspective on the impact of interconnect technology scaling on SOC designs covering scaling trends and new challenges in sub-50nm regime, electron scattering effects and its impact on resistance, the impact of intra-cell RC parameters on circuit performance and sources of interconnect process variations and potential solutions. About 55 people from both industry and academia attended this seminar and it received positive comments from the audience.

A seminar on "Parasitic Extraction - First Principle Methods" was given by Dr. Shabeer Batterywalla, Advanced Technology Group, Synopsys, Bangalore, on February 24th . Dr. Shabeer talked about fundamental techniques which can be used to compute on-chip interconnect parasitics accurately. Resistance, capacitance and inductance extraction problems were discussed with commonly used solution techniques. A brief overview of how the extraction problem is solved in industry was also discussed. Also, the issues facing the extraction problem with modern processes were highlighted. This talk was attended by about 70 people.

Dr. Linton Salmon, Vice President and Director, Texas Instruments, Dallas, gave a talk on Challenges for Silicon Technology at 45nm and Beyond", on March 23rd and he addressed some of the major challenges facing the industry as we scale integrated circuit dimensions to the 45nm node. Lithography, materials and architecture approaches to meet these challenges were also discussed. About 80 people attended.

AP/ED Bombay

- by Mahesh Patil

The following events occurred during the first quarter of 2006.

On January 16, Dr. Rajiv V. Joshi, Research staff member at IBM, T.J. Watson Research Center, Yorktown Heights, New York, USA, gave a talk on "Impact of technology on sub 90 nm VLSI circuits".

On January 28, Dr. Vijay Singh, Homi Bhabha Centre for Science Education, Mumbai, India, gave a talk on "Scaling Laws for Semiconductor Nanostructures".

Dr. Krishna K. Bhuwalka, Universität der Bundeswehr, Munich, Germany, gave a talk on "Novel Tunneling Devices for Future CMOS Technologies", on February 10, 2006.

ED Calcutta

- by Chandan Sarkar

Two IEEE distinguished lectures were held on January 3, 2006 at Meghnad Saha Auditorium, University of Calcutta. It was jointly organized by the EDS and LEOS chapters of the IEEE Calcutta Section. The distinguished lectures were delivered by Prof. Hiroshi Iwai from the Tokyo Institute of Technology, Japan, and Prof. Bishnu Pal from the Indian Institute of Technology, Delhi, India. The talk delivered by Prof. B. Pal was on "Photonic Bandgap Bragg Fibers: A New Platform for Realizing Application Specific Specialty Optical Fibers and Components". The topic of the talk by Prof. H. Iwai was "Future of CMOS Scaling and its Manufacturing".

Prof. Supriyo Bandyopadhyay from the Department of Electrical Engineering and Department of Physics, Virginia Commonwealth University, USA, was invited to deliver an IEEE distinguished lec-

Prof. Hiroshi Iwai delivering the IEEE Distinguished Lecture

ture on January 9, 2006, at the Departmental Committee Room of the Department of Electronics & Telecommunications Engineering, Jadavpur University, Calcutta. The topic of his talk was "Quantum Computing", in which he demonstrated the present scenario of quantum computation paradigms. This talk was organized by the IEEE ED Calcutta Chapter.

On January 13, 2006, the ED Calcutta Chapter organized an IEEE technical talk and the invited speaker Prof. Ashim Kumar Ray from the Department of Materials, Queen Mary College, University of London, UK, spoke on the topic "Wet Technology for Nano-Electronics".

The Calcutta IEEE Section and IEEE Electron Devices Society (EDS) Chapters of IEEE Calcutta, jointly organized an IEEE technical talk on February 7, 2006, delivered by Mr. Sagnik Dey, a graduate research assistant from the Department of Electrical and Computer Engineering, University of Texas at Austin, USA. The topic was "Novel 3-D MOSFET Architecture for sub 50nm Nodes".

Dr. Manas Kumar Ray was jointly invited by the IEEE Calcutta Section and the ED Calcutta Chapter, to deliver an IEEE technical talk on "Tunable Filter for Software – Driven Radio and Other Systems" on February 10, 2006. The venue of the talk was also at Jadavpur University, Calcutta.

ED/MTT India

- by Kandala Chari

The Chapter pursued many diverse efforts in the last 6 months. A summary of major initiatives follows:

The Chapter has co-sponsored three conferences. First, the International Componex/Electronics India 2006, held at Delhi during January 23-25, 2006. In conjunction with this meeting, the 11th International Conference cum Exhibition of Electronic Components, Materials and Production Equipment was held. More than 700 exhibitors from 22 countries participated with visitors numbering over 18,000. A second International Conference, "Challenges and Opportunities in Electronics Manufacturing" was held at the same venue January 23-34, 2006. This event featured 20 lead speakers covering various aspects of Manufacturing including global scenario, Global Market key sectors, design and development issues, challenges in manufacturing, test and inspection methods, supply chain solutions etc. Mr. S. Swaran, Editor-in-Chief of the Electronics Today Journal organized these two events. The third is a "National Workshop on VLSI Design and Embedded Systems (NEVDES) 2006" held at the Birla Institute of Technology, Pilani, February 24-26, 2006. The Workshop covered various aspects of CMOS circuit design, synthesis, digital design with Verilog HDL etc. Over 40 faculty and researchers from different institutes attended the event. This event was coordinated by Dr. (Ms.) Anu Gupta and Dr. Rajnish Sharma, faculty at BITS.

The Chapter co-sponsored e-kranti, an annual inter institute meeting of students from various IT and Management Institutes, to foster idea generation, mutual exchanges, and reward the best performances and ideas of these community. The event held at the campus of the Institute of Management Education (IME) on February 24, 2006, contained both technical and cultural items. The event included Design Mania (teams to develop on theme given on the spot), Dare To Answer (a quiz competition on IT, gadgets and applications), Dream 2020 (to showcase possible scenarios of emerging technical world in 2020), Techno Show (ramp event to show "electronic gadgetry"), Antardwand (speaker speaking both for and against the motion alternately in given time), Ad Mad Show (a mix of media, product mix, graffiti), etc. The Chapter awarded prizes for the winning teams in Dream 2020 and Techno Shows. Over 500 Students from 6 colleges attended the event. Dr. Charul Bhatnagar and Mr. Sanjay Sharma of IME coordinated the event.

BITS Workshop 2006, which was held at the Birla Institute of Technology and co-sponsored by the ED/MTT India Chapter.

A section of the audience at the e-kranti event, on the campus of the Institute of Management Education

Under the STAR effort, a team of 12 students from the KBMCGH School, Eluru, attended on February 22, 2006, a major congregation held at the Chinanindra Kolanu venue and spoke on Women empowerment matters, highlighting the importance of scientific knowledge for women, essentiality of science in daily life, use of science for women development, women employment and the role of science in keeping world peace. The interaction is a new initiative to help bridge the digital divide in society. Over 800 attendees graced these interactions. STAR students later visited the village fish ponds and witnessed the traditional methods of fish culture. Mr. R. Bhhaskara Naidu, Head Master, and faculty Ms. B. Subbalakshmi, coordinated the trip to the village and interactions.

The Chapter Chair visited MS Ramaiah School of Advanced Studies, Bangalore, on February 25, 2006, and addressed the faculty on the issues of Intellectual Property Evaluation, Chip design protection and Infringements. The Dean of R&D, and over 25 faculty and staff, attended the meeting. Dr. Shankapal, the Director of the school and R. Prakash, Asst. Professor, Embedded Systems Group, coordinated the meeting.

Dr. Young Yu, President SELCO, Korea/MYCAD Inc, USA, visited the Chapter March 21-23, 2006. Chapter members are requested to update the Chair on their e-mails, offer any suggestions and also vol-

unteer for activities in their areas to enable the chapter to expand its reach further.

ED Malaysia

- by Badariah Bais & Burhanuddin Yeop Majlis

The 2005 IEEE National Symposium on Microelectronics (NSM 2005) was held at Kuching Hilton, Sarawak, Malaysia, November 22-24, 2005. This is the fifth symposium organized by the Electron Devices Chapter of the IEEE Malaysia Section. The symposium was officiated by YB Dato Patinggi Tan Sri Dr. George Chan Nong Ham, Deputy Chief Minister of Sarawak. In this symposium, more than 100 papers were received but only 90 papers were selected to be published in the proceedings. The main scope of the symposium covers all aspects of the semiconductor technology from materials issues and device fabrication, MEMS technology, IC design and testing, reliability and failure analysis, manufacturing and system applications.

The first keynote invited paper titled "Challenges in Nanoscale Devices and Breakthrough" was presented by Prof. Dr. Jong Duk Lee from Seoul National University, Korea who is also an adjunct professor at the Institute of Microengineering and Nanoelectronics (IMEN) in Malaysia. The second keynote paper titled "Second-Tier Foundries: Options for Competitiveness" was presented by Dr. John Nelson, CEO of 1st Silicon (Malaysia) Sdn. Bhd. in Sarawak, Malaysia. There were about 90 participants from Malaysia and Singapore who attended the 2-day symposium.

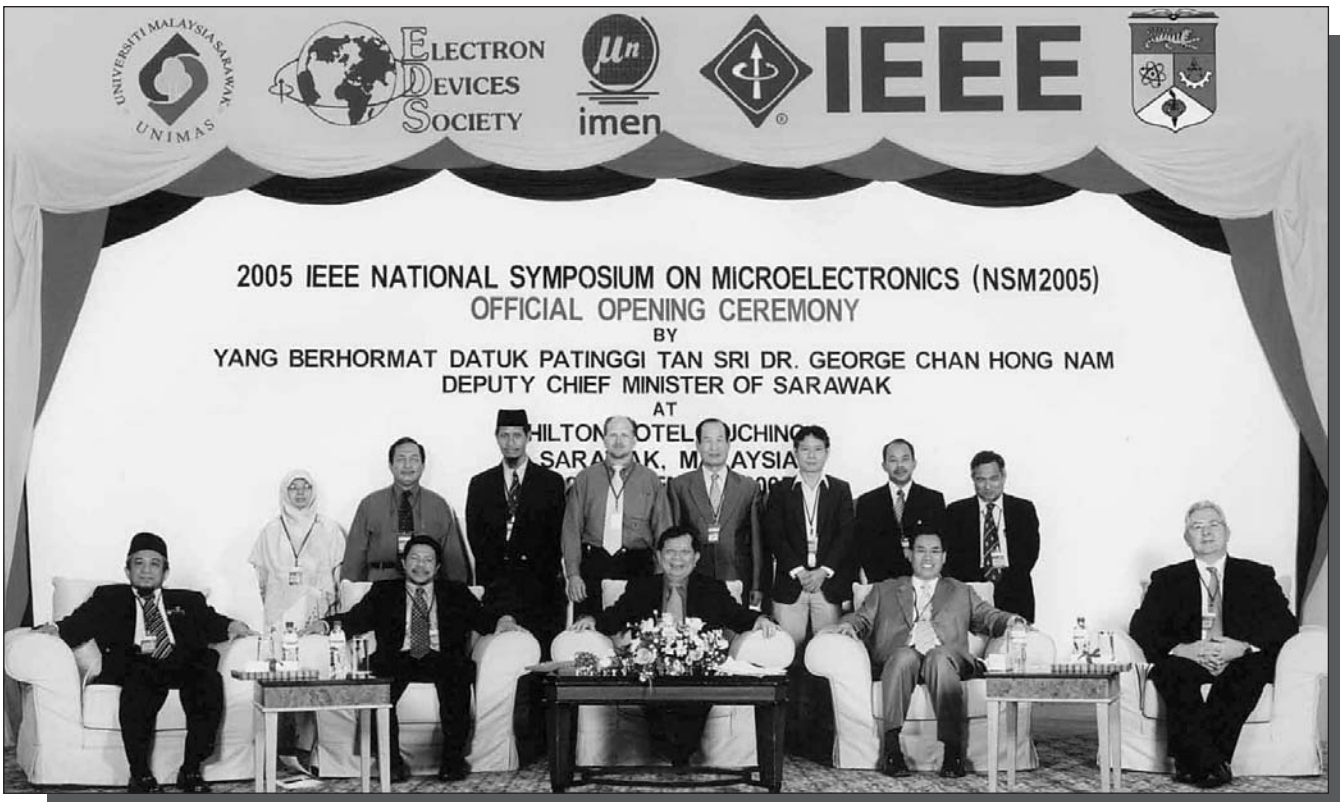
In conjuction with the symposium, two tutorials were held on November 21, 2005. The tutorials were given by Mr. Richard Keating from CMOS Training and Consulting, Penang, Malaysia, on Advanced Silicon Wafer Fabrication Process and by Mr. Max Lim Seong Chew, Staff Design Engineer in Integrated Circuit Design Services (M) Sdn. Bhd. on CMOS layout fundamental and ASIC physical design. About 30 participants attended the tutorials.The main sponsors of the symposium were 1st Silicon (Malaysia) Sdn. Bhd. and Silterra (M) Sdn. Bhd., with cooperation from the Institute of Microengineering and Nanoelectronics (IMEN) of Universiti Kebangsaan Malaysia and Universiti Malaysia Sarawak.

REL/CPMT/ED Singapore

- by Wilson Tan

During the first quarter of 2006, the Chapter had the following activities:

1. Distinguished Lectures
   - On January 9, 2006, Prof. Edmund Seebauer, Department of Chemical & Biomolecular Engineering, University of Illinois at Urbana-Champaign, gave a DL talk on "New Methods for Defect Engineering in Semiconductors".
   - On the same day, Prof. Vijay K. Arora, Wilkes University, also gave a DL talk on "Failure of Ohm's Law: Its Implications on Circuit Design".



Opening Ceremony of NSM2005. Sitting (left to right): Assoc. Prof. Dr. Norman Mariun (IEEE Malaysia Section Chair), Prof. Dr. Burhanuddin Yeop Majlis (ED Chapter Chair/Conference Chair), YB Dato Patinggi Tan Sri Dr. George Chan Nong Ham (Deputy Chief Minister of Sarawak), Assoc. Prof. Dr. Awangku Abdul Rahman and Dr. John Nelson (keynote speaker). Standing (left to right): Dr. Roslina Mohd Sidek, Prof. Dr. Sahbudin Shaari, Assoc. Prof. Ibrahim Ahmad, Richard Keating, Prof. Dr. Jong Duk Lee (keynote speaker), Prof. Dr. Tou Teck Yong, Rahman Wagiran and Prof. Dr. Muhamad Mat Salleh.

2. Workshop on Silicon-based Technologies

Jointly organized by Pall Filtration Private Limited & Microelectronics Center, School of EEE, Nanyang Technological University (NTU) and the Chapter, a workshop on "Technology of Silicon-based Nanodevices" was successfully held on February 24, 2006, in NTU. Pall Filtration financially funded the workshop. Four overseas speakers and six local speakers presented talks on topics ranging from new filtration technologies on defectivity reduction to advanced sub-30nm transistor technologies

The workshop attracted more than 180 participants from the industry, research institutions and universities. The Chapter plans to organize similar workshops annually.

3. Conferences

IPFA 2006

Preparations are well underway for the 13th IPFA which will be held July 3-7, in the Meritus Mandarin Hotel, in the heart of Singapore's central business district.

At the time of writing, the abstract review process has just been completed and authors have been informed of the results. Of the approximately 100 hundred abstracts submitted, 44 papers have been accepted for oral presentation and 25 for the poster session. This year, for the first time, paper submission and registration will be via a web-based on-line procedure. The Keynote Speaker will be Prof Hiroshi Iwai from the Tokyo Institute of Technology.

In a paper exchange arrangement, the best papers from ESREF 2005 and ISTFA 2005 will be presented at IPFA 2006, while the best papers in reliability and failure analysis from IPFA 2006 will be presented at the corresponding ESREF & ISTFA conferences.

In conjunction with the three day technical symposium, two days of tutorials will be held on the July 3-4, 2006.

The exhibition will be held in parallel with the symposium between July 5-7 and is expected to draw just under 30 companies.

The 11th WIMNACT-Singapore has been planned on 4 July and will be co-located with IPFA, with cross publicity for both events. Five invited Distinguished Lecturers from overseas will participate in the event.

EPTC 2006

The 8th Electronics Packaging Technology Conference (EPTC 2006), an International event organized by the IEEE Reliability/CPMT/ED Singapore Chapter, sponsored by IEEE CPMT Society with technical sponsorship from IMAPS, will be held from December 6-8, 2006, at the Pan Pacific Hotel, Singapore. The 1st call for papers has been announced recently.

4. Others

- The Chapter donated a book prize of US $2,500 to the School of Materials Science & Engineering, NTU. This book prize entitled "IEEE Singapore Reliability/CPMT/ED Chapter Book Prize" is awarded to the student who has distinguished himself/herself in the Microelectronics related subjects, offered in the third and final year of the Engineering (Materials Science & Engineering) course of next 5 years, commencing in 2006.
- The Chapter also donated a Subject Prize of US $1,500 to the Temasek Polytechnic Engineering School. This award is entitled the "Subject Prize" for the student who graduates with a Diploma with Merit in the Diploma in Microelectronics course of next 5 academic years, commencing in 2006.

ED SJCE Student Branch

- by Karthik Y

"When the going gets tough, the tough gets going!" being the motive of the IEEE ED student chapter, has proved to be very true during the academic year 2005-06.

Working successfully on the fast track, the chapter has organized a series of events with the steering from Dr. Navakanta Bhat, Prof. IISc, Bangalore, and Dr. C.R. Venugopal, Prof. Dept. of Electronics and Communication, SJCE, Mysore.

The blinds were unfurled on November 15, 2005, by "Paper Panacea", an activity which imparted an idea to the students, by means of demonstrations, regarding technical paper presentations, their format and the way of presentation.

A state level "Hardware Design Contest" was conducted on November 19, 2005, presided over by Dr. Navakanta Bhat, Prof. IISc, Bangalore. The inaugural of the event was followed by his talk on "Giga Scale Integration Using Nanoscale Building Blocks", which touched upon the basic fabrication of devices and designing of integrated chips.

The contest then played along with over 150 participants and two arduous rounds of written and practical designs.

To keep up the momentum, weekly tests and quizzes are conducted on Basic Electronics to refresh and review the basic designing skills of the students and generate some hands on practical exposure.

As a part of the activities during "CYBERIA 2006", a national level technical fest conducted by the IEEE SJCE Student Branch, the ED Student Chapter has planned to coordinate two events:

- "X86", an assembly level programming contest, on April 1-2, 2006, and
- "Impedance", a hardware design contest based on basic analog and digital electronics, on April 2nd.

These being the activities so far, this subchapter aims to channel a gamut of events for this academic year and broaden the motley with new ideas.

~ Xing Zhou, Editor

A well-attended ED SJCE Student Branch event

EDS MEETINGS CALENDAR

(As of May 18, 2006)

The complete EDS Calendar can be found at our web site:
http://www.ieee.org/society/eds/meetings/meetings_calendar.xml Please visit!

July 1 - 5, 2006, T **Siberian Russian Workshop and Tutorial on Electron Devices and Materials**, Location: Novosibirsk State Technical University, Novosibirsk, Russia, Contact: Alexander Gridchin, E-Mail: ieeensk@yandex.ru, Deadline: Not Available, www: Not Available

July 3 - 7, 2006, T **IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits**, Location: Meritus Mandarin, Singapore, Contact: Jasmine Leong, E-Mail: ipfa@pacific.net.sg, Deadline: 2/3/06, www: http://www.ieee.org/ipfa

July 3 - 7, 2006, T **International Conference on Nanoscience and Nanotechnology**, Location: Brisbane Convention and Exhibition Centre, Brisbane, Australia, Contact: Chennupati Jagadish, E-Mail: chennupati.jagadish@anu.edu.au, Deadline: 3/20/06, www: http://www.ausnano.net/iconn2006/

July 16 - 20, 2006, T **IEEE Conference on Nanotechnology**, Location: Westin Cincinnati, Cincinnati, OH, USA, Contact: Clifford Lau, E-Mail: lauc@onr.navy.mil, Deadline: 2/28/06, www: http://ewh.ieee.org/tc/nanotech/

July 17 - 20, 2006, @ **International Vacuum Nanoelectronics Conference**, Location: Guilin Waterfall Hotel, Guilin, China, Contact: Biyun Chen, E-Mail: stdp13@zsu.edu.cn, Deadline: 4/1/06, www: http://ivnc-ifes-06.net

August 2 - 4, 2006, T **Lester Eastman Biennial Conference on High Performance Devices**, Location: Cornell University, Ithaca, NY, USA, Contact: Michael Spencer, E-Mail: spencer@ece.cornell, Deadline: 5/1/06, www: http://lec.iiiv.cornell.edu/lec2006/call.htm

August 13 - 17, 2006, T **IEEE International Symposium on Compound Semiconductors**, Location: University of British Columbia, Vancouver, Canada, Contact: Tom Tiedje, E-Mail: ttiedje@phas.ubc.ca, Deadline: 6/3/06, www: www.iscs2006.ca

August 28 - September 1, 2006, T **Symposium on Microelectronics Technology & Devices**, Location: Ouro Preto, Brazil, Contact: Jacobus Swart, E-Mail: jacobus@led.unicamp.br, Deadline: 3/5/06, www: www.lecom.dcc.ufmg.br/sbcci/en/sbmicro.php

September 6 - 8, 2006, @ **IEEE International Conference on Simulation of Semiconductor Processes and Devices**, Location: Monterey Plaza Hotel, Monterey, CA, USA, Contact: Fely Barrera, E-Mail: sispad06@gloworm.stanford.edu, Deadline: 2/24/06, www: www-tcad.stanford.edu/sispad06

September 6 - 8, 2006, T **International Conference on Electrical and Electronics Engineering**, Location: Veracruz, Mexico, Contact: Judith Esparza-Azcoitia, E-Mail: iceee@cinvestav.mx, Deadline: 5/15/06, www: http://iceee.ie.cinvestav.mx

September 10 - 13, 2006, T **IEEE Custom Integrated Circuits Conference**, Location: Double Tree Hotel, San Jose, CA, USA, Contact: Melissa Widerkehr, E-Mail: melissaw@widerkehr.com, Deadline: 4/7/06, www: http://www.ieee-cicc.org

September 10 - 13, 2006, T **IEEE European Microwave Integrated Circuits Conference**, Location: G-Mex/MICC Exhibition & Int'l Conference Centre, Manchester, United Kingdom, Contact: Andy Dearn, E-Mail: AWD@plextek.co.uk, Deadline: 2/17/06, www: www.eumw2006.com

September 11 - 15, 2006, T **International Crimean Microwave Conference "Microwave & Telecommunication Technology"**, Location: Sevastopol National Technical University, Sevastopol, Ukraine, Contact: Sergey Smolskiy, E-Mail: smolskiysm@mail.ru, Deadline: 5/11/06, www: http://ieee.orbita.ru/aps/crim06e.htm

September 12 - 15, 2006, T **International Conference on Solid-State Devices and Materials**, Location: Pacifico Yokohama, Yokohama, Japan, Contact: SSDM Conference Secretariat, E-Mail: ssdm@intergroup.co.jp, Deadline: 5/10/06, www: http://www.ssdm.jp

September 14 - 16, 2006, T **International Conference on Nano-Networks**, Location: Ecole Polytechnique Federale de Lausanne, Lausanne, Switzerland, Contact: Gian Mario Maggio, E-Mail: maggio@ieee.org, Deadline: 6/1/06, www: http://www.nanonets.org

September 17 - 20, 2006, T **IEEE Conference on Intelligent Transportation Systems**, Location: Toronto Marriott Downtown Eaton Centre, Toronto, Canada, Contact: Baher Abdulhai, E-Mail: baher.abdulhai@utoronto.ca, Deadline: 3/1/06, www: www.itsc2006.org

September 18 - 22, 2006, T **European Solid-State Device Research Conference**, Location: Montreux Convention Center, Montreux, Switzerland, Contact: Yusuf Leblebici, E-Mail: yusuf.leblebici@epfl.ch, Deadline: 4/7/06, www: http://www.essderc2006.com

September 20 - 21, 2006, T **International Conference on Actual Problems of Electron Device Engineering**, Location: Saratov State Technical University, Saratov, Russia, Contact: Alexei Miroshnichenko, E-Mail: alexm@sstu.ru, Deadline: Not Available, www: http://www.sstu.ru/sstu/win/konf/apede2005.html

September 25 - 27, 2006, T **World Thermophotovoltaic Generation of Electricity Conference**, Location: EUROFORUM Infantes, San Lorenzo del Escorial, Madrid, Spain, Contact: Victoria Corregidor, E-Mail: vicky.corregidor@ies-def.upm.es, Deadline: 5/15/06, www: http://www.ies.upm.es/TPV7/index.html

September 26 - 28, 2006, T **International Conference on Actual Problems of Electronic Instrument Engineering**, Location: Novosibirsk State Technical University, Novosibirsk, Russia, Contact: Alexander Gridchin, E-Mail: ieeensk@yandex.ru, Deadline: Not Available, www: http://sstu.ru/sstu/win/konf/apede

September 27 - 29, 2006, T **International Symposium on Advanced Gate Stack Technology**, Location: Omni Hotel, Austin, TX, USA, Contact: Hsing Tseng, E-Mail: hsinghuang.tseng@sematech.org, Deadline: 7/31/06, www: Not Available

September 27 - 29, 2006, * **International Semiconductor Conference**, Location: Sinaia Hotel, Sinaia, Romania, Contact: Dan Dascalu, E-

Mail: dascalu@imt.ro, Deadline: 5/28/06, www: www.imt.ro/CAS

October 1 - 4, 2006, T **IEEE International Conference on Computer Design**, Location: Doubletree Hotel, San Jose, CA, USA, Contact: Pranav Ashar, E-Mail: ashar@realintent.com, Deadline: 5/6/06, www: http://www.iccd-conference.org

October 2 - 5, 2006, * **IEEE International SOI Conference**, Location: Holiday Inn Select Niagara Falls, Niagara Falls, NY, USA, Contact: Bobbi Armbruster, E-Mail: bobbi@bacminc.com, Deadline: 5/5/06, www: www.soiconference.org

October 3 - 6, 2006, T **European Symposium on Reliability of Electron Devices, Failure Physics and Analysis**, Location: Historische Stadthalle Wuppertal, Wuppertal, Germany, Contact: Mechthild Knippschild, E-Mail: knippsch@uni-wuppertal.de, Deadline: 3/31/06, www: www.esref.org

October 4 - 6, 2006, T **International Symposium on Low-Power Electronics and Design**, Location: Rothach-Egern Conference Center, Tegernsee, Germany, Contact: Mircea Stan, E-Mail: mircea@virginia.edu, Deadline: 3/3/06, www: http://www.islped.org

October 8 - 10, 2006, @ **Bipolar/BiCMOS Circuits and Technology Meeting**, Location: Maastricht Exposition and Congress Centre, Maastricht, The Netherlands, Contact: John Long, E-Mail: j.r.long@ewi.tudelft.nl, Deadline: 3/12/06, www: www.ieee-bctm.org

October 10 - 13, 2006, T **International Conference on Advanced Thermal Processing of Semiconductors**, Location: Kyoto Brighton Hotel, Kyoto, Japan, Contact: Bo Lojek, E-Mail: blojek@atmel.com, Deadline: 5/31/06, www: www.ieee-rtp.org

October 12 - 13, 2006, T **IEEE International Seminar/Workshop on Direct and Inverse Problems of Electromagnetic and Acoustic Wave Theory**, Location: Tbilisi State University, Tbilisi, Ukraine, Contact: Mykhalyo Andriychuk, E-Mail: andr@iapmm.lviv.ua, Deadline: 7/1/06, www: http://www.ewh.ieee.org/soc/cpmt/ukraine/

October 15 - 19, 2006, T **International Advanced Research Workshop**, Location: Big Yalta, Crimea, Ukraine, Contact: Yuri Houk, E-Mail: houk@lab15.kiev.ua, Deadline: 7/15/06, www: http://www.liv.ac.uk/eee/SOIWorkshop/SOIWorkshop.htm

October 16 - 18, 2006, T **International Conference on Advanced Semiconductor Devices and Microsystems**, Location: The Castle of Smolenice, Bratislava, Slovak Republic, Contact: Erik Vavrinsky, E-Mail: erik.vavrinsky@stuba.sk, Deadline: 5/15/06, www: http://www.kme.elf.stuba.sk/asdam/index.php

October 16 - 19, 2006, * IEEE **International Integrated Reliability Workshop**, Location: Stanford Sierra Conference Centers, South Lake Tahoe, CA, USA, Contact: Roy and Becky Walker, E-Mail: roy@sar101.com, Deadline: 7/12/06, www: www.iirw.org

October 18 - 20, 2006, T **International Forum on Strategic Technology**, Location: Lotte Hotel, Ulsan, Korea, Contact: Ui Pil Chong, E-Mail: upchong@ulsan.ac.kr, Deadline: 6/15/06, www: http://ifost.ulsan.ac.kr

October 22 - 25, 2006, T **IEEE International Conference on Sensors**, Location: Daegu Exhibition & Convention Center, Daegu, Korea, Contact: Sukhan Lee, E-Mail: lsh@ece.skku.ac.kr, Deadline: 5/1/06, www: www.ieee-sensors2006.org

October 23 - 26, 2006, T **International Conference on Solid-State & Integrated Circuits Technology**, Location: Hotel Equator Shanghai, Shanghai, China, Contact: Mengqi Zhou, E-Mail: mqzhou@public3.bta.net.cn, Deadline: 7/15/06, www: http://www.ICSICT2006.com

November 5 - 8, 2006, T **Non-Volatile Memory Technology Symposium**, Location: San Mateo Marriott, at San Francisco Airport, San Francisco, CA, USA, Contact: Jeffrey Peloquin, E-Mail: jpeloquin@chem.boisestate.edu, Deadline:, 6/9/06, www: http://coen.boisestate.edu/nvmts/

November 5 - 9, 2006, T **IEEE International Conference on Computer Aided Design**, Location: DoubleTree Hotel, San Jose, CA, USA, Contact: Kathy MacLennan, E-Mail: kathy@mpassociates.com, Deadline: 4/19/06, www: http://www.iccad.com/future.html

November 8 - 10, 2006, T **International Workshop on Dielectric Thin Films for Future ULSI Devices: Science and Technology**, Location: Kawasaki City Industrial Promotion Hall, Kanagawa, Japan, Contact: Takanobu Watanabe, E-Mail: watanabe-t@waseda.jp, Deadline: 7/24/06, www: http://home.hiroshima-u.ac.jp/iwdtf/

November 12 - 12, 2006, T **Reliability of Compound Semiconductors Workshop**, Location: Marriott Riverwalk Hotel, San Antonio, TX, USA, Contact: Anthony Immorlica, E-Mail: anthony.a.immorlica@baesystems.com, Deadline: Not Available, www: http://www.jedec.org/home/gaas

November 12 - 15, 2006, * **IEEE Compound Semiconductor IC Symposium**, Location: Marriott Riverwalk Hotel, San Antonio, TX, USA, Contact: Mitchell Shifrin, E-Mail: mitchs@hittite.com, Deadline: 5/15/06, www: http://www.csics.org

December 4 - 5, 2006, T **IEEE Wireless and Microwave Technology Conference**, Location: Marriott Suites Sand Key, Clearwater, FL, USA, Contact: John Conrad, E-Mail: john.conrad@ieee.org, Deadline: 6/23/06, www: http://wamicon.eng.usf.edu

December 6 - 8, 2006, T **Conference on Optoelectronic and Microelectronic Materials & Devices**, Location: The University of Western Australia, Crawley (Perth), Australia, Contact: Sabine Betts, E-Mail: commad06@ee.uwa.edu.au, Deadline: 5/31/06, www: http://commad06.ee.uwa.edu.au/

December 6 - 8, 2006, T **IEEE International Conference on Semiconductor Electronics**, Location: Hyatt Regency Kinabalu, Kota Kinabalu, Malaysia, Contact: Burhanuddin Yeop Majlis, E-Mail: burhan@vlsi.eng.ukm.my, Deadline: 8/1/06, www: http://www.eng.ukm.my/~eds/

December 7 - 9, 2006, * **IEEE Semiconductor Interface Specialists Conference**, Location: The Catamaran Resort Hotel, San Diego, CA, USA, Contact: Ben Kaczer, E-Mail: kaczer@imec.be, Deadline: Not Available, www: www.ieeesisc.org

December 11 - 13, 2006, * **IEEE International Electron Devices Meeting**, Location: San Francisco Hilton and Towers, San Francisco, CA, USA, Contact: Phyllis Mahoney, E-Mail: phyllism@widerkehr.com, Deadline: Not Available, www: www.ieee.org/conference/iedm

December 16 - 19, 2006, T **International Conference on Microelectronics**, Location: King Fahd University of Petroleum and Minerals, Dhahran, Saudi Arabia, Contact: Alaa Hussein, E-Mail: husseina@kfupm.edu.sa, Deadline: 8/1/06, www: http://icm2006.kfupm.edu.sa/

December 18 - 20, 2006, T **International Conference on Computers and Devices for Communication**, Location: SINP Convention Center, Kolkata, Kolkata, India, Contact: Animesh Maitra, E-Mail: codec2006@yahoo.com, Deadline: 5/31/06, www: http://www.irpel.org/php-files/codec-06.php

EDS All India Chapters Meeting

Standing (L-R) : C. R. Venugopal (ED Mysore SJCE), J. Behari (ED Delhi), H. P. Vyas (IEEE Delhi), P. R. Suresh (ED Bangalore), S. D. Gupta (ED Bombay), C. Sarkar (ED Calcutta); Sitting (L-R : M. K. Radhakrishnan (Chapter Partner), R. Gupta (ED Delhi), Renuka Jindal (Chapter Partner), S. A. Gangal (ED Pune)

The 3rd EDS All India Chapters Meeting – joint meeting of Chapter Chairs and representatives from the EDS Chapters in India and Chapter Partners - was held at New Delhi, December 31, 2005. Radhey Gupta of Delhi University, hosted the event on behalf of the IEEE Delhi Section at the University's South Campus. All the Chapters in India were represented at the meeting, except the ED/MT India Chapter. The status of various EDS activities by the Chapters were reviewed. It was noted that individually all the Chapters are performing well, as indicated by the Best Chapter awards received by the Bombay and India Chapters in yester years and the Bangalore Chapter in 2005.

More joint activities are planned for the coming years. These include DL mini-colloquiums, joint inter-disciplinary programs like those with biomedicals and microelectronics, instituting a best paper award for the papers published from India in the EDS journals, etc.

It was decided to extend the activities of the Calcutta Chapter to the northeastern region of India. As the electron device related activities, especially design, are booming in many cities in India, the EDS membership is also growing. A need for new Chapters to serve this growing community, in a better way, was felt. It was identified that Chennai, Hyderabad and Pune are locations where new EDS Chapters can be formed. This meeting was attended by representatives from Pune and Delhi who are interested in the formation of new Chapters. The Chapter partners will work with these groups to explore the possibilities. A common web site will be launched for all the EDS Chapters in India, to which all individual Chapters will have a web link. Also, for better communication between the Chapters, a common point of contact was instituted.

The afternoon session of the full day event had two DL talks – Renuka Jindal on "From Millibits to Terabits and Beyond – Over 50 Years of Innovation" and M. K. Radhakrishnan on "Limitations and Challenges in Gate Structures as MOSFET Shrinks to sub-100nm Regime". More than 30 participants – EDS members from Delhi and students – attended the DLs.

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