IEEE
ELECTRON DEVICES SOCIETY
Newsletter

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2007 IEEE INTERNATIONAL SOI CONFERENCE

The premier conference dedicated to current trends in Silicon-on-Insulator technology will be held October 1–4, 2007 at the luxurious Miramonte Resort & Spa in Indian Wells, California. The conference will be preceded by a one-day tutorial Short Course on Monday, October 1, and will introduce a new half-day educational class focusing on the fundamentals of SOI technology.

The conference was established with the support of IEEE to provide a forum for open discussion in all areas of silicon-on-insulator technologies and their applications. Ever increasing demand and advances in this technology make it essential to meet to discuss new gains and accomplishments, as well as to consider the new developments introduced in original papers

Miramonte Resort & Spa, Indian Wells, California

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YOUR COMMENTS SOLICITED

Your comments are most welcome. Please write directly to the Editor-in-Chief of the Newsletter at nstojadinovic@elfak.ni.ac.yu

ELECTRON DEVICES SOCIETY

EDS AdCom
Elected Members-at-Large

Elected for a three-year term (maximum two terms) with 'full' voting privileges

2007	Term	2008	Term	2009	Term
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		S. Tyagi	(1)		

NEWSLETTER EDITORIAL STAFF

CONTRIBUTIONS WELCOME

Readers are encouraged to submit news items concerning the Society and its members. Please send your ideas/articles directly to either the Editor-in-Chief or appropriate Editor. The e-mail addresses of these individuals are listed on this page. Whenever possible, e-mail is the preferred form of submission.

Newsletter Deadlines

Issue	Due Date
January	October 1st
April	January 1st
July	April 1st
October	July 1st

The EDS Newsletter archive can be found on the Society web site at https://www.ieee.org/portal/pages/society/eds/pubs/newsletters/newsletter.html. The archive contains issues from July 1994 to the present.

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EDS President's Message

Ilesanmi Adesida

How time flies! It has been a year that I expressed here on this page the special honor of serving as the President of our great Society, the IEEE Electron Devices Society. The Presidents of our Society serve two-year terms and mine will be ending at the end of this calendar year. Although, the term will be ending, my service to the Society will not. I still have duties as Past-President for the next many years which I will joyfully fulfill in order to make our Society stronger and more vibrant for our time and for the future. I call upon all members to strive for service and to contribute to the well-being of our Society.

As we have ascertained in the past and continue to stress, the information revolution that we are witnessing is the product of the science and technologies that emanated from our members; and we can say that the world is better off due to the fruits of our labor. This is a legacy that we must not only preserve, but must continue to embellish. The question is how do we do this? Membership development and the creation of new chapters to accommodate and serve our members are critical elements in this quest. Membership affliations with societies in the IEEE have declined to some extent; and we have not been left out of that trend. Whereas, the decline for our Society has been less than average, we are making efforts to reverse this trend.

Many initiatives (both old and new) are being developed and pursued to cultivate new members, develop future leaders, and to increase the value of membership. We are developing a Career Guide on CD/DVD for students at various stages of their education to consider engineering as a career. We are all aware of the lack of interest in the sciences and engineering by students all the way to grade school levels which has been cogently pointed out in the United States' National Academy of Engineering's study under the title "Rising Above the Gathering Storm: Energizing and Employing America for a Brighter Economic Future." The challenge is not limited to the United States only but actually germane across significant parts of the world. Therefore any effort that we can make in sensitizing our young ones to the dynamic nature and the impact of the sciences and engineering on all our lives is important. Our GOLD members will be intimately involved in this CD/DVD project. This is a path to developing future leaders for our Society. A GOLD Conference to be held in conjunction with the IEDM is also under development. The ideas and energies of our GOLD members are cardinal to developing strategies for engaging students as new members.

Our globalization strategy is being strongly continued. It has become a tradition of the Society to hold the mid-year executive and administrative committee meetings at sites outside of the United States. Last year, it was held in Naples (Italy), and this year, it was held in Beijing, China. In both cases, regional chapters meetings were also held. Membership is growing in Region 10 which reflects intense activities in semiconductor manufacturing in the region. Our Vice President for Regions/Chapters, Juin Liou, the Vice President for Membership, Albert Wang, and others have done a great job over the last few years in developing memberships and growing chapters in this region. There have been additions to both regular and student chapters in India, China, Korea, Australia, Taiwan, and many other countries in the region. They were all well represented at the recent meeting in Beijing. There are new developments in Region 9 (Latin America) with increasing interests in EDS. There will be a Region 9 Chapters meeting in Brazil in September this year. EDS chapter subsidies have been increased this past year to amplify activities in all these chapters, and indeed, in our chapters across the world.

EDS continues to encourage and promote its fairly unique concept of mini-colloquia, using it as a means to bring together chapter members and disseminate technical information as well as increase the value of EDS membership. For 2006, EDS held eight mini-colloquia, primarily in Region 10 (Asia & Pacific), although events were held in the US and Italy as well. Five colloquia have been held so far in 2007 with three more already scheduled for later in the year. The vitality of the mini-colloquia concept and its value to EDS continue to increase each year. It should also be mentioned that the mini-colloquia concept was an outgrowth of the EDS Distinguished Lecturer Program which continues to serve our chapters and members exceptionally well reaching all-time highs in 2006 of 152 lectures performed by 71 different lecturers.

As previously reported, EDS has been participating in the IEEE program, Expert Now, whereby one-hour educational courses and tutorials from conferences are developed and made available online at a low cost to IEEE members. There are currently about sixty courses available and twenty or so in development, with EDS serving as the sponsor and providing the technical content for seven of them. Also in the area of Education, EDS has expanded its Graduate Student Fellowship Program to now offer fellowships to students pursuing their 'Masters' degree, as well as those who are attempting to obtain their PhDs. This is the first year of the EDS Masters Student Fellowship Program. Finally in the area of Education, EDS announced its first winner of a new Education Award at the IEDM this past December. This Award was developed to recognize an IEEE/EDS member from an academic, industrial or government organization with distinguished contributions to education within the field of interest of EDS.

One new membership benefit close to being released is QuestEDS. This is a

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Upcoming Technical Meetings

2007 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)

The 2007 IEEE Bipolar/BiCMOS Circuits and Technology Meeting will be held from September 30, 2007 to Tuesday, October 2 at the Boston Marriott Long Wharf Hotel in Boston, Massachusetts (http://marriott.com/hotels/travel/boslw-boston-marriott-long-wharf).

You will want to be at this conference if you're interested in the leading edge processes, devices, and circuits used in state of the art telecommunication systems and power control systems. Bipolar and BiCMOS technologies, particularly SiGe HBT BiCMOS technologies, continue to play a key role in these systems.

Papers covering the design, performance, fabrication, testing and application of bipolar and BiCMOS integrated circuits, bipolar phenomena, and discrete bipolar devices are presented.

Boston's harbourfront district is the city's center for exploration by land and by sea. Follow the red brick cobblestones of the Freedom Trail to historic sites of the American Revolution. Pass through Christopher Columbus Park to the North End, once the gateway for newcomers to New England and now the location of spirited caffes and restaurant gems. At the Faneuil Hall Marketplace, you will find what you are looking for in the variety of shops and pubs located in a building characteristic of Boston's 18th century architecture. The conference will be held during the fall season when the autumn leaves begin to change and the city is energized by interactions between students, researchers, and innovative industry and commerce. For details on local attractions and activities and to learn more about the city, please follow this link to the city of Boston's visitor web guide: (http://www.cityofboston.gov/visitors/thingstodo.asp).

The conference starts with a one day short course, followed by two full days of contributed and invited papers, including a special session on Emerging Technologies. The BCTM Banquet will be held on Monday evening at the New England Aquarium, located at Long Wharf. Following the conference on Wednesday, there will be a workshop on compact modeling for RF/Microwave applications organized by TU Delft.

Boston Marriott Long Wharf Hotel, Boston, Massachusetts

We are fortunate to have Dr. Tak H. Ning for the keynote. Dr. Ning and his colleagues invented and developed the polysilicon-emitter self-aligned bipolar transistor, which is the basis of modern bipolar transistor technology. This is a great opportunity to come and hear Dr. Ning speak.

The short course features three renowned experts on "Bipolar IC Design Beyond Handsets and Into Millimeter Waves: Challenges and Opportunities for Power Amplifier and mm-wave Transceiver IC Design." Short course invited speakers include:

• "Bipolar-based Power Amplifier design Beyond Handsets and into MM-wave integrated circuits: Design, Modeling, Characterization, Packaging, Reliability" Larry Larson (UCSD, USA)

• "MM-wave SiGe BiCMOS circuit design for automotive application" Herbert Knapp (Infineon, Germany)

• "MM-wave SiGe BiCMOS circuit design for mm-wave application" Brian Floyd (IBM, USA)

Invited speakers include:

• "On the Feasibility of few-THz Bipolar Transistors" Mark Rodwell (UCSB, USA)

• "Device, Antenna and Packaging Technology for MM Applications" Brian Floyd, (IBM, USA)

• "Satellite radio" A Maxim (Silicon Laboratories, USA)

• "Challenges in Design of Very-High-Speed Si-Bipolar IC's Operating up to 100 Gbit/s" Michael Möller (Saarland University, Germany)

• "SOI-based devices and technologies for High Voltage ICs" Florin Udrea (Univ. Cambridge, UK)

Two days of technical paper sessions, a luncheon with guest speaker, exhibits and the evening banquet round out the program. Booths feature the latest products of interest to the bipolar community. The banquet will be held at Boston's New England Aquarium featuring the 4-story tall Giant Ocean Tank, a 200,000 gallon ocean habitat coral reef home to seaturtles, sharks, moray eels and over 50 species of tropical fish. We look forward to you joining us and connecting with your colleagues at this year's BCTM. Find full details and registration for the conference on the conference web page (http:// www.ieee-bctm.org).

See you in Boston!

Yih-Feng Chyan
2007 BCTM General Chair
Broadcom
Irvine, CA, USA

2007 IEEE International Integrated Reliability Workshop (IIRW)

The 2007 International Integrated Reliability Workshop (IIRW), sponsored by the IEEE Reliability Society and the IEEE Electron Devices Society, will be held at the Stanford Sierra Camp on the shore of Fallen Leaf Lake near South Lake Tahoe, CA from October 15-18, 2007. This workshop provides a unique forum for open and frank discussions of all areas of reliability research and technology for present and future semiconductor applications. Please visit www.iirw.org for the Call for Papers and to submit your abstract to the Technical Program Chair, Patrick Lenahan, Pennsylvania State University, (pmlesm@engr.psu.edu). The submission deadline is July 13, 2007.

The IIRW is very different from a typical technical conference. From the moment you arrive, after winding slowly back to the south shore of Fallen Leaf Lake, you realize that you are taking part in something special. Attendees stay in cabins without TVs or phones, dress is casual to rustic, affiliations are downplayed, and meals are provided at the lodge dining room, family-style. Attendees of the workshop are expected to participate actively. You feel yourself drawn into technical discussions from the start. Every aspect of this conference, from the isolated location to the format of the technical program, is designed to encourage attendees to interact.

The peaceful setting, free from the distractions and annoyances of modern life, presents a terrific opportunity to get to know your colleagues, including internationally renowned experts. This is an opportunity not usually available at other conferences. In addition to the technical presentations, participants spend their evenings at discussion groups, poster sessions, and special interest groups (SIGs), all with refreshments provided to stimulate discussions. Expanded versions of selected workshop manuscripts will be published in an Integrated Reliability Workshop Special Proceedings Issue of *IEEE Transactions in Device and Material Reliability* (TDMR), June 2008.

This year's IIRW 2007 Keynote Topic is: "Microelectronics for Space Applications - Challenges and Opportunities", presented by Sammy Kayali, Mission Assurance Manager, Jet Propulsion Laboratory.

Another advantage of attending the IIRW is the extensive Tutorial Courses, presented by world-class experts and included at no additional cost. This year's tutorial courses cover Electron Spin Resonance, Reliability in BEOL High-k, SRAM and FLASH Memory, Radiation Effects, Failure Analysis Techniques.

One unique aspect of this workshop is the opportunity for every attendee to present a poster of his or her own research. Either arrange for space when you register or bring last-minute results in your briefcase or backpack. This is a great way to share your latest results and to get world-class feedback. The open poster sessions are but one example of the opportunities for the intense interaction that sets the IIRW apart from other conferences.

Another distinction of the IIRW is the moderated Discussion Groups that are held in the evenings. This year's Discussion Group Topics include: 1) High-k Gate Dielectrics, 2) NBTI, 3) Interconnects, and 4) Product and Memory Reliability. Lively conversation and debate among participants is promised and written summaries will be included in the workshop proceedings.

The Discussion Groups are followed by the Special Interest Group meetings (SIG). The SIGs are composed of small groups of researchers and engineers with a mutual interest who often continue their conversations and collaborations even after they leave the workshop. Every attendee has the opportunity to become part of an existing SIG or suggest a new topic and start one of their own.

Additional information about the workshop is available on the IIRW website at www.iirw.org, or by contacting Yuan Chen, JPL (yuan.chen@jpl.nasa.gov), 2007 IIRW General Chair. If you want to take part, please register early as space at the Stanford Sierra Camp is limited to roughly 120 attendees.

On behalf of the 2007 International Integrated Reliability Workshop Committee, I look forward to meeting you in Lake Tahoe!

George Goffman
2007 IIRW Communications Chair
Medtronic Inc.
Tempe, AZ, USA

Stanford Sierra Camp on the shore of Fallen Leaf Lake, near South Lake Tahoe, California

2007 IEEE Compound Semiconductor IC Symposium (CSICS)

We cordially invite you to the 2007 Compound Semiconductor IC Symposium being held October 14 – 17 in beautiful Portland, Oregon. The high-performance wireless and high-speed digital communications markets are thriving due to impressive strides in new materials and devices, greater integration levels, novel circuit implementations, and ever-changing systems partitions. Over the last 29 years the Compound Semiconductor IC Symposium (CSICS – formerly named the GaAs IC Symposium) has been and continues to be the preeminent international forum in which advances in semiconductor circuit and device technology are presented, debated, and discussed. The scope of the Symposium encompasses devices and circuits in GaAs, SiGe, InP, GaN, and InSb as well as targeting the fields of RF/mm-Wave CMOS and high-speed digital CMOS to provide a truly comprehensive conference. This is the ideal forum for presentation of the latest results in high-speed digital, analog, microwave/ millimeter wave, mixed mode, and optoelectronic integrated circuits.

This year's 2007 CSIC Symposium is comprised of a full 3-day technical program, 2 short courses, a primer course, and a technology exhibition. The technical program consists of approximately 60 high quality state-of-the-art technical papers, 4 panel sessions, 2 Short Courses on "Compound Semiconductor Devices and Integrated Circuits for Millimeter Wave Imaging" and "Compound Semiconductor Power Amplifiers" and an Industry Exhibit. The Symposium will also be offering the popular annual introductory level Primer Course on "Basics of Compound Semiconductor ICs". This year the Symposium will feature approximately 15 invited papers on a wide range of important topics encompassing device engineering to circuit application using advanced compound and other related semiconductor technologies. In addition, the Symposium will continue the tradition of including important "late breaking news" papers.

View of Mt. Hood from the Hilton Portland & Executive Tower

The technology exhibition will be held on Monday and Tuesday. The exhibition will feature informative and interesting displays with corporate representatives on hand. The list of exhibitors can be found in the CSICS advance program which will be published and distributed in late June. To complement the Symposium, there are several social events which include the Sunday Evening CSICS Opening Reception, the Monday CSICS Exhibition Opening Reception, the CSICS Tuesday evening Theme Party to be held at McMenamins Pub and Breweries Crystal Ballroom, and the CSICS Exhibition Luncheon on Tuesday. The Theme Party will include entertainment and a tasting of locally produced Oregon wine and beer. A breakfast will also be served on Monday, Tuesday, and Wednesday

The 2007 IEEE CSICS will be held in Portland, Oregon in the Hilton Portland and Executive Tower located in downtown Portland. Proclaimed as North America's "Best Big City," according to Money magazine, Portland exhibits unmatched natural beauty as well as a wealth of opportunities for leisure, sports, shopping, and outdoor activities. The conference downtown location is within easy access to the vibrant Pearl District with destination restaurants, art galleries, and shopping. While you're in Portland, be sure to enjoy the scenic beauty of the Columbia River Gorge, enjoy the hike to Multnomah Falls and the drive the Historic Columbia River Highway. Other local attractions include Mt Hood, the Willamette River, the rose gardens, the Japanese garden, the Oregon Coast, and the wine country. Portland has an excellent light rail system which can be used as transportation from the Airport to the Hilton and for getting around town.

For registration and further information, please visit the CSICS website at http://www.csics.org. Further questions may be addressed to the Symposium Technical Program Chair: William Peatman, Ph: +1-908-668-5000 ext. 5842, Email: wpeatman@anadigics.com. We hope you can attend.

Dan Scherrer
2007 CSICS Publicity Chair
Northrop Grumman
Redondo Beach, CA, USA

2007 IEEE International SOI Conference

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presented at the conference. The 33rd annual IEEE International SOI Conference will begin with a half-day plenary session followed by two days of oral sessions, a poster session and a late news session. Also new this year, two Best Paper Awards will be presented at the conference; one for the best oral presentation and one for the best poster presentation.

Participants are free on Wednesday afternoon to explore the desert resort area of Palm Springs, enjoy a treatment at The Well (the Miramonte's own world famous spa), get a little work done, or just relax. An evening discussion panel session where attendees are encouraged to share their opinions and expertise on the chosen topics of discussion will round off Wednesday evening.

Also on Wednesday afternoon, the conference is introducing an optional, intermediate-level class intended for individuals from a variety of fields including circuit design, material scientists/engineering, process technology, modeling, and device design. This inaugural SOI fundamentals class will cover the basics of SOI device design and characterization and will provide attendees with a broad perspective of SOI MOSFET operation and the characterization of SOI materials and devices.

The 2007 SOI Conference seeks papers on a wide range of SOI technology including:

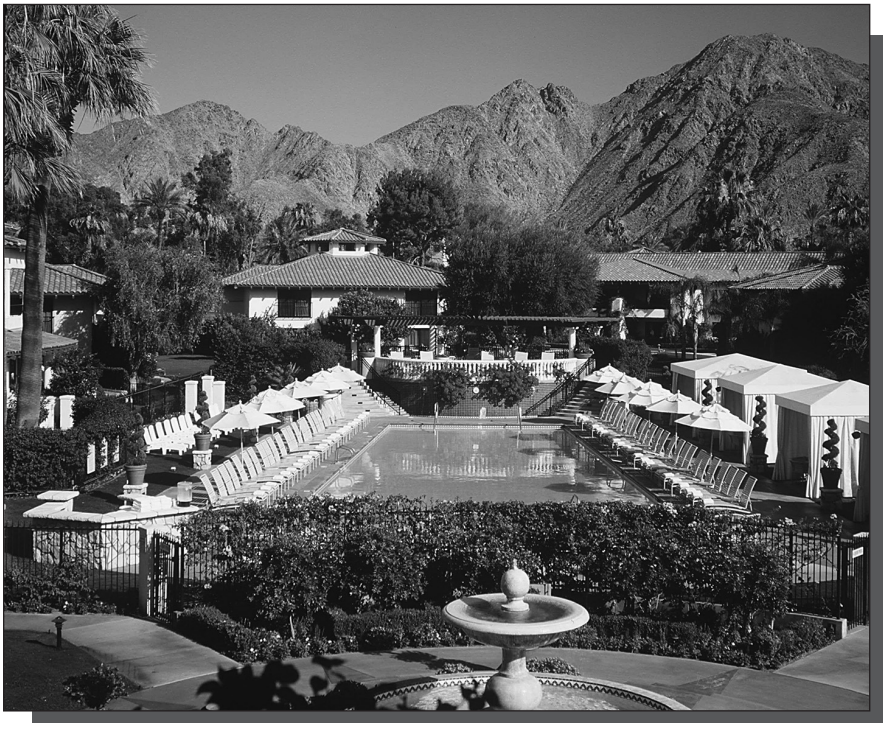
- SOI material science/modification, material characterization, manufacture and substrate engineering
- SOI device physics and modeling
- Manufacturability and process integration of SOI devices and circuits
- SOI design infrastructure
- SOI circuit applications (high-performance MPU, SRAM, ASIC, low power, high-voltage, rf, analog, mixed mode, etc.)
- Double & Multiple Gate/Vertical Channel Structures; Other Novel Structures
- New SOI structures, Circuits, and applications (3D integration, displays, microactuators - MEMS, microsensors, novel memories, optics, etc.)
- SOI reliability issues (hot-carrier effects, radiation effects, high-temperature effects, etc.)
- Engineered substrates

Abstracts for SOI 2007 Conference were due May 4, 2007. Late news papers with exceptional merit will be considered for the Late News session if submitted on or before August 20, 2007 to: conference management, by e-mail ONLY to SOIPaper@bacminc.com in PDF format.

Once again, the popular One-Day Tutorial Short Course will be offered preceding the 2007 SOI International Conference. Tutorial Short Course instructors have many years of experience in the field of silicon-on-insulator technology. The course is intended to educate attendees in detail about current trends and issues in the SOI industry. The 2007 tutorial Short Course is entitled "SOI Devices and Process Technologies" and will present a comprehensive overview of advanced SOI device and process technologies from the viewpoint of specific circuit applications including high performance, low power, rf, multigate, imagers and 3D circuits. Participants will receive copies of all visual presentations.

For registration forms and additional information, please go to the conference web site www.soiconference.org, or contact the 2007 IEEE International SOI Conference at 520 Washington Blvd., #378, Marina del Rey, CA 90292, Tel: 310-305-7885; Fax: 310-305-1038; Email: bobbi@bacminc.com.

Christophe Tretz
2007 SOI Publicity & Development Chair
IBM
San Jose, CA, USA



Miramonte Resort & Spa, Indian Wells, California

EDS President's Message

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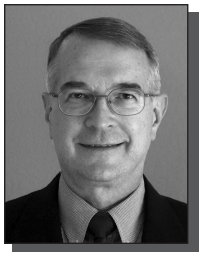
free service whereby EDS members can submit questions online in the EDS Field of Interest and EDS experts will provide the answers which will be posted online as well. The target turnaround time from the date of submission of an online request to the date of online posting of an answer will be two weeks. Another publication-related benefit to take effect this year is a free subscription to a new magazine being developed by the Nanotechnology Council, i.e., the Nanotechnology Magazine. At its December 2006 meeting, the EDS AdCom voted to provide EDS members with a free two-year subscription to the Magazine. The EDS AdCom also voted at its December 2006 meeting to join the soon-to-be-formed IEEE Technology Management Council (formerly the IEEE Engineering Management Society) as a sustaining member. We believe EDS members will find such a decision to be very useful in this day of increased entrepreneurial activities, providing them with a chance to learn and participate in the Council's activities. EDS also has a long-term initiative to add the legacy proceedings (prior to 1988) of its conferences to IEEE Xplore to further enhance the technical content available online to its members.

So you can see from the number of initiatives and activities I have mentioned that EDS has made increasing the value of membership an extremely high priority. We welcome any comments or suggestions you may have concerning our future membership strategies and offerings. My sincere thanks for maintaining your IEEE and EDS memberships and we hope to continue to bring you new and exciting benefits in the future.

Ilesanmi Adesida
EDS President
University of Illinois
Urbana, IL, USA

Society News

EDS Semiconductor Manufacturing Committee Report



Robert R. Doering

During the past two years, the IEEE EDS Semiconductor Manufacturing Technical Committee has grown from 10 to 13 members. In keeping with our goal to further diversify the membership internationally, the committee now has members from the U.S., Japan, Korea, Taiwan, Germany, and Egypt.

At the time of this writing, several of the committee members are attending the 2007 International Conference on Frontiers of Characterization and Metrology for Nanoelectronics, which is being held March 27-29, 2007, at the National Institute of Standards and Technology (NIST) in Gaithersburg, Maryland. This year, we have arranged for the conference to be technically co-sponsored by the IEEE EDS. The previous meeting of this conference was in 2005, after which the committee put together a selection of conference papers that were accepted for a special section in the November, 2006 edition of the *IEEE Transactions on Semiconductor Manufacturing* (TSM). We plan to do the same with a few outstanding papers from this year's conference.

During 2006, our committee members were active in organizing and speaking at quite a few conferences/sessions on semiconductor manufacturing, including: the International Symposium on Semiconductor Manufacturing (this will feed several special sections of the TSM), Nanotechnology in Society and Manufacturing (a special session co-sponsored by the Corporate Associates of the American Institute of Physics at the 2006 Meeting of the Amercan Vacuum Society), the 2006 SEMI NanoForum/NanoUniversity (co-sponsored with the IEEE), and the 2006 Semiconductors, Automated Manufacturing, Electronics – Training and Education Conference (SAME-TEC).

A large project for several of our committee members this year is the 2007 edition of the International Technology Roadmap for Semiconductors (ITRS). Since this is the 15th anniversary edition of the ITRS its "current year" coincides with the 15-year horizon of the inaugural 1992 NTRS, which makes for interesting comparisons! It's also the first edition for which the horizon extends beyond 2020, which has been set as a target by the Semiconductor Industry Association (SIA) for the introduction of a "beyond CMOS" logic technology. In our previous (2005) article for the EDS Newsletter, the SIA had just launched the Nanoelectronics Research Initiative (NRI) with the goal of identifying potential beyond-CMOS device concepts. Since then, several of our committee members have been active in the NRI program, which now sponsors three multi-university Nanoelectronics Centers and partners with the NSF to co-fund nanoelectronics supplements to several NSF Nanotechnology Science and Engineering Centers (NSECS) and Materials Research Science and Engineering Centers (MRSECS). Much of the work in these centers is aimed at developing new computational state variables such as spin, pseudo-spin, quantum phase, or molecular state, rather than the traditional "bulk charge." Of course, we anticipate that new directions in manufacturing, metrology, and characterization might be required to produce integrated circuits based on these device concepts, and the Semiconductor Manufacturing Technical Committee is definitely interested in helping EDS members keep up with the emerging possibilities.

Robert R. Doering
EDS Semiconductor Manufacturing Committee Chair
Texas Instruments, Inc.
Dallas, TX, USA

EDS Technology Computer Aided Design Committee Report

Enrico Sangiorgi

The EDS Technology Computer Aided Design Technical Committee (TCADTC) continues to make progress towards the goal to improve the capability of Modeling and Simulation of Process, Device, and Manufacturing for Integrated Circuits to fulfill the growing needs of the electron device community. The Committee pursues these goals by proposing special journal issues to cover important Modeling and Simulation topics, organizing panel sessions and short courses at major conferences, providing suggestions for invited speakers in the Modeling & Simulation areas at EDS sponsored international conferences.

In June 2006 the Committee launched a Call for Papers for a Special Issue of the *IEEE Transactions on Electron Devices* on "Simulation and Modeling of Nanoelectronics Devices". The aim is to present the advances in this topic to a device oriented community

represented by the readers of the *IEEE Transactions on Electron Devices*.

The contributions will address advances in physical models and modeling methodologies in the following areas: process modeling, device modeling, process equipment modeling, atomistic modeling, topics on manufacturability and variability.

The EDS TCAD Technical Committee will act as the Guest Editor for this special issue. Enrico Sangiorgi, Chairman of the Committee, will be the responsible focal point. Numerous invited and contributing papers contributions were submitted and right now the review process is in place. Scheduled publication date is September 2007.

Effective January 1, 2007, the TCAD committee has 13 members representing a very wide spectrum of technical expertise ranging from process to device to manufacturing simulation and modeling.

The present members are:

- Enrico Sangiorgi (University of Bologna, Italy) – Chair.
- Asen Asenov (Glasgow University, UK)
- Herbert S. Bennett (National Institute of Standards and Technology, Gaithersburg, MD, USA)
- Robert W. Dutton (Stanford University, Stanford, CA, USA)
- David Esseni (University of Udine, Italy)
- Martin D. Giles (Intel Corporation, Hillsboro, OR, USA)
- Masami Hane (NEC Corporation, Sagamihara, Japan)
- Christoph Jungemann (University of the Armed Forces, Munich, Germany)
- Kenji Nishi (Kinki University Technical College, Mie, Japan)
- Marcel D. Profirescu (Technical University of Bucharest, Romania)
- Siegfried Selberherr (Technical University of Vienna, Wien, Austria)
- Shinichi Takagi (The University of Tokyo, Japan)
- Paul D. Yoder (Georgia Institute of Technology, Savannah, GA)

Enrico Sangiorgi
EDS TCAD Technical Committee Chair
University of Bologna
Bologna, Italy

ANNOUNCEMENT OF NEWLY ELECTED ADCOM MEMBERS

On December 10, 2006, the EDS AdCom held its annual election of officers and members-at-large. The following are the results of the election and brief biographies of the individuals elected.

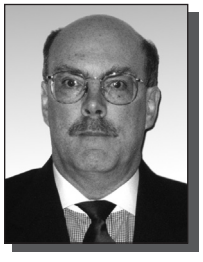
I. OFFICERS

The following individuals were elected as officers for a one-year term beginning 1/1/2007:

STEPHEN A. PARKE (Treasurer) received the BS and MS degrees in electrical engineering from Purdue University in 1984. He then joined IBM Microelectronics where he worked in device and process development for the 4Mb, 16Mb, and 64Mb DRAM designs. In 1989, he was awarded an IBM Ph.D. Fellowship, and joined the UC Berkeley Device Research group, where he studied the behavior of deep-sub-micron MOSFET and lateral bipolar transistors on thin-film SOI. In 1993, he received the Ph.D. degree and joined the IBM Semiconductor R&D Center in Fishkill, NY where he worked in the 256Mb DRAM Triad alliance between IBM, Toshiba, and Infineon. This effort accelerated the 0.25 micron process development, leading to the world's first fully-functional 256 Mb DRAM chip in 1995.

In 1996, he joined the Electrical Engineering faculty of Boise State University at the inception of its new College of Engineering. He helped lead the creation and development of the ECE Department at BSU over its first ten years. Dr. Parke has a passion for technology transfer. In Boise, he advised three start-up companies in the electronics field, and currently serves on the Board of Directors of American Semiconductor, Inc.

In 2006, Dr. Parke joined Tennessee Tech University as Professor and Chair of the TTU Electrical and Computer Engineering Dept. Dr. Parke's research is in the areas of Double-Gated Nanoscale Silicon-On-Insulator Transistors and Non-Volatile Memories. He holds ten US patents with five pending. He is the co-inventor of the DTMOS and FlexFET transistors. He has published and/or presented over 30 papers. He has served the IEEE Electron Devices Society as Graduate Student Fellowship Chair, WMED General Chair, UGIM General Chair, and currently as the Treasurer. He received the IEEE Millennium Medal in 2000 for his service. He is also a member of Tau Beta Pi and Eta Kappa Nu honorary societies.



JOHN K. LOWELL *(Secretary)* received the Ph.D. degree in Applied Physics from the University of London. He has held technical and managerial assignments for United Technologies, Northern Telecom, Mostek, Texas Instruments, British Telecom/Dupont, AMD, Applied Materials, Oracle and PDF Solutions. Presently, he is the President and Chief Consultant at Lowell Consulting in Dallas. He has also been a Professor at Texas Tech University and in the University of Texas system, and held Consulting Professorships at other universities in addition to being a Visiting Scholar at the NSF Center for the Synthesis, Growth and Characterization of Electronic Materials at the University of Texas at Austin.

Dr. Lowell is a Senior Member of the IEEE, a Distinguished Lecturer of the EDS and has held AdCom-level positions previously within the LEO and CAS societies. For fifteen years, he was also the Associate Editor-in-Chief of the IEEE Division I Circuits & Devices Magazine, and was its Guest Editor twice.

ADCOM MEMBERS-AT-LARGE

A total of seven persons were elected

to three-year terms (2007-2009) as members-at-large of the EDS AdCom. Four of the seven individuals were re-elected for a second term, while the other three were first-time electees. The backgrounds of the electees span a wide range of professional and technical interests.

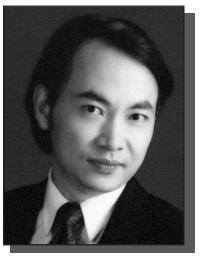
A. SECOND TERM ELECTEES:

STEVE S. CHUNG received his Ph.D. degree from the University of Illinois at Urbana-Champaign, in Electrical Engineering in 1985. Currently, he is an NCTU Chair Professor and UMC Chair Professor at the National Chiao Tung University (NCTU), where he is also a CEO of a 5Y50B Aiming for Top-University plan. He was a Visiting Scholar with Stanford University in 2001. He was also the consultant to TSMC on developing CMOS and flash memory technologies. His current research areas include CMOS devices, flash memory technology and reliability. He has published more than 150 journal and conference papers, one textbook, and holds 20 patents.

He is an IEEE Fellow, AdCom member, Distinguished Lecturer, Regions/Chapters Vice-Chair of EDS, and Editor of EDL. He has served on premiere conferences, e.g., VLSI Technology, IEDM, IRPS, etc. ED Taipei chapter was awarded the 2002 EDS Chapter of the Year Award under his leadership as the Chapter Chair. He received 3 times outstanding Research Award for excellence in research, and was also granted Distinguished EE Professor and Engineering Professor by the Engineering Societies of Taiwan.

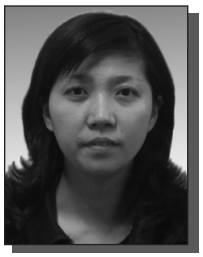
MARK S. LUNDSTROM is the Don and Carol Scifres Distinguished Professor of Electrical and Computer Engineering at Purdue University where he directs the NSF's Network for Computational Nanotechnology. He earned his bachelor's and master's degrees from the University of Minnesota and joined the Purdue faculty upon completing his doctorate there in 1980. Before attending Purdue, he worked at Hewlett-Packard Corporation. Lundstrom is a Fellow of the IEEE, the American Physical Society, and the American Association for the Advancement of Science. He is the recipient of several awards for teaching and research, most recently the 2006 Education Award from the IEEE Electron Devices Society.

ALBERT WANG received his B. Eng. and PhD degrees in EE from Tsinghua University, China, and State University of New York at Buffalo in 1985 and 1996, respectively. From 1995 to 1998, he was with National Semiconductor Corp. He joined the Faculty of ECE at the Illinois Institute of Technology in 1998. His research center on RF/Analog/Mixed-Signal ICs, on-Chip ESD Protection, IC CAD and Modeling, SoCs and Nano Devices, etc. He received the NSF CAREER Award in 2002. He authored one book and 110+ papers. He is an Editor for IEEE Electron Device Letters, an Associate Editor for IEEE Transactions on Circuits and Systems. He is an IEEE Distinguished Lecturer for the Electron Devices Society and the Solid-State Circuits Society. He currently serves as Vice President for IEEE Electron Devices Society and on the ITRS Committee.



XING ZHOU received his B.E. degree in electrical engineering from Tsinghua University in 1983, M.S. and Ph.D. degrees in electrical engineering from the University of Rochester in 1987 and 1990, respectively. He is currently an Associate Professor in the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore. His past research interests include Monte Carlo simulation of photo carrier transport and ultra fast phenomena as well as mixed-mode circuit simulation and CAD tool development. His recent research mainly focuses on nanoscale CMOS technology and device compact modeling. He is a Senior Member of the IEEE, an editor for *IEEE Electron Device Letters*, Chair of the EDS Asia Pacific Subcommittee for Regions/Chapters, a member of the EDS Compact Modeling and VLSI Technology and Circuits technical committees as well as Membership, Publications, and Educational Activities committees, an EDS Newsletter Editor for Region 10, and an EDS Distinguished Lecturer.

B. FIRST-TIME ELECTEES:



RU HUANG received her B.E. and M.S. degrees in EE from Southeast University, China in 1991 and 1994, respectively and Ph.D degree in EE from Peking University, China, in 1997. She joined Peking University in 1997 and became a professor in 2002. Currently she is the Chairman of Microelectronics Department and Deputy Dean of Institute of Microelectronics, Peking University. Her main research interests include nano-scaled CMOS devices, novel memory devices, modeling and simulation and RF technology.

She holds 11 patents, and has authored or co-authored 4 books and more than 140 academic papers. She was the winner of National Youth Science Award of China, Science and Technology Progress Award of China and other awards. She is a Senior Member of IEEE, and has been the technical program co-chair of ICSICT 2004 and technical program committee member of several other international conferences.

RENUKA P. JINDAL (S'77-M'81-SM'85-F'91) received his Ph.D. degree in Electrical Engineering from University of Minnesota 1981. Upon graduation, he joined Bell Laboratories at Murray Hill, New Jersey. In fall 2002 Dr. Jindal accepted the position as Board of Regents Eminent Scholar Endowed Chair in Telecommunications at University of Louisiana, Lafayette. In 1991, he was elected Fellow of the IEEE. From 1990 to

2000 he served as Editor-in-Chief of the *IEEE Transactions on Electron Devices*. In December 2000 he received the IEEE 3rd Millennium Medal. Currently he is Vice-President of Publications for the IEEE Electron Devices Society.

HISAYO S. MOMOSE received the M.S. degree from Ochanomizu Women's University, Japan, in 1984 and the Ph.D. degree from Tokyo Institute of Technology, Japan, in 2006.

In 1984, she joined Toshiba Corporation, where she was engaged in the development of static RAMs and logic LSIs and the research of hot-carrier reliability, oxynitride gate, Ni salicide and ultra-thin gate oxide MOSFETs in the direct-tunneling regime. Her current interests include RF characteristics and the related issues of CMOS analog devices. She has authored or co-authored more than 100 papers published in technical journals or presented at international conferences.

She is an IEEE Fellow. She served as a technical program committee member for IRPS, IEDM, EDSSC and MIXDES. Since 2005, she has also served as an editor of *IEEE Transactions on Electron Devices and the Microelectronics Reliability*.

Hiroshi Iwai
EDS Nominations and Elections Chair
Tokyo Institute of Technology
Yokohama, Japan

Call for Nominations - EDS AdCom

The Electron Devices Society of the IEEE invites the submission of nominations for election to its Administrative Committee (AdCom). Presently, the AdCom meets twice per year and is composed of 22 members. Seven members will be elected this year for a term of three years, and a maximum of two consecutive terms is allowed. In 2007, the election will be held after the AdCom meeting on Sunday, 9 December. Electees begin their term in office on 1 January 2008. For your information, the nominees do not need to attend the AdCom Meeting/Election to run.

Nominees are being sought to fill the slate of candidates. Nominees may be self-nominated, or may be nominated by another person; in the latter case, the nominee must have been contacted and have agreed to serve if elected. Any member of EDS in good standing is eligible to be nominated. As another condition for nomination and election, a nominee is expected to attend the two annual AdCom meetings, if elected in his/her term. In general, the travel and accommodation costs to attend these meetings are borne by the elected member.

Please send your nominee's name, address, and supporting information to the EDS Executive Office Sr. Administrator, Laura J. Riello, IEEE, 445 Hoes Lane, Piscataway, NJ 08854, Fax: 732-235-1626, E-Mail: l.riello@ieee.org in time to be received by the deadline of 15 October 2007. It is very desirable that submissions include a biographical summary in a standard two-page format. The EDS Executive Office can provide you with an example of the format. If you have any questions regarding the nomination requirements or process, feel free to contact Laura Riello (l.riello@ieee.org).

Hiroshi Iwai
EDS Nominations & Elections Chair
Tokyo Institute of Technology
Yokohama, Japan

EDS Administrative Committee Election Process

The Members-at-Large (MAL) of the EDS AdCom are elected for staggered three-year terms, with a maximum of two consecutive terms. The 1993 Constitution and Bylaws changes mandated increasing the number of elected MAL from 18 to 22, and required that there be at least two members from both IEEE Region 8 (Europe, Middle East & Africa) and Region 10 (Asia & Pacific). In 2003, EDS made changes to its Constitution and Bylaws to require that at least one elected AdCom member is a Graduate of the Last Decade (GOLD member). A GOLD member is defined by IEEE as a member who graduated with his/her first professional degree within the last ten years. It is also required that there are at least 1.5 candidates for each opening. In 2007, seven positions will be filled.

The election procedure begins with the announcement and Call for Nominations in the EDS Newsletter. The slate of nominees is developed by the EDS Nominations Committee and includes the non-Committee and self-nominations received. Nominees are asked to submit a two-page biographical resume in a standard format. Nominations are closed on 15 October, and the biographical resumes are distributed to the 'full' voting members of AdCom prior to the December AdCom meeting. The election is then held after the conclusion of the meeting. The nominees do not need to attend the AdCom Meeting/Election to run. On the other hand, if elected, are expected to attend the two AdCom meetings a year. In general, the travel and accommodation costs to attend these meetings are borne by the elected member.

A continuing flow of new AdCom members who are interested in working for the improvement of the Society and its related technical areas is essential for the continued development of EDS and the field of electron devices. Those interested in the field, the Society, and its operations are encouraged to attend AdCom meetings, become involved in Society activities, and consider running for election to AdCom.

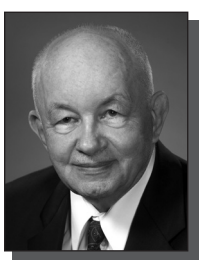
Hiroshi Iwai
EDS Nominations & Elections Chair
Tokyo Institute of Technology
Yokohama, Japan

EDS MEMBERS NAMED WINNERS OF THE 2007 IEEE TECHNICAL FIELD AWARDS

Four EDS Members were among the winners of the 2007 IEEE Technical Field Awards. They are:

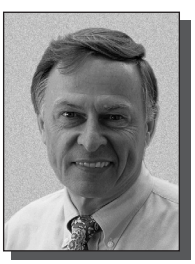
Sandip Tiwari of Cornell University., Ithaca, NY, won the 2007 IEEE Cledo Brunetti Award. His citation states, "For pioneering contributions to nano-crystal memories and to quantum effect devices"

Sandip Tiwari, the Charles N. Mellowes Professor of Engineering at Cornell University in Ithaca, N.Y., has made seminal contributions to the field of nanotechnology, resulting in greatly increased storage capacities for compact devices used in mobile communications, computing and other applications. Over his career, he has repeatedly broken new ground in areas spanning heterostructures, quantum confinement and nano-devices. Dr. Tiwari's early research led to several technologies currently in use in compound semiconductors and other device phenomena including electron injection processes in coupled confined systems and frequency limitations of quantum-wire lasers due to gain compression. His research with semiconductors, nonlinearity, coupling across scales and adaptation also helped advance the fields of electronics and photonics. An IEEE Fellow, he received the 1991 Young Scientist Award from the Institute of Physics and the 2003 Distinguished Alumnus Award from the Indian Institute of Technology.



Dimitry Grabbe of Worcester Polytechnic Institute, Worcester, MA, won the 2007 IEEE Components, Packaging & Manufacturing Technology Award. His citation states, "For contributions to the fields of electrical/electronic connector technology, and development of multi-layer printed wiring boards"

Dimitry Grabbe played an integral part in advancing U.S. space exploration. His pioneering work has produced nearly 500 U.S. and foreign patents covering machine design, semiconductor packaging, electronics assembly and optoelectronic connector design. His work in printed circuit board technology for electronic packaging led to the development of large, multi-layer printed circuit boards. This proved crucial in helping U.S. astronauts gain greater real-time control of their space-exploration activities. In 1964, Mr. Grabbe founded the Maine Research Corporation which specialized in high-end printed circuit boards; the company was dissolved in 1972. He joined AMP, Inc. in 1973, and helped it become a world leader in electrical/electronic connector technology, test socket technology and miniature semiconductor packages. Today, Mr. Grabbe is assisting Dr. Pryputniewicz, professor of mechanical engineering and founding director of the center for holographic studies and laser micromechaTronics (CHSLT) at Worcester Polytechnic Institute (WPI) in Worcester, Mass. with research on gyroscopes and accelerometers. An IEEE Life Fellow, Mr. Grabbe has also been recognized by AMP (now part of Tyco Electronics) with a Lifetime Achievement Award, and by the American Society of Mechnical Engineers, which chose him for its Leonardo da Vinci Award.



James D. Plummer of Stanford University, Stanford, CA, won the 2007 IEEE Andrew S. Grove Award. His citation states, "For seminal contributions to the modeling, simulation, and physics of silicon devices"

For over 30 years, James Plummer has made significant contributions in three main areas of electronic devices, namely, computer-aided design of silicon devices and fabrication processes, high-voltage power devices and circuits, and novel devices for memory and logic applications. His early work focused on high-voltage integrated circuits (IC) and high-voltage device structures, including seminal contributions to the insulated gate bipolar transistor (IGBT), a device that has become a key component of the multi-billion-dollar high-power electronics industry. Dr. Plummer's work on silicon process modeling led to the development of several generations of the process modeling program SUPREM, which today is the standard process-modeling tool used worldwide. Most recently, Dr. Plummer has worked on nanoscale silicon devices for logic and memory applications. An IEEE Fellow, he has received numerous recognitions for his work, including IEEE awards, Semiconductor Research Corporation Awards, "best paper" awards, the Electrochemical Society's 1991 Solid State Science and Technology Award and election to the National Academy of Engineering.

Umesh K. Mishra of University of California, Santa Barbara, CA, won the 2007 IEEE David Sarnoff Award. His citation states, "For development of gallium nitride electronics"

Professor and associate dean of the College of Engineering at the University of California in Santa Barbara, Umesh Mishra is a leader in developing compound semiconductor electronics and a driving force behind the rapid progress in gallium

(continued on page 14)

nitride (GaN)-based microwave devices and circuits. He began his career researching gallium arsenide and indium phosphide (InP) high electron mobility transistors (HEMTs) for low noise amplifiers, which became the leading receiver technology for many space-based platforms. Dr. Mishra's research group was the first to demonstrate that the unique wide bandgap and electron transport properties of gallium nitride could be harnessed to create devices with an unprecedented combination of high-frequency performance and microwave power output. Since then, Dr. Mishra has continued to make key advances in both the fundamental understanding and the technological exploitation of GaN/A1GaN HEMT devices. An IEEE Fellow, Dr. Mishra has a bachelor's from the Indian Institute of Technology in Kanpur, India, a master's from Lehigh University in Bethlehem, Pa., and a doctorate from Cornell University in Ithaca, N.Y., all in electrical engineering.

Alfred U. Mac Rae
EDS Awards Vice-President
Mac Rae Technologies
Berkeley Heights, NJ, USA

Status Report from the 2006 Graduate Student Fellowship Winners

In 2000, the IEEE approved the establishment of the Electron Devices Society Graduate Student Fellowship Program. The Program is designed to promote, recognize, and support graduate level study and research within the Electron Devices Society's Fields of Interest: which include: All aspects of the engineering, physics, theory, experiment and simulation of electron and ion devices involving insulators, metals, organic materials, plasmas, semiconductors, quantum-effect materials, vacuum, and emerging materials. Specific applications of these devices include bioelectronics, biomedical, computation, communications, displays, electro and micro mechanics, imaging, micro actuators, optical, photovoltaics, power, sensors and signal processing. In deference to the increasing globalization of our Society, at least one fellowship is to be awarded to students in each of three geographical regions: Americas, Europe/Mid-East/Africa, and Asia & Pacific.

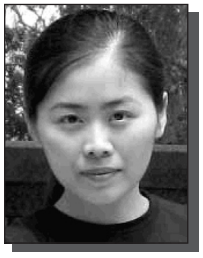
In July 2006, EDS announced the winners of the 2006 Fellowships. The four winners were: Ravi Todi of the University of Central Florida, Orlando, FL, USA; Rimoon Abaiby, University of Newcastle, Newcastle Upon Tyne, United Kingdom; Wen Wu, Hong Kong University of Science & Technology, Hong Kong; and Chi Yung Ng, Nanyang Technological University, Singapore. The winners are pursuing distinctly different research topics for their doctoral degrees. The following are brief progress reports written by the award winners.

RAVI TODI

I received my Ph.D. degree from the School of Electrical Engineering and Computer Science at University of Central Florida in May 2007. My dissertation was in the area of gate stack and channel engineering with specific focus on binary metal alloys and germanium channel devices. Since May 2007, I have been working as Advisory Engineer/Scientist at IBM's Microelectronics Division, East Fishkill, New York.

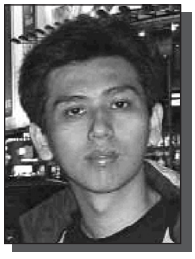
RIMOON ABAIBY

At present, I am looking into the potential of advanced MOSFETs with strained Si channels for different applications. Several studies are currently in preparation (1) temperature dependant degradation in SiON gate dielectrics on strained Si channels with SiGe thin/thick strain relaxed buffers (2) assessing the potential of advanced strained Si MOSFETs in mixed signal applications (3) insight into the effect of surface morphology and processing conditions on the quality of SiON gate dielectrics on strained SOI. These studies promise to bring to light several reliability issues which were never considered. My Ph.D. thesis should be complete by September 2007.



WEN WU

Her research at HKUST covers a broad area in silicon devices design and modeling, ranging from design optimization of traditional devices to compact model development for non-traditional emerging devices for RF/Microwave applications. Recently, she has been involved in the international joint NEDO project to develop a modeling framework for next-generation MOS devices. She derived a physical model to account for the parasitic effects on the characteristics of non-planar multi-gate devices. The results have been published in the 2007 issues of I*EEE Transactions on Electron Devices and Solid-State Electronics*. In addition, she has authored two invited conference papers on compact modeling.



CHI YUNG NG

He joined Nanyang Technological University, Singapore, to pursue a Ph.D. degree in Microelectronics. His Ph.D. thesis title is "Synthesis, characterizations and device applications of silicon nanocrystal", under the guidance of Assoc. Prof. Tupei Chen. He has

authored or coauthored 27 international peer-reviewed journal papers during the 4 years of Ph.D. studies. His research interest includes physical properties and device applications based on semiconductor nanostructure, nonvolatile memory devices and nanoscale CMOS devices. His thesis has been submitted for review. He can be reached at chiyung@ieee.org.

Agis A. Iliadis
2007 EDS Student Fellowships Chair
Electrical and Computer Engr. Dept.
University of Maryland
College Park, MD, USA

IEEE NANOTECHNOLOGY COUNCIL ANNOUNCES 2007 AWARD WINNERS

IEEE Nanotechnology Council Awards Committee (Chaired by Prof. Chennupati Jagadish) announced its 2007 award winners for IEEE Nanotechnology Pioneer Award, IEEE NTC Distinguished Service Award and IEEE NTC Early Career Award. These awards will be presented at IEEE NANO 2007 in Hong Kong in August 2007.

Nanotechnology Pioneer Award

The NTC Pioneer Award in nanotechnology is to recognize individuals who by virtue of initiating new areas of research, development or engineering have had a significant impact on the field of nanotechnology. The winners of the 2007 award are:

- Professor Pallab Bhattacharya (University of Michigan) for contributions to "Quantum Dot Optoelectronic Devices"
- Professor Mark Reed (Yale University) for contributions to "Nano and Molecular Electronics"

Distinguished Service Award

The purpose of the Distinguished Service Award is to recognize an individual who has performed outstanding service for the benefit and advancement of the IEEE Nanotechnology Council.

- Toshio Fukuda (Nagoya University) is the winner for his outstanding service to the Council as its Founding President and in many other roles

Nanotechnology Early Career Award

The purpose of the Nanotechnology Early Career Award is to recognize individuals who have made contributions with major impact on the field of nanotechnology. The winner of the 2007 award is

- Professor Chongwu Zhou (University of Southern California) for his contributions to "Nanowire and Nanotube Electronics"

Professor Chennupati Jagadish
IEEE NTC Awards Committee Chair
Research School of Physical Sciences and Engineering
The Australian National University
Canberra, ACT 0200, Australia

CALL FOR NOMINATIONS

IEEE Nanotechnology Council (NTC) Awards

The IEEE Nanotechnology Council (NTC) is accepting nominations for the three NTC awards to be presented at IEEE NANO 2008. All nominees need to be IEEE members. Please send nominations (electronic and one hard copy) with supporting material to: Prof. Chennupati Jagadish, Chair, IEEE NTC Awards Committee, Research School of Physical Sciences and Engineering, The Australian National University, Canberra, ACT 0200, Australia. Ph: +61-2-6125-0363, Fax: +61-2-6125-0511, Email: c.jagadish@ieee.org. All nomination material including reference letters should reach the NTC awards committee by October 15, 2007.

1. Pioneer Award In Nanotechnology

Description: The NTC Pioneer Award in nanotechnology is to recognize individuals who by virtue of initiating new areas of research, development or engineering have had a significant impact on the field of nanotechnology. The award is intended for people who are in the mid or late portions of their careers, i.e., at least 10 years beyond his or her highest earned academic degree.

Eligibility: Any current member of the IEEE working in the Nanotechnology who is at least 10 years beyond his or her highest earned academic degree.

Employment of Candidates: The Council may grant two awards in this category, if the Awards Committee determines that the nominations are worthy. There may be one award for academics (persons employed by colleges or universities) and one for persons employed by industry or government organizations.

Prize Items: The award consists of $1000 ($500 each if two awards are made) honorarium and a commemorative plaque.

Selection/Basis for Judging: Factors that will be considered are: Distinction in long-term technical achievement, leadership, innovation, breadth, and impact on nanotechnology and engineering.

2. Early Career Award In Nanotechnology

Description: The Nano Technology Council to establish an Early Career Award to recognize individuals who have made contributions with major impact on the field of nanotechnology.

Eligibility: Any current member of the IEEE who is in the early stage of his or her career in the nanotechnology field, i.e., less than 7 years after being granted his or her highest earned academic degree.

Employment of Candidates: The Society may grant two awards in this category, if the Awards Committee determines that the nominations are worthy. There may be one award for academics (persons employed by colleges or universities) and one for persons employed by industry or government organizations.

Prize Items: The award consists of $1000 ($500 each if two awards are made) honorarium and a commemorative plaque.

Selection/Basis for Judging: Factors that will be considered are: Distinction in technical innovation and achievement, and impact on nanotechnology and engineering.

3. NTC Distinguished Service Award

Description: Nanotechnology Council to establish a Distinguished Service Award to recognize an individual who has performed outstanding service for the benefit and advancement of Nanotechnology Council.

Eligibility: Any current or former member of IEEE Nanotechnology Council with outstanding service in one or more of the following areas: conferences and meetings, publications, editors, administrative committee, chapter leadership, or other distinguished services and activities for the Nanotechnology Council.

Prize Items: The award consists of $1,000 honorarium and a commemorative plaque. Selection/Basis for Judging: Factors that will be considered are: Impact of service and contributions to the Council, leadership, innovation, activity, duration, breadth of participation and cooperation.

Congratulations to the EDS Members Recently Elected to IEEE Senior Member Grade!

Parhat Ahmet
Pietro Andreani
Ciaran Conneely*
Paul Crump
Gana Dash
Grzegorz Deptuch
Donald Disney
Tomas Gonzalez*
Jyh-Chyurn Guo
Allen Hanson
Tony Heinz
Albert Henning
Leonardo Hillkirk*
Digh Hisamoto
Lalit Kumar
Po-Tsun Liu*
Eduard Llobet*
Joao Martino
Yoshinori Matsubara
Gaudenzio Meneghesso
Joe Mcalexander*
Jian Mi*
Matthew Nowak
Chul Park
Lindsay Quarrie
Vesna Roje
James Sewell*
Sivalingham Sivananthan
Karl Strauss
Lisa Su
Mani Sundaram
Kazuo Tsutsui
Klaus Johannes Weber
Richard Williams
Gilson Wirth*
Ying Wu
Ji-Woon Yang
Zhiping Yin
Franco Zappa*
Jun-Fei Zheng*
Babak Ziaie
Christian Zorman*

* = Individual designated EDS as nominating entity

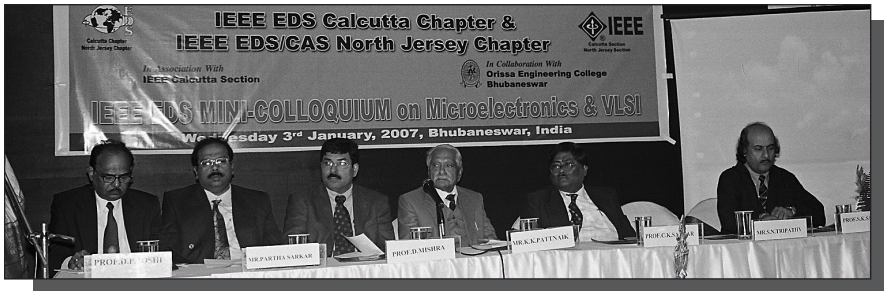
If you have been in professional practice for 10 years, you may be eligible for Senior Membership, the highest grade of membership for which an individual can apply. New senior members receive a wood and bronze plaque and a credit certificate for up to US $25 for a new IEEE society membership. Upon request, a letter will be sent to employers, recognizing this new status.

For more information on senior member status, visit http:// www.ieee.org/web/membership/senior-members/status.html. To apply for senior member status, fill out an application at http://www.ieee.org/ organizations/ rab/md/smelev.htm.

EDS Chapter Subsidies for 2008

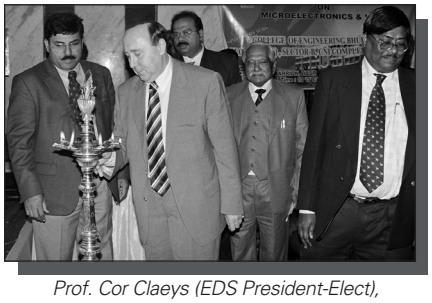
The deadline for EDS chapters to request a subsidy for 2008 is 1 September 2007. For 2007, the EDS AdCom awarded funding to 59 chapters, with most amounts primarily ranging from US$250 to US$1,500. Recently, Chapter Chairs were sent an e-mail notifying them of the current funding cycle and providing them with a list of guidelines. In general, activities which are considered fundable include, but are not limited to, membership promotion travel allowances for invited speakers to chapter events, and support for student activities at local institutions. Subsidy requests should be sent via e-mail or fax to the EDS Sr. Administrator, Laura J. Riello, IEEE, EDS Executive Office, 445 Hoes Lane, Piscataway, NJ 08854, l.riello@ieee.org or fax 732-235-1626. Prior to the submission of the subsidy request, the Chapter Chair must submit a chapter activity report to its respective SRC Chair and Laura Riello of the EDS Executive Office by July 1. This report should include a general summary of chapter activities (one to two pages) for the prior July 1st - June 30th period. You must also attach a copy of the activity report to your chapter subsidy request. Final decisions concerning subsidies will be made by the EDS SRC Chairs/Vice Chairs in December. Subsidy checks will be issued by late January.

EDS Distinguished Lecturers Visit Bhubaneswar, India



Inaugural ceremony of IEEE EDS Mini-Colloquium on Microelectronics and VLSI, held jointly on 3 January 2007, organized by the ED Calcutta and ED/CAS North Jersey Chapter. From left to right: Prof. D.P. Joshi, Prof. P. Sarkar, Prof. D. Misra, Mr. K.K. Patnaik, Prof. C.K. Sarkar, Prof. S.K. Sanyal

The ED Calcutta Chapter, which started its activities three years ago, was proud to organize a mini-colloquium jointly with the ED North Jersey Chapter and the IEEE Calcutta Section successfully. The theme of the mini-colloquium was MICROELECTRONICS and VLSI. The venue of the mini-colloquium was chosen in the temple city of Orrisa Bhubaneswara. Recently, Bhubaneswar has grown into a modern capital city with air and rail connections to different parts of India such as Mumbai and New Delhi. The city has many engineering colleges in and around it and also several IT software industries, significantly contributing to the Indian economy. The choice of the venue was very appropriate and also found to be fruitful.



Prof. Cor Claeys (EDS President-Elect), inaugurating the mini-colloquium by lighting the lamps, with Prof. D. Misra, ED North Jersey Chapter Chair and Prof. C.K. Sarkar, ED Calcutta Chapter Chair

The colloquium was arranged in The New Marion Bhubaneswar on January 3, 2007 and seven IEEE Distinguished Lecturers were invited from different countries. The speakers, very famous and well established in the area of Microelectronics and VLSI, were Prof. Cor Claeys (Belgium), Prof. Durga Misra (USA), Prof. L. Pfitzner (Germany), Prof. M. Bushnell (USA), Prof. H. Iwai, (Japan), Prof. R. Jindal (USA) and Prof. R.V. Rao (India). Unfortunately, two of the speakers, Prof. Jindal and Prof. Pfitzner, could not participate due to travel schedule disruptions.

The presentations of the other speakers were excellent and very much appreciated by the participants. The one hundred participants that registered for the colloquium, were mainly faculty and students from engineering institutions and practicing engineers from industries.

The event was primarily sponsored by IEEE EDS (USA), through the IEEE ED Calcutta Chapter, along with the ED New Jersey Chapter and the IEEE Calcutta Section. Mr. Partha Sarkar, ED Calcutta Chapter Secretary and HOD, Electronics Engineering Dept. of Orissa Engineering College, Bhubaneswar, took great initiative in getting sponsorships from various engineering colleges in Bhubaneswar and publicizing the event on a big scale, drawing large numbers of participants for the colloquium. Orissa Engineering College emerged as a major sponsor of the event providing great help with the logistics and infrastructure, making the colloquium a grand success.

The major outcome of the event is that many faculty members and students showed their interests in joining IEEE and EDS. Approximately, thirty new members joined the organization. Also, they insisted on organizing similar EDS events in the future for Orissa. The organizing secretary is taking an effort to form a new EDS chapter at Bhubaneswar very soon

Finally, the EDS mini-colloquium in Bhubaneswar has generated a strong motivation for spreading the objective of the IEEE EDS among prospective engineering colleges.

Chandan K. Sarkar
ED Calcutta Chapter Chair

Durga Misra
ED/CAS Chapter Chair and
EDS SRC-NAE Chair

Participants, organizers and EDS Distinguished Lecturers attending the IEEE EDS Mini-Colloquium at Bhubaneswar

In Memory of Prof. Gerold Neudeck, Purdue University

Dr. Gerold W. Neudeck, a pioneer in 3-D silicon device research, well-known textbook author, and a beloved teacher at Purdue University for the past 40 years, lost a courageous battle with cancer and passed away, April 25, 2007. Dr. Neudeck was an IEEE Fellow since 1990, a former editor of Transaction on Electron Devices, recipient of the 1992 Nyquist Award, and recipient of the 2001 SRC Aristotle Award.

Gerry was born Sept. 25, 1936 in Beach, North Dakota. He attended the University of North Dakota, receiving a bachelor's degree in 1959 and master's degree in 1960. He was assistant professor of electrical engineering there from 1960 to 1964. He was an instructor and research assistant at Purdue University between 1964 and 1968, while completing his Ph.D., and was a professor of Electrical Engineering at Purdue from that time until his retirement on December 31, 2006. Dr. Neudeck served as Purdue's Associate Dean of Engineering between 1988 and 1991.

Gerry is survived by his wife of 45 years, Mariellen, and their two sons, Phil of Omsted Falls, Ohio and Alex of Windsor, Colorado. Both of his sons also graduated with Ph.D. degrees in Electrical Engineering from Purdue University and are IEEE EDS members. He is also survived by his mother, Helen Anderson of Spearfish, SD and two sisters, Joyce Freese of Spearfish and Lyla Anderson of Bellevue, WA, as well as four granddaughters.

Dr. Neudeck was the author or co-author of 9 widely used solid-state devices and microelectronic circuit design textbooks and 271 refereed professional publications. He held 15 patents for various MOSFET and BJT devices. His research focused on novel silicon device structures, physics, and fabrication technologies. This included amorphous silicon TFT's,

polysilicon emitter BJT's, and especially selective (SEG) silicon epitaxial lateral overgrowth (ELO) for the fabrication of fully-depleted, double-gated SOI MOSFET's, micromechanical sensors, and multiple stacked layers of SOI devices for 3-D integration.

His teaching awards included the Purdue University Book of Great Teachers in 1999; the Honeywell Teaching Award in 1995; the D.D. Ewing Award in 1973, the A.A. Potter Award in 1973 and the Dow Outstanding Young Faculty Award, Illinois-Indiana section of the American Society for Engineering Education.

Dr. Neudeck was a member of several honorary societies, including Sigma Xi, Sigma Tau, Eta Kappa Nu and Sigma Pi Sigma. He also was a board member for NICHES (Northern Indiana Citizens Helping Ecosystems Survive), was Parlor Club president from 2006 to 2007, and served on the Greater Lafayette Public Transportation Board between 1979 and 1980.

Gerry was given a lifetime honor in 1999 by being chosen by Purdue students for inclusion in The Book of Great Teachers, who have devoted their lives to excellence in teaching and scholarship. The success of a teacher is probably best measured by the success of his students. Professor Neudeck graduated 26 MS and 28 Ph.D. students who have been very successful in both industry and academia. Here are some comments from his former students:

"Dr. Neudeck has been a lifelong role model for me, shaping both my teaching style and research approach. He is my example for how to respect and genuinely care for both the professional and personal lives of my students and colleagues."

"Gerry taught me how to effectively and successfully manage all aspects of a complicated program. His continuous support, encouragement, and coaching gave me tremendous confidence when I started as an engineer at AMD."

"If you want your organization to be successful, you must foster a healthy emotional environment, you must stress the fundamentals, and you must be committed to the success of your colleagues. Dr. Neudeck taught these lessons by example…he was committed to my success above and beyond his own."

"I believe the main reason that Prof. Neudeck was a successful researcher and excellent mentor was his ability to get his students to work as a team. He helped students mature academically and professionally by getting them to take ownership of their projects"

"After eight years in several different engineering groups, I still think of Professor Neudeck as the model of what I'd like to become."

He will be greatly missed by the electron devices and IEEE community.

Stephen A. Parke
EDS Treasurer
Tennessee Tech University
Cookeville, TN, USA

EDS DISTINGUISHED LECTURER PROGRAM - LECTURERS RESIDING IN EASTERN USA & CANADA

The EDS Distinguished Lecturer Program exists for the purpose of providing EDS Chapters with a list of quality lecturers who can potentially give talks at local chapter meetings. To arrange for a lecture, the EDS chapters should contact the Distinguished Lecturer directly. A general guideline for the visit, but not the absolute rule, is that the lecturer should be able to include the meeting site with an already planned travel schedule at a small incremental cost to the travel plan. Alternatively, a prior coincident travel plan would not be required if the lecturer is already located within an approximate fifty mile radius of a meeting site. Although the concept of the program is to have the lecturers minimize travel costs by combining their visits with planned business trips, EDS will help subsidize lecturer travel in cases where few/no lecturers will be visiting an area and/or a chapter cannot pay for all the expenses for a lecturer trip. For a full listing of EDS Distinguished Lecturers and travel plans please contact Laura Riello of the EDS Executive Office (Tel: 1-732-562-3927, Fax: 1-732-235-1626, E-Mail: l.riello@ieee.org).

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- Single photon, and standing wave photodetectors in bulk and SOI CMOS technologies.
- Devices for mixed analog/digital circuits 3D SOI-CMOS: challenges and opportunities
- Hybrid CMOS/living cells structures: Where are we now and where are we heading to?
- Integration and packaging challenges in hybrid silicon/silicone (PDMS) microsystems for the life sciences.

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- Integrated-Circuit Engineering
- High-Field Effects in Quantum-Confined Systems
- Hot Electrons: A Myth or Realty?
- The Role of Physical and Behavioral Sciences in the Development of Strategic Technologies in Nano/Micro-Systems
- Outcome-Based Education, Training, and Leadership for Competitive Excellence

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- Comparison of Theory & Exp
- Consensus-Based Planning for Compound Semiconductor Technologies (Technology Roadmaps)
- RF and Analog Mixed-Signal Technologies for Wireless Communications
- The United States Measurement System: Technological Innovation
- Imaging as a Biomarker: Change Measurement in Therapy

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- RF Performance MOSFETs and RFICs - Effects of Electrical Stress
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- Band Edge Defects in High-k Gate Dielectrics and at Their Internal Device Structure Interfaces
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- Silicon technology — future trends from a system application perspective

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- Strain Effects in Advanced CMOS and MEMS Piezoresistive Sensors
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- The ESD Technology Roadmap
- Electrostatic discharge (ESD) in RF Technologies
- CMOS Latchup in CMOS and BiCMOS SiGe Technology

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- Electronic Skin, Electrotextiles Flexible, Deformable, and Elastic Electronic Surfaces

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- Nano-scaled CMOS Device and Circuit Reliability

Report on the IEEE EDS Mini-Colloquium, Santa Clara, CA

EDS Distinguished Lecturers and organizers of the Santa Clara University EDS Mini-Colloquium. From left to right: Prof. C. Claeys, Dr. T. Krishnamohan, Prof. J.J. Liou, Dr. N.D. Arora, Dr. P. Jansen, Dr. S. Saha, Prof. C.Y. Yang, Prof. P.K. Yu, and Prof. S. Krishnan

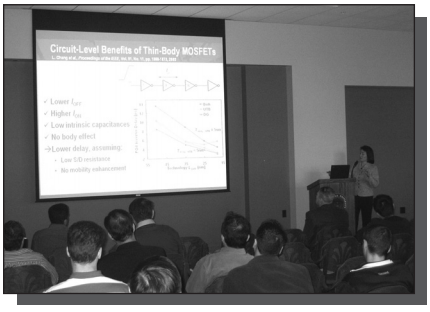
The Electron Devices Society (EDS) Santa Clara Valley (SCV) Chapter, in collaboration with the Santa Clara University (SCU) Chapter, hosted a mini-colloquium on Friday, February 23, 2007, at the SCU Campus, Santa Clara, CA. The objective of this mini-colloquium was to provide technical perspective on "Next Generation Device Technologies" by EDS Distinguish Lecturers (DLs) and student researchers working in the field. There were six talks and three student posters with a total attendance of about 120.

The event started with a welcome address by Prof. Cary Yang of SCU, followed by three talks in the morning session. The first presentation, "Strain Engineering and Device Performance: Benefit or Compromise?" was offered by Prof. Cor Claeys, IMEC. He started with an overview of presently known different strain engineering techniques and presented a global approach based on the strained Si on strain-relaxed SiGe buffer layers and the use of process-induced stressors like an embedded SiGe layer and a contact etch stop layer (CESL) in a FinFET technology. He also, highlighted the major advantages and disadvantages of different strain-engineering approaches and discussed the use of Ge and GeOI as high-mobility substrates. The second speaker, Prof. Juin Liou, of UCF, presented "Robust Electrostatic Discharge (ESD) Protection in CMOS Technology." He provided an overview of the ESD sources, models, and protection schemes with examples of recent development on robust ESD solutions for protecting data communication transceivers and gas-sensor microchips. Prof. Liou then discussed the results of technology CAD-based ESD modeling. The third talk was by Dr. Tejas Krishnamohan of Intel, on "High Mobility Materials and Novel Device Structures for High Performance Nanoscale MOSFETs." He discussed the limitations of presently used techniques to scale MOSFETs to sub-20 nm regime and showed higher mobility materials like Ge, strained-SiGe, strained-Ge, and III-V materials like GaAs, InAs, InSb, and InGaAs together with innovative device structures as alternatives for future devices. Dr. Krishnamohan showed that Ge could be suitable for p-MOS while high electron mobility III-V materials could be suitable for n-MOS. However,

for both Ge and III-V devices the problems of leakage need to be solved and novel heterostructures will be needed to exploit the promise advantages of Ge and III-V based devices.

During lunch hour, SCU student researchers, working under the supervision of Prof. Cary Yang and Prof. Shoba Krishnan presented three posters. The first poster, "Carbon Nanofiber Interconnects: Contact Annealing and High-Current Breakdown" by Q.X. Ngo, H. Kitsuki, M. Suzuki, A. Cassell, C. Moylan, J. Li, K. Gleason, and C.Y. Yang; the second, "Characterizing Neuronal Networks Using Carbon Nanotube Microelectrode Array," by A. Seger, E. de Asis, W. Won, L. Wang, K. Kagoo, J. Hieb, M.S. Isaacson, and C.Y. Yang; and the third poster, "The Carbon Nanotube Enhanced Tunneling Diode Via In Situ Highly Controlled Electric Field Induced Surface Functionalization," by A.J. Austin, C. Estonilo, Q.X. Ngo, C.V. Nguyen, and S. Krishnan.

The afternoon session started with the presentation on "RCL Characterization and Modeling of X Architecture Diagonal Wires for VLSI Design," by Dr. Narain Arora of Cadence. He showed that for sub-100 nm copper CMOS processes, X Architecture diagonal wire interconnects offer faster and smaller IC Chips compared to the same design in Manhattan routing and he also discussed the results of RCL characterization, modeling, SEM/FIB analysis of these diagonal lines for VLSI design. The second talk



Professor Tsu-Jae King Liu speaking on "FinFET Technology for Nanoscale CMOS Digital Integrated Circuits"

by Prof. Paul Yu of UC San Diego, on "Recent Advances in Photonic Devices for RF/Wireless Communication Applications." reviewed the advances in the state-of-the-art photonics devices for analog links such as laser diodes, high power lasers, external modulators, semiconductor amplifiers, erbium doped fiber amplifier, and photodetectors and compared the direct modulation scheme with that of external modulation. Prof. Yu also discussed the research frontiers in external optical modulators. The final presentation was offered by Prof. Tsu-Jae King Liu, UC Berkeley, on "FinFET Technology for Nanoscale CMOS Digital Integrated Circuits." Prof. Liu provided details of FinFET technology and discussed how it can be used to improve the performance, standby power consumption, and variability in nanoscale-CMOS digital ICs.

The mini-colloquium was organized by Samar Saha, EDS SCV Chapter Vice-Chair, Prof. Shoba Krishnan, Faculty Advisor of the IEEE SCU Chapter, and SCU Student Chapter President, Alexander Austin, with Prof. Cary Yang as the advisor and Ms. Amber Delacruz of EE Department, SCU, as the event assistant. All the talks were interactive with active participation from the attendees.

Samar Saha
ED Santa Clara Valley Chapter Vice-Chair
DSM Solutions, Inc.
Los Gatos, CA, USA

Call for Nominations for the EDS Chapter of the Year Award

The EDS Chapter of the Year Award is given each year based on the quantity and quality of the activities and programs implemented by the chapters during the prior July 1st – June 30th period. Nominations for the award can only be made by Chapter Partners, SRC Chairs/Vice-Chairs, or self-nominated by Chapter Chairs.

The winning chapter will receive a certificate and check for $1,000 to be presented at the International Electron Devices Meeting (IEDM).

As of the 2007 Award, the EDS AdCom approved a ruling whereby a chapter that wins the Chapter of the Year Award cannot win again until after a lapse of 3 years.

The schedule for the award process is as follows:

ACTION	DATE
Call for Nominations E-Mailed to Chapter Chairs, Chapter Partners, SRC Chairs & SRC Vice-Chairs	June
Deadline for Nominations	9/15
Regions/Chapters Committee Selects Winner	Early-October
Award given to Chapter Representative at IEDM	First week of December

Not an undergraduate anymore? EDS Cares!!

Success! You have completed your undergraduate degree in engineering after years of study – years of essays, exams, labs, and assessments – years of erratic sleep patterns and far too much caffeine! The inevitable question remains...now what? Following graduation, life changes quickly and you will soon find yourself in a new environment. Whatever path you choose to take, be it industry or further postgraduate study, know that the IEEE via GOLD (Graduates Of the Last Decade), and EDS are there to assist you in your transition. The GOLD program supports young IEEE members (if you are an IEEE Member who graduated with your first professional degree within the last ten years, you are automatically part of IEEE GOLD!), GOLD affinity groups, and the GOLD-Society Interaction Project. Both the IEEE and GOLD already offer a comprehensive array of products and services that can assist young IEEE members (see below); however, EDS would like to do more for its young members – more for new graduates like you. EDS needs to know what the Society can do (or is already doing!) to provide you with value for your continued membership and to help you grow professionally. In your opinion...

What sort of programs would you like to see sponsored by the Society? Would you be interested in participating in online seminars with distinguished leaders in the electron device field? What topics are of interest to you – technical subjects relating to your field of work or soft skills subjects such as developing your leadership, team building, and networking and communication skills? Would you like to see EDS sponsored GOLD seminars and or workshops? Would you like to see more networking events in your area? What would make Society membership renewal more appealing to you and your peers? EDS would like to hear from its YOUNG professional members. Reader, please share your ideas, comments and constructive criticisms with your EDS IEEE GOLD Coordinator, Ravi Todi (rtodi@ieee.org), as we are keen for advice and projects for 2007!

IEEE and GOLD Products and Services for Young Members

Online resources:

- IEEE: http://www.ieee.org/membership/congrats
- GOLD: http://www.ieee.org/organizations/rab/gold/
- IEEE Xplore ® – access the world of IEEE information online through one dynamic interface.
- IEEE Spectrum – this monthly magazine is the flagship publication of the IEEE for technology innovators, business leaders, and the intellectually curious. Spectrum explores future technology trends and the impact of those trends on society and business.
- IEEE Job Site - post your resume and receive a confidential email when a job listing matches your skill set.
- IEEE Career & Employment Resources.
- IEEE Center for Education & Training.
- Electro-Technology Industries (ETI) database.
- GOLD-sponsored internet conferences, seminars, and professional workshops.

Personal Benefits:

- IEEE Personal Email Alias - identify yourself as part of a worldwide community of innovators by registering for a free IEEE email alias, complete with virus scanning software.
- What's New @ IEEE - subscribe to one of eleven monthly email newsletters that feature IEEE information, career assistance and industry news.
- Your own Web account for online services.
- IEEE Financial Advantage Program - includes insurance programs, credit cards and investment opportunities.
- Opportunity to volunteer and travel to exotic locations; keep current in your technical focus, follow industry trends; publish in IEEE Journals and magazines.

Network & Exchange Information at:

- Technical Conference Listing - search through the conference database to find the next IEEE-sponsored conference/symposia in your area of expertise;
- Local section and Society chapter and affinity group meetings;
- Fun social events.

Discount for Graduating Student Members:

- IEEE student members who graduate and are elevated to full IEEE membership will automatically receive a one-year discount of 50% off of the full higher grade IEEE and Society membership dues rates upon renewal.

New Member Grade for Grad Students – In 2007, a new Graduate Student Member (GSM) grade goes into effect, and the IEEE will make all the changes necessary for those who qualify. Essentially, GSMs continue to pay the low student dues rate, but will be able to vote in IEEE elections (unlike student members) and will be eligible to hold volunteer positions previously restricted to member grade or higher in IEEE sections, chapters, and the affinity groups of GOLD and Women in Engineering. If you have any queries, or for further details, contact IEEE Member Services (Tel: +1 732 981 0060 or E-mail: member-services@ieee.org).

Ravi M. Todi
EDS IEEE GOLD Representative
IBM
East Fishkill, NY, USA

How to Form an IEEE Student Branch and Student Branch Chapter

An IEEE Student Branch gives students the opportunity to meet and learn from fellow students, as well as faculty members and professionals in the field. A good IEEE Student Branch can be one of the most positive elements in an Electrical Engineering, Computer Engineering or Engineering Technology department. IEEE Student Branches are established at over 1,000 universities and colleges throughout the world. Student Branch activities offer numerous educational, technical, and professional advantages of IEEE membership through special projects, activities, meetings, tours and field trips.

Establishing an IEEE Student Branch requires the signatures of 20 IEEE Student members on a petition. The petition must specify the name of the Branch, and the names of the Interim Student Chair and faculty member who will serve as Counselor of the Branch. The petition must also be approved by the Department Chair and two faculty members, who are also IEEE members above student grade. Submit the petition to IEEE Student Services to begin the approval process, which includes verification of the IEEE membership of the students and the faculty members on the petition, review of the programs offered at the educational institution, review and approval by the IEEE Regional Director, the Regional Student Activities Committee Chair and the IEEE Regional Activities Board (RAB). If further information is required, please contact: IEEE Student Services, Phone +1 732 562 5527/5392, Fax +1 732 463 3657 or e-mail: student-services@ieee.org

Once a university/college has established an IEEE Student Branch, an affiliation can be made with one or more of IEEE's technical societies to form a Student Branch 'Chapter'. There are currently over 300 IEEE Student Branch Chapters, with the Electron Devices Society having 10 at various institutions in a number of regions. The requirements for the establishment of an IEEE Student Branch Chapter for EDS are as follows:

- A petition by not less than twelve (12) Student Branch members, who are members of the IEEE technical Society, must be submitted to Spring Shen of the EDS Executive Office at 445 Hoes Lane, Piscataway, NJ 08854 USA or via fax at 732-235-1626.
- The petition must specify the name of the Student Branch, the name of the technical Society with which the Student Branch Chapter will be affiliated, the name of the interim Branch Chapter Chair and the name of the faculty Advisor, who must be a member of IEEE and the technical Society above student grade.
- After the Advisor and the IEEE Student Branch Executive Committee have approved the petition, it should be sent to the EDS Executive Office.
- Upon receipt of the petition, the EDS Office will forward it to IEEE Student Services to verify the IEEE and technical Society membership of individuals who signed the petition. If the petition is in order, Student Services staff will take the necessary action to obtain formal approval of the petition by the Society President, the Regional Director and the Regional Student Activities Committee Chair. Student Services staff will acknowledge receipt of the petition and will keep the faculty advisor informed of the status of the request.

EDS welcomes the formation of new Student Branch Chapters and we look forward to hearing from you. If you have any further questions, please contact Spring Shen (spring.shen@ieee.org).

Regional and Chapter News

USA, Canada & Latin America (Regions 1-6, 7 & 9)

2008 ISPSD

- by Don Disney

The 20th Annual International Symposium on Power Semiconductor Devices and ICs (ISPSD) will be held May 18–22, 2008, in Orlando, Florida, USA. This conference is the premier forum for technical discussions in all areas of power semiconductor devices, power integrated circuits, hybrid packaging arrangements, and power IC applications. This is a truly international conference, with a venue that rotates on a three-year cycle among North America, Europe, and Asia. The 2008 conference will be located just outside the entrance to the Walt Disney World Resort in Orlando, Florida.

To submit an abstract for consideration, please visit the conference website: www.ecse.rpi.edu/conf/ispsd08 or contact the conference General Chair, Prof. T. Paul Chow (chowt@rpi.edu) or the Technical Chair, Dr. Mohamed Darwish (mohamed.darwish@fultec.com). All abstracts must be submitted by October 21, 2007.

EDS DL Visits the ED Central North Carolina Chapter

- by Albert Wang

Prof. Numan Dogan (front-left), Dimitrios Efstathiou (standing, left-fourth) and Albert Wang (standing, right-third)

Prof. Albert Wang of the Illinois Institute of Technology and EDS Vice-President of Membership, visited the ED/SSC/MTT Central North Carolina Chapter and delivered a Distinguished Lecturer (DL) seminar on April 20, 2007. The DL seminar was held at the Analog Devices Inc. (ADI) Design Center in Greensboro, North Carolina. Prof. Wang was hosted by the Chapter Chair, Dimitrios Efstathiou of ADI, and Prof. Numan Dogan of North Carolina A&T University (NCATU). Wang's DL talk, entitled "Advanced ESD Protection Design for RF ICs", discussed the emerging challenges in ESD-protected RF IC designs ranging from ESD protection theory to new RF ESD protection design techniques to practical design examples. About thirty people, including practice engineers, professors and students from ADI, RF Micro Devices and NCATU, etc, attended the seminar. The DL seminar was followed by discussions on various IC design topics and IEEE society activities.

ED/CPMT Orlando

- by Slavica Malobabic

On January 19th, over one hundred graduate students and professors attended Dr. Steven Voldman's talk on electrostatic protection discharge in semiconductor technology. The technical seminar entitled "Electrostatic Discharge (ESD) in the Nanoelectronic Era" was organized by the ED/CPMT Orlando Chapter and the School of Electrical Engineering and Computer Science at the University of Central Florida (UCF), Orlando, with help from the IEEE UCF Student Chapter and the ESD Association.

Dr. Voldman is an IEEE Fellow for "Contributions in ESD protection in CMOS, Silicon On Insulator (SOI) and Silicon Germanium (SiGe) Technology" and he is a member of the IBM Burlington Vermont technology team. He is the founder of the "ESD on Campus" lecture program in which he provides lectures internationally to encourage understanding of the field of electrostatic discharge, electrical overstress and latchup in today's materials, electronic components, and electrical systems. Dr. Voldman is an author of a three book series, the first one on ESD physics, ESD: Physics and Devices; a second text on ESD circuits, ESD: Circuits and Devices, and a new text ESD: RF Technology and Circuits, as well as a contributor to the text Silicon Germanium: Technology, Modeling and Design. He has written over 150 technical papers, and recipient of 160 issued US patents in the area of semiconductor technology, CMOS latchup and ESD.

For additional information contact Slavica Malobabic at smalobabic@ieee.org.

Dr. Steven H. Voldman, Dr. J.J. Liou (5th & 6th from left), as well as students and faculty of the University of Central Florida (UCF)

EDS DL Visits the ED/CPMT Orlando Chapter

- by Slavica Malobabic

The ED/CPMT Orlando Chapter and the School of Electrical Engineering and Computer Science at the University of Central Florida (UCF), Orlando, with help from the IEEE UCF Student Chapter in Orlando, Florida, have had a great pleasure to host EDS Distinguished Lecturer, Dr. Ortiz Conde. On April 11, a technical seminar entitled "Compact modeling of modern MOSFETs" took place at UCF, Orlando. Professor Ortiz Conde presented an overview of MOSFET models available and up-to-date description of modern multi gate MOSFETs and their compact modeling. Prof. Ortiz Conde is with the Department of Electronics at Universidad Simón Bolívar, Caracas, Venezuela. He has authored numerous papers in national and international conferences and a textbook, Analysis and Design of MOSFETs: Modeling, Simulation and Parameter Extraction.

IEEE EDS Distinguished lecturer Dr. Ortiz Conde (right) and Dr. J.J. Liou (left) at the UCF talk

Very active discussion by the graduate students and professors took place during the questions and answers session.

For additional information contact Slavica Malobabic at smalobabic@ieee.org.

~ Ibrahim M. Abdel-Motaleb, Editor

2007 WMED

- by Steve Groothius

Dear Fellow IEEE Members,

The Fifth Annual IEEE Workshop on Microelectronics and Electron Devices (WMED), held at Boise State University, Boise, Idaho, on April 20, 2007, held at Boise State University, Boise, Idaho, on Friday, April 20, 2007, proved to be a valuable experience for everyone who attended. It provided a forum for 150+ attendees who were interested in reviewing and discussing all aspects of microelectronics including processing, electrical characterization, design, and new device technologies. Even after the workshop, the 2007 IEEE WMED website can give you a feeling for the details and environment of the workshop through the uploaded presentation copies and photographs of the speakers and attendees. The website can be found at: http://www.ewh.ieee.org/r6/boise/wmed2007/WMED2007.htm

Dr. Hans Stork (2007 IEEE WMED Keynote Speaker) explains some of the barriers and solutions in high technology manufacturing

This workshop consisted of 5 invited talks (with 3 IEEE Electron Devices Society Distinguished Lecturers), 15 contributed papers, 3 popular tutorials, as well as 6 student posters in early evening. There were over 40 IEEE members in the audience throughout the day at the workshop. Several talks and posters presented "work-in-progress" research.

Invited WMED Speakers

- Dr. Hans Stork, Sr. VP & Chief Technology Officer, Texas Instruments, Keynote Speaker - "{Technology Challenges for CMOS Density Scaling"
- Dr. Jamal Deen, McMaster University, "Noise Issues in CMOS Devices and Circuits"
- Dr. Juin J. Liou, University of Central Florida - "ESD Protection in CMOS Technology"
- Dr. Prashant Majhi, SEMATECH/Intel - "CMOS Scaling Beyond High k-Metal Gates: Opportunities and Challenges"
- Dr. Nety Krishna, Applied Materials - "New Directions for Process Technologies: Materials, Equipment & Integration"

Invited Tutorials

- Dr. Charlie Zhai, Advanced Micro Devices - "Stress Simulation of Semiconductor Devices and Packaging", The talk focused on the importance of having a strong background in solid mechanics and vision to accurately apply stress simulation principles from the nanometer scale of electronic device features up to the millimeter scale of semiconductor packaging.
- Dr. Kenneth Goodson, Stanford University - "Heat Generation and Transport in Nanometer Scale Transistors", The talk explained the diversity of heat transfer methods in nanometer scale device features, the role of phonons, and the types

The 150+ person audience listened intently and asked some very focused questions for all of our invited speakers

of thermal characterization techniques that are available for both materials and functioning devices. A section of phase change memory development was also discussed.

- Dr. Hanmant Belgal, Intel/IM Flash Technologies, "Reliability of Floating-Gate Flash Memories", This talk provided the insight for determining the key concepts, role of defects, reliability degradation mechanisms, Flash cell structure and operation, media management, and qualification methods.

The success of a regional IEEE workshop like WMED can only be attributed to the hard work and determination of volunteers in the Treasure Valley. The IEEE Boise Electron Devices Society Chapter officers and members believe in the WMED concept and felt that this particular workshop provides the needed interaction between well-known speakers, microelectronic technologists, and future engineers involved in the semiconductor industry, a forum to discuss research, explore new techniques, and to network with local and remote colleagues. We had a continuation of last year's High School Program which brings in key engineers, university students, and experts to discuss items of interest to college-bound students. This year's talks and panel discussion challenged these students to give some serious thought to the career of engineering and science.

The goal of the 2007 IEEE WMED was to provide a set of high quality professional speakers to discuss pertinent issues and concepts within today's semiconductor industry. Judging by the attendee feedback, we are proud to say that the intended goal was met and exceeded.

This Workshop is receiving technical co-sponsorship support from the IEEE Electron Devices Society. We would also like to thank the other financial sponsors, which include Boise State University's College of Engineering, Micron Foundation, the IEEE Boise Section, and the IEEE Boise Electron Devices Society Chapter.

~ Sunit Tyagi, Editor

ED Puebla

- by Claudia Reyes-Betanzo

On January 17, 2007, Professor Juin J. Liou, the IEEE EDS Regions/Chapters Vice-President, visited the ED Puebla Chapter in order to promote chapter activities. At the same time, Professor Liou presented a talk entitled, "Robust Electrostatic Discharge Protection in CMOS Technology", for students and researchers of the National Institute for Astrophysics, Optics and Electronics – INAOE, Puebla Chapter head office. There were about 50 attendees at the talk. The ED Puebla Chapter is grateful to Prof. Liou for his visit and interest in the chapter and his promotion task.

CAS/ED/PEL Venezuela

- by A. Ortiz-Conde

Venezuela's CAS/ED/PEL Joint Chapter continued with its series of seminars and workshops. On Thursday, March 22, 2007, it organized a two-hour technical seminar at Simón Bolívar University, Caracas, entitled "Current Tendencies in Integrated Circuit Design." Dr. Jesús Finol, Senior Engineering Director, Freescale Semiconductor, Arizona, USA, was the special invited speaker for this occasion. Dr. Finol is well known internationally for his R&D activities in IC design for telecommunication systems, such as wireless IC design for cellular telephony, paging systems and two-way radios. He has authored numerous papers in national and international conferences and has been awarded nine U.S. patents in integrated circuit design, with three more pending. The seminar presented a comprehensive and up-to-date description of modern integrated circuit design methodologies, and their connection to the evolution of the semiconductor industry due to aggressive device feature size reduction. More than 50 university faculty members and graduate and undergraduate students attended the seminar. There was a very active participation of the audience, and the many interesting questions and answers motivated additional informal meetings, which took place after the conclusion of the official seminar. The

Prof. Juin J. Liou (right) and Puebla Chapter Chair, Claudia Reyes-Betanzo

Dr. Finol during his presentation at Simón Bolívar University, Caracas, Venezuela

following day, Dr. Finol met with different research groups of Simón Bolívar University to discuss ongoing collaborative activities.

For additional information contact Professor Adelmo Ortiz-Conde at ortizc@ieee.org.

~ Jacobus W. Swart, Editor

EUROPE, MIDDLE EAST & AFRICA (REGION 8)

ED Israel

- by Gady Golan

On Wednesday, January 24, 2007, Dr Eyal Brami of Motorola Israel, delivered his lecture "Mobile Display Market Overview Applications" at the Holon Institute of Technology (HIT), Holon, Israel.

Dr. Brami gave a review of the display market, the major driving forces for growth and historical review, styling and other critical features in cell phones. How cell phones and displays are related to each other. Cellular phones market, tiers, variations, their impact on displays in general and displays in cell phones in particular. There were around 80 people attending the lecture.

On Wednesday, April 11, 2007, Dr. Eyal Sharon, Eastronics, Israel, presented his talk on "Trends in Programmable devices - Altera", to around 65 attendees at the Holon Institute of Technology (HIT), Hilon, Israel.

Both talks were chaired by Prof. Gady Golan, EDS Israel Chapter Chair.

2007 ISSS-MDBS

- by Fei Chen

The 4th International Summer School and Symposium on Medical Devices and Biosensors (ISSS-MDBS), sponsored by the IEEE Engineering in Medicine and Biology Society (IEEE-EMBS), will be held at St. Catharine's College, Cambridge University, UK, August 19-22, 2007. The theme is "From Terahertz Imaging to Telehealth Technologies".

Terahertz imaging and spectroscopy techniques have progressed rapidly over the last decade and numerous medical applications are currently being explored. This combined summer school and symposium is intended to promote awareness of terahertz technology in the medical field and to inform terahertz scientists of the latest advancements in medical devices and telehealth, with a view to integrating terahertz technology into medical devices in the future.

In the symposium sessions, invited and contributed talks will describe original work in research and development. There will also be poster sessions of additional contributed work. The summer school sessions will include informative tutorials about the main topics of interest of: Imaging techniques; spectroscopy techniques; medical applications; pharmaceutical applications; wearable medical devices; body sensor networks; low-cost healthcare equipment; standards for healthcare devices; and textile electronics. Laboratory tours will be held on 22 August giving scientists from all backgrounds further opportunities to broaden their knowledge of medical science.

This event directly precedes the 29th Annual International Conference of IEEE-EMBS in Lyon (23-26 August) themed "Sciences and Technologies for Health".

For inquiries, contact: Dr. E. Pickwell-MacPherson (emma@ee.cuhk.edu.hk), Tel: +852 2609-8260 or Prof. Y.T. Zhang (ytzhang@ee.cuhk.edu.hk), Tel: +852 2609-8459.

~ Zhirun Hu, Editor

ASIA & PACIFIC (REGION 10)

ED Japan

- by Atsushi Kurobe

On January 23rd, the annual meeting of the ED Japan Chapter was held in Tokyo. Dr. Atsushi Kurobe, Japan Chapter Chair reported the 2005 activities and the 2006 plan for the Chapter. At the meeting, the 2005 EDS Japan Chapter Student Award was presented to two students for their outstanding activities in the research of electron devices last year. Tetsu Ohtou (Univ. of Tokyo) and Masaharu Kobayashi (Univ. of Tokyo) received the awards for their excellent IEDM papers, "Experimental demonstrations of superior characteristics of variable body-factor (g) fully-depleted SOI MOSFETs with extremely thin BOX of 10 nm" and "Experimental study on quantum structure of silicon nanowire and its impact on nanowire MOSFET and single-electron transistor, " respectively.

The committee meeting of the ED Japan Chapter this January. From right to left, front row: Prof. H. Iwai, Partner and EDS Jr. Past President; Dr. T. Ikegami, Vice Chair of Japan Council; Dr. A. Kurobe, ED Japan Chapter Chair; Dr. T. Sugawara, Secretary of Tokyo Chapter. At the back: Prof. K. Asada, Chapter Operations Committee Chair; Prof. K. Tsutsui, EDS Newsletter Regional Editor; Dr. H. S. Momose, Secretary of the ED Japan Chapter

Following the annual meeting on the same day, the Briefing Session on the 2006 IEDM was held. Six speakers gave summary talks on the highlights of the IEDM. They were "Modeling and simulation" by Dr. M. Hane (NEC Corp.), "Nanodevices" by Dr. K. Uchida (Toshiba Corp.), "III-V and quantum devices" by Prof. K. Yo (Hokkaido Univ.), "CMOS process" by Dr. M. Kase (Fujitsu Ltd.), "CMOS device" by Dr. H. Wakabayashi (Sony Corp.) and "Integrated Circuits" by Dr. Y. Matsui (Hitachi Ltd.). This session has gained widespread popularity among engineers in Japan who are unable to attend the IEDM, since it is an opportunity for them to familiarize themselves with the latest information on electron device technology. This year's Briefing Session was very successful with more than 70 participants.

The committee meeting of the ED Japan Chapter was also held this January. The guests, namely, Dr. Tetsuhiko Ikegami, Vice Chair of Japan Council; Prof. Kunihiro Asada, Chapter Operations Committee Chair; Dr. Tsutomu Sugawara, Secretary of

Tokyo Chapter; Prof. Hiroshi Iwai, EDS Jr. Past President; Prof. Kenji Taniguchi, EDS Kansai Chapter ex-Chair; and Prof. Kazuo Tsutsui, EDS Newsletter Regional Editor, were a source of much valuable advice for the Chapter. The 2005 activities and the 2006 plan for the Chapter were approved at the meeting.

ED Kansai

- by Michinori Nishihara

The ED Kansai Chapter held a Technical Meeting at Osaka University, Nakanoshima Center, Osaka, Japan, on January 26, 2007. Three prestigious lecturers gave presentations on device technology trends reviewing papers presented at the 2006 International Electron Devices Meeting. This is a good opportunity for ED Kansai Chapter members who could not attend IEDM 2006 to learn the most advanced device technology topics. The first talk was on the latest silicon device technology trend by Dr. Tomohiro Yamashita (Renesas Technology Corp.). He described topics about the most advanced device technology including High-k and metal gate technology. The second talk on silicon process technology including gatestack technology was given by Dr. Jiro Yugami (Renesas Technology Corp.) He identified possibility of recent research activities regarding mobility enhancement technique using hybrid orientation and other strained silicon technology. The last speaker was Dr. Yasuhiro Uemoto (Matsushita Electric). He reviewed compound and power semiconductor technology concerning GaN, SiC and other materials. He talked about promising future of GaN power devices for high frequency applications. Prof. Yasuhisa Omura of Kansai Univ. chaired the meeting and the number of participants was 28 including students and researchers from industries.

Technical Meeting at Osaka University, Nakanoshima Center, on January 26, 2007

ED Korea

- by Hyungcheol Shin

For the ED Korea Chapter, there have been several activities, including the following two this year. The first activity is awarding of the best poster papers and the second one is the Distinguished Lecturer Program. These activities are described specifically below.

Best Poster Paper Awards

The IEEE ED Korea Chapter awarded two 'Best Poster Awards' to Koo Bon Tae from the Electronics and Telecommunications Research Institute, and Song Yong Seon from Kyungpook National University, at the 14th Korean Conference on Semiconductors which was held in Jeju, Korea, from February 8-9, 2007. The two papers, "SoC Design of Ground Wave Receiver" written by Koo Bon Tae and "Unintentionally Doped P Type GaN Film on Si Substrate with Extremely High Mole Mobility" written by Song Yong Seon and Lee Dong Sik had been accepted by the 13th conference held in February 2006 and selected as 'Best Poster Papers' by reviewers among its committee.

Koo Bon Tae from Electronics and Telecommunications Research Institute and Yong Yong Seon from Kyungpook National University received Best Paper Awards

Invitation of IEEE Distinguished Lecturer, Prof. Juin J. Liou

We invited an IEEE Distinguished Lecturer, Prof. Juin J. Liou. He received his Ph.D. in electrical engineering from the University of Central Florida, Orlando, in 1987, where he is now a professor. His seminar was held in Seoul National University on January 29, 2007. The title of the seminar was "Robust Electronics Discharge (ESD) Protection in CMOS Technology."

Prof. Shin and Prof. Liou after the seminar

~ Kazuo Tsutsui, Editor

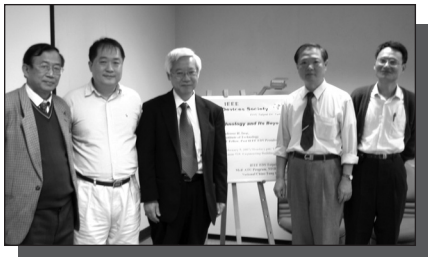
ED Taipei

- by Steve Chung

The ED Taipei Chapter held a DL talk on February, 5, 2007. Prof. Hiroshi Iwai of the Tokyo Institute of Technology, was invited to deliver a lecture entitled "Nano-CMOS Technology and Its Beyond". In the talk, he addressed various technological possibilities, such as new channel materials, III-V high mobility FET, high-k materials, and silicon nanowire transistors, after the conventional CMOS technology reaching its limit. The talk was attended by 60 participants from local universities. Prof. Iwai was then invited by United Microelectronics Corporation (UMC) to have a technical tour to Tainan Science Park in southern Taiwan.

The upcoming international event to be held in Taiwan is the IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC'07). The Conference will be held December 20-22, 2007, hosted by the Southern Taiwan University in Tainan and is the first time to move from Hong Kong to Taiwan. The submission deadline is July 26, 2007. You may take this opportunity to visit the new Science-Based Industrial Park in southern Taiwan, where several major semiconductor manufacturing companies, such as TSMC and UMC, and display manufacturers, such Chi-Mei, are located. Further information

of the EDSSC'07 can be found at http://www2.eecs.stut.edu.tw/~edssc2007/.



ED Taipei held a DL talk on February 5th. Prof. H. Iwai (middle) pictured with (from left to right) Professors. H. L. Huang, Albert Chin, Steve Chung (Chapter Chair), and K. S. Chang-Liaolwc

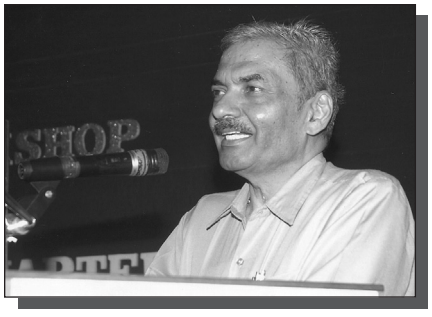
~ Hei Wong, Editor

ED/MTT India

- by Kandala Chari

In the last quarter, the ED/MTT Chapter activities covered the following events:

- The Chapter co-sponsored two international events organized by Electronics Today. First is an international meeting Componex/Electronic India 2007, held in Delhi, on February 6-8, 2007. A major Trade Fair cum Exhibition of Electronic Components, Materials and Production Equipment was held in Pragati Maidan. More than 800 exhibitors from 25 countries participated and the event attracted over 25,000 visitors from India, SAARC and other countries. Concurrent with this event, the International Conference on "Electronic Contract Manufacturing- Indian Perspective" was held on February 7th. This later event featured 15 lead speakers in three sessions touching on various aspects of EMS in India, Contract Manufacturing/EMS scenario and Technologies in CM. The discussions have brought out the EMS opportunities in the Indian subcontinent; supply chain management, IT hardware business area, Equipment supplier matters, China/India modes, stress free singulation of PCB's, High resolution X-ray inspection, Cost effective PCB testing in production and Lead free soldering, etc. The events were also co-sponsored by 23 other organizations/ associations of India and overseas. Mr. S. Swaran, Editor-in-Chief, coordinated these two events.



VLSI Awareness Workshop,VLBJCET, Coimbatore

- The Chapter co-sponsored a one-day VLSI Awareness Workshop on February 23, 2007, organized by the Department of Electronics and Communication Engineering, VLB Janakiammal College of Engineering and Technology (VLBJCET), Coimbatore, Tamil Nadu. The Workshop featured 4 sessions: Analog IC Design by Prof. K. Radhakrishna Rao, TI Bangalore; Digital VLSI Design Flow by Mr. D. S. Harish Ram, ECE Department, VLBJCET; IC Testing by Dr. M. C. Bhuvaneswari; and FPGA Design and Architecture of FPGAs by Mr. G. V. Srinivasa, Agama Design and training centre, Bangalore. The talks covered basics to advanced concepts in digital and analog designs, mixed signal elements, test methodologies for combinational and sequential circuits, FPGA design issues and a demo of FPGA based SOC design flow using embedded tools. The workshop was attended by over 150 students and faculty from 7 engineering and technology colleges in and around Coimbatore.

- The Chapter co-sponsored a 3-day Workshop on "Analog and RF Design" organized by EEE Group, Brita Institute of Technology, Pilani, Rajasthan, on their campus during March 16-18, 2007. The Workshop featured talks by 8 key resource persons from academia and the VLSI industry. Topics covered ranged from VLSI architectural explorations, scalability and power issues, Low power deep submicron, Bandgap and voltage regulators, PLL, Analog Filters and RF Transceivers. Attendees were also given hands-on experience on design tools, Mentor Graphics and Cadence. Dr. Anu Gupta and Dr. Rajnish Sharma of BITS coordinated the event from the BITS side.

- The Chapter has also co-sponsored a workshop cum Symposium on "Electromagnetic Fields in Environment: Implications and Solutions (EMF-ENVIS 2007)" organized by the School of Environmental Sciences, New Delhi, from March 23-24, 2007. Details will follow in the next report.

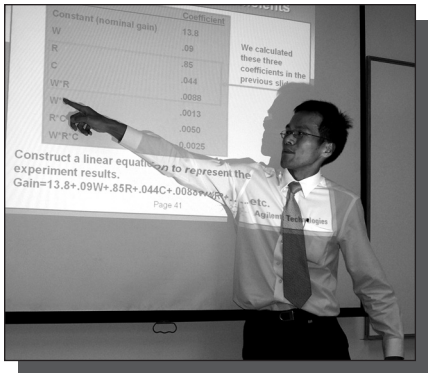
- Under the STAR programme, the chapter co-sponsored the Science Day events and Exhibition held at the KBMC Girls High School Eluru, on February 28, 2007. STAR students won several prizes at the events. Ms. VDPJ Srilakshmi, Ms. M. Ayesha and Ms. P. Padmaja won in essay writing; Ms. K. Nagamani, Ms. P. Bhagyasree, and Ms. Durga Bhavani in science exhibits. Ms. Dharani, faculty and STAR rep, coordinated the events.

MTT/AP/ED Penang

- by Richard Keating

The MTT/AP/ED Penang Chapter is a new Joint Chapter, whose members are mainly from the High Tech companies in and around Penang. The chapter had three excellent talks at the beginning of the year. The first was by Dr. Hong Shi, from the Packaging Technology Department of Altera Corporation. His talk was titled "Signal Integrity in FPGA Devices and applications". It was held at the Penang Skills Development Center in Bayan Lepas on December 28, 2006. Dr. Hong Shi

Dr. Hong Shi presenting his paper



Mr. Ng Aik Chun presenting his talk

Felicitation Ceremony of Dr. Navakanta Bhat at SJCE campus. People presiding are (from left to right) Mr. Karthik Y, Dr. Navakanta Bhat, Prof. M Sukumar and Dr. Ashok Rao

gave a very well received talk on the problems associated with Noise on advanced FPGA devices.

The Chapter was then visited on February 13, 2007, by Dr. Steve C. Cripps, an independent design consultant. His talk was titled "A New Perspective on PA Efficiency Enhancement Techniques". This was Dr. Cripps' second presentation to our chapter, having also presented in 2006.

Ng Aik Chun presented his talk on "MMIC Design for Manufacturing Saves Time and Money". Mr. Ng's talk focused on the Design for Manufacturing functions that exist within Agilent ADS software for RF and MMIC design. He is a member of Agilent's EEsof EDA Division. Mr. Ng described the four aspects to the DFM functions of the ADS software.

We would like to thank PSDC and Motorola for their support of our Chapter.

ED SJCE Student Branch Chapter

-by Karthik Y

With the endless pursuits of the zealous students, the ED SJCE Student Branch Chapter, yet again came out with flying colours organizing a series of workshops and talks, thus standing true to the words 'Redefining Technicality'. The ED SJCE, which has always strived to hone the technical skills of the students, has now proved to be a forum to celebrate the vitality of technology. The major events held this semester were:

Felicitation of Dr. Navakanta Bhat:
The feather to the cap of the ED SJCE Student Branch Chapter this year came with the Felicitation of Dr. Navakanta Bhat, Prof., IISc, Bangalore (also one of the chapter mentors of IEEE EDS SJCE) on March 17, 2007. The ED SJCE student chapter took an opportunity to felicitate Dr. Navakanta Bhat who was awarded the SATHISH DHAWAN AWARD for his outstanding research work for the government of Karnataka. The ceremony was presided by Dr. Navakanta Bhat, Dr. Ashok Rao, Former head, CEDT (Centre for Electronics Design and Technology), Prof. M. Sukumar, Head of the Department of Instrumentation Technology, SJCE and Mr. Karthik Y, Chairman, EDS SJCE Student Branch Chapter. Dr. C. R. Venugopal, Chapter counselor of the ED SJCE, also graced the occasion.

The felicitation was followed by an informative talk by Dr. Navakanta Bhat, which gave an insight into "Nanoelectronics, An exploration through the periodic table", regarding the various elements which can be used in silicon fabrication, was indeed thought-provoking. Thus touching on the basic aspects of VLSI, the talk also gave a peek into the developments and the immense research taking place in the world of Nanotechnology, particularly in Nanoelectronics.

This was followed by a general meeting of EDS members with Dr. Navakanta Bhat and Dr. C. R. Venugopal, which emphasized the future plans of EDS. The initiative to have a lab for EDS on the college campus and to arrange for field trips evinced the enthusiasm of the students, though the practical implementation would need tremendous efforts. Thus, Dr. Navakanta Bhat's presence rejuvenated the young minds, infusing new spirits.

Workshop on Basic Electronic Circuits:
The Workshop on the Basic Electronics lab was conducted on March 2, 2007, in the Analog Lab of SJCE. The main aim of this workshop was to introduce the inquisitive students of the circuit branches to hobby circuits, which would not only help the students to experience the practical implementation of their theoretical knowledge, but also help them to explore the various possibilities to build more efficient circuits. The workshop was conducted by Mr. Arun Raj, a 4th semester student of Instrumentation Technology. The circuit the students worked on was a Light Sensitive Burglar Alarm, precisely, a basic Laser security system.

Workshop on Microcontroller 8051:
With Embedded Systems gaining a huge momentum in the present world, it was the perfect time to hold a workshop on 8051 to encourage students to take up hardware programming. The workshop concentrated on the instruction set, the different addressing modes and the other important aspects of the microcontroller. It was made appealing to the

students by first showing them the practicality of the program which was to generate various patterns of light using LEDs. The program written for that was explained on the basis of the experiment, which ensured an interactive and lively crowd.

Role of EDS in CYBERIA '07:
The ED SJCE Student Branch Chapter is organizing two exhilarating hardware events for CYBERIA '07, the national level technical fete of IEEE-SJCE, scheduled to be held from March 22-25, 2007. The two events include IMPEDANCE and µ8X. While Impedance is a hardware designing contest where students are encouraged to come up with an efficient design to realize a particular circuit, µ8X is an assembly language programming contest.

Thus EDS aims at fueling the students to come up with innovative concepts beating the conventional ones. EDS plans to conduct a series of technical events in the future. Encountering new frontiers each year, EDS gets stronger, infusing vibrant aspirations and undeemed spirits among the students, thus trying to groom them and aid them to thrive in this technically challenging world.

REL/CPMT/ED Singapore

- by Alastair Trigg

Electrostatic Discharge (EDS) was the focus of two of our talks during the first quarter of 2007. On February 1st, J.J. Liou of the Department of Electrical and Computer Engineering, University of Central Florida, EDS Distinguished Lecturer, gave a talk on "Robust Electrostatic Discharge (ESD) Protection in CMOS Technology" at Nanyang Technological University (NTU). The talk attracted over 60 participants.

Prof. J.J. Liou (middle) with chapter committee members, K.L. Pey (left) and X. Zhou (right)

Later in the month another Distinguished Lecturer and IEEE Fellow, Steven Voldman of IBM, spoke on "Electrostatic Discharge ESD in the Nano electronic Era", also at NTU. Again the talk was very well attended. The challenge of ESD for current and future generation devices is one that has attracted the attention of many engineers in Singapore both in industry and the academic world.

Earlier in the year on January 25th, Dr. Thomas O'Reilly of MIT, talked on a very different topic, "Interference Lithography, Practice and Applications", in a meeting co-organized with the Singapore Student Chapter of the Optical Society of America. The talk concentrated on practical issues in using interference lithography, the system layout and optimization with photoresist. Dr. O'Reilly described later work which makes use of immersion techniques and provides a smallest feature size of ~ 160 nm. After his one- hour talk, questions and answers with the 30 participants continued for another 30 minutes.

Our Chapter co-sponsored the two-day Symposium of the Singapore MIT Alliance (SMA). This year the symposium focused on "Challenges for Advanced Silicon-Based Devices" and "Nanotechnology on a Silicon Platform". The symposium covered a wide range of topics from relatively conventional but cutting edge semiconductor developments to more "blue skies" work on nanotubes and self organising devices.

During the lunch break of the second day there was a student poster competition at which many of the students considered not only technology but also the commercial and IP aspects of implementing it. After the symposium most of the contributors and organizers attended a dinner held at Haw Par Villa, an early twentieth century theme park dedicated to Chinese mythology. After a traditional Chinese banquet, many of the participants showed off their singing abilities in a karaoke session.

Chapter organizes two major conferences each year, International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA) and the Electronics Packaging Technology Conference (EPTC). This year IPFA will be held in Bangalore, India, a first for the conference. The Conference will be held in July and the closing date for abstract submission has now passed but full information can be found at the website: http://ewh.ieee.org/reg/10/ipfa/html/2007/index.htm.

The abstract submission deadline for EPTC, which will be held in Singapore in December, is May 15, 2007. Full details of EPTC can be found at the website: http://eptc2007.confs.org/.

~ Xing Zhou, Editor

Correction

Correction to the 2006 EDS Education Award Winner article in the April 2007 Issue – Society News section, page 21

The textbook, *Fundamentals of Carrier Transport*, was published in 2000 by Cambridge University Press (not Oxford as stated).

EDS MEETINGS CALENDAR
(As of June 18, 2007)

The complete EDS Calendar can be found at our web site:
http://www.ieee.org/society/eds/meetings/meetings_calendar.xml Please visit!

August 16 - 17, 2007, T **IEEE International Symposium on Microwave, Antenna, Propagation and EMC Technologies for Wireless Communications** Location: Dianzi University Hotel, Hangzhou, China Contact: Mengqi Zhou E-Mail: mqzhou@public.bta.net.cn Deadline: 3/31/07 www: www.cie-china.org/mape2007

August 21 - 24, 2007, T **Topical Workshop on Heterostructure Microelectronics** Location: Kazusa Arc, Kisarazu-shi, Chiba, Japan Contact: Takatomo Enoki E-Mail: tenoki@aecl.ntt.co.jp Deadline: 4/9/07 www: http://www.twhm.net/

August 26 - 30, 2007, * **IEEE Non-Volatile Semiconductor Memory Workshop** Location: Hyatt Regency Monterey, Monterey, CA, USA Contact: Stephen Keeney E-Mail: stephen.n.keeney@intel.com Deadline: 5/25/07 www: http://www.ewh.ieee.org/soc/eds/nvsmw/

August 27 - 29, 2007, T **International Symposium on Low-Power Electronics and Design** Location: Embassy Suites, Portland, OR, USA Contact: Anand Raghunathan E-Mail: anand@nec-labs.com Deadline: 3/2/07 www: http://www.islped.org

September 3 - 6, 2007, T **Symposium on Microelectronics Technology & Devices** Location: Rio Othon Palace Hotel, Rio de Janeiro, RJ, Brazil Contact: Jacobus Swart E-Mail: iwpsd@ee.iitm.ernet.in Deadline: 3/26/07 www: www.sbmicro.org.br/sbmicro

September 5 - 7, 2007, T **International Conference on Electrical and Electronics Engineering** Location: Hotel Ejecutivo, Mexico City, Mexico Contact: Arturo Minor Martinez E-Mail: aminor@cinvestav.mx Deadline: 5/21/07 www: iceee.ie.cinvestav.mx

September 9 - 14, 2007, T **International Conference on Noise in Physical Systems and 1/F Fluctuations** Location: National Institute for Youth Education, Shibuya-ku, Tokyo, Japan Contact: Munecazu Tacano E-Mail: tacano@ee.meisei-u.ac.jp Deadline: 1/31/07 www: http://icnf.meisei-u.ac.jp/

September 10 - 14, 2007, T **European Solid-State Device Research Conference** Location: TU Muenchen Arcisstrasse, Munich, Germany Contact: Philip Teichmann E-Mail: teichmann@tum.de Deadline: 4/7/07 www: http://www.essderc.org/

September 10 - 14, 2007, T **International Crimean Microwave Conference "Microwave & Telecommunication Technology"** Location: Sevastopol National Technical University, Sevastopol, Ukraine Contact: Pavel Yermolov E-Mail: 10.99057@gmail.com Deadline: 5/11/07 www: www.crimico.org

September 15 - 17, 2007, @ **IEEE International Symposium on Semiconductor Manufacturing** Location: Marriott Santa Clara, Santa Clara, CA, USA Contact: Maria Hess E-Mail: maria.hess@amd.com Deadline: 5/25/07 www: www.issm.com

September 16 - 19, 2007, T **IEEE Custom Integrated Circuits Conference** Location: Double Tree Hotel, San Jose, CA, USA Contact: Melissa Widerkehr E-Mail: melissaw@widerkehr.com Deadline: 4/19/07 www: http://www.ieee-cicc.org

September 16 - 21, 2007, T **International Conference on Nitride Semiconductors** Location: MGM Grand Hotel, Las Vegas, NV, USA Contact: TMS Meeting Services E-Mail: mtgserv@tms.org Deadline: 4/2/07 www: www.tms.org/Meetings/specialty/icns7/home.html

September 17 - 21, 2007, T **International Conference on Electromagnetics in Advanced Applications** Location: Torino Incontra Congress Center, Torino, Italy Contact: Guido Lombardi E-Mail: info@iceaa.polito.it Deadline: 2/23/07 www: www.iceaa.polito.it

September 17 - 19, 2007, T **European Conference on High Temperature Electronics** Location: Oxford, United Kingdom Contact: E-Mail: Not Available Deadline: Not Available www: Not Available

September 17 - 20, 2007, T **IEEE International Seminar/Workshop on Direct and Inverse Problems of Electromagnetic and Acoustic Wave Theory** Location: Inst. Of Applied Prob. Of Mechanics & Math (NASU), Lviv, Ukraine Contact: Mykhalyo Andriychuk E-Mail: andr@iapmm.lviv.ua Deadline: 7/15/07 www: Not Available

September 18 - 21, 2007, T **International Conference on Solid-State Devices and Materials** Location: Tsukuba International Congress Center, Tsukuba, Ibaraki, Japan Contact: Naomi Kutsuna E-Mail: ssdm@intergroup.co.jp Deadline: 5/10/07 www: www.ssdm.jp

September 19 - 21, 2007, T **International Conference on Microelectronics and Computer Science** Location: Technical University of Moldova, Chisinau, Moldova Contact: Ion Tiginyanu E-Mail: tiginyanu@asm.md Deadline: 6/1/07 www: www.icmcs.utm.md/

September 25 - 27, 2007, @ **IEEE International Conference on Simulation of Semiconductor Processes and Devices** Location: TU Vienna, Vienna, Austria Contact: Tibor Grasser E-Mail: Grasser@iue.tuwien.ac.at Deadline: 3/1/07 www: http://www.sispad.org

September 26 - 28, 2007, T **International Symposium on Advanced Gate Stack Technology** Location: Westin City Center Hotel, Dallas, TX, USA Contact: Cassandra Muse E-Mail: cassandra.muse@sematech.org Deadline: Not Available www: sematech.org

September 30 - October 3, 2007, T **IEEE Conference on Intelligent Transportation Systems** Location: Hilton Hotel, Bellevue, WA, USA Contact: Paul Kostek E-Mail: p.kostek@ieee.org Deadline: 3/1/07 www: http://www.ewh.ieee.org/tc/its/

September 30 - October 2, 2007, @ **IEEE Bipolar/BiCMOS Circuits and Technology Meeting** Location: Boston Marriott Long Wharf, Boston, MA, USA Contact: Janice Jopke E-Mail: ccs@mn.rr.com Deadline: 3/1/07 www: www.ieee-bctm.org

October 1 - 4, 2007, * **IEEE International SOI Conference** Location: Miramonte Resort & Spa, Indian Wells, CA, USA Contact: Bobbi Armbruster E-Mail: bobbi@bacminc.com Deadline: Not Available www: www.soiconference.org

October 2 - 5, 2007, T **International Conference on Advanced Thermal Processing of Semiconductors** Location: Grand Hotel Baia Verde, Cannizzaro, Catania, Sicily, Italy Contact: Bo Lojek E-Mail: blojek@atmel.com Deadline: 5/31/07 www: www.ieee-rtp.org

October 3 - 5, 2007, * **International Semiconductor Conference** Location: Sinaia Hotel, Sinaia, Romania Contact: Cristina Buiculescu E-Mail: cas@imt.ro Deadline: 6/10/07 www: www.imt.ro/cas

October 7 - 12, 2007, T **Symposium on ULSI Process Integration** Location: Hilton, Washington, DC, USA Contact: Cor Claeys E-Mail: c.claeys@ieee.org Deadline: 5/26/07 www: N/A

October 8 - 10, 2007, T **International Workshop on Computational Electronics** Location: Campus Center of University of Massachusetts, Amherst, MA, USA Contact: Massimo Fischetti E-Mail: fischett@ecs.umass.edu Deadline: 6/1/07 www: www.ecs.umass.edu/iwce

October 8 - 10, 2007, T **IEEE International Conference on Computer Design** Location: Squaw Creek Resort, Squaw Valley, CA, USA Contact: Kevin Rudd E-Mail: Kevin.w.rudd@intel.com Deadline: Not Available www: www.iccd-conference.org

October 8 - 10, 2007, T **IEEE European Microwave Integrated Circuits Conference** Location: ICM, Munich International Congress Centre, Munich, Germany Contact: Fred Schindler E-Mail: m.schindler@ieee.org Deadline: 2/25/07 www: www.eumweek.com

October 8 - 12, 2007, T **European Symposium on Reliability of Electron Devices, Failure Physics and Analysis** Location: Palatium-Arcachon, Bordeaux, France Contact: M. Garcia E-Mail: esref@adera.fr Deadline: 3/16/07 www: http://esref07.ixl.fr/welcome/index.html

October 14 - 17, 2007, * **IEEE Compound Semiconductor IC Symposium** Location: Hilton Portland & Executive Tower, Portland, OR, USA Contact: Mohammad Madihian E-Mail: madihian@nec-labs.com Deadline: 5/7/07 www: http://www.csics.org/

October 15 - 16, 2007, T **International SoC Design Conference** Location: Coex Conference Center, Seoul, Korea Contact: Seongsoo Lee E-Mail: sslee@ssu.ac.kr Deadline: Not Available www: www.isocc.org

October 15 - 17, 2007, T **IFIP International Conference on Very Large Scale Integration** Location: Georgia Tech Hotel, Atlanta, GA, USA Contact: Vincent Mooney, III E-Mail: vlsisoc2007@gatech.edu Deadline: 4/9/07 www: www.vlsisoc2007.gatech.edu

October 15 - 18, 2007, * **IEEE International Integrated Reliability Workshop** Location: Stanford Sierra Conference Centers, South Lake Tahoe, CA, USA Contact: Roy and Becky Walker E-Mail: roy@sar101.com Deadline: 7/13/07 www: www.iirw.org

October 28 - 31, 2007, T **IEEE International Conference on Sensors** Location: Hyatt Regency Atlanta, Atlanta, GA, USA Contact: Katharine Cline E-Mail: kkcline@pmmiconferences.com Deadline: 4/3/07 www: www.ieee-sensors2007.org

November 4 - 8, 2007, T **IEEE International Conference on Computer Aided Design** Location: DoubleTree Hotel San Jose, San Jose, CA, USA Contact: Kathy Embler E-Mail: kathy@dac.com Deadline: 4/11/07 www: www.iccad.com

November 5 - 8, 2007, T **International Microprocesses and Nanotechnology Conference** Location: Kyoto International Conference Hall, Kyoto, Japan Contact: E-Mail: Not Available Deadline: 6/30/07 www: www.imnc.jp

November 6, 2007, T **IEEE Electron Devices Activities in Western New York Conference** Location: University of Rochester, Rochester, NY, USA Contact: Karl Hirschman E-Mail: kdhemc@rit.edu Deadline: Not Available www: Not Available

November 10 - 13, 2007, T **Non-Volatile Memory Technology Symposium**, Location: Hyatt Regency Albuquerque, Albuquerque, NM, USA, Contact: Kristy Campbell, E-Mail: kriscampbell@boisestate.edu, Deadline: 6/2/07, www: coen.boisestate.edu/nvmts

December 3 - 7, 2007, T **International Photovoltaic Science & Engineering Conference** Location: Fukuoka International Congress Center, Fukuoka, Japan Contact: Yoshio Ohsita E-Mail: pvsec17@toyota-ti-ac.jp Deadline: 7/15/07 www: http://www.pvsec17.jp

December 6 - 8, 2007, * **IEEE Semiconductor Interface Specialists Conference** Location: Key Bridge Marriott, Arlington, VA, USA Contact: Dina Triyoso E-Mail: dina.triyoso@freescale.com Deadline: 7/21/06 www: www.ieeesisc.org

December 10 - 12, 2007, * **IEEE International Electron Devices Meeting** Location: Washington Hilton and Towers, Washington, DC, USA Contact: Phyllis Mahoney E-Mail: phyllism@widerkehr.com Deadline: June 22, 2007 www: http://www.ieee.org/conference/iedm

December 12 - 14, 2007, T **International Semiconductor Device Research Symposium** Location: Stamp Student Union, Unv. Of Maryland, College Park, MD, USA Contact: Phillip Thompson E-Mail: phillip.thompson@nrl.navy.mil Deadline: Not Available www: www.ece.umd.edu/isdrs2007

December 12 - 14, 2007, T **International Conference on Field-Programmable Technology**, Location: Kitakyusyu International Conference Center, Kitakyusyu, Japan, Contact: Tadao Nakamura E-Mail: nakamura@archi.is.tohoku.ac.jp, Deadline: 6/25/07, www: www.kameyama.ecei.tohoku.ac.jp/icfpt07

December 15 - 19, 2007, T **Advanced Workshop on 'Frontiers in Electronics'**, Location: Park Royal Hotel, Cozumel, Mexico, Contact: Michael Shur, E-Mail: shurm@rpi.edu, Deadline: 10/1/07, www: nina.ecse.rpi.edu/shur/wofe07/

December 16 - 20, 2007, T **International Workshop on the Physics of Semiconductor Devices** Location: Indian Inst. Of Tech., Bombay & TIFR Mumbai, Mumbai, India Contact: V.Ramgopal Rao E-Mail: rrao@ee.iitb.ac.in Deadline: 5/15/07 www: http://www.iwpsd.net/

December 20 - 22, 2007, T **IEEE Conference on Electron Devices and Solid State Circuits** Location: Southern Taiwan University of Technology, Tainan, Taiwan Contact: T.K. Chiang E-Mail: tkchiang@mail.stut.ed.tw Deadline: 7/29/07 www: www2.eecs.stut.edu.tw/~edssc2007

December 20 - 23, 2007, T **IEEE International Workshop and Tutorials on Microtechnologies in Electronics** Location: Novosibirsk State Technical University, Novosibirsk, Russia Contact: Alexander Gridchin E-Mail: ieeensk@yandex.ru Deadline: 8/20/07 www: Not Available

December 29 - 31, 2007, T **International Conference on Microelectronics** Location: Nile Hilton, Cairo, Egypt Contact: Mohab Anis E-Mail: manis@vlsi.uwaterloo.ca Deadline: 6/15/07 www: www.ieee-icm.com

January 22 - 24, 2008, T **IEEE Radio and Wireless Symposium** Location: Long Beach Convention Center, Orlando, FL, USA Contact: Tom Weller E-Mail: weller@eng.usf.edu Deadline: Not Available www: http://www.radiowireless.org

Report on Prof. Hiroshi Iwai's visit to the ED Bangladesh Chapter

- by Anisul Haque

Prof. Hiroshi Iwai, Tokyo Institute of Technology, and EDS Distinguished Lecturer, visited the Bangladesh Chapter December 19-23, 2006. He formally inaugurated the ED Bangladesh Chapter on December 19th at the East West University, Dhaka. Prof. M. Ataul Karim, Vice President for Research, Old Dominion University, USA, was also present at the inaugural ceremony as the special guest. Prof. Mohammad Musa, Vice Chancellor (Acting), East West University, chaired the program and Prof. Anisul Haque, Chair, ED Bangladesh Chapter, delivered the welcome address. The program was attended by more than 100 participants including around 15 EDS members and 20 IEEE student members.

Prof. Iwai also presented a technical talk on Electronic Devices for Human Society after the inaugural. The talk generated a lot of interest, particularly among the EDS and student members.

Prof. Iwai attended the 4th International Conference on Electrical and Computer Engineering (ICECE 2006) held in Dhaka, December 19–21. He presented a key note talk on December 21st. The title of his talk was Nano CMOS Technology and Manufacturing and his presentation was followed by an exciting question and answer session.

Prof. Iwai visited the Bangladesh University of Engineering & Technology (BUET) on December 20th . He met Prof. S. P. Majumder, Head, EEE Department, who showed him around the various labs and resources of the department. Prof. Iwai was also introduced to Prof. A. M. M. Saifullah, Vice Chancellor, BUET. They discussed a possible collaboration between Bangladeshi and Japanese universities in the electron device area.

Prof. Iwai delivering his talk at the inaugural ceremony of the ED Bangladesh Chapter on December 19, 2006

Guests at the inaugural ceremony of the ED Bangladesh Chapter on December 19, 2006

Prof. Iwai's visit to BUET on December 20, 2006. From left to right: Prof. A. B. M. Harun Ur-Rashid, Secretary/Treasurer, ED Bangladesh, Prof. Anisul Haque, Chair, ED Bangladesh, Prof. Hiroshi Iwai, Prof. Satya Prasad Majumder, Head, EEE, BUET, and Prof. A. M. M. Safiullah, Vice Chancellor, BUET