



# IEEE ELECTRON DEVICES SOCIETY

## Newsletter

JULY 2008 VOL. 15, NO. 3 ISSN:1074 1879

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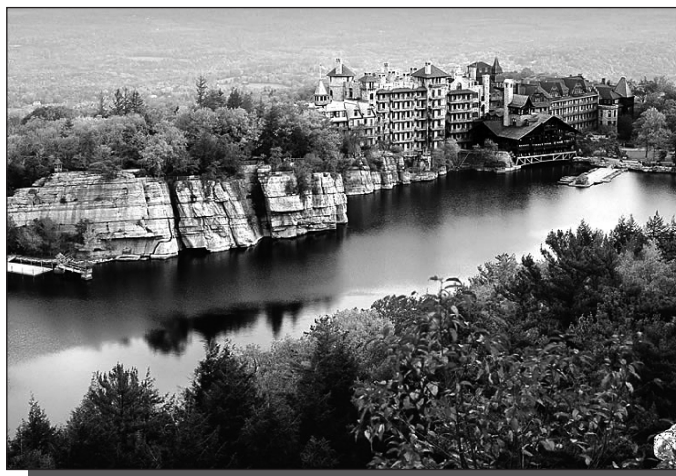
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## 2008 IEEE INTERNATIONAL SOI CONFERENCE



*Mohonk Mountain House, New Paltz, New York*

The premier conference dedicated to current trends in Silicon-On-Insulator technology will be held October 6 – 9, 2008, at the Mohonk Mountain House in the beautiful Hudson River Valley in upstate New York. The conference will be preceded by a one-day tutorial Short Course on Monday, October 6th and will also feature a half-day educational class focusing on the fundamentals of SOI technology.

The conference was established with the support of IEEE to provide a forum for open discussion in all areas of silicon-on-insulator technologies and their applications. Ever increasing demand and advances in this technology make it essential to meet to discuss new gains and accomplishments, as well as to consider the new developments introduced in original papers presented at the conference. The 34th annual IEEE International SOI Conference will begin with a half-day plenary session

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#### YOUR COMMENTS SOLICITED

Your comments are most welcome. Please write directly to the Editor-in-Chief of the Newsletter at [nstojadinovic@elfak.ni.ac.yu](mailto:nstojadinovic@elfak.ni.ac.yu)

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Elected for a three-year term (maximum two terms) with 'full' voting privileges

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## CONTRIBUTIONS WELCOME

Readers are encouraged to submit news items concerning the Society and its members. Please send your ideas/articles directly to either the Editor-in-Chief or appropriate Editor. The e-mail addresses of these individuals are listed on this page. Whenever possible, e-mail is the preferred form of submission.

## Newsletter Deadlines

Issue	Due Date
January	October 1st
April	January 1st
July	April 1st
October	July 1st

The EDS Newsletter archive can be found on the Society web site at <https://www.ieee.org/portal/pages/society/eds/pubs/newsletters/newsletter.html>. The archive contains issues from July 1994 to the present.

**IEEE Electron Devices Society Newsletter** (ISSN 1074 1879) is published quarterly by the Electron Devices Society of the Institute of Electrical and Electronics Engineers, Inc. Headquarters: 3 Park Avenue, 17th Floor, New York, NY 10016-5997. Printed in the U.S.A. One dollar (\$1.00) per member per year is included in the Society fee for each member of the Electron Devices Society. Periodicals postage paid at New York, NY and at additional mailing offices. **Postmaster:** Send address changes to IEEE Electron Devices Society Newsletter, IEEE, 445 Hoes Lane, Piscataway, NJ 08855.

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## EDS PRESIDENT'S MESSAGE



Cor L. Claey's

As the first President elected from Region 8 (Europe, Africa and Middle East) it is a great honor and privilege to serve for 2008 and 2009 as President of the Electron Devices Society. Being a volunteer since 1995 and having enjoyed serving in a variety of positions I am well familiar with the objectives of the Society aiming at giving value to its members. It is a privilege, but at the same time a great challenge, as many things are rapidly changing since electronic communication has entered the scene, offering great new possibilities which were not available before. Strategies set out by the Junior and Senior Past Presidents, Ilesanmi Adesida and Hiroshi Iwai, respectively, will be further worked out, fine-tuned and adopted where needed in order to enhance benefits for Society members. The key question to answer is how we can best serve our members today and in the future, both from a professional and personal perspective. The fact that the Society is financially healthy enables us to start-up new initiatives and focus on serving our members.

The Field of Interest of the Society has been updated and is now taking into account emerging technologies required for new application fields such as environmental control, automotives, ambient intelligence, domotics, health care, infotainment, renewable energy, etc. Electron Devices has been and will remain open for new device technologies entering the research era. To cover the three main lines of the Research Agenda, i.e., More Moore (scaling), Beyond CMOS (spintronics, quantum computing, molecular electronics, bio-chips, carbon nanotubes, grapheme, etc), and More Than Moore (heterogeneous integration, 3D wafer level packaging, etc), the

Society members are becoming more multi-disciplinary, which should also be reflected in the Society key activities such as publications and conferences. EDS should become a home base for this new type of engineer. In order to get a much better feeling of the expectations of the individual members and non-members, a survey was developed and will have been distributed via e-mail prior to the mailing of this newsletter issue. This initiative is considered as very important and of great value for determining the future orientation of the Society and the technical fields to be covered.

A key aspect of the Society is the Globalization strategy, which was initiated several years ago and resulted in a large number of new Chapters in countries like China and India. Both countries are important because of their increasing activities in the field of semiconductor research and manufacturing. Once the momentum is given, the action continues almost automatically. The focus is not only on Region 10, but much action is also on going to form new Chapters in Region 9. Additional initiatives will also be taken for the other Regions. In 2007, 18 new Chapters were formed and discussions are on going with about 40 potential new Chapters. Currently, we have 142 Chapters worldwide, making Electron Devices one of the most active societies within IEEE from a Chapters point of view. We all know that not only the number of Chapters is important, but essential is the degree to which these Chapters are active and serving the members. I am therefore very pleased to notice that there is a strong increase in the use of the Distinguished Lecturer (DL) Program and that more and more mini-colloquia are organized. This necessitated increasing the budget for these activities. Similar to 2007, the subsidy to the chapters will again be 50% higher this year. The globalization effect is also reflected in the increase of non USA members in the different admin-

istrative and technical committees. One of the two annual EDS Executive and Administrative Committee meetings is always held outside the United States. This year the mid-year meeting will be in Athens, Greece, while for 2009, it is scheduled to take place in India.

Great successes of the Society are the Conferences and Workshops. Last year, EDS supported 124 conferences, including 22 financially sponsored ones. The Vice Presidents of Meetings and Technical Activities are working on researching and gathering information to get a better view on the topics covered, the geographical distribution, the meeting calendars and the success of the meetings. A strategy will be worked out to streamline the conferences offered and to avoid too much overlap and/or overkill. The above-mentioned membership survey will be used to detect new or emerging technical areas which could be addressed in the future.

The Society has over the years been strongly interacting with the academic world and that community is well convinced of the benefits of joining the Society. Last year a new Education Award was established. Different initiatives are in place to increase the involvement of students and several new student chapters were formed last year. The Fellowship Program is available to both Graduate and Master students. However, it is as important for the Society to establish strong interactions with the industrial community and the engineers in the field. Initiatives are therefore taken to also better serve these members by organizing the appropriate type of events, to have them well represented in the different committees and to better inform them on their eligibility to be nominated for several of the existing awards. Similar actions are taken at the IEEE level as reflected in the increasing number of IEEE Fellows coming from industry.

*(continued on page 9)*

# UPCOMING TECHNICAL MEETINGS

## 2008 IEEE BIPOLAR/BICMOS CIRCUITS AND TECHNOLOGY MEETING (BCTM)

The 2008 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) will be held from Monday, October 13 until Thursday, October 16, 2008, at the Portola Plaza Hotel in beautiful Monterey, California. This year, the BCTM conference will be collocated with the 2008 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS).

Anyone interested in leading edge processes, devices, and circuits used in state of the art telecommunication systems and power control systems will not want to miss this conference. Bipolar and BiCMOS technologies, particularly SiGe HBT BiCMOS technologies, continue to play a key role in these systems.

Papers covering the design, performance, fabrication, testing, modeling, and application of bipolar and BiCMOS integrated circuits, bipolar phenomena, and discrete bipolar devices are presented.

Situated along the coast of California just 115 miles from San Francisco, Monterey is easily accessible from multiple airports. Monterey is the home of the world-class Monterey Bay Aquarium, located on the street immortalized in John Steinbeck's novel *Cannery Row*, and features renowned events such as the annual Monterey Jazz Festival. The area has numerous attractions including the Big Sur, Fisherman's Wharf, Pebble Beach Golf Resort, along with wonderful restaurants, hotels, galleries, and shops. You are also just a short drive away from some of California's finest wineries.

The conference starts with a one day short course followed by two full days of contributed and invited

papers including a special session on Emerging Technologies. The BCTM Banquet will be held on Tuesday evening at the Chateau Julien Wine Estate. Following the conference on Thursday, there will be a workshop on compact modeling for RF/Microwave applications organized by TU Delft.



*Portola Plaza Hotel, Monterey, California*

We are fortunate to have Dr. Gil Amelio as this year's keynote speaker. Dr. Amelio is the CEO of Jazz Semiconductor and he will discuss "Technology Convergence Creating New Opportunities for Innovation." This is a great opportunity to meet Dr. Amelio and learn about the latest technologies designed to produce analog-intensive mixed-signal (AIMS) semiconductor devices including high performance telecommunication systems.

The short course features five renowned experts on "100 Gbps Ethernet and High-Speed Data Converters". Short course invited talks include: "High-speed SiGe BiCMOS technologies for applications beyond 40 Gb/s", Pascal Chevalier (STMicroelectronics), "High-speed data converters for 10+Gb/s applications", Peter

Schvan (Nortel), and "System architectures and circuits for 100 Gb/s Ethernet applications", Yves Baeyens, Lucent-Alcatel Bell Labs.

The conference also includes a plenary session which features 6 invited talks:

- "Special RF/mWave Devices in Silicon-on-Glass Technology" Lis Nanver (TU Delft)
- "Silicon Front-End Integration" J. Costa (RFMD)
- "High-Speed A/D & D/A Conversion: A Survey" J.B. Begueret (IMS Bordeaux)
- "Digital Control Power - The Key to Intelligent Energy Efficiency" Manfred Schlenk (Infineon)
- "From Measurement to Intrinsic Device Characteristics: Test Structures and Parasitics Determination" F. Pourchon (ST Microelectronics)
- "Highly-Efficient Wideband Monolithic RF Polar Transmitters Using Envelope-Tracking" D. Lie (Texas Tech University)

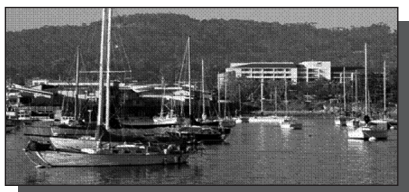
Two days of technical paper sessions, a luncheon with guest speaker, exhibits, and the evening banquet roll out the program. Booths feature the latest products of interest to the bipolar community. The banquet will be held at the Chateau Julien Wine Estate where you will be able to connect with your colleagues and make new acquaintances. We look forward to welcoming you at BCTM 2008. Find full details and registration information for the conference on the BCTM web page (<http://www.ieee-bctm.org/>).

See you in Monterey!

*Marise Bafleur  
2008 BCTM General Chair  
LAAS-CNRS  
Toulouse, France*



# 2008 IEEE COMPOUND SEMICONDUCTOR IC SYMPOSIUM (CSICS)



Portola Plaza Hotel

The 2008 IEEE Compound Semiconductor IC Symposium (CSICS) will be held at the Portola Plaza Hotel and adjacent Monterey Convention Center in beautiful Monterey, CA from October 12-15, 2008. Formerly known as the GaAs IC Symposium, CSICS has over its 30 years history become the preeminent international forum on developments in integrated circuits using compound semiconductors including GaAs, GaN, InP, SiGe and other related materials. Participants' interests span all aspects of the technology from materials issues and device fabrication, through IC design and testing, high volume manufacturing, and system applications. In its earlier years, the Symposium was driven by the high rate of innovation in GaAs materials and devices for high speed digital and emerging wireless applications. Significant funding for these activities came from government and military sponsored research as well as corporate R&D programs. As the markets for compound semiconductor devices and ICs matured, particularly in the area of specialty cellular wireless products like power amplifiers and rf switches, the technology for GaAs ICs reached a more mature phase. Increasingly, newer materials such as GaN, InP, SiGe and other compound semiconductors, as well as CMOS variants targeting ultra high speed and wireless applications, have become the focus for highly innovative and exciting breakthroughs in research and development labs around the world. Today, CSICS draws support from a wide range of corporate, governmental and academic groups located across the globe. This confluence of both

mature and emerging technologies, varied materials and applications thrusts, and the diverse backgrounds of the participants active in these fields continues to lend a vibrance and youthfulness to CSICS much like in the early days of its colorful past.

We are very pleased to announce that CSICS will co-locate with the IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) this year in Monterey. Joint functions including technical sessions, social functions and the exhibition will permit cross-fertilization of ideas between these two technical meetings.

The location for this years Symposium, Monterey, CA, is famous for its natural beauty, history and culture. Local attractions available to our attendees include the world-renowned Monterey Bay Aquarium, Fisherman's Wharf, the Marina, the historic town of Monterey, and of course the stunning scenery throughout the Monterey Peninsula. An easy drive from Silicon Valley and the greater San Francisco area, Monterey has always been one of our most popular conference locations.

## Symposium Highlights

High quality technical papers will be selected from worldwide submissions for oral presentation and publication in the Symposium Digest. Extended versions of selected papers from the Symposium will be published in a special issue of the *IEEE Journal of Solid State Circuits*. For prospective authors and presenting companies, CSICS provides the ideal forum to report your latest results in high-speed digital, analog, microwave/millimeter wave, mixed mode, and optoelectronic integrated circuits. First-time papers concerned with the utilization and application of GaAs, GaN, InP, SiGe, rf CMOS and related semiconductors in military and commercial products are invited. Specific technical areas of interest include

- Innovative RFIC Device & Circuit Concepts
- Millimeter-wave/High-Speed CMOS IC
- Circuit Design & Fabrication
- Manufacturing Technology & Cost Issues
- CAD/CAM/CAT Tools & Techniques
- IC Testing & Methodology
- Packaging Technology
- Reliability
- Advanced Device Applications
- System Applications (e.g., wireless, vehicular, RADAR, military)
- Optoelectronic and OEIC applications

Information on the late News Paper submission procedure can be found on our website [www.csics.org](http://www.csics.org) or by contacting the Technical Program Chair, Marko Sokolich, at [msokolich@hrl.com](mailto:msokolich@hrl.com)

This year, CSICS will offer two short courses which will be held on Sunday, October 12, 2008. The courses are entitled "Phased Arrays - Technology, Systems and Circuits" and "A Modeling Toolbox for RF Designers". For more information, please contact the Short Course Organizer and Technical Program Vice Chairman, Dave Halchin, at [dhalchin@rfmd.com](mailto:dhalchin@rfmd.com). The Symposium will again offer the popular primer course, "Basics of GaAs, InP and SiGe RFICs," an introductory-level class intended for those wishing to obtain a broad overview of RFIC technology. The Sunday evening course will cover materials and processes, device operation, and both analog/microwave and digital ICs. The Course will be tailored to provide the specific background needed for participants to understand and appreciate the papers presented in the Symposium Technical Program.

The CSICS Technology Exhibition will take place in the Monterey Convention Center adjacent to the Portola Plaza Hotel. The close proximity of the Exhibition and the technical sessions will promote a highly integrated

experience for our attendees. The Exhibition will offer our vendors an opportunity to showcase various products and services including specialty semiconductor materials (epitaxy, substrates, high purity gases and related compounds), manufacturing equipment including photolithography, etch, thin films, ion implantation, wafer surface analysis and metrology equipment and services, test and characterization equip-

ment, simulation and modeling software, and complete foundry services for GaAs and related compound semiconductor technologies. More information on the CSICS Exhibition can be found on the website or by contacting the Exhibition Manager, Sue Kingston, at [s.kingston@ieee.org](mailto:s.kingston@ieee.org).

We look forward to seeing you at the 2008 IEEE Compound Semiconductor IC Symposium this October in Monterey, CA!

*William Peatman*  
2008 CSICS Symposium Chair  
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*Marko Sokolich*  
2008 CSICS Technical  
Program Chair  
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Malibu, CA, USA

## 2008 IEEE INTERNATIONAL SOI CONFERENCE

*(continued from page 1)*

followed by two days of oral sessions, a poster session and a late news session. In addition, two Best Paper Awards will be presented at the conference; one for the best oral presentation and one for the best poster presentation.

Participants are free on Wednesday afternoon to explore the Hudson River Valley, get a little work done, or just relax. An evening discussion panel session where attendees are encouraged to share their opinions and expertise will round off Wednesday evening. This year's topic is "Will SOI Enter the Foundry Market?"

Also on Wednesday afternoon, the conference is offering an optional, intermediate-level class intended for individuals from a variety of fields including circuit design, material scientists/engineering, process technology, modeling, and device design. This second SOI fundamentals class will provide attendees improvement and better understanding of their knowledge on SOI devices physics and SOI circuits design. The educational classes consist of two lectures of 1.5 hours each. They will be given by world recognized experts in their respective areas.

The 2008 SOI Conference seeks papers on a wide range of SOI technology including:

- SOI material science/modification, material characterization, manufacture and substrate engineering
- SOI device physics and modeling
- Manufacturability and process integration of SOI devices and circuits.
- SOI design infrastructure
- SOI circuit applications (high-performance MPU, SRAM, ASIC, low power, high-voltage, RF, analog, mixed mode, etc.)
- Double & Multiple Gate/Vertical Channel Structures, other advanced SOI devices
- New SOI structures, circuits, and applications (3D integration, displays, microactuators - MEMS, microsensors, novel memories, optics, etc.)
- SOI reliability issues (hot-carrier effects, radiation effects, high-temperature effects, etc.)
- SEngineered substrates

Abstracts for the SOI 2008 Conference were due May 2, 2008 to the conference manager, by e-mail ONLY to [soipaper@bacminc.com](mailto:soipaper@bacminc.com) in PDF format. Late news papers with exceptional merit will be considered for the Late News session if submitted on or before August 25, 2008.

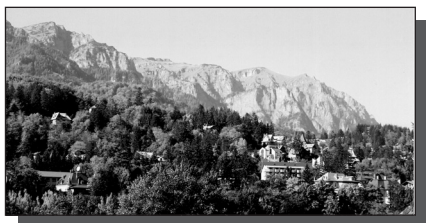
Once again, the popular One-

Day Tutorial Short Course will be offered preceding the 2008 SOI International Conference. Tutorial Short Course instructors have many years of experience in the field of silicon-on-insulator technology. The course is intended to educate attendees in details about current trends and issues in the SOI industry. The 2008 tutorial Short Course is entitled "Extreme SOI - Technology, Applications, Test" and will present a comprehensive overview of the following topics: Ultra low power technology, Soft errors in advanced technologies, High temperature electronics, Built In Self Test (BIST), Photonic circuits, and future devices. Participants will receive copies of all visual presentations.

For registration forms and additional information, please go to the conference web site [www.soiconference.org](http://www.soiconference.org), or contact the 2008 IEEE International SOI Conference at 578 Washington Blvd., #350, Marina del Rey, CA 90292, Tel: 310-305-7885; Fax: 310-305-1038; Email: [bobbi@bacminc.com](mailto:bobbi@bacminc.com).

*Pierre Fazan*  
2008 SOI General Chair  
Innovative Silicon  
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# 2008 INTERNATIONAL SEMICONDUCTOR CONFERENCE (CAS)



*Sinaia resort and the Bucegi Mountains*

The 31st edition of the International Semiconductor Conference (CAS 2008), co-sponsored by the IEEE Electron Devices Society, will be held in Romania, at the Hotel Sinaia, from the mountain resort of Sinaia, from October 13-15, 2008. The aim of the conference is two-fold. First, it provides a forum of debate on selected topics of scientific research and technological development. On the other hand, this is an occasion for refreshing a broad perspective of the participants through invited papers and tutorials. The Conference is underlying the development in micro- and nanotechnologies and it still maintaining the "traditional" connection with semiconductor electronics.

The CAS conference is taking place every year since 1978. It was organized until 1996 as an *Annual Semiconductor Conference* (in Romanian – Conferința Anuală de Semiconductoare – CAS). Starting with the year 1991, CAS was opened to the international scientific community and changed its name accordingly to the *International Semiconductor Conference*, still maintaining the same acronym (CAS). Starting with the 1995 edition, the conference has been an IEEE event, being sponsored by the IEEE Electron Devices Society. Since 1997 the organizer of CAS has been the National Institute for Research and Development in Microtechnologies (IMT-Bucharest).

The organizer of the conference, IMT-Bucharest (National Institute for Research and Development in Microtechnologies), coordinated by the Romanian Ministry of Education and Research, is the first institute with this profile in Eastern Europe and the main actor in microtechnologies in Romania. Mission of IMT consists in research and development in micro- and nanotech-

nologies, technology transfer, education and training, dissemination. The institute is a pole of multidisciplinary research, integrating research, education and technology transfer, emerging as a regional centre.

In the last decade, the Conference profile has been gradually extended from semiconductor device physics and technology (including semiconductor materials and microelectronics) to micro- and nano-technologies. The conference is an ideal forum for presentation of the latest results in:

- **Simulation and fabrication of microstructures and microsystems:** surface and bulk micro-machining, microengineering techniques, electro-opto-mechanical microsystems, microsensor and actuator integration, signal processing, computational intelligence and system interfacing, biosensors and microsystems for biomedical applications; optical, opto-electronic and photonic functional components, RF MEMS;
- **Science and technology of nanostructures and nanostructured materials:** composite nanoparticles and nanostructures with selective properties, nanostructures and nanostructured materials with special properties, nanotechnologies and nanostructures;
- **Semiconductor device physics and technology:** device modelling and simulation, silicon and compound semiconductor devices, heterostructures, advanced materials and processes, reliability and defect engineering;
- **Design and technology of microelectronic components:** microelectronic, microphotonic and microwave integrated subsystems, devices and modules for power control and conversion, specialized electronic circuits integrated in the microelectronic technology, testing and reliability.

The conference will begin with a half-day plenary session, followed by two and a half days of oral and poster

sessions. The program includes a Student Papers Session. The best paper will be awarded by IEEE-Romania Section-EDS Chapter. To be eligible, the paper must be based on the student's own work and the authors should mention their option to be registered in this session.

CAS 2008 will be held in the mountain resort Sinaia, Romania, during the fall season when the autumn leaves begins to change, at the hotel having the same name, Sinaia. The "Henri Coanda" Otopeni International Airport is 115 Km far from Sinaia. The organizer of the conference provides car transportation to all participants arriving by plane at Otopeni. Sinaia is situated at 800 meter altitude, just near the Bucegi mountains chain, on the Prahova river valley. The mountains have 2500 meters highest altitude. Sinaia was developed around the Sinaia Monastery build at the end of the 17th century. His name comes from the Mount Sinai. The small town of Sinaia, with its famous Peles Castle, formerly the Summer Royal Residence, is the favorite place outside Bucharest for international conferences and high-level meetings. The rocky landscape of the Prahova valley is a paradise for mountain climbers. You may reach the height of 2000 or 2200 meters by cable or by car and enjoy a walk, without any special equipment

Please visit [www.imt.ro/cas/](http://www.imt.ro/cas/) for the Call for Papers and to submit online your paper to the Technical Program Committee. The submission deadline is June 1st 2008. The papers should be original, previously unpublished and will be published in the CAS 2008 Proceedings.

For paper submission, call for papers, advance program, registration and further information, please visit the CAS website <http://www.imt.ro/cas/>. For additional information contact us at the email address: [cas@imt.ro](mailto:cas@imt.ro). We hope you can attend.

Dan Dascalu  
2008 CAS General Chairman  
IMT Bucharest  
Romania

# SOCIETY NEWS

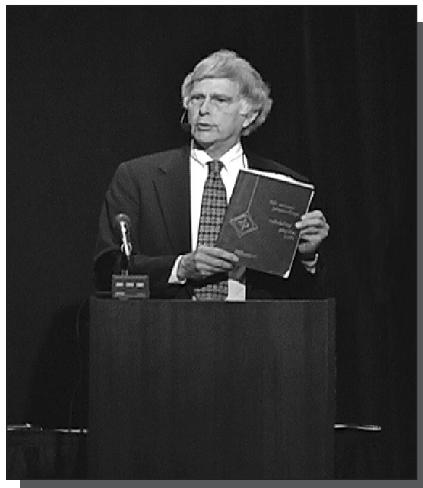
## IN MEMORY OF ROBERT W. THOMAS

*Bob Thomas was an energetic, innovative, and dedicated facilitator and promoter of reliability engineering. He worked effectively over the decades to help make sure that IRPS remained both technologically and technically the best in the world.*

He was the General Chair of IRPS in 1988 and a member of its Board of Directors for eight years. In supporting IRPS, he also presented many strikingly memorable papers at IRPS, such as his hugely successful presentation of void and hillock growth in aluminum metallization undergoing electromigration and his campaign to reduce human contamination during microcircuit manufacturing by using a "spittle" film to raise awareness. He saw the value of an electronic journal for the timely reporting of developments in reliability and championed the IEEE Transactions on Device and Materials Reliability serving on the editorial board and was on the guest editor team of three Special Issues. Many of us also remember with great fondness the smaller meetings, such as the annual Fine Line Conductor Meeting at Minnowbrook Conference Center, Blue Mountain Lake, NY, which he organized and led with uncommon grace. He provided an informal, stimulating forum for discussing and sharing the results of important ideas and work in reliability. Bob was a colleague and loving friend to many of us who will dearly miss his guidance, encouragement, wisdom, and joie de vivre.

Dr. Thomas earned a BS degree from San Jose State University, an MS degree from the University of California at Berkeley and a Ph.D. in solid state sciences from Syracuse University.

Dr. Thomas spent 32 years as a government research scientist at the Rome Air Development Center



Robert W. Thomas  
1937–2008

(USAF). During this time he worked as a research scientist in the silicon IC fabrication facility. In the 1980's he managed the Product Evaluation Laboratory, evaluating the quality and reliability of Military Grade IC's. In 1988 he was appointed Reliability Assistant to the Reliability Directorate at Rome Laboratories. He conducted research programs in epitaxial growth, package moisture measurement, contamination control and electromigration while working at Rome Air Development Center. In addition to experience in semiconductor manufacturing and product evaluation, Dr. Thomas's background includes lecturing in many countries on Total Quality Management, and developing the Mil Process Line Certification culminating in the issuance of Mil-I-38535. As part of this development, Dr. Thomas performed quality assessments on many of the major semiconductor manufacturers in the US, Europe and Asia. Since his retirement from the Air Force in 1992, he managed a commercial analytical laboratory and ran his own consulting business.

Dr. Thomas was a member of the US Electronic Component Certification Board, a representative to the International Electrotechnical Commission meeting in Beijing in October 2002, and an editor and member of the Advisory Board of the IEEE Transaction on Device and Materials Reliability. He was active in JEDEC committees, co-chairing a committee that prepared the National Electronic Process Standard (EIA-599). He chaired a hybrid committee under the International Electrotechnical Commission (IEC). Dr. Thomas was an RADC Fellow and a Fellow of the IEEE.

Bob was also involved in research associated with the history of the Newport Tower located in Tourro Park in Newport, Rhode Island. He made a cameo appearance on this subject in the PBS documentary "1421: The Year China Discovered America" produced in 2004.

### Contributors:

Rich Blish (Spancion, Sunnyvale, CA, USA)

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## EDS PRESIDENT'S MESSAGE

(continued from page 3)

Along the same line, there will this year be a strong focus towards the Graduates of the Last Decade (GOLD) members. Within IEEE, EDS is playing a leading role. New initiatives presently under discussion are: a GOLD lecture linked to EDS conferences, an initiative that started at IEDM 2007 in Washington; setting-up an EDS GOLD committee: adding GOLD members to 20 EDS Standing and Technical committees; starting a GOLD Ambassadors Program which is basically an extension of the DL program; and, possibly establishing a dedicated award for Early Career Development of GOLD members.

The flagship publications, *IEEE Transactions on Electron Devices* (TED), and *IEEE Electron Device Letters* (EDL), already have two of the leading submission to publication turnaround times as compared to the IEEE publications in their respective categories. In addition, for EDL, we started to perform the review process from 'submission to publication' electronically as of the first of the year. In the future, it is planned to have the TED review process performed online as well. Also more proceedings of EDS sponsored conferences are

become accessible via IEEE Xplore and effort is taken to have also proceedings from previous years electronically accessible.

Essential for the optimal operation of the Society is the support of all the volunteers and the staff members. As of the end of 2007, more than 650 volunteers were active within the Society. Their efforts and devotion to the Society, which are highly appreciated, are needed for the success of EDS and to make it the premiere Society within IEEE. As nowadays everybody is more and more under pressure to perform in an efficient manner, it is important that being a volunteer is also giving benefits for the professional career development and/or at the personal level. We will surely help the volunteers as much as we can.

To better serve the existing members and to attract potential new members, it is essential to optimize the members' benefits. The EDS Archival Collection on DVD, which includes all issues of *Transactions on Electron Devices*, *Electron Device Letters* and all digests of our flagship conference the International Electron Devices Meeting (IEDM), has become very popular. EDS has an annual

DVD Update Package which is compatible with the Archival Collection DVD, so EDS members always have available (on DVD and online) a full set of the core EDS articles published. The most recent action taken to increase member benefits was the announcement in the last quarter of 2007 of QuestEDS, the on-line feedback system allowing members to ask technical questions. Different EDS committees are working closely together to come up with new initiatives. Suggestions from individual members are more than welcome.

Electron Devices is a great Society with enthusiastic volunteers and professional staff members and I am very confident that all together we will achieve our goals and even increase the value of membership. I will regularly report on the progress of the Society in the Newsletter. The Society is here for its members and all possible comments and suggestions that you may have will be discussed and taken into consideration. Let us go for it jointly.

Cor L. Claeys  
EDS President  
IMEC  
Leuven, Belgium

### CONGRATULATIONS TO THE EDS MEMBERS RECENTLY ELECTED TO IEEE SENIOR MEMBER GRADE!

Khamis Badr	Tushar Ghosh*	Yiannos Manoli	Nobuikazu Teranishi
Prabhu Benakop	Helena Gleskova*	Jae-Hyun Ryou	Vinayak Tilak
Virginia Chu	Christopher Hierold	Wayne Shiroma	Fernando Tomasel
Chion Chui	S. Kanjanachuchai*	Levent Sipahi	
David Fanning*	Sergei Malyshev	Paul Tasker	

\* = Individual designated EDS as nominating entity

If you have been in professional practice for 10 years, you may be eligible for Senior Membership, the highest grade of membership for which an individual can apply. New senior members receive a wood and bronze plaque and a credit certificate for up to US \$25 for a new IEEE society membership. Upon request, a letter will be sent to employers, recognizing this new status.

For more information on senior member status, visit <http://www.ieee.org/web/membership/senior-members/status.html>. To apply for senior member status, fill out an application at <http://www.ieee.org/organizations/rab/md/smelev.htm>.

# ANNOUNCEMENT OF NEWLY ELECTED OFFICERS AND ADCOM MEMBERS

On December 9, 2007, the EDS AdCom held its annual election of officers and members-at-large. The following are the results of the election and brief biographies of the individuals elected.

## I. OFFICERS

The following individuals were elected as officers for a one-year term beginning 1/1/2008:



**RENUKA P. JINDAL**

(President-Elect) received his Ph.D. degree in Electrical Engineering from the University of Minnesota in 1981. Upon graduation, he joined Bell Laboratories at Murray Hill, New Jersey and became Distinguished Member of Technical Staff in 1989. In fall 2002, Dr. Jindal accepted the position as William Hansen Hall Board of Regents Eminent Scholar Endowed Chair at University of Louisiana. In 1991, he was elected Fellow of the IEEE. From 1990 to 2000 he served as Editor-in-Chief of the IEEE Transactions on Electron Devices. In December 2000, he received the IEEE 3rd Millennium Medal. Since 2000 he has served as Vice-President of Publications for the IEEE Electron Devices Society.



**STEPHEN A. PARKE**

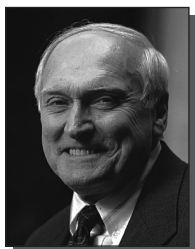
(Treasurer) received the BS and MS degrees in electrical engineering from Purdue University in 1984. He then

joined IBM Microelectronics where he worked in device and process development for the 4Mb, 16Mb, and 64Mb DRAM designs. In 1989, he was awarded an IBM Ph.D. Fellowship, and joined the UC Berkeley Device Research group, where he studied the behavior of deep-sub-micron MOSFET and lateral bipolar transistors on thin-

film SOI. In 1993, he received the Ph.D. degree and joined the IBM Semiconductor R&D Center in Fishkill, NY where he worked in the 256Mb DRAM Triad alliance between IBM, Toshiba, and Infineon. This effort accelerated the 0.25 micron process development, leading to the world's first fully-functional 256 Mb DRAM chip in 1995.

In 1996, he joined the Electrical Engineering faculty of Boise State University at the inception of its new College of Engineering. He helped lead the creation and development of the ECE Department at BSU over its first ten years. Dr. Parke has a passion for technology transfer. In Boise, he advised three start-up companies in the electronics field, and currently serves on the Board of Directors of American Semiconductor, Inc.

In 2006, Dr. Parke joined Tennessee Tech University as Professor and Chair of the TTU Electrical and Computer Engineering Dept. Dr. Parke's research is in the areas of Double-Gated Nanoscale Silicon-On-Insulator Transistors and Non-Volatile Memories. He holds ten US patents with five pending. He is the co-inventor of the DTMOS and FlexFET transistors. He has published and/or presented over 30 papers. He has served the IEEE Electron Devices Society as Graduate Student Fellowship Chair, WMED General Chair, UGIM General Chair, and currently as the Treasurer. He received the IEEE Millennium Medal in 2000 for his service. He is also a member of Tau Beta Pi and Eta Kappa Nu honorary societies.



**JAMES L. MERZ**

(Secretary) Dr. Merz received the B.S. degree in Physics from the University of Notre Dame in 1959, and attended the University of Göttingen, Germany, 1959-60. He received his M.A. degree in 1961 and Ph.D. in Applied Physics in 1967 from Harvard. He joined Bell Lab-

oratories in 1966, and in 1978 moved to UCSB as a Professor of Electrical Engineering. He was appointed Department Chair in 1982, Associate Dean for Research for Engineering from 1984 to 1986, and Associate Vice Chancellor from January to September, 1988. He was Director of the Center for Quantized Electronic Structures (QUEST), a NSF Science and Technology Center, from 1989 until he moved to Notre Dame in 1994, where he served as VP for Graduate Studies and Research from 1996 to 2001. He also served as Interim Dean of Engineering, July 2006 to January 2008.

Dr. Merz was awarded an Honorary Doctorate by Linköping University, Sweden, in 1993. He is a Fellow of the APS, IEEE, and AAAS. He was awarded the IEEE Third Millennium Medal in 2000, and received an Alexander von Humboldt Award to carry out research in Germany in 2002. He served for five years as Secretary of the Electron Devices Society of the IEEE and a member of its Executive Committee, and resumes that duty in December 2007. He is currently a member of the Board of Directors of the Tyndall National Institute in Cork, Ireland.

## II. ADCOM MEMBERS-AT-LARGE

A total of seven persons were elected to three-year terms (2008-2010) as members-at-large of the EDS AdCom. Five of the seven individuals were re-elected for a second term, while the other two were first-time electees. The backgrounds of the electees span a wide range of professional and technical interests.

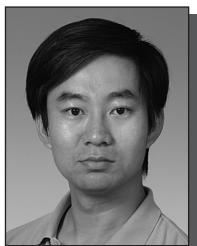
### A. SECOND TERM ELECTEES:



**JOACHIM N. BURGHARTZ**

received the M.S. (Dipl. Ing.) degree from the RWTH Aachen, Germany, in 1982 and the Ph.D. (Dr.-Ing.) degree from the University of Stuttgart, Germany, in

1987, both in electrical engineering. From 1987 to 1998 he was with the IBM Research, working on Si and SiGe bipolar technologies, advanced CMOS, and high-quality spiral inductors on silicon. From 1998 to 2005 he was a full professor at TU Delft, the Netherlands, also serving from 2001 as the Scientific Director of the research institute DIMES. Since October 1, 2005 he is Director of the Institute for Microelectronics Stuttgart (IMS-CHIPS) and full professor at the University of Stuttgart, Germany. He is Fellow of the IEEE, has published more than 250 reviewed articles and holds 22 patents.



#### **MANSUN CHAN**

received his Ph.D. degree from University of California at Berkeley where his research contributes to the unified BSIM model

for SPICE, which has been accepted by most US companies and the Compact Model Council (CMC) as the first industrial standard MOSFET model. Currently, he is with the ECE department of Hong Kong University of Science and Technology. His research interests include nanodevices, image sensors, 3D IC, non-volatile and BioNEMS. Between July 2001 and December 2002, he was a Visiting Professor at University of California at Berkeley and the Co-director of the BSIM program.



#### **SHUJI IKEDA**

received the B.S. degree from Tokyo Institute of Technology, Tokyo, Japan in 1978, the M.S.E.E. degree from Princeton

University, Princeton, New Jersey and Ph.D. degree from Tokyo Institute of Technology. He joined Semiconductor Division, Hitachi Ltd., Tokyo, Japan in 1978, where he was engaged in research and development of state of the art SRAM process and devices, including high resistive poly load / thin

film transistors for SRAM application. He was also working on developing process technology for LOGIC, embedded memories, Flash and CMOS power RF devices. In October 2000, he joined Trecetti Technologies Inc. He chaired IEDM in 2002. He is a Fellow of IEEE.



#### **REBECCA J. NIKOLIC**

received the B.S. degree in Electrical Engineering from the University of California at Davis in 1997. In 1999 she received the

M.S. degree and in 2002 the Ph. D. degree in Electrical Engineering, specializing in Applied Physics, from the University of California at San Diego. Her dissertation research focused on high-speed GaInP/ GaAs and GaAs/ GaInNAs based heterojunction bipolar transistors (HBTs). In 2002 she joined Lawrence Livermore National Laboratory as a Staff Research Engineer in the area of optoelectronic device development in III-V materials has focused on the development of photonic integrated circuits and radiation detectors. Her research interests are in device physics of electron and optoelectronic devices and advanced process technology.



#### **JEFFREY J. WELSER**

received his Ph.D. in Electrical Engineering from Stanford University in 1995, and joined IBM's T.J. Watson Research Center.

His graduate work focused on utilizing strained-Si and SiGe materials for FET devices. Since joining IBM, Jeff has worked on a variety of novel devices, including nano-crystal and quantum-dot memories, vertical-FET DRAM, and Si-based optical detectors, in addition to teaching as an adjunct professor at Columbia University. In 2000, Jeff moved to the Microelectronics division, as project manager and then Director of high-performance SOI and BEOL technology development and IBM manager for the Sony, Toshiba, and

AMD development alliances. Jeff returned to the Research division in 2003 as Director Next Generation Technology Components, working on future server components and systems. He is currently on assignment to the Semiconductor Research Corporation (SRC) as Director of the Nanoelectronics Research Initiative, directing university-based research on future nanoscale logic devices. He is based at the IBM Almaden Research Center in San Jose, CA.

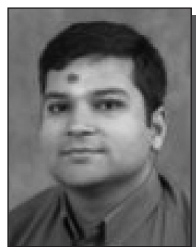
#### **B. FIRST-TIME ELECTEES:**



#### **TIAN-LING REN**

received his Ph.D. degree in solid-state physics from Tsinghua University, Beijing, China in 1997. He is full professor of institute

of microelectronics, Tsinghua University. Currently, he also serves as the vice chair of IEEE Electron Devices Society Beijing Chapter, and Distinguished Lecturer (DL) of IEEE Electron Devices Society. His present research interests are novel micro/nano devices and systems, such as nonvolatile memories, MEMS, integrated ferroelectric devices, and integrated magnetic devices. He chaired the International Workshop on Electron Devices and Semiconductor Technology (IEDST) in 2007.



#### **RAVI M. TODDI**

received his B.S. degree in Electrical engineering from Mumbai University, India, in 2002 and M.S. degree in Electrical

and Mechanical Engineering from University of Central Florida in 2004 and 2005 respectively, and his doctoral degree in Electrical Engineering in 2007. His graduate research work was focused on gate stack engineering, with emphasis on binary metal alloys as gate electrode and on high mobility Ge channel devices. His research interest includes semiconductor process

integration and device technology, non-conventional CMOS scaling and nano and bio devices. Since 2007 he is working as Advisory Engineer/Scientist at Semiconductor

Research and Development Center at IBM Microelectronics Division focusing on high performance eDRAM integration on 45nm SOI logic platform.

*Ilesanmi Adesida  
EDS Chair of Nominations  
and Elections  
University of Illinois  
Urbana, IL, USA*

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## CALL FOR NOMINATIONS - EDS AdCOM

The Electron Devices Society of the IEEE invites the submission of nominations for election to its Administrative Committee (AdCom). Presently, the AdCom meets twice per year and is composed of 22 members. Eight members will be elected this year for a term of three years, and a maximum of two consecutive terms is allowed. In 2008, the election will be held after the AdCom meeting on Sunday, 14 December. Electees begin their term in office on 1 January 2009. For your information, the nominees do not need to attend the AdCom Meeting/Election to run.

Nominees are being sought to fill the slate of candidates. Nominees

may be self-nominated, or may be nominated by another person; in the latter case, the nominee must have been contacted and have agreed to serve if elected. Any member of EDS in good standing is eligible to be nominated. The nominees do not need to attend the AdCom Meeting/Election to run. On the other hand, if elected, the nominees are expected to attend the two AdCom meetings a year. In general, the travel and accommodation costs to attend these meetings are borne by the elected member.

Please send your nominee's name, address, and supporting information to the EDS Executive Office Sr. Administrator, Laura J. Riello,

IEEE, 445 Hoes Lane, Piscataway, NJ 08854, Fax: 732-235-1626, E-Mail: [l.riello@ieee.org](mailto:l.riello@ieee.org) in time to be received by the deadline of 15 October 2008. It is very desirable that submissions include a biographical summary in a standard two-page format. The EDS Executive Office can provide you with an example of the format. If you have any questions regarding the nomination requirements or process, feel free to contact Laura Riello ([l.riello@ieee.org](mailto:l.riello@ieee.org)).

*Ilesanmi Adesida  
EDS Chair of Nominations & Elections  
University of Illinois  
Urbana, IL, USA*

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## EDS ADMINISTRATIVE COMMITTEE ELECTION PROCESS

The Members-at-Large (MAL) of the EDS AdCom are elected for staggered three-year terms, with a maximum of two consecutive terms. The 1993 Constitution and Bylaws changes mandated increasing the number of elected MAL from 18 to 22, and required that there be at least two members from both IEEE Region 8 (Europe, Middle East & Africa) and Region 10 (Asia & Pacific). In 2003, EDS made changes to its Constitution and Bylaws to require that at least one elected AdCom member is a Graduate of the Last Decade (GOLD member). A GOLD member is defined by IEEE as a member who graduated with his/her first professional degree within the last ten years. It is also required that there be at least 1.5 candidates for each

opening. In 2008, eight positions will be filled.

The election procedure begins with the announcement and Call For Nominations in the EDS Newsletter. The slate of nominees is developed by the EDS Nominations Committee and includes the non-Committee and self-nominations received. Nominees are asked to submit a two-page biographical resume in a standard format. Nominations are closed on 15 October, and the biographical resumes are distributed to the 'full' voting members of AdCom prior to the December AdCom meeting. The election is then held after the conclusion of the meeting. The nominees do not need to attend the AdCom Meeting/Election to run. On the other hand, if elected, the nominees are expected to attend the two AdCom

meetings a year. In general, the travel and accommodation costs to attend these meetings are borne by the elected member.

A continuing flow of new AdCom members who are interested in working for the improvement of the Society and its related technical areas is essential for the continued development of EDS and the field of electron devices. Those interested in the field, the Society, and its operations are encouraged to attend AdCom meetings, become involved in Society activities, and consider running for election to AdCom.

*Ilesanmi Adesida  
EDS Chair of Nominations  
& Elections  
University of Illinois  
Urbana, IL, USA*



## SUMMARY OF CHANGES TO THE EDS CONSTITUTION & BYLAWS

As recently required by the IEEE, the following statement concerning the vote of the presiding officer was included in the EDS Constitution:

### Article V Organization

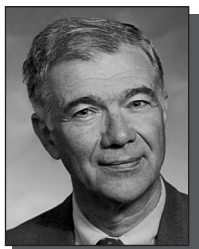
**Section 14.** Vote of the Presiding officer. The presiding officer of the Administrative Committee or any Standing, Technical or Adhoc Committee shall have no vote on the Administrative Committee or any Standing, Technical, or Adhoc Committee, except if the vote is by secret ballot or unless the Chair's vote can change the outcome of the vote.

This change will take effect 30 days following its publication in this copy of the Newsletter (distributed to all EDS members), unless objections are received from at least 5% of the EDS membership.

The complete EDS Constitution and Bylaws may be obtained from the EDS Executive Office or on the web at <http://www.ieee.org/eds> (click on Administrative Committee).

*Cor L. Claeys  
EDS President  
IMEC  
Leuven, Belgium*

## EDS AWARDS COMMITTEE REPORT



*Alfred U. Mac Rae*

Nominate a colleague! The success of our awards program is dependent on nominations. So, take the time to fill out a nomination form to honor a person who has made a major contribution

to the technology that is in the field of interest of our Society. Fortunately there are many awards, both EDS and IEEE, that embrace our technologies and interests. EDS in particular has the J.J. Ebers Award for contributions of recognized scientific, economic, or social significance in the broad field of electron devices, the Education Award for contributions to education and several awards for best papers in our journals and meetings, Graduate Student Fellowships and student paper awards. The IEEE has numerous medals, and technical field awards that tend to be dominated by Electron Devices Society members. I suggest that you go to the IEEE Awards web site at <http://www.ieee.org/about/>

awards/ and pick out an award that best suits the contribution of a colleague and then go ahead and prepare the nomination. And don't forget the Fellows program, which is conferred by the IEEE Board of Directors upon a person with an extraordinary record of accomplishments in any of the IEEE fields of interest. While numerous EDS members are IEEE Fellows, it often surprises me to learn about members who have made major contributions to electron devices and who are not a Fellow. Such members are deserving of the effort of existing Fellows to prepare a nomination.

An important aspect our awards program is the many dedicated members who serve on the committees that select the recipients of the awards. I shall not attempt to name them all here in this article. I am sure that I would overlook someone, so I'll skip that attempt. Many of them are listed in the web pages that describe the awards. However, I would like to single out members of our EDS Awards Committee for special recognition. They are Lou Parrillo, Chair of the J. J. Ebers Award, Cary Yang,

Chair of the Education Award, Rick Dill, Past Chair of our Distinguished Service Award and Mark Bohr, Yoshirio Hirayama, Jeffrey Weisner, Hiroshi Iwai, Renuka Jindal and Jayasimha Prasad. In many instances, you may be aware of a significant technical contribution, but are not sure who exactly made that contribution. On the other hand, you may be aware of the person who made a contribution, but don't know the name of an appropriate individual who will prepare the nomination. If so, contact me or one of the members of the EDS Awards Committee for help.

Perhaps I am biased, but I feel that members of our EDS have made a disproportionate number of contributions that have had a major impact on the world's economies and the well being of the world's people. I look forward to seeing these people recognized for their contributions. Go for it! Nominate a colleague!

*Alfred U. Mac Rae  
EDS Vice-President of Awards  
Mac Rae Technologies  
Berkeley Heights, NJ, USA*

## EDS COMPACT MODELING COMMITTEE REPORT



Samar Saha

The IEEE Electron Devices Society (EDS) Compact Modeling Technical Committee (CMTC) is actively involved to objectively identify, examine, and evaluate emerging compact models

for circuit simulation and promote interactions among compact model developers, technology developers, and circuit designers. The present CMTC consists of 21 members worldwide who are actively involved in R&D on compact modeling and real time applications of compact models.

The CMTC's activities are spread around the globe. Over the past two years, the most significant activities of CMTC include the publication of the Special Issue (SI) of IEEE Transactions on Electron Devices (T-ED) on "Advanced compact models and 45-nm modeling challenges," organization of annual Workshop on Compact Modeling (WCM) under the Program Chair, Prof. X. Zhou of CMTC member, and submission of a proposal for a new interactive online journal on compact modeling, IEEE Transactions on Applied Compact Modeling (T-ACM), aimed at reporting leading edge technical information critical to the industrial usage of compact models.

In addition to WCM 2008 in June 1-5 at Boston, the major plans of CMTC in the year 2008 include:

- Propose a T-ED SI on "Compact Interconnect Models for Giga Scale Integration"
- Organize a workshop on "Compact Models for Thin-Film Transistors (TFT)," an emerging compact modeling Field-of-Interest
- Organize a mini-colloquia (MQ) on "New Frontiers of Compact Modeling"

The proposal for the T-ED SI has been submitted to the Editor-In-Chief with a tentative scheduled publication date, September 2009. The objective of the proposed SI is to bring together a diversity of R&D activities and advancement in compact interconnect models

for circuit simulation to accurately analyze the effect of on-chip interconnects of the existing and emerging interconnect materials and technologies.

In recent years, the increasing demands for flat-panel-displays in commercial electronic devices have drawn a significant attention to Thin-Film Transistors (TFT) and technology. In this context, CMTC's objective is to provide a forum for discussions of emerging compact TFT modeling through a workshop on "Compact Models for Thin-Film Transistors." The workshop is scheduled on September 11, 2008 at Cambridge, UK and is intended to bring together a diversity of R&D activities on TFT modeling and inspire future developments.

Another planned activity of CMTC is the MQ on "New Frontiers of Compact Modeling," scheduled on October 3, 2008 at Santa Clara University, CA, USA and is focused on the emerging compact device and interconnect models such as Bio-transistors, Carbon Nano Tube interconnects (CNT), and so on. Six EDS distinguished speakers who are actively involved in R&D activities of emerging compact device and interconnect models are invited as speakers. Furthermore, the MQ has posted a "call for student papers and posters" to encourage the student researchers of the local institutions to actively participate in EDS activities.

The future plans of CMTC is to survey the financial feasibility of the proposed interactive online journal, IEEE T-ACM and develop a comprehensive plan to setup an infrastructure for interactivity. The other important goals are promoting interactions among the model developers and foundries for the characterization of emerging compact-models and continue organizing IEEE seminars, distinguished lectures, conference sessions, etc. on compact modeling. Finally, CMTC's goal is to work closely with Compact Modeling Council to harness the R&D results on compact modeling for industrial use.

Samar Saha

EDS Compact Modeling Technical  
Committee Chair  
Silterra USA, Inc.  
San Jose, CA, USA



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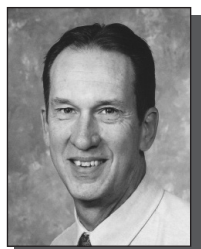


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## EDS MEMBERS NAMED WINNERS OF THE 2008 IEEE TECHNICAL FIELD AWARDS

Five EDS Members were among the winners of the 2008 IEEE Technical Field Awards. They are:

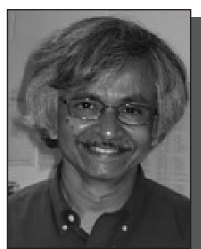


**James J. Coleman**

of the University of Illinois at Urbana-Champaign, Urbana, IL, won the 2008 IEEE David Sarnoff Award. His cita-

tion states, "For leadership in the development of highly reliable strain-layered lasers"

James J. Coleman is an expert in laser design and leader in the field of optoelectronics. He is currently the Intel Alumni Endowed Chair in Electrical and Computer Engineering at the University of Illinois at Urbana-Champaign. His study of strain-layered lasers led to the development of the 980 nm pump laser used throughout fiber-optic telecommunications systems. Prior to his current position, Dr. Coleman worked at Rockwell International, where he helped develop the metalorganic chemical vapor deposition (MOCVD) process used to grow III-V semiconductor lasers and photonic devices, which are used for optical storage and medical applications. An IEEE Fellow and co-author of 375 journal publications and 7 patents, Dr. Coleman has received several awards and honors, including the IEEE William Streifer Scientific Achievement Award and was an IEEE LEOS distinguished lecturer. He holds a bachelor's, masters and doctorate, all in electrical engineering, from the University of Illinois, Urbana-Champaign.

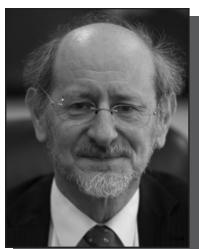


**Supriyo Datta**

of Purdue University, West Lafayette, IN, won the 2008 IEEE Leon K. Kirchmayer Graduate Teaching Award.

His citation states, "For his unique approach to quantum transport that has inspired and educated graduate students in the field of nanoscale electronic devices"

Supriyo Datta, the Thomas Duncan Distinguished Professor of Electrical and Computer Engineering at Purdue University, Indiana, has inspired and educated hundreds of graduate students through his unique approach to the complex concepts of nanoelectronics. Dr. Datta, a leading figure in the modeling and understanding of nanoscale electronic conduction, laid the foundation for quantum-transport simulation tools based on the non-equilibrium Greens function formalism, and made pioneering contributions to the emerging fields of spintronics and molecular electronics. A distinctive aspect of his style that contributes to his effectiveness in teaching is his emphasis on critical thinking, in addition to technical problem-solving skills. Datta's classroom lectures have been videotaped and made available to students around the world by the National Science Foundation-funded Network for Computational Nanotechnology through the nanoHUB, a Web site serving nearly 10,000 users per year. An IEEE Fellow, Dr. Datta has received numerous awards and has authored several books. He holds a bachelor's in technology from the Indian Institute of Technology, Kharagpur, India and a doctorate from the University of Illinois at Urbana-Champaign.



**Gilbert J. Declerck**

of IMEC, Leuven, Belgium, won the 2008 IEEE Frederik Philips Award. His citation states, "For leadership in the creation of international R&D

alliances in semiconductor technologies"

Gilbert J. Declerck, co-founder, president and CEO of the Interuniversity Microelectronics Center (IMEC), Leuven, Belgium, is credited with developing IMEC into one of the world's most advanced semiconductor research centers. Under his guidance, IMEC has created a unique alliance with the top integrated device manufacturers, foundries, system houses, fables and fab-lite companies and researchers in academia and industry. Dr. Declerck's leadership has continued the expansion of IMEC's R&D capabilities into cutting edge transistor scaling beyond the 32nm node. Today IMEC is recognized worldwide and runs several industrial affiliation programs with global participation in the fields of semiconductor technology, system-on-chip design, heterogeneous integration and advanced packaging technologies. Dr. Declerck's success in bringing together preeminent researchers in semiconductors and other fields, including nanotechnology, has earned him numerous appointments to several advisory boards of scientific organizations and companies. An IEEE Fellow, Dr. Declerck has authored and co-authored more than 200 papers. He holds a bachelor's and masters in electrical engineering, and a doctorate in applied sciences from the Katholieke Universiteit Leuven, Belgium.



**Meyya Meyyappan**

of NASA Ames Research Center, Moffett Field, CA, won the 2008 IEEE Judith A. Resnik Award. His cita-

tion states, "For the development of nanoscience and technology in aerospace applications and leadership in nanotechnology"

Meyya Meyyappan has spearheaded major advancements in the field of space engineering through

his pioneering research and development of nanotechnology applications for aerospace and industry. Dr. Meyyappan is chief scientist for Exploration Technology and until recently was director of the Center for Nanotechnology, NASA Ames Research Center in Moffett Field, Calif., which he helped found in 1997. The Center is considered the strongest and most creative nanotechnology research laboratory of any of the federal labs. A respected author, Dr. Meyyappan has published more than 180 referenced technical papers, 15 books and nine patents. An IEEE Fellow, he is also the recipient of several awards for his work and leadership in nanotechnology, including Presidential Meritorious Award and the Arthur Fleming Award given by the Fleming Foundation and George Washington University. He holds a bachelor's from Madras University, India; a master's from Aston University, Birmingham, U.K.; and doctorate from Clarkson University, Potsdam, N.Y.



#### **Saied Tehrani**

of Freescale Semiconductor, Chandler, AZ, won the 2008 IEEE Daniel E. Noble Award, along with James M. Daughton and

Stuart Parkin. The citation states, "For fundamental contributions to the development of magneto-resistive devices for non-volatile, high density, random access memory"

James M. Daughton, Stuart Parkin and Saied Tehrani each made key contributions to Magneto-Resistive Random Access Memory (MRAM) technology. The work of Dr. Daughton in sensors and couplers, Dr. Parkin in Magnetic Tunnel Junction, and Dr. Tehrani in materials and processes, when combined, helped make MRAM a viable memory technology for both military and commercial applications. MRAM is an integrated-circuit access memory fabricated with nanotechnology. Using an electron spin to store

data, it has the capability to combine many of the best attributes of different types of semiconductor memories.

Dr. Tehrani is Director of Analog and Mixed Signal Technologies at Freescale Semiconductor (formerly the semiconductor division of Motorola, Inc.). His R&D team is responsible for the development of power, analog, RF, sensor, and magneto-resistive random access memory (MRAM) technologies. Dr. Tehrani became a Motorola Fellow in 2000 and a Freescale Semiconductor Fellow in 2006. He has co-authored more than 80 articles in refereed journals, given more than 20 invited presentations at various international conferences, and has 75 issued patents. He received a bachelor's from the University of North Carolina, Charlotte and a masters and doctorate in electrical engineering from the University of Florida, Gainesville.

*Alfred U. Mac Rae  
EDS Vice-President of Awards  
Mac Rae Technologies  
Berkeley Heights, NJ, USA*

## **CALL FOR NOMINATIONS FOR THE EDS CHAPTER OF THE YEAR AWARD**

The EDS Chapter of the Year Award is given each year based on the quantity and quality of the activities and programs implemented by the chapters during the prior July 1st – June 30th period. Nominations for the award can only be made by Chapter Partners, SRC Chairs/Vice-Chairs, or self-nominated by Chapter Chairs. The nomination form is available at [www.ieee.org/eds](http://www.ieee.org/eds) or by contacting Laura Riello ([l.riello@ieee.org](mailto:l.riello@ieee.org)) from the EDS Executive Office.

The winning chapter will receive a certificate and check for \$1,000 to be presented at the IEEE International Electron Devices Meeting (IEDM).

As of the 2007 Award, the EDS AdCom approved a ruling whereby a chapter that wins the Chapter of the Year Award cannot win again until after a lapse of 3 years.

The schedule for the award process is as follows:

Action	Date
Call for Nominations E-Mailed to Chapter Chairs, Chapter Partners, SRC Chairs & SRC Vice-Chairs	6/1
Deadline for Nominations	9/15
Regions/Chapters Committee Selects Winner	Early-October
Award given to Chapter Representative at IEDM	First week of December



## STATUS REPORT FROM THE 2007 EDS PHD STUDENT FELLOWSHIP WINNERS

In 2000, the IEEE approved the establishment of the Electron Devices Society Ph.D. Student Fellowship Program. The Program is designed to promote, recognize, and support graduate level study and research within the Electron Devices Society's Fields of Interest, which include: All aspects of the engineering, physics, theory, experiment and simulation of electron and ion devices involving insulators, metals, organic materials, plasmas, semiconductors, quantum-effect materials, vacuum, and emerging materials. Specific applications of these devices include bioelectronics, biomedical, computation, communications, displays, electro and micro mechanics, imaging, micro actuators, optical, photovoltaics, power, sensors and signal processing. In deference to the increasing globalization of our Society, at least one fellowship is to be awarded to students in each of three geographical regions: Americas, Europe/Mid-East/Africa, and Asia & Pacific.

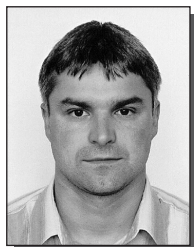
In July 2007, EDS announced the winners of the 2007 Fellowships. The four winners were: Kah-Wee Ang of the National University of Singapore, Singapore; Danijel Dankovi, University of Nis, Nis, Serbia; Tuo-Hung Hou, Cornell University, Ithaca, NY; and Chen Yang, Tsinghua University, Beijing, China. The winners are pursuing distinctly different research topics for their doctoral degrees. The following are brief progress reports written by the award winners.

**Kah-Wee Ang's** research interests focus on the application of novel device structures coupled with strained-silicon technology for extending CMOS speed performance beyond the 32 nm technolo-



*Kah-Wee Ang*

gy generation. In the course of his research, he has published more than 35 technical articles in top-tier journals and international conferences. His Ph.D. thesis titled "Strain Engineering for Enhanced Transistor Performance" has been reviewed and will be expected to receive his Ph.D. degree from the National University of Singapore in April 2008. Currently, he is deployed at the Institute of Microelectronics, Singapore, working on the development of high bandwidth optical receiver monolithically integrated in silicon-CMOS technology platform for cost-effective telecommunication applications.



*Danijel Dankovi*

**Danijel Dankovi's** current research project involves the study of negative and positive bias temperature instabilities (NBTI and PBTI) in both p- and n-channel power VDMOS-FETs. An important part of his study is devoted to estimating the VDMOS device lifetime. He has authored or coauthored 25 scientific papers, 7 among them in the refereed international journals. Also, he has 4 papers in progress. The title of his PhD thesis is "Bias temperature instabilities in commercial power VDMOSFETs". His PhD thesis is to be completed in 2009.

**Tuo-Hung Hou** is currently pursuing his Ph.D. degree under the guidance of Professor Edwin C. Kan in the School of Electrical and Computer



*Tuo-Hung Hou*

Engineering, Cornell University. His research centers on the combined theoretical and experimental study of non-volatile-charge-based devices in heterogeneous integration with nanocrystals, fullerenes, and carbon nanotubes. His works on the design optimization of nanocrystal memory, the redox states of molecular floating gate and the molecule-embedded tunnel oxide are hoped to not only benefit the scaling of non-volatile memory, but also shed light on the potential of hybrid molecular/Si electronics. His dissertation is expected to complete by May 2008.



*Chen Yang*

**Chen Yang's** research at Institute of Microelectronics, Tsinghua University, is on high-performance on-chip passive RFIC devices, with focus on miniaturized novel magnetic passive inductors and transformers. Recently, he is working on the magnetic-medium-fully-filled inductor under CMOS process. He has authored or coauthored 23 peer-reviewed journal and conference papers. His PhD thesis should be complete by July 2008. He serves as the Chair of EDS Tsinghua University Student Branch Chapter. He can be reached at [chenyang@ieee.org](mailto:chenyang@ieee.org).

*Agis A. Iliadis  
2007 EDS Chair Graduate  
Student Fellowships  
University of Maryland  
College Park, MD, USA*

## REPORT ON THE IEEE ED ORLANDO MINI-COLLOQUIUM



*Slavica Malobabic*

On February 21st and 22nd, the Orlando Electron Devices Chapter hosted the ED Colloquium in Orlando at the University of Central Florida.

On the first day, Dr. Issa Batarseh, Director of the School of Electrical Engineering and Computer Science, gave an overview of the school. Dr. Juin J. Liou, IEEE EDS Vice President of Regions/Chapters, gave an opening speech.

The technical program consisted of nine talks given by internationally recognized lecturers in the field of electron devices. The topics included:

- Dr. Cor Claeys (IMEC, Belgium) - Processing and Defect Control of Advanced Ge Technologies
- Dr. James Vinson (Intersil, USA) - Designing Electrical Over stress Robust Integrated Circuits
- Dr. Subramanian Iyer (IBM, USA) - Beyond Scaling – Teaching the Old Dog some New Tricks!
- Dr. Eric Kay (IBM, USA) - Synthesis, Properties and Applications of Granular Composite Thin Film Systems
- Dr. Frank Schwierz (TU Ilmenau, Germany) - Physics and Performance of Ultra High Frequency Field-Effect Transistors
- Dr. Francisco Garcia Sanchez (Simon Bolivar University,

Venezuela) – A Succinct Overview of Electron Device Evolution

- Dr. Steven Voldman (Qimonda, USA) - Latch-up in Semiconductor Technology
- Dr. Jean-Jacques Hajjar (Analog Devices, USA) - Predicting Circuit ESD Performance Through SPICE-type Simulation
- Dr. Paul Yu (UC San Diego, USA) - Optical Modulators for Transparent Analog Fiber Link

The approximately 140 attendees of the colloquium, mostly students of UCF, socialized with the speakers during the lunches and coffee breaks within the colloquium. At the banquet dinner on the 21st, the speakers sat down with the organizing committee and the IEEE Orlando Section Executive Committee in a relaxed atmosphere, and on the 22nd, the speakers were invited on a tour to the Kennedy Space Center.

The presentation slides were posted on the Orlando section website (<http://ewh.ieee.org/r3/orlando/>) in May. The Colloquium was co-sponsored by IEEE Electron Devices Society, IEEE and AVS Student Chapters of UCF, Student Government Association of UCF, IEEE Orlando Section, and UCF School of Electrical Engineering and Computer Science.

*Slavica Malobabic  
ED Orlando Chapter Chair  
University of Central Florida  
Orlando, FL, USA*



From Left to Right (speakers and some organizing committee members): Dr. Frank Schwierz, Dr. Juin J. Liou, Dr. Cor Claeys, Dr. Jim Vinson, Dr. Eric Kay, Dr. Francisco Garcia Sanchez, Slavica Malobabic, Vinit Todi, David Ellis, Dr. Subramanian Iyer, Lifang Lou, Dr. Steven Voldman, and Dr. K. B. Sundaram

## EDS CHAPTER SUBSIDIES FOR 2009



The deadline for EDS chapters to request a subsidy for 2009 is 1 September 2008. For 2008, the EDS AdCom awarded funding to 66 chapters, with most amounts primarily ranging from US\$250 to US\$1,500. In June, Chapter Chairs were sent an e-mail notifying them of the current funding cycle and providing them with a list of guidelines. In general, activities which are considered fundable include, but are not limited to, membership promotion travel allowances for invited speakers to chapter events, and support for student activities at local institutions. Subsidy requests should be sent via e-mail or fax to the EDS Sr. Administrator, Laura J. Riello, IEEE, EDS Executive Office, 445 Hoes Lane, Piscataway, NJ 08854, [l.riello@ieee.org](mailto:l.riello@ieee.org) or fax 732 235 1626. Prior to the submission of the subsidy request, the Chapter Chair must submit a chapter activity report to its respective SRC Chair and Laura Riello of the EDS Executive Office by July 1. This report should include a general summary of chapter activities (one to two pages) for the prior July 1st - June 30th period. You must also attach a copy of the activity report to your chapter subsidy request. Final decisions concerning subsidies will be made by the EDS SRC Chairs/Vice Chairs in December. Subsidy checks will be issued by late January.

## REPORT ON THE MINI-COLLOQUIUM ON “COMPACT MODELING OF ADVANCE MOSFET STRUCTURES AND MIXED MODE APPLICATIONS”

The IEEE ED Delhi Chapter, formed in March 2007, organized a mini-colloquium on “Compact modeling of advance MOSFET structures and mixed mode applications”. The mini-colloquium was held January 5-6, 2008, and sponsored by the IEEE Electron Devices Society under its Distinguished Lecturer Program. This mini-colloquium on “Compact modeling of advance MOSFET structures and mixed mode applications” is an attempt to bring together researchers, device and circuit engineers working in the area of developing compact models for emerging MOSFET structures. Compact Models for device and circuit simulation, which have been at the heart of CAD tools for circuit design and are playing an ever increasingly important role with the advent of new nanoscale MOSFET structures. As the mainstream MOS technology is scaled into the nanometer regime, development of a physics based compact model for circuit simulation that covers device geometry, gate and drain bias, temperature, digital and analog performance along-with noise characteristics become a major challenge. The objective is to create a forum for discussion among students and experts in the field as well as feedback from technology developers and circuit designers. The topics cover all important aspects of compact model development within

the main theme - compact models for circuit simulation:

- Emerging novel MOSFET architecture and modeling schemes
- RF- and noise models
- Interconnect modeling techniques
- Quantum-mechanical compact models
- TCAD simulation
- Model parameter extraction and optimization
- SAW Devices

Five IEEE Distinguished Lectures and 20 student poster presentations were held during the Mini-Colloquium.

### IEEE-Distinguished Lecturer talks on January 5, 2008:

- i. “Interconnect Design Issues of Nano CMOS”, by Professor Kazuya Masu from Integrated Research Institute, Tokyo Institute of Technology, Nagatsuta, Yokohama, Japan.
- ii. “Physics Technology and performance of high speed CMOS technologies”, by Dr. Sunit Tyagi from Intel India technology Private Limited, Bangalore, Karnataka, India.
- iii. “Silicon quantum dots: the future of electronics” by Professor Shunri Oda from Professor, Quantum Nanoelectronics, Research Center Tokyo Institute of Technology, Ookayama, Meguro-ku, Tokyo, Japan.

- iv. “Device Design and Optimization for Nanoscale and Multi-gate MOSFETs” by Professor V. Ramgopal Rao from Dept. of Electrical Engineering, IIT Bombay, Powai, Mumbai, India

### IEEE-Distinguished Lecturer talk on January 6, 2008:

- i. “Nano-Electronic Devices based on Silicon MOS Structure” by Professor C. K. Sarkar from Jadavpur University, Dept. of Electronics and Telecommunication, Calcutta, India
- ii. Apart from the above mentioned IEEE-EDS DL talks another technical talk was given on “Extraction of and its frequency dependence in Nitrided Tunnel oxides using MOS Capacitors and MOSFETs” Professor K. N. Bhat, Indian Institute of Science, Bangalore, India. Nearly 50 participants from all over India from different academic Institutions and R&D laboratories attended the mini-colloquium.

*Radhey S. Gupta*  
ED Delhi Chapter Chair

*Mridula Gupta*  
ED Delhi Chapter Secretary

*Manoj Saxena*  
ED Delhi Executive  
Committee Member

## EDS DISTINGUISHED LECTURERS PARTICIPATE IN THE 14TH WIMNACT HELD IN SIKKIM, INDIA

The ED Calcutta Chapter is a relatively new chapter to join the IEEE Calcutta Section, but it has been very active in organizing various technical lectures and tutorials for the benefit of students and researchers, as well as co-sponsoring various conferences and academic meetings.

In 2007, the ED Calcutta Chapter and the ED North Jersey Chap-

ter (USA), jointly organized a mini-colloquium on Microelectronics and VLSI, held at The New Marion Hotel at Bhubaneswar (the temple city of India), with the objective of spreading the cause of IEEE and EDS among the academic community of Sikkim. The mini-colloquium was successful in many ways. First of all it initiated a

new EDS Chapter at Bhubaneswar, with inclusion of new members and attracted a large number of students and faculty members from various academic institutions and attendees from industries. Five EDS Distinguished Lecturers participated and as a result, the new ED Calcutta Chapter was formed.





*Banquet group photo with DLs and organizers of WIMNACT 2008, held at Sikkim Manipal Institute of Technology (SMIT), India*



*WIMNACT 08 group photo with DL speakers Prof. Iwai, Prof. Oda, Prof. Shiraishi, Prof. Deleonibus Simon and Prof. Durga Misra*



*Professor Iwai is introduced in traditional sikkim way and presented with flowers*

After this success, the chapter organized another mini-colloquium (called WIMNACT 2008), held March 6-8, 2008, with the theme, Nano Electronics. The event was supported and jointly organized by EDS chapters from Japan and Bhubaneswar and the IEEE Calcutta Section. Faculty members and students of the host institute, Sikkim Manipal Institute of Technology (SMIT), Majitar, Sikkim, (located outside the metro area of Calcutta), also participated in the WIMNACT. The mini-colloquium was also co-sponsored by the Nalanda Institute of Technology, Bhubaneswar.

WIMNACT 2008 was inaugurated on March 6th by the Vice Chancellor of the Central University of Sikkim, other dignitaries of SMIT and officers of the sponsoring EDS chapters. Five EDS DL speakers presented talks: Professor H. Iwai (Tokyo Institute of Technology, Japan), Professor S. Oda (Tokyo Institute of Technology, Japan), Professor K. Shiraishi (Tsukuba University, Japan), Professor Deleonibus Simon (LETI, France) and Professor Durga Misra (NJIT, USA). Apart from the DL talks, there were invited speakers from different parts of India, who also presented with an objective to expose students to the area of Nano electronics. The students were also given the opportunity to present their own work in the WIMNACT program.

Overall, it was a fruitful experience to bring several academic institutions to take part in this event, with the publicity attracting participants outside the Sikkim area. The quality of the DL talks were extremely good and motivated many to look into the possibility of developing collaborations in the area of Nanoelectronics with institutions belonging to the DLs. The major outcome of WIMNACT – Sikkim was a successful exercise to communicate the message of EDS and IEEE and to encourage the faculty members as well as the students to join. In a similar context of Bhubaneswar, a great effort has already started to form a new EDS chapter at SMIT, Sikkim.

*Chandan K. Sarkar  
ED Calcutta Chapter Chair  
Jadavpur University  
Kolkata, India*



## EDS DISTINGUISHED LECTURERS PARTICIPATE IN THE 15TH WIMNACT JOINTLY HELD IN SHANGHAI AND HANGZHOU

The 15th Workshop and IEEE EDS Mini-colloquium on Nanometer CMOS Technology (WIMNACT) was a twin mini-colloquia (MQ) successfully held on March 24 and 28, 2008, in Shanghai and Hangzhou, China, respectively, which was in conjunction with the 2nd IEEE International Nanoelectronics Conference (INEC'08) in Shanghai March 25-27, 2008. The two half-day MQ are co-sponsored by the EDS Distinguished Lecturer (DL) Program and the ED Shanghai/Hangzhou Chapters with local hosts by the Shanghai Research Institute of Microelectronics (SHRIME), Peking University (PKU) in Shanghai and Zhejiang University in Hangzhou.

Five DL speakers, who are also invitees to INEC'08, presented at the Shanghai MQ, which attracted more than 70 participants from the SHRIME as well as local industries. Prof. Vijay K. Arora of Wilkes University gave a DL talk on "The Role of Scattering-Limited and Ballistic Transport in Performance Evaluation of Nano-CMOS Circuit". Prof. Xing Zhou from Nanyang Technological University (NTU) talked on "Unified Compact Modeling of Emerging Multiple-Gate MOSFETs". Prof. Cher Ming Tan from NTU who is also the general chair of INEC'08, gave the talk on "Modeling of Electromigration for ULSI Interconnections". Prof. Albert Wang's topic was on "RF CMOS SoC", who is from University of California, Riverside. Prof. Yuhua Cheng of SHRIME, who is also the main local organizer, gave the talk on "Design for Manufacturing (DFM) in Nano-CMOS Era". The four DLs (except for Prof. Albert Wang) traveled to Hangzhou, and were joined by Prof. Cary Yang of Santa Clara University, who gave the DL talk on "Failure Mechanisms in Carbon Nanofiber Interconnects" together with the four DL talks at Zhejiang University, Hangzhou. The Hangzhou MQ attracted more than 40 participants with very active discussions during the workshop. Prof. Wenquan Sui, who is with Zhejiang-California International

NanoSystems Institute (ZCNI) as well as Zhejiang University, and Prof. Lingling Sun (chapter chair) and Prof. Wenjun Li, who are with Hangzhou Dianzi University, jointly organized the Hangzhou MQ and the local hospitality.

This joint mini-colloquia event was very successful, especially with the full support of local chapters and institutions as well as in conjunction with a conference at which the DLs are participating. Following the successful joint WIMNACT-13 in Hong Kong and Singapore, this form of MQ sets a good example for promoting technical activities and participation with local chap-

ters. We would like to thank all the local organizers and student helpers in making the twin-MQ a success.

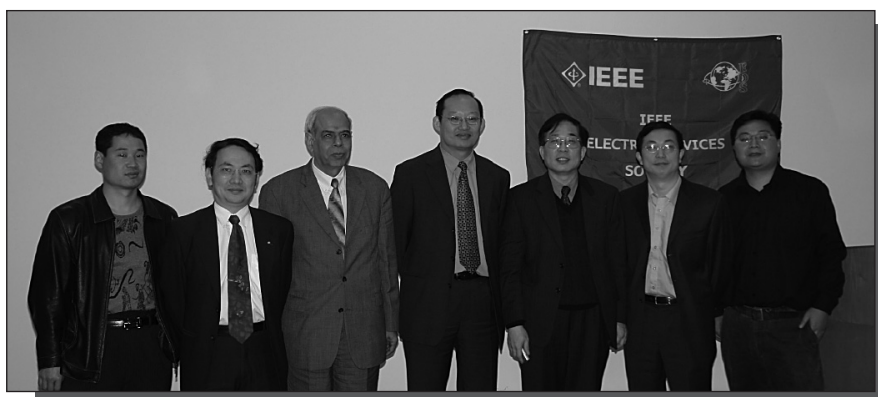
### Co-organizers:

*Xing Zhou*  
EDS SRC Chair for Asia & Pacific  
Nanyang Technological University  
Singapore

*Yuhua Cheng*  
EDS Membership  
Committee Member  
Peking University  
Beijing, China



*DL speakers at WIMNACT-Shanghai. From left to right:  
Albert Wang, Cher Ming Tan, Yuhua Cheng, Vijay Arora, Xing Zhou*



*Organizers and DL speakers at WIMNACT-Hangzhou. From left to right: Haipeng Zhang (chapter secretary-general), Xing Zhou, Vijay Arora, Cher Ming Tan, Yuhua Cheng, Wenquan Sui (organizer), Wenjun Li (chapter secretary)*

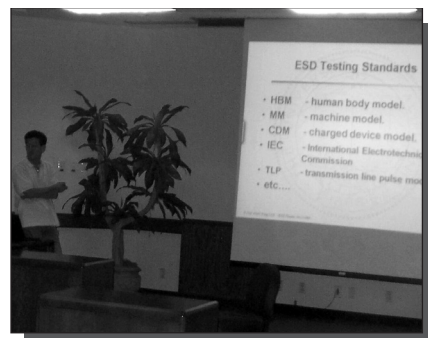
## EDS DISTINGUISHED LECTURER VISITS THE PHOENIX AREA WAVES AND DEVICES CHAPTER

- by Albert Wang

Professor Albert Wang of the University of California, Riverside, and a Distinguished Lecturer for the Solid-State Circuits Society, delivered a talk to the IEEE Waves and Devices (WAD) Chapter at the campus of Freescale Semiconductor in Tempe, Arizona, April 25, 2008. Dr. Wang was invited and hosted by Steve Rockwell of Motorola Labs in Tempe.

Dr. Wang's DL talk, entitled "Advanced ESD Protection Design for

RF/AMS ICs" was well received by over 20 technologists from the Phoenix area, representing Freescale, Motorola, On Semiconductor, Broadcom, and others. Dr. Wang also gave a similar talk at the Arizona State University (ASU) campus to members of the SSC society and held talks with members of Connection One, the National Science Foundation Industry/ University Cooperative Research Center at ASU.



Prof. Wang at the DL WAD talk in Tempe, AZ

## IEEE NANOTECHNOLOGY COUNCIL ANNOUNCES 2008 AWARD WINNERS

IEEE Nanotechnology Council Awards Committee (Chaired by Prof. Chennupati Jagadish) announced its 2008 award winners for IEEE Nanotechnology Pioneer Award, IEEE NTC Distinguished Service Award and IEEE NTC Early Career Award. These awards will be presented at IEEE NANO 2008 in Arlington, Texas in August 2008.

### Nanotechnology Pioneer Award

The NTC Pioneer Award in nanotechnology is to recognize individuals who by virtue of initiating new areas of research, development or engineering have had a significant impact on the field of nanotechnology. The winner of the 2008 award is:

Professor Sajeed John (University of Toronto) for the "Discovery of photonic crystals, their light trapping properties and development of applications"

### Distinguished Service Award

The purpose of the Distinguished Service Award is to recognize an individual who has performed outstanding service for the benefit and advancement of the IEEE Nanotechnology Council. The winner of the 2008 award is:

Ms. Evelyn Hirt (Pacific Northwest National Laboratory) for her "outstanding service to the Council as Vice-President-Conferences, Secretary and many other roles"

### Nanotechnology Early Career Award

The purpose of the Nanotechnology Early Career Award is to recognize individuals who have made contributions with major impact on the field of nanotechnology. The winner of the 2008 award is:

Professor Sanjay Krishna (University of New Mexico) for his contributions to the "Development of quantum dots in a well (DWELL) heterostructures for infrared focal plane arrays"

*Professor Chennupati Jagadish  
IEEE NTC Awards Committee Chair  
Research School of Physical Sciences and Engineering  
The Australian National University  
Canberra, ACT 0200, Australia*

## IEEE EDS MINI-COLLOQUIUM HELD IN TARRAGONA, SPAIN

An IEEE EDS Mini-Colloquium was held in Tarragona, Spain, April 7-9, 2008, as part of the First International Symposium on Flexible Electronics (ISFE). The ISFE Symposium was organized by the Engineering Conferences International (ECI) Foundation and the Universitat Rovira i Virgili (URV, Tarragona, Spain). URV also organized the IEEE EDS Mini-Colloquium that was integrated into the ISFE Symposium. The Chairman of ISFE and the IEEE EDS Mini-Colloquium was Prof. Benjamin Iñiguez, from URV.

The goals of the conference and the IEEE EDS Mini-Colloquium were to present and discuss recent advances in all topics related to flexible electronics, from the material to the circuit and system levels.

Four EDS Distinguished Lecturers gave talks at the IEEE EDS Mini-Colloquium, regarding different topics in the field of Flexible Electronics. Prof. Yue Kuo (Texas A&M University) talked about "Low temperature a-Si:H and poly-Si TFTs for flexible electronics". He examined low temperature a-Si:H and poly-Si TFTs fabrication processes, device characteristics, and reliability for flexible electronics, showing and discussing examples of new and advanced applications that require flexible substrates. In spite of a number of technology challenges, Prof. Kuo concluded that the realization of flexible electronics will enormously extend the semiconductor technology to many new areas.

Professor M. Jamal Deen (McMaster University, Hamilton, ON, Canada) addressed in his talk the "Contacts effects on the charge transport in polymer IC thin-film field-effect transistors (PTFTs)". He reported detailed experimental results and analysis for PTFTs, using the characteristics in the reverse mode of biasing. He showed that the transport characteristics in the reverse mode can be explained



From left to right, Michael S. Shur, Benjamin Iñiguez, Yue Kuo and Jamal Deen.

by a modified MOSFETs linear I-V expression that includes the contact effects and a bulk current. By applying a model based on the theory of space-charge-limited conduction, the dependence of the threshold voltage on the contacts and the shifts observed in the threshold voltage of transistors with different polymer film thicknesses was explained. This model was also applied to explain the effects of light in reducing the contact resistance.

Professor Michael S. Shur (Rensselaer Polytechnic Institute, Troy, NY) conducted a lecture presenting a "Compact capacitance model for thin film transistors with non-ideal contacts". This model is valid for short channel disordered transistors, such as organic TFTs, amorphous Si transistors, and transition metal oxide transistors on rigid and flexible substrates. In all these transistors, the capacitively induced charges affect both the channel and access resistances, and the access contact regions contribute to frequency dispersion of capacitance-voltage characteristics. The new model accounts for the frequency dispersion by introducing the effective carrier transit times under the contacts and in the device channel. The model was successfully compared with the measured capacitance-voltage characteristics of a-Si and zinc-tin-oxide (ZTO) Self-Aligned Imprint Lithography (SAIL) transistors

with channel lengths ranging from 1 to 100  $\mu\text{m}$ .

Professor Benjamin Iñiguez (URV, Tarragona, Spain) presented a work entitled "Variation of the electrical characteristics of PMMA on P3HT polymer TFTs under stress", which was carried out with the collaboration of the group led by Prof. Magali Estrada (EDS Distinguished Lecturer) in CINVESTAV (Mexico). The PMMA on P3HT polymer TFTs were recently demonstrated to show a very low

interface density of charge and a good stability when working in ambient conditions. In his lecture, Prof. Iñiguez analyzed the behaviour of these new devices under two stressing conditions: Gate Bias Stress, when a high gate voltage is applied in low drain voltage conditions, and Stress in Saturation regime, when a high bias is applied to both gate and drain regions. The induced mechanisms that changed the device characteristics were identified. Anyway, the observed variations of the electrical characteristics remain within a range allowing the proper functioning of the device.

The ISFE and the IEEE EDS Mini-Colloquium were attended by more than 40 people, coming both from academia and industry. The social program included one gala dinner and one tourist visit of the historical downtown of Tarragona, which was one of the most important cities in the Roman Empire. Attendees considered the conference as very successful in terms of organization, technical quality of the contributions and opportunities for discussions. As a result of this positive impression, it is planned to organize again the ISFE Symposium and the related IEEE EDS Mini-colloquium in 2009.

*Benjamin Iñiguez  
2008 ISFE Symposium Chair  
Universitat Rovira i Virgili  
Tarragona, Spain*



# REGIONAL AND CHAPTER NEWS

## USA, CANADA & LATIN AMERICA (REGIONS 1-6, 7 & 9)

### 2007 ISDRS

The 2007 International Semiconductor Device Research Symposium (ISDRS) was held at the Stamp Student Union of the University of Maryland, College Park, December 12 – 14, 2007. This is a student-centric, broad technical based symposium held in the Washington, DC area, immediately following the IEDM. There were more than 360 attendees representing 25 states and 27 countries. Technical areas included wide-bandgap materials and devices, optoelectronics, sensors and biosensors, nanoelectronics, space applications, oxides and dielectrics, and modeling and simulations. There were 330 contributed, invit-

ed, and plenary presentations in four parallel sessions. The plenary session had three excellent presentations by: 1) Dr. Robert Chau, Intel Corporation, "The Challenges and Opportunities of Emerging Nanotechnology for Future VLSI Nanoelectronics", 2) Dr. Mark S. Lundstrom, Purdue University, "The Ultimate MOSFET and the Limits of Miniaturization" and 3) Dr. Mark Rosker, Defense Advanced Research Projects Agency (DARPA), "The Coming Revolution in RF Electronics." Dr. Dieter Schroder, Professor of Electrical Engineering at the University of Arizona was presented the van der Zeil Award for his distinguished career as an educator and researcher. The financial sponsors of the Symposium are the Air Force Office of Scientific Research, the National Science Foundation, the National Institute of Standards and Technology, the Army Research Office, the Electrical and Computer Engineering Department of the University of Maryland, and the Nanocenter at the University of Maryland. The Symposium is under the technical sponsorship of the IEEE Electron Devices Society and the IEEE Laser and Electro-Optics Society. Selected papers from the symposium will be published in a special edition of the Journal Solid-State Electronics.

~ **Ibrahim Abdel-Motaleb, Editor**

### ED Ottawa

- **Ram Achar**

EDS Distinguished Lecturer, Prof. Juin J. Liou, visited Silicon Valley North, Ottawa, a tech and innovation hub of Canada, on November 19, 2007. He delivered his distinguished lecture, entitled "Advanced Electrostatic Discharge (ESD) Protection in BiCMOS/CMOS", and discussed ESD issues and advanced protection methodologies in BiCMOS/CMOS circuits. The talk was extremely well received by the Ottawa audience of approximately 21, which included attendees from both the academia and leading industries of Ottawa. The session was highly interactive and the audience greatly benefited from Prof. Liou's lecture and by the depth of the discussions. This talk was organized by the ED Ottawa Chapter (jointly with the CAS/SSCS chapters) and held at Carleton University, Ottawa. The chapter also conducted two other DLs this year.

~ **Jamal Deen, Editor**

### ED South Brazil

- **by Joao Antonio Martino and Marcelo Antonio Pavanello**

In the first semester of 2008, the ED South Brazil Chapter organized the Distinguished Lecturer presentation given by Prof. Siegfried Selberherr, from Technical University of Wien, Austria. Prof. Selberherr proffered the talk "Process Simulation for Mod-



Professor Dieter Schroder received the van der Zeil Award for his distinguished career as an educator and researcher at the International Semiconductor Device Research Symposium, College Park, Maryland, December 13th, from the symposium chair, Dr. Phillip E. Thompson, NRL



Conference Room of Prof. Selberherr at University of Sao Paulo, Brazil



ern Microelectronics Technologies" on February 13th at the University of Sao Paulo, Brazil. This seminar was attended by several graduate and undergraduate students as well as some IEEE members.

In continuation of this semester's activities, the chapter is also organizing the IV SEMINATEC – Workshop on Semiconductors and Micro&Nano Technology, which will be held at the University of Sao Paulo, April 10-11. In this workshop the chapter will contribute with a Distinguished Lecturer presentation by Prof. Francisco Garcia-Sanchez, from Simon Bolivar University, Venezuela.

~**Jacobus W. Swart, Editor**

## EUROPE, MIDDLE EAST & AFRICA (REGION 8)

### EUROSOL

- *Francisco Gamiz*

In 2003, the European Commission supported the formation of a European Network on Silicon on Insulator Technology, Devices and Circuits, whose main goal was to create a discussion forum for the exchange of ideas and results on the topic of Silicon-On-Insulator (SOI) technologies in Europe, and to facilitate the synergy between research groups which enables the use SOI technology as an effective tool to push the limits of CMOS and prepare for post-CMOS. Today, EUROSOL network comprises more than 30 partners all over Europe, with expertise in all the fields of the SOI technology. EUROSOL network successfully organized workshops, training events, scientific exchanges and achieved the EUROSOL roadmap and state of the art documents.

In the framework of the new FP7, a new project, EUROSOL+ as been launched. The first goal of the new project is upgrading and maintaining this important forum, providing upgraded versions of the State-of-the-Art report, Roadmap, facilitating scientific exchanges between partners, organizing workshops and later on, to use it as a launching platform for other important objectives:

- Creation of a Durable European School on SOI Technology.
- Fostering and co-ordinating the initiatives and activities required to successfully face some of the challenges identified and listed in the EUROSOL Roadmap for the future. Promotion of industrial participation in Network activities.
- Co-ordination of the development of a research-dedicated platform in order to address circuit design aspects, focussing on the advantage of SOI technology for Low Power applications. This platform will provide, through the integration at some point in EUROPRACTICE, prototyping and Multi-Projects-Wafers (MPW) in SOI open to European research groups and Fabless Semiconductor companies (SMEs) using LETI SOI process in two-three years.

The kick-off meeting of this new project was held at Tyndall Institute (Cork, Ireland) on January 23-25, 2008. About 70 people attended the workshop, consisting of 6 short courses, 31 oral presentations and 23 posters.

~ **Cora Salm, Editor**

## ASIA & PACIFIC (REGION 10)

### ED Japan

- *by Mitsumasa Koyanagi*

The officers of the ED Japan Chapter retired upon termination of their 2

year term at the end of 2007. For 2008-2009, the chapter has a new chair and staff. They are Prof. Mitsumasa Koyanagi (Tohoku Univ.), Chair; Dr. Shinichiro Kimura (Hitachi Ltd.), Vice-chair; Prof. Tetsu Tanaka (Tohoku Univ.), Secretary; and Dr. Kazuyoshi Torii (Hitachi Ltd.), Treasurer. We would like to thank the former executive officers for their great contributions to the ED Japan Chapter.

On January 8th, the annual meeting of the ED Japan Chapter was held in Tokyo. The new executive officers were introduced to the members. The 2007 activities and the 2008 plans of the chapter were unanimously approved. At the meeting, the 2007 EDS Japan Chapter Student Award was given to four students for their outstanding activities in the research of electron devices last year. They are Kenichi Abe (Tohoku Univ.), Ken Shimizu (Univ. of Tokyo), Toshitake Takahashi (Univ. of Tokyo), and Kazuyuki Hiram (Waseda Univ.). They received the metallic certificate plaques and premiums from Dr. Atsushi Kurobe (Toshiba Corp.), the 2006-2007 chapter chair.

Following the annual meeting on the same day, the briefing session regarding the 2007 IEDM was held. Seven speakers gave summary talks on the highlights of the IEDM. This session has gained widespread popularity among engineers and researchers in Japan who did not have a chance to attend the last IEDM. They obtained the latest information on electron device technologies. The session, with 120 participants, was very successful.



*The committee meeting of the ED Japan Chapter (January, 2008). (front row, left: Dr. Tadashi Nishimura, EDS Kansai Chapter Chair; Prof. Fumio Harashima, IEEE Japan Council Chair; Prof. Mitsumasa Koyanagi, new Chair; Dr. Atsushi Kurobe, ex-Chair; and Dr. Tsutomu Sugawara, IEEE Japan Council Secretary*



Prof. John Roberson and the audience from the ED Japan Chapter seminar

In addition, on January 25th, the ED Japan Chapter provided a seminar to members in the field of work-function control of high-k insulator at Suzukakedai Campus in Tokyo Institute of Technology, Yokohama, Japan. The lecturer was Prof. John Robertson of Cambridge University, and the title of the seminar was, "Work function control in HfO<sub>2</sub> - metal gate stacks". Ideal interfaces without Fermi level pinning, Fermi level pinning effect, SiO<sub>2</sub>+O vacancy model, and layer model were explained. The seminar was very useful for the researchers in the field of high-k metal gate stack technology for advanced integrated circuits.

## ED Kansai

- by Takashi Ipposhi

The ED Kansai Chapter held a Technical Meeting at Kansai University, Kansai University Centenary Memorial Hall, Osaka, Japan, on January 25, 2008. Two prestigious lecturers gave presentations on device technology trends reviewing papers presented at

the 2007 IEEE International Electron Devices Meeting. This is a good opportunity for ED Kansai Chapter members who could not attend IEDM 2007 to learn the most advanced device technology topics. The first talk was on the latest silicon device and process technology trends by Dr. Tomohiro



Prof. Jong-Ho Lee (on left) awarding a recipient (4th from left) their prize

Yamashita (Renesas Technology Corp.). He described topics about the most advanced device technology including high-k and metal gate technology, 32nm-node platform technology, high-performance CMOSFET and new device structure. Especially, the high-k & metal gate technology's having come to be applied to an actual product gave the audience a strong impression. The second speaker was Dr. Yasuhiro Uemoto (Matsushita Electric). He reviewed compound and power semiconductor technology concerning GaN, SiC and other materials. Dr. Hiroshi Kotaki of Sharp Corp. chaired the meeting and the number of participants was 24, including students and researchers from industries.



Technical Meeting at Kansai University on January 25, 2008

## ED Korea

- by Jong-Ho Lee

On February 21, 2008, the chair of the ED Korea Chapter bestowed two recipients with a best paper award at the 15th Korean Conference on Semiconductors. The ED Korea Chapter supports the award annually. The conference is the biggest conference on semiconductors in Korea, and includes semiconductor materials, processes, devices, and integrated circuits. The acceptance rate of oral papers is less than 50% depending on topics. One of the best papers, entitled "Charge storage effect in Si nanoclusters formed by a pulse-type gas feeding method in LPCVD", was presented by Mr. Kyongmin Kim of the University of Seoul and the second paper entitled "Dry etching of GST(225)/TiN films by Cl<sub>2</sub>/Ar etching gases", by Seongsil Cho from Hynix Semiconductors.

## ED/SSC Seoul

- by Kwang Sub Yoon

The IEEE ED/SSCS Seoul Chapter served the third Asian Solid-State Circuits Conference (A-SSCC 2007), held on November 12-14, 2007, in Jeju, Korea, at the Ramada Plaza Hotel on the beautiful island's seashore. The conference is held every year in a region with rapidly growing IC research, production, and sales, such as in Taiwan (2005), China (2006), and Korea (2007). It has provided unique opportunities for IC design experts as well as leaders in technology and business areas to gather in Asia and to exchange ideas and information.



Technical Program Committee members and Organizing Committee members during A-SSCC 2007

The theme of the A-SSCC 2007 was "The Blossoming of IC Design and Business in Asia." The IC sales in Asia reached about US\$135 billion in 2006, approximately 65% of the worldwide IC market. Following the business growth, research and development on IC designs have also been blossoming, as evidenced by the substantial growth of papers submitted from Asia to this conference. The A-SSCC 2007 received 345 paper submissions, from which only 111 papers were selected for presentation. One of the highlights of this conference was to invite four plenary talks presented by distinguished leaders. The first speaker was Dr. Heegook Lee, President and CTO of LG Electronics Inc. (Korea), who gave a speech entitled "The Strategic Considerations for Digital-TV System-on-Chip Products." The second speaker was Prof. Willy Sansen of the Katholieke Universiteit Leuven (Belgium), who

gave a talk entitled "Analog Design Challenges in Nanometer CMOS Technologies." On the second day, the first speaker was Dr. Frank Wen, Board Director and President of UMC (Taiwan), who talked about "Recent Business Models and Technology Trends and Their Impact on the Semiconductor Industry." The last speaker was Dr. Satoru Ito, Chairman of Renesas Technology Corp. (Japan), who talked on "Convergence and Divergence in Parallel for the Ubiquitous Era."

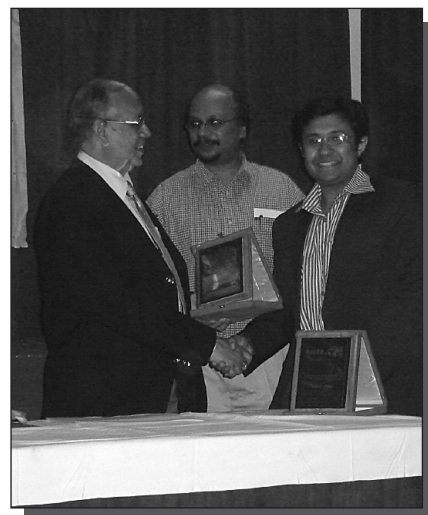
As to A-SSCC's collaboration with the Journal of Solid-State Circuits (JSSC), and the International Solid-State Circuits Conference (ISSCC), some of the technical papers selected from the A-SSCC will be printed in a special edition of JSSC after being carefully reviewed. Also, the best three Student Design Contest papers were presented at the ISSCC 2008.

~ Kazuo Tsutsui, Editor

## ED Bangladesh

- by Anisul Haque

The award giving ceremony of the Student Paper Contest 2007, organized by the IEEE ED Bangladesh Chapter, was held on February 12, 2008, at the Bangladesh University of Engineering and Technology (BUET). Prof. A. M. M. Safiullah, Vice Chancellor, BUET, gave away the awards. The awards included certificates, crests and one year complimentary membership for IEEE and EDS. A proceeding of the Student Paper Contest was published with nine student papers. The first and the second prize winners also presented their works in the ceremony.



Prof. A. M. M. Safiullah, presenting the 2007 IEEE ED Bangladesh Chapter Student Paper Contest award to the first prize winner, Md. M. Satter

### Winners of the IEEE ED Bangladesh Chapter Student Paper Contest 2007

<b>First Prize</b>	Md. M. Satter and A. Haque	Effects of Non-uniform Interface Trap States Distribution on the Gate C-V Characteristics of MOS Devices with Ultrathin High-K Gate Dielectrics
<b>Second Prize</b>	M. K. Alam and Quazi D. M. Khosru	On the Self-Consistent Calculation of Ultra Thin Body Double Gate MOSFET
<b>Honorable Mention</b>	Md. Itrat Bin Shams	Improved Compact Gate C-V Model for High-k gate Dielectrics Using Modified Airy Function Solution
<b>Honorable Mention</b>	Md. Tanvir Hasan, M. Majharul Haque, Tapon Paul, M. Galib Hasan and Ashraful G. Bhuiyan	InN-based High Electron Mobility Transistors (HEMTs)
<b>Honorable Mention</b>	Samia Nawar Rahman, Hasan Mohammad Faraby and Md. Manzur Rahman	A Theoretical Analysis of Electrostatic Properties of <110> Uniaxially Strained Silicon n Channel MOSFET



## ED Delhi

- by R. S. Gupta

The IEEE ED Delhi Chapter was formed in March 2007 with its first Annual General Meeting held April 29, 2007, where office bearers were elected with Professor R. S. Gupta as chairman. The chapter had its first executive meeting on June 18, 2007, followed by two more in the month of December to discuss the organization of the Mini-Colloquium.

The chapter organized three IEEE DL talks throughout the year:

1. Prof. Vijay K. Arora from Division of Engineering, Wilkes University, Wilkes-Barre, USA, on "Failure of Ohm's Law: Its Implications on the Design of Nanoelectronic Devices and Circuits", November 5, 2007
2. Dr. Ashok K. Kapoor, TSMC, on "Growth of Semiconductor Technology driven by the needs of information Technology", July 9, 2007
3. Dr. M. K. Radhakrishnan (EDS Chapter Partner & Point of Contact for EDS Chapters in South-Asia), on "Nanoelectronic Devices – Analysis Challenges" on February 9, 2008

A Mini-colloquium on "Compact modeling of advance MOSFET structures and mixed mode applications" was organized on January 5-6, 2008, sponsored by the IEEE Electron Devices Society under its Distinguished Lecturer Program. Five IEEE Distinguished Lectures and 20 student poster presentations were held apart from a technical talk on "*Extraction of  $D_{it}$  and its frequency dependence in Nitrided Tunnel oxides using MOS Capacitors and MOSFETs*", by Professor K. N. Bhat, Indian Institute of Science, Bangalore, India. Nearly 50 participants from all over India attended the mini-colloquium.

IEEE-Distinguished Lecturer talks on January 5, 2008:

- i. "*Interconnect Design Issues of Nano CMOS*", by Professor Kazuya Masu from Integrated Research Institute, Tokyo Institute of Technology, Nagatsuta, Yokohama, Japan.
- ii. "*Physics Technology and performance of high speed CMOS technologies*", by Dr. Sunit Tyagi from Intel India technology Private Limited, Bangalore, Karnataka, India.

iii. "Silicon quantum dots: the future of electronics" by Professor Shunri Oda from Quantum Nanoelectronics, Research Center Tokyo Institute of Technology, O-okayama, Meguro-ku, Tokyo, Japan.

iv. "*Device Design and Optimization for Nanoscale and Multi-gate MOSFETs*" by Professor V. Ramgopal Rao from Dept. of Electrical Engineering, IIT Bombay, Powai, Mumbai, India.

IEEE-Distinguished Lecturer talk on January 6, 2008:

- i. "*Nano-Electronic Devices based on Silicon MOS Structure*" by Professor C. K. Sarkar from Jadavpur University, Dept. of Electronics and Telecommunication, Calcutta, India.

After the Mini-Colloquium two more Executive Committee meetings were held with Dr. Renuka P. Jindal, EDS President-Elect, on January 11, 2008, and with Dr. M. K. Radhakrishnan, EDS Chapter Partner & Point of Contact for EDS Chapters in South-Asia, on February 9, 2008.

## ED SJCE Student Branch Chapter

- by P. M. Pavan

*Knowledge is Power. Quest for knowledge is divine.*

Sharing of knowledge has been an everlasting pursuit of this student branch.

### ROBOTICS WORKSHOP:

A two-day hands-on workshop on Robotics was organized on February 9th and 10th 2008 in association with TechSouls. The workshop aimed to empower students with the basics of robotics and provided essential guidelines to build a robot.

The various aspects covered in the workshop included:

- Programming aspects of Robotics and Embedded C.
- Hardware aspects using a computing platform, 'Arduino'.
- Mechanical aspects of designing the Chassis and Sensors.
- Using simulation Software in development of a Robot.

It was indeed an exciting platform for the young and the enthusiastic students to get acquainted with the field of robotics. The robots coming alive with the efforts of the students were indeed an achievement by itself.

### EVENTS BY ED SJCE FOR CYBERIA'08:

CYBERIA'08, the National Level Technical Fest by IEEE ED SJCE, had a major contribution to this through the events Robo Eureka and Embed Me.

Also EDS built an efficient scroll board for the display of the event details which again proved the technical proficiency of the ED SJCE Student Branch.

### ROBO-EUREKA:

To challenge the alchemist lurking in the convolutions of grey matter, Robo-Eureka was introduced for the first time this year. What really mattered in this contest was the enhancement of the three basic actions of a robot – sensing, thinking, and movement. The contest was judged on the basis of innovation, cost reduction, and practical applicability. Fifteen abstracts were submitted for the initial round, out of which 5 made it to a physical realization of the robots.

### EMBED Me:

EMBED Me was another contest organized by IEEE ED SJCE for Cyberia'08.

EMBED Me was an assembly level programming contest where perceptive programmers were asked to write a program for a given problem statement. 30 participants exploited their skills in the prelims and 5 finalists were bestowed with the opportunity to display their programming expertise.

### TALK ON "HOW GOOGLE SEARCH ENGINE WORKS?" by Dr. C. S. Yogananda:

A talk on "How Google Search Engine works" by Dr. C. S. Yogananda, Head of Department of Mathematics, SJCE, was organized on March 11, 2008.

Enumerating the various mathematical algorithms involved, it was indeed a thought-provoking talk bringing into lime light the various aspects involved in it. It paved the way for students to realize the intricate problems of a search engine, which also ignited students to take up projects in quest for



the better solutions for a few of the minor problems.

#### WORKSHOP ON MICRO-CONTROLLER:

A modular workshop on the 8051 Microcontroller is being held every week by Mr. Arun Raj, a 6th semester student from the department of Instrumentation Technology. A basic overview will be followed by the implementation of the acquired knowledge into the project by each group of students involved in this workshop.

*IEEE ED SJCE indeed strives endlessly for technical excellence. With an explicit blend of knowledge and zeal, all the endeavors have been fruitful. This semester has added yet another feather to the cap of the IEEE ED SJCE*

*Student Branch Chapter.*

#### REL/CPMT/ED Singapore

*- by Alastair Trigg*

In February 2008, the Chapter organized a EDS DL talk by Prof. J. J. Liou of the University of Central Florida, USA, on Electrostatic Discharge (ESD) Protection for RF ICs.

Planning is well underway for the Chapter's flagship conference, The International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA), which will be held in Singapore on July 7-11, 2008, and will comprise two days of tutorials followed by three days of technical sessions. An equipment exhibition will be held in conjunction with the technical sessions.

The technical sessions will begin with two keynote papers on "Trends and Requirements of Future High-Performance CMOS" by Prof Dimitri Antoniadis; MIT, USA, and another packaging-related keynote by Dr. Raj Master, AMD, USA.

Full details of IPFA 2008 can be found at the website: <http://ewh.ieee.org/reg/10/ipfa>

The Chapter's other flagship conference, EPTC 2008, will be held in Singapore from December 9-12, 2008. The abstract submission deadline was May 15, 2008. Full details of EPTC can be found at the website: <http://www.eptc-ieee.net/>

*~ Xing Zhou, Editor*



#### QUEST EDS



QuestEDS is an EDS member benefit service where EDS members can submit questions online concerning the EDS field of interest and can view online the answers provided by experts in the field.

Questions and answers are posted online in QuestEDS Questions and Answers within two weeks.

**Why QuestEDS?** Technological advancements dictate how we do business in this information age. This is especially true in the publication world where access to the world-wide-web has resulted in a paradigm shift. Libraries have relinquished their role as portals of technical information, their function being taken over by web portals via your desktop or laptop. Making this information available almost for free presents unique challenges to professional societies such as IEEE EDS. One of our traditional values as a provider of highly-prized technical information is being eroded. We feel that one way to inject new value in the membership is via QuestEDS. This new service provides a means of fulfilling the needs of our members by yet another level of service which has hitherto not existed.

As an EDS member, simply by logging on to the web-site, you can ask questions on any technical matter within the Field-of-Interest of EDS. The methodology to process these requests is parallel to the way we handle submission of a manuscript to our publications. The questions will be handled by an editor with the authority of outright rejection if in the judgment of the editor the question is outside the Field-of-Interest of EDS, is a request for evaluation of competing commercial products, or help on a take-home exam or the like. Experts within and outside IEEE will be consulted. Our goal is to provide a timely response in TWO WEEKS. The response will be posted on the QuestEDS webpage accessible to EDS members, but without explicit reference to either the source of the question or the answer.

We hope to enhance the value of EDS membership by this new service making this society more meaningful globally to technical professionals including academicians, practicing engineers, researchers and students. We would like to hear from you, whether you are pleased with this new service or have suggestions on how to enhance it further. Please click the feedback button to send your valued input.

*R.P. Jindal  
EDS Vice-President of Publications  
IEEE Electron Devices Society*

Please visit the EDS website at: <http://www.ieee.org/portal/pages/society/eds/membership/QuestEDS.html>, to take advantage of this new tool.

# EDS MEETINGS CALENDAR

## (AS OF MAY 15, 2008)

THE COMPLETE EDS CALENDAR CAN BE FOUND AT OUR WEB SITE:  
[HTTP://WWW.IEEE.ORG/SOCIETY/EDS/MEETINGS/MEETINGS\\_CALENDAR.XML](http://www.ieee.org/society/eds/meetings/meetings_calendar.xml) PLEASE VISIT!

July 1 - 5, 2008, T **International Siberian Workshop and Tutorial on Electron Devices and Materials**, Location: Novosibirsk State Technical University, Novosibirsk, Russia, Contact: Alexander Gridchin, E-Mail: ieeensk@yandex.ru, Deadline: 3/15/08, www: <http://www.nstu.ru/edm>

July 1, 2008, T **Conference on Optoelectronic and Microelectronic Materials & Devices**, Location: Sidney, Australia, Contact: Chennupati Jagadish, E-Mail: chennupati.jagadish@anu.edu.au, Deadline: Not Available, www: Not Available

July 6 - 11, 2008, T **International Conference on High-Power Particle Beams**, Location: Inst. Of Fluid Physics China Academy of Eng. Phys., Xian, China, Contact: JianJun Deng, E-Mail: djleap@my-public.sc.cninfo.net, Deadline: 2/29/08, www: <http://ifp.caep.ac.cn/beams2008/>

July 7 - 11, 2008, T **IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits**, Location: Grand Copthorne Waterfront Hotel, Singapore, China, Contact: Chih-Hang Tung, E-Mail: chihhang@ime.a-star.edu.sg, Deadline: 1/18/08, www: <http://ewh.ieee.org/reg/10/ipfa/>

July 13 - 16, 2008, T **University/Government/Industry Microelectronics Symposium**, Location: University of Louisville, Louisville, KY, USA, Contact: Kevin Walsh, E-Mail: walsh@louisville.edu or walsh@ieee.org, Deadline: 4/21/08, www: [www.louisville.edu/micronano/](http://www.louisville.edu/micronano/) UGIM2008

July 13 - 17, 2008, @ **IEEE International Vacuum Nanoelectronics Conference**, Location: Wroclaw University, Wroclaw, Poland, Contact: Jan Dziuban, E-Mail: jan.dziuban@pwr.wroc.pl, Deadline: 4/5/08, www: [www.wemif.pwr.wroc.pl/ivnc](http://www.wemif.pwr.wroc.pl/ivnc)

July 21 - 25, 2008, T **European Electromagnetics Conference**, Location: Swiss Federal Inst. Of Technology, Lausanne, Switzerland, Contact: Farhad Rachidi, E-Mail: farhad.rachidi@epfl.ch, Deadline: 1/31/08, www: [www.euroem.org](http://www.euroem.org)

July 27 - August 1, 2008, T **International Conference on the Physics of Semiconductors**, Location: Rio de Janeiro, Brazil, Contact: ICPS, E-Mail: icps2008@cetuc.puc-rio.br, Deadline: 3/1/08, www: [www.icps2008.org](http://www.icps2008.org)

August 3 - 6, 2008, @ **International Vacuum Electron Sources Conference**, Location: Queen Mary, University of London, London, United Kingdom, Contact: Asim Ray, E-Mail: a.k.ray@qmul.ac.uk, Deadline: 6/9/08, www: <http://www.materials.qmul.ac.uk/conferences/ivesc2008/>

August 3 - 8, 2008, T **IEEE International Conference on Molecular Beam Epitaxy**, Location: University of British Columbia, Vancouver, BC, Canada, Contact: Tom Tiedje, E-Mail: ttiedje@phas.ubc.ca, Deadline: 4/1/08, www: [www.mbe2008.ca](http://www.mbe2008.ca)

August 4 - 6, 2008, T **International Symposium on Low-Power Electronics and Design**, Location: Bangalore, India, Contact: Vijaykrishnan Narayanan, E-Mail: vijay@cse.psu.edu, Deadline: Not Available, www: [www.islpd.org](http://www.islpd.org)

August 5 - 7, 2008, T **Lester Eastman Biennial Conference on High Performance Devices**, Location: University of Delaware, Newark, DE, USA, Contact: Michael Shur, E-Mail: shurm@rpi.edu, Deadline: 5/1/08, www: <http://nina.ecse.rpi.edu/shur/EastmanConference/>

August 18 - 22, 2008, \* **IEEE International Conference on Portable Information Devices**, Location: University of Jyväskylä Convention Center, Jyväskylä, Finland, Contact: Ephraim Suhir, E-Mail: suhire@aol.com, Deadline: 3/15/08, www: [www.portable2008.com](http://www.portable2008.com)

August 18 - 21, 2008, T **IEEE Conference on Nanotechnology**, Location: Sheraton Hotel & Arlington Convention Center, Arlington, TX, USA, Contact: Supriyo Bandyopadhyay, E-Mail: sbandy@vcu.edu, Deadline: 11/16/07, www: [http://www.ewh.ieee.org/r5/fort\\_worth/nano2008.html](http://www.ewh.ieee.org/r5/fort_worth/nano2008.html)

August 20 - 24, 2008, T **International Conference on Hot-Wire (Cat-CVD) Process**, Location: MIT, Cambridge, MA, USA, Contact: Karen Gleason, E-Mail: kkgleasn@mit.edu, Deadline: 1/15/08, www: <http://web.mit.edu/hwcvd5/>

September 4 - 8, 2008, T **Symposium on Microelectronics Technology & Devices**, Location: Rio Othon Palace, Gramado, Brazil, Contact: Jacobus Swart, E-Mail: jacobus@fee.unicamp.br, Deadline: 3/19/08, www: [www.sbmicro.org.br/sbmicro](http://www.sbmicro.org.br/sbmicro)

September 7 - 11, 2008, T **Electrical Overstress/Electrostatic Discharge Symposium**, Location: Westin La Paloma, Tucson, AZ, USA, Contact: Lisa Pimpinella, E-Mail: info@esda.org, Deadline: 1/11/08, www: <http://www.esda.org/index.htm>

September 8 - 12, 2008, T **International Crimean Microwave Conference "Microwave & Telecommunication Technology"**, Location: Sevastopol National Technical University, Sevastopol, Ukraine, Contact: Sergey Smolskiy, E-Mail: smolskiys@mail.ru, Deadline: 5/20/08, www: [www.crimico.org](http://www.crimico.org)

September 9 - 11, 2008, @ **International Conference on Simulation of Semiconductor Processes and Devices**, Location: Yumoto Fujiya Hotel, Hakone-machi, Japan, Contact: Kazuya Matsuzawa, E-Mail: kazuya.matsuzawa@toshiba.co.jp, Deadline: 3/1/08, www: <http://www6.eie.eng.osaka-u.ac.jp/sis-pad/2008/>

September 15 - 19, 2008, T **European Solid-State Device Research Conference**, Location: Edinburgh International Conference Centre, Edinburgh, Scotland, Contact: Anthony Walton, E-Mail: anthony.walton@ee.ed.ac.uk, Deadline: 4/5/08, www: <http://www.essdrc2008.org/>

September 21 - 24, 2008, T **IEEE Custom Integrated Circuits Conference**, Location: Double Tree Hotel, San Jose, CA, USA, Contact: Melissa Widerkehr, E-Mail: melissaw@widerkehr.com, Deadline: Not Available, www: <http://www.ieee-cicc.org>

September 22 - 24, 2008, T **International Symposium on Ultra Clean Processing of Silicon Surfaces**, Location: Oud Sint-Jan Conference Center, Bruges, Belgium, Contact: Professional Conference Organizer MOMENTUM, E-Mail: ucps@momentum-pco.be, Deadline: 3/31/08, www: <http://ucps.org/>

September 22 - 25, 2008, T **IEEE International Seminar/Workshop on Direct and Inverse Problems of Electromagnetic and Acoustic Wave Theory**, Location: Tbilisi State University, Tbilisi, Ukraine, Contact: Mykhalyo Andriychuk, E-Mail: andr@iapmm.lviv.ua, Deadline: 8/1/08, www: [www.ewh.ieee.org/soc/qpm/ukraine](http://www.ewh.ieee.org/soc/qpm/ukraine)

September 23 - 26, 2008, T **International Conference on Solid-State Devices and Materials**, Location: Tsukuba International Congress Center, Ibaraki, Japan, Contact: Naomi Kutsuna, E-Mail: ssdm@intergroup.co.jp, Deadline: 5/8/08, www: [www.ssdm.jp](http://www.ssdm.jp)

September 24 - 25, 2008, T **International Conference on Actual Problems of Electron Device Engineering**, Location: Saratov State Technical University, Saratov, Russia, Contact: Natalia Akafieva, E-Mail: alexm@sstu.ru, Deadline: 6/1/08, www: [http://www.apede2008.sstu.ru/strmain\\_eng.html](http://www.apede2008.sstu.ru/strmain_eng.html)

September 26 - 28, 2008, T **International Symposium on Advanced Gate Stack Technology**, Location: Not Available, Contact: Cassandra Muse, E-Mail: cassandra.muse@sematech.org, Deadline: Not Available, www: Not Available

September 29 - October 2, 2008, T **European Symposium on Reliability of Electron Devices, Failure Physics and Analysis**, Location: Maastrichts Expositie & Congress Centrum (MECC), Maastricht, The Netherlands, Contact: Jaap Bisschop, E-Mail: jaap.bisschop@nxp.com, Deadline: 4/30/08, www: www.esref.org

September 30 - October 3, 2008, T **International Conference on Advanced Thermal Processing of Semiconductors**, Location: The Platinum Hotel & Spa, Las Vegas, NV, USA, Contact: Bo Lojek, E-Mail: blojek@atmel.com, Deadline: 5/31/08, www: www.ieee-rtp.org

October 6 - 9, 2008, \* **IEEE International SOI Conference**, Location: Mohonk Mountain House, New Paltz, NY, USA, Contact: Bobbi Armbruster, E-Mail: bobbi@bacmnc.com, Deadline: 5/2/08, www: www.soiconference.org

October 12 - 16, 2008, T **International Conference on Advanced Semiconductor Devices and Microsystems**, Location: Smolenice Castle, Smolenice, Slovak Republic, Contact: Jozef Osvald, E-Mail: elekosva@savba.sk, Deadline: 4/15/08, www: Not Available

October 12 - 15, 2008, T **IEEE International Conference on Computer Design**, Location: Resort at Squaw Creek, Lake Tahoe, CA, USA, Contact: Kevin Rudd, E-Mail: Kevin.w.rudd@intel.com, Deadline: 5/9/08, www: www.iccd.et.tudelft.nl

October 12 - 16, 2008, \* **IEEE International Integrated Reliability Workshop**, Location: Stanford Sierra Conference Center, South Lake Tahoe, CA, USA, Contact: Roy and Becky Walker, E-Mail: roy@sar101.com, Deadline: 7/11/08, www: http://www.iirw.org

October 12 - 12, 2008, T **Reliability of Compound Semiconductors Workshop**, Location: Portola Plaza Hotel, Monterey, CA, USA, Contact: Anthony Immorlica, E-Mail: anthony.a.immorlica@baesystems.com, Deadline: 8/4/08, www: www.jedec.org/home/gaas

October 12 - 15, 2008, \* **IEEE Compound Semiconductor IC Symposium**, Location: Monterey Portola Plaza, Monterey, CA, USA, Contact: Mohammad Madhian, E-Mail: madih@mve.biglobe.ne.jp, Deadline: 5/12/08, www: www.csics.org

October 13 - 15, 2008, \* **International Semiconductor Conference**, Location: Sinaia Hotel, Sinaia, Romania, Contact: Cristina Buiculescu, E-Mail: cas@imt.ro, Deadline: 6/1/08, www: http://www.imt.ro/CAS

October 13 - 15, 2008, T **IFIP International Conference on Very Large Scale Integration**, Location: Democritus University of Thrace, Rhode Island, Greece, Contact: Dimitrios Soudris, E-Mail: dsoudres@ee.duth.gr, Deadline: 3/28/08, www: http://vlsi.ee.duth.gr/vlsisoc-2008/

October 13 - 16, 2008, @ **IEEE Bipolar/BiCMOS Circuits and Technology Meeting**, Location: Monterey Portola Plaza, Monterey, CA, USA, Contact: Janice Jopke, E-Mail: ccsevents@comcast.net, Deadline: 3/17/08, www: www.ieee-bctm.org

October 20 - 23, 2008, T **International Conference on Solid-State & Integrated Circuits Technology**, Location: Beijing Jingyan Hotel, Beijing, China, Contact: Yang-Yuan Wang, E-Mail: yyw@ime.pku.edu.cn, Deadline: 5/31/08, www: www.ime.pku.edu.cn/icsit

October 26 - 29, 2008, T **IEEE International Conference on Sensors**, Location: Grand Hotel Tiziano e dei Congressi, Lecce, Italy, Contact: Roma Multiservizi S.r.l., E-Mail: info@romamultiservizi.com, Deadline: 4/11/08, www: www.ieee-sensors2008.org

October 27 - 30, 2008, T **International Microprocesses and Nanotechnology Conference**, Location: JAL Resort Sea Hawk Hotel, Fukuoka, Japan, Contact: Hiroaki Masuko, E-Mail: secretariat@imnc.jp, Deadline: Not Available, www: www.imnc.jp

October 27 - 29, 2008, T **IEEE European Microwave Integrated Circuits Conference**, Location: RAI Congress Centre, Amsterdam, The Netherlands, Contact: Frank Van Vliet, E-Mail: frank.vanvliet@tno.nl, Deadline: 2/24/08, www: www.eumw2008.com

November 5 - 7, 2008, T **Dielectric Thin Films for Future ULSI Devices: Science and Technology**, Location: Tokyo Institute of Technology, Meguro-ku, Japan, Contact: Jiro Yugami, E-Mail: yugami.jiro@renesas.com, Deadline: 7/25/08, www: http://home.hiroshima-u.ac.jp/iwdf

November 10 - 13, 2008, T **IEEE International Conference on Computer Aided Design**, Location: Double Tree Hotel, San Jose, CA, USA, Contact: Kathy Embler, E-Mail: kathy@dac.com, Deadline: 4/14/08, www: http://www.iccad.com

November 11 - 14, 2008, T **Non-Volatile Memory Technology Symposium**, Location: Asilomar Conference Grounds, Pacific Grove, CA, USA, Contact: Kristy Campbell, E-Mail: kriscampbell@boisestate.edu, Deadline: 6/2/08, www: www.nvmts.org

November 12 - 14, 2008, T **International Conference on Electrical Engineering, Computing Science and Automatic Control**, Location: Research Center CINVESTAV-IPN, Mexico City, Mexico, Contact: Judith Esparza-Azcoitia, E-Mail: iceee@cinvestav.mx, Deadline: 6/16/08, www: http://cce.cinvestav.mx

December 8 - 10, 2008, T **International Conference on Field-Programmable Technology**, Location: Grand Formosa Regent, Taipei, Taiwan, Contact: Wai-Kei Mak, E-Mail: wkmak@cs.nthu.edu.tw, Deadline: 6/9/08, www: http://www.icfpt.org

December 11 - 13, 2008, \* **IEEE Semiconductor Interface Specialists Conference**, Location: Catamaran Hotel Resort, San Diego, CA, USA, Contact: Martin Frank, E-Mail: mmfrank@us.ibm.com, Deadline: 7/25/08, www: http://www.ieeesisc.org

December 14 - 16, 2008, T **International Conference on Microelectronics**, Location: Millennium Hotel, Sharjah, United Arab Emirates, Contact: Mohab Anis, E-Mail: manis@vlsi.uwaterloo.ca, Deadline: 5/1/08, www: www.ieee-icm.com

December 15 - 17, 2008, \* **IEEE International Electron Devices Meeting**, Location: Hilton San Francisco and Towers, San Francisco, CA, USA, Contact: Phyllis Mahoney, E-Mail: phyllism@widerkehr.com, Deadline: June 2008, www: http://www.ieee.org/conference/iedm

March 27 - 28, 2009, T **IEEE International Siberian Conference on Control and Communication**, Location: Tomsk State University of Control Systems, Tomsk, Russia, Contact: Sergei Lukianov, E-Mail: ieee@main.tsur.ru, Deadline: 12/10/08, www: www.comsoc.org/tomsk

March 30 - April 2, 2009, @ **International Conference on Microelectronic Test Structures**, Location: Embassy Suites Mandalay Beach Resort, Oxnard, CA, USA, Contact: Wendy Walker, E-Mail: wendyw@widerkehr.com, Deadline: 9/15/08, www: http://www.see.ed.ac.uk/ICMTS

May 10 - 14, 2009, @ **IEEE International Conference on Indium Phosphide and Related Materials**, Location: Marriott Newport Beach Hotel & Spa, Newport Beach, CA, USA, Contact: Mary Hendrickx, E-Mail: m.hendrickx@ieee.org, Deadline: Not Available, www: http://www.i-leos.org

June 14 - 18, 2009, @ **TRANSDUCERS - International Conference on Solid-State Sensors, Actuators and Microsystems**, Location: Adams Mark Hotel, Denver, CO, USA, Contact: Khalil Najafi, E-Mail: najafi@eecs.umich.edu, Deadline: Not Available, www: http://www.transducers09.org/

September 15 - 19, 2009, T **European Solid-State Device Research Conference**, Location: Athens, Greece, Contact: E-Mail: Not Available, Deadline: Not Available, www: http://www.essdrc.org/en/page/ess07.aspx

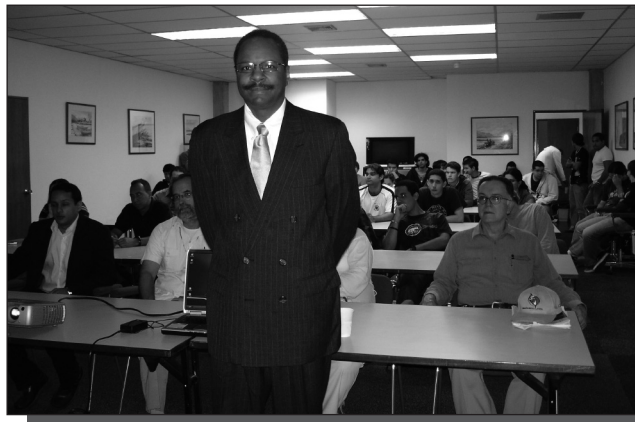
December 7 - 9, 2009, \* **IEEE International Electron Devices Meeting**, Location: Washington Hilton and Towers, Washington, DC, USA, Contact: Phyllis Mahoney, E-Mail: phyllism@widerkehr.com, Deadline: Not Available, www: http://www.ieee.org/conference/iedm

## EDS DISTINGUISHED LECTURER VISITS VENEZUELA

Venezuela's CAS/ED/PEL Joint Chapter continued with its series of seminars and workshops. On Thursday, 28 February 2008, it organized a two-hour technical seminar at Simón Bolívar University, Caracas, entitled "Applications and Trends in RF MEMS." Dr. Hector J. De Los Santos, President and CTO of NanoMEMS Research, LLC, Irvine, CA, was the special invited speaker for this occasion. Dr. De Los Santos is well known internationally for his R&D activities in Nanoelectromechanical Quantum Circuits and Systems and RF MEMS (NanoMEMS). He is an IEEE Fellow and IEEE EDS Distinguished Lecturer. Dr. De Los Santos holds 16 US patents, and is author of best-seller textbooks, including Introduction to Microelectromechanical (MEM) Microwave Systems (1999), now in Artech House IPF® (In-Print-Forever®) series, and RF MEMS Circuit Design for Wireless Communications (2001). His most recent book, Principles and Applications of NanoMEMS Physics, was published by Springer in 2005.

The seminar presented a comprehensive and up-to-date description

of Microelectromechanical Systems (MEMS) applications in RF and microwave electronics and its revolutionizing impact in wireless communications. In particular, the ability



*Dr. De Los Santos during his presentation held at Simón Bolívar University, Caracas, Venezuela*

of MEMS' fabrication techniques to enhance the performance of passive components, e.g., capacitors, inductors, transmission lines, and switches, was addressed, and a number of potential wireless system opportunities, namely, wireless transceivers, routing networks, and tracking antennas for mobile multimedia communications, awaiting the matu-

ration of MEMS, were discussed. The seminar concluded with the unveiling of several new opportunities for innovation in the fields of electronics and medicine afforded by the imminent evolution of miniaturized mechanical systems into the quantum regime, NanoMEMS.

More than 50 university faculty members and graduate and undergraduate students, from various universities in Venezuela, attended the seminar. There was a very active participation of the audience, and the many interesting questions and answers motivated additional informal meetings, which took place after the conclusion of the official seminar. The previous day, Dr. De Los Santos met with different research groups of Simón Bolívar University to discuss ongoing research activities.

For additional information contact Professor Adelmo Ortiz-Conde at [ortizc@ieee.org](mailto:ortizc@ieee.org).

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