IEEE
ELECTRON DEVICES SOCIETY
Newsletter

JULY 2019 VOL. 26, NO. 3 ISSN: 1074 1879 EDITOR-IN-CHIEF: CARMEN M. LILLEY

Table of Contents

100th Issue!

Celebrating 25 Years of Renewed Publishing 1994–2019

IEEE

Your Comments Solicited

Your comments are most welcome. Please write directly to the Editor-in-Chief of the Newsletter at clilley@uic.edu

ELECTRON DEVICES SOCIETY

EDS Board of Governors (BoG)
Elected Members-at-Large

Elected for a three-year term (maximum two terms) with 'full' voting privileges

2019	Term	2020	Term	2021	Term
Joachim N. Burghartz	(1)	Roger Booth	(1)	Paul Berger	(1)
Ru Huang	(2)	Mukta Farooq	(2)	Navakanta Bhat	(2)
Shuji Ikeda	(1)	Edmundo A. Gutierrez-D.	(1)	Maria De Souza	(1)
Meyya Meyyappan	(1)	Benjamin Iniguez	(1)	Kazunari Ishimaru	(1)
Arokia Nathan	(1)	Carmen M. Lilley	(2)	William (Bill) Nehrer	(1)
Jacobus W. Swart	(2)	Durga Misra	(2)	Murty Polavarapu	(2)
Bin Zhao	(1)	Manoj Saxena	(1)	Camilo Velez Cuervo	(1)
		Sumant Sood	(1)		

IEEE prohibits discrimination, harassment, and bullying. For more information, visit http://www.ieee.org/web/aboutus/whatis/policies/p9-26.html.

NEWSLETTER EDITORIAL STAFF

CONTRIBUTIONS WELCOME

Readers are encouraged to submit news items concerning the Society and its members. Please send your ideas/articles directly to either Editor-in Chief or the Regional Editor for your region. The e-mail addresses of all Regional Editors are listed on this page. E-mail is the preferred form of submission.

NEWSLETTER DEADLINES

Issue	Due Date
July	April 1st
October	July 1st
January	October 1st
April	January 1st

The EDS Newsletter archive can be found on the Society web site at http://eds.ieee.org/eds-newsletters.html. The archive contains issues from July 1994 to the present.

IEEE Electron Devices Society Newsletter (ISSN 1074 1879) is published quarterly by the Electron Devices Society of the Institute of Electrical and Electronics Engineers, Inc. Headquarters: 3 Park Avenue, 17th Floor, New York, NY 10016–5997. Printed in the U.S.A. One dollar ($1.00) per member per year is included in the Society fee for each member of the Electron Devices Society. Periodicals postage paid at New York, NY and at additional mailing offices. Postmaster: Send address changes to IEEE Electron Devices Society Newsletter, IEEE, 445 Hoes Lane, Piscataway, NJ 08854.

EDS Newsletter Notable 'Firsts'

JULY 1994

Society renews publishing newsletter after a 10-year hiatus

FOUNDING EDITOR 1994-2002

Krishna Shenai

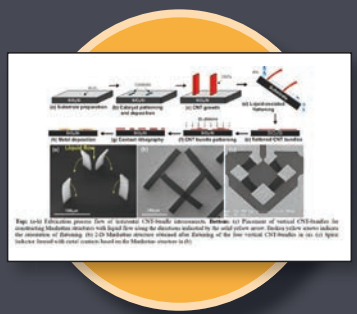
Strategic Improvements in Design and Content

MID 1990s

Goals to enhance membership value, increase society membership and improve chapter relationships

EDITOR-IN-CHIEF 2012-2017

M. K. Radhakrishnan



APRIL 2014

New content – technical briefs, young professionals, and recognition of outstanding chapters

JULY 2014

New Flipbook version developed for mobile devices

EARLY 2000s

Electronic archive created on Society website

EDITOR-IN-CHIEF 2002--2012

Ninoslav D. Stojadinovic

OCTOBER 2010

Recognition of esteemed leaders in electron devices—EDS Celebrated Members

MID 2000s

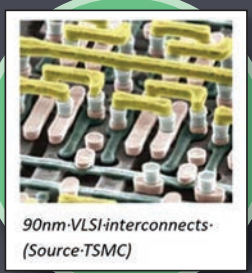
New content highlighting student chapter activity, and distinguished lectures

EDITOR-IN-CHIEF 2017-PRESENT

Carmen M. Lilley

APRIL 2018

HTML electronic newsletter developed



JULY 2018

Full color images in all technical briefs

Thanks to Our Dedicated Volunteer Editors

Newsletter Editor-in-Chiefs	Years of Service
Krishna Shenai	1994–2002
Ninoslav D. Stojadinovic	2002–2012
M. K. Radhakrishnan	2012–2017
Carmen M. Lilley	2017–

Regional Editors (Years of Service)			Regional Editors (Years of Service)	
Elias D. Towe	1994–1998		Jamal Deen	2004–2010
Paul K.L. Yu	1994–1999		Hei Wong	2002–2008
Terry H. Oxley	1994–1999		Zhirun Hu	2005–2011
Adrian Veron	1994–1998		Kazuo Tsutsui	2005–2011
Paul Y.S. Cheung	1994–1995		Jacobus W. Swart	2005–2008
Hiroshi Iwai	1994–1999		Samar Saha	2008–2010
Cuong T. Nguyen	1995–1996		Tomislav Suligoj	2008–2015
S.C. Sun	1995–1999		Zygmunt Ciota	2008–2015
Mikael L. Ostling	1995–2001		Francisco Garcia Sanchez	2009–2014
M. Ayman Shibib	1995–2001		Mansun Chan	2009–2015
Robert G. Adde	1995–1998		Adam M. Conway	2009–2015
Savvas G. Chamberlain	1995–1998		Jan Vobecky	2010–2017
Chennupati Jagadish	1996–1998		M K Radhakrishnan	2010–2016
Mark Weichold	1998–2000		Peyman Servati	2011–2014
Wee Kiong Choi	1998–2004		Fernando Guarin	2011–2014
Arokia Nathan	1998–2004		Jonathan Terry	2013–
Ninoslav D. Stojadinovic	1998–2001		Kuniyuki Kakushima	2012–2018
Christian Zardini	1998–2004		Mukta Farooq	2015–2017
Gady Golan	1999–2005		Susthitha Menon	2015–
Stephen A. Parke	2000–2002		Manoj Saxena	2015–
Hisayo Sasaki Momose	2000–2005		Joao Antonio Martino	2015–2017
Charles B. Yarling	2000–2002		Karim S. Karim	2015–2017
Adelmo Ortiz-Conde	2000–2005		Mariusz Orlikowski	2015–2017
Tahui Wang	2000–2002		Daniel Tomaszewski	2015–
Murty S. Polavarapu	2002–2004		Kyle H. Montgomery	2016–2019
Sunit Tyagi	2002–2007		Ming Liu	2016–
Alexander V. Gridchin	2002–2007		Michael Adachi	2017–
Andrzej Napieralski	2002–2007		Mike Schwartz	2018–
Zhou Xing	2004–2009		Marcin Janicki	2018–
Cora Salm	2004–2009		Edmundo Guiterrez	2018–
Ibrahim Abdel-Motaleb	2004–2010		Rinus Lee	2018–

Message from Editor-in-Chief

Dear EDS Members and Readers,

Carmen M. Lilley
EDS Newsletter
Editor-in-Chief

I want to welcome you to enjoy our 100th issue, celebrating 25 years of renewed publication of the EDS Newsletter. To provide a short historical perspective of the newsletter, in 1966, EDS began publishing a member's newsletter. As found in the EDS 50th Anniversary Booklet, "That year, the long-envisioned goal of publishing a quarterly newsletter was finally realized; the first edition of the Newsletter of the Electron Devices Group appeared in June. Edited by Jan M. Engel of IBM Research in San Jose, California, it provided a convenient forum for recent news of the organization and other matters that could not be covered well in the Transactions—such as highlights of AdCom meetings, reports from the device-research conferences and other professional gatherings, as well as notices of future meetings of interest to the membership." In 1976, the Electron Devices Group became the Electron Devices Society and in 1982, the newsletter became a member's service. The newsletter was published uninterrupted until 1984, when the newsletter was replaced with the Circuits and Devices magazine. However, by 1993 the EDS newsletter was reestablished, and publishing began again in 1994 as a renewed publication. In this issue, we celebrate renewing the newsletter as a member product with the goal to communicate technical information, outreach and efforts by EDS members around the world. I want to thank regional editor Manoj Saxena for suggesting the special content to celebrate the 100th issue and Joyce Lombardini for the extra help needed in assembling this issue.

Sincerely,
Carmen M. Lilley

Message from EDS President

Dear EDS Colleagues:

Fernando Guarin
EDS President
(2018–2019)

I am pleased to take this opportunity to share my EDS President's message. This is the 100th issue of our EDS Newsletter, a very special milestone for this publication. Our newsletter establishes a very close connection between EDS and its members. It has evolved over the years to achieve the unique balance we now enjoy between technical content, and news and activities shared across our 208 chapters and over 9,000 members around the world. This significant landmark has been achieved thanks to the dedication and arduous work by the many talented volunteers that have contributed with distinction over the span of many years. As we complete the first half of 2019, I would like to share with you the latest accomplishments and challenges; our financial position is sound, we finished 2018 with a surplus of $172K, of which $86K was invested back in EDS. From November 2018 to May 2019 our membership dropped by 2.7% but our student membership grew by 1.6%, but we are considering membership agreements with other societies that will provide sustainable growth. We have started the implementation stage of our future strategy, with the clearly defined objective "To collaborate, network, and be the center of excellence in electron device technology." There is a standing committee under Past President Samar Saha's leadership to follow up and track on the progress in the monitoring of our implementation on this important endeavor.

In the publications arena, under the leadership of our new publications chair Tsu-Jae King Liu, the submission to publication time of EDS journals continue to maintain a best in class record pace among IEEE publications. EDL leads the way at 4.2 weeks and JEDS continues to solidify our leadership position in Open Access. JEDS had budgeted $102K in revenue for 2018 and it achieved $221K. Our conference portfolio continues to grow stronger as we continue to execute on new opportunities. The Singapore team ran an outstanding EDTM2019 conference, continuing with 100% EDS ownership and solidifying its position as the EDS flagship conference in Asia; in Region 9, we launched the first edition of the LAEDC in February 2019, in Colombia. The second IEEE IFETC2019 will be held in August 2019 with 100% EDS financing. We continue to maintain very close collaboration with key conferences; PVSC, IEDM, EDTM, IRPS, ISPSD, IVEC, VLSI, IFETC etc., and continue to sponsor special issues based on best conference papers and highly relevant topics for TED and JEDS. Our educational activities remain strong, with four webinars in the first half of 2019 and many DL's and MQ's held around the globe, in addition to many outreach activities in EDS-ETC and other volunteer-led school visits.

The mid-year BoG meeting will have been held in Tarragona, Spain on May 26th by the time you read this article. I invite you to check out the results by logging into our newly designed web site: https://eds.ieee.org/

Our new social media platforms (Facebook, LinkedIn, Twitter and

IEEE Collabratec), continues to grow successfully and has been actively used at our recent EDTM and LAEDC conferences. I invite you to join us and participate:

Facebook https://www.facebook.com/IEEE-Electron-Devices-Society-1581398582006248

LinkedIn https://www.linkedin.com/company/edsglobal

Twitter https://twitter.com/IEEEEDS

As in previous occasions, I would like to finish by extending my sincere gratitude for the efforts of the many dedicated volunteers that have positioned EDS on solid ground in the technical, outreach and financial arenas. As a volunteer-led, volunteer-driven organization, we rely on the dedication of individuals like you who share their time, talent, and energy to help make EDS the premier global society devoted to advancing the field of electron devices for the benefit of humanity. I invite you to become an engaged member, and play a vital role as we shape the future of our society.

Fernando Guarin
EDS President

Message from EDS President-Elect

Greetings to the EDS community.

Meyya Meyyappan
EDS President-Elect

Congratulations to EDS on celebrating the 100th issue of this Newsletter. Remarkable achievement indeed. It is a valuable resource providing highlights of EDS governance, upcoming events, accomplishments of our members and many other news of interest to our broad membership. My favorite is the section devoted to the chapter activities, which seems to be the biggest section in every issue. It should be. I like the pictures where everyone is posing with smiling faces, holding the EDS banner. I wish us all another 100 editions of this newsletter and more. Going forward, please contact the EIC with your suggestions if you want to see any new features.

I am writing this column right after returning from the EDS mid-year Board of Governors meeting in Tarragona, Spain. Among many things we discussed, revitalizing some of our less active chapters is an item I would like to draw your attention to. I urge all of you to actively participate in the activities of your local chapter. It would be ideal if all chapters organize monthly events, and this can take several forms: seminars, distinguished lectures, occasional half or full day event featuring multiple speakers, social gatherings, job fairs, etc. Many chapters are active but we need all our chapters to be vibrant in all ten regions. Please contact our VP for Regional Activities MK. Radhakrishnan (radhakrishnan@ieee.org) if you need help or suggestions.

Summer is here. Schools are out. For all those academics among us, it is time to catch up on writing the pending journal papers and preparing the next grant proposals. Take a breather and enjoy the break. Happy summer everyone.

Meyya Meyyappan
EDS President-Elect

Reflections From Former EDS Newsletter EiCs

To celebrate the 100th issue of the renewed EDS Newsletter, the three previous Editors-in-Chief (EiC) were asked to share their reflections on their tenure and impressions of the newsletter. Below are their responses to the interview questions.

Interview with Dr. Krishna Shenai, Founding Editor-in-Chief (EiC) of the New EDS Newsletter

What was your vision for the EDS newsletter under your leadership?

In 1994, the EDS AdCom had recognized the fact that a Society Newsletter was instrumental in reaching out to chapters and become more global. It was obvious that the chapters were disconnected from each other. The problems were more severe internationally than in the US. The new EDS Newsletter was established in an attempt to get back in touch with members and with other chapters. This increased interaction was important to grow internationally by increasing the presence globally by offering new members more for their membership. With this vision in mind, the EDS

AdCom requested me to serve as the founding Editor-in-Chief (EiC) of the new EDS Newsletter and I graciously accepted the invitation.

What are some notable moments or milestones that you recall during your tenure as EiC for the EDS Newsletter?

The new EDS Newsletter underwent a series of design improvements and content enhancements since its launching in 1994. Bill Van Der Vort, then Director of the EDS Executive Office, was a source of constant inspiration and support throughout my tenure as EiC. Some of these improvements included the introduction of Regional Editors and colored contents, announcement of Society awards and meetings calendar, periodic messages from society officers and conference chairs, and sustained reporting by chapter chairs globally on key events held in the respective regions. Clearly, the Newsletter served its purpose and assisted in rapidly expanding the EDS membership globally, especially in emerging economies of the world including China, India, Latin American and Eastern European countries.

Are there any comments or stories you want to add about the evolution of the EDS Newsletter over the last 25 years?

In the last 25 years, the EDS Newsletter has played a pivotal role in communicating major technology advances and history of technology evolution to the membership. It has also been instrumental in linking intersociety activities that has broadened the impact of electron devices in general while offering significant new opportunities to the membership. For instance, I can remember the important role it played in 1996 in the establishment and promotion of IEEE Intelligent Transportation Systems Council (ITSC) and its activities.

Krishna Shenai served as the founding Editor-in-Chief (EiC) of the new EDS Newsletter from 1994 to 2002. He earned his B. Tech. (electronics) degree from IIT-Madras in 1979, MS (EE) degree from the University of Maryland—College Park, Maryland (USA) in 1981, and PhD (EE) degree from Stanford University, Stanford, California (USA) in 1986. For nearly 40 years, Dr. Shenai and his students have made seminal contributions to silicon and wide bandgap (WBG) power electronics technologies that have shaped the world-wide industry. He is a Fellow of IEEE, a Fellow of American Association for the Advancement of Science (AAAS), a Fellow of the American Physical Society (APS), and a member of the Academy of Engineers of Serbia (AES). Dr. Shenai currently serves as a Distinguished Lecturer of IEEE Power Electronics Society (PELS) and as an Editor of IEEE J. Electron Devices Society (EDS). He has authored over 450 peer-reviewed archived papers in top international conference digests and journals, 10 books, 9 book chapters, and holds 12 issued US patents.

Interview with Ninoslav Stojadinovic Editor-in-Chief (EiC) of the New EDS Newsletter (2002–2012)

What was your vision for the EDS newsletter under your leadership?

My vision was to extend EDS Newsletter's visibility, thus promoting its main activities to the whole world, including some countries of Former Soviet Union, Africa, Latin & South America and Asia.

What are some notable moments or milestones that you recall during your tenure as EiC for the EDS newsletter?

We practically encouraged for the first time publication of articles on activities and accomplishments of Students Branches and Chapters, as well as awarding of both regular and students chapters. Also, the DL program received significant emphasis during my terms as EiC. Finally, the most important EDS events, such as conferences and workshops were announced by specially prepared articles.

Were there any technical highlights or review articles that standout during the course of your tenure? Or, articles celebrating notable EDS members, groups or events?

There were some initiatives to begin publishing technical highlights and review articles, but, honestly speaking, I was not in favor of this idea. On the other hand, I was in favor of articles celebrating notable EDS members, groups and events.

Are there any comments or stories you want to add about the evolution of the EDS newsletter over the last 25 years?

I do not think our job is finished yet, and EDS Newsletter should be improved further. Actually, this is the fun part of this job, often it is the journey that is more enjoyable than the destination itself.

Interview with M.K. Radhakrishnan Editor-in-Chief (EiC) of the New EDS Newsletter (2013 July to 2017 April)

What was your vision for the EDS newsletter under your leadership?

When I accepted the invitation to take up the EDS newsletter leadership, I had more than a decade of association with the Newsletter as a contributor and as a preceding Regional Editor for few years. The Newsletter at that time was a vehicle to communicate Society's messages, news items like meetings, conferences and chapter activities to the members. Knowing the importance of this media in the EDS fraternity, my vision was to transform the Newsletter to a Technical Magazine useful for all

professionals, while allocating sufficient space for Society news. As such, during my first meeting with Newsletter Oversight Committee and BoG as EiC in Dec. 2013, I projected few aspirations like (1) initiate Technical Briefs on the advancements in the fields of EDS which are palatable to any member/reader, (2) provide a platform for Young Professionals, and (3) initiate online publication of Newsletter. Both the forums overwhelmingly supported the suggestions, which helped me to proceed with my vision of a publication with at least 50 percent technical articles along with Society news items.

What are some notable moments or milestones that you recall during your tenure as EiC for the EDS newsletter?
Major milestones during my tenure as EiC include:

- Initiation of Invited Technical Articles (Tech Briefs) by experts in every issue. First of its kind through invitation. The key point I insisted in my invitations was the narration of scientific content in a language palpable to any reader. Each of the issues had tech briefs on different key topics by leading experts in those areas.
- Technical highlights of key papers from major EDS conferences like IEDM. The idea was mooted from the advance publication of conference highlights by nonIEEE magazines, but not by EDS. The effort to get such contents to EDS own magazine was successful after a strong networking.
- A special column for Young Professionals to express their ideas and reflections. As EiC, I could personally interview the YPs for each issue and that resulted in their manifestations of vigour and thoughts about the future.
- Publication of each issue of the Newsletter on the first day of the publication month itself (or within the first week). This was the resultant of the perpetrated team work of the Editorial team—all Regional Editors and the well-timed effort and dedication by Joyce Lombardini.
- Initiation of online version of Newsletter, accessible to everyone, not only EDS members. This provided more exposure not only to the Newsletter, but to the Society as a whole.

Were there any technical highlights or review articles that standout during the course of your tenure? Or, articles celebrating notable EDS members, groups or events?
The encouraging feedback from readers is the best measure to highlight the significance of articles. I am proud to mention that when we first published the IEDM highlights, as well as the article on 2014 Nobel Prize winners and the blue LEDs, the response from readers was much cheering. Apart from these, many invited articles stand out, the diversity of topics was the key. The reflections from different EDS Young Professionals through EiC's interviews with them were another highlight which probably was the first of its kind in a Society Newsletter.

Are there any comments or stories you want to add about the evolution of the EDS newsletter over the last 25 years?
As an IEEE/EDS member and an active volunteer for more than 35 years, I was much familiar with the IEEE Society newsletters—not only that of EDS, but couple of other IEEE Societies also. The way EDS newsletter evolved from the keen efforts of Krishna Shenai, first EiC, to convey the Society news items and messages is in my memory. Further, my predecessor Nino Stojadinovic, a stalwart in editing and publishing technical journals shaped the EDS Newsletter in its physical format. I was fortunate to work with Nino in assisting him as a Regional Editor as well. My aim as EiC was to keep the format as such and develop the newsletter to a Technical magazine. All the initial plans like Tech Briefs, YP interviews, etc were successful. I would like to specially mention that my invitation to all the experts to write Tech Briefs in common man's language was well accepted by everyone I invited. More interestingly no one ever delayed any article, even though all of them were extremely busy. Kudos to all. Similar is the support received from YPs, Regional Editors, Chapter Chairs and many whom I could personally contact as Newsletter EiC. I strongly feel that such a closeknit communication and cooperation of all clubbed with timely release of each issue of the Newsletter is the key for the success, no matter whether it is hard copy format or online publication or available in social media. Even though I was ousted from the EiC, I am sure that one day this publication could accomplish my vision, a Technical Magazine useful for all who love the science and dedicate their efforts towards devices.

Edited by Manoj Saxena

Marvellous Concepts & Techniques Before and During Moore's Law Era

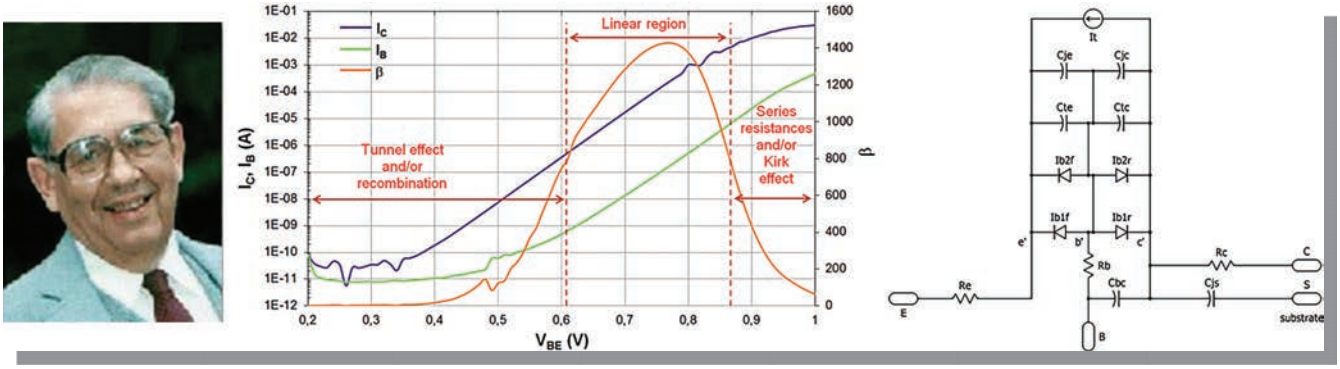
By Joachim N. Burghartz

Who doesn't know the Gummel Plot, the measured characteristics of the bipolar transistor that tells almost everything about the dc behavior of the device that dominated the semiconductor technology before MOS took over in the 1970s. That semi log plot of the base and collector current as a function of the base-emitter voltage exhibits the impact of tunnel and recombination effects on the base current and of series resistance and high-injection effects (e. g. Kirk effect).

Herrmann Gummel, a Bell Labs semiconductor pioneer, is in his mid-90s today and blessed to still be able to live at home thanks to the care of his family. His daughter Margi Gummel-Taylor sent me a copy of a paper by Gummel and Poon presented at the 1970 IEEE Solid State Circuits Conference (ISSCC) [1] held at the University of Pennsylvania in a session chaired by Donald O. Pederson. According to her, that presentation "was an early preview of the 'Gummel-Poon Model', including a figure that shows a semi-logarithmic plot of the current gain (presumably a Gummel Plot) which was a natural byproduct of the thought processes leading to the 'Gummel-Poon Model'." The Gummel Plot became the key measurement in bipolar technology, telling engineers right away about the overall quality of the device. Therefore, the Gummel Plot is a true marvel of microelectronic engineering in the category electrical characterization techniques. Hermann Gummel received—to name a few—the IEEE David Sarnoff (1986) and Phil Kaufmann (1994) Awards, and he became a member of the US National Academy of Engineering in 1985.

There are also marvellous concepts in device modeling worth mentioning, such as the Gummel-Poon model addressed above, through which both dc and ac characteristics of a bipolar transistor can be represented. On the one hand, Gummel-Poon can be considered an expansion of the pioneer Ebers-Moll model, on the other hand, it is the key step towards the development of SPICE [4] and all circuit simulation tools thereafter. Larry Nagel, co-inventor and developer of SPICE (see below) has a distinct opinion, why and how a semiconductor model could be considered a marvel: "I think a model is a marvel only if it reveals additional knowledge about the operation of the semiconductor device it is modeling. Ideally, the model is predictive, that is, it predicts new behavior that was not understood before, in addition to accurately portraying the operation of the device that was understood before." With respect to the Gummel-Poon model he told me: "The Integral Charge Model (or Gummel-Poon model or GP model) that Hermann Gummel developed is a classic example of a predictive model. The GP model was developed in the late 60s, when the only available bipolar model was an Ebers-Moll model [5] with additional 'second-order' effects bolted on in an empirical and physically incorrect method. In these 'extended Ebers-Moll' models, collector current was computed with the classical formula and base current was calculated using a table for the beta of the transistor. Hermann was able to show that in high level injection collector current rolled off due to high level injection, rather than having base current increase as predicted by a beta model. This is a perfect example of using a parameter of dubious physical meaning (beta) to attempt to explain charges and currents in a device. Instead, by using fairly simple physics, Gummel was able to explain high level injection in a bipolar transistor as well as base-width modulation and base push-out. Quite an accomplishment!"

Another such dubious parameter is the threshold voltage of the MOSFET, according to Colin McAndrew from NXP Semiconductors. "MOSFETs were considered to be in either 'off' or 'on' states, hence the concept of a 'threshold voltage' as the boundary between these two operating states became accepted. Modeling followed that path for many years and reached a pinnacle in the BSIM4 model [6], which has been used for the design of more integrated circuits than any other model. As supply voltages decreased and requirements for RF and precision analog CMOS circuit design became more exacting, the empirical underpinnings of the threshold voltage viewpoint and its lack of a physical foundation became apparent. Analysis based on the surface-potential is now recognized as the most physical approach, and was pioneered by H. C. Pao and C.-T. Sah in the mid-1960s [7]. While still recognized as the "gold standard" of comparison for all other MOS transistor models, the Pao-Sah model is too complex to use for circuit design. Reduction



Herrmann Gummel (left; courtesy of ESD-Alliance), Gummel Plot of a SiGe bipolar transistor (middle; [2]) and Gummel-Poon compact model (right; [3])

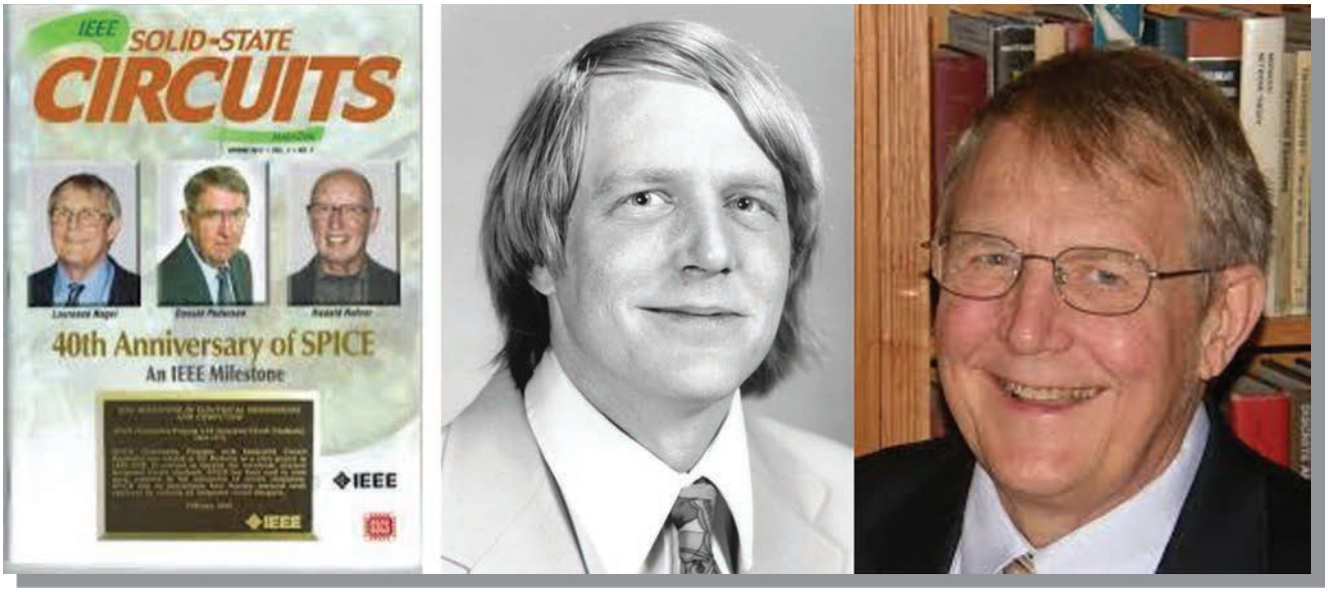
to a practical form took about 4 decades, and a key step in this was the symmetric linearization approach developed by Gennady Gildenblat [8] jointly with Philips, when he was at Pennsylvania State University. This naturally embodied the physics of MOS transistors (use a transverse field to induce a conducting charge sheet, apply a longitudinal voltage to drive a current through that charge sheet), and introduced the 'symmetric linearization' procedure, which enabled the PSP (Pennsylvania State University and Philips) model to meet the stringent requirements, especially of symmetry, of precision analog and RF CMOS circuit design."

Larry Nagel considers the PSP MOSFET model [8] developed by Gennady Gildenblatt a marvel. "The PSP model discarded the physically dubious concept of a threshold voltage and instead was able to derive a much more realistic model for a MOSFET. By using physics and some clever mathematical assumptions, Gennady was able to come up with one model that explained cutoff, subthreshold, and strong inversion, all with one equation. Again, quite an accomplishment!"

Now, Larry Nagel himself is associated with a true marvel that had a totally unexpected impact. While a PhD student at Berkeley, he developed the Simulation Program with Integrated Circuit Emphasis (SPICE) as an open-source analog circuit simulator; SPICE1 is described in his PhD thesis from 1975. His advisor was Prof. Donald O. Pederson who chaired Gummel's paper presentation about the Gummel-Poon compact model at the ISSCC in 1970. He announced SPICE in Waterloo, Canada, at the 16th Midwest Symposium on Circuit Theory on April 12, 1973 [9]. Larry Nagel remembers: "I don't think anybody had a clue of the impact of that paper or the computer program it described." In an invited talk at the 1996 BCTM [10] Larry said: "But I can speculate. The biggest reason is that SPICE was developed at a public university and was public domain from the beginning. Because it was developed primarily as a teaching tool to provide students insight into integrated circuit performance, SPICE was rapidly embraced by many engineering colleagues throughout the world." SPICE was largely a derivative of the CANCER program which was announced two years earlier at the 1971 ISSCC meeting [11] by Berkeley professor Ronald A. Rohrer, the supervisor of Nagel's master thesis. "It is amazing what graduate students spend time on. The name CANCER was not the most popular in industry, mainly because of the medical implications, and my first job was to find a new name. I figured this whole project wouldn't go anywhere without a catchy name, and eventually SPICE was born."

SPICE was released as a public domain software in 1971 (SPICE1) and 1975 (SPICE2) by Larry Nagel; the version SPICE2.G.6 is still available from Berkeley today. SPICE came out of a true team effort: "Rohrer did the early research, Nagel took care of its development, and Pederson had the overall lead and handled the marketing; sales was done by the Berkeley students who carried SPICE to their workplaces in industry. It took SPICE 10 years to obtain commercial viability." Pederson is considered the father of SPICE. He received the 1998 IEEE Medal of Honor for his contributions to SPICE and IC simulation. The IEEE Solid State Circuits Society (SSCS) issues the IEEE Donald O. Pederson award since 1987. Our article comes right on time to congratulate Larry Nagel for receiving the 2019 IEEE Donald O. Pederson Award in Solid-State Circuits. Even though SPICE falls into the domain of SSCS, it directly relates to compact modeling and, thus, to EDS as well. The emergence of SPICE is clearly a marvel of microelectronic engineering. Without the advanced circuit simulation programs that have succeeded SPICE, the complex integrated circuits from the 1980's until today would simply not have been feasible.

Another key enabler of today's state of microelectronics is MOS device scaling which, like SPICE, had been underrated in its infancy. Scaling was introduced by Robert Dennard, Fritz Gaensslen, Larry Kuhn and Hwa Yu when they presented



Cover of the IEEE Solid State Circuits Magazine (left), Larry Nagel in the early 1970's (middle; [4]) and more recently (right; courtesy of Omega-Enterprises)

their theory at the 1972 IEDM [12], not yet knowing about the impact their research would have in the years to come. The initiative was driven by the DRAM program at IBM. Bob Dennard joined IBM Research in the mid-1960s to work on MOS field effect transistors, which were demonstrated just a few years ago. At IBM they were told to look for a replacement of the magnetic-core memory technology using MOS transistors. That research eventually led to the DRAM concept, invented and patented by Bob Dennard. (This would certainly be worth mentioning in this present article on Concepts & Techniques. However, we will devote substantial time to DRAM in our next article of the series in the October 2019 issue of the EDS Newsletter.) Dale Critchlow, to whom Bob Dennard reported, told about the path to MOS scaling in the 2007 newsletter of the IEEE Solid-State Circuits Society [13]. "There were a number of options including shift registers and CCDs, but Dennard as the inventor was keen on pursuing the one-transistor DRAM cell. Bob did some preliminary analyses, and concluded that we would need feature sizes of about 1μm, a 5X shrink from those in manufacturing, to achieve our goals. We realized that we would have to scale the vertical dimensions (oxide thickness and junction depth) and adjust the doping level of the substrate to maintain usable device characteristics. Further, we would have to scale the operating voltages as well to preserve reliability and limit power dissipation. In fact, we had done this twice before in the 1960s, first from 24V to 12V and then to 6V using rudimentary scaling to guide our designs." He further said: "Within a few days Bob, Fritz and Larry had formalized the constant-field scaling theory and its limitations. The implications of scaling were remarkable. If all dimensions, voltages (including threshold voltage) and doping levels were scaled by a constant factor κ: a) the circuit delay was decreased by κ, b) the power/circuit was decreased by κ^2, and c) the power delay product was reduced by κ^3. Further, the power/unit area of silicon remained constant! These were exactly the results we needed to develop a competitive low-cost memory." The paper that is generally considered the 'saling paper' appeared in the IEEE Journal of Solid-State Circuits in October 1974 [14]. Also worth mentioning is a paper on the generalized scaling theory by Giorgio Baccarani, Matt Wordeman and Bob Dennard in April 1984 in the IEEE Transactions on Electron Devices [15]. When I asked Bob Dennard whether the scaling law was tightly related to high density DRAM integration rather than to FET miniaturization in logic transistor, he replied" "Yes, and No. The principles of scaling apply to all kinds of MOS transistor applications, from logic devices to power devices. DRAM was our target when we set the goal to reduce the DRAM cell size by a factor of 25. We then devised the MOS scaling principles to show how to make much smaller devices with properly reduced drain induced barrier lowering (DIBL). To demonstrate scaling we started with 5-micron logic devices because that is what our base process was setup to do. It may have been underrated by some who doubted insulator thickness could be scaled past 1000 Å, but our evidence for a micron length device with 200 Å was very strong. And one did not have to scale by 5x to get started. Intel adopted scaling immediately and very soon announced, I think, 5V SRAM referencing our scaling laws. To me DRAM means the 1-T cell,

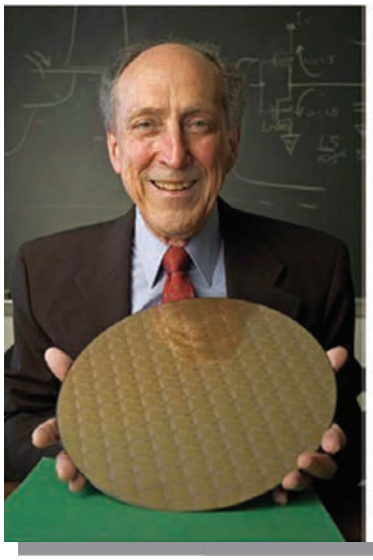


Table 1
Scaling Results for Circuit Performance

Device or Circuit Parameter	Scaling Factor
Device dimension t_{ox}, L, W	$1/\kappa$
Doping concentration N_a	κ
Voltage V	$1/\kappa$
Current I	$1/\kappa$
Capacitance $\epsilon A/t$	$1/\kappa$
Delay time/circuit VC/I	$1/\kappa$
Power dissipation/circuit VI	$1/\kappa^2$
Power density VI/A	1

Bob Dennard (left; Courtesy of IBM) and scaling rules from the 1974 scaling paper in IEEE JSSCC [14] (right)

and its development came after, not before, our scaling talk and paper." Bob Dennard further told me: "Our partner H.N. Yu designed and built a properly scaled 1-micron logic device. My coworker Fritz Gaensslen found a nice way to produce normalized measured characteristics for the two devices, showing that our scaling principles worked. A great Eureka moment! About four years later 1T-DRAM production started and it became the large volume product that drove scaling for many generations." Dale Critchlow concludes: "The Impact of MOSFET Scaling has been monumental. Scaled CMOS has become the dominant technology for digital and many analog applications and will continue to be a fundamental driving force of the industry for years to come."

Bob Dennard received numerous and outstanding honors for his seminal achievements to DRAM and MOS scaling. In 1988 he received the National Medal of Engineering from President Ronald Reagan for the invention of DRAM. In 2000, he received the IEEE Edison Medal, in 2007 the Benjamin Franklin Medal, in 2009 the IEEE Medal of Honor, and in 2013 the Kyoto Award, just to name a few.

References

[1] H.K. Gummel and H.C. Poon, "A Compact Bipolar Transistor Model", Dig. Techn. P. of IEEE International Solid-State Circuits Conference (ISSCC), pp. 78–79, (1970)

[2] https://en.wikipedia.org/wiki/Gummel_plot

[3] https://en.wikipedia.org/wiki/Gummel%E2%80%93Poon_model

[4] http://www.omega-enterprises.net/The%20Origins%20of%20SPICE.html

[5] J.J. Ebers and J.L. Moll, Proc. IRE 42, (1954)

[6] https://bsim.berkeley.edu/models/bsim4/

[7] Pao HC, Sah CT., "Effects of diffusion current on characteristics of metal-oxide (insulator)-semiconductor transistors", Solid-State Electronics, 927–937, (1966)

[8] Gildenblat G, Li X, Wu W, WangH, Jha A, van Langevelde R,Smit G, Scholten A, KlaassenD., "PSP: an advanced surface-potential-based MOSFET model for circuit simulation.", IEEE Transactions on Electron Devices, pp.1979–1993, (2006)

[9] Donald O. Peterson, "Simulation program with integrated circuit emphasis", Sixteenth Midwest Symposium on Circuit Theory, (1973)

10] Larry Nagel, "The Life of SPICE", Luncheon Speed at the 1996 BCTM, Minneapolis, USA; see also: http://web.engr.oregonstate.edu/~karti/ece521/life-of-spice.pdf

[11] R. Rohrer, L.W. Nagel, R. Meyer, L. Weber, "CANCER: Computer analysis of nonlinear circuits excluding radiation", Dig. Techn. P. of IEEE International Solid-State Circuits Conference (ISSCC), pp. 124–125, (1971)

[12] R.H. Dennard, F.H. Gaensslen, L. Kuhn, H.N. Yu, "Design of Micron MOS Switching Devices", Techn. Dig. International Electron Devices Meeting (IEDM), pp. 168–170, (1972)

[13] D.L. Critchlow, "Recollections on MOSFET Scaling", Newsletter of the IEEE Solid-State Circuits Society, pp. 19–22, (2007)

[14] R.H. Dennard, F.H. Gaensslen, H.N. Yu, V.L. Rideout, E. Bassous, A.R. LeBlanc "Design of ion-implanted MOSFET's with very small physical dimensions", *IEEE Journal of Solid-State Circuits*, vol. 9, pp. 256–268, (1974)

[15] G. Baccarani, M.R. Wordeman, R.H. Dennard "Generalized scaling theory and its application to a sub-micrometer MOSFET design", *IEEE Transactions on Electron Devices*, vol. 31, pp. 452–462, (1984)

Upcoming Technical Meetings

2019 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium

Late Breaking News Submission Deadline: August 9, 2019

COURTESY OF LOEWS VANDERBILT HOTEL

It is with great pleasure that we welcome you to be a part of the 2019 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS). After 39 years of the Compound Semiconductor IC Symposium (CSICS), and 32 years of the Bipolar/BiCMOS Circuit and Technology Meeting (BCTM), the second meeting of this combined symposium will be held on Sunday November 3 to Wednesday November 6 at the Loews Vanderbilt Hotel in Nashville, Tennessee.

BCICTS continues the long history, from BCTM and CSICS, of international gatherings where distinguished experts present their latest results in bipolar, SiGe BiCMOS, and compound semiconductor circuits, devices, and technology. There are no other events in the world where you can see leading edge bipolar/BiCMOS devices and technology, 5G ICs, GaN HPAs, InP THz PAs, optical CMOS/SiGe transceivers, GaN HEMT power devices, and advances in compact modeling, all presented together.

This second BCICTS includes presentations from worldwide submissions on all aspects of the technology. Topics span process technology, device advances, TCAD modeling, compact modeling to IC design and testing, high-volume manufacturing, and system applications. BCICTS will also feature the very latest results in RF/microwave, millimeter-wave, THz, analog mixed signal, and optoelectronic integrated circuits.

On Sunday, November 3rd, BCICTS offers a topical short course on Millimeter-wave radar: systems, circuits, and process technologies. Taught by leading experts, the short course is intended for both technologists and IC designers who seek a comprehensive understanding of the latest industry trends and techniques.

On Monday, November 4th (prior to the opening of the symposium) we offer a more basic primer course. The primer course is intended to be a tutorial which introduces Gallium Nitride device technology and circuit design.

As a complement to the technical program, the symposium includes numerous social events that allow participants to interact and network in a friendly, relaxed setting. These events include the Monday Evening Exhibition Opening Reception, and the Technology Exhibition Luncheon on Tuesday.

For registration and up-to-date information please visit the BCICTS website at www.bcicts.org. Further questions may be addressed to the Symposium Co-Chairs: Peter Zampardi pete.zampardi@qorvo.com and Sorin Voinigescu sorinv@ece.utoronto.ca .

We hope you can attend.
2019 IEEE BCICTS Organizing Committee

Craig Steinbeiser
2019 BCICTS Publicity Chair

Mid-Year EDS Governance Meeting, Tarragona, Spain

By Benjamin Iniguez and Jacobus Swart

Jacobus Swart
EDS Secretary

The Mid-Year 2019 EDS Governance Meeting was held in Tarragona, Spain on May 25–26, 2019. It was organized by EDS in collaboration with the University Rovira i Virgili (Tarragona).

Meetings of Technical and Standing (Membership, Finance, Education, Publications, Fellow Evaluations, Regions & Chapters) Committees took place on May 25th, as well as the ExCOM Meeting. Besides, in the afternoon there was a meeting of the Region 8 Chapters.

The Board of Governors Meeting was held on May 26th. Fernando Guarin (EDS President), Ravi Todi (Vice President of Technical Committees and Meetings), Jim Skowrenski (EDS Operations Director), Jacobus Swart (EDS Secretary), M. K. Radhakrishnan (Vice President of Regions & Chapters), Ru Huang (Vice President of Membership and Services), Tsu-Jae King Liu (Vice President of Publications and Products), Samar Saha (Chair of the Awards Committee), Camilo Vélez-Cuervo (Chair of EDS Young Professionals Committee), and Cor Claeys (Chair of the Fellows Evaluation Committee) presented proposals and results of previous discussions. Several motions were approved.

Some highlights from the initial general overview presented by EDS President Fernando Guarin and followed by specific presentations by others are:

- EDS keeps a healthy finance balance, with a surplus of $172k in 2018. Fifty percent of this surplus will be used for new initiatives in 2019. This will add to the 3% of the reserves (corresponding to $215k) that are allowed to be spent on new projects.
- Membership was reduced a little by 2.7%, while the student membership was increased by 11%. Noticeable was the increase of memberships in Region 9 by 76%. New ideas to increase the number of members and its benefits were presented by Ru Huang.
- Submission-to-publication time of EDS journals in gradually shortening and EDL is being the fastest in all IEEE journals (~4.2 weeks). Paper submissions to EDL are steadily growing and T-ED and J-EDS are becoming more selective. While the three solely EDS journals are presenting healthy net revenues, the six joint publications present modest numbers and special care should be given to T-SM, that is needing some revitalization according to Tsu-Jae King Liu.
- New conferences recently started are success cases, especially EDTM. The 1st LAEDC (Latin America Electron Device Conference) was held in Colombia last February; 2nd IEEE IFETC 2019 (IEEE International Flexible Electronics Technology Conference) is scheduled for August in Vancouver, Canada, and the 3rd EDTM 2019 was held in Singapore in March.
- Educational activities are enlarging, with 4 webinars scheduled in the first half of 2019 and an EDS Center of Excellence, co-funded by local agencies, is started as a common education and outreach initiative. Summer school initiative was discussed and a call for proposals will be announced soon.
- Total number of chapters came to 208, after closing non active chapters and forming some new ones. Among these chapters, 71 are student chapters. Mentioned by M. K. Radhakrishnan, VP Regions/Chapters, is the motto "Healthy & Self-sustainable Chapters." The total subsidy amount for the chapters in 2019 was $54k.
- The EDS Mission Fund grew to a balance of almost $130k. Plans are being worked out on how the fund may be expended. Mission Fund has been established to support EDS mission-driven humanitarian, educational, and research initiatives. Currently it supports the EDS-ETC program (*Engineers Demonstrating Science: an Engineer Teacher Connection*) and the EDS Student Fellowship program. Presently, an expanded fund definition is being drafted; to cover all future anticipated Humanitarian, Educational and Research activities.
- EDS strategic plan is moving forward under the guidance of EDS Past-President, Samar Saha. An Ad Hoc committee has been appointed to assure correct implementation, while short and long-term goals were collected from the different standing and technical committees.

Attendees of the EDS Board of Governors Meeting in Tarragona, Spain, May 26, 2019

- New social media (Facebook, LinkedIn, Twitter and IEEE Collabratec) grew successfully through a six-month test, showing great numbers of impressions. This action is being conducted by the Young Professionals Committee, that contracted a social media company, called Proambientales. Camilo Vélez-Cuervo pointed out there are 4,868 fans on Facebook, 208 followers on Twitter and 71 on LinkedIn.
- The redesigned EDS website was launched in May.
- EDS future directions aligning with IEEE are being discussed and defined, including engagements with IoT (*Internet of Things*) multi-society technical group (5% partnership) and 5G initiative. EDS also participates actively with Roadmap projects: IEEE Device and Systems Roadmap (IRDS) and Packaging Heterogeneous Integration Roadmap (HIR).
- Also important in the society are the annual awards, recognizing the prominent people for their work and contributions. Presently there are twelve EDS sponsored awards and three new ones are pending at IEEE for final approval. Among these, one was proposed in this meeting, called Lester F. Eastman Award, *for outstanding achievement in high-performance electronic and optoelectronic devices.*

Included in the presentations and discussions, several motions were approved. The main ones were:

- The December 2018 EDS BoG Meeting Minutes
- New members for several committees were appointed.
- EDS members to have the option to request the print copy of the EDS Newsletter, with the electronic version being the default method of distribution. This will not cause any reduction in member benefits.
- Increase the annual EDS membership fee from $18.00 to $20.00.
- Approval to spend $85.8k of the 2018 surplus for new education and outreach activities.
- Approval to spend $215k of the reserves for new initiative for education and outreach activities in 2020. Call for suggestions are open on the floor.
- Distinguished Lecturer and Mini-Colloquia budget will be increased by $33.3k.
- Approval of publication prices/budget.
- Approval of page budget for publications.
- Create a new award: EDS Lester Eastman Award. This proposal was sent to IEEE for final approval.
- Next mid year meeting location will be in Sydney, Australia, IEEE Region 10, in May 2020 (this was voted afterwards by email).

2019 IEEE William R. Cherry Award Winner

Professor Harry Atwater, Howard Hughes Professor of Applied Physics and Materials Science at the California Institute of Technology, received the William Cherry Award in recognition of his many and outstanding contributions to photovoltaic science and technology.

Over more than 35 years, Harry Atwater's research topics have shown his passion for PV from his first paper forming silicon absorbers via zone-melt crystallization (1982) to his most recent on optics for spectral-splitting to achieve ultrahigh efficient modules. His contributions to both the science and technology of photovoltaics, as disseminated through PVSC and EDS, and his creativity are widely recognized and seemingly unbounded, evident in more than 450 publications. Equally remarkable, he co-founded six companies including ETC Solar (commercializing effectively transparent contacts), Luminescent Energy, and Alta Devices.

Harry Atwater's scientific interests have two themes: photovoltaic solar energy conversion and light-matter interactions in materials. He has created new high efficiency solar cell designs and has pioneered principles for light management in solar cells. Atwater is the co-founder of Alta Devices, a solar photovoltaics company in Santa Clara, California, that holds the current world records for one-Sun single-junction solar cell efficiency and module efficiency. Atwater is also an early pioneer in nanophotonics and plasmonics.

He is the founding Editor in Chief for the journal ACS Photonics, and is Associate Editor for the IEEE Journal of Photovoltaics. In 2006, he founded the Gordon Research Conference on Plasmonics, where he served as chair in 2008. He is also the founding Director of the Resnick Sustainability Institute at Caltech, and he currently serves as Director of the DOE Joint Center for Artificial Photosynthesis, and as the Strategic Director for the QESST ERC program.

Professor Atwater received his B. S., M. S. and Ph.D. degrees from the Massachusetts Institute of Technology respectively in 1981, 1983 and 1987. He held the IBM Postdoctoral Fellowship at Harvard University from 1987–1988 and has been a member of the Caltech faculty since 1988.

Pierre Verlinden
2019 Cherry Award Chair

Call for Nominations—EDS Board of Governors

Samar Saha
Chair of EDS Nominations & Elections

The IEEE Electron Devices Society invites nominations for election to its Board of Governors—BoG (formerly AdCom) members-at-large. The next election will be held after the BoG meeting on Sunday, December 8, 2019. This year, seven out of the twenty-two members will be elected for a 3-year term, with a maximum of two terms.

According to the two related motions passed at the mid-year BoG meeting held in Kochi, India, in May 2017 a member can only serve for a maximum of two terms as a BoG member in a lifetime, and the pilot program for one of the BoG Member-at-Large seats to be elected via the entire EDS membership will be discontinued going forward. Therefore, the eligibility will be verified for all nominees who will be voted on by the EDS BoG. All electees begin their term in office on January 1, 2020. The nominees need not be present to run for the election. In 2019, seven positions will be filled.

Any EDS member who has served for a minimum of one year as an EDS Officer, Vice-President, Standing & Technical Committee Chair/Member, Publication Editor and Chapter Chair is eligible to be nominated, unless otherwise precluded from doing so

in the EDS Constitution and Bylaws. The electees are required to attend at least one BoG meeting every year. While the December meeting is organized in conjunction with the *IEEE International Electron Devices Meeting*, the mid-year meeting is frequently held outside the US. Partial travel support is available to attend BoG meetings.

All nominees must be endorsed by one BoG member, i.e., one of the four officers (President, President-Elect, Treasurer or Secretary), the Jr. or Sr. Past President or one of the 22 current BoG Members-at-Large. It is the responsibility of the nominators and the endorsers to make sure that, if elected, the nominee is willing to actively serve in the position as a BoG member-at-large.

Please submit your EDS BoG nomination by October 15, 2019, using the online nomination form at: (https://ieeeforms.wufoo.com/forms/k4vnyad0ys3o4z/).

Also, all endorsement letters should be emailed to Laura Riello, EDS Executive Office (l.riello@ieee.org) by October 15, 2019. If you have any questions, please feel free to contact Laura Riello with a copy to me at samar@ieee.org.

Samar Saha
Chair of EDS Nominations & Elections

EDS Board of Governors (BoG) Members-at-Large Election Process

The Members-at-Large (MAL) of the EDS Board of Governors (BoG) are elected for staggered 3-year terms. The 1993 Constitution and Bylaws changes mandated increasing the number of elected MAL from 18 to 22, and required that there be at least two members from each of the following geographic areas: Regions 1–7 and 9; Region 8; and Region 10. In 2003, EDS made changes to its Constitution and Bylaws to require that at least one elected BoG member is a Young Professional (YP—formerly Gold member). A Young Professional member is defined by IEEE as a member who graduated with his/her first professional degree within the last fifteen years. It is also required that there are at least 1.5 candidates for each opening. On May 20, 2017, the BoG approved to set a life time limit of two terms for a volunteer to serve as a BoG Member-at-Large, which must be considered for nominations. The EDS BoG also approved to discontinue the pilot program for one of the BoG Member-at-Large seats to be elected via the entire EDS membership. Accordingly, all nominees will be voted on by the EDS BoG in its meeting in December, 2019. All electees begin their term in office on January 1, 2020. The nominees need not be present to run for the election. In 2019, seven positions will be filled.

The election procedure begins with the announcement of Call for Nominations in the *EDS Newsletter*. The slate of nominees is developed by the EDS Nominations & Elections Committee. Nominees are asked to submit a two page biographical resume and an optional 50 word personal statement in a standard format.

Any EDS member who has served for a minimum of one year as an EDS Officer, Vice-President, Standing & Technical Committee Chair/Member, Publication Editor & Chapter Chair is eligible to be nominated, unless otherwise precluded from doing so in the EDS Bylaws. All nominees must be endorsed by one BoG member, i.e., one of the four officers (President, President-Elect, Treasurer or Secretary), the Jr. or Sr. Past President or one of the 22 current BoG MAL. Self-nomination is allowed. Endorsers should send a brief email to Laura Riello (l.riello@ieee.org), stating that they would like to endorse the candidate. Please note that there is no limit to the number of candidates that a full voting BoG member can endorse.

The deadline for Nominations will be October 15, 2019. The biographical resumes and endorsement letters will be distributed to the BoG prior to the December BoG meeting. The election will be held after the conclusion of the BoG meeting on December 8, 2019.

Samar Saha
Chair of EDS Nominations & Elections

Call for Nominations Editor-in-Chief IEEE Transactions on Device and Materials Reliability

The *IEEE Transactions on Device and Materials Reliability (TDMR)* provides leading edge/state of the art information that is critically relevant to the creation of reliable microelectronic products. The Transactions is a forum for interdisciplinary studies on reliability and publishes original and significant research contributions on reliability of Electronic and Photonic Devices, Materials, Processes, Interfaces, Integrated Microsystems (including MEMS & Sensors), Process Technology (CMOS, BiCMOS, etc.) and Integrated Circuits (IC, SSI, MSI, LSI, ULSI, etc.) and Packages. The measurement and understanding of the reliability of such entities at each phase, from the concept stage through research and development and into manufacturing scale-up, provides the overall database of the reliability of the devices, materials, processes, package and other necessities for the successful introduction of a product to market. Reliability, in a sense, is everything that can be or has to be done to guarantee that the product successfully performs in the field under customer conditions. Our goal is to capture these advances.

Founded in 2000, TDMR publishes original papers and letters. The editor-in-chief together with the editorial team also solicits review articles, invited papers for special issues on highly topical themes. TDMR is co-sponsored by the IEEE Electron Devices and the IEEE Reliability Societies.

Nominations are invited for the position of Editor-in-Chief (EiC) for TDMR for a 3-year term beginning in **January 2020**. The EiC's ongoing duties include assigning submitted manuscripts to one of the editors who cover the range of reliability issues within TDMR's scope. The EiC makes the final decision regarding the disposition of each manuscript submitted to TDMR based upon the recommendation of the editor. TDMR publishes four issues per year, each approximately 150-200 pages in length.

The EiC is helped administratively by a person from the IEEE publications staff.

Criteria for the Nominees:

- Ability and motivation to spend sufficient time to assign manuscripts and reviewing the acceptance or rejection recommendations made by the editors;
- Demonstrated technical leadership within the field of reliability evaluation and characterization;
- Formal support from the institution for which the nominee works (waived if self-employed or employed at an academic institution);
- Experience serving as an editor of TDMR or another journal whose scope includes the field of reliability of microelectronic devices;
- Commitment to guide TDMR according to this Call for Nominations and to further actively develop the journal;
- Willingness to work collaboratively with internal and external stakeholders to ensure the technical leadership and fiscal health of TDMR.

Requirements for Nominations:

- A brief IEEE-style biography (up to 250 words) of the nominee;
- A complete CV and list-of-publications of the nominee;
- A brief statement from the nominator on nominee's qualification and how the nominee meets the criteria listed above;
- A letter from nominee's employer indicating support for the EiC activity (can be waived, see above);
- Endorsement from two IEEE members on the nomination;
- Optionally, a statement (up to 500 words) from the nominee on his/her vision for the journal.

Please email the nomination materials to James Skowrenski (j.skowrenski@ieee.org), no later than **July 31, 2019**.

Souvik Mahapatra
Chairman
IEEE TDMR Steering Committee

Call for Nominations Editor-in-Chief IEEE Journal of the Electron Devices Society

The *IEEE Journal of the Electron Devices Society (J-EDS)* is an open-access, fully electronic scientific journal publishing papers ranging from fundamental to applied research that are scientifically rigorous and relevant to electron devices. The J-EDS publishes original and significant contributions relating to the theory, modelling, design, performance, and reliability of electron and ion integrated circuit devices and interconnects, involving insulators, metals, organic materials, micro-plasmas, semiconductors, quantum-effect structures, vacuum devices, and emerging materials with applications in bioelectronics, biomedical electronics, computation, communications, displays, microelectromechanics, imaging, micro-actuators, nanodevices, optoelectronics, photovoltaics, power IC's, and microsensors. Tutorial and review papers on these subjects are, also, published. And, occasionally special issues with a collection of papers on particular areas in more depth and breadth are, also, published.

We invite nominations for the position of Editor-in-Chief (EiC) for J-EDS for a 3-year term beginning in **January of 2020**.

The weekly EiC's duties include assigning papers to one of the associate editors who cover the different processes, equipment, and factory operations involved in the manufacture of semiconductor integrated circuits as well as periodically answer questions from associate editors and authors. Monthly the EiC sends a memo with new peer reviewers to the associate editors. Quarterly the EiC reviews the table of contents and assigns papers to subject areas and assures the three special sections published annually are complete and include a guest editorial. Issues close about one month prior to the issue date. Annually the EiC initiates the process to select the best paper published in the prior year. The EiC is helped administratively by a person from the IEEE Publications staff.

Criteria for the Nominees:

- Ability and motivation to spend sufficient time each week assigning papers and reviewing the acceptance can rejection decisions made by the associate editors;
- Demonstrated technical leadership in at least one of the disciplines included in the EDS Field-of-Interest, which includes all electron and ion based devices, in their classical or quantum states, using environments and materials in their lowest to highest conducting phase, in simple or engineered assembly, interacting with and delivering photo-electronic, electro-magnetic, electromechanical, electro-thermal, and bio-electronic signals. The Society sponsors and reports on education, research, development and manufacturing aspects and is involved in science, theory, engineering, experimentation, simulation, modeling, design, fabrication, interconnection, reliability of such devices and their applications.
- Formal support from the institution for which the nominee works (waived if self-employed);
- Has served or currently is serving as editor or associate editor on the editorial board of T-ED, EDL, or J-EDS;
- Commitment to guide J-EDS according to this Call for Nominations;
- Suitable temperament (ability to work at all levels: editorial boards, IEEEE/EDS staff, volunteers, authors, reviewers, officers, etc.) and judgment;
- Be a member of EDS.

Requirements for Nominations:

- A brief IEEE-style biography (up to 250 words) of the nominee;
- A complete CV and list-of-publications of the nominee;
- A brief statement from the nominator on nominee's qualification and how the nominee meets the criteria listed above;
- A letter from nominee's employer indicating support for the EiC activity;
- Endorsement from two IEEE members on the nomination;
- Optionally, a statement (up to 500 words) from the nominee on his/her vision for the journal.
- Self-nominations are encouraged.

Please email the nomination materials to: James Skowrenski (J.Skowrenski@ieee.org) no later than **August 16, 2019**.

Tsu-Jae King Liu
Vice President—Publications & Products
IEEE Electron Devices Society

IEEE Annual Election

This is a reminder for EDS members to vote in the 2019 IEEE Annual Election for the following positions and candidates. Listed below are the positions and candidates that will appear on the 2019 IEEE Annual Election ballot.

The order of candidate names has been pre-determined by lottery, and indicates no preference.

Position	Candidate
IEEE President-Elect, 2020	• Susan K. "Kathy" Land (Nominated by IEEE Board of Directors) • Dejan S. Milojicic (Nominated by IEEE Board of Directors)
IEEE Division I Delegate, 2020-2021	• Alfred E. Dunlop (Nominated by IEEE Assembly)
IEEE Region Delegate-Elect/Director-Elect, 2020–2021 Region 1 (Northeastern USA)	• Bala S. Prasanna (Nominated by IEEE Region 1) • Greg T. Gdowski (Nominated by IEEE Region 1)
IEEE Region Delegate-Elect/Director-Elect, 2020–2021 Region 3 (Southern USA)	• Theresa A. Brunasso (Nominated by IEEE Region 3) • Eric Grigorian (Nominated by IEEE Region 3)
IEEE Region Delegate-Elect/Director-Elect, 2020–2021 Region 5 (Southwestern USA)	• Bob G. Becnel (Nominated by IEEE Region 5) • Ken Stuerke (Nominated by IEEE Region 5)
IEEE Region Delegate-Elect/Director-Elect, 2020–2021 Region 7 (Canada)	• Robert L. Anderson (Nominated by IEEE Region 7) • Venkataramakrishnan "Rama" Vinnakota (Nominated by IEEE Region 7)
IEEE Region Delegate-Elect/Director-Elect, 2020–2021 Region 9 (Latin America)	• Jose-David Cely (Nominated by Petition) • Lorena Garcia (Nominated by IEEE Region 9) • Enrique A. Tejera (Nominated by IEEE Region 9) • Irene P. Viana (Nominated by IEEE Region 9)
IEEE Standards Association President-Elect, 2020	• James E. Matthews (Nominated by IEEE Standards Association) • Stephen D. Dukes (Nominated by IEEE Standards Association)
IEEE Standards Association Board of Governors Member-at-Large, 2020-2021	• Andrew F. Myles (Nominated by IEEE Standards Assoc.) • Masayuki Ariyoshi (Nominated by IEEE Standards Assoc.) • Yu Yuan (Nominated by IEEE Standards Association)
IEEE Technical Activities Vice President-Elect, 2020	• Maciej J. Ogorzalek (Nominated by IEEE Tech. Activities) • Roger U. Fujii (Nominated by IEEE Technical Activities)
IEEE-USA President-Elect, 2020	• Katherine J. Duncan (Nominated by IEEE-USA) • Brendan B. Godfrey (Nominated by IEEE-USA)

Balloting period starts on 15 August 2019 and ends at 12:00 PM, Eastern Time USA (16:00 UTC) on 1 October 2019. All eligible voting members can access their ballot electronically at www.ieee.org/elections. In accordance with their member communication preferences on record on 30 June 2019, voters will receive voting instructions via email and/or a ballot package via postal mail (members can vote electronically, on paper ballots, but only one ballot will be accepted.) For more information on the election and candidates, visit the IEEE Annual Election web page at www.ieee.org/elections, or email election@ieee.org.

CALL FOR NOMINATIONS

2019 IEEE EDS Early Career Award

Description: Awarded annually to an individual to promote, recognize and support Early Career Technical Development within the Electron Devices Society's field of interest

Prize: An award of US$1,000, a plaque; and if needed, travel expenses not to exceed US$1,500 for a recipient residing in the US and not to exceed US$3,000 for a recipient residing outside the US to attend the award presentation.

Eligibility: Candidate must be an IEEE EDS member and must have received his/her first professional degree within the 10th year defined by the August 15 nomination deadline and has made contributions in an EDS field of interest area. Nominator must be an IEEE EDS member. Previous award winners are ineligible.

Selection/Basis for Judging: The nominator will be required to submit a nomination package comprised of the following:

- The nomination form that is found on the EDS web site, containing such technical information as the nominee's contributions, accomplishments and impact on the profession or economy and a biographical description.
- A minimum of two and a maximum of three letters of recommendation from individuals familiar with the candidate's technical contributions and other credentials, with emphasis on the specific contributions and their impacts.

The basis for judging includes such factors as: the demonstration of field leadership in a specific area; specific technical contribution(s); impact on the profession or economy; originality; breadth; inventive value; publications; honors; and other appropriate achievements.

Schedule: Nominations are due to the EDS Executive Office on August 15th each year. The candidate will be selected by the end of September, with presentation to be made in December.

Presentation: At the EDS Awards Dinner that is held in conjunction with the IEEE International Electron Devices Meeting (IEDM) in December. The recipient will also be recognized at the December EDS Board of Governors Meeting.

Nomination Form: Complete the nomination form by August 15, 2019. All endorsement letters should be sent to l.riello@ieee.org by the deadline.

For more information contact: l.riello@ieee.org or visit: http://eds.ieee.org/early-career-award.html

The IEEE Electron Devices Society is looking for volunteers to act as our information channels and promoters of networking between the regions. Interested volunteers should contact the EDS Young Professional Chair.

We would like to continue sharing what we do around the world to strengthen the EDS mission. We invite you to contribute chapter news or relevant information that may be posted on our social networks.

EDS Mission Statement

To foster professional growth of its members by satisfying their needs for easy access to and exchange of technical information, publishing, education, and technical recognition and enhancing public visibility in the field of Electron Devices.

IEEE Advancing Technology for Humanity

IEEE Electron Devices Society

Please follow us on social media:

IEEE Electron Devices Society

@IEEEElectronDevicesSociety

@IEEEEDS

Chapter News

2019 EDS Chapter of the Year Award— Call for Nominations

ED Malaysia Chapter officers - proud recipients of the 2018 EDS Chapter of the Year Award, presented by MK Radhakrishnan, EDS Vice President of Regions and Chapters (right)

The EDS Chapter of the Year Award is given each year based on the quantity and quality of the activities and programs organized by the chapters for the benefit of members and professionals during the prior July 1st – June 30th period.

Each year EDS will award one Chapter from each of the following Regions:

- **Regions 1-7**
- **Region 8**
- **Region 9**
- **Region 10**

Nominations for the awards can only be made by SRC Chairs/Vice-Chairs, Regions/Chapters Committee Members or self-nominated by Chapter Chairs. Please visit the EDS website to submit your nomination form (http://eds.ieee.org/chapter-of-the-year-award.html).

Each winning chapter will receive a plaque and check for $500 to be presented at an EDS chapter meeting of their choice. Travel reimbursement will not be provided. A chapter that wins the Chapter of the Year Award is eligible for nomination after a lapse of 3 years only.

The schedule for the award process is as follows:

Action	**Date**
Call for nominations e-mailed to chapter chairs, SRC Chairs, SRC Vice-Chairs and Regions/Chapters Committee	June 1st
Deadline for nominations	September 15th
Regions/Chapters Committee & SRC Chairs & Vice Chairs selects winners	Early-October
Award given to chapter representative at requested chapter meeting	Open

ED UNICAMP Student Chapter Organizes SEMINATEC 2019

By Lucas Spejo, Paula Petrini, Lucas Zucchi and Lenon Costa

The 14th Workshop on Semiconductors and Micro & Nano Technology—SEMINATEC 2019—was held on April 11 and 12, 2019 at the State University of Campinas (UNICAMP), Brazil. The purpose of SEMINATEC is to promote the interaction among industry, academy, research and development centers, government and students, all looking for real opportunities towards improving semiconductor and micro & nano technologies, research, and education. A total of 120 persons attended the Workshop. This year, SEMINATEC was organized by the EDS Student Chapter at UNICAMP, with additional support and funding from EDS and SSCS South Brazil Chapters and the EDS student chapter at FEI. Each of these four chapters invited a Distinguished Lecturer (DL) to visit them and participate at SEMINATEC to deliver a keynote talk. The four Distinguished Lecturers (DLs) and titles were as follows:

- *"Self-Heating in FinFETs and Its Impact on Logic Circuits,"* by Prof. Durga Misra (NJIT)
- *"A review of DC extraction methods for MOSFET series resistance and mobility degradation model parameters,"* Prof. Adelmo Ortiz-Conde (Simon Bolivar University)
- *"Fully Printable and Autonomously Powered Electronic Nodes for the Internet of Everything,"* by Prof. Paul Berger (Ohio State University)
- *"Low power clocking for energy conscious IoT systems,"* by Prof. Sudhakar Pamarti (UCLA).

SEMINATEC 2019—Distinguished Lecturers and organizing committee members, from left to right, sitting: Sudhakar Pamarti, Durga Misra, Adelmo Ortiz, Paul Berger, Jacobus Swart; Standing: Lenon da Costa, Paula Petrini, Lucas Spejo, Joao Martino, Jose Diniz, Marcelo Pavanello, Lucas Zucchi and Aymara Silva

SEMINATEC 2019—Poster Session

These talks covered state-of-the-art new devices, models, circuit design and applications, making the event of interest to members of both EDS and SSCS communities. In addition, company leaders and government officers gave presentations about local activities and challenges in the field of micro and nanoelectronics, especially companies doing IC design and packaging. A list of the companies and institutions that gave presentations are as follows: CADENCE, CCSNano, CEITEC, Chipus, CTI, Eldorado Institute, Idea! Sistemas Eletronicos, Imec, LSI/USP, MCTIC and Smart Modular Technologies. These additional presentations gave added value to SEMINATEC, attracting students and promoting discussions about possible collaborations. A poster session was held on the first day and over 40 selected papers

were presented. The four DLs helped to review the posters in order to select one for the best paper award. The selected best paper was "*Magneto-electrical Transport Improvements of Postgrowth Annealed Iron–Cobalt Nanocomposites: A Route for Future Room-Temperature Spintronics,*" presented by M. V. Puydinger dos Santos. A second paper, entitled *"Back Enhanced (BE) SOI pMOSFET Light Sensor"* presented by J. A. Padovese, received an Honorable Mention.

More details on SEMINATEC 2019 are available at the website: https://www.ccs.unicamp.br/seminatec/

Partial funding for the Workshop was granted by CNPq (Brazilian Agency for S&T) and coffee breaks were financed by four sponsoring companies. No registration fee was requested to participants in order to attract a broader audience and to promote the IEEE EDS and SSCS societies.

~ Edmundo Guiterrez, Editor

Save The Date—MQs and DLs of Region 8

Dear IEEE EDS members, please keep the following upcoming MQs & DLs of Region 8 in mind.

In July two DLs are announced: On July 11th, the Arokia Nathan Distinguished Lecture is held at Universitat Rovira Virgili (Tarragona, Spain). Detailed information are available by Benjamin Iniguez (benjamin.iniguez@urv.cat).

The second DL is given on July 26th. Detailed information of the Rajiv Joshi Distinguished Lecture are available by Shih-Chii Liu (shih@ini.uzh.ch).

In September a DL with Prof. Vijay K. Arora is announced: On September 12th, the Vijay K. Arora Distinguished Lecture is held at imec (Leuven, Belgium). Detailed information are available by Eddy Simoen (Eddy.Simoen@imec.be).

EDS Chapter Subsidies for 2020

EDS is providing funds to those EDS chapters that are requesting a subsidy based on the EDS chapter subsidy guidelines. The deadline for EDS chapters to request a subsidy for 2020 is September 1, 2019. In 2019, EDS awarded subsidy funds to 69 chapters, with most amounts primarily ranging from US$500 to US$1,000. All Chapter Chairs were informed through an email notifying the subsidy details and guidelines in June. Chapter subsidy is pegged to the activities reported to IEEE and EDS through online activity reports and chapter growth.

In general, activities which are considered fundable include, but are not limited to, membership promotion, travel allowances for invited speakers to chapter events, and support for EDS student activities at local institutions.

Chapter Subsidies can be requested by completing the EDS Chapter Subsidy Request Form http://eds.ieee.org/chapter-subsidy-program.html. Please note that the 2020 subsidy request needs to be submitted by September 1, 2019.

Final decisions concerning subsidies will be made in December 2019. Subsidy funds will be issued by early January of the following year. Please visit the EDS website http://eds.ieee.org/chapter-subsidy-program.html for more information.

Symposium on Schottky Barrier MOS Devices "Towards Neuromorphic and Quantum Computing Applications"

By Mike Schwarz

A symposium on Schottky Barrier MOS (SB-MOS) devices is planned for October 4, 2019, at the new Center for Nanoscience and Nanotechnology laboratory in Palaiseau, France. This is the third meeting of an enthusiastic group of Schottky barrier researchers. This year's symposium is sponsored by LabexNanoSaclay, the IEEE EDS France Chapter, the Robert Bosch GmbH and Silvaco, Inc.

Before announcing more details, a brief history. The first meeting of this group was held on August, 5, 2016, in Ueberherrn, Germany, a spontaneous workshop organized by Dr. Mike Schwarz (Robert Bosch GmbH, Germany), Dr. Tillmann Krauss (TU Darmstadt, Germany), and Dr. John P. Snyder (JCap, LLC). Shortly after the meeting, Dr. Laurie E. Calvet (Université Paris-Sud, France), Prof. Udo E. Schwalke (TU Darmstadt, Germany) and Prof. Alexander Kloes (THM, Germany) got together, and some great contributions were the result, e.g. "On the Physical Behavior of Cryogenic IV and III-V Schottky Barrier MOSFET Devices M. Schwarz," L.E. Calvet, J.P. Snyder, T. Krauss, U. Schwalke, A. Kloes, *IEEE Transactions on Electron Devices* 64 (9), 3808–3815. The 2nd symposium followed at the Institut für Halbleitertechnik und Nanoelektronik (IHTN) of TU Darmstadt on August 7, 2018, on Schottky barrier MOS devices—"devil or savior." A report on this event was published in the April 2018 issue of this newsletter. More contributions are in progress and will hopefully find their way into the EDS community.

This year the theme of the symposium is *"Towards neuromorphic and quantum computing applications,"* organized by Dr. Laurie Calvet (C2N, Palaiseau, France), Dr. Francesca Chiodi (C2N, Palaiseau, France), Dr. Mireille Mouis (IMEP-LAHC, Grenoble INP, France) and Dr. Mike Schwarz (Robert Bosch GmbH, NanoP THM, Germany) and the staff at the Centre of Nanoscience and Nanotechnology at the Université Paris-Sud.

The symposium begins on October 4th at 9:00 a.m. and the following speakers have confirmed their invitations: Prof. Benjamin Iniguez (DEEEA, Universitaet Rovira I Virgili), Dr. Laurie E. Calvet (C2N, CNRS-Université Paris-Sud), Dr. Mike Schwarz (Robert Bosch GmbH, NanoP THM, Germany), Dr. David Green / Dr. Ahmed Nejim (Silvaco Inc.), Dr. John Snyder (JCAP, LLC), Dr. Francesca Chiodi (C2N, CNRS-Université Paris-Sud), Dr. François Lefloch (CEA, Grenoble), and Dr. Fabrice Nemouchi (CEA, Grenoble).

All are welcome to attend the symposium. Further information and a registration form are available at https://ssbmos.blogspot.com/

Distinguished Lecture at ED/CAS North Jersey Chapter

by Durga Misra

The North Jersey Chapter and New Jersey Institute of Technology in Newark, New Jersey, organized an IEEE Electron Devices Society Distinguished Lecture (DL) on May 1, 2019. The DL was also co-sponsored by the AP/MTT and Photonic chapters of North Jersey Section. The EDS Distinguished Lecturer, Dr. Anirban Bandyopadhyay, Director, RF Strategic Applications & Business Development, of GLOBALFOUNDRIES, Inc., USA, gave a talk on "5G Enhanced Mobile Broadband Radio interface on mmWave—Hardware Architecture and role of Silicon Technologies." The talk outlined the 5G, the next generation cellular standard that covers different usage scenarios covering enhanced mobile broadband (eMBB), ultra-reliable, low latency communication (uRLLC) and low power massive machine-to-machine communication (mMTC). The talk highlighted the need for mmWave based mobile communication, different hardware architecture options for the radio interface of mmWave 5G eMBB and technology challenges associated with each option to be implemented. The key figures of merits for 5G mmWave radio hardware, different chip partitioning options and how different silicon technologies like partially and *fully depleted SOI, Silicon-Germanium BiCMOS* were discussed.

From left to right: Edip Niver, Durga Misra, Anirban Bandyopadhyay, Ajay Poddar, Naresh Chand, Har Dayal

ED Scotland Chapter Initiative to Grow IEEE Student Branches

by Marc Desmulliez

ED Scotland, the Scottish Chapter of the IEEE Electron Devices Society has an ongoing initiative to help establish and grow IEEE Student Branches within Scottish Universities. In January, as part of this initiative, the Chair of ED Scotland, Professor Marc Desmulliez participated in the Semester 2 Opening Meeting of the Heriot-Watt University IEEE Student Branch.

In a presentation given by the current Chair of the Student Branch, Duncan Fraser, the large and appreciative audience was provided with details of the present and future activities of the Branch, as well as the various volunteer opportunities available. Two key upcoming events for the Branch will be workshops on both *Public Speaking* and *Python Programming*.

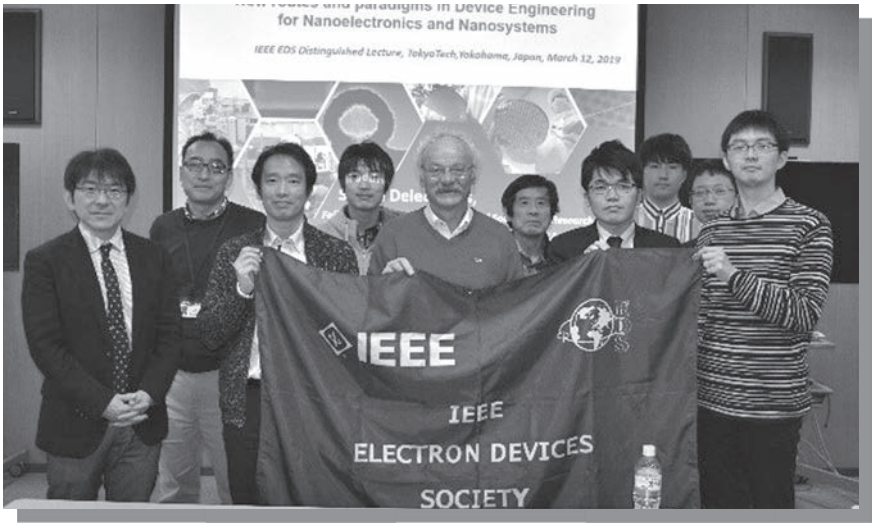
Duncan Fraser (left) and Marc Desmulliez at the Heriot-Watt University IEEE Student Branch Semester 2 Opening Meeting

~ Jon Terry, Editor

EDS Distinguished Lecture at ED Japan Chapter

by Akira Nishiyama and Yuichiro Mitani

The ED Japan Joint Chapter (Chair: Akira Nishiyama) held an EDS Distinguished Lecturer program on March 12th in Tokyo, Japan, co-hosted with the Department of Electrical and Electronic Engineering (Prof. Kuniyuki Kakushima), Tokyo Institute of Technology. Dr. Simon Deleonibus, former LETI Chief Scientist, lectured on "New routes and paradigms in Device Engineering for Nanoelectronics and Nanosystems", in which novel transistor technologies including these diversification (e.g. the application to neuromorphic computing) was introduced after the comprehensive review of traditional electric devices. After his talk, the detail processes and the outlook of this technology were discussed with the attendees.



Dr. Simon Deleonibus, Prof. Kuniyuki Kakushima (Associate Professor of Department of Electrical and Electronic Engineering, Tokyo Institute of Technology), Dr. Yuichiro Mitani (Secretary of ED Japan Joint Chapter)

~ Kuniyuki Kakushima, Editor

EDS Malaysia Wins Outstanding Chapter Award 2018 from IEEE Malaysia Section

by S.Noorjannah Ibrahim, Zubaida Yusoff, Rosminazuin Ab Rahim & Aliza Aini

The ED Malaysia Chapter won the IEEE Malaysia Section's Outstanding Large Chapter Award 2018 during the Section Appreciation Dinner held at Everly Hotel Putrajaya on January 19, 2019. The purpose of the award is to recognize the outstanding performance of the best chapter among the 27 technical chapters in the Malaysia Section, which has successfully served their members and the technical community with voluntary service, while retaining their membership. Meanwhile Dr. Rosminaziun from EDS Malaysia and IIUM also won the IEEE Malaysia Section's Outstanding Volunteer Award 2018 as 2nd runner-up. Congratulations to EDS Malaysia Chapter volunteers!

EDS Malaysia receiving the Outstanding Large Chapter Award 2018 from IEEE Malaysia Section

Reaching Out to "Orang Asli" (Malaysia's Indigenous People) Through the EDS-ETC Program

The ED Malaysia Chapter in collaboration with Perintis Youth Club IIUM Chapter and Kulliyyah of Engineering, IIUM, organized a program named "Electronics Magic" for children from the *Orang Asli* (Malaysia's Indigenous People) Community from Asrama Darul Falah Kuala Lumpur (ASDAF). A total of 33 students, aged 13–17 years old participated in the event. The students were supervised by 2 ASDAF guardians throughout the program. The children were exposed to the beautiful world of science and electronics. By utilizing the easy to use Elenco Snap Circuits kits, students were able to learn about electronics through active learning. We believe it is important to touch their hearts through education that will make them realize how important they are to our local community. These young children and youth will return to their Orang Asli community and be an inspiration to their younger generations, which will improve their quality of life in the future. The students' feedback was positive, as they could understand the basic theory by constructing simple electronic circuits.

~ P Susthitha Menon, Editor

Group photo with IEEE volunteers and children's guardians

9th IEEE EDS Mini-Colloquium on "Quantum Electronics"

by Ajit Kumar Panda

The ED NIST Student Chapter organized a One-Day Mini-Colloquium on "Quantum Electronics" on March, 1, 2019 at NIST, Berhampur, Odisha, India, in which five Distinguished Lecturers from India participated (Dr. G. N. Dash, Dr. Subir Kumar Sarkar, Dr. Chandan Kumar Sarkar Dr. Brajesh Kumar Kaushik and Dr. Ajit Kumar Panda). In attendance were 135 students and faculty members from NIST-Berhampur, KIIT-Bhubaneswar, VSSUT-Burla, Berhampur University, SOA University, and the Institute of Electronics and Radio Physics, West-Bengal. The event was fully sponsored by the ECE Department of NIST.

Attendees of the IEEE EDS Mini-Colloquium at NIST

IEEE EDS Mini-Colloquia Organized by ED/CAS Hyderabad Chapter

by Mohammed Arifuddin Sohel

The ED/CAS Chapter of IEEE Hyderabad Section organized an IEEE EDS Mini-Colloquia on February 24, 2019 at The Plaza Hotel. Dr. Arif Sohel, Chair of the joint chapter and Dr. Charvaka Duvvury addressed the gathering about the key areas of focus of the IEEE Electron Devices Society and the various

Mini-Colloquia Attendees at ED/CAS Hyderabad Chapter

membership benefits offered by the society. This was followed by a Distinguished Lecture(DL) on "ESD Issues and Challenges for Advanced Semiconductor Technologies" by Dr. Duvvury, in which he focused on the understanding of ESD and how this is applied to develop protection at the IC level for Digital, Analog, and RF circuits.

The second DL on "FOSS TCAD/EDA Process/Device Simulations for Compact/SPICE Modeling" was delivered by Dr. Wladek Grabinski. His talk focused on the Compact modeling of circuit elements to enable advanced IC Design using nanoscale semiconductor technologies. The final lecture was given by Dr. Roberto Murphy who spoke about the "Fundamental aspects of CMOS RF Modeling and Characterization," in which he highlighted characterization techniques, substrate network effects and geometry effects which make the characterization more time consuming. There were 35 attendees at the MQ, of which 25 were IEEE members, with representatives from Industry, Academia and Research labs.

EDS-ETC Program at HIT Student Branch Chapter

The ED Heritage Institute of Technology Student Branch Chapter, Calcutta, India, jointly organized an EDS-ETC program with EDS CoE, Heritage Institute of Technology and ED HIT SBC on February 16, 2019 at the TAMAS Society, and on February 17, 2019 at the Shanti Rani Primary School Bansdroni, Kolkata. A few projects were demonstrated to the students with the help of the Elenco Snap Circuits© kits.

Snapshots of EDS-ETC Program in action

2019 IEEE International Conference on Modeling of Systems Circuits and Devices

by Mohammed Arifuddin Sohel

All the MOS-AK/India Conference participants at IIT Hyderabad

The MOS-AK Compact Modeling Association, a global standardization forum for semiconductor device models, held its consecutive 2nd International IEEE MOS-AK India Conference 2019 between February 25-27, 2019 at the IIT Hyderabad. The 2nd International IEEE MOS-AK India Conference 2019 is the results of join, collaborative effort. The conference organization would not be possible without direct involvements and financial support provided directly by Collage and IIT Hyderabad as well as the MOS-AK distinguished industrial sponsors including: ams semiconductors, Rhode and Schwarz, Keysight, Synergy, Synopsys, Xilinx and SCL. The MOS-AK India Conference has also drawn the attention of the Joint Chapter of the CAS and EDS Societies of the IEEE Hyderabad Section which provided direct technical program cosponsorship. The Indian Electronic Semiconductor Association (IESA) as well as Swissnex India have provide pronounced dissemination support. Inauguration session of 2nd International IEEE MOS-AK India Conference 2019 has been chaired by Prof. Mohammed Arifuddin Sohel, MJ College Hyderabad, who welcomed all MOS-AK participants and invited prominent guests Surinder Singh, Director, SCL; Sebasties Hug, CEO and Consul General of Swissnex; Sumohan Chenapayya, Dean R&D, IIT Hyderabad; V. Hanuma Sai, Director, ams semiconductors India Pvt. Ltd.; N. Venkatesh, Chair, IEEE Hyderabad Section; Wladek Grabinski, MOS AK (EU); P.A. Govindacharyulu, General Co Chair, MOS AK India 2019 to open the 2nd MOS-AK/India Conference. The MOS-AK India Conference program has been organized as three days scientific R&D event covering recent advances into the technology TCAD simulations, compact/SPICE modeling as well as the device level analog/RF and digital IC designs. The internationally renowned academic and industrial speakers and presenters have delivered 4 tutorial lectures [1–4], 7 keynote talks [5–11], 2 plenary talks [12–13] as well as 22 regular research papers. The MOS-AK Association is an open research forum adequately supporting all R&D activities. An open panel discussion was organized to review challenges and opportunities for women in engineering (WIE) [14]. The MOS-AK speakers shared their latest perspectives on compact/SPICE modeling and Verilog-A standardization in response to the dynamically evolving semiconductor industry and academic R&D efforts. The event featured advanced technical presentations covering compact model development, implementation, and deployment.

~ Manoj Saxena, Editor

Regional News

USA, Canada & Latin America (Regions 1–6, 7 & 9)

IEEE Latin America Regional Meeting

—by Edmundo Gutierrez

The IEEE Puebla Section and the ED Puebla Chapter were the local organizers of the Region 9 regional meeting held March 6–9, 2019, in Puebla, Mexico. This meeting had a total attendance of 74 delegates from Region 9, Canada, USA, and Europe. Some of the attendees were Jose Moura IEEE President, Jim Jefferies IEEE Past President, Francis Grosz VP-MGA, Stephen Welby IEEE Executive Director, Jamie Moesch Educational Activities Managing Director, Susan Kathy Land Past VP Technical Activities, Dejan Milojicic Past Director Division VIII, Fernando Guarin, EDS President, Maike Luken, IEEE Region 7 Director, Mary Lynne Nielsen Global Operations & Outreach Program Director IEEE Standards Association, Julianna Pichardo Program Specialist, Humanitarian Activities & Sustainable Development, Eva Veloso IEEE International Area Manager Southern Europe and Latin America, John Day Director Member Products & Programs, Julie Bernicker Product Specialist IEEE Collabractec, and Teofilo Ramos Region 9 Director.

The first day was dedicated to: 1. IEEE strategic directions, challenges and opportunities, 2. IEEE MGA strategy and focus, 3. educational activities opportunities, 4. leveraging local strengths, 5. industry engagement, 6. celebration and innovation of women in engineering meeting the challenges of sustainable development, 7. IEEE standards association and Region 9, 8. HAC and SIGHT opportunities, 9. IEEE Xplore, and 10. IEEE Collabratec update and direction.

The second day focused on 1. Collabratec training workshop, 2. Introduction to social return on investment (SROI) assessment methodology, and 3. Councils meetings. A social activity that consisted of a visit to the archaeological site Cacaxtla took place in the afternoon. The group visited the famous "gran basamento" founded between 100–1100 BC.

On the third day we had; 1. the IEEE President-Elect candidates presentations and Q&A, 2. Awards & recognitions, 3. Best Achievement Award, 4. Educational activities in Region 9, 5. student activities, and the final closing ceremony and official picture.

~ Edmundo Guiterrez, Editor

Europe, Middle East & Africa (Region 8)

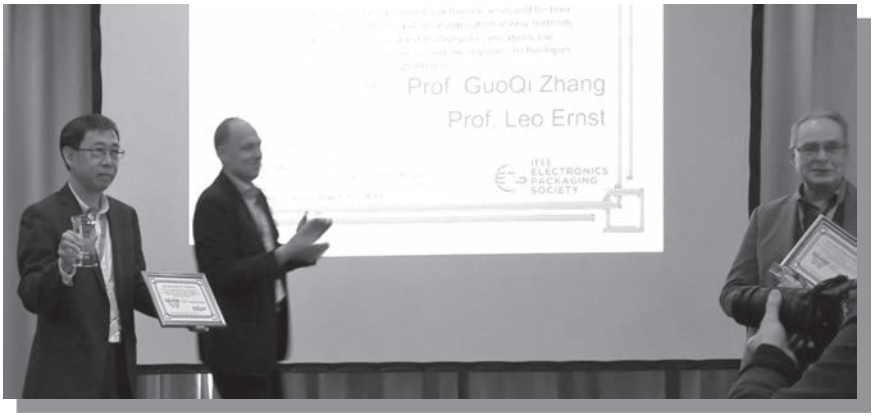
20th EuroSimE in Hanover, Germany

The 20th EuroSimE was held in the city of Hanover, Germany, from March, 24-27, 2019. It was supported by the Leibniz Universität Hanover Institute of Microelectronic Systems and as local organizer resri (reliability simulation & risk analysis) as well as Prof. Dr.-Ing. Dipl.-Phys. Kirsten Weide-Zaage.

The conference hosted 85 oral presentations and 15 posters on these topics:

- Solder joint reliability
- MEMS structures
- Thermal Behavioral Modelling
- Prognostics and health monitoring
- Multi-Physics process models
- Package level thermo-mechanical assessment
- System level mechanical reliability
- Thermal Modelling and Characterization

Attendees of the 2019 IEEE Latin America Regional Meeting in Puebla, Mexico



Prof. Leo Ernst (left), Prof. Willem van Driel and Prof. Guoqi Zhang during the Award ceremony

- Solid State Lighting
- Electronics reliability under vibration loadings
- Multiphysics/Scale analysis—including moisture, electromigration, etc.
- High power applications
- IC level thermo-mechanical analysis
- Advanced experimental analysis techniques

Twenty hours of short courses were given on the following topics:

- Prof. Dr.-Ing. Tamara Bechtold: System-Level Simulation of Microsystems-MOR
- Prof. Alberto Corigliano: Design for Reliability in MEMS
- Dr. Nancy Iwamoto: Molecular Modelling
- Prof. Sheng Liu: Power Electronics Packaging
- Prof. Reinhard Pufall: Reliability of Semiconductor Devices—Simulation as a crucial tool to support semiconductor reliability assessment
- Prof. Jeffrey C. Suhling: Applications of test chips

Additionally, the program hosted industry keynotes by:

- Udo-Martin Gómez (Robert Bosch GmbH): Pushing the limits of MEMS—Success factors design and simulation
- Ahmer Syed (Qualcomm): Package Developments at Qualcomm
- Darrel Frear (NXP): Package Development for Autonomous Driving

Furthermore, the conference included a visit to the Robert Bosch plant in Salzgitter.

During the conference, Prof. Leo Ernst and Prof. Guoqi Zhang received the "Achievement Award" of EuroSimE for their outstanding work during the last two decades.

EuroSimE 2019 was technically sponsored by the IEEE Electronics Packaging Society, and financially sponsored by Leibniz Universität Hanover, resri, Robert Bosch GmbH, Huawei, Philips and Siemens.

2019 IEEE International Nanodevices and Computing Conference (INC)

—by Mike Schwarz

The IEEE International Nanodevices and Computing Conference (INC), was held from April 3–5, in Grenoble, France, and hosted by the Maison Minatec conference center. This year's conference was sponsored by IEEE, IEEE Rebooting Computing, INC, IRDS, SINANO Institute, IEEE EDS France Chapter, IMEP-LAHC, CEA-LETI, NEREID, CNRS, Grenoble INP, Université Grenoble Alpes, hawAi.tech, Aeneas, PERSYVAL-Lab, FMNT, Labex MINOS and the Fondation nanoSCIENCES.

The new INC conference covered the continuously evolving technology ecosystem based on nanotechnology, nanodevices and computing, supporting the global information technology infrastructure. It included predictions on devices for computing and communications, computer architecture, and applications. Reports from 2017 IRDS™

Attendees of INC conference

and early results from 2018 IRDS™ reports were presented. In addition, state-of-the-art experimental results on these topics were presented by an international group of invited experts, covering Nano-devices and -materials in the fields of More Moore, More than Moore and Beyond-CMOS. Related subjects from the European Nanoelectronics Roadmap (NEREID) and the Systems and Devices Roadmap of Japan (SDRJ), as well as the latest results in the field of Neuromorphic Computing, Quantum Computing, Optical Computing and Energy Efficient Computing, were highlighted. A unique summary from reports of the upcoming FutureNetworks™ Beyond 5G roadmap were presented, as well as sessions on Software and Spintronics/Magnonics.

The conference hosted various presentations in 13 sessions on the topics of:

- Emerging technology for probabilistic interference
- Panel Session "The next 20 years"
- IRDS International Roadmap for Devices and Systems
- European NEIREID Roadmap
- Systems and Devices Roadmap of Japan (SDRJ)
- Status and trends in Advanced Nanodevices
- Neuromorphic computing
- Quantum and probabilistic computing
- Optical computing
- Energy efficient computing
- Communications Beyond 5G
- Software
- Spintronics/Magnonics

Additionally the program hosted keynotes by:

- Future Technologies–Dr. Bill Chappel, Microsystems Technology
- Architecture – Prof. Wen-mei Hwu, University of Illinois

Kuei-Shu Chang-Liao Distinguished Lecture

On April 1st the IEEE Distinguished Lecture "High-k Dielectric and Interface Engineering for High Performance Si/Ge MOS and FinFETs" by Prof. Kuei-Shu Chang-Liao from National Tsing Hua University, Department of Engineering and System Science, Hsinchu, Taiwan was held at IMEP-LAHC, Grenoble INP-Minatec.

Within the lecture the attendees learned from new experimental data how to engineer interfaces for high performance Si/Ge MOS and FinFETs and to include high-k dielectrics and their impact on performance boost of such devices.

~ Mike Schwarz, Editor

Asia & Pacific (Region 10)

ED Kansai

—by Hiroyuki Nishinaka

The ED Kansai Chapter held a Technical Meeting on January 19, 2019 at Kyoto Institute of Technology, Kyoto, Japan, and invited 2 prestigious lecturers. The 41 attendees, including EDS members and students enjoyed two distinguished talks:

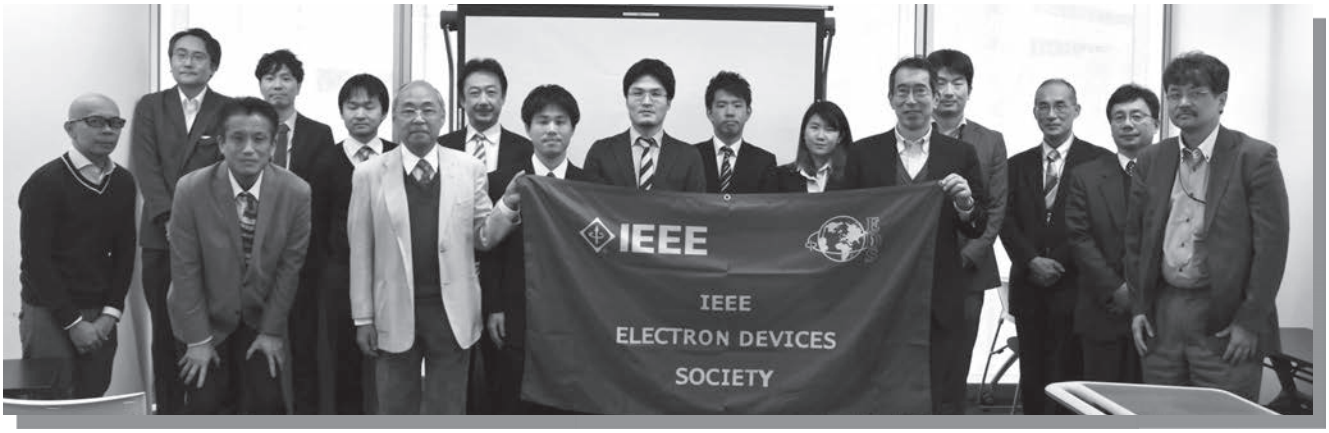
- "Research of brain-like devices, circuits, and systems using functional oxide materials and future prospects," by Dr. Hiroyuki Akinaga of Advanced Industrial Science and Technology (AIST).
- "Felloelectric application devices for IoT," by Dr. Akira Ando of Murata Manufacturing.

After the technical meeting, we held the annual general meeting to select new officers for a two-year term, to review chapter activities of 2018, and to discuss plans for 2019.

The 18th annual Kansai Colloquium Electron Devices Workshop on January 24, 2019 at Umeda Campus of Ryukoku University, Osaka, Japan was hosted and attended by 21 participants, including 15 IEEE members. The Workshop program committee members carefully reviewed papers published in the past 12 months from various prestige conferences and technical journals such as IEDM or SSDM as well as IEEE transactions to select top 10 papers from authors in the Kansai area.

The Award Committee selected one paper for the 18th IEEE EDS Kansai Chapter of the Year Award. The winning paper was "Reliability-aware design of metal/high-k gate stack for high-performance SiC MOSFET," by Dr. Takuji Hosoi of Osaka University. The committee also selected one paper from student presenters for the IEEE EDS Kansai Chapter MSFK Award. The winner was Dr. Satoshi Okuda of Osaka University for the paper entitled "Chemical sensing using graphene-based surface-acoustic-wave sensor." The presented papers were all excellent and stimulated many questions and discussions with the audience, as they were selected from already qualified papers of major conferences and technical journals. This workshop is playing an important role in encouraging students and young engineers in the industry to extend their technical knowledge and career.

Invited lecturers: (left photo) Dr. H. Akinaga, (right photo) Dr. A. Ando at the technical meeting



Participants of the 18th annual Kansai Colloquium Electron Devices Workshop

Annual Meeting of the ED Japan Joint Chapter

—by Akira Nishiyama and Yuichiro Mitani

On January 25, 2019, the annual meeting of the ED Japan Joint Chapter was held at Research Center for Advanced Science and Technology, The University of Tokyo. Dr. Akira Nishiyama, Japan Joint Chapter Chair and Prof. Toshiro Hiramoto, Vice Chair, reported 2018 activities and 2019 plans of the Chapter. At the meeting, the 2018 ED Japan Joint Chapter Student Award (VLSI & IEDM) was presented to 8 students, who made excellent presentations at the VLSI Symposia 2018 and IEDM 2018. The award winners are posted on the Japan Joint Chapter's webpage; (http://www.ieee-jp.org/japancouncil/chapter/ED-15/ed15_award.htm).

After the annual meeting, the IEDM 2018 Report Session was held, with 9 members of the IEDM program committee reporting on summary, topics and research trends of their sub-committees for more than seventy attendees. The session provided a good opportunity for the attendees to touch the latest technology trends, especially for those who were unable to attend the IEDM.

The executive committee meeting of the ED Japan Joint chapter was also held on the same day and the plans for 2019 were approved.

~ Kuniyuki Kakushima, Editor

17th ED Japan Joint Chapter Student Award winners, together with Dr. Akira Nishiyama; Chair, and Prof. Toshiro Hiramoto; Vice Chair on January 25, 2019, Tokyo

The annual meeting of EDS Japan Joint Chapter attendees on March. 25, 2019, Tokyo

IEEE EDS Distinguished Lectures Held in China

ED Hangzhou Chapter

—by Lingling Sun

A Distinguished Lecture was jointly organized by the ED Hangzhou Chapter and the School of Electronics and Information, Hangzhou Dianzi University, on March 12, 2019 at Hangzhou Dianzi University, Hangzhou, China. Dr. Xing Zhou, was invited to give a talk on "Future III-V/CMOS Co-Integrated Technology and Hybrid Circuit Design." Prof. Bin You of Hangzhou Dianzi University served as the chair of the DL. Dr. Xing Zhou, IEEE EDS Distinguished Lecturer from Nanyang Technological University, Singapore, presented an overview of the SMART-LEES (Singapore MIT Alliance for Research and Technology–Low Energy Electronic Systems) program. He also spoke about a unified compact model for generic GaN/InGaAs-based HEMTs in the context of the monolithic III-V + CMOS co-integrated technology being developed for future heterogeneous integrated circuits. His lecture attracted about 20 attendances of professors and graduate students.

ED/CPMT Shanghai Chapter

—by Yulong Jiang

On March 26, 2019, the ED/CPMT Shanghai Chapter held an EDS Distinguished Lecture at Fudan University. Prof. Hiroshi Iwai from Tokyo Institute of Technology, Japan, delivered the presentation with a topic of "End of CMOS miniaturization and technology development after that."

In Prof. Iwai's lecture, he mentioned that the CMOS miniaturization will reach its limit substantially in several years. However, semiconductor technology development will continue into the future after that. The limit of the CMOS miniaturization was explained and the semiconductor device technology development after reaching the scaling limit was discussed. About 20 EDS members and student members attended this activity.

ED Hangzhou DL on March 12 (first row from left) Xing Zhou (3rd, speaker), Lingling Sun (4th, Chapter Chair), Bin You (5th, Talk Chair)

ED/CPMT Shanghai Chapter, DL on March 26 (first row from right) Prof. Hiroshi Iwai (5th, speaker) with the other attendees

ED Xi'an Chapter

—by Jiale Sun

On January 1, 2019, Li Zhang, presented two talks on "A new delay design architecture for digital circuits" and "Crossbar structure based on memrister and its application in AI" at Xidian University, Xi'an, Shaanxi, China. This lecture was held at the Auditorium in the East Building. More than 100 students from the School of Microelectronics enjoyed her excellent presentation.

The performance of traditional digital circuits has reached its limit. In order to break through the computational bottleneck of the circuit, a new digital circuit delay design architecture was introduced in Dr. Zhang's first report. This new architecture ensured the normal operation of circuit functions and improves circuit safety through the use of utilities.

Inspired by the computational characteristics of the human brain, the computational architecture of neural morphology plays a great role in promoting the development of artificial intelligence. The second report presented a method for reducing the effects of aging and temperature in training and mapping engineering. This method can greatly improve the life and precision of Crossbar based on memristor, and had practical significance for promoting the application of this new circuit.

On March 14, 2019, Yonggang Zheng and Cong Liu from Mediatek (Hefei), Inc. presented talks on "The Glance On IC Low Power Design Technology" and "Data Converter Application and Trend" at Xidian University, Xi'an, Shaanxi, China. The lectures were held at the Auditorium in the East Building. More than 120 students from the School of Microelectronics participated in this event.

In recent years, China's imports of electronic components (including ASIC) has exceeded oil, to become the first major commodity import. The country is also strongly supporting the development of the Integrated Circuits industry. And that's why two advance managers were invited to lecture in this lecture series. In Yonggang Zheng's talk, he presented a brief introduction on low power technology in circuits design. Meanwhile, in Cong Liu's talk, he gave us an introduction on the Data Converter application and design trends.

On March 18, 2019, Guoqiao Tao, presented on "Reliability challenges in (GaN) RF Power Technology" at Xidian University, Xi'an, Shaanxi, China. This lecture was held at the Auditorium in the East Building. More than 100 students from the School of Microelectronics attended.

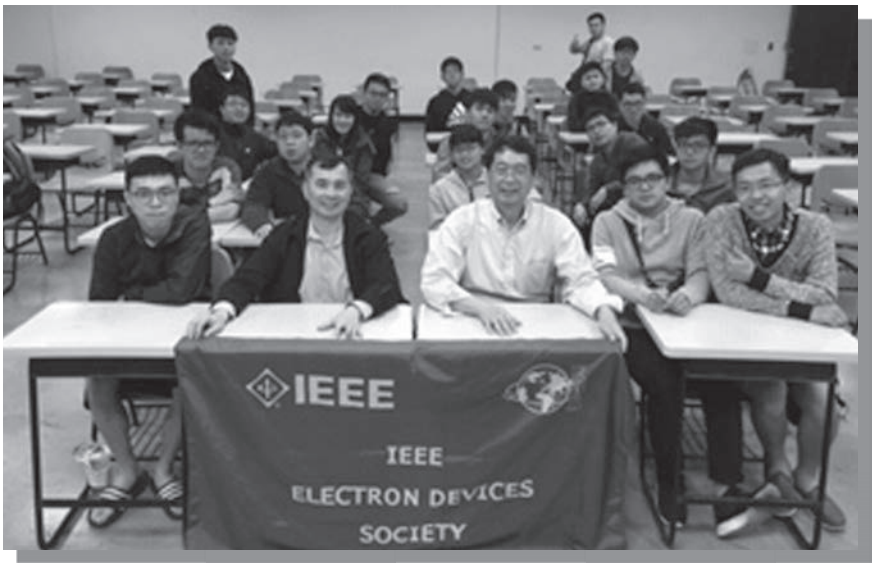
Tao's report was about the industrial reliability requirements, translating system requirements to device requirements, and to requirements per failure mode, acceleration models per failure mode, Front-end (chips) related or package related, scaling up in (industrialized) mass production mode—quality & reliability control.

IEEE EDS Distinguished Lecture at ED Tainan Chapter

—by Wen-Kuan Yeh

The ED Tainan Chapter organized one lecture at Kaohsiung, Taiwan, on March 14, 2019. Dr. Jiann-Shiun Yuan (Professor of Electrical Engineering, University of Central Florida) gave his presentation at National University of Kaohsiung (NUK). His talk, "GaN Power Device Characterization and Reliability Analysis," focused on the design and reliability of GaN devices for related applications. About 40 attendees and several professors of local universities attended.

~Ming Liu, Editor



ED Tainan, DL on March 14th
First row, left second and third: Prof. Wen-Kuan Yeh (Chair of EDS Tainan Chapter), Prof. Jiann-Shiun Yuan (DL Speaker), and some of attendees

ED Malaysia Kuala Lumpur Chapter

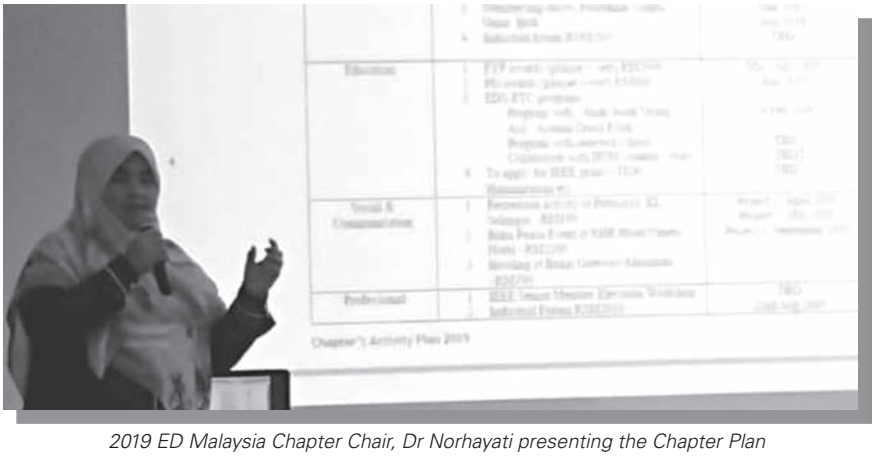
—by S.Noorjannah Ibrahim, Zubaida Yusoff, Rosminazuin Ab Rahim & Aliza Aini

Appreciation Lunch Meeting

An Appreciation Lunch Meeting was held January 17, 2019, at Hotel Bangi-Putrajaya to recognize the efforts and active volunteerism of IEEE EDS Malaysia committee members. During the meeting, the Outstanding IEEE EDS Malaysia Volunteer Award 2018 was presented to Dr Rosminazuin from International Islamic University Malaysia. The Outstanding IEEE EDS Malaysia Student Volunteer Award was presented to Gan Siew Mei from IMEN, UKM. All Excom members of 2018 were presented with appreciation certificates.

EDS Malaysia Outstanding Volunteer Awards 2018

Attendees of the 29th AGM of IEEE EDS Malaysia Chapter



2019 ED Malaysia Chapter Chair, Dr Norhayati presenting the Chapter Plan

EDS Malaysia Annual General Meeting 2019

The 29th Annual General Meeting (AGM) of the EDS Malaysia Chapter was held January 19, 2019, at Dorsett Hotel Putrajaya. The AGM was organized to table EDS events and financial activities in 2018, and was attended by 30 EDS members from all over Malaysia. New executive committees were elected and Prof Dr Norhayati Soin from Universiti Malaya was elected to lead the ED Malaysia Chapter for 2019. The list of new Excom members has been updated on the chapter website at http://ieeemalaysia-eds.org/.

2019 IEEE Malaysia Section Leadership Camp and Chapter Chair Meeting

The 2019 EDS Chair, Prof Dr Norhayati Soin and treasurer, participated in the Leadership Camp and Chapter Chair Meeting of the IEEE Malaysia Section held on March 9th, at Malaysian Global Innovation and Creativity Centre (MaGIC), Cyberjaya. The Camp is an annual gathering for chapter chairs and volunteers to discuss chapter planned activities, budget, and issues to get collective solutions for better management and coordination of IEEE Chapters in Malaysia.

~ P Susthitha Menon, Editor

ED Uttar Pradesh Section, Kanpur Chapter

—by Amit Verma

The ED Kanpur Chapter organized an EDS Distinguished Lecture on February 27, 2019. The lecture was delivered by Dr. Meyya Meyyappan who is the Chief Scientist for Exploration Technology at NASA Ames Research Center, USA. Dr. Meyappan discussed recent work done in his group on fabrication of nanoscale vacuum tubes on 8-inch Si wafers and their characterization. The lecture was attended by over 40 students and faculty members, which included 20 IEEE members.

Dr. Meyya Meyyappan's Distinguished Lecture at IIT Kanpur

Organizers and attendees of Dr. Durga Misra's EDS Distinguished Lecture at NIST, (3rd from right, front row)

ED St. Joseph College of Engineering Student Branch Chapter

—by G. S. Uthayakumar

The chapter conducted the Inter College Symposium at St. Joseph's College of Engineering, where more than 20 college students participated and showed their talents in various events conducted by our students. The IEEE APS and BTS societies conducted a Technical Quiz as a First round, Second round was conducted by the EDS and SP societies, in which a Technical Dub-C was conducted by asking questions related to various trending electronics and communication technologies. The Third round was conducted by the ComSoc and RAS societies.

The Chapter also organized "HACK & TACKLE", a technical quiz competition on February 14, 2019, which was aimed at ameliorating the knowledge of the students.

ED NIST (National Institute of Science & Technology) Student Branch Chapter

—by Ajit Kumar Panda

The Chapter organized a Distinguished Lecture January 10, 2019, at NIST campus on "Research Mobilization and Research Collaboration," by Prof. Durga Misra, NJIT, USA. In the second part, Dr. Mishra addressed the students on IoT Sensor and DL talk on "Reliability of Next Generation Nanoelectronic Devices: From FinFETs to Ge Devices." More than 200 students irrespective of departments attended.

On February 9, 2019, a technical lecture was organized on "ESD Protection and Challenges in Lower Technology Nodes" by Mr. Basudev Dash, Intel-US, USA who has worked in different technology nodes for various design and system level integrations. He discussed the FinFET era and new challenges in 5nm. Thirty students attended his lecture.

The chapter also organized the National Conference on Devices and Circuits (NCDC 2019) on February 3, 2019. Researchers from NIST-Berhampur, KIIT-Bhubaneswar, VSSUT-Burla, Berhampur University, SOA University, and the Institute of Electronics and Radio Physics, West-Bengal participated and presented their work. Twenty-one papers were selected for publication from this one-day event. The presentations were evaluated by the members and two papers one the best paper presentation award jointly: "Sub-threshold Performance Assessment of UTB-OI Negative Capacitance MOS Transistor" by Elina Priyadarshini and Subir Kumar Maity, and "ZnO Incorporated PDMS Pressure Sensor" by A. Choudhury, Parkarsh Kumar, Aditi Dutta, N. K. Mishra and Anshuman.

The chapter organized a technical lecture on "Grid Synchronization Control Schemes" on March 16, 2019, which was delivered by Prof. B. Subudhi, Department of Electrical Engineering, NIT Rourkela. Prof. Subudhi focused on different control schemes and algorithms to improve efficiency. Programmable devices can be adopted for automation with intelligence.

ED Meghnad Saha Institute of Technology Student Branch Chapter

—by Manash Chanda

The ED MSIT Student Branch Chapter and MSIT Student Branch, in association with the Department of ECE, MSIT organized the one-week hands- on-training on PCB designs and IoT based embedded device, January 7–14, 2019. Almost thirty students of the pre final year attended the training. Dr. Sudip Dogra and Dr. Manash Chanda coordinated the session. Out of the thirty students, about twelve were IEEE student members. Attendees learned about PCB designs and embedded language for programming IoT applications.

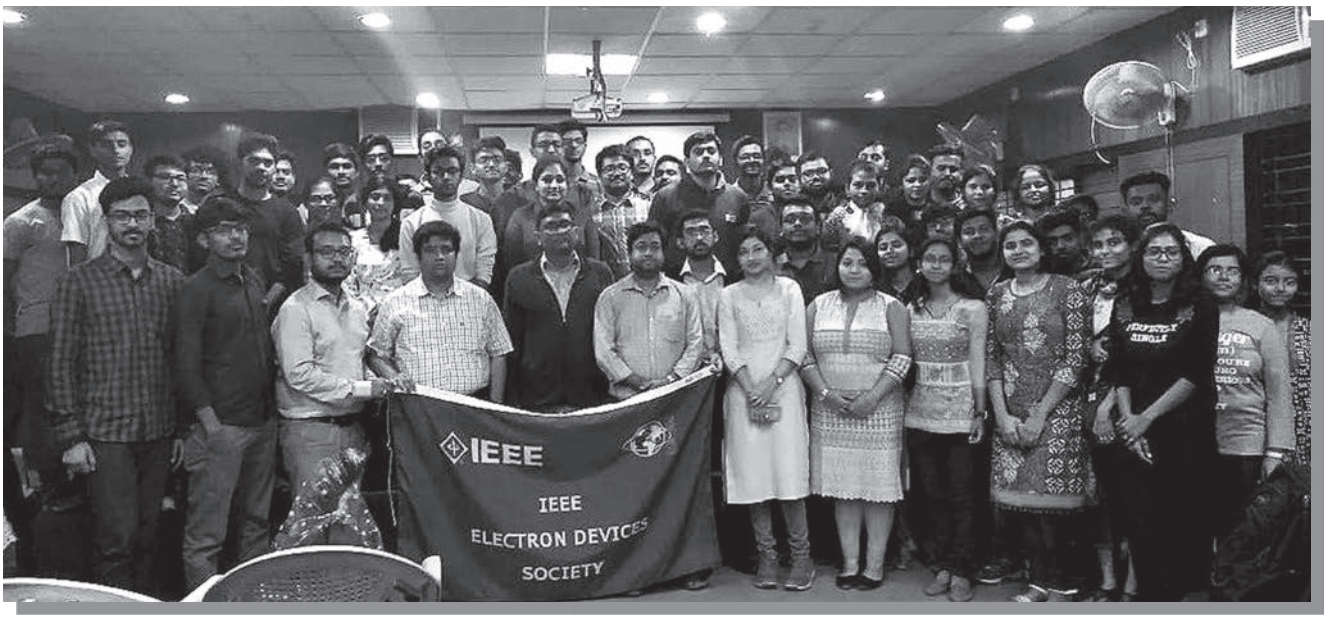
The ED MSIT Student Branch Chapter and MSIT Student Branch, in association with the Department of ECE, MSIT, organized a technical lecture by Dr. Angsuman Sarkar, Associate Professor of the Department of ECE, Kalyani Govt. Engineering College and Chairman, IEEE ED Kolkata Chapter . The lecture was given on February 14, 2019 at the Seminar Hall, MSIT on the topic of "Staggered Hetero Junction TFET." Almost eighty students attended the event, with twenty-four of the student being IEEE members.

The ED MSIT Student Branch Chapter and MSIT Student Branch, in association with the Department of ECE, MSIT, organized a talk by Dr. Subhankar Majumdar, Assistant Professor of the Department of ECE, NIT Meghalaya, on March 14, 2019, on "IoT Devices and Low power Applications." Almost fifty students attended the event, including twenty who were IEEE members.

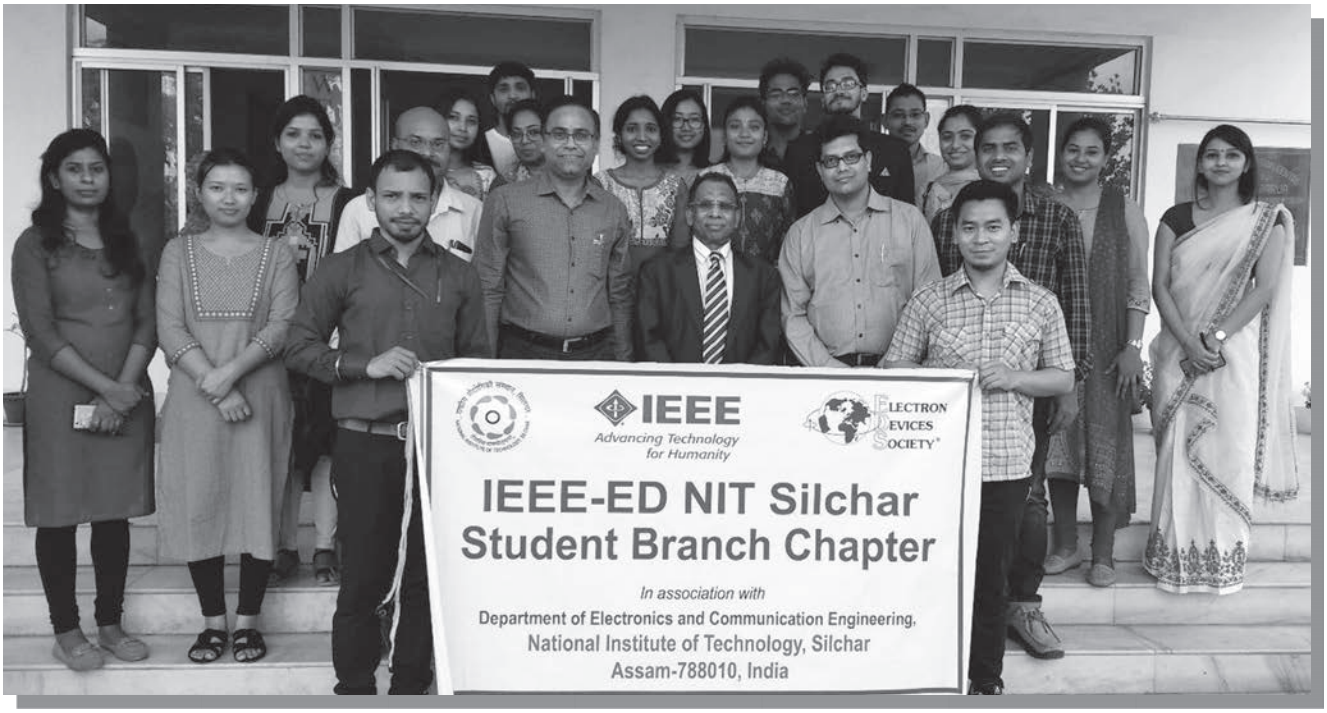
ED National Inst of Technology—Silchar Student Branch Chapter

—by T. R. Lenka

Prof. Samar Saha, EDS Jr. Past-President, visited the ED NIT Silchar Student Branch Chapter during *International Conference on Recent Trends in Electronics and Computer Science (ICRTECS 2019). The conference was held March 18–19*, 2019, at the Department of Electronics and Communication Engineering (ECE), National Institute of Technology Silchar, Assam, India, in collaboration with the ED NIT Silchar Student Branch Chapter. Prof. Saha addressed the audience with an invited talk on Nanoscale CMOS devices and its variability. More than 100 enthusiastic participants comprising of IEEE EDS members, IEEE student



Attendees of technical lecture by Dr. Angsuman Sarkar, organized by ED MSIT Student Branch Chapter and MSIT Student Branch

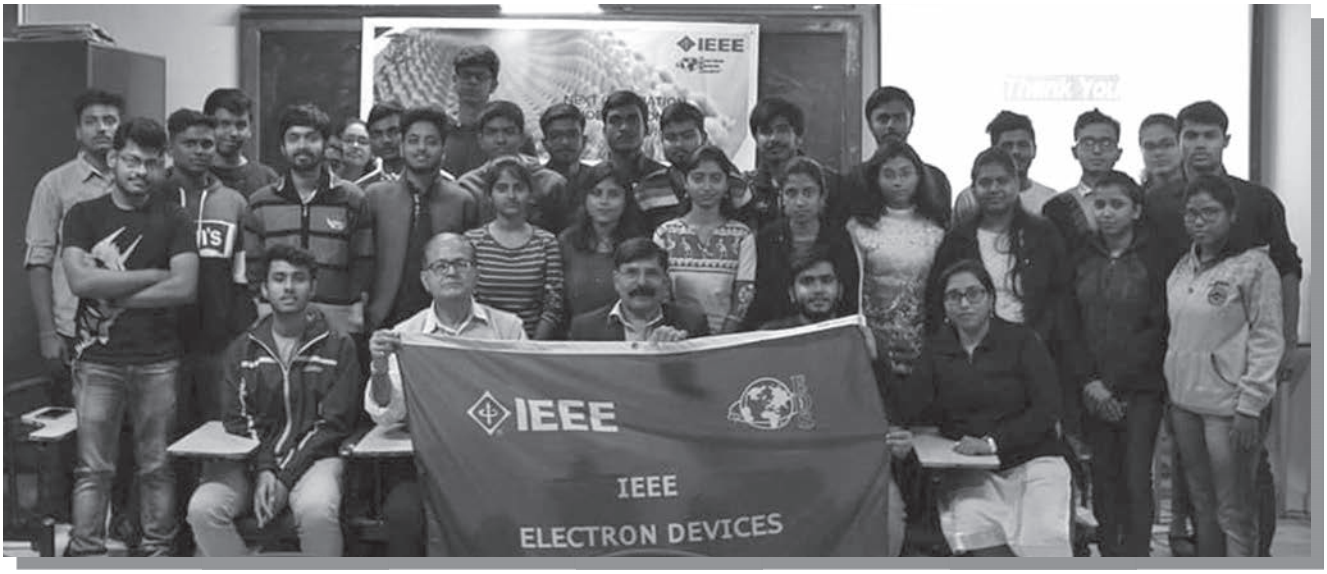


(2nd Left to Right) Aruna Chanu Soibam (Chapter Chair), Dr. S. K. Tripathy (Faculty), Dr. T. R. Lenka (Chapter Advisor), Prof. Samar Saha (Jr. Past President, EDS), Dr. Koushik Guha (Treasurer), Dr. M. Kavi Charan (Faculty)

members, and non-members attended the conference.

ED Netaji Subhash Engineering College Student Branch Chapter
—by Saheli Sarkhel

The ED Netaji Subhash Engineering College Student Branch Chapter in association with the Department of Electronics and Communication Engineering organized an IEEE EDS Distinguished Lecture on "Next Generation Nanoelectronic Devices" on January 12, 2019. Dr. Durga Misra, Professor and Associate Chair for Graduate Studies, Electrical and Computer Engineering Department, New Jersey Institute of Technology (NJIT), USA. Dr. Misra explained different methods to measure the self-heating in FinFETs with an objective to address the reliability issues associated with self-heating problem in downscaled FinFETs. The second part of his talk highlighted the incorporation of high mobility channel materials and high-k



Team ED Netaji Subhash Engineering College Student Branch Chapter with IEEE EDS Distinguished Lecturer, Prof. Durga Misra

gate dielectrics to enhance device performance with special emphasis on the deposition methodologies of such high-k dielectrics without compromising reliability. Almost 35 participants attended the event along with the members of the chapter.

The chapter in association with the Department of Electronics and Communication Engineering organized a one day seminar on "Recent trends in the IT industry and how to motivate oneself to cope with it" on March, 1, 2019, with industry experts Mr. Arka Gayen and Mr. Joyjit Das from Tata Consultancy Services. The lecture session emphasized on some of the advanced technologies trending in IT industry like Cloud computing, Big Data, data mining, AI, Analytics, Automation, etc. Almost 50 participants attended the event and had vivid discussions with the speakers regarding possible prospects in the IT industry.

ED/AP Bombay Chapter DL

Prof. Martinez delivering his talk at Tribhuvan University

ED/AP Bombay Chapter

—by Anil Kottantharayil

The IEEE AP/ED Bombay Chapter organized talks by Dr. Anshuman Singh, National Institute of Standards and Technology, Gaithersburg, USA; Mr. Reet Chaudhuri, third year Ph.D student in Electrical Engineering under Prof. Debdeep Jena and Prof. Huili (Grace) Xing at Cornell University and Dr. S. Subramanian, ARNDIT LLC., Portland, Oregon, USA.

Dr. Anshuman Singh, gave a talk titled "Manipulation of single photons using nanophotonics," which explained single photons that are fundamental constituents of many quantum technologies, encoding and communicating quantum information in various degrees of freedom such as polarization, wavelength, timing, or path and manipulation of the same using nanophotonics.

Mr. Reet Chaudhuri's talk titled, "Towards Complementary Logic in III-Nitrides : Is AlN the answer" presented AlN-substrate platform as an alternative to current technologies and how its material properties gives it an advantage over the conventionally used GaN-substrate based III-nitride devices.

Dr. S. Subramanian, spoke on "Thin Film PiezoMEMS and Microfluidics," giving an overview of PiezoMEMS technology with a focus on microfluidic devices. He also presented some of his own results on the characterization of piezo thin films.

ED Nepal Chapter-Kathmandul

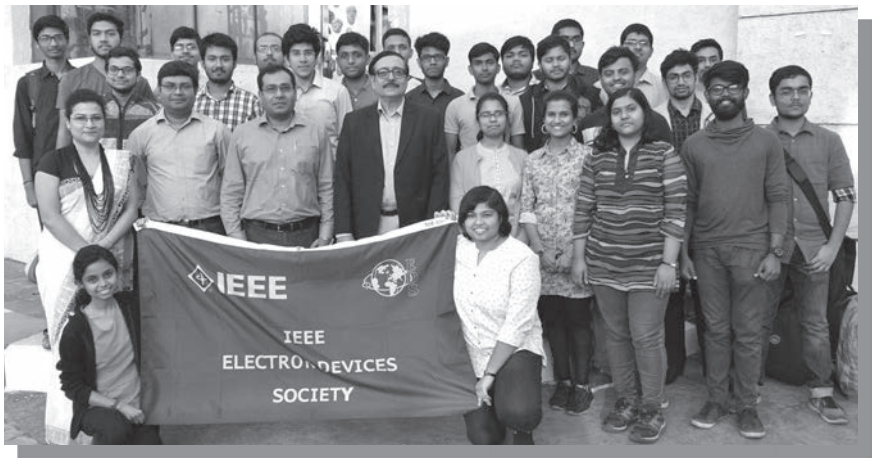
—by Bhadra Prasad Pokharel

The ED Nepal Chapter organized a Distinguished Lecture at Pulchowk Campus, Institute of Engineering, Tribhuvan University, Lalitpur on January 14, 2019. The talk was delivered by Dr. Brajesh Kumar Kaushik, Department of Electronics and Communication Engineering, IIT-Roorkee, Uttarakhand, India, on "Graphene based Interconnect Modelling." The second speaker was Prof. Javier Martinez Technical University of Madrid, Spain, who lectured on "Graphene for Energy applications." Total participants of the program numbered 42, with 15 IEEE members and 27 students and other faculty. The program was partially supported by MSc Materials Science and Engineering Program, Pulchowk Campus, Institute of Engineering, Nepal.

ED Heritage Institute of Technology Student Branch Chapter

—by Atanu Kundu

Dr. Nabarun Bhattacharyya, Senior Director & Centre Head, Centre for Development of Advanced Computing (C-DAC), Kolkata delivered a lecture on 'Sensors for Agriculture and



Participants of the Prof. Sujit Biswas lecture

Environment' at Heritage Institute of Technology on February 8, 2019. The program was attended by 18 participants and was jointly organized by EDS CoE, Heritage Institute of Technology and ED HIT SBC.

Prof. Sujit Biswas, Department of Electrical Engineering, Jadavpur University, Kolkata, delivered a talk on "Practical Problems in High Frequency Applications of Passive Components in Electronics" at IEEE EDS CoE, Heritage Institute of Technology on February 12, 2019, which was attended by 30 participants. The program was organized jointly with EDS CoE, Heritage Institute of Technology and ED HIT SBC.

The IEEE EDS Center of Excellence, Heritage Institute of Technology, hosted a one-day hands-on Autonomous Robotics Workshop 'Lord of the Tracks 3.0' on February 9, 2019. It is the third workshop in the series of Autonomous Robot Design Workshops conducted by nine IEEE EDS student volunteers. The workshop was attended by 24 participants.

Mr. Arijit Majumder, Scientist, Society for Applied Microwave Electronics Engineering and Research (SAMEER), Ministry of Electronics and Information Technology, Government of India, gave a technical lecture on "GaN HEMT—The Holy Grail for Power Amplifier Designers," February 20, 2019.

ED Kalyani Government Engineering College Student Branch Chapter-Kalyani

—by Angsuman Sarkar

The 3rd international conference "2019 Devices for Integrated Circuit (DevIC)," was completed successfully at Kalyani Government Engineering College, March 23–24, 2019. The conference was organized by the IEEE KGEC Student Branch Chapter, in association with Department of ECE, KGEC and technically co-sponsored by the ED Kolkata Chapter. There were keynote lectures/talks, tutorials, and oral presentations by eminent researchers. A total of 150 participants were present at the DevIC 2019 Conference.

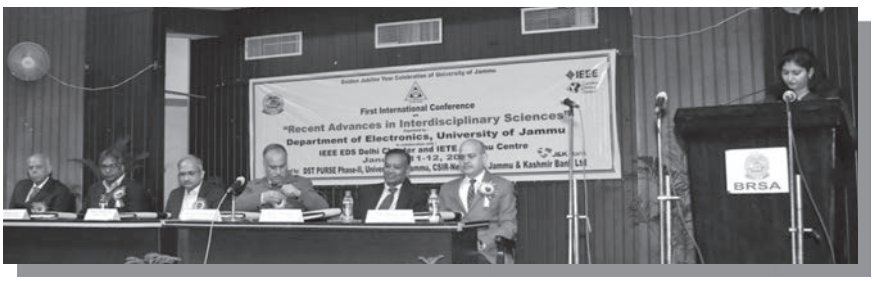
ED Delhi Chapter

—by Mridula Gupta and Sneha Kabra

The First International Conference on "Recent Advances in Interdisciplinary Sciences" was organized by the Department of Electronics, January 11–12, 2019, at the University of Jammu, in collaboration with the ED Delhi Chapter and IETE Jammu centre, and funded by DST PURSE Phase-II, CSIR New Delhi, J&K Bank Ltd.

Prof. V Ramgopal Rao, Director, IIT-Delhi, India, was the Chief Guest of this conference, with guests of honor Dr. Meyya Meyyappan, Chief Scientist for Exploration Technology, National Aeronautics and Space Administration (NASA) Ames Research Center Moffett Field, California, USA; Prof. Vijay K. Arora, Wilkes University, USA and IEEE EDS Distinguished Lecturer, USA; Prof. Ravi

Inauguration of DevIC 2019 at Kalyani Government Engineering College



Inaugural Session of the International Conference on Recent Advances in Interdisciplinary Sciences at Brig. Rajinder Singh auditorium of the University of Jammu

RNDr. Mgr. Jiri Martinu along with organizers and participants of the workshop

Silva-Director, Advanced Technology Institute (ATI) and Head of Nano-Electronics Centre, The University of Surrey, UK

The conference had over 500 participants from within India and other countries, representing various universities, and R&D institutions. There were 4 plenary talks, 20 invited talks, about 80 oral talks, and over 300 poster presentations from various universities, colleges and research institutes from within India and abroad.

The Robotics Club in collaboration with the Department of Instrumentation of Shaheed Rajguru College of Applied Sciences for Women, successfully conducted a three-day Lecture Series on "Artificial Intelligence and Robotics." The lecture series was delivered by RNDr. Mgr. Jiri Martinu, Erasmus Fellow, Department of Informatics and Applied Mathematics, Silesian University Opava, Czech Republic from February 6–8, 2019. The three-day workshop was attended by 107 students and college faculty members of the Department of Instrumentation, Electronics, Computer Science and Physics. The lecture series focused on giving hands-on exposure on "WEBOT", a robot designing platform. Undergraduate Students learned about the latest research going on in the field of artificial intelligence, sensors and actuators and algorithms used in robotics. Participants learned about the applications of Robotics in the field of Outer Space Applications, Intelligent Home Applications, Industry, Health Service, etc.

The Departments of Electronics & Communication Engineering, Amity University, Noida, India, in Collaboration with the ED Delhi Chapter organized the *Sixth International Conference on Signal Processing and Integrated Networks, SPIN 2019* on March 7–8, 2019. More than 500 international and national delegates, scientists and researchers participated in the conference which was devoted to advancements in Signal Processing and Integrated Networks. Researchers from all over the country and abroad gathered in order to introduce their recent advances in the field and thereby promoted the exchange of new ideas, results and techniques. Various technical sessions, panel discussions, Keynote Speeches, oral paper presentations and Special Sessions on Selected Topics were organized during the conference. The two-day conference offered a unique opportunity to gain insight into state-of-the-art technology in the field and to network with international researchers and scientists.

From March 11–12, 2019, a Science Festival was organized under the aegis of DBT Star College Program, Deen Dayal Upadhyaya College, and was financially supported by the ED Delhi Chapter and the National Academy of Science India (NASI) Delhi Chapter. Companies like Jaisbo, SILVACO, Cognitive Design Technologies, AGMATEL, Keysight Technologies, Dewinter, Silicom Electronics Pvt. Ltd., Binary Semantics and i3Indya Technologies, exhibited their products during the science exhibition. On March 11, 2019, the opening remarks were given by Professor Ajoy Ghatak, (NASI) and Chairperson Delhi Chapter .The Inaugural Address was delivered by Professor RK Kohli, Vice-Chancellor, Central University of Punjab, Bathinda and on March 12, 2019, the keynote address was delivered by Dr. Amulya Kumar Panda, Director, National Institute of Immunology.

Eighty-one posters, projects and models, as well as 18 papers were presented by over 180 participants from 25 different institutions across India. Thirty-one teams comprising of 100 students participated in the Science Quiz competition. The Hands-on-Workshop on "Bird Nest making for assisting the conservation of House Sparrow" was also organized during the science fest in which 30 students participated. A film on the life of Great Indian Mathematician 'Srinivasa Ramanujan' was also screened on March 12, 2019. Binary Semantics conducted Faculty Development Program and a Quiz on STEM Education for the audience. Deen Dayal Upadhyaya College won the quiz and got Free Maple Ambassador License. A two-hour interactive Panel Discussion on "Science Communication" was also organized.

~Manoj Saxena, Editor

EDS MEETINGS CALENDAR

THE COMPLETE EDS CALENDAR CAN BE FOUND AT OUR WEB SITE: HTTP://EDS.IEEE.ORG. PLEASE VISIT.

2019 IEEE 26th International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)	02 Jul – 05 Jul 2019	Zhejiang, China
2019 26th International Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD)	02 Jul –05 Jul 2019	Kyoto, Japan
2019 IEEE International Flexible Electronics Technology Conference (IFETC)	11 Aug – 14 Aug 2019	Vancouver, BC Canada
2019 34th Symposium on Microelectronics Technology and Devices (SBMicro)	26 Aug – 30 Aug 2019	Sao Paulo, Brazil
2019 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)	04 Sept – 06 Sept 2019	UDINE, Italy
2019 XXIVth International Seminar/Workshop on Direct and Inverse Problems of Electromagnetic and Acoustic Wave Theory (DIPED)	12 Sept – 14 Sept 2019	Ukraine
2019 IEEE 31st International Conference on Microelectronics (MIEL)	16 Sept – 18 Sept 2019	Nis, Serbia
ESSCIRC 2019 - IEEE 45th European Solid State Circuits Conference (ESSCIRC)	23 Sept – 26 Sept 2019	Cracow, Poland
ESSDERC 2019 - 49th European Solid-State Device Research Conference (ESSDERC)	23 Sept – 26 Sept 2019	Cracow, Poland

2019 8th International Symposium on Next Generation Electronics (ISNE)	09 Oct – 11 Oct 2019	Zhengzhou, China
2019 International Semiconductor Conference (CAS)	09 Oct – 11 Oct 2019	Sinaia, Romania
2019 IEEE International Integrated Reliability Workshop (IIRW)	13 Oct – 17 Oct 2019	South Lake Tahoe, CA
2019 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)	14 Oct – 17 Oct 2019	San Jose, CA, USA
2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)	29 Oct – 31 Oct 2019	NC, USA
2019 IEEE BiCMOS and Compound semiconductor Integrated Circuits and Technology Symposium (BCICTS)	03 Nov – 06 Nov 2019	Nashville, TN USA
2019 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)	04 Nov – 07 Nov 2019	Westminster, CO
2019 IEEE International Electron Devices Meeting (IEDM)	09 Dec – 11 Dec 2019	San Francisco, CA
2019 IEEE 50th Semiconductor Interface Specialists Conference (SISC)	11 Dec – 14 Dec 2019	San Diego, CA
2020 IEEE Electron Devices Technology & Manufacturing Conference (EDTM)	15 Mar – 18 Mar 2020	Malaysia
2020 IEEE International Reliability Physics Symposium (IRPS)	29 Mar – 03 April 2020	TX, USA
2020 IEEE 32nd International Conference on Microelectronic Test Structures (ICMTS)	06 April – 09 April 2020	Edinburgh, United Kingdom
2020 IEEE 21st International Conference on Vacuum Electronics (IVEC)	20 April – 23 April 2020	Monterey, CA USA

EDS Mission Fund – A Call to Members

The Electron Devices Society (EDS), in partnership with the IEEE Foundation, is proud to announce the establishment of the **IEEE Electron Devices Mission Fund of the IEEE Foundation**. As a new endeavor for the society, this fund will be used to greatly enhance the humanitarian, educational, and research initiatives of EDS by providing members and other constituents of the EDS community with the ability to contribute directly to our mission-driven imperatives, such as EDS-ETC Program and EDS Student Fellowship Program.

EDS's mission is to *promote excellence in the field of electron devices for the benefit of humanity*. As a volunteer-led, volunteer-driven society we pride ourselves on doing the utmost to realize this mission. With the establishment of this fund, all EDS members can play a direct role in this vital work.

Membership in EDS is $20 per year for higher level members. Our affordable membership rates are designed to ensure that money is never a barrier to joining EDS. And we're honored to provide all the benefits of membership at this subsidized rate. However, despite a robust operating budget, the revenue collected from dues is not enough to fully support all our wonderful humanitarian efforts.

About the IEEE Foundation

As the philanthropic arm of the IEEE, the IEEE Foundation is a leader in transforming lives through the power of technology and education. The IEEE Foundation enables IEEE programs that enhance technology access, literacy, and education; supports the IEEE professional community; and inspires the generosity of donors. The IEEE Foundation is qualified under U.S. Internal Revenue Code 501(c)(3). Charitable contributions to the IEEE Foundation are tax deductible to the fullest extent allowed by law in the United States. For other countries, please check with your local tax advisors. To learn more, visit www.ieeefoundation.org.

Therefore, to our members who are able to give more than just the cost of membership, especially those who no longer pay dues to be a part of EDS, please consider contributing to the **EDS Mission Fund**.

Donating is simple. Just go to the IEEE Foundation Online-giving page at www.ieee.org/donate, choose your donation amount, and select "**The IEEE Electron Devices Mission Fund**" in the "Designations" pull down menu. If you prefer to write a check, please make it payable to the **IEEE EDS Mission Fund of the IEEE Foundation** and mail it to the IEEE Foundation, 445 Hoes Lane, Piscataway, NJ, 08854, USA. 100% of your donation will be used exclusively for the humanitarian, educational, and research initiatives of EDS.

EDS Vision, Mission and Field of Interest Statements

Vision Statement
Promoting excellence in the field of electron devices for the benefit of humanity.

Mission Statement
To foster professional growth of its members by satisfying their needs for easy access to and exchange of technical information, publishing, education, and technical recognition and enhancing public visibility in the field of Electron Devices.

New EDS Field of Interest Approved by the EDS BOG
The EDS field-of-interest includes all electron and ion based devices, in their classical or quantum states, using environments and materials in their lowest to highest conducting phase, in simple or engineered assembly, interacting with and delivering photo-electronic, electro-magnetic, electromechanical, electro-thermal, and bio-electronic signals. The Society sponsors and reports on education, research, development and manufacturing aspects and is involved in science, theory, engineering, experimentation, simulation, modeling, design, fabrication, interconnection, reliability of such devices and their applications.