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TECHNICAL BRIEFS

THE INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS (IRDS)

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Introduction

The IRDS focuses on producing a roadmap of the fundamental building blocks of the electronics industry spanning from devices to systems and from systems to devices. These are the foundations of the AI-centric social-infrastructure of the IoT that will be connected via high speed network communication as illustrated in Fig. 1. The IRDS offers a 15-year outlook that allows enough time for researchers to study solutions to solve difficult problems looming 10 years ahead and beyond, while offering a series of short-term technological and system options that can come to full fruition within the next 5 to 10 years. Finally, the IRDS closely monitors advancements of the electronics industry in the next coming 5 years to verify that previously reported projections had indeed been consistent with actual technology and system actual implementations adopted in high-volume manufacturing by the electronics and semiconductor industries.

The 2020 IRDS predicts that many fundamental changes will occur in the next 15 years. For instance, as device scaling reaches fundamental limits around the year 2030, Moore's Law will continue to hold by stacking multiple layers of transistors in the vertical dimension and by means of new innovative architectures. *Will eventually quantum technology and algorithms allow increasing functionality per unit area to continue by allowing multiple bits to physically coexist?*

1. Roadmap Methodology Background

The IRDS is the third generation of the roadmap methodology firstly empirically outlined by Gordon Moore as far back as 1965 (1).

(continued on page 3)

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NEWSLETTER DEADLINES

ISSUE	DUE DATE
October	July 1st
January	October 1st
April	January 1st
July	April 1st

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THE INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS (IRDS)

(continued from page 1)

At that time he predicted that the number of transistors that could be integrated in a single die (i.e., in an integrated circuit, (IC)) will double every year for the subsequent 10 years. His prediction turned out to be correct and in 1975 he revised his prediction to a doubling of transistors every 2 years for the foreseeable future (2). He also identified three fundamental contributors to achieving these results: IC architecture, miniaturization of components and the ability to produce increasingly larger dice at low cost due to high manufacturing yields. Around that time Robert Dennard published

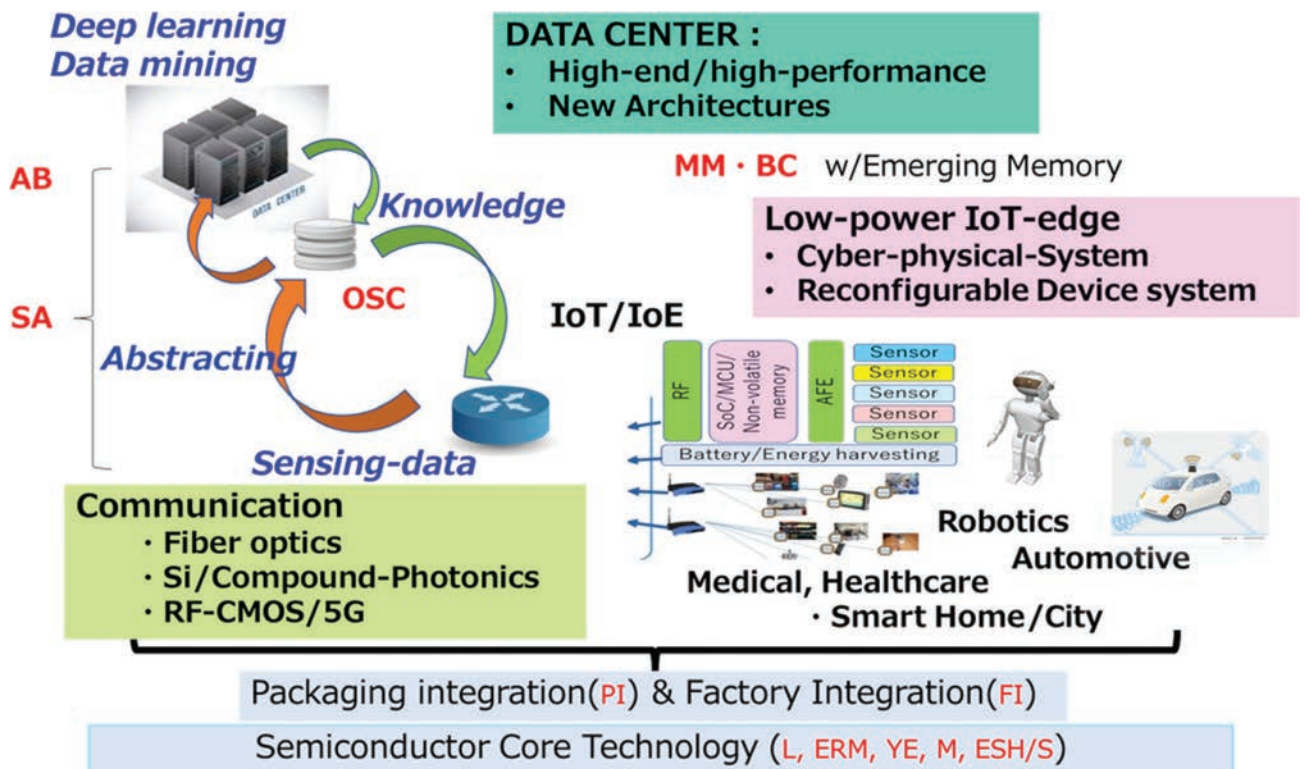
a set of rules on how to easily predict performance of scaled down transistors (3). The semiconductor industry diligently followed these guidelines for the subsequent 15 years.

Dennard methodology held true until about 2005. Conversely, Moore's Law still holds true to this day and it is anticipated that will continue to be valid for at least the next 10 years.

In 1991 universities, industry and government organizations in the US got together and decided to formalize in a comprehensive document the details of future trends governing the future of the semiconductor and electronics indus-

tries with a 15-year outlook. The question of this exercise was: "How long will Moore's Law continue to be applicable?" For this purpose 11 Technology Working Groups (TWGs) were formed. The National Technology Roadmap for Semiconductors (NTRS) was published in 1992, 1994 and 1997, respectively.

By 1996 it became clear that major roadblocks were going to be encountered by the beginning of the next decade; for instance, the thickness of the gate dielectric would have been nullified by 2005 at the latest. Solving these problems required a full re-engineering of the transistor structure



AB: Applications Benchmark, **SA:** Systems and Architecture, **OSC:** Outside System Connectivity, **BC:** Beyond CMOS, **PI:** Packaging Integration, **FI:** Factory Integration, **L:** Lithography, **M:** Metrology, **ERM:** Emerging Research Materials, **YE:** Yield Enhancement, **ESH/S:** Environment, Safety & Health and Sustainability

Fig. 1. IRDS provides the building blocks of the future IoT society

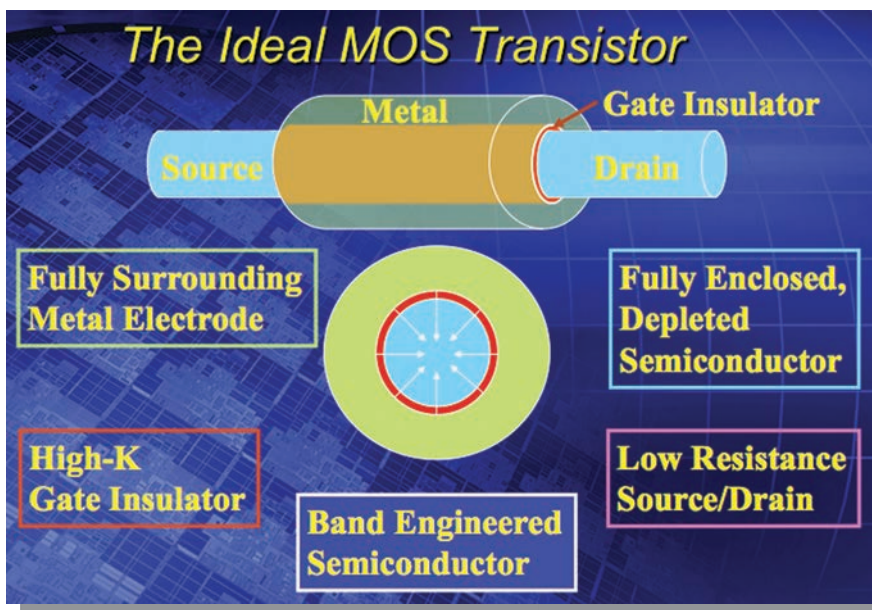


Fig. 2. 1998ITRS proposed transistor structure

in a way that had been done before. This was no longer a US-only problem; it affected the entire semiconductor industry and electronics industries around the world.

To efficiently tackle this problem, the International Technology Roadmap for Semiconductors (ITRS) was formed in 1998 with participation of organizations from Europe, Japan, Korea, Taiwan and the US. An aggressive and revolutionary program to completely overhaul how transistors are structured and manufactured was outlined (Fig. 2).

Extensive cooperation of universities, suppliers, multiple governments' funded programs and consortia around the world led to the systematic introduction in rapid succession of strained silicon, high-k/metal-gate, FinFET in manufacturing. This effort was completed by 2011 and saved the semiconductor and the electronics industry.

2. The Continuously Evolving Supply Chain

The introduction of the personal computer (PC) in the 80s revolutionized the semiconductor industry. Until then semiconductor manufacturers had sold their products to cor-

porations that integrated different semiconductor products into unique systems (e.g., mainframe computers), that were sold or leased to other corporations. However, the diffusion of the PC quickly reached the consumer market and the advent of the Internet further popularized the adoption of notebooks as communication devices. However, consumers continually have different requirements—most of all they want new and exciting products on an almost monthly schedule never experienced before by the semiconductor industry. The combination of Intel, as the integrated device manufacturer (IDM) and Microsoft, as the almost exclusive software provider arose to the task and was able to respond to this escalating demand. Additionally, Intel dominated the PC market leaving the role of the system integrators to mere receivers of software and technology with limited choices on how to integrate the PC or notebook (e.g., screen size, amount of memory, etc.).

The introduction of the iPhone in 2007 and the introduction of the iPad in 2010 revolutionized the supply chain model even further. Apple demonstrated that system integra-

tors could design their own products, design their own chips and have them successfully manufactured by a foundry.

In the PC-era Intel and Microsoft controlled the pace of the electronics market, in the smart phone-era the system integrators (in association with foundries) had finally regained the driver seat position controlling the growth of the electronics industry.

3. From ITRS to IRDS

In the 2013 ITRS it was anticipated that some fundamental dimensional and architectural limits were going to be reached in the not too distant future, first by memory products and then by logic products as well. In essence, increasing transistor density by making them smaller was going to become too expensive for memory manufactures due to escalating lithography costs. On the other hand, logic circuits were becoming too crowded to simultaneously accommodate for higher functional density and reduced power dissipation.

The 2013 ITRS recommendation consisted in aggressively utilizing the vertical dimension to increase the number of transistors packed per unit area (Fig. 3). Flash memory manufacturers were fast to respond to this recommendation and by 2015 new Flash products stacking tens of layers of memory cells were announced; forecasts of adding hundreds of layers as time went by were projected also. This vertical approach to increasing transistor density has become today's reality as Flash memory products with more than 100 layers have been reported for imminent introduction.

Furthermore, by 2012 it had become clear that requirements formulated by system integrators were solidly controlling designs of new semiconductor circuits. New capabilities were constantly required to be added to new custom ICs driven by consumers' needs. As a response, the ITRS number of TWGs and

roadmap chapters had grown to 17. To evolve in synchronicity with the new ecosystem the roadmap evolved and transitioned in 2014 into an interim structure under the name of "ITRS 2.0." With this transformation the TWGs were integrated into clusters accordingly to the level of interdependence of their activities. In addition, new clusters covering subjects not considered before were formed under the new terminology of International Focus Teams (IFTs).

In the new methodology, system requirements percolated down into IC requirements and IC innovations quickly escalated up to create new options for system integrators. This transformation was completed by late 2015 and published under the name of "2015 ITRS 2.0."

With this transformation completed the new broader mission of the roadmap going forward was sealed under a new name: International Roadmap of Devices and Systems (IRDS). The International Roadmap Committee (IRC) is composed of representatives from the European Academic and Scientific Association for NanoElectronics (SiNANO), the System and Device Roadmap of Japan (SDRJ), the IEEE Electron Devices Society (EDS), and from the IEEE Computer Society (CS).

During this transformational period, the structure of the electronics industry and the semiconductor industry had completely changed. Faced with increasing costs of research, design and manufacturing multiple companies decided to give up on manufacturing leading-edge digital semiconductors to concentrate all their resources on IC designs and, in limited cases, to still produce specialty semiconductors. Nowadays the system integrators–foundry model increasingly has replaced the IDM-system integrators model of the past decades. Under these conditions it became evident that the IRDS had evolved far beyond the initial world of semiconductors and needed to move to a much broader orga-

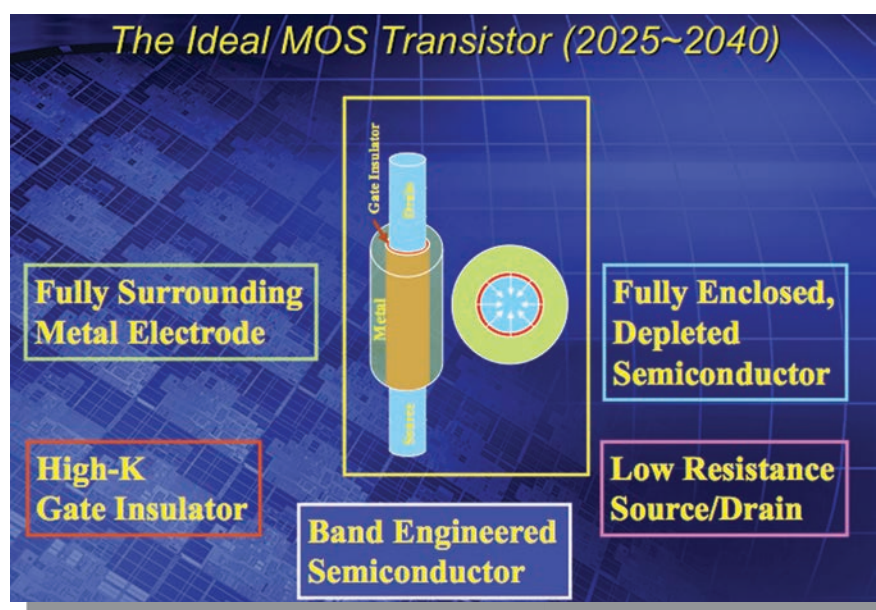


Fig. 3. 2013ITRS proposed vertical transistor evolution

nization. In May 2016, IEEE adopted the IRDS under the umbrella of the Rebooting Computing Initiative (RCI) as the two organizations were serendipity complementing each other.

The System device roadmap committees of Japan (SDRJ) supported by the Japan Society of Applied Physics (JSAP), and the European SiNANO institute have been actively participating in the IRDS from 2017 and 2018 respectively.

The international organizations from Japan and EU have been contributing to the IEEE IRDS™ by jointly addressing technical topics and directions making it a true international effort. Monthly international webinars are regularly held to exchange regional information and recommendations on technical and management subjects.

4. IRDS Structure: The IFTs

1. Applications Benchmarking (AB)

The mission of the Applications Benchmarking (AB) IFT in the IRDS is to update and identify key application drivers, and to track and roadmap the performance of these applications for the next 15 years. The output of the AB market drivers in

conjunction with the drivers of the Systems and Architectures (SA) IFT, generates a cross-matrix map showing which application(s) are important or critical (gating) for each market.

2. Systems and Architecture (SA) The mission of the System Architecture (SA) chapter in the IRDS is to establish a top-down, system-driven 15-year roadmapping framework for key market drivers of the semiconductor industry. The SA chapter is proposing roadmaps of relevant system metrics for mobile applications, datacenter, IoT, and cyber-physical systems (CPS).
3. Outside system Connectivity (OSC)

The mission of the OSC IFT in the IRDS consists in identifying and assessing capabilities needed to connect most elements of the Internet of Everything (IoE) and highlight technology needs and gaps. This includes supporting interconnection of a broad range of sensors, devices, and products to support information communication, processing and analysis for many applications including

automobiles, aerospace, and a wide range of IoT applications for personal use, home, transportation, factory, and warehouse. Communication of data over fiber optic circuits to data centers and fiber optic communication within data centers is in scope for this chapter.

4. More Moore (MM)

The More Moore (MM) IFT of the IRDS provides physical, electrical and reliability requirements for logic and memory technologies to sustain More Moore (Power, performance, area, cost (PPAC) scaling for big data, mobility, and cloud (IoT and server) applications and forecasted logic and memory technologies (15 years) in main-stream/high-volume manufacturing (HVM). The 2013 ITRS already anticipated that fundamental limits of 2D scaling were going to be reached for all product lines between 2015 and 2021.

Already 72–96 layers of Flash memory cells have been demonstrated in manufacturing. It is anticipated that logic technologies will transition to 3D approaches in the next few years. These technological solutions will assure continuation of Moore's Law for additional 10–15 years.

5. Beyond CMOS (BC)

The goal of the Beyond CMOS (BC) IFT of the IRDS is to survey, assess, and catalog viable new information processing devices and system architectures due to their relevance on technological choices. It is also important to identify the scientific/technological challenges gating their acceptance by the semiconductor industry as having acceptable risk for further development. Another goal is to pursue long-term alternative solutions to technologies addressed in More-than-Moore (MtM) entries.

6. Cryogenics Electronics and Quantum Information Processing (CE&QIP)

The goal of this chapter for the IRDS is to survey, catalog, and assess the status of technologies in the areas of cryogenic electronics and quantum information processing. Application drivers are identified for sufficiently developed technologies and application needs are mapped as a function of time against projected capabilities to identify challenges requiring research and development effort. Cryogenic electronics (also referred to as low-temperature electronics or cold electronics) is defined by operation at cryogenic temperatures (below -150°C or 123.15 K) and includes devices and circuits made from a variety of materials including insulators, conductors, semiconductors, superconductors, or topological materials. Existing and emerging applications are driving development of novel cryogenic electronic technologies.

Quantum information processing is different in that it uses qubits, two-state quantum-mechanical systems that can be in coherent superpositions of both states at the same time, which can have computational advantages. Measurement of a qubit causes it to collapse to either one state or the other.

7. Packaging Integration (PI)

The Packaging Integration (PI) focus of the IRDS is divided between the near-term assembly and packaging roadmap requirements and the introduction of many new requirements and potential solutions to meet market needs in the longer term. Packaging integration is the final manufacturing process transforming semiconductor devices into

functional products for the end user. Packaging provides electrical connections for signal transmission, power input, and voltage control. It also provides solutions for thermal dissipation and the physical protection required for reliability. Heterogeneous integration of multiple technologies has become a dominant factor in the past 10 years enabling a variety of new products, especially in the mobile category.

8. Factory Integration (FI)

The Factory Integration (FI) focus area is dedicated to ensuring that the semiconductor-manufacturing infrastructure contains the necessary components to produce items at affordable cost and high volume. Realizing the potential of Moore's Law requires taking full advantage of device feature size reductions, new materials, yield improvement to near 100%, wafer size increases, and other manufacturing productivity improvements. This in turn requires a factory system that can fully integrate additional factory components and utilize these components collectively to deliver items that meet specifications determined by other IRDS focus areas as well as cost, volume, and yield targets.

9. Lithography (L)

The Lithography (L) focus area of patterning technology has been high-performance logic chips, DRAM memory, and Flash memory. High performance logic chips are now the drivers for better resolution features, Extreme Ultraviolet Lithography (EUVL) is now being implemented into manufacturing for leading edge logic due to the benefits it offers in reducing development cycle and manufacturing cycle times, decreasing the numbers

of patterning levels and reducing overall complexity. DRAM memory is trailing high performance logic in critical dimensions and in using EUVL. Flash memory has switched from scaling horizontally to stacking vertically and its patterning challenges relate to cost and to finding processes that reduce process steps.

10. Yield Enhancement (YE)

The Yield Enhancement (YE) focus area is dedicated to activities ensuring that semiconductor manufacturing is optimized for production of the maximum number of functional units. Identifying, reducing, and avoiding relevant defects and contamination that can adversely affect and reduce overall product output are necessary to accomplish this goal. Yield in most industries has been defined as the number of functional and sealable products made divided by the number of products that can be potentially made. In the semiconductor industry, yield is represented by the functionality and reliability of integrated circuits produced on the wafer surfaces. During the manufacturing of ICs yield loss is caused, for example, by defects, faults, process variations, and design. The Yield chapter of the IRDS presents the current advanced and next generation future requirements for high-yielding manufacturing of More Moore as well as More than Moore products.

11. Metrology (M)

The Metrology Chapter (M) of the IRDS identifies emerging measurement challenges from devices, systems, and integration in the semiconductor industry and describes research and development pathways for overcoming them. Metrology Chapter focused on reviewing and updating references. This

includes, but is not limited to, measurement needs for extending CMOS, beyond CMOS technologies, novel communication devices, sensors and transducers, materials characterization and structure/function relationships. This also includes metrology required in research and development, and techniques providing process control in manufacturing, yield, and failure analysis.

12. Environment, Safety, Health, and Sustainability (ESH/S)

The Environmental, Safety, Health, and Sustainability (ESH/S) chapter of the IRDS serves to provide a long-range framework and process for all key stakeholders in the semiconductor and microelectronics industry, to develop proactive technical solutions to address critical ESH/S challenges up front, without gating industry R&D, mitigating cost, ensuring business continuity, and identifying key new markets and opportunities.

13. More Than Moore (MtM)

The More than Moore chapter of the 2020 IRDS is devoted to the incorporation into smart electronic systems of non-digital functionalities that do not necessarily scale according to Moore's Law. These new functionalities provide additional value in the field of sensors, actuators, or power management. This functional diversification allows a number of systems to more efficiently interact with each other and also offer new ways to communicate with the outside world while minimizing energy consumption by powering the nano-systems with "free" energy harvesting.

5. Planning for the next 15 years with the IRDS

Several events are predicted by the 2020 IRDS that could lead to a yet

new ecosystem of the electronics industry in the third decade of this century. However, the transition will not happen very smoothly or *even at all* unless action is taken immediately. The warning given by the 2020 IRDS is meant to stimulate initiation of programs in a timely manner. A few of these transition points stand out:

Most of All, Scaling Will Reach Its Limits in the Second Half of This Decade

Feature scaling has substantially contributed to increasing the number of transistors per die in accordance with Moore's Law (1,2) since the beginning of the IC industry. Imaging of features of smaller dimensions to increase transistor density and performance has been accomplished for the past 50 years utilizing light of progressively smaller wavelength and lenses of higher numerical apertures. During this time, the exposure wavelength of lithographic equipment evolved from 436 nm to 193 nm, yielding a reduction of device features from the 10-micron range in the 1970s to tens of nanometers nowadays.

EUV imaging technology (13.5 nm) has been introduced into manufacturing in the past couple of years, after more than 20 years in development. The NA of the present equipment is 0.33 and the ultimate exposure tool with NA better than 0.5 will be introduced by 2023. The downside is that according to all experts no new cost-effective imaging technology will be available in the future. It is expected that features around 7–8 nm will be in manufacturing somewhat before 2030 but no additional feature reductions are anticipated beyond that (Fig. 4).

Fear not, the game is not over! All Flash memory manufacturers are aggressively using the vertical dimension of ICs to increase the number of transistors per unit area. Logic device manufacture will follow later in the decade. Innovative architecture will

Reconnecting with NTRS/ITRS Technology Nodes (1/2 of metal pitch)

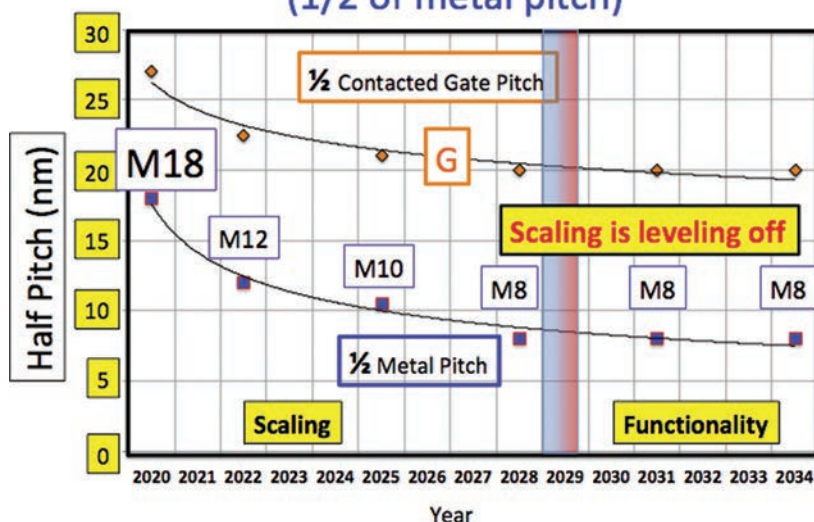


Fig. 4. 2020IRDS Preparing for scaling leveling off

continue to increase functionality. As AI technologies and architectures continue to advance in combination with leading-edge ultra-low-power semiconductor technologies, it will be possible to realize AI-equipped-cyber-physical systems to be deployed

in the IoT-edge systems; eventually some of these applications will be “attached” on/in our bodies for medication and healthcare. Furthermore, a variety of quantum computing and information technologies are fighting to replace scaling—promising innova-

tive avenues to increase functionality. The adoption of multiple bits per component will open up the 4th dimension to increasing functionality without requirements for reducing feature size.

Read all the details of the IRDS in the currently on line issues 2016, 2017 and 2018 and the latest 2020 IRDS at the following address <https://irds.ieee.org/editions> and in the multiple articles coming up on this publication in the following months.

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HIGHLIGHTS OF THE 4TH IEEE ELECTRON DEVICES TECHNOLOGY AND MANUFACTURING EDTM VIRTUAL CONFERENCE, 2020

The 4th IEEE Electron Devices Technology and Manufacturing (EDTM) virtual conference was held from April 6 to April 21, 2020. The EDTM 2020 virtual conference was the 1st of its kind EDS-sponsored conference and has been a learning experience for the conference organizers, and participating authors, plenary speakers, sponsors & exhibitors, and attendees.

The EDTM 2020 was planned as a full three-day event at the *Hotel Equatorial*, Penang, Malaysia from March 16 to 18, 2020. However, as the health and wellbeing of all concerned

became a huge threat due to the COVID-19 pandemic, the organizing committee by calling an emergency meeting decided to hold the conference as a *virtual event* with the help of the IEEE Meetings, Conferences & Events (MCE) *Digital Events Team*. In this virtual event, all PowerPoint presentations with narrations/voice were prepared as MP4 videos and uploaded on the EDTM 2020 Digital Platform (ON24) created and maintained by the IEEE MCE Digital Events Team. The EDTM 2020 virtual conference went live on April 6 at 9:00 AM (Malaysia Time, MYT) and closed on

April 21, 3:00 PM (MYT). Thus, the attendees of 27 participating countries from different time zones had 24/7 access to the EDTM 2020 Digital Platform for over two weeks and listen to the presentations at any time from any part of the world on mobile or any other computing device.

The EDTM 2020 virtual event featured a technical program of 182 papers by the very best expert and young scientists and engineers in the field of electron devices technology and manufacturing from 27 different countries worldwide; six Plenary Talks by internationally recognized technical

leaders from the industry and academia spread over three scheduled days of the conference; and *four* local (Penang) high school student Posters; as well as presentations from 13 sponsors and one exhibitor. *The EDTM 2020 prepared to offer four Tutorials and three Short Courses by the highly accomplished Instructors on Sunday, March 15, 2020; however, these pre-conference academic programs as well as the conference social events were cancelled for the convenience of this 1st EDS virtual conference.*

Three Plenary Talks in Day 1 of the program were:

- “The Forever Exponential? Moore’s Law: Past, Present and Future,” by Kaizad Mistry, Corporate Vice President, Intel Corporation.
- “Semiconductor Nanowires for Optoelectronics Applications,” by Chennupati Jagadish, Professor, the Australian National University, Canberra, Australia.
- “Rapid Yield Improvement Using Intelligent Data Mining,” by Vivek Jain, Senior Vice President, Maxim Integrated.

Next, two Plenary Talks in Day 2 of the program were:

- Critical Feature Size of Device Manufacturing for Dominating MOSFET Evolutions, by Digh Hisamoto, Research & Development, Hitachi, Ltd.
- “Research Toward Monolithic Three-Dimensional ICs,” by

Lance Li, Director, Corporate Research, Taiwan Semiconductor Manufacturing Company (TSMC). And, the Day 3 Plenary Talk was:

- “Nanocarbon Interconnects—from 1D to 3D,” by Cary Y. Yang, Professor, Santa Clara University.

The conference technical program was organized into a total of 32 sessions with multiple parallel and focused sessions featuring papers on the emerging areas of the electron devices technology and manufacturing for systems integration from 10 technical subcommittees:

- Materials;
- Process and Tools for Manufacturing;
- Devices and Smart Systems for Internet of Things (IoT);
- Smart Power and Renewable Energy Devices;
- Modeling and Simulation;
- Reliability;
- Packaging and Heterogeneous Integration;
- Manufacturing Yield;
- Emerging Photonics, Bio-photonics, Optoelectronics Technologies, and Novel Photovoltaic Devices;
- Artificial Intelligence (AI) and Machine Learning;

Each session included contributed and invited papers on cutting-edge device and manufacturing technology (<https://ewh.ieee.org/conf/edtm/2020/virtual/sessions.html>). In this brief review, no attempt is made to summarize these papers. The following

basic trends are observed from the presented papers at the EDTM 2020 virtual conference.

A large number of presentations were on materials for manufacturing showing a huge R&D effort in this area. The papers include nanotechnology materials for manufacturing; materials for novel devices; 2D-materials and devices; materials processing; and 2.5D/3D integration.

The papers on device technology included presentations from all major areas including planar and non-planar MOSFETs devices and CMOS technology; sensors and inductors; emerging memory devices; RF devices; emerging photovoltaic devices and detectors; power devices including GaN and III-V, and SiC devices, emerging memory devices; and flexible electronics devices and wearables. The numerical simulation and device modeling included a large number of theoretical research papers on emerging devices in the search for post-CMOS alternative devices.

There has been a number of excellent papers on manufacturing and device characterization as well as packaging and heterogeneous integration. Also, excellent research papers on artificial intelligence and machine learning were presented in EDTM 2020 virtual conference.

Samar Saha
Prospicient Devices, USA
EDTM 2020 Co-General Chair



IEEE-Branded Virtual Backgrounds for Video Conferencing Tools

IEEE has created IEEE-branded virtual backgrounds for video conferencing tools like Zoom and Microsoft Team. [Visit the page](#) to download the images and view instructions on how to upload the background images for meetings.

UPCOMING TECHNICAL MEETINGS



IEEE INTERNATIONAL ELECTRON DEVICES MEETING TO BE HELD VIRTUALLY

Special focus sessions will be held on the following topics:

- Technologies Enabling 5G and Beyond
- Future Interconnect Technology
- Advanced IC Design and Integration in Wide-Bandgap Technologies
- Device Technologies for Cryogenic Electronics
- Energy Harvesting and Wireless Power Transmission
- Next Generation Design-Technology Co-Optimization (DTCO)

PISCATAWAY, NJ—Under the theme “Innovative Devices for a Better Future,” the 66th annual IEEE International Electron Devices Meeting (IEDM) will take place December 12–16, 2020 as a virtual conference, given the ongoing uncertainties posed by the prevailing COVID-19 pandemic. A mix of live and recorded sessions will be used to showcase and discuss the world’s best original work in all areas of microelectronics research and development.

IEDM 2020 has issued a Call for Papers seeking the world’s best original work in all areas of microelectronics research and development.

The paper submission deadline is Friday, August 28, 2020. Authors

are asked to submit four-page camera-ready papers. Accepted papers will be published as-is in the proceedings. A few late-news papers also will be accepted, covering only the most recent and noteworthy developments. The late-news submission deadline is Friday, October 2, 2020.

The IEDM is the premier forum for technological breakthroughs in semiconductor and electron device technology, manufacturing, design, physics and modeling. Each year, the world’s leading technologists gather to participate in a technical program of more than 220 presentations, plus panels, focus sessions, tutorials, Short Courses, supplier exhibits, IEEE/EDS award presentations and other events highlighting the industry’s best work.

“Last year’s IEDM conference was a great success, with about 1,900 attendees, the most in more than a decade, and the highest participation ever in our tutorials and short courses. No matter where you turned something exciting was happening, whether it was a greatly anticipated late-news paper on 5nm technology; thought-provoking plenary talks; the popular quantum computing infrastructure focus session and Saturday tutorials; or the many papers on novel 3D and memory technologies, just to name a few,” said Dina Triyoso, IEDM 2020 Publicity Chair and Technologist at TEL Technology Center, America, LLC. “This year, the IEDM Executive Committee has decided that in the interest of prioritizing the health and safety of the scientific community,



Linda Somerville, VP, Micro Technology, speaking at the IEDM career luncheon.

a virtual approach is the best option," she said.

"Transistors and other electron devices are the building blocks of electronic systems which are used in a greater number of applications, to solve a wider variety of problems, than ever before," said Meng-Fan (Marvin) Chang, IEEE Fellow and Distinguished Professor of Electrical Engineering at National Tsing Hua University. "Helping to make this possible are the state-of-the-art results that will be presented at IEDM, and the opportunity to interact with colleagues from academia and industry around the world."

IEDM 2020 encourages submissions in all areas, with special emphasis on:

- Neuromorphic computing/AI
- Quantum computing devices
- Devices for RF, 5G, THz and mmWave
- Advanced memory technologies
- Technologies for advanced logic nodes
- Non-charge-based devices and systems
- Advanced power devices, modules and systems
- Sensors, MEMS and bioelectronics
- Package-device level interactions
- Electron device simulation and modeling
- Robustness/security of electronic circuits and systems
- Optoelectronics, displays and imaging systems
- Power Devices and Systems (PDS)
- Reliability of Systems and Devices (RSD)
- Sensors, MEMS and Bioelectronics (SMB)

Further information

For more information, visit the IEDM 2020 home page at www.ieee-iedm.org.

Follow IEDM via social media

- Twitter: www.ieee-iedm.org/twitter
- LinkedIn: www.ieee-iedm.org/linkedin
- Facebook: www.ieee-iedm.org/facebook

The IEDM technical subcommittees are as follows:

- Advanced Logic Technology (ALT)
- Emerging Device and Compute Technology (EDT)
- Memory Technology (MT)
- Microwave, Millimeter Wave and Analog Technology (MAT)
- Modeling and Simulation (MS)
- Optoelectronics, Displays and Imagers (ODI)

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2020 IEEE INTERNATIONAL INTEGRATED RELIABILITY WORKSHOP (IIRW)



CHANGED TO A VIRTUAL EVENT

The 2020 IEEE International Integrated Reliability Workshop (IIRW), sponsored by the IEEE Electron Devices Society and the IEEE Reliability Society, will be held at the Stanford Sierra Conference Center on the shores of Fallen Leaf Lake near South Lake Tahoe, California, October 4–8, 2020. This workshop provides a unique forum for open, lively discussions of all areas of semiconductor device and materials reliability in an intimate setting.

The workshop will include such semiconductor reliability topics as: emerging memory technologies, Fin-FET on bulk and SOI, high- k and nitrided SiO_2 gate dielectrics, the reliability assessment of novel devices, power devices and wideband gap material reliability, organic electronics, transistor reliability including hot carriers and NBTI/PBTI, MOL and BEOL interconnects and low- k dielectrics. The conference will also cover product reliability, the impact of transistor degradation on circuit reliability, reliability modeling and simulation, optoelectronics, single event upsets, array testing and others. Special focus this year will be on thermal stress and self-heating effects, power and wide-bandgap device reliability, and defect-driven high volume manufacturing reliability impacts.

Located 6400 feet above sea level in the California Sierra Nevada, the Stanford Sierra Conference Center provides an ideal atmosphere for a relaxing and

informative technical workshop. All aspects of the workshop, including the remote location and absence of typical distractions encourages extensive interaction among the workshop attendees. IIRW participants are drawn into technical discussions from the start; and the format of the technical program, engages attendees with high quality content and time for enjoyment of the natural surroundings.

The conference traditionally begins Sunday evening after the majority of attendees arrive. The Sunday night talk, designed for the weary traveler, is a presentation on an interesting topic either peripherally related to reliability, or simply an interesting hobby or business from one of the attendees.

Over the previous 2 years, the IIRW “Reliability Experts Forum” has become an integral part of the conference. This forum brings reliability experts to one platform leading to very invigorating discussions. This year, the forum will be focus on the current Back End of Line and Middle of Line (BEOL & MOL) reliability physics and reliability related challenges. The event is expected to have participation from experts as panelists and researchers as participants. It aims to have discussion on Electromigration, stress-migration, and the oxide integrity of MOL and BEOL dielectrics, such as Kristoff Croes (*imec*), Lado Filipovic (TU Vienna), and JR Lloyd (SUNY Polytechnic).

IIRW also provides several moderated discussion groups held in the evenings, followed up with multiple Special Interest Groups. These groups are composed of small groups of attendees who want to continue their discussions on a particular topic of interest, which often continue even after the workshop.

One unique aspect of the workshop is the opportunity for any attendee to present a walk-in poster of their latest work. Finally, attendees have Wednesday afternoon off to enjoy a variety of outdoor activities such as hiking, volleyball, sailing or kayaking, biking, walking, or simply continuing that intriguing conversation from the night before. This free afternoon is a great way to not only network, but also to build long-lasting friendships.

Additional information about the workshop is available on the IIRW website at www.iirw.org, or by contacting Stanislav Tyaginov, 2020 IIRW General Chair, (gc.iirw@gmail.com). Information on the Stanford Camp is available at stanfordsierra.org.

On behalf of the 2020 IIRW Management Committee, I look forward to meeting you at the Stanford Sierra Camp on Fallen Leaf Lake in October 2020.

*Matt Ring
2020 IIRW TPC Chair
tpc.iirw@gmail.com
ON Semiconductor
S. Portland, ME*

MID-YEAR BOARD OF GOVERNORS MEETING—2020



*MK Radhakrishnan
EDS Secretary*

First time in the history of EDS, a Board of Governors meeting had to be organized virtually due to the COVID19 pandemic worldwide. Earlier plan to have the BoG meeting in Sydney, Australia during the first weekend of June 2020 had to be cancelled. Instead, a very successful virtual BoG meeting was organized on June 7, 2020, using Cisco WebEx with the support of EDS office staff. As a virtual meeting, the schedule was limited to three hours from 9:00–12:00 US Eastern Time, but incorporating all the presentations as usual. The meeting was attended by almost all elected members of the BoG and EDS Forum members joining online from countries far and wide at different time zones.

EDS President, Meyya Meyyapan welcomed the online attendees and informed that the meeting would have presentations by all the VPs and others scheduled in the agenda, but limited to 10 minutes each. The Q&A was managed by RaviTodi, President-Elect, with questions and comments sent to him directly by email. All the motions were presented with the voting to take place via email after the meeting. All the presentations were made available through the EDS BoG Agenda link in advance, which allowed everyone to go through the presentations prior to the meeting. Highlights of the presentations and deliberations include the following.

Bin Zhao, EDSTreasurer, presented the financial status, reporting a surplus of \$1214K in 2019, 50% of which can be utilized for new initiatives. The

budget for 2020 has been revised due to the pandemic situation. Both revenue and expenses have been revised with a substantial reduction in conferences related activities. EDS planned 17 financially sponsored conferences in 2020 along with technical co-sponsorship of 75-80 other conferences, as reported by the VP of Meetings, Kazunari Izhimaru. Out of the financially sponsored conferences, 3 have been cancelled and 8 go virtual due to the pandemic impact. Five others are now being planned as scheduled during the later half of the year and one has been postponed. First virtual conference of EDS was EDTM 2020 in Malaysia in April, which was a great success through all virtual presentations.

Educational activities ramped up this year with many new initiatives as reported by Navakanta Bhat, VP of Education. EDS summer school request for 2020 had excellent response with 11 proposals, out of which one was selected. Enhanced emphasis on the EDS webinars and one webinar each every two weeks addressing the latest trends in technology is in progress. EDS certification program is a new initiative with a combination of many programs providing opportunities for professional development while allowing participants acquire online credits leading to IEEE certificates. Also, building a strong industry base for Chapters and broadening the base targeting the students of all allied disciplines with a motto of “catch them young” was discussed.

Joachim Burghartz, VP Publications & Products informed that all EDS journals (TED, EDL and JEDS) are growing in the number of papers submitted. The acceptance rate remains as that of previous years with EDL

20% as the lowest. The acceptance rate for EDS co-sponsored journals is on the average 40–50%. The processing time is improving for all journals with 3.9 weeks for EDL from submission to e-publication. The 2019 revenue has increased for both EDL and TED. Special issues/Sections for selected conference papers of LAEDEC and ESSDERC has been planned.

Murty Polavarapu, VP Regions and Chapters, reported that EDS has 211 chapters at present with 6 new chapters in Region 9. The chapter activity reporting has to be streamlined through Vtools only. All the Chapter subsidy requests received for 2020 have been disbursed. Due to travel restrictions resulting from the pandemic, the DL visits have been suspended for a while along with MQ plans. However, the DL activity is ongoing through online DL talks using different media platforms, which now can benefit not only the arranging Chapter, but also members everywhere. Such a very successful set of DLs recently organized by the EDS Delhi Chapter can be a model for all the global chapters. Improving chapter vitality and re-energizing under-performing student Chapters are the priority for 2020.

EDS membership growth trends for recent years was presented by Patrick Fay, VP for Membership. The overall membership has been decreasing for the last two decades in every Region, except Region 9 and 10. A continuous reduction is observed in Regions 1–6, whereas the growth is fluctuating in Region 8 with a current downward trend. EDS growth may depend on increase in the value proposition for non-academics and young professionals.

John Dallesasse, VP for Technical Committees, presented the summary

of activities for the 14 TCs in EDS. The mission of the TCs is to promote the technical and related activities in the specific areas for the professional growth of members. Some of these are in close collaboration with Education, Conferences and Regions and Chapters. Promoting activities like TC-sponsored Mini Colloquia and supporting Webinars through TC member involvement are being planned. Also, contributions to conferences, journals and Newsletter are in the pipeline.

Paul Berger, VP Strategic Directions, presented a plan for EDS growth through membership development in view of a vision for the future. Engaging sister societies and utilizing resources for collaborative activity for updating products and services to support the multidisciplinary and dynamic nature of emerging technology are in the pipeline. Meyya Meyyappan requested the VP and his strategic team to focus on future visions for EDS, 20 years and beyond, considering what EDS and its members would be engaged in for professional activities, new technical areas, job prospects and related matters.

Young Professionals committee activities were presented by Camilo Velez, Committee Chair. The committee has 15 members from around the globe engaged in organizing YP events in conferences like LAEDC and IEDM 2019. EDS has a strong presence in social media platforms—Facebook, Twitter and LinkedIn. YP is developing Twitter and LinkedIn as main channels to increase brand awareness and engagement.

Fernando Guarin, EDS Awards/Nominations and Elections Chair informed the status of awards and nominations including the 2020 BoG election. As EDS Humanitarian Activities Chair, Fernando explained various activities including those organized in conjunction with EDS conferences like LAEDC and projects like smart drip irrigation, embedded water quality sensors and solar powered desalinization. EDS collaboration with IEEE SIGHT is progressing with projects in Nicaragua.

Samar Saha, EDS Fellow Committee Chair, reported that 31 nominations were received this year and the review was organized by virtual meeting of the committee. EDS Newsletter Status Report and Development plan

was presented by MK Radhakrishnan, Newsletter Oversight Committee Chair. The development plans by Newsletter EiC, Daniel Tomaszewski, includes preparation of guidelines for contents, enhance YP and WIE news and contents in every issue of Newsletter and social media promotion of the key articles.

As planned earlier, the motions were circulated via email to all Forum members, all of which are now approved. These motions include—approval of December 2019 BoG meeting minutes, June 2020 appointments, 2021 publication prices and page budgets, Membership dues for 2021, Changes in the Region 9 Awards committee and the location for 2021 mid-year Governors meeting.

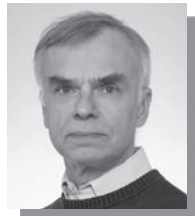
The 2021 mid-year BoG meeting is planned to be in Sydney, Australia on May 29–30, 2021.

The first ever virtual meeting was concluded on time. Meyya Meyyappan thanked all the participants and attendees around the globe, and adjourned the mid-year BoG meeting.

*MK Radhakrishnan
EDS Secretary*

A MESSAGE FROM EDITOR-IN-CHIEF

Dear Readers, Members of the IEEE EDS Community,



*Daniel Tomaszewski
Editor-in-Chief, EDS
Newsletter*

Welcome to the July 2020 issue of the EDS Newsletter.

We all are aware of today's unstable and difficult situation in the World, which suffers from the COVID-19 pandemic. Many people have been touched by diseases triggered by SARS-CoV-2 virus. We share the sorrow of the pandemic victim's relatives. Medical services heavily struggle against the pandemic.

They are supported by researchers who try to develop virus vaccines, and engineers who design and manufacture equipment for medical care. We do hope that their efforts will appear successful in the near future. We also hope that the pandemic and struggle against it will enhance efforts of humans, organizations and societies towards protecting the World and its resources, towards more sustainable human activity.

The pandemic dramatically affects economics, business and social relations worldwide. Services, industry are pushed into emergency operations, see e.g. a case of ON Semi-

conductor (evertiq.com/news/48085). Also universities, schools, societies have suspended or postponed operations. It is also a case of the IEEE Electron Devices Society. A program of EDS Distinguished Lectures has been temporarily suspended. Numerous conferences, technical and organizational meetings have been cancelled, postponed, or transferred into virtual mode. For the Society it is a difficult situation. However, a lot of efforts are made to cope with it. The Newsletter Editorial team also tries to mitigate effects of the pandemic and provide you with news from the Society. However, we are not always able to inform

you in advance about recent updates of the upcoming events. As mentioned in the April 2020 Issue, reach out the event websites, please. Thank you.

We hope that you will find many items of interest in the issue.

Following the past issues of the Newsletter we continue a Technical Briefs series. It is our great pleasure to welcome Dr. Paolo Gargini, who introduces a series of articles inspired by the International Roadmap for Devices and Systems (IRDS™) reports. We believe that articles presenting the future of electronic devices in a popular form may not only be of interest to you, but may also increase your expertise. Do not hesitate to share with us your comments, please. Apart from this series we will be inviting other experts to contribute to the Technical Briefs series as well.

We are very glad to publish messages from the Vice-Presidents of the Membership and Technical Committees. It is our mission to provide a platform for communication between the

Standing and Technical Committees and EDS readers. The message from the VP of the Technical Committees is accompanied by a message from the Chair of the Compound Semiconductor Devices & Circuits Committee. We hope to welcome Chairs of other Technical Committees and have their messages in the next Newsletter issues.

The Regional and Chapter News Sections contain reports from the Chapters in Asia and Europe. We should make efforts to increase visibility of other Chapters as well. A map of the Chapter activities should be more uniform. It will depend both on the Chapters and on the Newsletter Regional Editors.

The Young Professionals section is well represented thanks to our Colleagues from the chapters in India and Germany, who shared with us encouraging messages illustrating a positive effect of the EDS membership on their activities as professionals and volunteers.

As you can easily notice, the Newsletter Editorial Team suffers from

vacancies at the Regional Editor positions for Regions 5 & 6—Southwestern & Western USA and Region 8—United Kingdom, Middle East & Africa. Due to this we cannot provide you with information about the Society activities in those regions. I dare to say, vacancies always hinder operation of the master bodies, including semiconductors and editorial teams. Therefore, one of the most urgent tasks for us is to fill these gaps. For this we will closely cooperate with the Newsletter Oversight Committee and Board of Governors.

Please, send us your feedback, recommendations, comments regarding the Newsletter contents. We, Joyce (j.lombardini@ieee.org) and me (dtomasz@ite.waw.pl) are looking forward to hearing from you.

Stay safe and healthy in this unstable, difficult time. If possible, have a restful vacation time too.

*Sincerely,
Daniel Tomaszewski*

OBITUARY OF DR. RICHARD L. ANDERSON



Richard L. Anderson, IEEE Life Fellow, died on May 30, 2020. He was known for his early work on heterojunctions. His model for the band

alignment based upon the experimentally measured electron affinities of the contributing semiconductors, known as the Anderson's rule, had a large impact on development of generations of heterojunction devices.

Richard Anderson was born in Minneapolis, Minnesota in February 1927. At age 4 he moved (with his family) to a farm north of Milaca, MN. He at-

tended a one-room school for grades one through eight, and then he went to high school in the town of Milaca. When he turned 17 years of age, he enlisted in the U. S. Navy. During World War II he served aboard the aircraft carrier U. S. S. Shangri-La in the Pacific theater. The Shangri-La was referred to as the Tokyo Express since its planes were the first to bomb Tokyo. After the war, the Shangri-La was involved in the two atomic bomb tests at Bikini Atoll in the Marshall Islands. (While three tests were originally scheduled, the third was cancelled because the radiation from the first two tests was too intense for the available measuring equipment.)

Upon returning to the United States, he spent several months in a Naval Hospital and received a medical discharge in 1947. He then attended the University of Minnesota where in 1951 he met and married Claire Petersen. He received a BS and an MS in Electrical Engineering from the University of Minnesota. He then worked on semiconductor research at the IBM Research Laboratory in Poughkeepsie, New York. While there, he earned his Ph.D. in materials science at Syracuse University. The dissertation contained basics of the Anderson's rule mentioned above. In 1960, he received a Fulbright-Hays teaching Fellowship in the Physics

Department at the University of Madrid. After returning from Spain, he was employed as a Professor of Electrical Engineering at Syracuse University from 1961 to 1978. During his time at Syracuse University, he spent two years of sabbatical leave at the Escola Polytechnica of the University of São Paulo, Brazil, where he was instrumental in establishing a semiconductor laboratory. In 1978, he accepted a position as Professor of

Electrical Engineering and Materials Science at the University of Vermont. From 1981 to 1991, he was chairman of the Program in Materials Science.

During his professional career, he lectured extensively in Europe and South America. He consulted for the United Nations, the Organization of American States, the Brazilian National Science Foundation, the Council for Informatics in Campinas, Brazil, the US State Department, the U. S. National

Science Foundation, and the Ministries of Education in Ecuador and Colombia, as well as several US companies. In 1970, he was awarded a Fellow in the Institute for Electrical and Electronics Engineers, and an honorary doctorate from the University of São Paulo. He is survived by his wife, two children, and six grandchildren.

Daniel Tomaszewski
EDS Newsletter Editor-in-Chief

EDS VICE PRESIDENT OF MEMBERSHIP AND SERVICES REPORT



Patrick Fay
EDS Vice President
of Membership and
Services

I am extremely grateful for the opportunity to serve you, my fellow members of the Electron Devices Society, as the incoming vice-president of membership and services. EDS exists to serve our members, and the role of the membership committee is first and foremost to ensure that we are responsive to your needs and desires for the society's growth and evolution. EDS is a robust and active technical society, with more than 10,000 members. The common thread that binds us together is that we are united by a shared interest in, and appreciation

of, electronic devices. Our membership ranges from undergraduate students to senior faculty, researchers in academic and cutting-edge industrial settings, practicing engineers and management in production settings, and beyond. This breadth and depth of collective experience and expertise is a genuine strength of EDS.

Since our goal as a society is to serve you, our members, please let me or other members of the membership committee know if you have thoughts or ideas that would improve the value of the society for you. EDS is very active in providing high-quality publication venues (including Electron Device Letters, Transactions on Electron Devices, the Journal of the Electron Devices Society, Transactions on Semiconductor Manufacturing, the

Journal of Microelectromechanical Systems, Transactions on Device and Materials Reliability, and the Journal of Photovoltaics), as well as premier electron-device focused technical conferences, educational opportunities such as the distinguished lecture series and webinars, and outreach and service opportunities. The membership committee is in the process of developing plans to further enhance the value of membership in EDS; toward that end, we very much value any suggestions you have. The current membership committee consists of Shuji Ikeda, Benjamin Iniguez, Carmen Lilley, Durga Misra, Angele H. M. E. Reinders, and Bin Zhao. I hope you will pass along your thoughts or suggestions directly to me or to any of us on the committee.

HIGHLIGHTING THE COMPOUND SEMICONDUCTOR DEVICES AND CIRCUITS TECHNICAL COMMITTEE

By *PATRICK FAY AND JOHN DALLESASSE*

The EDS Technical Committees serve the IEEE EDS community by helping to coordinate the creation of relevant and timely technical material in a variety of technical areas. The chairs and members of these committees are dedicated individuals who donate their time and talent to ensure continued vibrancy of the society. The technical areas and the associate technical committee chairs are Compact Modeling (Benjamin Iniguez), Compound Semiconductor Devices & Circuits (Patrick Fay), Device Reliability Physics (Souvik Mahapatra), Electronic Materials (Muhammad Mustafa Hussain), Flexible Electronics and Displays (Ta-Ya Chu), Microelectromechanical Systems (Sumant Sood), Nanotechnology (Mario Lanza), Optoelectronic Devices (Can Bayram), Photovoltaic Devices (Juzer Vasi), Power Devices and ICs (WaiTung Ng), Semiconductor Manufacturing (William Nehrer), Technology Computer Aided Design (Geert Eneman), Vacuum Electronics (Claudio Paoloni), and VLSI Technology and Circuits (Hitoshi Wakabayashi). The members of these committees work with the Editor-in-Chiefs of journals to create review papers and special issues, help to coordinate webinars on emerging topics, help to coordinate mini-colloquia, and work with conference organizers when appropriate to provide guidance and content. As an example of the type of work done by these committees, an update from Professor Patrick Fay, chair of the Compound Semiconductor Devices and Circuits Technical Committee, is provided below.

It has been a productive year for the Compound Semiconductor Devices and Circuits Technical Committee, one made possible by the significant efforts of the committee members. We are extremely grateful to have such a dedicated and active group of volunteers on the committee. With members from industry and academia, and hailing from all over the globe, the committee has been very active this year in supporting initiatives intended to serve the EDS membership with interests in the compound semiconductor area.

One major activity has been the preparation of a special section in IEEE Transactions on Electron Devices. With a planned publication date of October 2020, this special section will focus on wide band gap semiconductors and devices for power control and conversion applications. This special section was formed recognizing that electronics for power control and conversion is going through a renaissance, with new device concepts, extensions of known concepts to new materials, and new applications all emerging simultaneously. Fundamental materials-level work in alpha and beta-Ga₂O₃, diamond, Al(Ga) N-channel devices, boron nitride, and other wide band gap materials have begun to produce device results commensurate with the fundamental advantages that these material promise for power control and conversion applications. With potential applications from automotive, data center power management, grid control, industrial and locomotive traction

control, and beyond, these emerging materials have tremendous promise, but yet also require much more research. The role of intrinsic and extrinsic defects in these materials and their impact on device performance, optimal strategies for device design and fabrication, surface passivation and dielectric materials suitable for the high electric fields supported by these materials, device structures and concepts for achieving the best possible electrical performance, appropriate approaches to thermal management, and the potential and challenges of integration of these devices with other semiconductors for system implementation are all areas in which rapid progress is being made; this special issue promises to capture the state of the art from leading researchers worldwide and make it available to the community through our society's flagship journal.

Another subcommittee activity has been to prepare for the inaugural Lester F. Eastman Award. Formed to recognize individuals that have made outstanding contributions to high-performance semiconductor devices, Prof. Eastman was one of the world leaders in the physics and technology of compound semiconductor materials and devices. His group at Cornell made many key contributions to the field of compound semiconductor materials and devices, and he was a long-term member of the compound semiconductor technical community. We look forward to honoring his legacy through this award.

2020 IEEE EDS WILLIAM R. CHERRY AWARD WINNER



Professor James Sites, professor of physics at Colorado State University, has been named the 2020 William R. Cherry

Award winner in recognition of his many and outstanding contributions to photovoltaic science and technology.

James Sites is a Professor of Physics at Colorado State University. He began his photovoltaics career 45 years ago with cells made by ion-beam sputtering of indium–tin–oxide onto silicon. Since then, he has primarily focused on the device physics of polycrystalline thin-film solar cells, particularly CIGS and CdTe, that are compatible with cost-effective manufacturing. His goals have been to quantitatively separate the various solar-cell loss mechanisms, to explain

the details of the mechanisms, and to suggest strategies for improved performance. In recent years he has collaborated closely with Prof. W.S. Sampath on the fabrication, characterization, and analysis of high-efficiency CdTe cells.

Prof. Sites has always enjoyed working closely with students at all levels. Several generations of his students have helped him build a comprehensive PV measurement lab, and together they have developed a variety of analytical and simulation techniques. Thirty of his students have now completed their PhD degree, over forty their MS, and many of them have continued with active roles in the photovoltaics community.

Over time, Prof. Sites has assumed an increasing leadership role with thin-film solar-cell research, and he collaborates closely with several com-

panies and other universities in the U.S. and abroad. He has had a particular focus on increasing the collaboration among the different groups working on CdTe at the device level, which has led to several productive joint projects and a series of annual workshops.

Prof. Sites was an undergraduate at Duke and a graduate student at Cornell, where he built the first dilution refrigerator in the U.S. and then cooled ^3He to millikelvin temperatures by compressing the liquid to solid. As a postdoc at Los Alamos, he continued with low temperatures to magnetically align nuclei to measure their gamma-ray distributions. Since joining the Colorado State faculty, however, he has focused on semiconductor physics with the bulk of his work for many years in photovoltaics.

*Eli Yablonovitch
2020 Cherry Award Chair*

CALL FOR NOMINATIONS—EDS BOARD OF GOVERNORS



*Fernando Guarin
EDS Nominations &
Elections Chair*

The IEEE Electron Devices Society invites nominations for election to its Board of Governors—BoG (formerly AdCom) members-at-large. The next election will be held after the BoG meeting

on Sunday, December 13, 2020. This year, eight out of the twenty-two members will be elected for a 3-year term, with a maximum of two terms.

According to the two related motions passed at the mid-year BoG

meeting held in Kochi, India, on May 21, a member can only serve for a maximum of two terms as a BoG member in a life time and the pilot program for one of the BoG Member-at-Large seats to be elected via the entire EDS membership will be discontinued going forward. Therefore, the eligibility will be verified for all nominees who will be voted on by the EDS BoG. All electees begin their term in office on January 1, 2021. The nominees need not be present to run for the election.

Any EDS member who has served for a minimum of one year as an EDS Officer, Vice-President, Standing & Technical Committee Chair/Member,

Publication Editor and Chapter Chair is eligible to be nominated, unless otherwise precluded from doing so in the EDS Constitution and Bylaws. The electees are required to attend at least one BoG meeting every year. While the December meeting is organized in conjunction with the IEEE International Electron Devices Meeting, the mid-year meeting is frequently held outside the US. Partial travel support is available to attend BoG meetings.

All nominees must be endorsed by one BoG member, i.e., one of the four officers (President, President-Elect, Treasurer or Secretary), the Jr. or Sr. Past President or one of the 22

current BoG Members-at-Large. It is the responsibility of the nominators and the endorsers to make sure that, if elected, the nominee is willing to actively serve in the position as a BoG member-at-large.

Please submit your EDS BoG nomination by October 15, 2020, using the

online nomination form at: (<https://ieeeforms.wufoo.com/forms/k4vnyad0ys3o4z/>).

Also, all endorsements letters should be submitted using the online form: <https://ieeeforms.wufoo.com/forms/q1d5l2jz1pps20g/> by October 15, 2020.

If you have any questions, please feel free to contact Laura Riello (l.riello@ieee.org) with a copy to me at samar@ieee.org.

*Fernando Guarin
Chair of EDS Nominations
& Elections*

EDS BOARD OF GOVERNORS (BoG) MEMBERS-AT-LARGE ELECTION PROCESS

The Member-at-Large (MAL) of the EDS Board of Governors (BoG) are elected for staggered 3-year terms. The 1993 Constitution and Bylaws changes mandated increasing the number of elected MAL from 18 to 22, and required that there be at least two members from each of the following geographic areas: Regions 1–7 and 9; Region 8; and Region 10. In 2003, EDS made changes to its Constitution and Bylaws to require that at least one elected BoG member is a Young Professional (YP—formerly Gold member). A Young Professional member is defined by IEEE as a member who graduated with his/her first professional degree within the last fifteen years. It is also required that there are at least 1.5 candidates for each opening. On May 20, 2017, the BoG approved to set a life time limit of two terms for a volunteer to serve as a BoG Member-at-Large, which must be considered for nominations. The EDS BoG also approved to discon-

tinue the pilot program for one of the BoG Member-at-Large seats to be elected via the entire EDS membership. Accordingly, all nominees will be voted on by the EDS BoG in its meeting in December, 2020. All electees begin their term in office on January 1, 2021. The nominees need not be present to run for the election. In 2020, eight positions will be filled.

The election procedure begins with the announcement of Call for Nominations in the *EDS Newsletter*. The slate of nominees is developed by the EDS Nominations & Elections Committee. Nominees are asked to submit a two-page biographical resume and an optional 50 word personal statement in a standard format.

Any EDS member who has served for a minimum of one year as an EDS Officer, Vice-President, Standing & Technical Committee Chair/Member, Publication Editor & Chapter Chair is eligible to be nominated,

unless otherwise precluded from doing so in the EDS Bylaws. All nominees must be endorsed by one BoG member, i.e., one of the four officers (President, President-Elect, Treasurer or Secretary), the Jr. or Sr. Past President or one of the 22 current BoG MAL. Self-nomination is allowed. Endorsers should submit their online endorsement form by the deadline. Please note that there is no limit to the number of candidates that a full voting BoG member can endorse.

The deadline for Nominations will be October 15, 2020. The biographical resumes and endorsement letters will be distributed to the BoG prior to the December BoG meeting. The election will be held after the conclusion of the BoG meeting on December 13, 2020.

*Fernando Guarin
Chair EDS of Nominations
& Elections*

IEEE ANNUAL ELECTION

This is a reminder for EDS members to vote in the 2020 IEEE Annual Election for the following positions and candidates. Listed below are the positions and candidates that will appear on the 2020 IEEE Annual Election ballot.

The order of candidate names has been pre-determined by lottery, and indicates no preference.



Position	Candidate
IEEE President-Elect, 2021	<ul style="list-style-type: none"> • K. J. Ray Liu (Nominated by IEEE Board of Directors) • Saifur Rahman (Nominated by Petition) • S. K. Ramesh (Nominated by IEEE Board of Directors)
IEEE Division Delegate-Elect/Director-Elect, 2021 IEEE Division I	<ul style="list-style-type: none"> • Rakesh Kumar (Nominated by IEEE Division I) • Franco Maloberti (Nominated by IEEE Division I) • Samar K. Saha (Nominated by Petition)
IEEE Region Delegate-Elect/Director-Elect, 2021-2022	
Region 2 (Eastern USA)	<ul style="list-style-type: none"> • Andrew D. Lowery (Nominated by IEEE Region 2) • Philip M. Gonski (Nominated by IEEE Region 2)
Region 4 (Central USA)	<ul style="list-style-type: none"> • Tarek Lahdhiri (Nominated by IEEE Region 4) • Vickie A. Ozburn (Nominated by IEEE Region 4)
Region 6 (Western USA)	<ul style="list-style-type: none"> • Kathy Hayashi (Nominated by IEEE Region 6) • Scott M. Tamashiro (Nominated by IEEE Region 6) • Chris R. Gunning (Nominated by IEEE Region 6)
Region 8 (Africa, Europe, Middle East)	<ul style="list-style-type: none"> • Igor Kuzle (Nominated by IEEE Region 8) • Vincenzo Piuri (Nominated by IEEE Region 8)
Region 10 (Asia and Pacific)	<ul style="list-style-type: none"> • Supavadee Aramvith (Nominated by IEEE Region 10) • Chun Che "Lance" Fung (Nominated by IEEE Region 10) • Norliza M. Noor (Nominated by IEEE Region 10) • Celia Shahnaz (Nominated by Petition)
IEEE Standards Association Board of Governors Member-at-Large, 2021-2022	<ul style="list-style-type: none"> • Stephen D. Dukes (Nominated by IEEE-SA) • Mehmet Ulema (Nominated by IEEE-SA)
Position 1:	<ul style="list-style-type: none"> • Haiying Lu (Nominated by IEEE-SA) • Subhas Chandra Mondal (Nominated by IEEE-SA)
Position 2:	<ul style="list-style-type: none"> • Bruno Meyer (nominated by IEEE Technical Activities) • F. D. "Don" Tan (nominated by IEEE Technical Activities)
IEEE Technical Activities Vice President-Elect, 2021 IEEE-USA President-Elect, 2021	<ul style="list-style-type: none"> • Deborah M. Cooper (Nominated by IEEE-USA) • Keith A. Moore (Nominated by IEEE-USA)

Balloting period starts on 17 August 2020 and ends at 12:00 PM, Eastern Time USA (16:00 UTC) on 1 October 2020. All eligible voting members can access their ballot electronically at www.ieee.org/elections. In accordance with their member communication preferences on record on 30 June 2020, voters will receive voting instructions via email and/or a ballot package via postal mail (members can vote electronically or on paper ballots, but only one ballot will be accepted.) For more information on the election and candidates, visit the IEEE Annual Election web page at www.ieee.org/elections, or email election@ieee.org.

YOUNG PROFESSIONALS

WHY YOU SHOULD BE AN IEEE AND EDS MEMBER

BY MIKE SCHWARZ

Dear EDS community, I am writing to you to share my thoughts why it is beneficial to become an EDS member and/or renew it.

When I was a student it was not in my focus to become an IEEE member or EDS member. The question is why? First, I was not aware of it! Second, it was not obvious for me what the benefits are. This changed after my PhD and after I had started my professional career several years ago at the company Robert Bosch GmbH.

Why? I see my profession still in doing research and that's beside my work. I am doing research during my free time, so far as my family allows for. It is my passion to contribute somehow new knowledge to the community. Of course, my resources are limited, and that is how the membership of IEEE and EDS comes into the game. The magic is networking!

The membership offers me so many opportunities to exchange with colleagues all over the world, within the community and beyond. I met so many new researchers which are on the identical wavelength as me. New collaborations were the result without any cost. Many of these researchers became my friends and I am really glad to meet them at conferences or virtual meetings. This ben-



efit is beyond the typical measures you can get from the membership, i.e. discounts for IEEE conferences, paper access, etc.

After a few years of using this excellent membership I got the offer to be an active volunteering part of IEEE EDS. I became the Newsletter Editor for Western Europe. From the beginning, my welcome was very friendly and the staff of IEEE EDS is

very helpful. Let me thank you here for the support during this time, the exchange of information and help with occurring issues. Furthermore, I would like to thank the contributors of all the chapters, which make such great work possible! It works only with you!

I enjoyed the opportunity to get involved in IEEE EDS and to have the possibility to make the difference. I became a Vice-Chair of the Young Professionals in Germany and we established a team which is young and energetic. We re-established the YP activities in Germany and more is on the horizon.

One step further was the involvement of EDS in Germany by becoming the new chapter Chair since February this year. A lot of challenges and opportunities are waiting on the new team. But isn't it the undiscovered country which makes it so fascinating? Here, I would like to thank the participating satellites and members for being part of the chapter!

I personally can only encourage you to take the chance to influence something, be it with a report, an event or active participation in a committee.

With kind regards,
Mike

2018-2019 EDS REGION 9 OUTSTANDING STUDENT PAPER AWARD

The Electron Devices Society confers its prestigious Region 9 Outstanding Student Paper Award to the best Region 9 student paper published in an internationally recognized IEEE sponsored journal or conference in the field of electron devices related topics. The winning paper is entitled, "*Reconfigurable NanoFETs: Performance Projections for Multiple-Top-Gate Architectures*". This paper was published in the *IEEE Transactions on Nanotechnology* and was authored by Rebeca Moura, Nils Tiencken, Sven Mothes, Martin Claus and Stefan Blawid. The award will be presented at a future LAEDC or SBMicro. The Award consists of a certificate and reimbursement of up to US \$1,500 to cover one author's travel and accommodations to attend the conference. On behalf of the Electron Devices Society, I would like to congratulate Rebeca Moura and the remaining authors for this achievement. Brief biographies of all the authors of the paper are given below.



Rebeca dos Santos de Moura received the Master's degree in Electronics and Automation Engineering from Universidade de Brasília, Brazil, in

2018 and the Bachelor's degree in Computer Engineering from Universidade de Brasília, Brazil, in 2016. She is

currently pursuing a Ph.D. degree with the Geographic Information Systems Laboratory (LSIE) in the Geography Department at Universidade de Brasília, researching neural networks and deep learning algorithms to classify high spectral satellite images.



Stefan Blawid received his Dipl.-Phys. degree from the Freie Universität Berlin in 1993 and his PhD from the Max Planck

Physics of Complex Systems in 1997. He has extensive working experience both in academia (TU Braunschweig, 2001–2004, TU Dresden, 2009–2010, Universidade de Brasília, 2011–2019) as well as in semiconductor industry (Senior TCAD Expert at the memory company Qimonda, 2004–2009). Since 2019, Stefan Blawid is a Professor for Computer Engineering at the Federal University of Pernambuco, Recife, Brazil. His scientific activities focus currently on Computational Electronics, Quantum Information and Printed Organic Electronics.



Martin Claus received the Dr. Ing. degree in electrical engineering from the Technische Universität Dresden (TU Dresden), Germany, in

2011. From 2013 to 2017, he was an independent Research Group Leader for the modeling and simulation of emerging electronics at the Center for Advancing Electronics Dresden (Cfaed), Germany, focussing on nanotube, nanowire and organic electronics. In 2016 he expanded his field of expertise to stretchable thin film electronics as a Visiting Scholar at the Stanford University, USA. From 2012 to 2017 Martin Claus was also with Universidade de Brasília, Brazil, as a Visiting Scholar. Since 2017, he is with Infineon Technologies AG responsible for the development and enablement of high-frequency BiCMOS technologies.



Sven Mothes received the Dr.-Ing. degree in electrical engineering from Technische Universität Dresden, Dresden, Germany, in 2019. His

research interest includes modeling of carbon nanotube transistors and TCAD simulation of emerging devices. He works for Globalfoundries since 2019.

Nils Tiencken

No bio available

Arturo Escobosa
EDS Region 9 Outstanding Student
Paper Award Chair
CINESTAV-IPN
Mexico



CALL FOR NOMINATIONS

2020 IEEE EDS Early Career Award

Description: Awarded annually to an individual to promote, recognize and support Early Career Technical Development within the Electron Devices Society's field of interest

Prize: An award of US\$1,000, a plaque; and if needed, travel expenses not to exceed US\$1,500 for a recipient residing in the US and not to exceed US\$3,000 for a recipient residing outside the US to attend the award presentation.

Eligibility: Candidate must be an IEEE EDS member and must have received his/her first professional degree within the 10th year defined by the August 15 nomination deadline and has made contributions in an EDS field of interest area. Nominator must be an IEEE EDS member. Previous award winners are ineligible.

Selection/Basis for Judging: The nominator will be required to submit a nomination package comprised of the following:

- The nomination form that is found on the EDS web site, containing such technical information as the nominee's contributions, accomplishments and impact on the profession or economy and a biographical description.
- A minimum of two and a maximum of three letters of recommendation from individuals familiar with the candidate's technical contributions and other credentials, with emphasis on the specific contributions and their impacts.

The basis for judging includes such factors as: the demonstration of field leadership in a specific area; specific technical contribution(s); impact on the profession or economy; originality; breadth; inventive value; publications; honors; and other appropriate achievements.

Schedule: Nominations are due to the EDS Executive Office on August 15th each year. The candidate will be selected by the end of September, with presentation to be made in December.

Presentation: At the EDS Awards Dinner that is held in conjunction with the International Electron Devices Meeting (IEDM) in December. The recipient will also be recognized at the December EDS BoG Meeting.

Nomination Form: Complete the [nomination form](#) by August 15, 2020. All endorsement letters should be sent to l.riello@ieee.org by the deadline.

For more information contact: l.riello@ieee.org or visit: <http://eds.ieee.org/early-career-award.html>

EDS ELECTRONIC SNAP CIRCUITS DEMONSTRATION: EDS-ETC PROGRAM

By BHADRA POKHAREL

The ED Nepal Chapter in association with Nepalese Society for Women in Physics (NSWIP) Kathmandu, Nepal organized a demonstration program “Electronic Snap Circuits” as part of the EDS-ETC program. The event was held at Janak Nath Memorial Hish

School, Lainchaur, Kathmandu, Nepal, on December 11, 2019. Dr. Leela Pradhan Joshi, along with her colleagues, conducted this program by showing various interesting minor projects using electronic snap circuits. More than 30 students and science teachers

participated in the program, among which most of them were girls. The students showed their zeal towards learning the electronic and electrical circuits assembled in everyday devices such as mobile phones, solar cells, electric motors, etc.

ED National Institute of Technology—Silchar Student Branch Chapter, India

—by T. R. Lenka

IEEE Day was celebrated at NIT Silchar on October 1, 2019. The theme of IEEE Day was “Grow with IEEE EDS.” Several graduate, master and undergraduate students shared their views regarding what they liked the most about IEEE EDS, how the society helps them build their career, on the importance of joining students chapter and becoming members, on the activities that can be done under the banner of IEEE EDS, and most importantly, how to keep ourselves updated with current technology. The event was attended by 25 students and faculty members.



Attendees of the demonstration program “Electronic Snap Circuits”



IEEE Day at NIT Silchar; 1st row from left- Dr. Bijit Choudhury, Dr. Banani Basu, Dr. Puspa Devi, Prof. S. Baishya (Dean Academic, NIT Silchar), Prof. F. A. Talukdar (Branch Counselor), Dr. T. R. Lenka (Chair & Faculty Advisor), Dr. Kavi Charan



1st row from left to right- Ms. Anusmita Kakoti (Co-Chair), Prof. F. A. Talukdar (Branch Counselor), Prof. L. M. Patnaik (IEEE Fellow), Dr. T. R. Lenka (Faculty Advisor), Ms. Aparajita Modak (Co-Chair)

On November 18, 2019, Professor Gana Nath Dash gave a Distinguished Lecture on "Some New Results on Graphene FET (Graphene Nanoribbon FET," held at the Department of ECE, NIT Silchar, Assam, India. The research scholars working on quantum effects in electron devices highly benefited from the interactive session.

An invited talk by Prof. L. M. Patnaik "Deep Learning," was organized on February 26, 2020. Prof. Patnaik discussed emerging topics like Artificial Intelligence, Machine Learning and Deep Learning.

ED Delhi Chapter—Women in Science Workshop —by Mridula Gupta and Harsupreet Kaur

The Science Foundation and MHRD-Institution Innovation Council Deen Dayal Upadhyaya College (DDUC) Chapter, in collaboration with National Academy of Sciences India (NASI) Delhi Chapter, and the ED Delhi Chapter to organize on February 26-27, 2020 a "National Level Lecture Workshop on Women in Science: A Career in Science." The event was

aimed to apprise students about various career options for women in science and to showcase the work done by women scientists. Various parallel sessions covering Biological Sciences, Physics, Chemistry, and Computer Science & Electronics were organized and various noted speakers were invited to talk about emerging research and technological trends in these areas. The two-day workshop was well attended by 650 students and faculty members.

~Manoj Saxena, Editor



Invited speakers, organizers and participants of the workshop on the women careers in science

CHAPTER NEWS

2020 EDS CHAPTER OF THE YEAR AWARD— CALL FOR NOMINATIONS

The IEEE EDS Chapter of the Year Award is given each year based on the quantity and quality of the activities and programs implemented by the chapters during the prior July 1st – June 30th period (for 2021 subsidies—activities and programs between July 1, 2019 and June 30, 2020). Virtual events can also be included.

EDS recently revised our Chapter of the Year Award to award one non-student chapter and one student chapter in any geographic location.

Nominations for the awards can only be made by Regions/Chapters Committee Members, SRC Chairs/Vice-Chairs, or self-nominated by Chapter Chairs. Please visit the EDS

website to submit your nomination form (<http://eds.ieee.org/chapter-of-the-year-award.html>).

Each year each winning chapter (max 2) will receive a plaque and check for \$500 to be presented at an EDS chapter meeting of their choice. Travel

reimbursement will not be provided. A chapter that has previously received the Chapter of the Year Award is eligible for re-nomination only after three years from the year of award.

The schedule for the award process is as follows:

Action	Date
Call for nominations e-mailed to chapter chairs, SRC Chairs, SRC Vice-Chairs and Regions/Chapters Committee	June 1st
Deadline for nominations	September 15th
Regions/Chapters Committee & SRC Chairs & Vice Chairs selects winners	Early-October
Award given to chapter representative at requested chapter meeting	Open

EDS CHAPTER SUBSIDIES FOR 2021

EDS is providing funds to those EDS chapters that are requesting a subsidy based on the EDS chapter subsidy guidelines. The deadline for EDS chapters to request a subsidy for 2021 is September 1, 2020. All Chapter Chairs were informed through an email notifying the subsidy details and guidelines in June. Chapter subsidy is pegged to the activities reported to IEEE through Vtools. In general, activities which are considered fundable include but are not limited to, membership promotion, travel allowances for invited



speakers to chapter events, and support for EDS student activities at local institutions.

Chapter Subsidies can be requested by completing the EDS Chapter Subsidy Request Form <https://ieeeforms.wufoo.com/forms/2021-eds-chapter-subsidy-request-form/>. Please note that the 2021 subsidy request needs to be submitted by September 1, 2020.

Final decisions concerning subsidies will be made in December 2020. Subsidy funds will be issued by early January of the following year. Please visit the EDS website <https://eds.ieee.org/chapters/chapter-subsidy-program> for more information.

REPORT ON LAEDC 2020, SIGHT WORKSHOP AND EDS-ETC TRAINING

BY LUIS M. QUEVEDO AND MARIO ALEMAN

The Latin America Electron Devices Conference (LAEDC 2020) held in San Jose Costa Rica, gathered at least 27 EDS student and professional leaders and volunteer members from EDS chapters of Central America. Many volunteers participated actively in the conference delivering presentations during a poster session as part of the conference technical program. EDS volunteers and leaders received support from their respective chapters and EDS scholarships to attend the conference. Most of these volunteers stated that this was the first time attending an international conference from an IEEE technical society.

During LAEDC, a SIGHT (Special Interest Group on Humanitarian Technology) workshop was also organized, sponsored by the IEEE Humanitarian Activities Committee (HAC), where attendees learned about funding opportunities and benefits, and best practices in the deployment of technology projects in underserved communities. The workshop was delivered by Dr. Pritpal Singh (SIGHT Assessment Subcommittee Chair) and Dr. Fernando Guarin (SIGHT Education Subcommittee Chair). Furthermore, Dr. Singh as invited speaker presented a talk entitled "R&D Opportunities in Photovoltaic Systems". During the event there was also a SIGHT outreach table available for the conference participants. More information on the SIGHT blog announcement.

There was also a Snap Circuits Training organized as a part of the EDS-ETC program. It was held at the Costa Rica Institute of Technology (TEC) on February 25th, and was organized by the TEC EDS Student Chapter. The session was attended by volunteers and officers from the EDS chapters in Latin America: Guatemala, El Salvador, Honduras, Nicaragua, Costa Rica and Argentina, including YP and WIE members from the Costa Rica Section. The training was delivered by Luis Miguel Quevedo (Chair of YP for EDS in R9) and Dr. Fernando Guarin (EDS Past-President).



Students from EDS Chapters in Central America



EDS-ETC Training for EDS Volunteers from Region 9



SIGHT Workshop presented by Dr. Pritpal Singh

REGIONAL NEWS

LATIN AMERICA (REGION 9)

EDS Mini-Colloquium Held in Costa Rica

—by Lluís Marsal and Benjamin Iñiguez

On Tuesday, February 25, 2018, the Costa Rica EDS Student Chapter organized a mini-colloquium (MQ) held the day before the start of the 2nd LAEDC. Five invited speakers, all of them EDS Distinguished Lecturers, conducted talks ranging from advanced materials and semiconductor device technologies to design, compact modeling and reliability.

Dr. Fernando Guarín, from GlobalFoundries, East Fishkill, (NY, USA) delivered a presentation entitled “Leveraging semiconductor technology for the benefit of society”. Prof. Durga Misra, from New Jersey Institute of Technology, NJIT (NJ USA) gave his lecture entitled “Nanoelectronics to Nanotechnology: Challenges and Directions.” Dr. Ravi Todi, from Western Digital, Milpitas, (CA, USA) delivered a talk titled “Semiconductor Industry: “A story of unprecedented growth, and we are just getting started!” Prof. Jesús del Alamo, from the Massachusetts Institute of Technology, (MA, USA) presented a talk on “Reliability and Instability of GaN Power Field-Effect Transistors.” Finally, Prof L. F. Marsal from the University Rovira i Virgili (Spain) gave a talk entitled “Current Progress and Advances in Polymer Solar Cell.” The MQ was attended by about 80 participants including researchers and students both IEEE EDS members and non-members.

The afternoon sessions were dedicated to device modeling. Prof. Marcelo Pavanello (Centro Universitario FEI, Sao Bernardo do Campo, Brazil) gave as EDS Distinguished Lecturer a talk entitled “Influence of Substrate



EDS DL Ravi Todi during the lecture, “Semiconductor Industry: “A story of unprecedented growth, and we are just getting started!”



EDS DL Marcelo Pavanello during the lecture, “Influence of Substrate Bias on the Mobility of Nanowire MOSFETs”

Bias on the Mobility of Nanowire MOSFETs.”

Afterwards, the 2nd Latin American edition of the MOS-AK Workshop on Compact Modeling was held. It was chaired by Prof. Benjamin Iñiguez (Universitat Rovira i Virgili, Tarragona, Spain). It included five talks. Prof. Antonio Cerdeira (CINVESTAV, Mexico) presented an “Analytical Current-Voltage Model for Double Gate a-IG-

ZO TFTs with Symmetric Structure.” Prof. Alexander Kloes (Technische Hochschule Mittelhessen, Giessen, Germany) addressed “Approaches for Analytical (Compact) Modeling of Tunneling Currents in MOS Transistors.” Prof. Jean-Michel Sallese (EPFL, Switzerland) gave a talk about “Modeling the Junctionless Ion Sensitive Field Effect Transistor.” Prof. Gilson Wirth (UFRGS, Porto Alegre, Brazil)

targeted “The area scaling of charge trap induced time-dependent variability.” Finally, Prof. Benjamin Iñiguez (Universitat Rovira i Virgili, Tarragona, Spain) talked about “Characterization and modeling of 1/f noise in organic and IGZOTFTs.”

Over 70 academics, professionals and students attended these events and enjoyed the discussions with the speakers.

2020 LAEDC Conference Report

—by Arturo Escobosa,
Lluís Marsal, Benjamín Iñiguez
and Mario Aleman

The 2nd Latin American Electron Device Conference (LAEDC 2020), sponsored by the IEEE Electron Devices Society (EDS), was held from February 25–28, 2020 in San Jose, Costa Rica, was held in conjunction with the Latin American Symposium on Circuits and Systems (LASCAS 2020). This conference attracts students as well as young researchers and its main goal is to bring together specialists from all Electron Device related fields from Latin America and the rest of the world. The main topics of interest were: All electron based devices, Semiconductor, MEMS, and Nanotechnologies, Packaging, 3D integration, Sensors and Actuators, Display technology, Modeling and Simulation, Reliability and Yield, Device Characterization, Energy Harvesting, Biomedical Devices, Circuit-Device Interaction, Novel Materials and Process Modules, Technology Roadmaps, Electron Device Engineering Education, Electron Device Outreach and Optoelectronics, Photovoltaic and Photonic Devices and Systems.

The organizing committee included Mario Aleman (General Chair), Arturo Escobosa (CINVESTAV, Program Chair), Benjamín Iñiguez (URV, Technical co-Chair), and Lluís F. Marsal (URV, Technical co-Chair).

We received contributions from authors of the Americas, Europe and Asia: Spain (13), Mexico (11),

Nicaragua (9), USA (7), Brazil (5), France (5), El Salvador (4), Germany (4), Switzerland (3), Costa Rica (2), Austria (2), Estonia (2), Belarus (1), Belgium (1), Canada (1), China (1), Korea (1), Puerto Rico (1), Russia (2), United Kingdom (1) and Uruguay (1). There were also representatives from major companies such as GlobalFoundries, Western Digital, HP and Intel.

The conference had 77 participants and 59 accepted papers presented during 12 sessions organized in four main fields: Devices Physics, Devices and Materials, Modelling; and Organic Devices. Fourteen contributions were presented as posters in a session mostly dedicated to regional activities. The number of contributions has more than doubled from the first LAEDC edition.

One of the highlights of the conference was the keynote delivered by Prof. Jesus A. del Alamo from Massachusetts Institute of Technology (MIT) “Nanoscale III-V Electronics: InGaAs-FinFETs and Vertical Nanowire MOSFETs” where he delivered a very interesting presentation on his group’s research and accomplishments covering aspects from fabrication to testing and reliability topics.

Conference participants enjoyed the very friendly atmosphere that was conducive to many fruitful discussions, most of them while enjoying the wonderful local coffee. Various social events were held like; a welcome reception, a well-attended Young Professionals/Women in Engineering mixer, and a conference banquet where the local flavors were mixed with music and a performance by a dance group. Several activities were also conducted to further increase participation in the EDS chapter activities in Central America and increase EDS membership. A special highlight were two sessions devoted to Women in Engineering and Young Professionals, a special session for SIGHT (Special Interest Group on Humanitarian Technology). There was

also an IEEE EDS-ETC Snap Circuits Workshop.

More information on the LAEDC Conference is available at <https://laedc.cinvestav.mx>.

~Edmundo Guiterrez-D., Editor

EUROPE, MIDDLE EAST & AFRICA (REGION 8)

ED/AP/MTT/COM/EMC Tomsk
Joint Chapter
**Moscow Workshop on Electronic
and Networking Technologies
MWENT 2020**

—by O.V. Stukach

The three-day MWENT 2020 Workshop, technically co-sponsored by EDS, endorsed by IEEE Russia Central Section and Tomsk Joint Chapter, was organized in Moscow, Russia. This biennial three-track event has rapidly become one of the highlight workshops on networks and electronic technologies, gathering researchers from both academia and industry. The host organization was Moscow Institute of Electronics and Mathematics of National Research University Higher School of Economics (MIEM HSE), one of the most prestigious education institutions in Russia. The main goal of the workshop was to stress the importance of survivability aspects in the growing content-oriented networks and reliability of electron devices. Technical networks exhibit many interdependencies that are to be comprehensively measured and modeled. The network design leads typically to multi-objective optimization problems involving an interplay between resilience, sustainability, and robustness. The current network design and evaluation methods are often unable to cope with these interdependencies. MWENT aimed at their better understanding and implementation. Throughout the extensive review and discussion, it was confirmed that

ongoing network infrastructures are globally progressing rapidly and that new application domains are emerging mainly based on IoT beyond all kinds of communication.

The MWENT Award Ceremony at the Museum of Radio Electronics Development

An increase in community interest in MWENT has been observed this year. A total amount of 200 regular submissions were reviewed by TPC members and external reviewers. As a result, we have 157 peer-reviewed manuscripts in the Proceedings. The accepted papers were organized into the following sessions: Fundamental Problems of Electronics, Network and Telecommunication, Technologies of Electronic Instrument Engineering, Information Security, Signal Processing, Satellite Communications, and Measurements. The technical program was enriched by a comprehensive overview of MIEM scientific programs. As a tradition of MWENT, in addition to the IEEE Xplore publication, participants were also provided with electronic proceedings. The next edition of our events, the 15th International Siberian Conference on Control and Communications (SIBCON) will be held in Kazan, Russia, on May 13–15, 2021. For more information, please follow the link <https://kpfu.ru/sibcon2021>.

~Kateryna Arkhylova, Editor

ASIA & PACIFIC (REGION 10)

Annual Meeting of the EDS Japan Joint Chapter

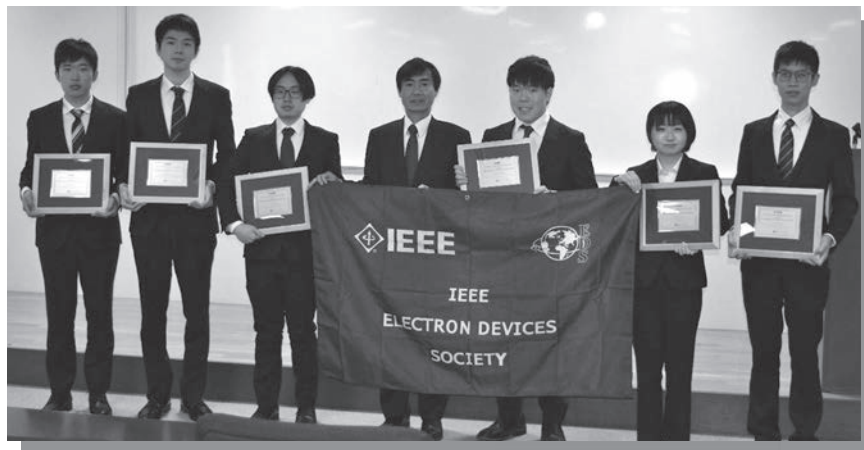
*—by Akira Nishiyama and
Yuichiro Mitani*

On February 7, 2020, the annual meeting of the EDS Japan Joint Chapter was held at Institute of Industrial Science, The University of Tokyo. Dr. Akira Nishiyama, Japan Joint Chapter Chair and Prof. Toshiro Hiramoto, Vice Chair, reported 2019 activities and 2020 plans of the Chapter. New officers of the EDS Japan Joint Chapter (Chair: Prof. Hiramoto, Vice-chair: Dr. Sugii, Secretary: Prof. Kobayashi, Treasurer: Dr. Watanabe), was also introduced at the meeting. After this, the 2019

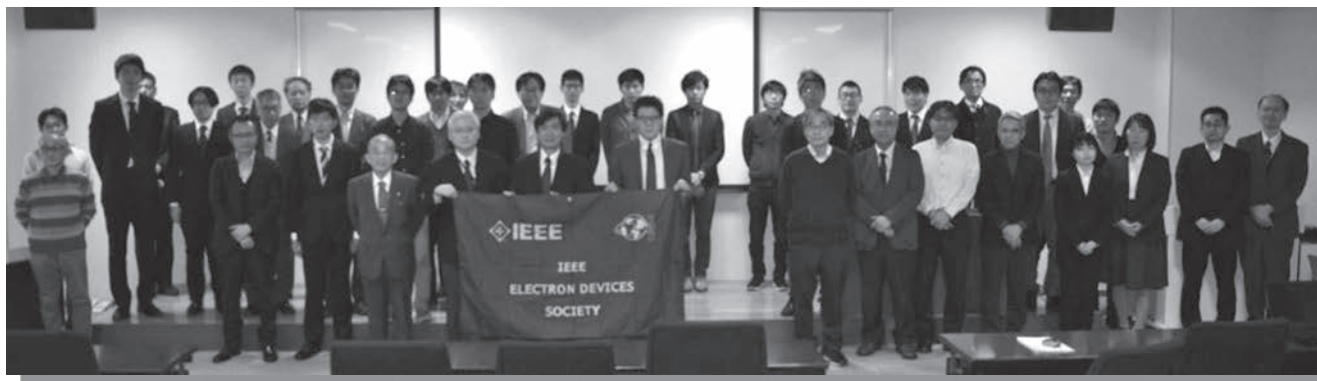
EDS Japan Joint Chapter Student Award (VLSI & IEDM) was presented to 6 students, who made excellent presentations at the VLSI Symposia 2019 and IEDM 2019. The award winners are posted on the Japan Joint Chapter's webpage; (http://www.ieee-jp.org/japancouncil/chapter/ED-15/ed15_award.htm).

After the annual meeting, the IEDM 2019 Report Session was held, with 9 members of the IEDM program committee reporting on summary, topics and research trends of their subcommittees to more than seventy attendees. The session provided a good opportunity for the attendees to touch the latest technology trends, especially for those who were unable to attend the IEDM.

The executive committee meeting of the EDS Japan Joint chapter was also held on the same day and the



18th EDS Japan Joint Chapter Student Award winners, with Prof. Toshiro Hiramoto; New Chair (2020~) on February 7, 2020, Tokyo



The annual meeting of EDS Japan Joint Chapter attendees on February 7, 2020, Tokyo



The executive committee meeting the EDS Japan Joint Chapter on February 7, 2020, Tokyo

plans for 2020 of the Chapter were approved.

ED Tsinghua University Student Branch Chapter

—by Yancong Qiao

On January 23, 2020, Professor Takao Someya and his team from the University of Tokyo came to the EDS Tsinghua Chapter for academic communication and held an academic workshop. The two sides had in-depth communication on wearable electronic devices, electronic skin, physiological signal monitoring, etc. Five students from Professor Someya's research group gave wonderful reports, and six students

from the Chapter also gave research reports. Finally, Professors Someya and Tian-Ling Ren made comments.

Reports by Prof. Someya's group:

1. Long-term monitoring of mastication using Nanomesh electrodes, by Yutaro Sumi
2. Organic electrochemical transistor, by Jiabin Wang
3. All-nanofibre-based, Ultra-sensitive, Gas-permeable Mechano-acoustic Sensors for Continuous Long-term Heart Monitoring, by Osman Goni Nayeem
4. Advanced Microelectrode Arrays for Monitoring Electrophysiological Activities, by Jimbo

5. Nanomesh pressure sensors for ionic solution environments, by Faezeh Arab Hassani
Reports by students of EDS Tsinghua Chapter:

1. Graphene electronic skin, by Yancong Qiao
2. ECG-Machine Learning-Review, by Xiaoshi Li
3. Graphene based Glucose Sensing Device, by Jinming Jian
4. Highly Sensitive and Transparent Sensors With Graphene for Continuous and Non-invasive Intraocular Pressure Monitoring, by Jiandong Xu
5. Human Pulse Sensing and Diagnosing System, by Rui Guo
6. Research on Intelligent Insole System Based on Graphene Pressure Sensor, by Xiaolin Han

Finally, Professor Someya gave a report "Electronic skins for robotics and wearables" at the main building to all students of Tsinghua University.

IEEE EDS Distinguished Lecture—ED Guangzhou Chapter

—by Lei Wang

Professor Jie Yu, IEEE Fellow, gave a Distinguished Lecture entitled "Optical Communication Chip Technology for 5G Networks and Data Centers," on May 20, 2019, at the ED Guangzhou Chapter. Over 50 engineers, academics and students attended this



EDS workshop on January 23rd, for ED Tsinghua University Student Branch Chapter

event and enjoyed the discussions with the speaker.

Professor Xing Zhou, IEEE EDS Distinguished Lecturer, gave an interesting talk entitled “Future III-V/CMOS Co-Integrated Technology and

Hybrid Circuit Design,” on December 23, 2019, at the ED Guangzhou Chapter. Over 30 engineers, academics and students attended this event and enjoyed the discussions with the speaker.

2019 Reliability Physics Annual Meeting of China—ED Guangzhou Chapter

—by Lei Wang

The ED Guangzhou Chapter co-hosted the 2019 Reliability Physics Annual Meeting of China. The conference was held on October 16–18, 2019 at Guilin city, China. Over 150 engineers, academics and students attended this event and enjoyed the wonderful keynote speeches and session presentations. Keynote speakers include Professor Dao-Guo Yang from Guilin University of Electronic Technology, Professor Bo Sun from Beihang University, Professor Yun Huang from China CEPREI Lab., Professor Wen-Yan Yin, from Zhejiang University, et al.

2019 IEEE Electronic Exploration Camp—ED Guangzhou Chapter

—by Lei Wang

ED Guangzhou Chapter co-hosted the 2019 IEEE Electronic Exploration Camp in Guangzhou. On July 25, 52 local high school students from Guangzhou practiced the exploration course entitled “Exploration of Internal Structure of Chips,” including interactive theory teaching, optical microscope operation, electron microscope and 3D X-ray equipment visit. The combination of theory and practice of this activity



Prof. Jie Yu, DL talk on May 20, for ED Guangzhou Chapter with the audience



Prof. Xing Zhou, DL talk on December 23rd, for ED Guangzhou Chapter with the audience



2019 Reliability Physics Annual Meeting of China, ED Guangzhou Chapter



2019 IEEE Electronic Exploration Camp, ED Guangzhou Chapter

effectively stimulated the interest of middle school students on the chip structure. This year is the second time that the IEEE Electronic Exploration Camp has landed in Guangzhou. The series of activities have been carried out successively at the University of California (San Diego), the Hong Kong University of Science and Technology, Peking University, and the Institute of Microelectronics of the Chinese Academy of Sciences.

ED/SSC Beijing Section (Shenzhen) Chapter

—by Shengdong Zhang

Prof. Chip Hong Chang from Nanyang Technological University (NTU) of Singapore gave two lectures on January 15, 2020, hosted by the ED Shenzhen Chapter.

In the morning, Prof. Chip Hong Chang gave a lecture entitled “Design for Trust Techniques”. He mainly discussed the Design for Trust Techniques. An introduction to key gates and logic locking was first given to establish basic concepts. Then, he discussed more details by showing some examples of different logic locking and attack designs.

In the afternoon, Prof. Chip Hong Chang gave a talk on “Security of Hardware Implementation of Cryptographic Algorithms”. He introduced Non-invasive Passive and Active Attacks on Cryptographic Devices.



Invited talk by Prof. Chip Hong Chang, ED/SSC Beijing Section (Shenzhen) Chapter, January 15

He gave an introduction on several state-of-the-art works. He focused on the Asymmetric and Symmetric Key Crypto and detailed analyses, such as the side channel analyses and differential fault analysis.

~Ming Liu, Editor

EDS Malaysia Kuala Lumpur Chapter

—by Maizatul Zolkapli, Norhayati Soin, Nowshad Amin & Sharifah Fatmadiana Wan Muhammad Hatta

IEEE EDS Malaysia Annual General Meeting 2020

The 30th Annual General Meeting (AGM) of the EDS Malaysia Chap-

ter was held on January 18, 2020 at Pulse Grande Hotel, Putrajaya. 23 EDS members from all over Malaysia attended the meeting. Dr Zubaida Yusoff and Ir Azrif presented all the EDS events, activities and financial status in 2019. New executive committees for a one-year term were elected and Prof. Ir Dr. Norhayati Soin from Universiti Malaya will continue to lead ED Malaysia Chapter for the second year. During the meeting, the Best Volunteer award was presented to Dr Aliza Aini Md Ralib from International Islamic University Malaysia while the Best Student Volunteer Award was presented to Mr Chow Kuan Yan from IEEE EDS UKM Student Branch. All Excomm members

of 2019 were presented with appreciation certificates. Also, ED Malaysia Chapter was awarded the 1st prize in the Annual Website Competition during the IEEE Malaysia Section Annual General Meeting held on the same day and venue. A money prize of RM500 was awarded to the best website judged in terms of performance, mobile compatibility, search engine optimization and security. Congratulations to EDS Malaysia Chapter!

EDS Malaysia Chapter Membership Drive and Technical Talk

From February to March 2020, the IEEE EDS Malaysia Chapter had organized several membership drives in conjunction with technical talks held at community colleges and polytechnics across Malaysia. On February 7–8, a membership drive was held in conjunction with a grant proposal workshop at the KPJ Healthcare University College in Melaka. There were around 30 participants. On February 17–18, 2020, a membership drive was conducted at the Langkawi Tourism Academy, in conjunction with a technical workshop on grant applications where there were 10 participants. On March 5th, the IEEE EDS Malaysia Chapter had a membership drive event in conjunction with a technical talk on Industry 4.0 at the Polytechnic Sultan Idris Shah, Sabak Bernam where there were around 20 participants. On March 9th, a membership drive was conducted at the Pagoh Polytechnic, in conjunction with a technical talk on Research Project Methodology. There were around 30 attendees and all participants to these events consisted of polytechnic students and university college lecturers.

EDS Technical Talk: Solar Photovoltaic (PV) Energy for a Sustainable Greener World at German-Malaysian Institute

In collaboration with the GMI (German-Malaysian Institute), the IEEE EDS Malaysia Chapter conducted a Technical Talk on “Solar Photovoltaic (PV) Energy for a Sustainable Green-



Attendees of the 30th AGM of IEEE EDS Malaysia Chapter



Clockwise from Left: Membership drives at Community College Langkawi, KPJ Healthcare University College, Pagoh Polytechnic and Polytechnic Sultan Idris Shah, Sabak Bernam

er World.” The talk was given February 26, 2020 by Prof. Dr. Nowshad Amin, the strategic hire professor and Advisor to the Solar Photovoltaic Research wings of Universiti Tenaga Nasional (@UNITEN, The National Energy University). About 80 participants from GMI attended the talk and derived immense knowledge from the presentation. The Strategic Planning and Business Development Unit of GMI sponsored the event to create more awareness on on-going global warming issues together with the introduction of Solar Photovoltaic

Energy technologies as one of the possible solutions.

EDS Malaysia Lecture Series 1/2020

The first lecture series was held March 11, 2020 at Universiti Tenaga Nasional, Bangi. About 30 attendees, including EDS members and students enjoyed two talks “Carbon nanotube based biosensors: prospects and application,” by Dr. Iskandar bin Yahya of IMEN, UKM and “Flexible electronics for wearable technology,” by Prof. Ir Dr. Norhayati Soin of Center of Printable Electronics, UM.



Some moments from the technical talk (Prof. Dr. Nowshad Amin in the middle)

in the field of semiconductor electronics. This is the 14th ICSE organized by the Electron Devices Chapter of IEEE Malaysia Section and technically co-sponsored by the IEEE Electron Devices Society. Over the last twenty-eight years, ICSE conference series has become the prominent international forum on semiconductor electronics embracing all aspects of the semiconductor technology including circuit and device modelling and simulation, photonics and sensor technology, MEMS technology, process and fabrication, packaging technology and manufacturing, failure analysis and reliability, materials and devices for nanoelectronics. Please visit our website for further details <https://ieeemalaysia-eds.org/icse2020/>

~P Sushitha Menon, Editor

Mini-Colloquium on "Nanoelectronics to Nanotechnology"

—by Ajit Kumar Panda



Organizers and attendees of EDS Malaysia lecture series 1/2020

ED NIST (National Institute of Science & Technology) Student Branch Chapter, India organized on February 27–28, 2020, the 10th IEEE EDS Distinguished Lecturer Mini-Colloquium. It was held at NIST, Berhampur, Odisha, India, and was attended by 154 participants. Professor Souvik Mahapatra, IIT-Bombay delivered the DL lecture "CMOS Technology Scaling and Reliability" wherein he explained the fundamental understanding of MOS, concept of scaling and reliability issues. Professor Chandan Sarkar, Jadavpur University delivered the DL talk "Semiconductor Industry towards Tunnel-FET." Professor Subir Kumar Sarkar, Jadavpur University delivered the DL talk "BiCMOS: A Current Trend in VLSI." Professor Abhisek Dixit, IIT-Delhi had a talk "ABC to Y2Q of Quantum Computers" wherein he emphasized quantum computing and its supremacy. Also Professor T. R. Lenka, NIT-Silchar delivered a talk "III-Nitride Nanowires for Solar Photovoltaic."

28 - 29 JULY 2020 | KUALA LUMPUR
ICSE 2020



IEEE International Conference on Semiconductor Electronics (ICSE) 2020

EDS Malaysia Chapter is pleased to welcome everyone to participate in the 2020 IEEE International Confer-

ence on Semiconductor Electronics (ICSE) on July 28-29, 2020. This bi-annual technical conference since 1992 aims at bringing together researchers from industry and academia to gather and explore various issues and trends



Attendees of the 2020 IEEE EDS NIST Student Chapter MQ

Mini Colloquium on “Nano-Electronics and Advanced Semiconductor Devices for Future Electronics”

—by Mridula Gupta and Harsupreet Kaur

Department of Instrumentation of Shaheed Rajguru College of Applied Sciences for Women in collaboration with IEEE EDS Delhi Chapter jointly organised a Mini Colloquium “Nano-electronics and advanced semiconductor devices for future electronics” on February 27, 2020. The colloquium comprised a Distinguished Lecture by Dr. Héctor J. De Los Santos, Founder of NanoMEMS Research LLC, California, and lectures by Dr. Abhishek Dixit, Indian Institute of Technology Delhi

and Dr. Brajesh Kumar Kaushik, Indian Institute of Technology, Roorkee. The talks were focused on various aspects of Nano-Electron-Fluidic Logic (NFL), Quantum Computing and Spintronics. The speakers apprised the audience about the current technological trends, challenges and the emerging research aspects in these areas.

ED Kalyani Government Engineering College Student Branch Chapter

—by Angsuman Sarkar

The Chapter organized a Technical Lecture on February 19, 2020 by Dr. Imon Mondal, Dept. of Electrical Engineering, IIT Kanpur on “Wideband



Felicitations of Dr. Imon Mondal

Tunable True-Time-Delay Architecture Using a Variable Order All-Pass Filter and its Applications to Continuous-Time Pulse Processing.” The lecture was held in the Language Lab of Kalyani Government Engineering College, and was attended by 110 students.

ED NIST (National Institute of Science & Technology) Student Branch Chapter

—by Ajit Kumar Panda

The Chapter organized a technical lecture on “Innovation in Power” by Mr. Ranjit Kumar Dash who worked in semiconductor industries like Texas Instrument and National Semiconductor for more than twenty years at various positions. The lecture was held on November 7, 2019 at NIST Berhampur, Odisha, India. The speaker discussed switching of the regulators during the stand-by mode to reduce the power consumption by adopting various methods like using electronic shut-down circuits, line and load regulations, challenges in circuit design to maintain the maximum current and supporting high input and output voltage.

The chapter organized a Distinguished Lecture “Advanced Packaging” by Professor S. S. Iyer on December 21, 2019, at NIST campus. The lecturer discussed challenges in interconnections and routing and wafer level connectivity to miniaturize the packaged chip. The lecture was attended by 127 participants.



Attendees of the Mini-Colloquium



Attendees with Professor Durga Misra (top—behind banner)



Attendees with Professor Vijay Kumar Arora (standing in the center)

On January 9, 2020, a DL “Nanoelectronics to Nanotechnology: Challenges and Directions” was delivered by Prof. Durga Misra, NJIT, USA. It was held at the NIST campus. Professor Misra discussed self-heating in Fin-FETs, challenges and proposed solutions, issues of process technologies facing a rapidly growing demand, and most importantly AI driven semiconductor research.

On March 16, 2020, a DL “Nanoelectronics” was delivered by Prof. Vijay Kumar Arora, Professor of Electrical Engineering and Physics at Wilkes University. The speaker discussed the topic “Ohm to Arora: A New Paradigm for Nanoscale Devices and Circuits”. He also highlighted using MATLAB for developments in

nanoelectronics. 30 faculty members attended the talk.

ED National Institute of Technology—Silchar Student Branch Chapter

—by T. R. Lenka



1st row from left to right- Ms. Anusmita Kakoti (Co-Chair), Prof. F. A. Talukdar (Branch Counselor), Prof. L. M. Patnaik (IEEE Fellow), Dr. T. R. Lenka (Faculty Advisor), Ms. Aparajita Modak (Co-Chair)

On November 18, 2019, Professor Gana Nath Dash gave a Distinguished Lecture on the topic “Some New Results on Graphene FET (Graphene Nanoribbon FET),” held at Department of ECE, NIT Silchar, Assam, India. The research scholars working on quantum effects in electron devices highly benefited from the interactive session.

An invited talk by Prof. L. M. Patnaik “Deep Learning” was organized on February 26, 2020. Prof. Patnaik discussed emerging topics like Artificial Intelligence, Machine Learning and Deep Learning.

ED Indian Institute of Technology—Roorkee Student Branch Chapter

—by Sourabh Jindal & Ankit Gaurav

The chapter organized two technical talks on January 10, 2020. The first talk “Neuromorphic Computing: Algo, H/W and Devices” was delivered by Professor Kaushik Roy, Edward G. Tiedemann Jr. Distinguished Professor, Electrical and Computer Engineering Faculty at Purdue University, West Lafayette. The talk was held at Dept. of ECE, IIT Roorkee on January 10, 2020. The participants gained knowledge about design of AI systems from device to system level and Implementation of such systems with emerging devices. The second talk “Transistor based Analog H/W for AI” was delivered by Dr. D. Bhowmik, Dept. of EE, IIT Delhi, India. About 70 students and faculty members attended the lecture. His talk was

focused on Analog hardware neural networks with spintronic devices.

A technical talk “Processor Technology & Architecture Past, Present & Future” was organized on January 17, 2020. The guest speaker was Dr. Vivek De, Intel Fellow and the Director of Circuit Technology Research in Intel Labs, India. He discussed a processor performance scaling driven by CMOS technology, a multi-core exploit thread-level and task-level parallelism via multi-core design, and a more flexible fine-grain power and thermal management. About 60 students attended the lecture.

On January 20, 2020, technical talk was delivered by Rakshit Jain, Ph.D. student in applied physics at Cornell working with Ralph and Buhrman groups on the topic “Spin Orbit Torques in heavy metals and topological materials.” The talk was attended by about 60 students.

ED Netaji Subhash Engineering College (NSEC) Student Branch Chapter

—by Saheli Sarkhel, Ayush Thakur and Sneha Upadhyay

The chapter in association with the Department of ECE organized a “Hands-on workshop in Embedded System” on November 9, 2019. EDS SBC members were trainers for this workshop. This seven-hour long workshop (attended by 30 students) was divided into two sessions. The first session gave the participants an in-depth introduction on Arduino including C/C++ programming for Arduino. The second session dealt with operation of motor drivers, applications and an overview of gyroscope and accelerometer sensor.

On January 17, 2020, the chapter in association with the Department of ECE, NSEC organized an IEEE EDS Distinguished Lecture by Dr. Ajit Kumar Panda, Professor and Dean, National Institute of Science and Technology, Berhampur, India. The topic was “GaN-HEMT based front end transceiver for 5G communication technology.” More than 45 par-



Technical talk by Professor Kaushik Roy at IIT Roorkee, India on January 17, 2020

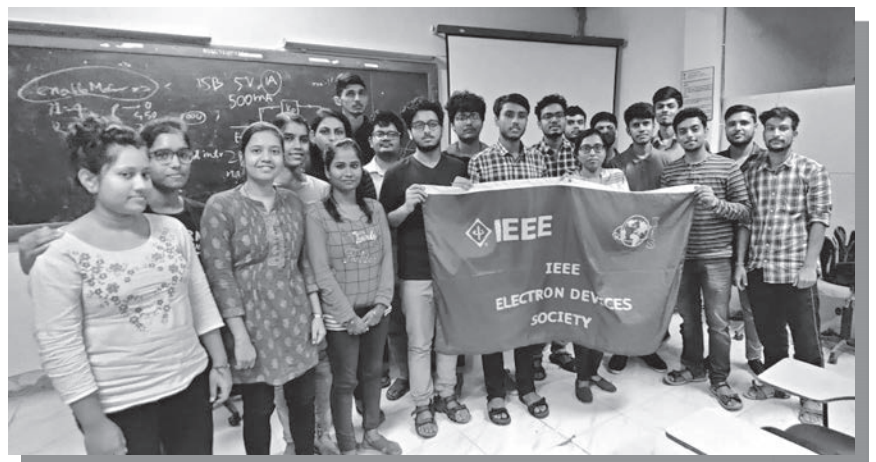


Technical talk by Dr. Vivek De at IIT Roorkee, India on January 17, 2020

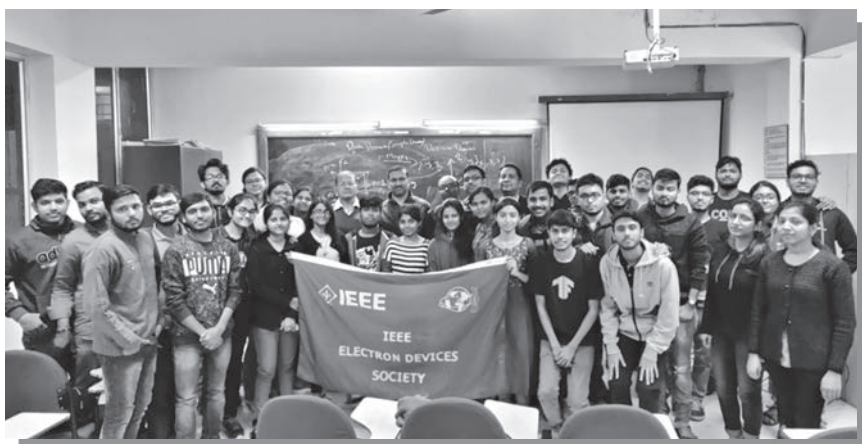
ticipants including IEEE EDS SBC members, students of ECE and EE departments attended the seminar.

On January 27, 2020, the chapter in association with the Department of ECE, NSEC organized a one-day seminar on “Machine Learn-

ing for IoT Analytics” by Prof. Amlan Chakrabarti, Professor and Director, A.K. Chowdhury School of Information Technology, University of Calcutta. He discussed various factors which paved the way for rapid developments in hardware and software,



Attendees of “Hands-on workshop in Embedded System”



Team of ED NSEC Student Branch Chapter, participants and faculty members with Prof. A. Chakrabarti (middle, back row)



Participants of One Day Workshop on "Instrumentation of Materials Science"



Prof. Subir Kumar Sarkar delivering a Lecture at the IEEE EDS Center of Excellence, HITK

communication advancements, and the need for IoT these days. Almost 40 IoT enthusiastic students participated in this seminar.

ED Nepal Chapter

—by Bhadra Prasad Pokharel

IEEE EDS Nepal Chapter, in association with Materials Science and Engineering Program organized on January 23, 2020 a technical talk in Pulchowk Campus, Institute of Engineering, Pulchowk, Nepal. The talk "Research on ferroelectrics at the Low Dimensional Materials Research Centre, University of Malaya" was delivered by Dr. Thamil S. Velayutham, Low Dimensional Materials Research Centre, Department of Physics, Faculty of Science, University of Malaya, Kuala Lumpur, Malaysia. The seminar was attended by about 20 students and faculty members.

The chapter also organized on February 20, 2020, a One Day Workshop "Instrumentation of Materials Science", held in Amrit Science Campus, Tribhuvan University, Kathmandu, Nepal. The lecturers of the program were Prof. Bhadra Pokharel, IEEE/EDS Nepal Chapter Chair and Prof. Lila Pradhan, Executive Committee Member. Prof. Pokharel presented slides on EDS and on a theoretical background of dielectric constant measurement using LCR meter, specially using a HIOKI Hitester. Prof. Pradhan presented a talk on how to operate a visible light spectrometer experimentally. She presented a theoretical background as well as an experimental procedure. The workshop was attended by 24 post-graduate students.

ED Heritage Institute of Technology Student Branch Chapter, Kolkata

—by Atanu Kundu

A Distinguished Lecture (DL) Program was organized on November 5, 2019 at the IEEE EDS Center of



Dr. Binit Syamal (in the middle behind the banner) with participants

Excellence, Heritage Institute of Technology. Prof. Subir Kumar Sarkar, Department of ETCE, Jadavpur University delivered a lecture 'Transient Electronics: a Brief Study of the Materials and Devices'.

In the second session, Dr. Binit Syamal, Research Scientist at Nanyang Technological University, Singapore delivered a talk 'How semiconductor Foundry works'. His meticulously prepared presentation of a complicated process was very informative and gave the students an insight into how the real world devices come to life. The sessions were attended by 20 participants.

ED Delhi Chapter

—by *Mridula Gupta and Harsupreet Kaur*

The Department of Electronics, Sri Venkateswara College (University of

Delhi), in association with IEEE EDS Delhi Chapter organized on September 18–19, 2019, a two days workshop "Data science." The resource persons were experts from Innovians Technologies and Technex'20, Indian Institute of Technology (BHU), Varanasi. It was an interactive training & hands-on workshop which equipped the students with practical understanding on the topic.

The Department of Instrumentation of Shaheed Rajguru College of Applied Sciences for Women, in collaboration with the chapter jointly organised on September 27, 2019, a DL "Nanotechnology Science and Engineering Amalgamation Emerging Liberalism of Homo Sapiens" by Professor Vijay K. Arora, UTM Distinguished Professor, Wilkes University, USA, and Universiti, Teknologi Malaysia. The technical talk was attended by 120 students and college faculty mem-

bers of the department of Instrumentation and Electronics. Prof. Mridula Gupta, Chairperson of the IEEE EDS Delhi chapter, delivered a talk on IEEE, its mission, vision and also explained IEEE membership benefits to the undergraduate students of the college.

A Fourth Lecture Workshop on Trans-disciplinary Areas of Research and Teaching by Shanti Swarup Bhatnagar Awardees, jointly organized by MHRD Institution Innovation Council (IIC)–DDUC Chapter, National Academy of Sciences India, Allahabad–Delhi Chapter, IEEE Electron Device Society (EDS)—Delhi Chapter, IEEE Delhi Section and Science Foundation, Deen Dayal Upadhyaya College (under the aegis of DBT Star College Program) was held on September 27–28, 2019. The first talk on September 27th, "Mathematical modeling as a transdisciplinary framework and its applications to neuroscience" was delivered by Prof. Karmeshu, Distinguished Prof. at Dept. of Computer Science and Engineering, Shiv Nadar University, Uttar Pradesh. The second talk "Origin and Early Evolution of the Solar System" was given by Dr. Jitendra Nath Goswami, Physical Research Laboratory, Gujarat. The third speaker was Prof. Surendra Prasad, Emeritus Professor at Department of Electrical Engineering, IIT Delhi. Prof. Ajoy Ghatak, delivered a talk "Evolution of Quantum Theory & Entanglement." The last talk "Photonics revolution" was delivered by Prof. Anurag Sharma, Dept. of Physics, IIT Delhi. On September 28th, Dr. G. Narahari Sastri, Director of CSIR-North East Institute of Science and Technology, Jorhat delivered a talk "Chemistry for a Better Tomorrow." The next talk "Sendai Virus Recruits Cellular Villin to Remodel Actin Cytoskeleton During Fusion with Hepatocytes: Implications in Liver Gene Therapy" was delivered by Professor D. P. Sarkar, Dept. of Biochemistry, Univ. of Delhi South Campus. The third talk "Unreal Molecules Doing



Prof. Mridula Gupta (Chairperson of EDS Delhi Chapter), organisers and participants of the "Data science" workshop



Prof. Cher Ming Tan with the Distinguished Lecture participants

Real Things in Unreal Times” was delivered by Prof. Balasubramanian Sundaram, Jawaharlal Nehru Centre for Advanced Scientific Research (JNCASR), Bangalore. The fourth talk “Current Status of Malaria Vaccine Development” was delivered by Prof. Deepak Gaur, Jawaharlal Nehru University, New Delhi. The last talk “New answers to old questions regarding long-standing questions about DNA synthesis by DNA polymerases” was delivered by Prof. Deepak Thankappan Nair, Regional Centre for Biotechnology, Faridabad. Over 450 students and faculty members from 20 different institutions attended the workshop.

Sixth hands-on workshop “VHDL programming & digital circuit designing with implementation on FPGA” was jointly organised on October 21–24, 2019 by Department of Electronics, Deen Dayal Upadhyaya College (University of Delhi) and the EDS Chapter. Participants gained

hands-on experience on NEXYS 4DDR FPGA Boards from *Xilinx*.

As a part of IEEE Day celebration and 100th birth centenary (1919–2019) of Dr. Vikram A Sarabhai, father of Indian space programme, a colloquium “Indian space programme: India’s incredible journey” was organized by Deen Dayal Upadhyay college, University of Delhi, in association with EDS Delhi Chapter. Various invited talks from eminent scientists and academicians were organised to apprise the participants about various geo-spatial technologies, reusable launch vehicles, trends in the space borne antenna system technologies for communication, navigation and satellites.

Department of Electronic Science, University of Delhi South Campus, in collaboration with the chapter organized on January 28, 2020 a DL “Computational Reliability – A paradigm shift in product reliability assurance” delivered by Professor Cher Ming Tan, Chang Gung University,

Taiwan. The technical talk was attended by 120 students and faculty members. Prof. Tan talked about product reliability that is becoming increasingly important in view of an increasing dependence of the products on technology.

The Robotics Club and Department of Instrumentation of Shaheed Rajguru College of Applied Sciences for Women, in collaboration with IEEE EDS Delhi chapter successfully conducted on February 17–18, 2020 a two days Hands-On Workshop “I-SENSO BOTZ for Embedded System Design”. The workshop was focused on application of robotics for designing embedded systems. The participants were encouraged to develop various projects based on microcontrollers using sensors, control circuits and motors with intelligent systems. The two day workshop was attended by 51 students and 10 faculty members.

~Manoj Saxena, Editor

EDS MEETINGS CALENDAR



THE COMPLETE EDS CALENDAR CAN BE FOUND AT OUR WEB SITE:

<https://eds.ieee.org/conferences/conferences-calendar>

PLEASE VISIT.

<u>2020 33rd International Vacuum Nanoelectronics Conference (IVNC)</u>	06 July – 08 July 2020	Virtual Event
<u>2020 IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)</u>	20 July – 23 July 2020	Cancelled
<u>2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)</u>	August 2020 Exact Dates are TBD	Virtual Event
<u>2020 International Symposium on VLSI Design, Automation and Test (VLSI-DAT)</u>	Aug 10 – Aug 13 2020	Hsinchu, Taiwan
<u>2020 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA)</u>	Aug 10 – Aug 13 2020	Hsinchu, Taiwan
<u>Advanced Semiconductor Manufacturing Conference (ASMC)</u>	Aug 23 – Aug 25 2020	Saratoga Springs, NY, USA
<u>2020 27th International Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD)</u>	01 Sept – 04 Sept 2020	Kyoto, Japan
<u>XXVth International Seminar/Workshop on DIRECT AND INVERSE PROBLEMS OF ELECTROMAGNETIC AND ACOUSTIC WAVE THEORY DIPED-2020 (DIPED)</u>	15 Sept – 18 Sept 2020	Tbilisi, Georgia
<u>2020 15th European Microwave Integrated Circuits Conference (EuMIC)</u>	15 Sept – 17 Sept 2020	Utrecht, Netherlands
<u>2020 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)</u>	23 Sept – 25 Sept 2020	Kobe, Japan
<u>2020 IEEE International Integrated Reliability Workshop (IIRW)</u>	04 Oct – 08 Oct 2020	Virtual Event

<u>2020 IEEE International Interconnect Technology Conference (IITC)</u>	05 Oct – 08 Oct 2020	San Jose, CA, USA
<u>2020 International Semiconductor Conference (CAS)</u>	07 Oct – 09 Oct 2020	Sinaia, Romania
<u>2020 13th International Conference on Advanced Semiconductor Devices And Microsystems (ASDAM)</u>	11 Oct – 14 Oct 2020	Smolenice, Slovakia
<u>2020 IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)</u>	25 Oct – 27 Oct 2020	Redondo Beach, CA, USA
<u>2020 International Conference On Computer Aided Design</u>	02 Nov – 05 Nov 2020	San Diego, Ca, USA
<u>2020 9th International Symposium on Next Generation Electronics (ISNE)</u>	07 Nov – 09 Nov 2020	Changsha, China
<u>2020 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)</u>	08 Nov – 11 Nov 2020	Monterey, CA, USA
<u>2020 International EOS/ESD Symposium on Design and System (IEDS)</u>	11 Nov – 13 Nov 2020	Chengdu, SICHUAN, China
<u>2020 IEEE International Electron Devices Meeting (IEDM)</u>	10 Dec – 18 Dec 2020	Virtual Event
<u>2020 IEEE 51st Semiconductor Interface Specialists Conference (SISC)</u>	16 Dec – 19 Dec 2020	San Diego, CA, USA

CHANGE IN EDS NEWSLETTER DISTRIBUTION

Attention All EDS Members,

Included in your annual EDS membership benefits are quarterly print copies of the newsletter, as well as electronic versions sent to your preferred email address.

In May 2019, the EDS Board of Governors approved to add the option to request a print version of the newsletter for those that have a preference, and making the electronic version the default. There is no extra cost to receive the print copy.

When you renew your EDS membership for 2021, if you wish to continue receiving the print copy of the EDS Newsletter, you must indicate this in your IEEE account. Thank you.

