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Technical Briefs

Beyond CMOS (BC)

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I. Introduction

CMOS scaling has driven a broad spectrum of applications through increased performance and complexity. As dimensional scaling of CMOS eventually approaches fundamental limits, new information processing devices and architectures have been explored extensively in both academia and industry. The Beyond CMOS (BC) chapter in the International Roadmap for Devices and Systems (IRDS) surveys, catalogs, and assesses viable emerging devices and novel architectures for their long-range potential, and identifies the scientific and technological challenges gating their acceptance by the semiconductor industry. In the previous International Technology Roadmap for Semiconductors (ITRS), the Emerging Research Devices (ERD) chapter covered a similar scope. The BC chapter in IRDS has inherited certain content, structure, and methodology from the ERD chapter in ITRS. During the transition from ITRS to IRDS, the importance of co-optimization of emerging devices and architectures has been increasingly recognized in the broad research community. Therefore, beyond the traditional focus on emerging memory and logic devices, the BC chapter has placed significant emphasis on emerging device-architecture interactions.

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Although the semiconductor industry faces difficult challenges in CMOS dimensional scaling, there are promising alternative directions for sustained improvement in chip performance and functionality. Integrating new high-speed, high-density, and low-power memory technologies onto the CMOS platform may break the "memory wall", improve system performance, and enable new computing paradigms (e.g., in-memory compute). Novel switches based on new materials, alternative mechanisms, and non-charge state variables (e.g., steep-slope transistors, phase-transition devices, nonvolatile switches) may achieve significantly better energy efficiency than CMOS transistors based on thermionic emission over the channel energy barrier. New information processing technologies substantially beyond the capabilities of CMOS may originate from an innovative combination of new devices, interconnect, and architecture for extending CMOS, which may eventually lead to new platform technologies. Ultimately scaled CMOS as a platform technology may also extend into new domain of functionalities and applications (e.g., security, sensing, communication), a general direction known as "more than Moore". For all these promising directions beyond CMOS and dimensional scaling, new materials and integration techniques play essential roles to enable their implementations.

The BC chapter covers the following major areas: 1) emerging memory and storage devices, 2) emerging logic and alternative information processing devices, 3) emerging device-architecture interactions (including new computing paradigms), and 4) emerging materials integration. This article will briefly review these areas of research and present key observations and recommendations.

II. Emerging Memory and Storage Devices

Memory is an essential element of computing, and the characteristics of the memory device technologies play a significant role in the architecture of an information processing system. A taxonomy of current memory devices is given in Fig. 1. Static and dynamic random access memory (SRAM and DRAM) remain the workhorse computing memory technologies, due to their high speed and endurance. Both are volatile and require backup storage when powered down. Nonvolatile memory includes flash, the most prominent and technologically mature baseline technology. The term "flash" refers to an array architecture for charge based memory cells such as floating gate and charge trapping memory, both of which serve as the main data storage mechanism for most modern information processing systems. SRAM, DRAM, and Flash memory have followed Moore's Law scaling for several decades, which was tracked by the ITRS until 2015 and is currently tracked by IRDS. Prototypical devices have matured to the point where the technology is in small-scale commercial production, and often the technology is making progress on factors such as scaling and density. In this case, prototypical devices that are making progress have historically been tracked by ITRS and expected future progress is predicted. These technologies include ferroelectric memory (FeRAM), phase change memory (PCM), field-switched magnetic memory (MRAM), and spin transfer torque magnetic memory (STT-MRAM). Several of these technologies, such as STT-MRAM started in the emerging category and have progressed to the prototypical phase and are continuing to progress commercially.

The primary purpose of the Emerging Memory Devices section is to track technical progress for those devices in the rightmost "emerging" column. This section provides a technical overview of each device, and is accompanied by tables that track key properties of these devices as reported in the literature, such as endurance, retention, switching characteristics, and minimum dimensions. These emerging memory devices are the subject of significant research, with potential to continue storage density scaling beyond physical limits of flash, improve computing efficiency by enabling storage class memory,

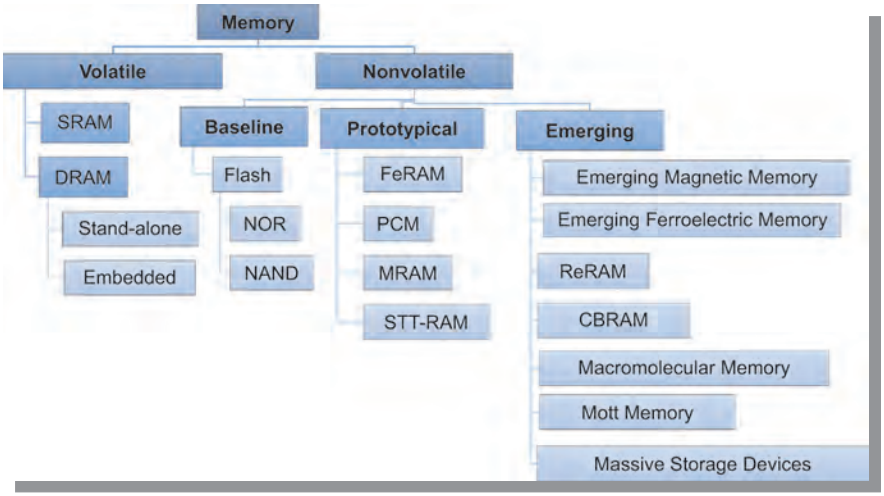

Figure 1. Emerging memory devices taxonomy.

and enable new computing paradigms such as in-memory compute.

One of the most active emerging memory research topics is magnetic memories. STT-MRAM has made significant progress in the past decade, and recently we have seen the emergence of several commercial products and integration in commercial foundries. This is due to excellent scalability, CMOS-compatible voltages, high endurance, and compatibility with back end of line CMOS processes. STT-MRAM has the potential for future use as a cache replacement, [1] although it will be important to reduce switching current, increase speed, and increase energy efficiency. This need for improved magnetic memory properties has prompted research in emerging magnetic devices. One example is the three terminal memory structure which harnesses spin orbit torque (SOT) effect, reducing the current density required to switch the magnetization of a magnetic tunnel junction (MTJ). Another active area of research is in voltage controlled magnetic anisotropy (VCMA), which harnesses magnetoelectric effects to reduce the energy and improve the speed of MTJ switching [2].

Resistive and conductive-bridge random access memory (ReRAM and CBRAM), have seen also significant commercial interest and research activity in the literature, due to potential for applications such as storage class memory, edge computing, and efficient processing of neural networks. These are two terminal resistive switching device structures, with a memory state defined by the resistance. This resistance is controlled by the connecting and breaking of metallic conductive filaments (CBRAM) or modulation of oxygen vacancy concentrations in a metal oxide (ReRAM). Resistive memories are highly scalable and CMOS-compatible, and hence are being integrated into foundry processes. Research challenges for these devices continue to be improving the understanding, parametric control, and reliability. Emerging polymer memories, which incorporation organic materials, often rely on similar physical mechanisms to ReRAM and CBRAM [3].

Ferroelectric memories, including the ferroelectric field effect transistor (FeFET) have seen a resurgence of interest recently due to the discovery of ferroelectricity in HfO [4] which has provided a path for FeFET scalability and CMOS compatibility. Other new technologies that are further from commercialization (and lack concrete benchmarks) have become the subject of significant research. For example, DNA storage (covered under massive storage devices) has the highest volumetric information storage capacity of any known medium, which has motivated research to tackle the practical challenges of using these complex organic molecules for information storage. It is hoped that the IRDS coverage of emerging memories can serve as a reference for the electron device community and engineers in understanding new memory devices and their impact on future computing systems, for funding agencies in understanding the memory research challenges, as well as for students and others in academia who need a better understanding of the memory research landscape.

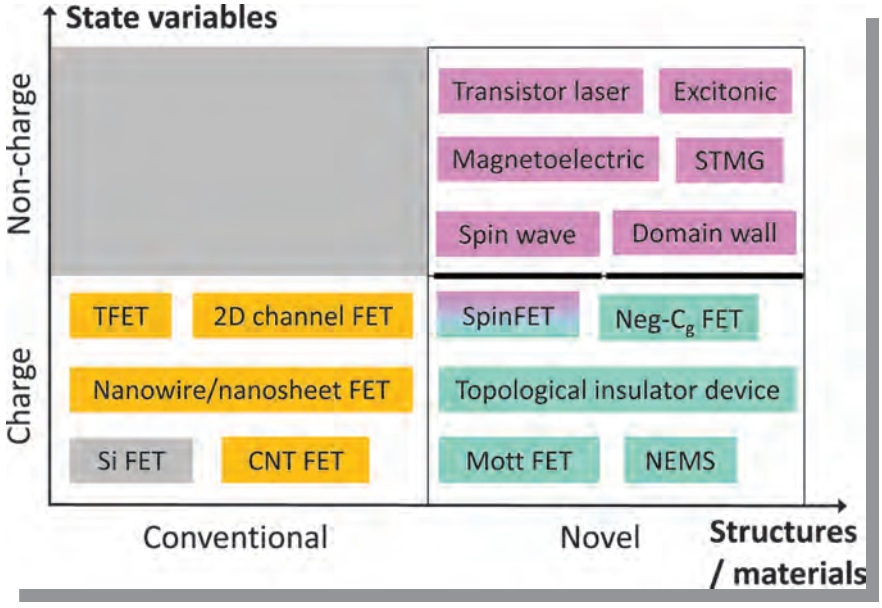

Figure 2. Taxonomy of logic devices beyond CMOS. Reproduced from Figure BC3.1 of the 2021 IRDS Beyond CMOS chapter.

III. Emerging Logic and Information Processing Devices

For nearly twenty years, the industry's semiconductor roadmap has featured device options that might surpass silicon CMOS as the driver for logic, computation, and information processing applications. Originally captured as Emerging Research Devices, recent editions of the IRDS present these as Logic Devices Beyond CMOS. Though silicon CMOS has proved exceptionally hardy and productive over the last twenty years, the roadmap continues to track Beyond-CMOS devices for both near-term successors and more disruptive, longer-term candidates.

Figure 2 depicts the taxonomy of emerging logic devices as conveyed in the IRDS. Such devices depart from the present state-of-the-art in two primary ways. First, the structure and materials constituting the device will be different to some degree from silicon planar FETs or FinFETs. This departure is shown on the horizontal axis. Second, the physical manifestation of digital information, also known as the state variable, may differ from the electric charge that is used in FETs. This is shown on the vertical

axis. Considering these elements together, a natural three-part grouping emerges that is used to characterize near-term vs. far-term candidates for the evolution of semiconductors.

The nearest of these candidates are the conventionally structured, charge-based devices listed in the lower left of the figure. Such devices include nanowire transistors and carbon nanotube transistors, for example. The intent with these devices is to obtain charge transport characteristics exceeding the semiconductor channels of conventional devices. Thus, a few of these candidates could be considered as potential channel-replacement technologies for near-future state-of-the-art devices and are also tracked within the "More Moore" component of the IRDS. This includes "stacked nanosheet" devices as well as vertical gate-all-around (VGAA) transistors.

Further evolutions of charge-based devices are considered in the lower right of the figure. Here, one begins to see mechanisms for modulating charge transport that differ from the electrostatic field effect. Some examples include using a type of metal-insulator phase transition (Mott transition) as a switch or using electromechanical potential to store a digital state. Because of the greater departure in materials systems from CMOS as compared with the first category of candidates, it is expected that integration with CMOS will be more complicated and take longer to manifest commercially. Also, it is less clear for any of these devices that there is a route to the kind of universal performance applicability and scalability that has made silicon CMOS economically viable for so long.

A recent addition to the Beyond CMOS roadmap in this second group of the figure is the topological insulator transistor. Research into topological insulators as materials has increased substantially in recent years, primarily for applications in quantum information science. Some of these research results suggest routes to using topological properties to increase the speed and power efficiency of field-effect devices. It is an ongoing line of inquiry to determine if such advantages can be materialized robustly at room temperature with commercially relevant yields.

Finally, the Beyond CMOS roadmap has always monitored the progress in devices shown at upper right in the figure, which represent a substantial departure both in form and function from conventional semiconductor field-effect transistors. Principally, these devices use a non-charge-based state variable, such as a remnant magnetization, exciton, or optical/photonic state. In some cases, state information can be transported via charges, such as with a spin-filtered electronic current. In others, the change in state variable also requires a novel form or material structure for the interconnect. Thus, development and commercial maturation for these candidates is expected to take significant time, or else such devices might only be used within heterogeneous integration contexts, i.e., alongside state-of-the-art silicon.

As the industry progresses and the nearer-term Beyond CMOS candidates become more central to the IRDS, the focus of logic device evaluation beyond CMOS will evolve. Though the core focus remains on digital information processing, it seems less and less likely that a candidate will emerge that will take over the mantle of the silicon FET as the workhorse of linear, multi-generational progression for the industry. Instead, a variety of devices tailored to a variety of applications and accelerators will need to be explored and matured using ultimate silicon as a foundation for experimentation and commercialization.

IV. Emerging Architectures and Device Interaction

Many new emerging devices will require co-design between devices and higher levels of computer design (*e.g.*, circuit, architecture, and application). These emerging devices are not intended simply as "drop-in" replacements for standard CMOS devices, but will require new types of circuit designs, new functional module architectures, and even new software to best utilize the new devices' capabilities [5].

Novel design issues that span the device and architecture levels especially need to be considered when adopting new low-level computing paradigms. Devices may be organized in radically new ways to carry out computation in a very different style from what we may consider the most "conventional" computing paradigm, which has relied on standard combinational and sequential non-reversible Boolean logic. The Beyond CMOS roadmap has begun tracking some of the most common building blocks for emerging systems and applications as shown in Fig 3.

At the device level, there are many types of devices that function as a synaptic device that both hold a stored state and use that state to modulate an analog input. This type of device is critical to overcoming the von Neumann Bottleneck: rather than moving data between memory and a processor, processing is directly integrated with each memory element. The analog processing of a synaptic device can also replace the 1,000's of transistors needed to do a digital operation with a single device. Another important class of devices are stochastic devices that generate a random binary or analog value. For many of the devices the probability distribution is tunable allowing for controllable randomness. Conventional digital logic is deterministic and cannot introduce true randomness, and instead require relatively expensive pseudo random number generators (PRNGs). Replacing a large expensive PRNG with a single device allows one to consider algorithms that are inherently stochastic and would otherwise be computationally expensive.

At the circuit level there are both circuits dedicated to computing a specific "neuron" function very efficiently, and circuits that are based on a crossbar array of synaptic devices

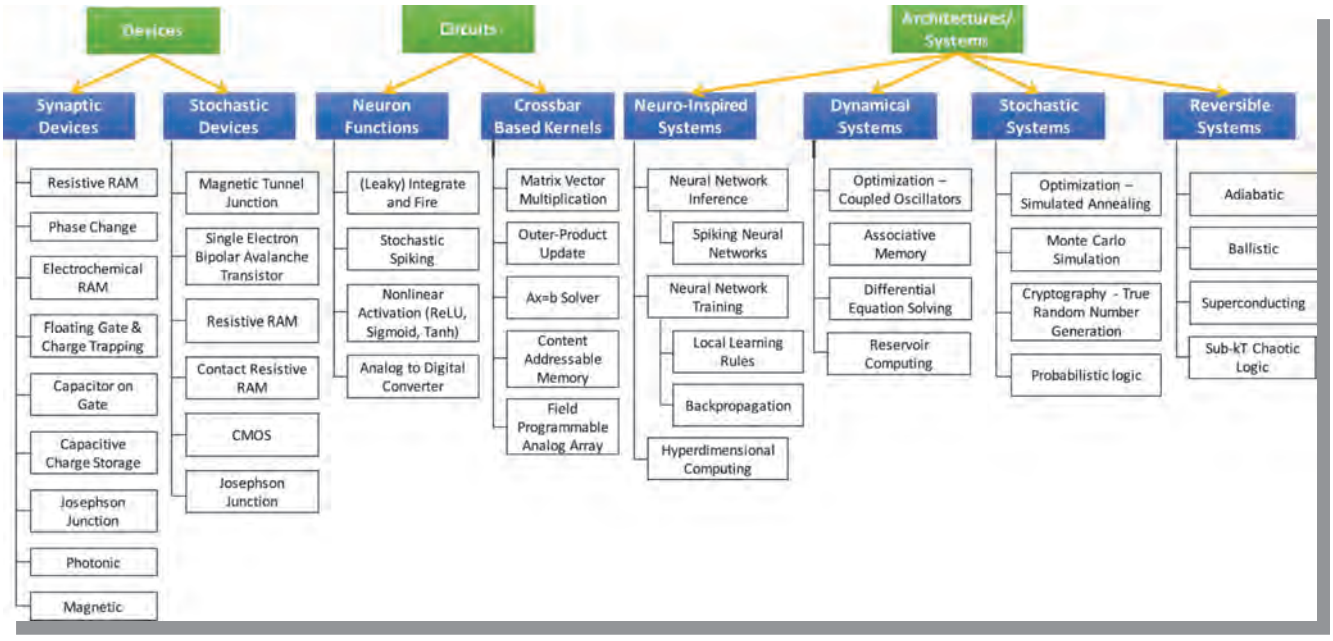

Figure 3. Emerging architectures require co-designing new devices, computational kernels and computational systems. Some of the possible building blocks are shown.

to compute a given matrix operation. Converting between analog and digital is typically a very expensive operation, and so neuron devices and circuits that can directly operate on an analog input avoid this cost. Common functions include leaky-integrate-and-fire neurons, stochastic spiking neurons, rectified linear neurons, and sigmoidal neurons. At the array level, there are computational kernels that can read a matrix in parallel by performing matrix vector multiplication, write a matrix in parallel by updating all values by the outer product of two input vectors, approximately solve the matrix equation $Ax = b$ for a vector x, implement a content addressable memory, and provide a reconfigurable analog computing substrate through a field programmable analog array.

These enabling devices and circuits can then be used to build a wide variety of architectures and systems. Neuro-inspired systems include conventional neural network inference and backpropagation based training. Spiking neural networks promise to reduce communication and analog to digital conversion (ADC) costs. New neural training algorithms based on local learning rules promise to drastically reduce the data-movement and buffering needed to train a neural network. Hyperdimensional computing is a new high-dimensional learning system that is enabled by large hardware-based content addressable memories.

Dynamical systems can use the temporal evolution of a recurrently connected system to solve a variety of problems. Coupled oscillators can be used to solve optimization problems. Associative memories can be stored in Hopfield networks. Differential equations can be mapped to analog substrates, and reservoir computing systems can be used to analyze temporal data. Chaotic logic networks can carry out monolithic reversible transformations of the state of a Boolean circuit even down to sub-kT signal levels.

Stochastic devices enable new systems that are built around repeated random sampling. Simulated annealing can be used to solve optimization problems. Stochastic devices enable Monte Carlo simulation. True random number generation is critical for cryptographic applications and tunable random devices enable probabilistic logic.

In addition to developing accelerators for specific computing functions, reversible computing systems aim to lower the energy dissipation of *general* digital logic, including both general-purpose programmable digital processors, and more specialized digital ASICs. Rigorous thermodynamic arguments have shown that the fundamental *Landauer limit* on energy efficiency can only be avoided in deterministic computational processes composed from local primitive operations if they have the property of (conditioned or unconditional) *logical reversibility* [6]. In addition to the potential for reducing minimum energy dissipation below conventional limits, reversible techniques can potentially exceed the conventional limits on larger-scale practical computing efficiency. Concrete examples of reversible computing systems based on both semiconducting and superconducting technology platforms have been demonstrated, and this area seems ripe for further development.

In this section, the Beyond CMOS roadmap has surveyed a variety of concepts and R&D directions for the development of novel beyond-CMOS computing technologies that represent an effort to think "outside the box," in the sense of looking beyond

just developing simple drop-in replacements for traditional logic and memory cells. More broadly, new hardware designs spanning multiple levels from the devices up through circuits and architectures must be considered, and the interactions between the various levels explored. More specifically, we expand the scope of future computing technologies beyond traditional irreversible, deterministic digital logic to include a broad range of alternative, unconventional computational paradigms, such as analog, probabilistic, and (classical) reversible computing paradigms.

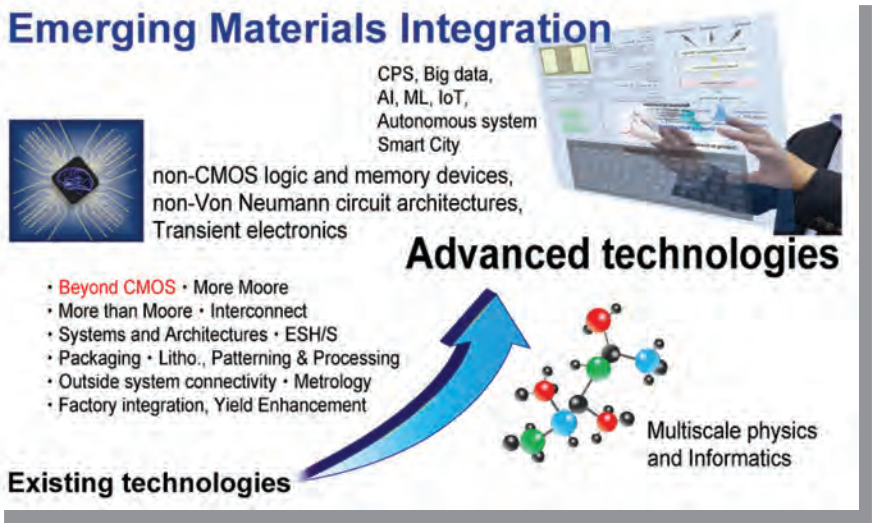

Figure 4. Emerging Material Integration promotes the advancement of existing technologies.

V. Emerging Materials Integration

In the previous ITRS activities that form integrated knowledge and collective intelligence in academia, consortia, and industry researchers, the international technology working group of Emerging Research Materials (ERM) presented potential solutions from a materials science perspective for future logic and memory devices, front end processing, interconnects, assembly and package, lithography, metrology, and life-cycle assessment of Environment, Safety, and Health (ESH)-related issues [7]. Taking over that experience, the IRDS 2020 edition set up "Emerging Materials Integration (EMI)" section in the "Beyond CMOS" chapter. While existing technologies are integrated on a Si-based platform, the majority of beyond-CMOS technologies are based on entirely new materials and cutting-edge material science. The key EMI challenge is to provide timely guidance on emerging materials, process performance, cost, reliability, and sustainable developments that will drive breakthroughs in the future. Figure 4 depicts the role of EMI, which is to promote the advancement of existing technologies.

The current EMI section emphasizes strategic challenges, novel breakthroughs, and potentially disruptive opportunities for emerging material properties, synthetic methods, and metrology, organized in the following areas: (1) Scaled technology materials needs for More Moore, (2) Novel materials for Beyond CMOS, and (3) Potentially disruptive material opportunities for functional scaling and convergent applications. Regarding materials for advanced More Moore technologies, high mobility transition metal dichalcogenides (TMD) with low defect density and low resistance ohmic contacts are listed as a long-term difficult challenge. Nano-carbon materials, complex metal oxides and spin-related materials are attracting attention as materials for non-CMOS logic and memory devices. Novel interlayer dielectrics, such as Metal Organic Framework (MOF) and Carbon Organic Framework (COF) will improve the interconnect reliability. Materials and processes that enable monolithically 3D integrated complex functionality, such as integration with flexible electronics and biocompatible functional materials, are also included in long-term challenges. As one of the convergent opportunities, EMI section refers to Big data and Digital transformation (DX) issues. Robust and ubiquitous information processing and independent power supplies (such as Energy Harvesting expanding the IoT utilization, one of the major topics in "More than Moore" chapter) will be a place for emerging materials to play an active role. Emerging materials have been spurring developments of non-von Neumann architectures for novel computing, such as neuromorphic computing, reinforcement learning, topological quantum computing, reversible computing, and probabilistic computing. A typical example is physical reservoir computing. Since computing performance in these systems depends on the unique material properties of the reservoir, the material research to optimize physical phenomena for reservoir computing will directly improve performance metrics such as energy efficiency. It is expected that the output of energy harvesting and the required power for novel computing approaches will be matched in the near future.

To drive emerging material technologies, the EMI section focuses on multiscale simulation. Conventional multiscale physics modeling was described previously in the ERM chapter of ITRS, where the physics to explain mesoscopic level phenomena is required to link electronic properties and device characterization. In the EMI section of the current BC chapter, a potential role for machine learning and informatics has been suggested as an alternative to the simulation in the

mesoscopic level, where inputs of molecular level phenomena provide an output describing continuum level phenomena. Transient electronics is introduced as one example of a disruptive technology. Here, materials, devices, and systems disappear with minimal or non-traceable remains in a controllable period of time. The spontaneous and transient functions in the material property, such as a conductance change with a controllable decay in atomic switches, are also treated with the appearance of transient electronics in the EMI section. This emerging electronics with a 'fading' capability will bring about intelligent applications, such as environmentally friendly electronics for one of the targets of SGDs Goal 12, to substantially reduce waste generation through prevention, reduction, recycling and reuse [8]. Future editions of EMI will provide additional descriptions and continue to adapt its scope to engage with societal environment, such as autonomous systems, smart cities and CPS. Cooperation with international standardization groups, which prepares a common protocol for assessing the properties of emerging materials, will also be considered part of EMI activities.

VI. Assessment

With a large variety of mechanisms and characteristics as well as different levels of maturity, beyond-CMOS devices present a unique challenge for assessment of their performance and potential. The BC chapter has referenced the emerging device benchmarking in the Nanoelectronics Research Initiative (NRI) for quantitative assessment [9]. The NRI benchmarking evaluates novel switches in conventional Boolean logic circuits (e.g., an inverter, a 2-input NAND gate) with quantitative metrics (e.g., speed, power dissipation, footprint, span of control, logical effort). Although the assessment of beyond-CMOS devices is an evolving effort and conclusions could be continuously altered by new research progress, some observations are worth noticing. First, the power-speed tradeoff commonly observed in CMOS continues to be a challenge for beyond-CMOS devices. Many beyond-CMOS devices utilize novel mechanisms and non-charge state variables to achieve low switching power; however, communication with many non-charge tokens is often significantly slower than moving charges. Second, most beyond-CMOS devices have not been shown to be capable of replacing CMOS with better power-speed performance. CMOS will remain the primary basis for IC chips for the coming years. Some promising beyond-CMOS technologies could be utilized to augment CMOS as special purpose accelerators to offload specific computations from the general-purpose processors. While integrating dissimilar technologies and materials is challenging, advance in heterogeneous integration may make this more feasible over time. Third, as the characteristics of beyond-CMOS devices become better understood and controlled, work on novel architectures that can leverage these unique devices becomes increasingly important. Co-optimization of emerging devices and architectures may have great potential to improve the energy efficiency and performance of computing systems. Last, the high-precision fabrication capabilities critical to CMOS (e.g., patterning, deposition, purity, doping, alignment) will continue to be important in the realization of systems built upon beyond-CMOS devices.

Previously, the ITRS ERD chapter utilized a survey-based critical review to assess the potential of beyond-CMOS devices, as a consensus among researchers participating in the survey. The ERD assessment measured devices on a scale of 1 to 3 on a set of criteria, including scalability, speed, energy-efficiency, gain (or on/off ratio), operational reliability, operational temperature, and CMOS compatibility. A spider chart was used to visualize the assessment. The ERD survey-based assessment has been widely cited in literature, although the scale of the survey sometimes raised questions about the accuracy of some assessment. At the same time, for highly exploratory devices without sufficient data, this assessment based on the survey of experts' perspective indeed provided an alternative measure of their potential.

As beyond-CMOS devices are being developed increasingly for novel computing paradigms beyond Boolean logic and von Neumann architecture, benchmarking cannot be simply performed at the device or logic gate levels. Benchmarking across multiple layers from devices to architectures is a great challenge that has to be addressed by interdisciplinary collaborations. Facing a large variety of design options and applications, benchmarking needs to be focused with well defined criteria and assumptions in order to produce meaningful results. Unlike in mature technologies where benchmarking may be more conclusive, beyond-CMOS benchmarking may provide guidance more than drawing definitive conclusions.

VII. Summary

Beyond-CMOS research has gone through a transition from a focus on novel devices with the potential to replace CMOS transistors to a holistic approach driven by device-architecture interaction and cooptimization to augment CMOS. The IRDS Beyond CMOS (BC) chapter not only tracks the progress of emerging logic and memory devices but also summarizes their utilization in unconventional computing architectures and applications. New computing paradigms may exploit unique characteristics of beyond-CMOS devices for more efficient native implementations of key functions. These promising devices often rely on emerging materials and advanced fabrication and integration techniques for demonstration and prototyping. The IRDS Beyond CMOS (BC) chapter covers promising research directions from materials and devices up to designs and architectures, to provide a comprehensive reference for research beyond conventional CMOS technologies, Boolean logic, and von Neumann architectures. As the dimensional scaling reaches its

limits, continued improvement of chip efficiency and performance may be driven by co-optimization, integration, and functional diversification. Beyond-CMOS devices and architectures may provide promising technology options for ongoing improvement.

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An Introduction to SiC Power Devices: Status, Challenges, and Outlook

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In an increasingly electrified technology driven world, power electronics is central to the entire manufacturing economy. Silicon (Si) power devices have dominated power electronics due to their low cost volume production, excellent starting material quality, ease of processing, and proven reliability. Although Si power devices continue to make significant progress, they are approaching their operational limits primarily due to their relatively low bandgap and critical electric field that result in high conduction and switching losses, and poor high temperature performance.

Wide bandgap power semiconductor devices like Silicon Carbide (SiC) and the III-IV nitrides are currently in production for high power/temperature applications. Silicon carbide (SiC) is ideally suited for power switching due to its high critical electric field strength, its large bandgap, its excellent thermal conductivity, and its high saturated drift-velocity. For power devices, the tenfold increase in critical electric field strength of SiC relative to Si allows high voltage blocking layers to be fabricated significantly thinner than those of comparable Si devices. This reduces device on-state resistance and the associated conduction and switching losses, while maintaining the same high voltage blocking capability. Lower switching losses allow for high frequency operation, which decreases the size and weight of a system's passive components. The low specific on-state resistance enables high-current operation at a relatively low forward voltage drop at a given breakdown voltage. In addition, the wide bandgap of SiC allows operation at high temperatures, where conventional Si devices fail, with low leakage and reduced cooling system requirements. A graphical summary of Si, SiC, and GaN relevant material properties is shown in Fig. 1, [1].

To exploit SiC's compelling material properties in power devices, significant efforts started in the 1980s to develop high quality, low defect SiC substrates and epitaxy. Today, 150 mm SiC wafers are primarily used in the production of SiC devices. 200 mm wafers were demonstrated in 2015 and are expected to become commercially available from several vendors as early as 2022. It should be noted that conventional SiC substrate growth is more complex than that of Si requiring the use of large seeds and

high process temperatures. SiC substrates are mainly grown by the seeded sublimation technique, as schematically shown in Fig. 2.

The raw material, SiC powder, is placed at the bottom of a graphite crucible. A seed wafer is placed at the top of the crucible, which is heated by RF coils to a temperature of ~2500 °C. The seed wafer is kept at lower temperature than the SiC powder and the sublimed SiC species condensate and crystallize on the seed wafer. Reported sublimation growth rates are in the order of 0.5–2 mm/h. Increasing the growth rate can have the undesirable side effect of increased structural defect inclusion in the boule. SiC material's hardness, which is comparable to that of diamond, makes sawing and polishing SiC substrates slow and costly relative to Si.

The epitaxial active SiC device layer is grown by chemical vapor deposition (CVD) in horizontal or planetary reactors at 1500–1650 °C. Pressure typically ranges from 30 to 90 torr and growth rate can be as high as 46 mm/hr. The epitaxial growth is done on 4-degree off-cut substrates to maintain the polytype stability of the substrate. Breakdown voltage capability is dependent on the doping concentration and thickness of the epitaxial layer. For example, the optimal epitaxial values for 1200 V devices are a drift layer doping of 1 × 10^{16} cm^{-3} and a thickness of 10 μm. For 10 kV devices, the optimal values are 7 × 10^{14} cm^{-3} and 95 μm, respectively. Uniformity control of doping and thickness is crucial in ensuring high device yields. "Thinner" SiC epitaxial growth is well established and strives to minimize defect propagation from the substrate to the epitaxial layer. Growing the thicker epitaxial layers that enable high voltage devices is more complex and a subject of research and development efforts.

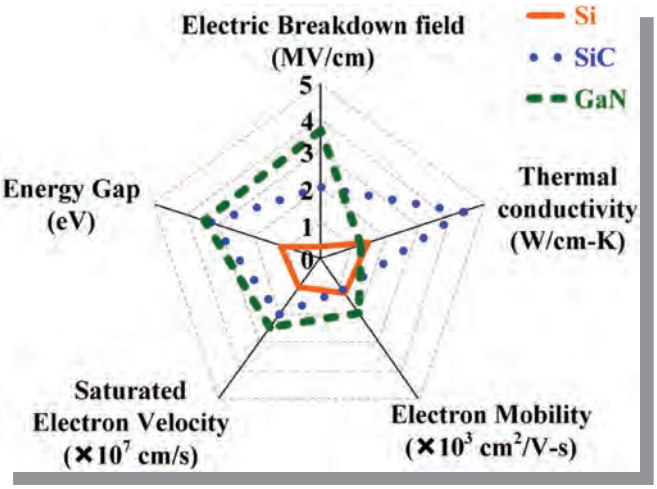

Figure 1. Graphical comparison of Si, SiC, and GaN material properties.

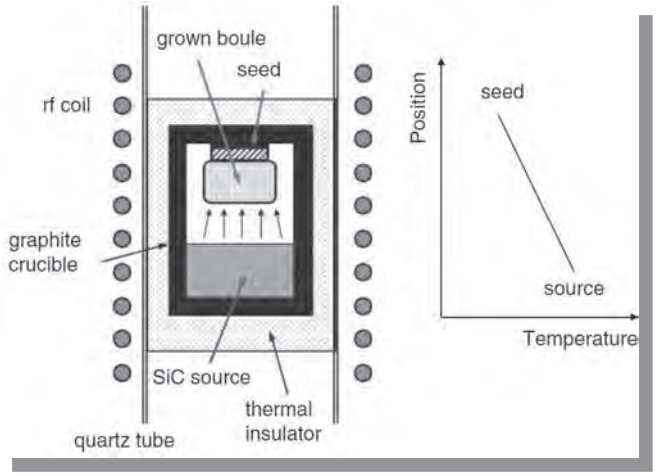

Figure 2. Schematic description of crucible for seeded sublimation growth of SiC substrates.

SiC Defects

Historically, killer defects limiting yield have been polytype inclusions and micropipes. These have practically been eliminated in commercial wafers. Micropipe density, which is detrimental to device operation, is typically below 0.1 cm^{-2}. Remaining structural defects are threading screw dislocations (300–600 cm^{-2}) that can increase reverse voltage leakage, threading edge dislocations (2000–5000 cm^{-2}) that are considered benign, and Basal-Plane-Dislocations (BPDs) (500–3000 cm^{-2}), which lead to device degradation under bipolar current flow. Although threading dislocations do result in measurable disturbances of epitaxial layer surface morphology, the practical effects of these disturbances on device performance and reliability are minimal [2]. BPDs are the major remaining "killer" defect impacting bipolar SiC devices as well as unipolar devices that conduct bipolar current during their operational cycle [3]. Basal plane dislocation defects are known to propagate from the wafer substrate through the thickness of the epitaxial layers where devices are fabricated. BPDs can also be generated during the high-temperature ion-implantation fabrication process. When bipolar current flows through a SiC transistor, electron–hole pair recombination at BPDs in the drift layer provides the energy to activate dislocation glides that give rise to stacking faults and degradation. To investigate the impact of BPDs on the electrical characteristics of _ion-implanted SiC transistors with 100–µm drift epilayers (10 kV rated), 17 JFETs of those specifications were stressed at a fixed gate-drain dc bipolar current density of 100 A/cm^2 for 5 hr. Representative curves are presented in Fig. 3 [4].

At 100 A/cm^2, the gate–drain *p-n* junction is turned on, as evidenced by the emission of blue/violet electroluminescence at the edges of the JFET (inset photograph of Fig. 3), and bipolar current flows. Of the 17 JFETs stressed, six exhibit no forward gate–drain voltage degradation, nine exhibit intermediate voltage

degradation, and two exhibit severe voltage degradation. Representative forward gate-drain voltages as a function of stress time curves, under the fixed 100-A/cm² dc bipolar stress, are shown in Fig. 3 for the three "voltage-degradation" cases. A measurement compliance of V_{GD} = 15 V is reached after 4 hr of bipolar injection for JFET 3–5. The forward/reverse gate-source, forward/reverse gate-drain, transfer, blocking voltage, and ON-state conduction electrical JFET characteristics are measured before and after the 5 hr bipolar-stressing period. Bipolar stress leads to forward gate–drain p-n junction and ON-state conduction degradations. Forward and reverse gate–source, transfer, reverse gate–drain, and blocking voltage JFET characteristics exhibit no degradation with bipolar stress.

Interestingly, transistor BPD-related electrical characteristic degradations can be fully reversed by annealing at 350 °C, while non-degraded characteristics remain unaffected by this annealing. Representative SiC JFET ON-state conduction, BPD-related degradation and full recovery by annealing are shown in Fig. 4 [4].

SiC Fabrication

For mass SiC commercialization, high yielding fabrication processes are required. Numerous well-established processes from silicon technology have been successfully transferred to SiC. However, SiC material properties necessitate development of specific

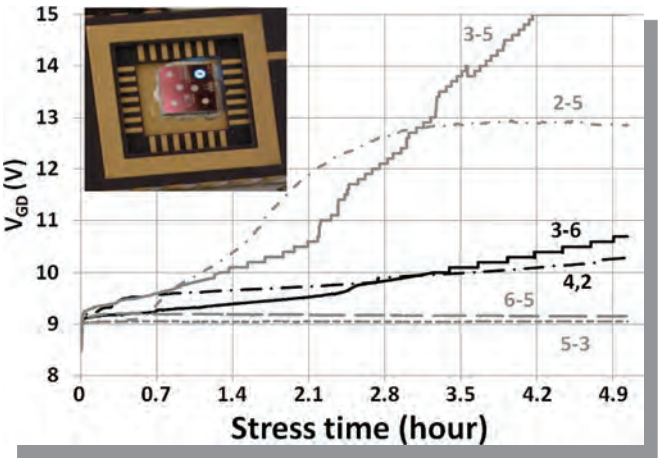

Figure 3. Representative SiC JFET forward gate–drain voltages as a function of time for a fixed dc 100-A/cm² gate–drain bipolar stress. The compliance is set at V_{GD} = 15 V. A biased JFET with its gate–drain diode's bipolar current giving rise to blue/violet electroluminescence is shown in the inset.

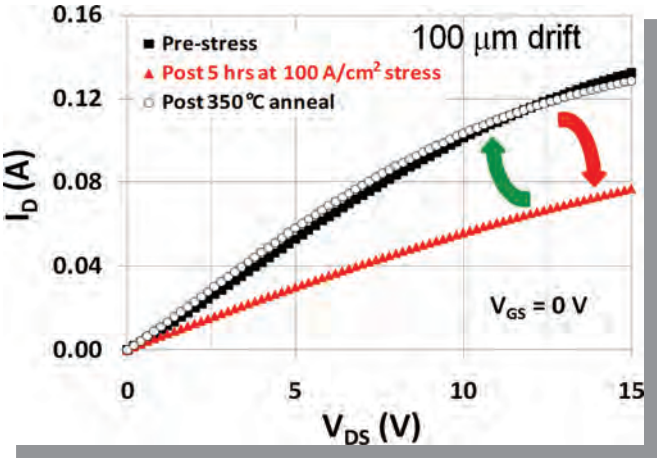

Figure 4. BPD-related SiC JFET ON-state conduction degradation and full recovery by annealing. The black squares, red triangles, and open circles represent the ON-state conduction electrical characteristics prior to bipolar stress, after 5 hours of 100-A/cm² bipolar stress, and after a 350 °C anneal, respectively.

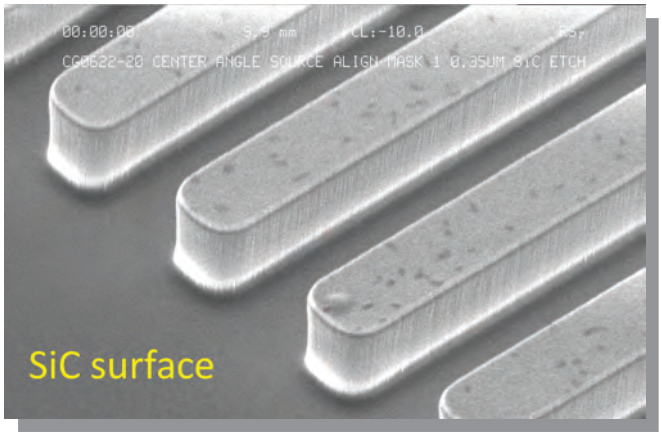

Figure 5. Reactive-ion etched 0.7 µm deep vertical SiC mesas using a Cr/Al mask.

processes, the parameters of which must be optimized and qualified [5]. SiC is inert against chemical solvents and only dry etching is practical. Furthermore, the hardness of SiC results in low photoresist selectivity and a "hard" mask, usually composed of metal or dielectrics, is required for SiC photolithographic patterning and etch. 0.7 µm deep SiC mesas, trenched using a "silicon" reactive-ion etch (RIE) tool and a Cr/Al mask, are shown in Fig. 5.

Cr assists with adhesion of metal layers to the underlying SiC surface. The RIE was fluorine-based for higher mask/SiC selectivity. RIE settings were optimized to eliminate micro-masking and achieve vertical etched sidewall profile formation.

Conventional thermal diffusion is not realistic in doping SiC due to its high melting point and the low diffusion constant of dopants within SiC. Heated ion-implantation is typically performed for doping densities of 10^{16}–10^{20} cm^{-3} (the higher doping densities assisting with ohmic contact formation), and room temperature implantation can work well for low implant doses (~10^{15} cm^{-3}). Nitrogen/Phosphorus and Aluminum are the preferred Impurities for n-type and p-type SiC doping, respectively. The as-implanted depth profiles are retained after the anneal for Al, P, and N as expected from their low diffusion constants. The lack of diffusion makes it easy to form shallow junctions and difficult to form deep ones. After ion implantation, a 1600–1800 °C anneal is performed

for lattice damage recovery, and high dopant electrical activation. A protective cap layer covering the SiC wafer protects its surface from degradation due to Si desorption and migration of surface atoms. Fig. 6 is a scanning electron microscopy image of a "post *p*+ ion-implantation" annealed wafer in the absence of a protective cap layer. The SiC wafer surface degrades due to Si desorption and migration of surface atoms. The wafer did not yield functional devices.

A wafer from the same fabrication lot, annealed simultaneously with that of Fig. 6 but with a carbon cap layer protecting its surface, exhibits excellent SiC morphology, Fig. 7, and high device yield. The high-energy ion-implantation bombardment signature is visible in the "nano-pits" of the implanted gate surface in Fig. 7.

The high value of the SiC/metal barrier results in rectifying metal contacts and post metal deposition anneal is required for ohmic contact formation. Typically, a 50–100 nm *Ni* layer is blanket deposited and patterned on the wafer for the simultaneous ohmic contact formation on the *n*-type and *p*-type doped regions, Fig. 8. Depending on the specifics of the fabrication process, isolating the source from the gate areas with dielectrics can facilitate high yields in the subsequent high temperature processing.

High temperature annealing of the *Ni* patterned wafer creates *Ni*-silicide for low resistivity ohmic contact formation. Rapid thermal annealing (RTA) at 950 °C, using standard silicon fabrication equipment, was used to create *Ni* silicide with no metal strings, Fig. 9. The dielectric isolates the source from the gate areas eliminating shorting during the high temperature silicide process.

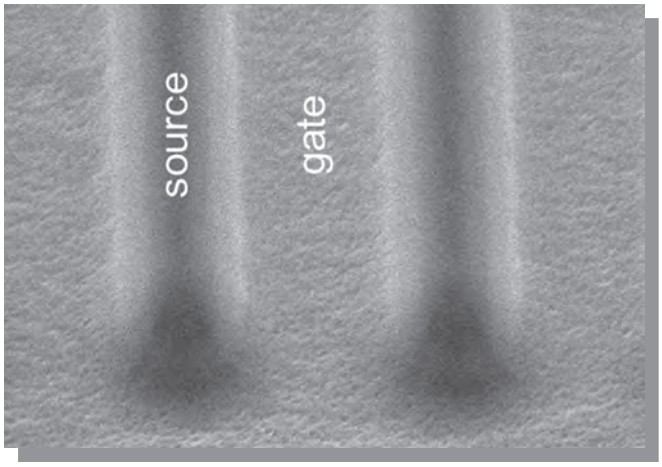

Figure 6. Scanning electron microscopy image of a "post p+ ion-implantation" annealed wafer in the absence of a protective cap layer. The SiC wafer surface has degraded due to Si desorption and migration of surface atoms.

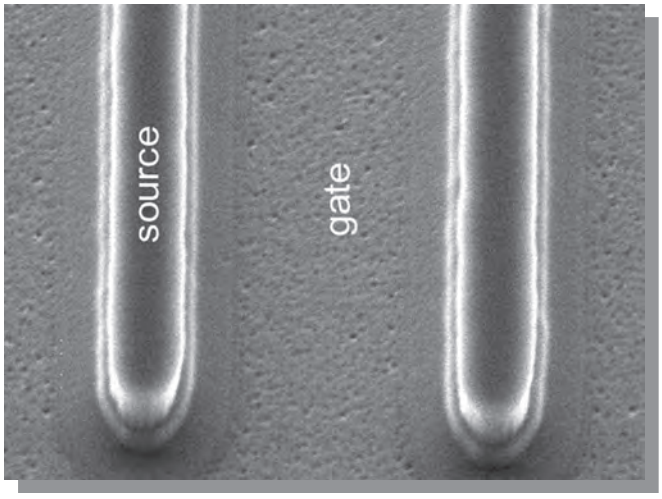

Figure 7. Scanning electron microscopy image of a "post p+ ion-implantation" annealed SiC wafer in the presence of a carbon protective cap layer. Excellent surface morphology and high device yield are attained.

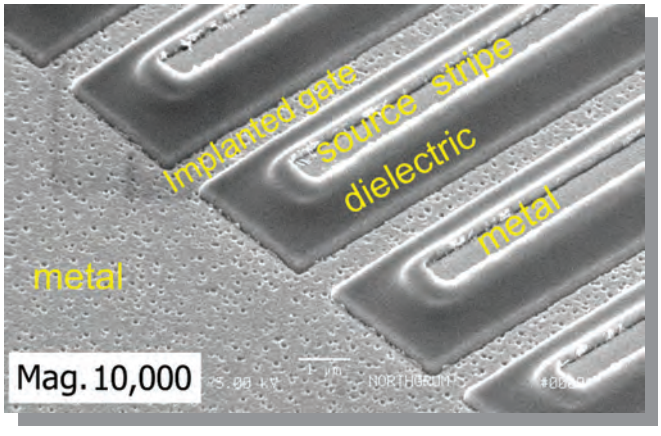

Figure 8. Scanning electron microscopy image of a patterned Ni layer on a SiC wafer surface. Dielectric isolates the metalized p+ implanted gate areas (pitted surface) from the n-doped source stripes.

Unlike Si wafers, SiC wafers are transparent. This complicates the use of "silicon" tools for CD-SEM and metrology measurements, as the focal plane is determined with the use of an optical microscope. SiC-specific wavelength metrology/inspection tools are now available from multiple vendors.

Another issue is the relative lack of flatness of SiC wafers, compared to those of Si, that can complicate photolithography. In addition, the high-temperature SiC processing can further degrade wafer flatness, occasionally rendering wafers unusable. This is particularly problematic with the thick epitaxy wafers used in +3.3 kV device fabrication. Efforts are underway to produce flatter starting SiC wafers, and to minimize flatness degradation during fabrication.

Lastly, the poor SiC/SiO_2 interface quality reduces inversion layer mobility, thus passivation techniques, including annealing in nitrides, are utilized to improve the SiC/SiO_2 interface quality. Furthermore, the high concentration of interface oxide traps leads to undesirable threshold voltage instability. A positive shift in threshold voltage increases conduction losses, while a negative threshold voltage

shift can lead to unintentional device turn-on.

SiC process integration technology has made significant advancements and optimizations are continuing. Today, SiC transistors are commercially available in the 650–1700 V range from multiple vendors.

Large Area SiC Transistors

To effectively compete with Si, large-area reliable and rugged SiC devices must be produced at competitive cost. Early proof-of-concept work paved the way for investments that contributed to SiC commercialization. In 2008, a 1680 V SiC JFET with an active area of 0.143 cm^2 (0.19 cm^2 total area) and an on-state current capability of 50 A was the largest transistor reported at the time, [6]. JFETs were soldered into "testing" packages and wire bonded using 10 mil (254 μm) diameter *Al* wires for electric characterization Fig. 10.

Room-temperature pulsed ON-state drain-current measurements were performed on packaged JFETs. The ON-state drain-current vs. voltage characteristics are shown in Fig. 11 at a gate bias range of 0 to 2.5V in steps of 0.5 V. To maintain voltage-control capability (high I_D/I_G gain), the gate must be biased below its 2.7 V built-in potential value. If the gate bias increases in excess of 2.7 V, significant gate current injection occurs into the channel of the JFET, and its current gain I_D/I_G degrades. At a gate-to-source bias of 2.5 V, the JFET outputs 53.6 A at a forward drain voltage drop of 2.08 V. The specific ON-state resistance is 5.5 m$\Omega \cdot cm^2$, and the transistor current gain is I_D/I_G = 26,800.

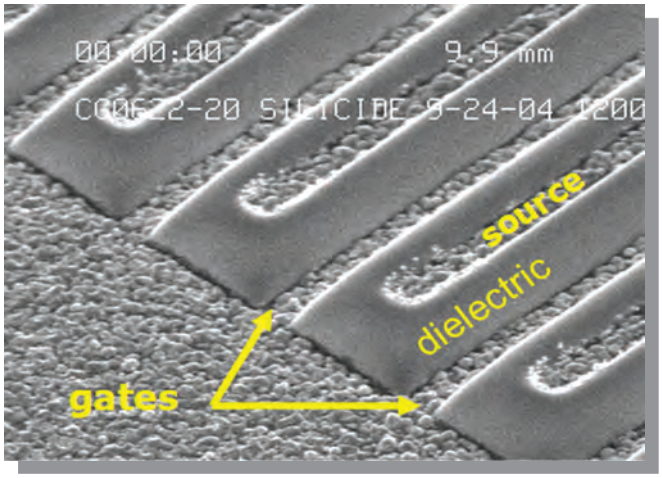

Figure 9. Scanning electron microscopy image of the Ni patterned SiC wafer of Fig. 8, after a 950 °C rapid-thermal-annealing event. Ni silicide is formed with no shorting of the p-gate to the n-source regions.

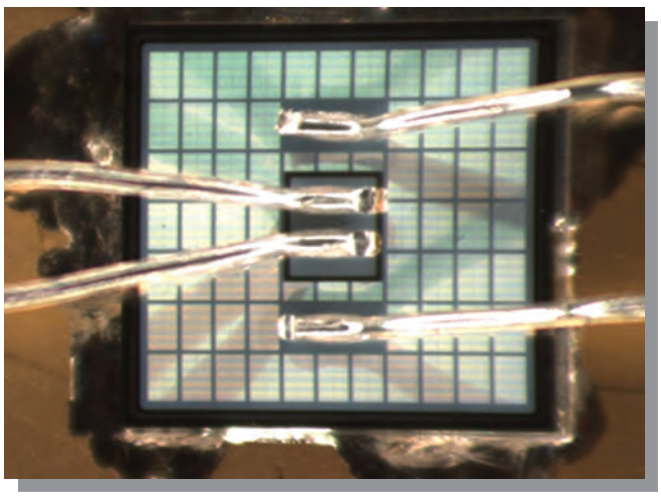

Fig. 10. Optical image of a 1680 V SiC JFET with an active area of 0.143 cm^2 (0.19 cm^2 total area) packaged for electrical characterization.

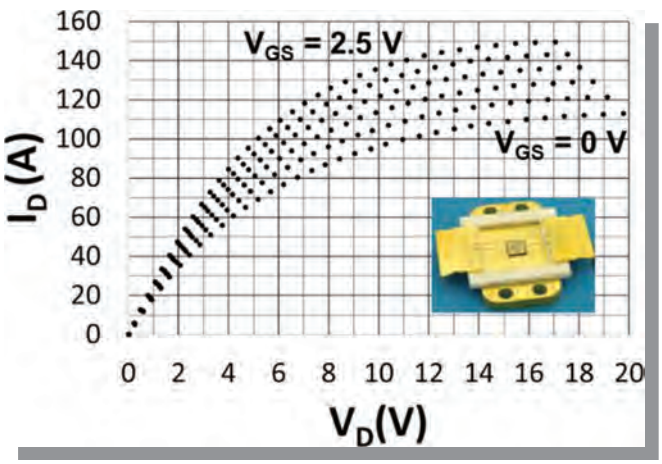

Figure 11. On-state drain current vs. voltage characteristics of a single 1680 V, 0.143 cm^2 packaged SiC JFET, at a gate bias range of 0 to 2.5V in steps of 0.5 V.

The blocking-voltage characteristics of the 0.143 cm^2 active area JFET at gate biases of –4 to –24 V, in steps of –2 V are shown in Fig. 12. At a gate-to-source bias of –24 V and a low drain–current density of 1 mA/cm^2 the JFET blocks 1680 V.

Specialized edge termination structures like *multiple junction termination extensions* and *floating guard rings* are fabricated to maximize the high-voltage performance [7]. The impact of edge termination in maximizing blocking voltage is graphically illustrated in Fig. 13. The blocking voltages of identical design and area SiC JFETs, fabricated next to each other on the same die of the same wafer, were measured. The JFETs had approximately equal resistance. One JFET was fabricated with a high performance floating guard ring edge termination while no edge termination was fabricated in the other. The former achieved a blocking voltage of 2022 V while the latter only blocked 450 V, Fig. 13. In short, a well-designed edge termination structure maximizes breakdown voltage with no associated increase in device resistance.

SiC Reliability and Ruggedness

Reliability and ruggedness demonstrations build confidence in SiC system insertion. An important contribution to SiC device reliability is reducing threshold-voltage

instability. In SiC MOSFETs, which are the dominant transistors in SiC-based power electronics applications, threshold-voltage instability is primarily due to the oxide traps at the SiC/gate-oxide interface. A positive shift in the SiC transistor's threshold voltage has the deleterious effect of increasing conduction losses, while a negative shift is undesirable as it can spontaneously turn the device on. To showcase the potential of SiC threshold-voltage stability, a JFET based all-SiC normally-off switch was implemented by combining a 1200 V normally-on (depletion mode) JFET with a low-voltage normally-off (enhancement mode) JFET in the cascode configuration [8]. To evaluate threshold voltage shift with temperature, the I_{DS}-V_{DS} characteristics of the all-SiC cascode switch were measured at junction temperatures of 25 °C, 100 °C, 200 °C and 300 °C and are shown in Fig. 14 [9]. The cascode's specific ON-state resistance was extracted from the data of Fig. 14 at V_{DS} = 0.5 V. The increase in ON-state resistance with temperature agrees well with the theoretical reduction of the 4H-SiC electron mobility.

Based on the JFET cascode's thermal measurements, the cascode threshold voltage was extracted and is plotted as a function of temperature on the left axis of the graph of Fig. 15.

The threshold voltage decreases from 1.6 V to 0.9 V as the temperature increases from 25 °C to 300 °C; the cascode switch remains normally-off at 300 °C. The cascode's gate-junction built-in potential variation with temperature was also extracted and plotted on the right axis of the graph of Fig. 15. As the temperature increases from 25 °C to 225 °C, the cascode's threshold voltage decreases by 0.54 V while its gate-junction built-in potential decreases by 0.52 V. This excellent agreement confirms that the decrease in cascode threshold voltage with temperature stems from the reduction of its gate-junction built-in potential as expected from theory. Thus, SiC JFETs, which have no gate oxides but rather use *pn* junctions to control the current flow

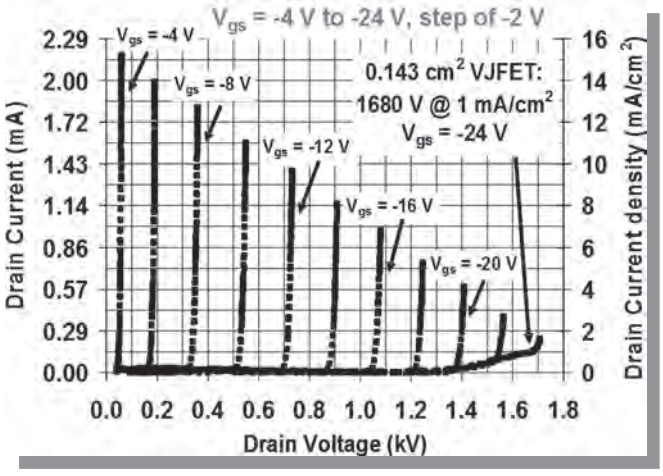

Figure 12. Blocking-voltage characteristics of the 0.143 cm² active area SiC JFET at gate biases of –4 to –24 V, in steps of –2 V. The JFET blocks 1680 V.

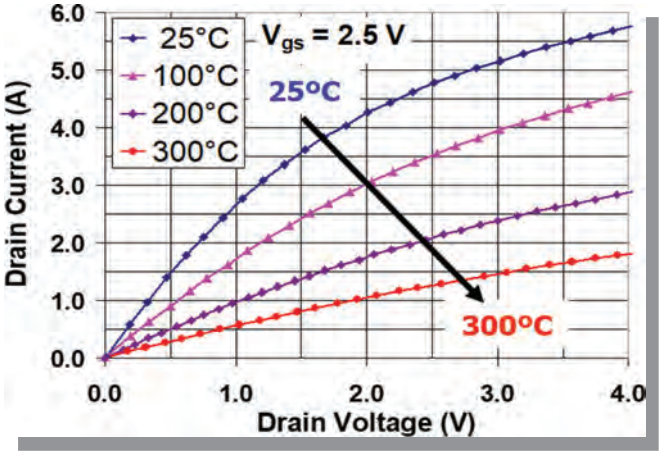

Figure 14. Temperature dependence of the SiC cascode's ON-state drain current at V_{GS} =2.5 V.

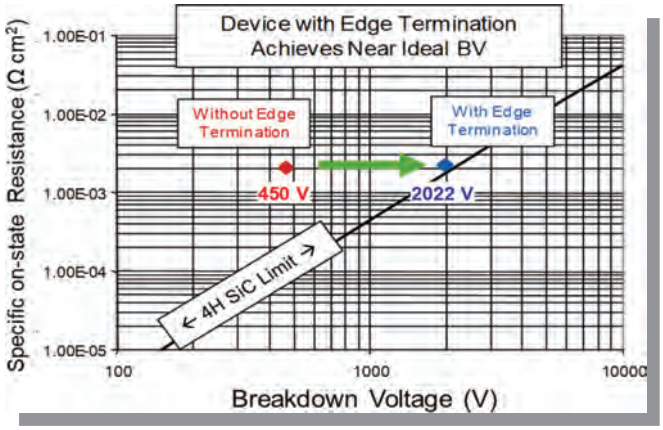

Figure 13. Blocking voltages of two SiC JFETs fabricated on the same die of the same wafer. Edge termination increases blocking voltage from 450 V to 2022 V with no associated increase in device resistance.

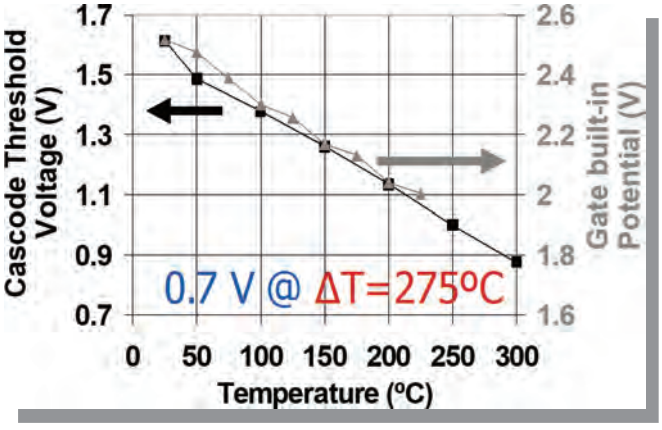

Figure 15. Temperature dependences of the SiC cascode's threshold-voltage (left axis) and gate-junction built-in potential (right axis). At a temperature swing of 275 °C, the threshold voltage only shifts by 0.7 V.

through their gates, have remarkably stable threshold voltages. As the quality of the SiC MOSFET gate oxide is being aggressively improved, similar threshold voltage stability is expected in the near future.

To demonstrate the ruggedness of SiC transistors, a SiC JFET was subjected to over 2.4 million 1200-V/115-A hard-switching events at what is 13 times its 150 °C rated current, Fig. 16 [10].

The JFET drain voltage is plotted in black (left axis) in Fig. 16; the current through the JFET is plotted in gray (right axis). By multiplying the JFET voltage by the current, the power dissipated by the JFET is calculated and plotted in the inset of Fig. 16. The energy dissipated by the JFET during each 1200-V/115-A switching transient is 73.2 mJ, and the peak dissipated power is 68.2 kW.

Figs. 17 and 18 show the ON-state current conduction and blocking voltage curves of the JFET before and after the 2.4 million 1200-V/115-A hard-switching events at 150 °C , respectively.

The black circles correspond to measurements taken prior to hard switching stressing. The gray circles represent measurements taken after the over 2.4 million hard switching events at 150 °C. As the JFET had not been subjected to burn-in stressing prior to the initiation of hard switch stressing, the slight improvement in the ON-state conduction JFET characteristics in Fig. 17 is attributed to burn-in effects stemming from the repetitive hard switching. The electrical characteristics do not degrade with stressing.

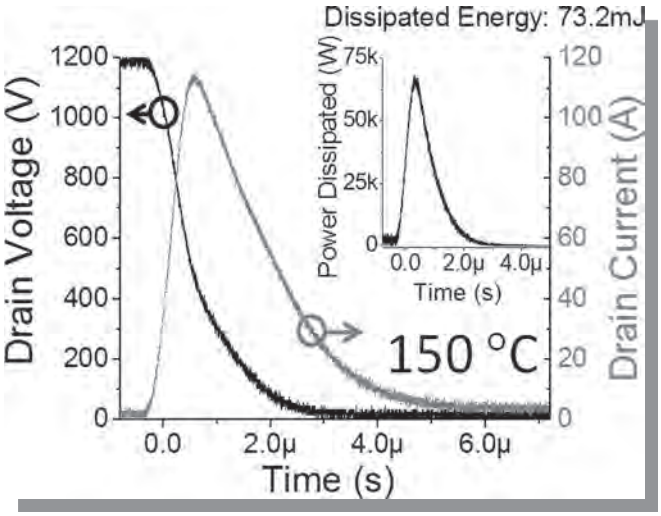

Figure 16. The 1200-V/115-A hard switching waveforms of the SiC JFET testing at 150 °C. The energy dissipated by the JFET during each hard switching event is 73.2 mJ (inset), and the peak dissipated power is 68.2 kW.

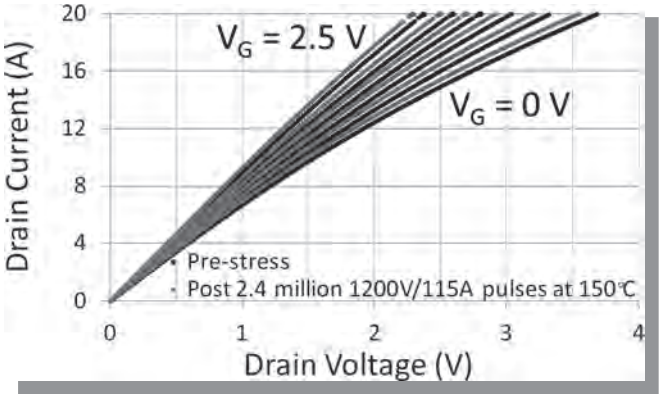

Figure 17. ON-state SiC JFET current conduction curves before (black circles) and after (gray circles) the over 2.4 million hard switching events at 150 °C. The slight improvement in JFET current conduction is attributed to burn-in of the JFET.

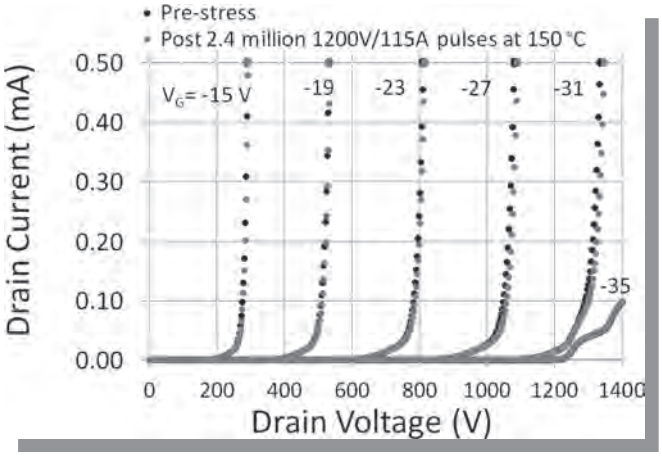

Figure 18. Blocking voltage SiC JFET curves before (black circles) and after (gray circles) more than 2.4 million hard-switching events at 150 °C and at 13 times the JFET's rated current. The blocking voltage characteristics are unchanged.

Therefore, the SiC transistor is rugged and operates reliably after the over 2.4 million hard switch stressing events at 13 times its 150 °C rated current.

SiC Schottky Barrier Diodes, planar and trench MOSFETs, and JFETs are commercially available as discrete components in the voltage range of 650 V to 1700 V from several US, European and Asian companies. Suppliers also provide modules with multiple transistors and high currents. 3.3 kV MOSFETs will become commercially available from large manufacturers as early as 2021. Historically, the 1200 V SiC MOSFET released by Cree in 2011 was the first commercially available SiC transistor [11]. Today, the SiC MOSFET is the dominant SiC switch used in power electronics and has steadily gained market share. However, high device cost, reliability/ruggedness concerns, and the need for a workforce trained in SiC system insertion are barriers to mass adoption. In several applications, like PV systems, insertion of SiC reduces overall system cost compared to Si, even though SiC devices cost 2–3 more than their Si counterparts. This is due to the passive component and cooling system simplifications enabled by SiC high frequency operation and properties. Nevertheless, reducing SiC device cost is highly desirable. The SiC wafer represents 50-70% of the overall SiC device cost, a consequence of the unique substrate fabrication specifics outlined in the discussion of Fig. 2. A SiC device cost reduction of over

20% is expected with the transition from 150 mm to 200 mm substrates. Further cost reductions can occur with SiC device manufacturing in fabs alongside Si. SiC devices fabricated in large Si volume fabs exploit economies of scale that lower cost. Through re-purposing older fully depreciated 150 mm and 200 mm Si foundries, SiC power devices can be manufactured with the relatively small investments necessary to support unique SiC processing steps like high temperature implantation and anneal, and ohmic contact formation. Minimizing fabrication cost by exploiting the mature Si volume production assumes the fab is loaded close to capacity with standard Si and SiC processes running on the same line. In addition, aggregating the demand for SiC substrates and epilayers in volume fabs contributes to lower material costs. Lower fabrication costs in a fully depreciated Si+SiC "capacity" loaded fab, coupled with decreased material costs leads to significant price reductions for SiC devices. This approach offers a new opportunity for outdated Si foundries, which have not kept up with the channel length reductions of the last two decades, to continue manufacturing legacy Si parts while ramping up SiC fabrication that requires relatively modest 0.3 micron design rules [12].

Progress in the areas of materials and cleanroom fabrication can result in device yield and reliability improvements. More planar wafers, reduction of BPDs and process-generated defects, and higher quality gate oxides that reduce threshold voltage instability are all being addressed. Valuable data is being accumulated over years of field operation and is analyzed to drive device optimization. Independent facilities that perform reliability analyses of SiC devices have been established and contribute to "SiC user confidence" [13]. SiC devices can be made more rugged by leveraging design trade-offs. This, combined with intelligent gate drives, can provide safe-operating-areas that rival those of Si. Finally, a workforce well trained in SiC power electronics is key in creating the large device demand that will spur mass manufacturing with its cost-lowering benefits. Entities like PowerAmerica carry out University/industry applied collaborative projects, offer industry-driven WBG short courses and tutorials at conferences, and match students with industrial internship opportunities [14]. These activities train the existing workforce and prepare the next generation of SiC technologists, facilitating accelerated deployment of SiC power electronics.

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A review of the 22nd International Vacuum Electronics Conference (IVEC)

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The 22nd edition of the International Vacuum Electronics Conference (www.ivec2021.org) was held in a virtual platform from the 27 to 30 April this year with the technical co-sponsorship of the IEEE EDS society. IVEC was created in the year 2000 by merging the US Power Tubes conferences and the European Space Agency TWTA Workshops.

Originally it was foreseen to hold this year's edition of the conference as a face-to-face event in the WTC conference center in Rotterdam, The Netherlands. Quite soon though it became clear that this was not going to be possible due to the restrictions in international travel and the event was converted into a fully virtual conference using the "Let's Get Digital" online platform.

By using the virtual platform, the organising committee was able to organise a conference which overcame the obstacles resulting from the worldwide travel restrictions and offered a highly interesting conference to all the participants.

To make the event a success, a novel conference concept was needed which combined the advantages of both in-person and virtual events. In this concept, there were three important aspects. First the conference should continue to focus on the established elements of IVEC like the plenary talks, the paper presentation sessions and the awards. Second, the conference should enable as much interaction between the participants as possible since this is the aspect which is inhibited the most in virtual conferences. Third, the conference should also have some novelties like the introduction of a new topic family, nano vacuum electronics.

With the new concept ready, the organisation could begin.

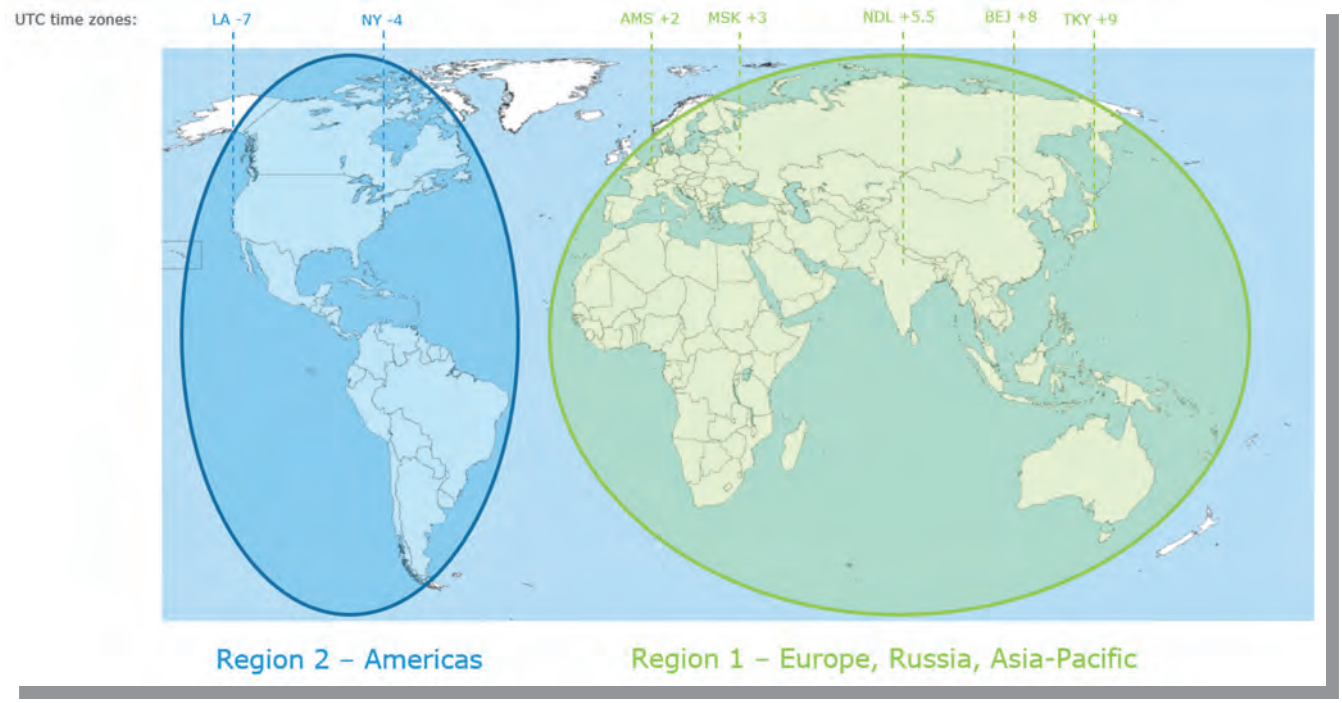
The first mentioned aspect was the most straightforward one, with the help of the technical programme committee, exactly 200 papers were accepted and a total of 20 oral paper presentation sessions could be put together. The topics of the sessions ranged from Traveling Wave Tubes over Thermionic Emission to Free Electron lasers and gave a good overview over the current research trends in the vacuum electronics community.

In addition to this, 4 plenary speakers gave more extensive talks about their current research and development projects. Yaxin Zhang from UESTC talked about *Terahertz Vacuum Electron Devices and Applications in High-Rate Communication and Imaging Systems*, Ernst Bosch from Thales lectured about *Electric propulsion—Game Changer for Satellites and New Possibilities for Applications*, Dimitris Pavlidis from the University of Florida gave an interesting talk about *Vacuum Nanoelectronics Based on Si and III-Nitride Semiconductors* and Erk Jensen from CERN gave an overview over *The Role of Vacuum Electronics in Future Particle Accelerators*.

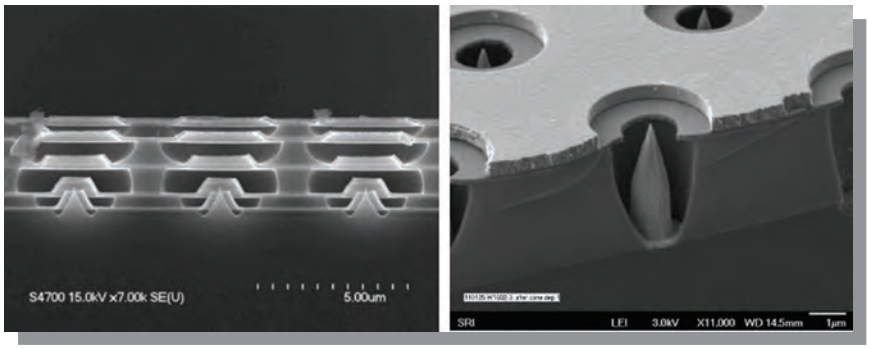
For everyone willing to extend their knowledge about vacuum electronics there were also a number of mini courses covering topics of general RF and vacuum electronics theory, manufacture and applications. Given that this year's IVEC was organised mainly by members of the European Space Agency, the selection of courses put part of the focus on the space applications of vacuum electronics.

The second aspect of the conference concept was the intention to create as much interaction between all the participants as possible.

With innovative ideas it was possible to get people from across the world to interact using all the means that the virtual conference platform offered. The elements of the live programme hereby closely followed a classical in-person scheduling. This meant that there were live opening and closing ceremonies, live plenary talks, live award ceremonies and one live keynote speech in each oral paper presentation session which were led by a live chairperson. On top of all of this there were live Q&A sessions that came along with each of the aforementioned parts. The recording of all the live content gave the participants an additional opportunity to follow or re-watch all the content at



Geographical regions introduced to facilitate attending IVEC 2021 by participants from different time zones



Examples of SEM images of devices presented at the vacuum nanoelectronics sessions

any time for a number of weeks after the end of the conference.

With participants coming from all over the world, it would have not been possible to set up a schedule that allowed for everyone to take part in all the live content. Instead it was decided to define two main geographical regions, one region being EU-Asia and the other region being the Americas. A distributed conference schedule was then set up with each live element taking place at a convenient time for either the EU-Asia region or the Americas region. This enabled people within each region to participate in part of the live program at times that were convenient for them, thus greatly increasing the interaction. Of course all participants could always join any session, even the ones scheduled at times more convenient to other regions. With this programme arrangement, the conference saw many interesting and fruitful discussions during the Q&A sessions of the plenaries and oral paper presentation sessions. As the live interactions between people are what keeps a scientific community alive, we believe that with this year's concept, IVEC could get as close as possible to an in-person event.

The third aspect of the conference concept was the introduction of a new topical group, nano vacuum electronics. Researchers from this up and coming field study special nanofabricated structures made mostly from semiconducting materials. Due to their size at nano-scale they are much smaller than the average free path length of electrons in air at ambient pressure. Therefore these devices behave as if they were placed in a vacuum, even though they are not. As a result, they exhibit properties of both classical vacuum electronics and solid state electronics. These structures can for example be integrated with a high density and at the same time be very tolerant to environmental effects like radiation, making them interesting for many different applications.

To put enough attention to this new topic and properly introduce it to the IVEC community, there was a mini-course focused on nano vacuum electronics for space applications by Jin-Woo Han from USRA NASA AMES research center. The plenary talk of Dimitris Pavlidis from

University of Florida focused also on this topic. With this and with enough submissions from the scientific community, one entire oral paper presentation session could be devoted to nano vacuum electronics.

Initially there was some uncertainty as to whether there would be a high interest in the conference even with the new digital platform since the previous year's IVEC had only taken place six months before. The reason for this was that the first wave of COVID-19 hit around the time that IVEC 2020 had been scheduled and the organisers were forced to move the event to a later date in order to be able to react to the changing situation.

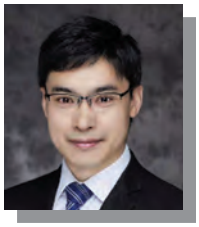
But with over 260 participants from 11 countries, this year's event was well-attended and showed the community's persistent interest in this conference even in its second year of going virtual.

Over the four days of the conference, there was a lot of active participation in all Q&A sessions, overall demonstrating that the conference concept showed the desired outcomes.

Thanks to the selection committees, the three awards traditionally awarded at IVEC went to researchers in recognition of their excellent scientific work.

Gun-Sik Park

This year's *John R. Pierce Award* was given out to Gun-Sik Park from Seoul National University for his outstanding contributions to vacuum electronics on a staggering number of different topics over many years.



Chao-Hai Du

The *Vacuum Electronics Young Scientist Award* was awarded to Prof. Chao-Hai Du from Peking University for his works on vacuum electronics theory, gyro-TWTs and frequency-tunable Gyrotrons.

After being presented the interesting works of the six finalists, the award panel selected Stephen Langellotti as the winner of this year's Best Student Paper Award with his paper on *Measurements of the Breakdown Threshold for Coaxial Multipactor and the Delay for Multipactor Onset*.

Last but not least, the organising committee wishes to express its deep gratitude to this year's sponsors, the IEEE EDS society and all the people that have contributed to the organisation of this year's event and helped carry it out. Special thanks go to this year's technical programme committee chaired by John Jelonnek and his co-chair Philippe Thouvenin and the IEEE EDS Vacuum Electronics Technical Committee chaired by Claudio Paoloni at the beginning and later by Monica Blank.

We are looking forward to meeting all of you at next year's IVEC 2022 in Monterey, California!

New Sources for Electron Device Content!
Visit the new EDS Resource Center, IEEEtv Channel and Instagram
Our Society now has three new online resources for technical content and society news!

EDS Resource Center – electron device educational content. The place to find short courses, technical panels, workshops, and more. Make this your first stop to find electron device technical training. New offerings added as they become available. Visit: https://resourcecenter.eds.ieee.org/. IEEE members enjoy discounted pricing, and EDS members have access for FREE! **Join IEEE and EDS** today to get discounted pricing.

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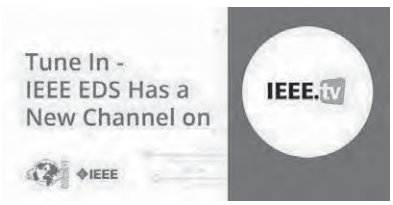

IEEE International Electron Devices Meeting Announces

2021 Call for Papers

IEDM 2021 will feature special Focus Sessions on the following topics:

- *Stacking of Devices, Circuits, Chips: Design, Fabrication and Metrology Challenges and Opportunities*
- *STCO for Memory-Centric Computing and 3D Integration*
- *Device Technology for Quantum Computing*
- *Topological Materials, Devices and Systems*
- *Technologies for AR/VR and Intelligent Sensors*

Under the theme "Devices for a New Era of Electronics: From 2D Materials to 3D Architectures," the 67th annual IEEE International Electron Devices Meeting (IEDM) has issued a Call for Papers seeking the world's best original work in all areas of microelectronics research and development.

The 2021 IEDM is being planned as an in-person conference 11–15 December 2021 at the Hilton San Francisco Union Square hotel, with on-demand access after the event for those who are unable to travel due to COVID-19 restrictions.

The paper submission deadline is Friday, 23 July 2021. Authors are asked to submit four-page camera-ready papers. Accepted papers will be published as-is in the proceedings. A few late-news papers also will be accepted, covering only the most recent and noteworthy developments. The late-news submission deadline is 30 August 2021.

The IEDM is the premier forum for technological breakthroughs in semiconductor and related device technology, manufacturing, design, physics and modeling. Each year, the world's leading technologists gather to participate in a technical program of more than 220 presentations, plus panels, focus sessions, tutorials, short courses, supplier exhibits, IEEE/EDS award presentations and other events highlighting the industry's best work.

Planned as an in-person conference with on-demand access to content after the event. . .

"IEDM is currently being planned as an in-person event in San Francisco in December with on-demand access to content available after the event, although meeting plans are subject to change to stay in compliance with COVID-19 guidelines," said Meng-Fan (Marvin) Chang, IEDM 2021 Publicity Chair and IEEE Fellow, Distinguished Professor of Electrical Engineering at National Tsing Hua University, and Director of Corporate Research at TSMC. "Should an in-person meeting not be feasible, IEDM will go fully virtual. Additional details will be made available later this year."

"Our theme this year was chosen to emphasize the many changes sweeping across the electronics industry and the diverse technologies that are enabling them," said Srabanti Chowdhury, IEDM 2021 Publicity Vice Chair and Associate Professor of Electrical Engineering at Stanford University. "IEDM 2021 will continue its long tradition of having a rich technical program full of relevant, state-of-the-art results, and the conference will give attendees the opportunity to interact with colleagues from academia and industry around the world."

IEDM 2021 encourages submissions in all areas, with special emphasis on:

- Neuromorphic computing/AI
- Quantum computing devices
- Devices for RF, 5G, THz and mmWave applications
- Advanced memory technologies
- Technologies for advanced logic nodes
- Non-charge-based devices and systems
- Advanced power devices, modules and systems
- Sensors, MEMS and bioelectronics
- Package-device level interactions
- Electron device simulation and modeling
- Robustness/security of electronic circuits and systems
- Optoelectronics, displays and imaging systems

The IEDM 2021 technical subcommittees are as follows:

- Advanced Logic Technology (ALT)
- Emerging Device and Compute Technology (EDT)
- Memory Technology (MT)
- Microwave, Millimeter Wave and Analog Technology (MAT)
- Modeling and Simulation (MS)
- Optoelectronics, Displays and Imaging Systems (ODI)
- Power Devices and Systems (PDS)

- Reliability of Systems and Devices (RSD)
- Sensors, MEMS and Bioelectronics (SMB)

Further Information
For more information, visit the IEDM 2021 home page at www.ieee-iedm.org.

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2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)

The 2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS) will be taking place in beautiful Monterey, California during 5–8 December, and is the 4th year of the successful merger between the original Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) and the Compound Semiconductor IC Symposium (CSICS). BCICTS is the premier forum for the presentation and discussion of the latest developments in bipolar, BiCMOS, and compound semiconductor circuits, devices, and technology. Coverage includes all aspects of these technologies, from materials, device fabrication, device phenomena, TCAD modeling, compact modeling, integrated circuit design, testing, and system applications. A wide range of integrated circuit technologies are covered, including bipolar and field- effect transistors realized in materials such as SiGe, GaAs, GaN, InP, SiC. The latest results in wireless, analog, RF, microwave, high-speed digital, mixed signal, optoelectronic, millimeter wave, and THz integrated circuits are embraced.

The conference itself will take place at the Monterey Marriott, near the many interesting sites located in the city of Monterey, including the Monterey Bay Aquarium, which displays thousands of marine animals and plants in both underwater and interactive exhibits, and both Old Fisherman's Wharf and Cannery Row, with their converted landmark buildings housing popular dining, shopping, and entertainment options. The Monterey Peninsula where the city is situated boasts spectacular views of the Pacific coast and ocean, with numerous options for hiking and exploring, and is also home to the internationally renowned Pebble Beach golf course.

PHOTO CREDIT: BIXBY CREEK BRIDGE OUTSIDE OF MONTEREY, CALIFORNIA

The technical committee for BCICTS has lined up an exciting and informative array of speakers for the 2021 conference, which will begin with a series of short courses on Sunday, 5 December, "Measurement techniques for mm-wave device and circuit on wafer characterization" including On-wafer mm-wave measurement principles and equipment modules; On-wafer calibration techniques for mm-wave characterization; Pulsed DC and S-parameter measurements; Large-signal on-wafer measurement techniques taught by internationally renowned experts of their field. Monday, 6 December will begin with a primer in the morning on "Circuits and Technologies for High-Speed Optical Links," taught by Sorin Voinigescu, from the University of Toronto, before the Plenary and contributing sessions begin. Anchoring the contributing sessions will be more than ten invited talks arranged by the technical sub-committees of BCICTS. These invited talks are representative of the wide range of topics and subject matter experts that the BCICTS conference brings together, a diversity and depth of synergistic knowledge covering the latest topics and advances in the rapidly progressing field of semiconductor technology and circuits unmatched by any other conference. For registration and up to date information, including a listing of the researchers who are scheduled to give an invited talk and their respective topics for this year's conference, please visit the BCICTS website at www.bcicts.org. The members of the BICICTS organizing committee cordially invite you to join us there!

Doug Weiser
BCICTS Publicity Chair
2021 IEEE BCICTS Organizing Committee

Mid-Year Board of Governors Meeting–2021

MK Radhakrishnan
EDS Secretary

In the midst of the fluctuating pandemic crisis, the mid-year meeting of EDS Board of Governors was organized virtually on 29 and 30 May 2021 using Cisco Webex with support of EDS staff. As a virtual meeting, the schedule was limited to three hours from 9.00–12.00 US Eastern Time on both days but incorporating all the presentations as usual. The meeting was attended by almost all elected members of the BoG and EDS Forum members joining online from countries far and wide at different time zones.

EDS President, Ravi Todi welcomed the online attendees and informed that the meeting would have presentations by all the VPs and others scheduled in the agenda but limited to 10 minutes each. Ravi presented the major highlights including the overall summary of the activities in 2020–21 and the successful culmination of the year 2020 with most of the technical activities going virtual but with a high financial operating margin. The Q&A was managed with questions and comments via chat box and email. All the motions were presented, and the voting will take place via email after the meeting. All the presentations were made available along with the EDS BoG Agenda link in advance, which allowed everyone to go through the presentations prior to the meeting. Highlights of the presentations and deliberations include the following.

Bin Zhao, EDS Treasurer, presented the financial status, reporting a surplus of $2654K in 2020, 50% of which can be utilized for new initiatives. The budget for 2021 has been revised considering the operational constraints due to the pandemic situation. The project spending in 2020 was $519K which includes 10 projects in 3% category and 16 new initiatives in 50% spending category. This is expected to be $540K for 2021 consisting of 5 and 22 projects in 3% and 50% category each. As such the total project spending for these two years may reach $1.06 M.

Out of the 17 financially sponsored conferences of EDS, 11 may go as virtual or hybrid mode in 2021 along with many in the technical co-sponsorship category, as reported by the VP of Meetings Kazunari Ishimaru. Pandemic impact on organizing conferences is still high resulting in cancellation or postponement of some events. EDTM 2021 held at Chengdu, China as a hybrid event was a success both in technical presentations and attendance of over 500 participants. Kazunari reported that the Women in Engineering committee in EDS is getting shape with dedicated volunteers and specific programs and events associated with conferences.

EDS VP of Education, Navakanta Bhat reported that the webinars organized during this pandemic period are very successful with at least one event in every two weeks. EDS summer school request for 2021 had 9 excellent proposals and 4 Chapters from R1, R9 and R10 were selected. EDS certification program and short courses has been initiated and 3 lectures completed with first course by Prof. Jayant Baliga and more recordings are planned for 2021. Podcasts of interviews with EDS luminaries is the new initiative and 12 such episodes are now available. EDS-ETC Robotics program in Malaysia was a successful event.

John Dallesasse, VP for Technical Committees, presented the summary of activities for the 14 TCs in EDS. With 138 TC members altogether, all these TCs are active with short courses, webinars, support to conferences and MQs and special issues in EDS journals. A new Technical Committee on Neuromorphic Computing is in the process of initiation in the lines of EDS strategic interests for which a motion has been presented to BoG for voting. Another new TC on Quantum Computing is being discussed. A major task by the end of 2021 is to identify and recruit few new committee members including chairs in place of outgoing members.

EDS VP Publications & Products, Joachim Burghartz informed that all EDS journals (TED, EDL and J-EDS) were healthy during the pandemic year with increase in related revenues. The IEEE Journal on Flexible Electronics (J-FLE), a new journal co-sponsored by EDS, SSC and CAS, is being initiated and the steering committee is in search for EiC. A motion for the new journal Transactions on Display Technology is being submitted. Publication awards for best papers in TED (Paul Rappaport Award), EDL (George Smith Award) and J-EDS (Leo Esaki Award) in the year 2020 have been announced.

Murty Polavarapu, VP Regions and Chapters, reported that EDS has 220 chapters at present with 6 new chapters during first half of 2021. Focused training for Chapter leaders were provided during 1Q of 2021, especially on using vTools and OU Analytics. There are 245 Chapter meetings reported to-date and Chapter subsidies for 2021 distributed. MQs were organized

in open, virtual and hybrid formats. DL roster has been updated. Calls for new DL nominations in targeted topical areas have been invited. Annual Chapter summit has been planned. EDS Chapter operations manual to be updated.

Patrick Fay, VP for Membership presented the overall EDS membership growth trends for recent years. An upward swing of 4.5% in the membership compared to April 2020 has been reported. However, excluding the undergraduate memberships the growth is negative in all regions. Various activities are currently undertaken to address issues of membership, which includes membership fee subsidy program, complimentary membership offers and additional publicity. Through YP, networking at conferences and mentor match programs membership enhancement is planned.

Strategic Directions VP, Paul Berger presented a plan for Strategic goals for EDS growth, especially to develop students and young professionals through a multifaceted planning. This include (i) update and upgradation of information through publications, conferences, and webinars, (ii) equitability fostering diverse and inclusive communities to facilitate information exchange, (iii) address sustainable development goals through humanitarian engineering and (iv) develop synergetic relationships through strategic alliances. The procedures are being developed to include in C&B through an appropriate motion in the next phase.

Young Professionals Committee report was presented by Camilo Velez, Committee Chair. The Committee is engaged in organizing YP events at different conferences. Mentoring YPs and how to navigate academia and industry in a virtual world is the theme of the networking event at the VLSI Symposium. YP Committee raised a concern about clarity in funding mechanisms for local YP activities.

Fernando Guarin, EDS Awards/Nominations and Elections Chair informed the status of awards and nominations including the 2021 BoG and officer elections. As EDS Humanitarian Activities Chair, Fernando explained various activities including those organized in conjunction with EDS conferences and projects. Samar Saha, EDS Fellow Committee Chair reported that 44 nominations were received this year and the review was organized by virtual meeting of the Committee. EDS Secretary's report and Newsletter Status was presented by MK Radhakrishnan, EDS Secretary & Newsletter Oversight Committee Chair. Newsletter EiCs are organizing WebEx meetings with Regional Editors and SRC Chairs and Vice Chairs to have more visibility of Chapters through Newsletter. Regular sections on WIE and YP were initiated in the April issue to provide a new and emphatic representation of professionals.

The 2022 mid-year BoG meeting is planned to be in Hawaii in conjunction with VLSI conference in June.

The two days virtual meeting was concluded on time. Ravi Todi thanked all the participants and attendees around the globe, and adjourned the mid-year BoG meeting.

MK Radhakrishnan
IEEE EDS Secretary

Message from EDS Newsletter Editor-in-Chief

Daniel Tomaszewski
EDS Newsletter
Editor-in-Chief

Dear Readers, Members of the IEEE EDS Community, Welcome to the IEEE EDS Newsletter issue July 2021. I do hope you are all healthy and in good shape.

The issue brings You interesting Technical Briefs. Among them you may read the next installment of the series based on the IRDS IFT reports. This article concerns the "Beyond CMOS" topic. Next, please find the article reporting achievements in technologies of SiC material and devices which demonstrate superb features for high voltage/high current electronics. The third Technical Brief contains highlights of the 22nd Int. Vacuum Electronics Conference (IVEC 2021) held in a virtual mode like many other technical events worldwide. Indeed, the COVID-19 pandemic still strongly affects our life and brings numerous challenges for activities of our and other societies. Nevertheless, I am very glad to have the IVEC report in the EDS Newsletter again after a pretty long break. In this issue we also announce two important technical conferences that will be held this year, namely BCICTS 2021, and IEDM 2021.

Thanks to the excellent work of Manoj Saxena, we can present further interesting materials in the sections EDS Women in Engineering (EDS WiE) and EDS Young Professionals (EDS YP). The WiE section includes an overview of the event organized by ED Malaysia Chapter, devoted to women activity in engineering. It is worthwhile to mention that these events have been initiated by Kazunari Ishimaru, IEEE EDS Vice-President of Meetings & Conferences. I am looking forward to the next successful meetings from this series. Except for this, you may find in this section two articles presenting women who are

outstanding researchers in the field of electron devices.

The YP section presents excerpts of interviews that Manoj made with two young researchers—Early Career Award recipients. It is interesting to read their thoughts concerning the present work and plans for the future. In the near future they will decide and determine the shape of the EDS.

We also try to put more attention on the humanitarian activities of EDS. Please, find in this issue a short article on such a project carried out in India. In the Chapter News and in the Regional News you may find as always articles on daily work of the chapters. I regret to say that we have a low number of contributions in Regional News. This problem was noticed at the last BoG meeting. Together with the Committee of Regions and Chapters we will try to address the issue.

I also would like to introduce three new members of the EDS Newsletter editorial team. Prof. Tuo-Hung (Alex) Hou from National Chiao Tung University, Hsinchu, Taiwan, has been appointed the Regional Editor for Region 10—North and East Asia. Prof. Paula Ghedini Der Agopian from Sao Paulo State University has been appointed the Regional Editor for Region 9—Latin America South. Prof. Joel Molina Reyes from the National Institute of Astrophysics, Optics and Electronics, Puebla, has been appointed the Regional Editor for Region 9—Latin America North. As you can see, due to an increasing number of EDS Chapters in Region 9 we now have two Regional Editors for Latin America. It is my great pleasure to welcome them and wish a fruitful work for the EDS Newsletter. At this point, I would like to thank the outgoing regional editors Ming Liu and Edmundo A. Gutiérrez D. for their dedication and excellent work, and wish them many successes at their highly responsible professional positions.

Tuo-Hung (Alex) Hou, EDS Newsletter Regional Editor

Paula Ghedini Der Agopian, EDS Newsletter Regional Editor

Joel Molina Reyes, EDS Newsletter Regional Editor

With these appointments we have reached the stable Editorial Team for around two years.

Dear Readers, if you have any suggestions, comments regarding the Newsletter contents, please do not hesitate to contact me or Manoj Saxena. We will be very glad to receive your feedback.

Finally, I would like to express my thanks to all the Authors of articles in this issue, to the Regional Editors and all the members of the Editorial Team.

Have a great summer time and stay safe.

Sincerely,
Daniel Tomaszewski

Call for Nominations—EDS Board of Governors

Fernando Guarin EDS Nominations & Elections Chair

The IEEE Electron Devices Society invites nominations for election to its Board of Governors—BoG (formerly AdCom) members-at-large. The next election will be held after the BoG meeting on Sunday, 12 December 2021. This year, seven out of the twenty-two members will be elected for a 3-year term, with a maximum of two terms.

A member can only serve for a maximum of two terms as a BoG member in a lifetime. Therefore, the eligibility will be verified for all nominees who will be voted on by the EDS BoG. All electees begin their term in office on 1 January 2022. The nominees need not be present to run for the election.

Any EDS member who has served for a minimum of one year as an EDS Officer, Vice-President, Standing and Technical Committee Chair/Member, Publication Editor and Chapter Chair is eligible to be nominated, unless otherwise precluded from doing so in the EDS Constitution and Bylaws. The electees are required to attend at least one BoG meeting every year. While the December meeting is organized in conjunction with the IEEE International Electron Devices Meeting, the mid-year meeting is frequently held outside the US. Partial travel support is available to attend BoG meetings.

All nominees must be endorsed by one BoG member, i.e., one of the four officers (President, President-Elect, Treasurer or Secretary), the Jr. or Sr. Past President, or one of the

22 current BoG Members-at-Large. It is the responsibility of the nominators and the endorsers to make sure that, if elected, the nominee is willing to actively serve in the position as a BoG member-at-large.

Please submit your EDS BoG nomination by 15 October 2021, using the online nomination form at: (https://ieeeforms.wufoo.com/forms/k4vnyad0ys3o4z/).

Also, all endorsements letters should be submitted using the online form: https://ieeeforms.wufoo.com/forms/q1d5l2jz1pps20g/ by 15 October 2021.

If you have any questions, please feel free to contact Laura Riello (l.riello@ieee.org) with a copy to me at fernando.guarin@ieee.org

Fernando Guarin
Chair of EDS Nominations & Elections

EDS Board of Governors (BoG) Members-at-Large Election Process

The Members-at-Large (MAL) of the EDS Board of Governors (BoG) are elected for staggered 3-year terms. The EDS Constitution and Bylaws mandates the number of elected MAL to be a total of 22 members with at least two members from each of the following geographic areas: Regions 1–7 and 9; Region 8; and Region 10. Our Constitution and Bylaws also require that at least one elected BoG member is a Young Professional (YP). A Young Professional member is defined by IEEE as a member who graduated with his/her first professional degree within the last fifteen years. It is also required that there is at least a slate of nominees for members-at-large comprising a minimum of 1.5 times the number of vacancies to occur on the BoG. We also have a two-term lifetime limit for a volunteer to serve as a BoG Member-at-Large, which must be considered for nominations. All nominees will be voted on by the EDS BoG at its December 2021 meeting. All electees begin their term in office on 1 January 2022. The nominees need not be present to run for the election. In 2021, seven positions will be filled.

The election procedure begins with the announcement of Call for Nominations in the *EDS Newsletter*. The slate of nominees is developed by the EDS Nominations & Elections Committee. Nominees are asked to submit a two-page biographical resume and an optional 50 word personal statement in a standard format.

Any EDS member who has served for a minimum of one year as an EDS Officer, Vice-President, Standing and Technical Committee Chair/Member, Publication Editor or Chapter Chair is eligible to be nominated, unless otherwise precluded from doing so in the EDS Bylaws. All nominees must be endorsed by one BoG member, i.e., one of the four officers (President, President-Elect, Treasurer or Secretary), the Jr. or Sr. Past President or one of the 22 current BoG MAL. Self-nomination is allowed. Endorsers should submit their online endorsement form by the deadline. Please note that there is no limit to the number of candidates that a full voting BoG member can endorse.

The deadline for Nominations will be 15 October 2021. The biographical resumes and endorsement letters will be distributed to the BoG prior to the December BoG meeting. The election will be held after the conclusion of the BoG meeting on 11 December 2021.

Fernando Guarin
Chair EDS of Nominations & Elections

2021 IEEE William Cherry Award Presented at the 48th IEEE PVSC to Professor Thorsten Trupke

Thorsten Trupke is a Professor at the School for Photovoltaic and Renewable Energy Engineering at the University of New South Wales where he leads a team of approximately 15 Ph.D students, Postdoctoral Fellows and staff. He is also Chief Technology Officer and co-founder of Sydney based company BT imaging and a Fellow of the Australian Academy of Technology and Engineering.

Thorsten holds a Ph.D in Physics from the University of Karlsruhe, Germany, which he completed under the supervision and guidance of Professor Peter Würfel. In 2001 he moved with his family (Thorsten is married with four children) from Germany to Australia, to join Prof Martin Green's new Centre for Third Generation Photovoltaics at UNSW, supported by a Feodor Lynen Fellowship provided by the Alexander von Humboldt Foundation. He proposed the concepts of combining conventional solar cells with up and/or down-conversion including limiting efficiency calculations and experimental proof of concept studies. In 2004 Thorsten joined forces with Dr Robert Bardos to develop novel luminescence-based characterization methods and systems, including QSS-Photoluminescence lifetime measurements and Suns-Photoluminescence. His most impactful contribution to date has arguably been the development of photoluminescence imaging for silicon wafers and solar cells, first demonstrated by Thorsten and Robert at UNSW in 2005. This measurement principle, and a large number of associated analysis methods, have since then become standard tools used by researchers and in PV production on a daily basis. The ability to detect a wide range of device and material defects accurately and quickly from PL images has contributed substantially to the rapid improvement and cost reduction of silicon solar cell technology over the last ten years. His team at UNSW continues to drive this technology and the associated fundamental device physics forward, recently with emphasis on downstream applications for outdoor module testing.

Thorsten Trupke, 2021 IEEE William R. Cherry Award Winner

Thorsten co-founded BT imaging in 2008, the company provides PL imaging systems to the R&D community and to wafer and solar cell manufacturers. PL tools by BT imaging are found in most R&D labs and in high volume manufacturing worldwide. He enjoys his dual roles in academia and in the industry and the resulting opportunities to work with optimistic colleagues and friends to turn fundamental and innovative research into real world applications and products.

In his private life Thorsten's favorite pastime is ocean swimming, he spends considerable time in the waters surrounding the beautiful coastline around Sydney.

About the Award

This award is named in honor of William R. Cherry, a founder of the photovoltaic community. In the 1950's, he was instrumental in establishing solar cells as the ideal power source for space satellites and for recognizing, advocating, and nurturing the use of photovoltaic systems for terrestrial applications. The William R. Cherry award was instituted in 1980, shortly after his death. The purpose of the award is to recognize an individual engineer or scientist who devoted a part of their professional life to the advancement of the science and technology of photovoltaic energy conversion. The nominee must have made significant contributions to the science and/or technology of PV energy conversion, with dissemination by substantial publications and presentations. Professional society activities, promotional and/or organizational efforts and achievements are not considerations in the election for the award.

2021 EDS Chapter of the Year Award—Call for Nominations

The IEEE EDS Chapter of the Year Award is given each year based on the quantity and quality of the activities and programs implemented by the chapters during the prior July 1st–June 30th period (for 2022 subsidies—activities and programs between 1 July 2020 and 30 June 2021). Virtual events can also be included.

The society recently changed the EDS Chapter of the Year Award to give it to one non-student chapter and one student chapter in any geographic location.

Nominations for the awards can only be made by Regions/Chapters Committee Members, SRC Chairs/Vice-Chairs, or self-nominated by Chapter Chairs. Please visit the EDS website to submit your nomination form (https://eds.ieee.org/awards/chapter-of-the-year-award).

Each year, the winning chapters (maximum 2) will receive a plaque and check for $500 to be presented at an EDS chapter meeting of their choice. Travel reimbursement will not be provided. A chapter that has previously received the EDS Chapter of the Year Award is eligible for re-nomination only after three years from the year of award.

The schedule for the award process is as follows:

Action	Date
Call for nominations emailed to Chapter Chairs, SRC Chairs, SRC Vice-Chairs and Regions/Chapters Committee	1 June
Deadline for nominations	15 September
Regions/Chapters Committee and SRC Chairs & Vice Chairs selects winners	Early-October
Award given to chapter representative at requested chapter meeting	Open

CALL FOR NOMINATIONS
2020–2021 IEEE EDS Region 9 Biennial Outstanding Student Paper Award

Description: Awarded to promote, recognize, and support meritorious research achievement on the part of Region 9 (Latin America and the Caribbean) students, and their advisors, through the public recognition of their published work, within the Electron Devices Society's field of interest: All aspects of the physics, engineering, theory and phenomena of electron and ion devices such as elemental and compound semiconductor devices, organic and other emerging materials based devices, quantum effect devices, optical devices, displays and imaging devices, photovoltaics, solid-state sensors and actuators, solid-state power devices, high frequency devices, micromechanics, tubes and other vacuum devices. The society is concerned with research, development, design, and manufacture related to the materials, processing, technology, and applications of such devices, and the scientific, technical and other activities that contribute to the advancement of this field.

Prize: A distinction will be conferred in the form of an Award certificate bestowed upon the most outstanding Student Paper nominated for the two-year period. The prize will be presented at either the Latin American Electron Devices Conference (LAEDC) or the Symposium on Microelectronics Technology and Devices (SBMicro). In addition to the recognition certificate, the recipient will receive a subsidy of up to $1,500 to attend the conference, where the award is to be presented. There will be a formal announcement of the winner in a future issue of the EDS Newsletter. The winner will also receive up to three years of complimentary IEEE and EDS student membership, as long as the winner remains eligible for student membership.

Eligibility: Nominees must be enrolled at a higher education institution located in Region 9. In the case of a co-authored paper, only eligible co-authors may be nominated. Papers should be written in English on an electron devices related topic. Papers should have been published, in full-feature form, during 2020–2021 in an internationally recognized IEEE sponsored journal or conference in the field of electron devices related topics. Statements by the student and by the faculty advisor should accompany the nomination. Nominators must be an IEEE EDS member. Previous winners of this award are ineligible. There must be a minimum of five nominations submitted in order for the award to be administered for that year.

Basis for Judging: Demonstration of Nominee's significant ability to perform outstanding research and report its results in the field of electron devices. Papers will be judged on: technical content merit, originality, structure, clarity of composition, writing skills, overall presentation. These criteria will be weighted by the assessment of the nominee's personal contribution and the linkage of the nominated work to the nominee's career plans.

Nomination Package:
- Nominating letter by an EDS member (it may be the faculty advisor)
- A brief one-page (maximum) biographical sketch of the student
- 1000 words (maximum) statement by the nominated student describing the significance and repercussion of the nominated work within the wider scope of the nominee's career plans
- 400 words (maximum) statement by the faculty advisor under whose guidance the nominated work was carried out. It should unmistakably state the faculty advisor's support of the nomination, and clearly explain the extent of the nominated student's contribution, as well as its relevance for the overall success of the reported work.
- A copy of the published paper

Timetable:
- Submit your nomination online: https://ieeeforms.wufoo.com/forms/zvywrvw03cy9rx/
- Nominations are due no later than **15 February 2022**
- Winners will be notified by 15 March 2022
- Recipients may choose to have the formal presentation of the award at either one of the conferences: LAEDC or SBMicro

For more information contact: Laura Riello, EDS Executive Office, l.riello@ieee.org or 732-562-3927.

Susan Lord—Cutting Ties, Forging Paths, and Speaking Up

I have had a successful career. My bio shows highlights including being an IEEE Fellow and receiving the IEEE Undergraduate Teaching Award for "*contributions to the development of more inclusive and innovative undergraduate teaching in electrical and computer engineering*." I'd like to share some personal reflections about my journey from a Ph.D student researching molecular beam epitaxy (MBE) to inclusive teaching. A critical part of this story is being a woman. I went to graduate school because I wanted to teach. I was offered fellowships from the National Science Foundation (NSF) and the AT&T Bell Laboratories Graduate Research Program for Women (GRPW). I almost turned down the GRPW to avoid the "stigma" of a women's program. Fortunately, I recognized its advantages including having Dexter Johnston as a mentor. Active in EDS, he encouraged me to join and helped me learn to prioritize my efforts. I remember his advice "You can save the world or you can graduate." I bristled at the time but am glad I decided to focus and graduate. I can now use my voice to make a difference! I expected graduate school to be challenging technically and it was. However, I was unprepared for the messages that I did not belong as a woman. For example:

- I was the only woman in a group of about 25 men. I felt like I worked in a locker room including my peers calling our advisor "coach" and I needed to wear "armor" every day.
- Male friends in EE declared "there's all these unqualified women and minorities in EE at Stanford." When I worked up my courage to ask "Do you mean me?" they quickly replied "Oh no, not you, but there are all these others." When I asked who, they had no names. If I hadn't been there, would I have been lumped in with "all those others?"
- At the opening session of my first EDS Device Research Conference, one of the organizers cut his tie with scissors to demonstrate the informal atmosphere. I was shocked. As a woman, I was not wearing a tie and did not feel welcome.

I'm tenacious and had strong support from family and friends but I understand how such experiences led others to leave the field. Sexism and racism are not abstract concepts. They have been embodied in this culture. I knew that women were about 10% of EE graduate school. I didn't know that I would often be the only woman in the room or lab. Male students repeatedly asked me "what do women think?" So I took Feminist Studies courses. This opened my eyes to a different world. It never occurred to me that people studied topics such as gender roles or the gender pay gap. These classes gave me a language to discuss issues. I was discouraged from exploring Feminist Studies because my engineering colleagues thought that areas outside of engineering were useless. This attitude prevents many engineers from recognizing valuable expertise and collaborating. After decades of teaching, I finally found a way to integrate aspects of social responsibility into my Circuits class [1]. I could not have done this without those feminist classes and collaborations with social scientists. My career has not been traditional. I've enjoyed combining things that others might consider separate including EE and Materials Science as an undergraduate, EE and Feminist Studies as a graduate student, and EE and engineering education research as a professor. I'm now leading an Integrated Engineering Department where we envision engineering as sociotechnical. I have forged my own path and had an impact beyond what I could have imagined when I was in graduate school. I chose to start my career at a teaching-focused university. And I loved it! I pivoted to engineering education research and have had an amazing community of support including local colleagues and a community of engineering education researchers in the IEEE Education Society and beyond. There are many paths to being a successful electrical engineer. Having been excluded as a woman, I strive to have all of my students feel included. The pain of exclusion led me to learn from disciplines outside of engineering which have helped me to be a better engineering professor. I believe that it is critically important to expand diversity and inclusion in IEEE and EDS. The rising awareness of systemic racism among White communities and the COVID-19 pandemic emphasize that business as usual is not sustainable. My research has shown that EE in the USA lags behind other engineering disciplines in the participation of women [2]–[4]. Many Black students are attracted to EE but do not graduate. EE must address these cultural problems with the same intellectual enthusiasm that we bring

to technical challenges. We need diverse perspectives because diverse teams produce better innovations and move towards social justice. It is not enough for those of us with different perspectives to be allowed in the room. We must be able to share our perspective, be heard, and supported. Those of us with privilege, in my case as a White person, must strive to be allies and use our privilege to support others. None of us are successful solely because of our own efforts. We need to learn from our own history of erasing or hiding contributions of women. Lynn Conway, a pioneer in microelectronics, waited 52 years for IBM to recognizes her contributions and apologize for firing her when she began a gender transition [5]. Katherine Johnson, a pioneer in space exploration at NASA, waited until she was almost 100 years old to be recognized for her mathematical contributions [6]. Advocating for positive cultural change shouldn't take decades. At this historical moment, women in engineering have an opportunity to change the culture if we are willing to speak up, not accept the status quo, and ally with others who experience marginalization. This will only succeed if men are willing to honestly listen, examine their own behaviors, and do things differently. I hope then that women can take off their armor and feel fully included in organizations like IEEE EDS.

Susan Lord is Professor and Chair of Integrated Engineering at the University of San Diego. She received a BS from Cornell University in Materials Science and Electrical Engineering (EE) and MS and Ph.D in EE from Stanford University. She taught at Bucknell University and has industrial experience at Bell Laboratories, NASA, and SPAWAR. Her research has been sponsored by the National Science Foundation (NSF) and focuses on the study and promotion of diversity in engineering including student pathways, military veterans, and inclusive teaching. She co-authored *The Borderlands of Education: Latinas in Engineering.* She has won best paper awards from the *Journal of Engineering Education* and *IEEE Transactions on Education*. Dr. Lord is a Fellow of ASEE and IEEE for *"professional leadership and contributions to engineering education."* She is on the team implementing "Developing Changemaking Engineers," an NSF-sponsored Revolutionizing Engineering Education (RED) project. She received the 2018 IEEE Undergraduate Teaching Award.

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Nadine Collaert—My Wonderful Journey in Science and Engineering

First, let me tell you a bit about myself and my career. I am currently a program director at Interuniversity Microelectronics Centre (imec), a R&D centre in nanoelectronics in Belgium. My research is focused on technologies and solutions for the next generation of wireless communication. But in my career, I have had the privilege to work on a diversity of topics going all the way from CMOS scaling to life-science, working as an integration engineer, working in the area of modelling, simulation and characterization. Next to that, in the last ten years, I had the opportunity to lead teams in my role as program manager and later program director, setting the strategy, interacting with industrial partners and academia.

I started my career as a researcher looking into the feasibility of vertical devices and heterojunction engineering for CMOS scaling beyond 100 nm, and the use of SiGe for buried channel

pMOS devices. In the early 2000's, imec quite early defined a program looking into FinFET devices, which were eventually adopted in 2011 by Intel for the 22 nm technology node and are currently the mainstream device architecture in advanced CMOS. Main highlights of my research lie in the demonstration of high-k/metal gate and the investigation of strain engineering for scaled FinFET devices. I then used my experience in Silicon-On-Insulator (SOI) technologies to work on floating body 1T-DRAM applications. My research in life-science allowed me to expand my knowledge in material science looking at biocompatible materials for lab-on-chip and neuro-probe applications. It was refreshing to step into a new application area, learn new things and at the same time apply my knowledge in CMOS processing and integration to this field. After that, it was time to nurture and broaden my other skills and I stepped into management, that besides technical and operational management also entailed the guiding of cross-disciplinary teams. In my role as program manager of the beyond Si program, we were the first to demonstrate Ge and III-V FinFET and Gate-All-Around devices on 300 mm Si substrates. In 2018, I started the analog/RF program looking at compound semiconductor devices like GaN and InP to tackle the challenges in speed, power and efficiency for the RF Front-End-Module (FEM) in 5G applications and beyond. The expertise we had built up in the area of compound semiconductor materials for logic applications, gave us the confidence that we could really make a difference in the area of wireless communications, where the higher data rates and lower latencies are required for ultra-broadband applications and new use cases like XR and holography. Specifically, the possibility to co-integrate these materials with advanced CMOS is beneficial for form-factor restricted use cases like handsets.

I have been interested in science and mathematics from a very young age. Understanding how things work, being part of enabling new ideas and creating innovations has always fascinated me. As such, studying engineering was a natural next step, and I have been blessed that my parents have always been very supportive about my choices. They have encouraged me and pushed me to always strive for the best. For them, it was only normal that women could excel in science and engineering jobs just like men.

It was during my Ph.D. that I realized I wanted to be in research, doing the groundwork, being at the basis of the innovations that are later taken up by industry. Realizing what you want to do and what you are good at is often a long process, but the road leading up to that realization is as worthwhile as the journey that comes afterwards. I could say that I have been lucky to be able to work in a diversity of topics and roles, but it has not just been luck. I saw the opportunities and grabbed them, and in a few cases I created the opportunities myself. That led me to believe one can achieve more than often thought and anticipated. And that is especially true for women.

The next generation of powerful women in science and engineering has lined up and is eager to do even better than the previous generations. But women in engineering are still underrepresented. And not only are they underrepresented, but many of them also leave the field after a few years. Women are often their own worst enemy. We don't believe enough in ourselves. We need to be brave and step outside of our comfort zones, always look for opportunities where you can try and develop new skills, where you can learn. Continuous learning is the key. Always strive for the best. It takes professional courage, but it is ultimately so rewarding. Know your strengths and weaknesses and be honest. Think about what to do with this knowledge. Strengthen your weaknesses or realize they are there and exploit your strengths.

In general, mentoring is a crucial part of attracting and retaining women in STEM. Having a community to share experiences, hear the inspiring stories of women who dedicated their lives to science and engineering, bounce off ideas, and getting the support to pursue a career is important. Therefore, having this community of Women in Engineering provided by IEEE, is so valuable. The seminars, workshops and events are tailored to connecting engineers from all over the world and providing a platform of mentorship.

In conclusion, I believe we have made progress in attracting more women in engineering, but it's not enough and in fact, we need to accelerate and make sure that future generations of women will be inspired even more to start a career in science and engineering.

Dr. Nadine Collaert is program director at imec. She is currently responsible for the advanced RF program looking at heterogeneous integration of III-V/III-N devices with advanced CMOS to tackle the challenges of next generation mobile communication. Before that she was program director of the LOGIC Beyond Si program focused on the research on novel CMOS devices and new material-enabled device and system approaches to increase functionality. She has been involved in the theory, design, and technology of FinFET devices, emerging memories, transducers for biomedical applications and the integration and characterization of biocompatible materials. She has a Ph.D in electrical engineering from the KU Leuven and she holds more than 400 publications and more than 10 patents in the field of device design and process technology.

IEEE Electron Devices Society's International Women's Day (IWD) Event

Ahmad Sabirin Zoolfakar, Nurul Ezaila Alias, Haslina Jaafar, P Susthitha Menon

In conjunction with International Women's Day (IWD) 2021 on 8 March, the IEEE ED Malaysia Chapter organized a virtual event to commemorate and celebrate the achievements and participation of Women in Engineering (WIE) members of IEEE EDS.

The theme for this year's IWD articulated by UN Women is "Women in leadership: Achieving an equal future in a COVID-19 world," whereas the IWD website provides the hashtag "Choose to Challenge." The Webex event, "*An Afternoon Virtual Session With Women Past Chairs of IEEE EDS Malaysia,*" was moderated by Dr. Nurul Ezaila Alias from Universiti Teknologi Malaysia. Three panel speakers were the Chapter's Past Chairs: Prof. Ir. Dr. Norhayati Soin from Universiti Malaya, Assoc. Prof. Dr. Badariah Bais, and Assoc. Prof. Dr. P. Susthitha Menon from Universiti Kebangsaan Malaysia. The IEEE Malaysia Section Chair, Assoc. Prof. Dr. Pauzi from Universiti Teknologi Malaysia, gave the welcoming speech followed by an introductory speech by the ED Malaysia Chapter Chair, Assoc. Prof. Dr. Ahmad Sabirin Zoolfakar from Universiti Teknologi MARA.

The event was attended by about 60 people. The panelists shared their experiences on a wide range of topics including their career path, academic and industrial experiences, work-family life balance, triumphs, challenges and last but not least some tips and tricks for young women academicians/engineers who are carving their niche in the electrical and electronics engineering field. The panel attendees also shared how their active volunteer involvement in IEEE EDS helped carve their career and personal growth.

This event was the first of its kind to support women engineers in IEEE EDS. The series was initiated by Kazunari Ishimaru from Kioxia Corporation, who is the IEEE EDS Vice President of Meetings & Conferences. The ED Malaysia Chapter would like to thank Dr. Haslina Jaafar from Universiti Putra Malaysia, and Dr. Nurul Ezaila under Social and WIE Portfolio of the ED Malaysia Chapter, for the successful execution of the event. The recorded event can be viewed at this link: https://youtu.be/cpqFi00exMo

The official poster advert for IEEE EDS's IWD event organized by IEEE EDS Malaysia Chapter.

EDS Young Professionals

Luisa Petti: Reflections from an EDS Young Professional

The Young Professional guest in this issue of the Newsletter is Luisa Petti, IEEE Electron Devices Society 2019 Early Career Award recipient for her early career technical achievements in the field of flexible electronic devices. She is an Associate Professor at the Faculty of Science and Technology, Free University of Bozen-Bolzano (Italy). Her perceptions about EDS and views regarding professional development and career growth are reflected in the excerpts of the interview made by Manoj Saxena, the Newsletter Associate Editor-in-Chief.

Manoj Saxena: **What was the specific temptation, if any, which made you join EDS which is the largest professional organization in the globe, at first?**

Luisa Petti: I had the fortune to be largely exposed to IEEE EDS during my Ph.D at ETH Zurich, especially attending EDS conferences such as IEEE ESSDERC and IEEE IEDM. What tempted me about joining EDS was the possibility to get to know many extraordinary scientists in my field of research and to be able to grow both technically and professionally. Back then I genuinely was not aware of how open this society is in welcoming young professionals and encouraging them to volunteer in so many great scientific, educational, social, and humanitarian projects. Only recently, after winning the EDS Early Career Award in 2019, I learned that being an active EDS member is an extraordinary growing and rewarding experience, which I would advise to every young professional working in the field of electron devices.

MS: You won the prestigious EDS Early Career Award, an honor most of the young professionals aspire. How do you consider this recognition and what are your plans to further develop your research career?

LP: I am extremely honored to be one of the three 2019 winners of this extremely prestigious award for young professionals. I consider such a recognition extremely important, not only because it plays a central role in a society like EDS where young professionals are so much considered, but also because it gave me the chance to get to know IEEE EDS better. In fact, before the IEEE EDS Early Career Award ceremony in conjunction with IEEE IEDM 2019, I have been invited to join the IEEE EDS Board of Governor (BoG) Meeting. On that occasion, I met many EDS executive committee members, as well as standing and technical committee chairs. Everyone was extremely open and friendly, suggesting that I volunteer in several interesting EDS activities. Following their advice, I joined several technical committees of EDS conferences, such as IEEE EDTM 2021 and IEEE IFETC 2021, furthermore becoming a member of the EDS Technical Committee of Flexible Electronics & Displays (FED) and of the newly started Women in Engineering (WiE) EDS activity. For the future I am planning to be more and more involved in EDS activities, as I believe that EDS activities can really make a difference in all the aspects of my academic work, from research, teaching up to general public educational and social activities.

MS: As a Young Professional, how do you position your interest in your own field with the activities and services you perform as an EDS member/volunteer?

LP: As a young professional, the activities and services I currently perform as an EDS member and volunteer are perfectly aligned with my research and educational interests in my field. In fact, as a member of the EDS Flexible Electronics and Displays Committee (FEDTC), I am currently organizing–together with other former and current TC members–a perspective report on the future of flexible thin-film transistors (TFTs). This topic is actually a very important topic for me, given my experience with flexible electronics and TFTs both in academia (ETH & Bolzano) and in companies (Apple, Cambridge Display Technology, FlexEnable). Together with leading experts in the fields (both from academia and industry), I will have the chance to try to answer complex questions like: "Are flexible TFTs really competing with Si technologies? What is the real market of this technology?", "Are flexible TFTs really cost-effective in real-world applications?" This is just so exciting, and I must thank EDS for this great occasion.

MS: What are your thoughts about the EDS membership and its paybacks? Whether the EDS membership benefited you at any time in your career growth? If so, how?

LP: I think my membership and now my active involvement in EDS

is currently a great benefit for my career growth, both as a scientist and as a lecturer. The network I am creating and expanding through EDS and its FEDTC is surely a great advantage in collaborations, publications, and grant writing, as everyone in EDS is open to discuss its research interests and find ways of working together internationally. Additionally, I am also growing tremendously in my teaching activities. For example, as a technical co-chair of the IEEE IFETC 2021 conference, I am supporting the creation of tutorials related to how to teach in the multidisciplinary area of flexible electronics. This is also a very important topic for me, as I will soon start teaching a Ph.D course at the Free University of Bozen-Bolzano entitled "Introduction to printing technologies and flexible components".

MS: As an YP, how do you consider the ED Society as a whole and what are the changes or developments you would like to see in evolving this professional body as a group devoted to humanity and its causes?

LP: As a YP, I consider EDS as an extremely important society in the field of engineering and electron devices. During this last year I have seen that EDS continuously questions itself on how to evolve in several directions, especially for what concerns social, humanitarian, educational and scientific causes. Personally, I think that EDS can further improve by involving members from more countries and different institutions, as well as more young professionals and female members. In my opinion it is extremely important to include diversity especially in executive positions.

MS: What are your suggestions and recommendations for those young professionals who may aspire to join EDS?

LP: My suggestion for young professionals aspiring to join EDS is to have an active participation to the society, i.e. by joining Local EDS Chapters and actively participating in the EDS Chapters meetings, participating to EDS conferences and workshops, listening to the EDS webinars (extremely frequent in this pandemic period), as well as volunteering in different EDS activities. Young professionals in this field should know that EDS is actively seeking volunteers ready to get involved in the Society activity, no matter how young they might be or how little scientific experience they might have!

Biography

Luisa Petti received her B.Sc. and M.Sc. in Electronic Engineering from Politecnico di Milano (Italy) in 2009 and 2011, respectively. She obtained her Ph.D. in Electrical Engineering from ETH Zurich (Switzerland) in 2016 with a thesis entitled "Metal oxide semiconductor thin-film transistors for flexible electronics," for which she won the ETH medal. After a short postdoc at ETH Zurich, she joined first Cambridge Display Technology Ltd in October 2016 and then FlexEnable Ltd in December 2017 in Cambridge (UK) as a research scientist. In 2018 she joined the Faculty of Science and Technology at the Free University of Bozen-Bolzano (Italy) as an Assistant Professor, where she has been recently appointed Associate Professor (from 1st of March 2021). In December 2019, Luisa was awarded the 2019 IEEE EDS Early Career Award as a recognition of her early career technical achievements in the field of flexible electronic devices.

Luisa's work is focused on the design, fabrication, and characterization of flexible, printed, and environmentally friendly electronic devices. In particular, her research activity at Free University of Bolzano aims at the realization of fully autonomous systems incorporating sensing, energy harvesting, storage, read-out and wireless communication functionality, to be used for IoT, environmental, health, food science, as well as precision agriculture applications.

Manan Suri: Reflections from an EDS Young Professional

The Young Professional guest in this issue of the Newsletter is Manan Suri, IEEE Electron Devices Society's 2018 Early Career Award winner and a faculty member at Department of Electrical Engineering, Indian Institute of Technology—Delhi, India. His perceptions about EDS and views regarding professional development and career growth are reflected in the discussion. Here are the excerpts of the interview with Manan Suri made by Manoj Saxena, the Newsletter Associate Editor-in-Chief.

Manoj Saxena: At first I would like to ask you what was the specific temptation, if any, which made you join EDS which is a branch of the largest professional organization in the globe?

Manan Suri: As a student I was always fascinated by nanoelectronics. Almost every exciting talk, seminar, student-event, career-event, free pizza that I attended, or any faculty/researcher whose work I admired, had one or the other EDS

connection. So my areas of interest and professional encounters during university days naturally led me to IEEE EDS.

MS: You won the prestigious EDS Early Career Award, an honor most of the young professionals aspire. How do you consider this recognition and what are your plans to further develop your research career?

M: I feel honoured and privileged to receive the Early Career Award and I'll use this occasion to express my deep gratitude towards the EDS society for this timely encouragement. In my opinion, a recognition like this is indeed a culmination of direct/indirect efforts and support from multiple corners (not individual alone). Some of whom I'd like to acknowledge in this recognition include my teachers, my Ph.D supervisors, mentors, colleagues, seniors, students, collaborators, funding agencies, staff and family. I consider this recognition as a source of personal responsibility (i) to uphold the quality of future research work, and (ii) to train, assist, guide young students, researchers in their individual journey on the path of science & technology. In future, I wish to continue contributing back to the scientific/technical community through some of our on-going research in domains such as non-volatile memory technology, NVM applications, AI/Neuromorphic, security hardware, memory-centric computing (LIM/IMC) etc.

MS: As a Young Professional, how do you position your interest in your own field with the activities and services you perform as an EDS member/volunteer?

M: I have been volunteering as reviewer for EDS journals/conferences and organizer of EDS related conferences, special sessions, symposia. Most of my EDS related activities are linked to research areas such as non-volatile memory technology, applications, neuromorphic devices, circuits, semiconductor hardware security primitives, etc.

MS: What are your thoughts about the EDS membership and its paybacks? Whether the EDS membership benefited you at any time in your career growth? If so, how?

M: IEEE EDS is one of the most relevant and leading professional societies on topics related to both, emerging and mainstream semiconductor device technologies. I have benefited from EDS membership and I'll certainly recommend it to aspiring researchers in the domain. EDS is a very enriching, diverse and friendly community of professionals, domain experts and peers. I have learnt a lot from EDS resources (such as TED, EDL, etc.) and its highly focussed events such as IEDM, IMW and more. EDS events provide some of the most focussed professional networking opportunities. Such opportunities/ focussed events can put young researchers on a steep learning trajectory and connect them with excellent experts or mentors.

MS: What are your suggestions and recommendations for those young professionals who may aspire to join EDS?

M: My suggestion to young professionals aspiring to join EDS would be to not hesitate or think twice before taking the plunge. It's a very friendly community and one from which you can learn a lot and grow in your career. Many young professionals all over the globe are already benefiting from the EDS membership.

MS: As an EDS Young Professional and a young researcher in the field, how do you consider the prospects of scientific research in this field for the progress of Humanity as a whole?

M: I'd like to go to the extent of saying that electron devices, semiconductors, have been the bedrock of most advances in our lives. Semiconductors, electron devices have been significantly enabling domains such as AI, big-data, Quantum, clean & renewable energy, security, HPC, etc. It is one of the most complex and interdisciplinary engineering topics. This layer of nanoscale reality sits at the bottom of all modern technologies, deeply embedded and hidden from the eye, enabling and empowering almost everything around us (like DNA of all modern tech-systems). Since this reality is so small (nanoscale) and so deeply hidden, often it remains underrated in terms of the true value that it has created for the entire human civilization, and the attention that it deserves. Present and future prospects of R&D in the field are as bright and promising as one can imagine. Pure CMOS scaling is no longer a straightforward answer to progression of electronic systems. With the emergence of multiple beyond CMOS devices (both for logic and memory), beyond silicon materials, 3D integration and advanced packaging techniques, several new avenues are opening up for exploration. Further, circuits are becoming more and more hybrid (i.e. CMOS + beyond CMOS devices). Such developments are also bridging the gaps between different layers of technology; these days, circuit designers need to talk more to device engineers, system architects need to interface with process engineers and so on. With exploitation of unconventional characteristics of emerging devices, rigid walls between research on materials, devices, circuits, architectures, algorithms, software and end-applications are getting blurred.

Biography

Dr. Manan Suri leads the NVM and Neuromorphic Hardware Research group at IIT-Delhi. His research interests include Semiconductor Non-Volatile Memory (NVM) Technology and its Advanced Applications (Neuromorphic, AI, Security, Computing, Sensing). He was selected by MIT Technology Review as one of the world's Top 35 Innovators under the age of 35 (MIT-TR 35 Global List - 2018). Dr. Suri received the prestigious

IEEE EDS Early Career Award (2018), Young Scientist Award (2017) from The National Academy of Sciences, Young Engineers Award (2016), from The Institution of Engineers, and Laureat du Prix (2014) from the French Nanosciences Foundation. Dr. Suri has filed several patents, authored ~80 publications, delivered 60+ Invited talks, and led 10+ research projects/consultancies as principal investigator. He has served as an advisor to leading AI-Hardware/NVM companies and government bodies. In the past, he has worked at NXP Semiconductors, Belgium as a Senior Scientist and CEA-LETI, France. Dr. Suri received his Ph.D from INP-Grenoble, France and Masters from Cornell University, USA. Web: https://web.iitd.ac.in/~manansuri/

Updates from the 2020 EDS Ph.D Student Fellowship Winners

The Electron Devices Society Ph.D Student Fellowship Program was designed to promote, recognize, and support Ph.D level study and research within the Electron Devices Society's field of interest. The 2020 EDS Ph.D Student Fellowship recipients were:

- Wangyong Chen—Peking University
- Nicolas Wainstein—Technion–Israel Institute of Technology
- Christopher Allemang—University of Michigan

Wangyong Chen (IEEE Student Member, EDS Member, and Young Professionals) received the B.S. degree in Electronics Science and Technology from Hunan University, Changsha, China, in 2016. He is currently pursuing the Ph.D. degree in Microelectronics and Solid State Electronics with the Institute of Microelectronics, Peking University, Beijing, China. His current research interests include multi-scale reliability modeling and simulation from devices to circuits as well as experimental characterization, including reliability-aware device-circuit co-design, self-heating characterization. He developed the trap dynamics based 3D Kinetic Monte Carlo simulator to capture the statistical charge distributions in the multilayer gate dielectric under arbitrary stress conditions in the presence of time-zero variations. The simulator provides a powerful tool for comprehensive reliability evaluation at the advanced technology node and traps impact identification over the entire bias space. Within the Ph.D. study, he did series of works on self-heating effect in advanced nanoscale devices ranging from experimental characterization to modeling and simulation, where an analytical model based on the multistage thermal network to effectively address the self- and mutual-heating in the scaled device was developed and a novel self-heating characterization method using the shared intrinsic series resistance was proposed. On the basis of the developed simulation tool for trap-related reliability, he also proposed an efficient variability- and reliability- aware device and circuit co-design methodology to predict the time-dependent delay degradation and potential critical paths in the digital circuits coupled with self-heating effect at operating conditions. He developed an analytical model of back gate modulation in FDSOI device including short-channel effects, quantum effects, trap variability, which can be applied to real-time dynamic performance compensation of FDSOI device using back bias. He proposed a new method based on the temperature dependence of gate leakage current for accurately characterizing thermal crosstalk, which offers a possible hardware solution to thermal monitor and management. He has published 30 technical papers and owned 3 patents during the doctoral study period, including conference and journal papers on the IEEE IEDM, EDL, T-ED and T-NANO. He received the IEEE IPFA Best Paper Award in 2018, and he was invited to deliver a report at the ESREF conference in 2018. He was selected for the Best Paper Award in the Microelectronics Forum of China in 2018. He won the title of outstanding graduate of Hunan Province and Hunan University in 2016. He was awarded the National Scholarship in China 5 times from 2013 to 2020. He won the Headmaster's Fellowship in 2019 which is the top honor prize for the graduate student in Peking University, and he was selected as Merit Student and Academic Innovation Award from Peking University for two consecutive years. He serves as the active reviewer for IEEE T-ED, EDL and J-EDS, etc.

Christopher Allemang In March 2020 when the COVID-19 pandemic hit the United States, in-person research was paused and I quickly transitioned into device modeling and writing from home. The work completed before the in-person research pause on high-performance ALD zinc-tin-oxide TFTs was virtually presented in IEEE's 78th Device Re-

search Conference and published in Advanced Electronic Materials. With in-person research ramping back up in June 2020, Professor Becky (R.L) Peterson and I could continue our collaboration with Professor Neil Dasgupta's and Professor Kira Barton's research groups at the University of Michigan. Through this interdisciplinary collaboration, we integrated our previously developed high-performance ALD films with patterning using electrohydrodynamic-printing to enable customizable additive manufacturing of thin-film electronics. This work was presented virtually in MRS's 62nd Electronic Materials Conference and published in ACS nano. In Fall 2020, I was a graduate student instructor for Introduction to Semiconductor Devices. During this time, I also mentored an undergraduate and graduate student and volunteered as an election worker. I look forward to sharing my continued work supported by the IEEE EDS Ph.D Student Fellowship at this summer's IEEE DRC.

Subramanian Iyer
Student Fellowship
Committee Chair
UCLA

Updates from the 2020 EDS Masters Student Fellowship Winners

Subramanian Iyer
Student Fellowship
Committee Chair

The Electron Devices Society Masters Student Fellowship Program was designed to promote, recognize, and support Masters level study and research within the Electron Devices Society's field of interest. The 2020 EDS Ph.D Masters Fellowship recipients were:

- Hong-Yi Tu—National Sun Yat-Sen University
- Prasanna Venkatesan Ravindran—Georgia Institute of Technology

Hong-Yi Tu was in the five-year bachelor's and Master's degree program pursuing the M.S. degree in 2020 in the department of Materials and Optoelectronic Science from National Sun Yat-Sen University, Kaohsiung, Taiwan. He was approved for the application of direct admission to doctoral program from master program in 2021. He is currently pursuing the Ph.D. degree with the department of Materials and Optoelectronic Science from National Sun Yat-Sen University. His current research includes low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs), amorphous metal oxide TFTs, and GaN high electron mobility transistors (HEMTs). His research focuses on the reliability issues and optimization of reliability in LTPS TFT, metal oxide TFT and GaN HEMT. To date, he has published 2 articles as primary author and 12 articles as co-author.

Prasanna Venkatesan Ravindran is a second year Ph.D student in Dr. Asif Khan's lab. He works on modelling Ferroelectrics, negative capacitance, domain dynamics and cryogenic measurements. His work, in collaboration with his colleague Nujhat Tasneem, on charge boost in ferroelectric-dielectric heterostructures, titled "Differential charge boost in hysteretic ferroelectric–dielectric heterostructure capacitors at steady state" was recently published in APL as part of the special topic on Ferroelectricity in Hafnium Oxide: Materials and Device. Here, they show that there is a differential charge boost in FE-DE heterostructures, and that it is a steady-state effect and not a transient. The work is also being presented at the MRS Spring Meet 2021.

Subramanian Iyer
Student Fellowship
Committee Chair
UCLA

Updates from the 2020 EDS Undergraduate Fellowship Winners

Samar Saha
Undergraduate Student Scholarship Committee Chair

The Electron Devices Society Undergraduate Student Fellowship Program was designed to promote, recognize, and support undergraduate level study and hands-on experience within the Electron Devices Society's field of interest.

The 2020 EDS Undergraduate Fellowship recipients were:

- Azwar Abdulsalam—Indian Institute of Technology Kharagpur
- Yanghao Wang—Peking University

Yanghao Wang—In the past year, I have been working on solving some interesting problems about how to handle spatiotemporal information by neuromorphic devices and how to optimize devices to meet corresponding requirements. I mainly focus on working memory and attention mechanisms and have demonstrated some possible methods to realize in-situ computing relying on memristor crossbars or a kind of new device named synaptic transistor. It may have some value in processing sensing signals efficiently. Besides, I also wrote a perspective about neuromorphic computing published in the Journal Of Semiconductors.

Azwar Abdulsalam—I am currently continuing my earlier works on developing a fully physics based compact model for p-GaN HEMT. We are in the final stages of preparing a manuscript on the very topic and hope to communicate our findings in the coming weeks. Apart from this, I have also started working on an exciting and emerging sub-domain of device modeling that of using machine learning and deep learning algorithms in device modeling. Our work so far has been confined to the application of machine learning (ML) and deep learning (DL) algorithms for calibrating and extracting parameters values of established models for different GaN power devices. Through this work we hope to greatly simplify the process of extracting model parameters which earlier used to be a very laborious task. This has been done by integrating ML optimization algorithms directly with circuit simulator software. In the coming future we hope to expand the application of ML and DL into developing robust models for planar and non-planar GaN devices as well as studying the effect of traps and fabrication processes on the device performance. I have recently been offered a Master's in Electrical Engineering at Purdue University. I hope to continue exploring many more exciting devices and studying the intricate physics behind these devices alongside some of the leading figures of the field at Purdue University.

Samar Saha
Undergraduate Student Scholarship Committee Chair
Prospicient Devices

NEW!

EDS Podcasts Available to Everyone!

EDS is pleased to announce our new podcast series. Join us as we host interviews with some of the most successful members of our Society sharing their lives and careers. Their insight and wisdom will be invaluable inspiration and knowledge for those in the engineering field. Stay tuned to our social media channels and website for future announcements on upcoming events.

2020 IEEE Industry Placement Scheme

By Prof. Merlyne De Souza, University of Sheffield

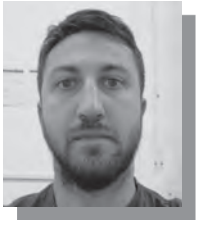
As society faces some of the biggest challenges of our times, it is even more important for young people to be aware of the role of Electron Device Engineers in decades to come. CMOS has been the driving force of the microelectronics revolution, from the first IC consisting of a few thousand components, to the latest chips integrating billions of transistors, that operate with lower power consumption, than the generation (technology node) before it. Over this period, industry has seen a remarkable consolidation, resulting in changes to the requirements of our skills-force. Although scaling will continue over the next 3–5 years towards the 2 nanometer technology node, there is much to look forward to, as we advance towards Quantum Technology, Neuromorphic computing/accelerators of AI, compound semiconductors (GaN and SiC), renewables and communications technologies for 5G and the Internet of Things (IOT). These newer areas will continue to be underpinned by CMOS and require trained device engineers, vital to sustain industry.

In 2020, our Society supported an industrial placement scheme to foster links between current and newly graduated students with companies working in the above topics to the tune of (US$1000) each. The student's activities ranged from interleaved resonant power factor correction circuits in GaN, to reliability characterization of RF front end modules and linearization techniques for 5G. There were two projects from India on recycling one of which was to estimate the economic costs of recycling photovoltaic panels to minimize waste and environmental pollution. Another student gained experience cleaning and installing solar panels in a lab located in Switzerland. Two students worked on mitigation techniques for adversarial attacks on biometrics for continuous authentication systems and methods for physical layer security of networks, both relying on AI accelerators.

Below are some of the experiences of the first batch of 10 students, 3 of whom were women. We hope these will inspire more young people from all backgrounds to consider studying and developing a career in EDS.

Hello, I'm Narges Pourshahrokhi, currently doing my Ph.D in machine learning at the University of Surrey UK. I undertook a 6-month industrial placement at the Applied research group in British multinational telecommunications (BT) based in Adastral Park, Ipswich, UK.

My main responsibilities included liaising with the security and cyber defence teams and Applied research to investigate cybersecurity attacks using the generative models in a continuous authentication (CA) system developed on biometric sensors. As a result of my placement, I have submitted an academic paper to one of the top conferences in cybersecurity with biometric, IJCB 2021. We had bi-weekly meetings with my supervisors, which helped me gain soft skills, such as presentation skills, writing minutes to track my progress and organise it. Another outstanding advantage from my placement was applying theoretical concepts that I learn at university in practice and industry. I believe I greatly benefited from completing the placement. I was put in the deep end and tasked with jobs that actually made a difference in the company and academia. I truly felt valued and part of a team, as well as being mentored and given development training by my managers. Working in the industry for 6 months has definitely challenged me and shaped my future career aspirations.



Hello, I'm Sebastian Matias Pazos. During this virtual placement I worked on a feasibility assessment of an IC design for mmWave reliability tests, targeting 5G applications in RFSOI CMOS technologies. This topic was well aligned to my thesis, in which we studied aging and reliability of RF circuits, design for reliability of RF power amplifiers and robust/adaptive RF circuit design and modeling.

Being able to discuss with my supervisor and other members of GF's reliability teams on the challenges and industrial requirements around these matters gave our work a clear perspective of its potential for application in the semiconductor industry. This meant invaluable experience and training for me and contributed towards finishing my dissertation early March, for which my industry supervisor was jury.

These interactions also led to the sponsorship by GF for an IC tape-out (previous signing of NDAs between the institutions involved) of the prototype of a hot-carrier resilient RF Power amplifier designed during my

Ph.D. Additionally, our institutions were granted access to design kits for RFSOI technologies, enabling further collaborations on the topic.

This initiative from the IEEE EDS is, from my perspective, a great chance for young professionals to directly apply their training on open problems in industry and get a glance at industrial activities as part of the professional experience during the Ph.D. This is especially valuable for students from region 9 where, more often than not, resources for research are scarce and industrial interaction is not as frequent as in highly developed countries. This type of grants allow us to widen our international collaboration perspectives alongside our professional horizons, adding value to the contributions performed from our region.

Dear all, my name is Jordi Muñoz Gorriz and I was a Ph.D student from the *Universitat Autònoma de Barcelona* (Spain) writing my thesis, when I was selected for the IEEE EDS industry placements. As a general statement, I liked a lot the possibility of being able to work with state-of-the-art devices that would be impossible for me to acquire from any other way. In fact, one of the things I learnt is how difficult it can be to collaborate with industry. Moreover, despite my awareness of NDAs and confidential information in industry, what surprised me the most, is the difference between the papers I am used to writing in academia compared to the lack of information in papers written by industry.

As an experience, not only I was able to work with very advanced devices, but also to study other aspects of breakdown phenomena that I had never worked with before. I love to learn new topics and this collaboration was the perfect excuse. However, I really missed being able to electrically characterize the devices. I also love going to the laboratory from time to time. But there was nothing to do about it, the remote working was the most secure and responsible decision. After this industry placement, I finished my thesis and now I am still working with my academic tutor. Also, we are still in contact with my industry mentor and we have made a new proposal to her group. We still don't know if this collaboration will succeed, but it is true that it will be easier thanks to this IEEE EDS industry placement!

Hello, I'm Abidemi Eleyele. I did my industrial placement, an internship position in the Digital Power group of Huawei Research and development centre, Sweden starting from February to October 2020. I could only spend just a month in the office before being asked to stay and work remotely from home.

It also happened that my master thesis was written during the internship period. My research project was to design an Isolated single-stage power factor correction (PFC) AC/DC converter with active and passive ripple cancellation circuit needed to remove the second-order output harmonic common to single-stage PFC converters. I was also tasked to study wide bandgap materials such as GaNs and Sic switches required to implement my research.

My supervisor was so supportive and always ready to help me while still teaching me how to work alone despite my little knowledge in the field. I quickly adapted to the recent trends and got me up and running in around ten weeks, starting from minimum expertise in the area. On top of that, I also learned and developed leadership capabilities and made networks in the industry.

After the internship program, He commended me for being an intelligent person with very high problem-solving skills. He also praised the core skills such as proficiency in power electronic circuit and control design abilities I developed. At Huawei, I was able to learn to work independently and learn how to solve very complex problems in a simple, fast and very efficient way.

Finally, due to my immense contribution to the group and the field of power electronics, my supervisor recommended that I be hired for a Power Electronics Engineer position, which I currently hold. The company is offering to sponsor me for an industrial Ph.D position, as I am now in talks with universities to secure a supervisor. Thanks.

Hello, my name is Aarti Rathi. Through this IEEE industrial sponsorship, I got to know about the working environment in industry. However, it was virtual, but the continuous support and regular interactions with my supervisors (both industry and academic) helped me in knowing and deeply understanding concepts. This work also helped me in gaining a publication in a prestigious conference i.e. IEEE International Reliability Physics Symposium (IRPS), based on the reliability characterization and analysis of power amplifier circuits in PDSOI MOSFETs in sub 6GHz that I undertook.

This internship also helped me in making contacts with the industry people (GlobalFoundries) that may further help me in my career growth. A heartfelt thanks to my supervisors and the EDS team.

Hello my name is Nagaditya Poluri. I had just finished my Ph.D at the University of Sheffield in March '20 when the pandemic arrived. Support from the IEEE EDS society was very welcome and enabled me to collaborate with the industry partner,

pSemi. The placement helped me to understand the current interests and focus aspects of the industry and consumer requirement in future communication system 5G. This understanding enabled me to orient the focus of my academic research specifically in the issues surrounding the design of linear chips at frequencies above 30 GHz. Additionally, a virtual tour of their lab introduced me to new equipment and measurement techniques.

The program will run again this year. Contact: m.desouza@sheffield.ac.uk.

2021 Sponsorships Towards Industrial Placement

As a result of a second year of funding from a new initiative, opportunities are available for current and newly graduated students to spend time in industry in any of the upcoming areas of quantum technologies, neuromorphic computing/accelerators of AI, compound semiconductors (GaN and SiC),5G/IOT and renewables. These funds are meant to enable placements of undergraduate/graduate/postgraduate/newly graduated students/postdocs in any company/research organization engaged in these subject areas. The initiative is open to all, but special consideration will be given to EDS student members. The funds will pay for travel and subsistence costs for placements that are a minimum of a week in duration and completed by 1 September 2021. We also encourage virtual placements, that will support subsistence costs, such as accommodation and living expenses, of candidates who are in a transition period due to COVID-19. In such a case, the placement will be based on completion of a project lasting a minimum of a month with the company. This is the first round of applications this year with a deadline of 15 July 2021. A budget of up to $1000 USD can be allocated per person. It is expected that the funds will be disbursed equally in the Americas, Europe, and students in Africa/Asia (including Australia).

Expressions of interest from prospective candidates/departments/supervisors/companies must be submitted by email, together with a description of the candidate CV (1 page), company contact to confirm the placement, with a paragraph about the work and duration by 15 July 2021 to m.desouza@sheffield.ac.uk. The candidates will be shortlisted by a selection committee. A final report consisting of a maximum of 2 A4 pages, endorsed by the training supervisor at the company, will be required, before disbursing the money at the end of the project. Applicants may make a case for a proportion of funds to be granted in advance of costs, where applicable.

Chapter News

Spotlight on ED Delhi Chapter's Activities and Awards

By Mridula Gupta and Rakhi Narang

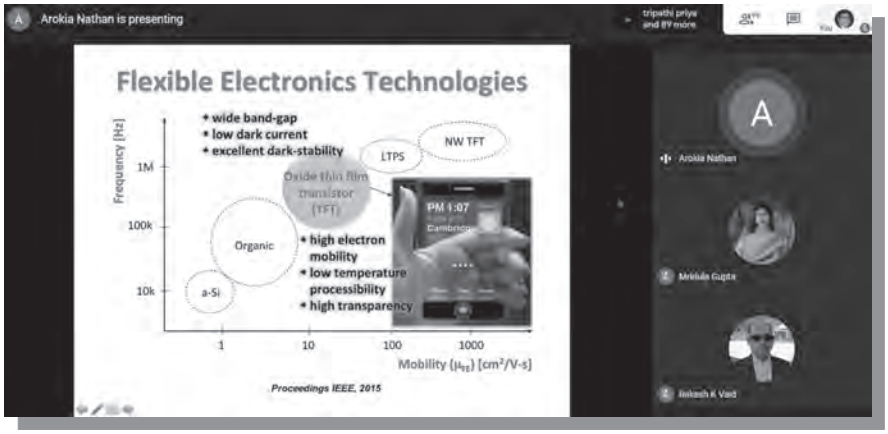
The Delhi Chapter of Electron Devices Society was established on 30 January 2007 with Prof. R. S. Gupta as its founder chairman. At Present, the ED Delhi Chapter is led by Prof. Mridula Gupta and comprises 131 members including one Fellow, 3 Life Senior Members, 22 Senior Members, 51 Members, apart from 54 Graduate/Student Members. The ED Delhi Chapter and its members are actively involved in the technical domain by organizing technical events such as Distinguished Lecturer Program, Mini Colloquia and sponsoring/ co-sponsoring various conferences and workshops.

Student Centric Activities: The chapter and its members have always emphasized on organizing lectures, symposia, workshops and outreach activities to foster learning and innovation among the students. The members are encouraged to organize events at different institutions and Universities located in various parts of Delhi & National Capital Region (NCR). This helps in reaching out to a wider audience composed of students as well as professional members. During the second edition of ED Delhi Chapter flagship conference NCRDE-2017, a special session was planned for undergraduate students to present and showcase their projects. The session was judged and best project presentations were awarded. Moreover, the outstation student paper presenters were also provided with travel support. This helped in providing opportunities to young scholars to showcase their talent and connect with their peers, researchers and experts from all parts of the country. This initiative was very well received both by the student members and academic community.

Volunteers are the strength and asset: The growth of any organization or society by leaps and bounds, largely depends on its volunteers and their passion to work toward a common cause or goal. The EDS chapter and its volunteers have always taken up the task to relentlessly work towards achieving the goals of IEEE and EDS in the advancement of technology.

Awards and recognition: The efforts were well appreciated and acknowledged by IEEE by bestowing the best volunteer award for the year 2012 to Dr. Manoj Saxena, the then Secretary of ED Delhi Chapter, for his outstanding contributions. The chapter takes pride in its capable leadership over the years and common technical interests of its members which has helped the chapter to win the most coveted Best Chapter of the year award not once but twice (in 2013 and 2017). Consistent and persistent effort by the members and volunteers in conducting versatile activities has been the key of the chapters' success story.

Virtual Drift: Due to COVID-19 pandemic, the organization of in-person activities came to a standstill. Then, as the virtual became the new normal, virtual meetings & webinars became the reality and the savior to stay in touch with the members and continue our activities. The technology proved to be a boon to connect not just with the local, but with the global experts. The chapter organized 14 distinguished lecturer talks in a short span of 30 days on various topics relevant to electron devices. The picture illustrates one of them . These lectures would have been impossible to conduct as in-person events. Each DL talk had more than 100 attendees: students, faculty members and participants from different parts of the country as well as from the world. Such a huge response and interest from the participants motivated the members to organize a week-long summer school and mini-colloquia subsequently. More than 400 students, researchers and faculty members attended the Summer School. The executive committee meetings were also conducted time to time in virtual mode through various online platforms.



Prof. Arokia Nathan (Cambridge Touch Technologies, UK) delivering a virtual DL talk. Prof. Mridula Gupta (Chairperson of EDS Delhi Chapter) and Dr. Rakesh Vaid (Jammu University, India)

In all, 2020 proved to be a very successful and remarkable year in terms of the knowledge exchange that took place during these events and reaching out to a wider audience like never before. In fact, the then EDS president Dr. Meyya Meyyapan, acknowledged and praised Delhi Chapter for the successful organization of multiple DLs during the IEEE Electron Devices Global Chapters Summit. Later on, in a message to EDS members published in the EDS Newsletter (January 2021 edition), he added that the initiative can prove to be a model for all the global chapters.

Prof. Mridula Gupta (Department of Electronic Science, Univ. of Delhi) is the Chapter chair and The other members of the Executive Board of this Chapter are: Vice Chair Dr. Subhasis Haldar (Motilal Nehru College, Univ. of Delhi) and Dr. Meena Mishra (SSPL, New Delhi), Secretary Dr. Harsupreet Kaur (Department of Electronic Science, Univ. of Delhi), Joint Secretary: Dr. Vandana Kumari (Maharaja Agrasen College, Univ. of Delhi) and Treasurer Dr. Rakhi Narang (Sri Venkateswara College, Univ. of Delhi). Chapter Website: https://edsdelhi.in/index.html

~Soumya Pandit, Editor

IEEE EDS Center of Excellence at Heritage Institute of Technology

By Mousiki Kar

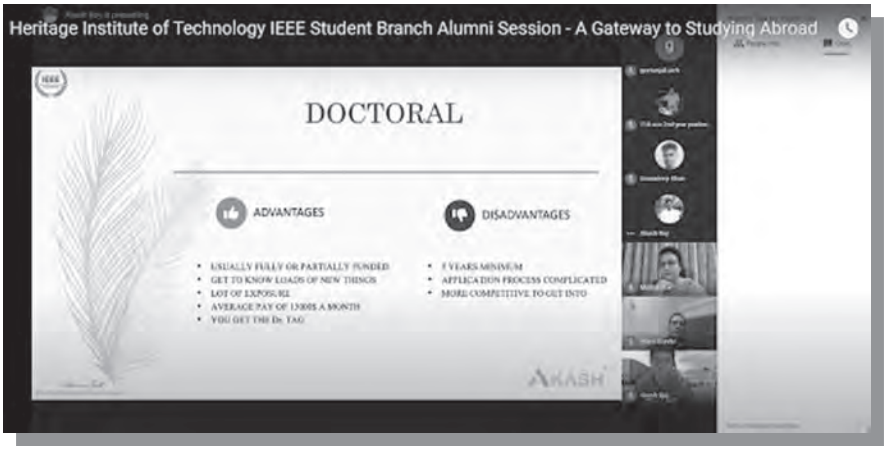
'Education for Empowerment' is the motto that drives the IEEE EDS Center of Excellence, HITK. In order to bridge the gap created by educational disparities between various socio-economic groups, the volunteers associated with this center organized an activity 'Light of Learning' during 20–22 March 2021. They reached out to 23 school-going underprivileged children, aged between 6 and 14 years. The children were given school stationery and books. Due to the pandemic, the volunteers who are confined to their localities conducted the activity in their neighbourhood, which spanned across the state of West Bengal, India in areas like Purulia, Bally, Chandannagar and Kolkata.

ED Heritage Institute of Technology Student Branch Chapter

by Atanu Kundu

An event series named 'Alumni Talk,' was launched by the Heritage Institute of Technology, Kolkata Student Branch Chapter. This initiative targets to connect and forge bonds with alumni of the Institute spread across the globe, and to build a strong alumni network.

The first talk of the series was delivered by Akash Roy, an alumnus of the Department of Electronics and Communication Engineering, who has joined the Ph.D program at University of Southern California. He presented a talk titled, "Beyond Undergraduate Engineering Education: A Roadmap," in which he shared his experience of the do's and don'ts of selecting an Institution for higher education. Akash explained that while selection of an institution one has to make sure that one's passion gets fulfilled, best universities to be shortlisted based on preferred areas, the course content should be thoroughly checked and finally the financial aspects to be considered. However, one should not blindly take up any course just because it is trending. The talk held on 6 February 2021 was attended by 44 participants.



Webinar delivered by Akash Roy, University of Southern California

~Soumya Pandit, Editor

Regional News

Europe, Middle East & Africa (Region 8)

ED/AP/MTT/COM/EMC Tomsk Joint Chapter

Moscow Workshop on Electronic and Networking Technologies MWENT 2020

—by O.V. Stukach

The three-day MWENT 2020 Workshop, technically co-sponsored by EDS, endorsed by IEEE Russia Central Section and Tomsk Joint Chapter, was organized in Moscow, Russia. This biennial three-track event has rapidly become one of the highlight workshops on networks and electronic technologies, gathering researchers from both academia and industry. The host organization was Moscow Institute of Electronics and Mathematics of National Research University Higher School of Economics (MIEM HSE), one of the most prestigious education institutions in Russia. The main goal of the workshop was to stress the importance of survivability aspects in the growing content-oriented networks and reliability of electron devices. Technical networks exhibit many interdependencies that are to be comprehensively measured and modeled. The network design leads typically to multi-objective optimization problems involving an interplay between resilience, sustainability, and robustness. The current network design and evaluation methods are often unable to cope with these interdependencies. MWENT aimed at their better understanding and implementation. Throughout the extensive review and discussion, it was confirmed that ongoing network infrastructures are globally progressing rapidly and that new application domains are emerging mainly based on IoT beyond all kinds of communication.

An increase in community interest in MWENT has been observed this year. A total amount of 200 regular submissions were reviewed by TPC members and external reviewers. As a result, we have 157 peer-reviewed manuscripts in the Proceedings. The accepted papers were organized into the following sessions: Fundamental Problems of Electronics, Network and Telecommunication, Technologies of Electronic Instrument Engineering, Information Security, Signal Processing, Satellite Communications, and Measurements. The technical program was enriched by a comprehensive overview of MIEM scientific programs. As a tradition of MWENT, in addition to the IEEE Xplore publication, participants were also provided with electronic proceedings. The next edition of our events, the 15th International Siberian Conference on Control and Communications (SIBCON) was held in Kazan, Russia, on 13–15 May 2021. For more information, please follow the link https://kpfu.ru/sibcon2021.

~Kateryna Arkhypova, Editor

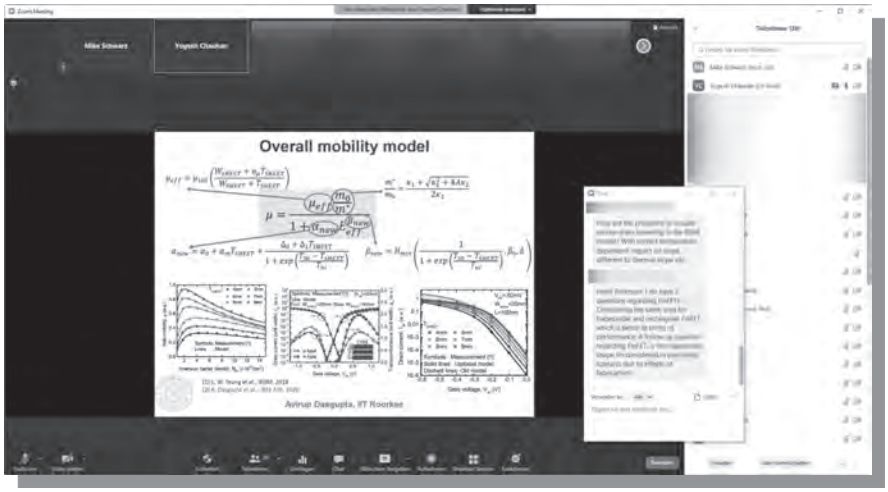
The MWENT Award Ceremony at the Museum of Radio Electronics Development

IEEE EDS Distinguished Lecture—Yogesh S. Chauhan, on Physics and Modeling of FinFET and Nanosheet Transistors

—by Mike Schwarz

The Distinguished Lecture on "Physics and Modeling of FinFET and Nanosheet Transistors" was held 17 March 2021. It was organized by the ED Germany Chapter and co-sponsored by the NanoP from THM—University of Applied Sciences. The DL was attended by 25 IEEE participants and 18 non-IEEE members.

The distinguished lecture of Prof. Chauhan from IIT Kanpur (India), began with an introduction into the basic functional principle of a MOSFET with the key performance parameters. Afterwards, the speaker showed the applied technology boosters of the recent decades, e.g. strained-silicon, high-k metal gate technology, etc. and also the movement from bulk towards FinFET and GAA technologies.



Prof. Yogesh Chauhan during the discussion on modeling of transistors

In the main part Prof. Chauhan, one of the main developers of the BSIM models (First industry standard SPICE model for IC simulation), showed the various BSIM models and their validity and comparison to experimental data. A discussion followed regarding the effects captured by the various evolutional BSIM models, e.g. short channel effect, quantum mechanics, temperature effects and geometrical impacts.

A prospective view into the future and the demands of modeling for 10nm and beyond were a hot topic during the presentation. Here, Prof. Chauhan showed examples of different material stacks and upcoming architectures. Among them there was a nanosheet transistor, one of the most promising candidates to replace the FinFET. In this context, especially for structures below 3nm, effects required to be captured more precisely were discussed, as the DoS (Density-of-States) depending on the geometry-related dimensionality (3D to 1D effects).

A discussion on the scaling and modeling of the FinFETs and the nanosheet transistors followed. Here, topics as transport regimes, modeling algorithms, and problems occurring during validation were discussed. Afterwards, Prof. Chauhan offered the new BSIM model, which includes the nanosheet transistor compact model.

IEEE EDS Distinguished Lecture—Elena Gnani, on Tunnel FETs: Device Physics and Realizations

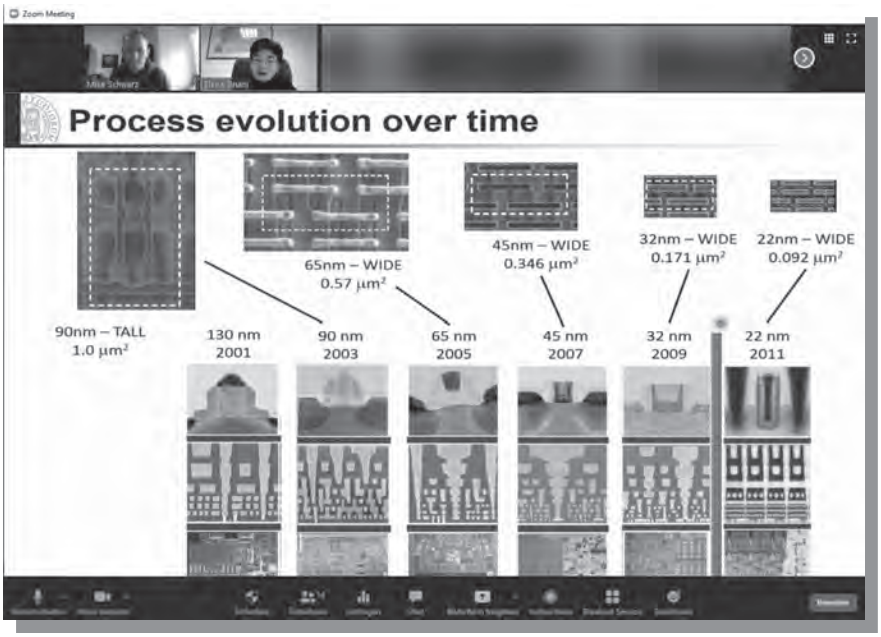
—by Mike Schwarz

The Distinguished Lecture on "Tunnel FETs: Device Physics and Realizations" was held 18 January 2021. It was organized by the ED Germany Chapter and co-sponsored by the NanoP from THM—University of Applied Sciences. The DL was attended by 15 participants, with 12 IEEE participants and 3 guests. It was a little bit disappointing, because 30 registrations took place.

Prof. Gnani from University of Bologna, Bologna, Italy, started with an introduction on some fundamental basics of device technology and its parameters, e.g. scaling rules. Afterwards, she continued with the process evolution over time and where the scaling roadblocks are. Energy, voltage supply and I_{off} relations followed and principles of FET operation for I_{off} were presented with the focus on where improvements impact potential device performance enhancements.

This was the cliffhanger to the Tunnel FET operation principle, where the relation of the exponential behavior of the Fermi function vanishes by the tunneling operation principle. This mainly performs in the linear region/relationship of the Fermi function. Basics and pros and cons of the Tunnel FET followed including an overview on a performance graph of prototypes of Tunnel FETs.

After the presentation and lecture, various questions were asked about the temperature effect on Tunnel FETs due to the band gap variation, which however seems to be a second order effect compared to the Trap Assisted Tunneling (TAT) dependency on temperature. Also constraints of the nanowire diameter due to quantum confinement and device to device



Prof. Elena Gnani during the lecture, Tunnel FETs: Device Physics and Realizations. A huge "thank you" to all participants and lecturers

variation were discussed. The nanowire FET application for automotive was discussed as well.

IEEE EDS Distinguished Lecture —Adrian Ionescu, on Electronic Devices Operating Near 100 millivolts

—by Mike Schwarz

The Distinguished Lecture on "Electronic devices operating near 100 millivolts" was held on 1 February 2021. It was organized by the ED Germany Chapter and co-sponsored by the NanoP from THM—University of Applied Sciences. The DL was attended by 16 IEEE participants.

The distinguished lecture of Prof. Ionescu from EPFL (Switzerland), began with an introduction into the topic "Towards energy efficient semiconductor technologies for Edge AI." The speaker gave some initial examples of successors of low power devices e.g. the iPhone, a wireless computer with sensors. These examples combine energy efficiency with new functionalities. Furthermore, Prof. Ionescu took focus on a so-called "Dark Silicon," which allows high transistor densities with actual high-end technology nodes by keeping e.g. 80% of the transistor silent, while 20% perform calculations. Such strategies allow controlling warming by the power dissipation and require the parallelism by multi-core systems. Nature and the human brain are idols in terms of dark systems. However, such strategies are approaching the sweet spot, where the N cores (128 cores) require more effort in organization, which finally costs performance gain of the parallelism.

To overcome these limitations, new device concepts such as the Tunnel FETs allow operating near the 100mV supply bias and improving the power dissipation issue by switching with steep slopes. Prof. Ionescu and his group at EPFL did pioneering work in this field and still improve and combine these devices with further concepts. He stated different potentials to optimize TFETs further, e.g. high-k dielectrics, narrower junction, thinner body, etc. Furthermore, Prof.

Prof. Adrian Ionescu thanks all collaborators of 2020

Ionescu offered the best experimental Tunnel FET so far from University Lund, a vertical heterostructure InAs/GaAsSb/GaSb Tunnel FET with an Ioff=1 nA/µm, Ion=10.6µA/µm at Vdd=0.3 V and a subthreshold slope of 44 mV/dec @50mV and 48 mV/dec @300 mV. Effects of TAT on Tunnel FETs characteristics were discussed and the effect of cancellation at low temperature (<100 K).

After intense discussion on the TFETs, a combination of TFETs and MOSFETs on the same 2D material, WSe2 flakes, showed potentials in various performance parameters. Moving forward, the Negative Capacitance Devices were highlighted by Prof. Ionescu and its potentials as technology booster for MOSFETs and Tunnel FETs down to 2 nm. He offered Negative Capacitance TFET (NC-TFET) results from the collaboration of IMEC and EPFL with an improved subthreshold slope of sub-60 over about 3 decades. Further examples followed, e.g. "Si-doped HfO_2 on NW Tunnel FET Array, Subthermionic NC FET biosensor" and more.

Finally, Prof. Ionescu discussed the potentials of steep slope and energy efficiency in phase change VO_2 devices for neuromorphic applications (MIT).

After the lecture, an intense discussion followed, e.g. the increasing impact of tolerances and variability while moving towards the 100 mV regime, which acts inverse proportional, but requires extensive analyses. Discussion on the conditions to achieve the TAT suppression at 100 K followed and further questions were answered by Prof. Ionescu.

Virtual Mini-Colloquium On Compact Modeling

—by Benjamin Iñiguez and Mike Schwarz

A Virtual EDS Mini-Colloquium (MQ) on Compact Modeling was held on 17 December 2020. It was sponsored by the ED Spain Chapter, the EDS Compact Modeling Technical Committee and the Department of Electronic, Electrical and Automatic Control Engineering of the University Rovira i Virgili (Tarragona, Catalonia, Spain). The Chair of this MQ was Prof. Benjamin Iñiguez, Chair of the ED Spain Chapter and the EDS Compact Modeling Technical Committee, and Full Professor at the University Rovira i Virgili. The MQ was attended in average by 30 participants simultaneously and in total by approximately 50 researchers and engineers from academia and industry.

The Mini-Colloquium included seven talks given by EDS Distinguished Lecturers:

- Prof. Yogesh S. Chauhan (Indian Institute of Technology Kanpur) conducted the first lecture, entitled "BSIM-BULK and BSIM-HV: Industry Standard SPICE Models for Analog, RF and High Voltage Applications"
- Prof. Manoj Saxena (University of Delhi, India), addressed "Modeling and Simulation of Robust Ultrasensitive Tunnel Field Effect Transistor Design for Biosensing Applications"
- Dr. Wladek Grabinski (Grabinski Modeling Consulting, Switzerland) made a presentation on "FOSS TCAD/EDA Tools for Semiconductor Device Modeling"
- Prof. Arokia Nathan (University of Cambridge, UK) gave a talk about "Physics-Based Parameter Extraction for TFTs"
- Prof. Marcelo Pavanello (Centro Universitario FEI, Brazil) targeted "Quantum Effects on the Mobility of SOI Nanowire MOSFETs Induced by the Active Substrate Bias"
- Prof. Michael S. Shur (Rensselaer Polytechnic Institute, Troy, New York, USA) addressed "THz Compact SPICE/ADS model"
- Prof. Edmundo Gutiérrez (INAOE, Puebla, Mexico) made the last presentation, entitled "RF MOSFET degradation modeling up to 67 GHz"

The panels during the membership drive program at Universiti Teknikal Malaysia Melaka

Asia & Pacific (Region 10)

ED Malaysia Kuala Lumpur Chapter

—by Maizatul Zolkapli, Norhayati Soin, Aliza Aini Md Ralib, Rosminazuin Ab Rahim, Sharifah Fatmadiana Wan Muhammad Hatta

ED Malaysia Virtual Annual General Meeting 2021

The 31st Annual General Meeting (AGM) of ED Malaysia Chapter was held on 23 January 2021 in virtual mode due to travel restrictions and the COVID-19 pandemic. The online mode was used for the first time in the history of the ED Malaysia Chapter. Twenty-seven EDS members from all over Malaysia attended the meeting. The EDS events, activities and financial status in 2020 was presented by Dr. Maizatul and Dr. Azrif. A new executive committee was elected for a two-year term. Assoc. Prof. Ir Dr. Ahmad Sabirin Zoolfakar from Universiti Teknologi MARA was elected to chair the ED Malaysia Chapter for the term 2021–2022. During the meeting, the Best Volunteer award was presented to Prof. AHM Zahirul Alam from International Islamic University Malaysia while the Best Student Volunteer Award was presented to Loke Chun Heo from Universiti Kebangsaan Malaysia. All the outgoing executive committee members of 2020 were presented with appreciation certificates.

ED Malaysia Chapter Membership Drive and Technical Talk

The ED Malaysia chapter organized a series of virtual membership drives in conjunction with a technical talk on Effective Supervision for Undergraduate and Postgraduate Students. The activity was held at Universiti Teknikal Malaysia Melaka on 27 January 2021. About 70 people participated in the events, mainly lecturers and students.

Invent from Home: Trash to Treasure

A project "Invent from Home: Trash to Treasure" was held virtually from 11–28 January 2021 through an online platform. The program was intended to encourage school students (Primary and Secondary levels) to excite their creative minds to innovate using recycled materials. This program was also targeted at university students to play an active role in helping the community, especially school students to face the pandemic positively through this video competition. The students were requested to produce videos of 3–5 minutes duration showing their inventions using recycled materials. Twelve school students participated in the program and 10 university students participated as the organizing committee. All the participants of this program were given a certificate of participation. Photos of winners will be posted on Instagram after their announcement.

EDS EA in Webinar "IEEE R10 EA Project Opening & Funding Portal and EA products"

On 27 March 2021, the IEEE Region 10 Educational Activities Committee organized a webinar "IEEE R10 EA Project Opening & Funding portal and EA products" with the aim to provide a platform for all the IEEE members to understand on the project openings offered by IEEE Region 10 EA and the funding portals. One of the panelists, Dr. Aliza Aini, a member of the R10 Educational

Activities Committee from ED Malaysia Chapter participated in the webinar to demonstrate the funding portal website. Dr. Rosminazuin, the Educational Activities Committee member from ED Malaysia Chapter also attended the webinar. The panelists, Jamie Moesch—Managing Director Educational Activities and Lorena Garcia—IEEE EAB Pre-University Education Coordinating Committee Chair explained the EA products and provided hints on orientation in TryEngineering & STEM portal respectively. Following all the recommendations, the activities related to Pre-University Education using TryEngineering will be conducted this year by the ED Malaysia Chapter.

Let's Talk by IEEE EDS

The ED Malaysia Chapter conducted 'Let's Talk' an online technical forum series on 30 December 2020 and 25 March 2021, respectively. The invited speakers represented both the academic and the industrial background, thus allowing the audience to capture highlights from each side of the discipline. The forum on the 30 December was focused on the topic of 'Sensors' where the panel speakers were: Prof. Dr. Mohd Nizar Hamidon from the Institute of Advanced Technology (Universiti Putra Malaysia—UPM), whose topic was 'Sensor Technology and Nanotechnology', Dr. Aminuddin Ahmad Kayani from the Functional Material and Microsystems Research Group (Royal Melbourne Institute of Technology—RMIT), whose topic was 'Wearable Sensors', and Dr. Muhammad Zamharir Ahmad from Malaysian Agricultural Research and Development Institute—MARDI, whose topic was 'Sensor for Agriculture Applications'. The forum was moderated by Dr. Maizatul Zolkapli from Universiti Teknologi MARA—UiTM. The forum on the 25 March was focused on the topic of 'Optoelectronics' where the panel speakers were: Associate Professor Dr. P. Susthitha Menon from the Institute of Microengineering and Nanoelectronics—IMEN, whose topic was 'Plasmonics in Optoelectronic Devices', Professor Dr. Nowshad Amin from Universiti Tenaga Nasional—UNITEN, whose topic was 'Solar Cells as The Heart of Solar PV Technology', and Dr. Shutesh Krishnan Shastri from ON Semiconductor, whose topic was 'Sense and Sensibility—seeing the invisible with technology'—The forum was moderated by Ir. Bernard Lim from Appscard Group AS. Both forums lasted for an hour—including 30 mins Q&A with the audience. The program attracted more than 60 attendees and received positive feedback from all the participants.

13th 2021 IEEE Regional Symposium on Micro and Nanoelectronics (RSM)

The ED Malaysia Chapter is pleased to welcome everyone to participate in the 2021 IEEE Regional Symposium on Micro and Nanoelectronics (RSM) on 2–4 August 2021. Since 1997, this bi-annual technical conference aims to bring together researchers from industry and academia to gather and explore various issues and trends in the field of semiconductor electronics. This will be the 13th RSM organized by the Electron Devices Chapter of IEEE Malaysia Section and technically co-sponsored by the IEEE Electron Devices Society. Over the last twenty-four years, RSM conference series has become the prominent international forum on semiconductor electronics embracing numerous aspects of the semiconductor technology including circuit and device modelling and simulation, photonics and sensor technology, MEMS technology, packaging technology, failure analysis and reliability, materials and devices for nanoelectronics. Please visit the website for further details https://ieeemalaysia-eds.org/rsm2021.

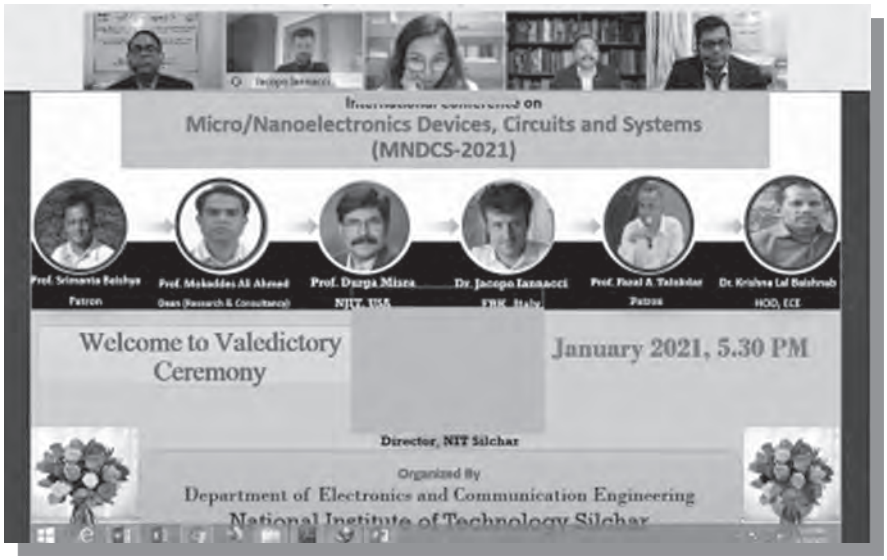
~ Sharma Rao Balakrishnan, Editor

ED NIT Silchar Student Branch Chapter

International Conference on Micro/Nanoelectronics Devices, Circuits and Systems (MNDCS-2021)

—By T. R. Lenka

The ED NIT Silchar Student Branch Chapter, Assam, India in association with IEEE Nanotechnology Council Chapter and Department of Electronics and Communication Engineering, National Institute of Technology Silchar organised an online International Conference on Micro/Nanoelectronics Devices, Circuits and Systems (MNDCS-2021) held 29–31 January 2021. The conference aimed to foster its theme through eight keynotes, four invited talks, and 56 oral presentations of research articles in the most relevant areas allied to the theme of the conference. The invited speakers were Prof. C. Jagadish and Prof. Lan Fu, ANU, Australia, Prof. Ilya Sychugov, KTH-RIT, Stockholm, Sweden, Prof. Samar Saha, Prospicient Devices, California, USA, Prof. P. Susthitha Menon, UKM, Malaysia, Prof. Zoran Jaksic and Dr. Olga Jaksic, University of Belgrade, Serbia, Prof. Yong Shi, Stevens Institute of Technology, New Jersey, USA, Prof. Hieu P. T. Nguyen, NJIT, USA, Prof. Ajay Agrawal, CEERI, Pilani, India, Mr. Ravi Teja Velpula, NJIT, USA and Dr. Jacopo Iannacci, Center for



Valedictory Ceremony of MNDCS-2021

Materials and Microsystems, Italy. The conference was attended by around 100 participants comprising IEEE EDS members and non-members including faculty members, UG/PG/Ph.D students from India and abroad.

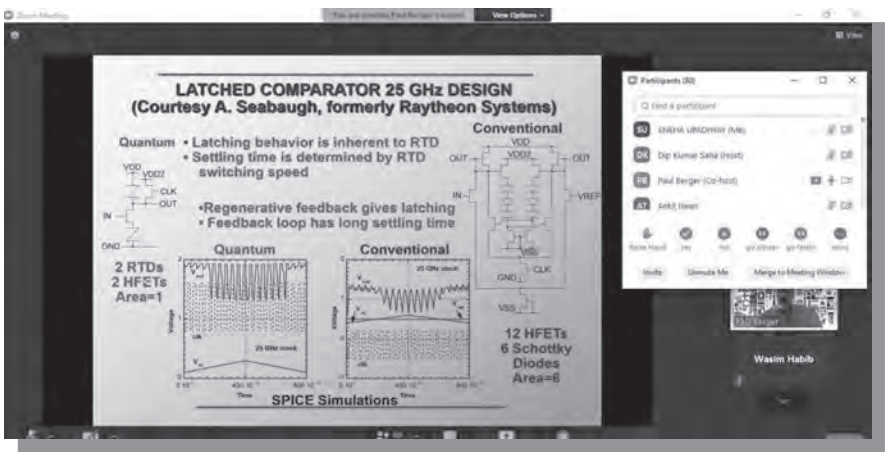
ED Netaji Subhash Engineering College Student Branch Chapter

—By Sneha Upadhyay and Saheli Sarkhel,

The ED Netaji Subhash Engineering College Student Branch Chapter in association with the GnZ Student Cell, Department of Electronics and Communication Engineering (ECE) organized an online Distinguished Lecture "Si-Based Resonant Interband Tunnel Diodes for Quantum Functional and Multi-Level Circuitry to Extend CMOS" by Prof. Paul R. Berger, Director of Organic and Printed Flexible Electronics Laboratory, Department of Electrical and Computer Engineering, the Ohio State University. The event was held on 13 February 2021 and had about 80 participants, including IEEE EDS members, B.Tech. students from 1st to 4th year of ECE department and faculty members. Prof. Berger gave a very clear and informative presentation on the latest Si-based tunnel devices and circuits and a summary of the results of device optimization and their monolithic integration with Si-based transistors. Prof. Berger also presented a range of circuit prototyping. The extension of negative differential resistance to ultra-low voltage memory was also discussed.

The presentation was followed by an interactive discussion with the participants.

On 13 February 2021, the chapter organized a one-day webinar "Ultra Low Power Logic Circuit Design Using Adiabatic Logic" by Dr. Manash Chanda, Assistant Professor, MSIT, Kolkata, and Vice Chairman, IEEE ED Kolkata Chapter. The speaker discussed fundamentals of ultra-low power logic circuit design and explained the adiabatic logic and its benefits in this circuit design. On the occasion of World Engineering Day the chapter organized a one-day webinar "Tunnel FETs: Opportunities, Trends and Challenges" by Dr. Angsuman Sarkar, professor of the department of Electronics & Communication Engineering, Kalyani Government Engineering College. The speaker explained in detail about TFETs, FinFETs and Double Gate FETs. The chapter also organized a one-day webinar on "Emerging Trends in Device Engineering for Improved Performances" by Dr. Navjeet Bagga, Assistant Professor, PDPM IIITDM Jabalpur, India. The speaker gave a brief introduction of emerging devices such as Tunnel FETs and Negative Capacitance (NC) FETs, and compared CMOS devices with the TFETs.

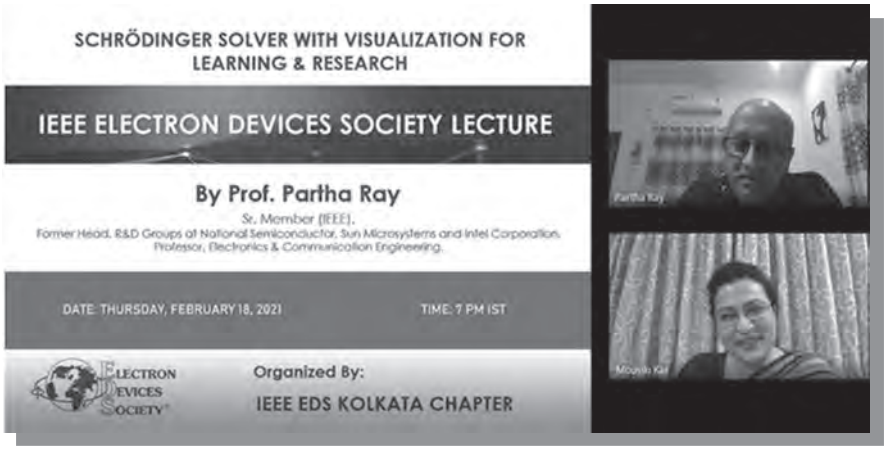


Webinar by Dr. Paul R. Berger

ED Kolkata Chapter

—By Mousiki Kar

A webinar was organized by the ED Kolkata Chapter on 18 February 2021. Dr. Partha Ray, Former Head of R&D Groups at National Semiconductor, Sun Microsystems and Intel Corporation spoke on the topic, "Schrödinger Solver with Visualization for Learning & Research." The speaker gave an elaborate demonstration of the solution of the Schrödinger equation through a visualization tool. It culminated in a deeper understanding of the



Dr. Partha Ray being greeted by Dr. Mousiki Kar

concept. The event was attended by 42 participants who were very enthusiastic about the session and had a productive after session discussion. On 30 March 2021 the Kolkata Chapter organized another webinar in association with the IEEE EDS Center of Excellence, Heritage Institute of Technology Kolkata. The speaker was Prof. Samit K. Ray, Director, S. N. Bose National Center for Basic Sciences. Dr. Ray spoke on the topic, 'Beyond Moore's Law -Towards New Generation Semiconductor Devices '. The evolution of devices over the past decades starting from point contact transistors to 1-D nanostructures and radial heterojunctions was presented in an elaborated way. The webinar was attended by 64 participants from various geographical locations of the eastern India.

ED Delhi Chapter

—By Harsupreet Kaur

The ED Delhi Chapter in association with the Department of Electronics, Sri Venkateswara College, University of Delhi, jointly organised on 20 February 2021 a webinar "Technologies' Worth Exploring" which was held in online mode. The Lecture was delivered by Dr. Ajay Aggarwal, Sr. Principal Scientist, Head of Technology Business Development Unit, CSIR-CEERI, Pilani, and Associate Dean, Engineering Sciences AcSIR. The webinar was attended by 74 students and faculty members. The talk focused on various aspects of innovative micro- and nanoscale technologies relevant to healthcare and environment care.

Department of Electronic Science, University of Delhi South Campus, and the ED Delhi Chapter jointly organized on 20 March 2021 the Annual Visitors' Program on "Recent Trends in Electronics and Communication," held in online/virtual mode. Four talks included in the programme were focused on the latest advancements and emerging paradigms in the areas of sensor technology, HEMT technology and radar systems and space technology. The first talk "*Electronics for Environmental and Healthcare Sensors*" was delivered by Dr. Ajay Aggarwal. Various aspects of the latest sensor technologies based on nanowire FETs were covered in this talk. Dr. D. S. Rawal, Scientist G and Associate Director of Solid-State Physics, Laboratory, DRDO, New Delhi, delivered the second talk on "*Advancement in AlGaN/GaN HEMT Technology for High Power, High Frequency Device Applications*." The third talk on "*Radar Technology and Trends*" was delivered by Dr. Ashotosh Kedar, Scientist F, Radar Antennas, Microwave Division, LRDE, DRDO, Bangalore. The last talk was delivered by Mr Rajiv Jyoti, Distinguished Scientist & Deputy Director, Space Application Center, ISRO, Ahmedabad on "*Space Systems: Opportunities and Challenges*." The talks were well attended by 115 students and faculty members.

ED Nepal Chapter

—By Rajendra Parajuli

The chapter organized an online seminar on 16 February 2021 on 'Strain induced electronic structure, and magnetic and structural properties in quaternary Heusler alloys ZrRhTiZ (Z = Al, In)', delivered by Dr. Gopi Chandra Kaphle (Secretary, EDS Nepal Chapter). In this talk, the electronic structure, and magnetic and structural properties of quaternary Heusler alloys ZrRhTiZ (Z = Al, In) have been analyzed from first principles calculations.

The chapter also organized a workshop on 'Experimental and Computational Approach of Metal Oxide Thin Film'. It was held on 18 and 19 March 2021 in the Department of Physics, Amrit Campus, Tribhuvan University. About 60 participants attended the workshop, 10 of whom were IEEE

Inaugural session of the workshop 'Experimental and Computational Approach of Metal Oxide Thin Film'

members. The workshop was supported by the International Science Program, Uppsala University, Sweden. In this workshop, women were given priority and a third of participants were women. The workshop topics were presented by national and international experts in the respective fields.

~Soumya Pandit, Editor

IEEE EDS Annual Meeting –ED Japan Joint Chapter

—by Toshiro Hiramoto and Masaharu Kobayashi

On 10 February 2021, the annual meeting of the EDS Japan Joint Chapter was held via the Webex platform. Prof. Toshiro Hiramoto, the Joint Chapter Chair and Dr. Nobuyuki Sugii, the Vice-Chair, reported 2020 activities and 2021 plans of the Chapter. Next, the 2020 EDS Japan Joint Chapter Student Awards (VLSI & IEDM) were presented to 5 students, who made excellent presentations at the VLSI Symposia 2020 and IEDM 2020. The award winners are posted on the Japan Joint Chapter's webpage: http://www.ieee-jp.org/japancouncil/chapter/ED-15/ed15_award.htm.

After the annual meeting, the IEDM 2020 Report Session was held. 8 members of the IEDM program committee reported on summary, topics, and research trends of their sub-committees for more than seventy attendees. The session provided a good opportunity for the attendees to touch the latest technology trends, especially for those who were unable to attend the IEDM.

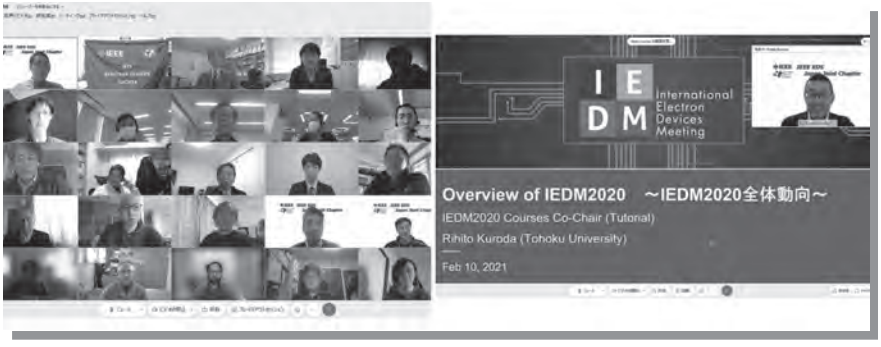
ED Tainan Chapter

— by Wen-Kuan Yeh

The ED Tainan Chapter, Taiwan Semiconductor Research Institutes (TSRI), and Synopsys Taiwan co-organized a Sentaurus TCAD workshop at TSRI, HsinChu, Taiwan on 26 March 2021. Four plenary presentations and four training courses were held in one day. This workshop focused on the development of Technology Computer-Aided Design (TCAD) for semiconductor devices and processes simulation. The workshop introduced the role of TCAD including: 3D structural simulation based on process flow, material modeling both macroscopic and atomistic, and process modeling. The exciting new TCAD modeling methodologies and challenges were also discussed.

Director Z.Q. Wu from TSMC gave a first talk on the topic "The expanding role of TCAD in semiconductor R & D". TCAD has a long history since the 1960s, first focused on modeling of semiconductor devices formed by implantation and diffusion, and has been instrumental in predicting device characteristics and guiding the process of fabricating such devices. The success of continued scaling of semiconductor technologies based on the famous Moore's Law pushed semiconductor technology toever increasing complexity including intricate 3D structures, advanced materials, complex processes, and equipment, etc. Optimization of these solely by experiments becomes increasingly difficult and costly. Therefore, computer simulations have become critical in the success of semiconductor technology development. Terry Ma, a Vice President of Synopsys in charge of the TCAD Business Unit, gave a second talk"Unleashing the Power of Smart Technology Development". He presented TCAD products and services to address semiconductor R&D needs for pathfinding and technology development. Prof. M. H. Chiang from National Cheng Kung University gave a third talk "Atomic-scale materials modeling and applications". The investigation for advanced materials, nanostructures, and nanoelectronic devices through ab-initio and NEGF calculation with Quantum ATK platform was briefly presented. The background of DFT-LCAO (density functional theory, linear combination

The Student Award ceremony held via Webex virtual format on 10 February 2021



The presentation by Prof. Rihito Kuroda (Tohoku University) in the IEDM 2020 report session. EDS Annual meeting; Japan Joint Chapter; 10 February 2021

Sentaurus TCAD workshop; Tainan Chapter; 26 March 2021

of atomic orbital) based on Kohn-Sham and NEGF was conceptually introduced. Next, the structure modeling was shortly described, including data importing, structure setup, and optimization. Finally, some applications of material analysis and electronic characteristics were demonstrated. Prof. Bin Su from National Yang Ming Chiao Tung University gave a fourth talk "Variability Studies of Ferroelectric FET Nonvolatile Memories enabled by TCAD." With an HfO_2-based ferroelectric compatible with CMOS process, the ferroelectric field-effect transistor (FeFET) has emerged as a strong competitor for future memory solutions and the FeFET-based embedded nonvolatile memory (NVM) integrated into leading-edge logic technology has been demonstrated. For scaled FeFET NVMs, however, the random variability is expected to be an important issue. Based on TCAD, the variations induced by the random FE-DE phase distribution and the interface trapped charges for scaled FeFET NVMs were discussed in this talk.

About 90 attendees including students, professors of universities, and engineers from HsinChu Science Park attended this workshop.

ED Beijing Chapter

—by Tianrui Cui

On 22 January 2021, EDS Beijing Chapter and 12th Research Institute of China Electronics Technology Group Corporation held a symposium on "The Development of High-Power Microwave Source Technology."

The symposium organizers invited Dr. Shengen Li and Dr. Jiandong Lang to give academic reports respectively, which were entitled "igh power microwave weapons and the development of microwave source" and "The new methods and the technical difficulties of the high-power magnetron development." The symposium focused on the present situation and the development of high-power microwave sources, new trends of high-power magnetron' s development and basic requirements, etc. Many young researchers working on the frontline participated in the technical symposium.

On 14 March 2021, EDS Beijing Chapter and 12th Research Institute of China Electronics Technology Group Corporation organized an academic seminar on strip injection technology.

Prof. Zhaoyun Yun and Prof. Yanyu Wei, both from School of Electronic Science and Engineering, University of Electronic Science and Technology of China, gave reports entitled "Research Progress of Terahertz Strip-Induced TWT" and "Research Progress of Strip-Injecting Sinusoidal Waveguide Traveling Wave Devices at Home and Abroad". Dr. Zhao Ding, an associate researcher of the Institute of Space and Space Information Innovation, Chinese Academy of Sciences, gave a report entitled "Research and Prospects of Strip Injecting Vacuum Electronic Devices". Senior engineer Zhang Changqing, from the 12th Research Institute of China Electronics Technology Group Corporation, gave a report entitled "G-band banded TWT". In addition to the reports mentioned above, Ph.D students Wei Shao, Ningjie Shi, and Hexin Wang from the University of Electronic Science and Technology of China, gave the reports entitled "Theoretical and experimental study of strip-injection terahertz TWT" and "New terahertz high-gain TWT" and "Plane miniaturization of low voltage TWT" respectively.

~Ming Liu, Editor

A Symposium "The Development of High-Power Microwave Source Technology"; ED Beijing Chapter; 22 January 2021

EDS MEETINGS CALENDAR

THE COMPLETE EDS CALENDAR CAN BE FOUND AT OUR WEB SITE: HTTP://EDS.IEEE.ORG. PLEASE VISIT.

2021 IEEE International Interconnect Technology Conference (IITC)	05 July – 08 July 2021	Virtual Event
2021 9th International Symposium on Next Generation Electronics (ISNE)	10 July – 12 July 2021	Changsha, China
2021 IEEE International Flexible Electronics Technology Conference (IFETC)	08 Aug – 11 Aug 2021	Virtual Event
2021 35th Symposium on Microelectronics Technology and Devices (SBMicro)	22 Aug – 26 Aug 2021	Campinas, Brazil
2021 28th International Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD)	01 Sept – 04 Sept 2021	Kyoto, Japan
2021 IEEE 32nd International Conference on Microelectronics (MIEL)	12 Sept – 14 Sept 2021	Virtual Event
2021 International Semiconductor Conference (CAS)	06 Oct – 08 Oct 2021	Virtual Event
2021 16th European Microwave Integrated Circuits Conference (EuMIC)	10 Oct – 11 Oct 2021	London, United Kingdom
2021 IEEE/ACM International Conference On Computer Aided Design (ICCAD)	31 Oct – 03 Nov 2021	Munich, Germany
2021 IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)	06 Nov – 08 Nov 2021	Redondo Beach, CA, USA

2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)	05 Dec – 08 Dec 2021	Monterey, CA, USA
2021 IEEE 52nd Semiconductor Interface Specialists Conference (SISC)	08 Dec – 11 Dec 2021	San Diego, CA, USA
2021 IEEE International Electron Devices Meeting (IEDM)	11 Dec – 16 Dec 2021	San Francisco, CA, USA
2021 16th European Microwave Integrated Circuits Conference (EuMIC)	14 Feb -15 Feb 2022	London, United Kingdom
2022 IEEE 34th International Conference on Microelectronic Test Structures (ICMTS)	20 Mar – 23 Mar 2022	Cleveland, OH, USA
2022 IEEE International Reliability Physics Symposium (IRPS)	27 Mar – 31 Mar 2022	Texas, USA
2022 23rd International Vacuum Electronics Conference (IVEC)	25 April – 28 April 2022	Monterey, CA, USA

Executive Summary of the 2021 IEEE Latin American Electron Devices Conference

By Fernando Guarin

LAEDC is the flagship Latin American electron device conference fully sponsored by the IEEE Electron Devices Society, (https://attend.ieee.org/laedc-2021/). It's main goal is to bring together specialists from all Electron Device related fields. The third edition of LAEDC took place from 18-21 April 2021 as a virtual conference. The 2021 LAEDC more than doubled last year's attendance and was a very successful event despite the challenging restrictions and uncertainties brought about by the global pandemic.

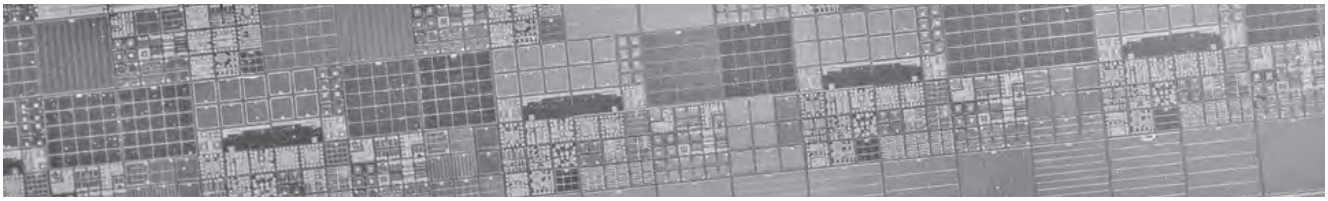
As a growing event, the number of paper submissions and participation for this year was higher than in previous editions, with a total of 194 registered participants representing more than 30 different countries from Asia, Europe, and the Americas. The conference had great student and young professional attendance with 104 registered attendees from those groups.

The technical program included a free MOS-AK workshop "*Enabling compact modeling and research exchange*," a panel session in Humanitarian Technology, 12 poster and project presentations, one networking session, a total of 70 technical presentations with over 30 invited speakers and three keynote presentations. The event with the highest attendance was the YP/WIE Networking Session with 145 guests, followed by the keynote presentation by Dr. Martin Green "*Can Solar PV save the World*," with more than 90 attendees. All of these sessions were available On Demand until 31 May in our virtual platform Engagez. The videos will be posted in the EDS Resource Center.

Proceedings will be published by IEEE and the accepted papers will be available on IEEE *Xplore*. Outstanding scientific papers presented in the conference will be considered for a publication in a special issue of the *IEEE Journal of the Electron Devices Society* (J-EDS).

As main sponsors for this event, we appreciate financial support received from EDS, Intel, IEEE Humanitarian Activities Committee (HAC), and IEEE Women in Engineering Affinity Group (WIE). We would also like to extend our appreciation to the technical sponsors; IEEE Industrial Electronics Society (IES), and IEEE Society on Social Implications of Technology (SSIT).

On behalf of the organizing committee, we would like to thank all your contributions and active participation and we look forward to seeing you next year at LAEDC, which we intend to offer as a hybrid conference.



IEEE Transactions on Semiconductor Manufacturing CALL FOR PAPERS for Special Issue on "*Process-Level Machine Learning Applications in Semiconductor Manufacturing*"

IEEE
Advancing Technology for Humanity

The constantly increasing availability of data, the rapid expansion in computational and storage capacities of IT systems, and algorithmic advances in Machine Learning (ML) and Artificial Intelligence (AI) are making a huge impact in the manufacturing industry for improving efficiency, operations and throughput. The semiconductor industry, being one of the most data-intensive industries, has seen in the past years the diffusion of several ML-based technologies. In order to develop effective ML-based technologies in the semiconductor manufacturing industry several issues have to be taken into account (scalability, heterogeneity of data, need for interpretability just to name some aspects): such a complex industrial environment calls for non-trivial ML approaches.

The objective of this Special Issue is to showcase real-world applications and algorithmic advancements of ML and AI-based technologies for process modeling and process optimization in semiconductor manufacturing. We are interested in contributions from both industrial practitioners and academics. We invite contributions that are based on (but not limited to) the following topics:

- Virtual Metrology;
- Predictive Maintenance;
- Sensor-based Fault Detection;
- Sensor-based Anomaly Detection;
- Image-based Defect Pattern Classification;
- Image-based Defect Classification;
- Dynamic Sampling;
- Cross-module process control;
- Machine learning applications in yield management and yield learning;
- Applications of AI/ML to Optical Proximity Correction algorithms for patterning.

Important Dates

- Paper submission deadline: August 31, 2021
- Completion of the first round review: November 30, 2021
- Completion of the second round review: January 31, 2022
- Final submission due: March 31, 2022
- Tentative publication date: June 1, 2022.

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Paper Submission

All papers are to be submitted through the IEEE 's **Manuscript Central** for Transactions on Semiconductor Manufacturing https://mc.manuscriptcentral.com/tsm-ieee. Please select "Special Issue" under Manuscript Category of your submission. All manuscripts must be prepared according to the IEEE Transactions on Semiconductor Manufacturing publication guidelines https://eds.ieee.org/publications/transactions-on-semiconductor-manufacturing. Please address inquiries to gianantonio.susto@unipd.it.

EDS Vision, Mission and Field of Interest Statements

Vision Statement
Promoting excellence in the field of electron devices for the benefit of humanity.

Mission Statement
To foster professional growth of its members by satisfying their needs for easy access to and exchange of technical information, publishing, education, and technical recognition and enhancing public visibility in the field of Electron Devices.

EDS Field of Interest
The EDS field-of-interest includes all electron and ion based devices, in their classical or quantum states, using environments and materials in their lowest to highest conducting phase, in simple or engineered assembly, interacting with and delivering photo-electronic, electro-magnetic, electromechanical, electro-thermal, and bio-electronic signals. The Society sponsors and reports on education, research, development and manufacturing aspects and is involved in science, theory, engineering, experimentation, simulation, modeling, design, fabrication, interconnection, reliability of such devices and their applications.