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75TH ANNIVERSARY OF THE TRANSISTOR

HISTORY AND EMERGING DESIGNS OF POWER TRANSISTORS

B. JAYANT BALIGA

NORTH CAROLINA STATE UNIVERSITY

Electricity was playing a major role in the lives of people by the middle of the 20th century. Electric lighting, pioneered by Edison, had improved productivity, quality of life, and safety by illumination of our streets, factories, and residences. Refrigeration, enabled by efficient motors, had transformed the storage of perishable foods in homes while preserving them during delivery from farms to the market. The replacement of mechanical actuators for these application with electronic switches became a possibility after the invention of the bipolar transistor (Shockley, Bardeen, and Brattain, Bell Labs, 1947). For applications operating at high power levels, the ideal electronic switches must exhibit the following characteristics: (a) high voltage blocking capability; (b) low on-state voltage drop to reduce conduction losses; (c) fast switching capability for the voltage and current to minimize switching losses; (d) ability to tolerate simultaneous imposition of high voltage and current during the switching transient for ruggedness; (e) control of current using a small voltage with low drive currents to allow integration of the drive electronics; and (f) current saturation under drive voltage control to avoid the need for snubber elements. In addition, an ideal power transistor should be able operate symmetrically in the first and third quadrants. The quest to create a power transistor that satisfies these requirements has driven innovations in the technology during the last 60 years.

This article highlights important power transistor innovations that have occurred since the 1960s allowing displacement of analog power control (phase control) with digital power control (pulse width modulation). These innovations initially required changes in device architecture and physics for silicon based transistors. Subsequently, even greater performance enhancements were achieved by



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HISTORY AND EMERGING DESIGNS OF POWER TRANSISTORS

(continued from page 1)

replacing silicon with wide band gap semiconductor materials.

The power bipolar transistor architecture (Fig. 1 left) was a departure from the signal transistor due to the need for supporting the high voltages and controlling the high currents required in power applications. The power transistor requires a vertical structure with one of the high current terminals (collector) located at the bottom of the chip, with the other high current terminal (emitter) formed at the top. The base terminal must be interdigitated with the emitter because on-state current flow concentrates at the emitter edges due to the emitter crowding effect. A thick drift region with low doping concentration is required to support the high voltages, resulting in a large on-state resistance despite some conductivity modulation. Most significantly, a large base width is necessary to avoid reach-through limited breakdown, resulting in a low current gain (typically < 10 in the on-state). A large reverse base drive current is needed during turn-off

to shorten the storage time, resulting in a current gain of only 2. Bulky and complex base drive circuits were consequently needed, which created reliability issues. The safe operating area of the power bipolar transistor was also poor, making addition of snubber components necessary.

The Darlington power bipolar transistor (Fig. 1 right) was developed to ameliorate the problem with low on-state current gain. It utilizes a base drive transistor T_1 to provide drive current to the output transistor T_2 , as shown by its equivalent circuit in Fig. 1. This approach allowed increasing the current gain in the on-state but the turn-off gain was still poor. More significantly, the Darlington power transistor has a diode-like on-state characteristics because of current flow of transistor T_1 through the base-emitter junction of transistor T_2 . This makes its on-state voltage drop much larger than the single bipolar transistor.

The availability of the CMOS technology for integrated circuits enabled making power Metal-Oxide-Semi-

conductor Field Effect Transistors (MOSFETs) in the 1970s. The double-diffused or D-MOSFET (Fig. 2 left) was first commercialized by several companies (International Rectifier, Siliconix). Its channel length is determined by the difference in diffusion depths of the P-base and N+ source regions, allowing short channel length (1 to 1.5 μm) to be achieved with 5 μm lithography process tolerances at that time. This device also has a vertical structure that contains a thick drift region with low doping concentration to support high voltages. It adds substantial on-state resistance for devices with high blocking voltages. On-state current flow occurs when a positive gate drive voltage is applied to the gate to induce an inversion layer at the surface of the P-base region to create a channel. The resistances of the channel and JFET regions contribute substantially to the total on-resistance for devices with low blocking voltages ($< 100\text{ V}$). This device exhibited most of the desired characteristics for the

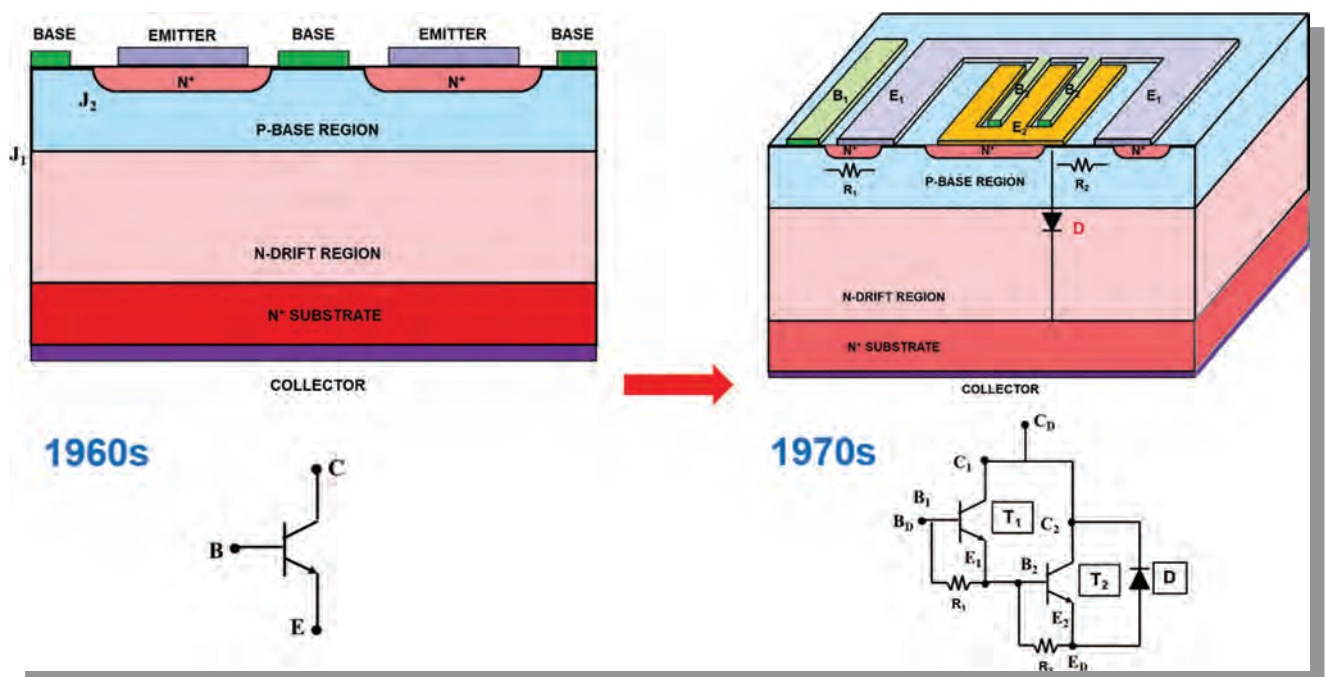


Figure 1. Evolution of Power Bipolar Transistors.

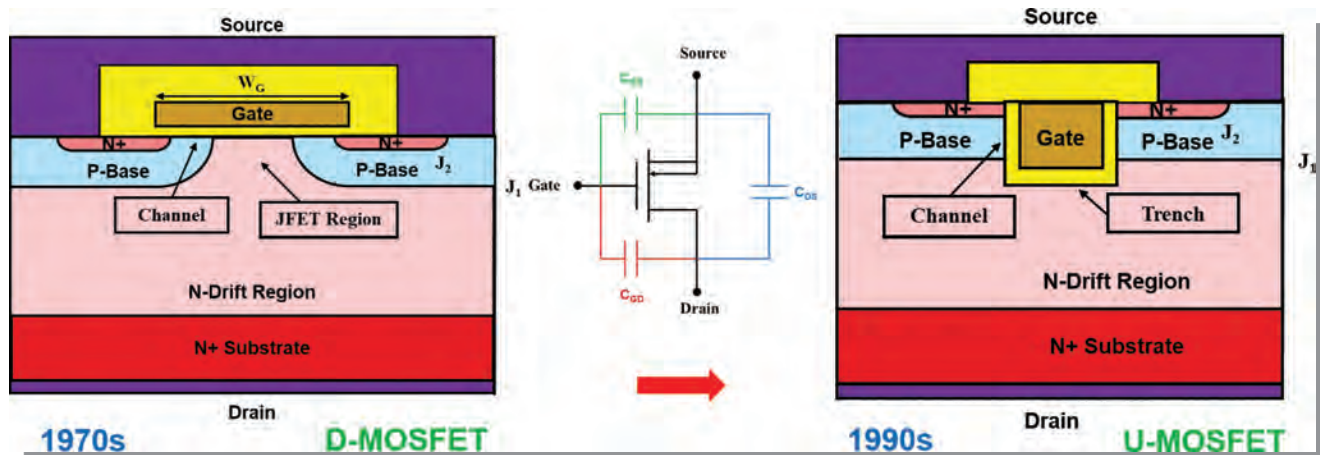


Figure 2. Evolution of Power Metal-Oxide-Semiconductor Field Effect Transistors.

ideal electronic switch when the blocking voltage was less than 100 V.

The quest to realize lower on-resistance lead to the introduction of the power U-MOSFET (Fig. 2 right) by the industry in the 1990s (Siliconix). The JFET region resistance was eliminated using this structure allowing increasing the channel density as well. The U-MOSFETs reduced the on-resistance by a factor 3x for devices with 30V ratings. However, the input capacitance for the devices (C_{GS} in the equivalent circuit in Fig. 2) increased substantially slowing down the switching speed. However, the overall performance im-

provement made this structural design dominant in the 1990s.

A major breakthrough in enhancing the performance of silicon power MOSFETs occurred with the introduction of the two-dimensional charge-coupling concept in the 1990s. The first approach (Baliga, NCSU, U.S. Patent 5,637,898, 1997) was proposed with a source electrode inside a deep trench to produce the desired 2D charge-coupling. The GD-MOSFET (Fig. 3 left) with a linearly graded doping profile in the drift region was shown to greatly improve the electric field distribution in the drift region, al-

lowing increasing its doping concentration far above ($> 10\times$) that possible with the previous designs shown in Fig. 2. This approach reduced the drift region resistance well below what was previously considered the limit for ideal on-resistance for silicon material. The device structure, now commonly called the split-gate MOSFET (a misnomer because it contains only one gate electrode), has become the most popular product manufactured by leading power device companies (Alpha and Omega, Infineon) with blocking voltages up to 150 V. These devices are widely used for building

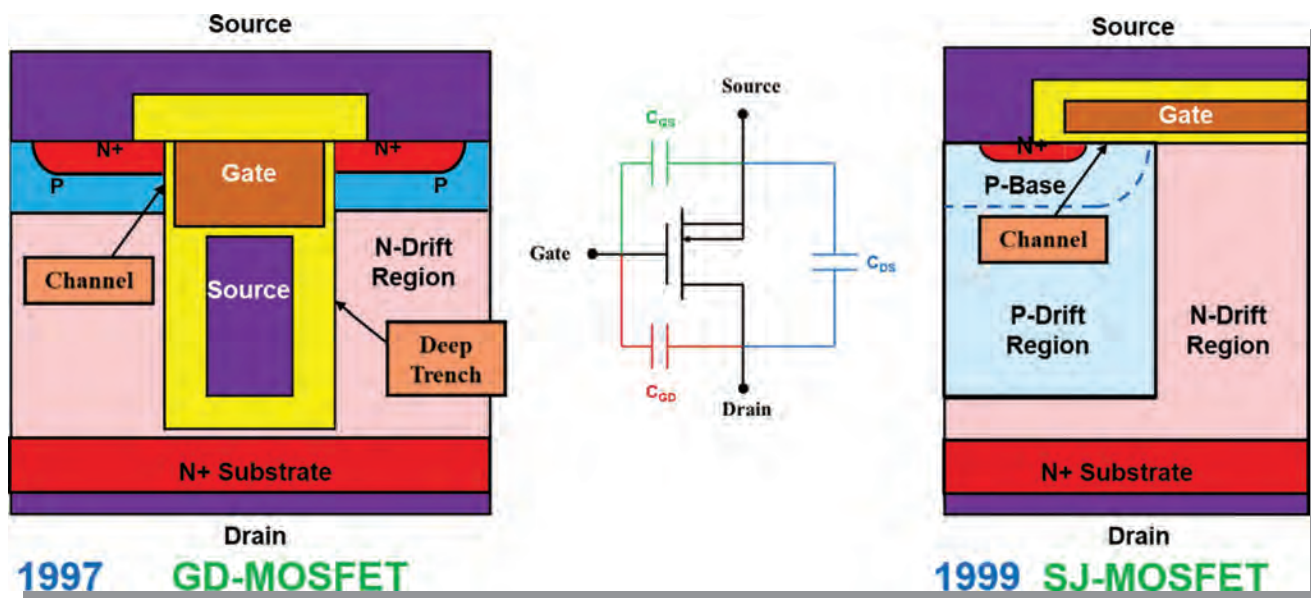


Figure 3. Evolution of Power Metal-Oxide-Semiconductor Field Effect Transistors.

power supplies to serve microprocessors and graphics chips in desktop and laptop computers.

The second approach (Lorenz, Infineon, ISPSD 1999) utilized a vertical junction produced by the addition of a deep P-type drift region operating in parallel with the N-type drift region to achieve the 2D charge-coupling. This device design (Fig. 3 right), commonly referred to as the super-junction (SJ) MOSFET, has become popular for making products with blocking voltages of 600 – 900 V. These devices are used in motor drive applications when switching losses are dominant. Products are available from many companies. (Infineon, ST Microelectronics).

The Insulated Gate Bipolar Transistor (IGBT) was invented, developed and commercialized in the early 1980s to replace the bipolar junction transistor due to its many short-comings (Baliga, General Electric, U.S. Patent 4,969,028, Filed 1980, Issued 1990). The device structure (Fig. 4 left) can be designed to be capable of blocking voltage in the first and third quadrant (Symmetric IGBT) at junctions J_1 and J_2 or only in the first quadrant (Asymmetric IGBT). The IGBT operates by creating an MOS-channel using a positive gate bias, which delivers the base drive current to the internal wide-base P-N-P bipolar transistor. Collector cur-

rent flow is generated using both electrons via the channel and holes via the P-N-P transistor within the same drift region. The device can be turned-off by reducing the gate voltage to zero to shut off the electron supply. The holes in the drift region are removed by recombination, creating a current tail that produces switching losses.

The proposed IGBT design was a radical departure because of employing a wide-base P-N-P transistor rather than the narrow-base N-P-N transistors used for power transistors at that time. Skeptics believed that this would severely limit the current flow making the device inferior to power bipolar transistors. My analysis, based upon high level injection physics within the N-base region (N-drift region), predicted P-i-N rectifier like on-state characteristics with low on-state voltage drop even at high current densities. This analysis was fortunately proven to be correct when actual devices were fabricated and tested.

A major hurdle for the IGBT was potential latch-up of the internal 4-layer thyristor, which could result in destructive failure. This issue was overcome using the deep P^+ region (Fig. 4 left) added to the basic double-diffused MOSFET process (Baliga and

Adler, General Electric, U.S. Patent 4,443,931, 1984). The IGBT was then believed to be limited to low operating frequencies, thus constraining its applications, because methods to control the minority carrier lifetime at that time led to damaging the MOS gate structure. Fortunately, I discovered a process that allowed using high energy electron irradiation to reduce the lifetime in the drift region followed by a low temperature annealing process that removed the damage in the gate oxide. This was crucial to creating IGBTs that could operate over a large range of switching speeds (Baliga, IEEE EDL, 1983), opening up a wide spectrum of applications within GE at first and then beyond.

Based on my pitch in November 1980 projecting wide-spread impact of the IGBT within the Motor Drives, Lighting, Appliances, and Medical divisions at the General Electric Company, the Chairman, Jack Welch, approved full support for my development and commercialization of the IGBT. Based on this support, I was able to engineer and build the IGBT directly in the power MOSFET manufacturing line in less than 10 months. This had to be accomplished with no flaws during chip design and process definition, to ensure first pass success, due to the intense corporate scrutiny.

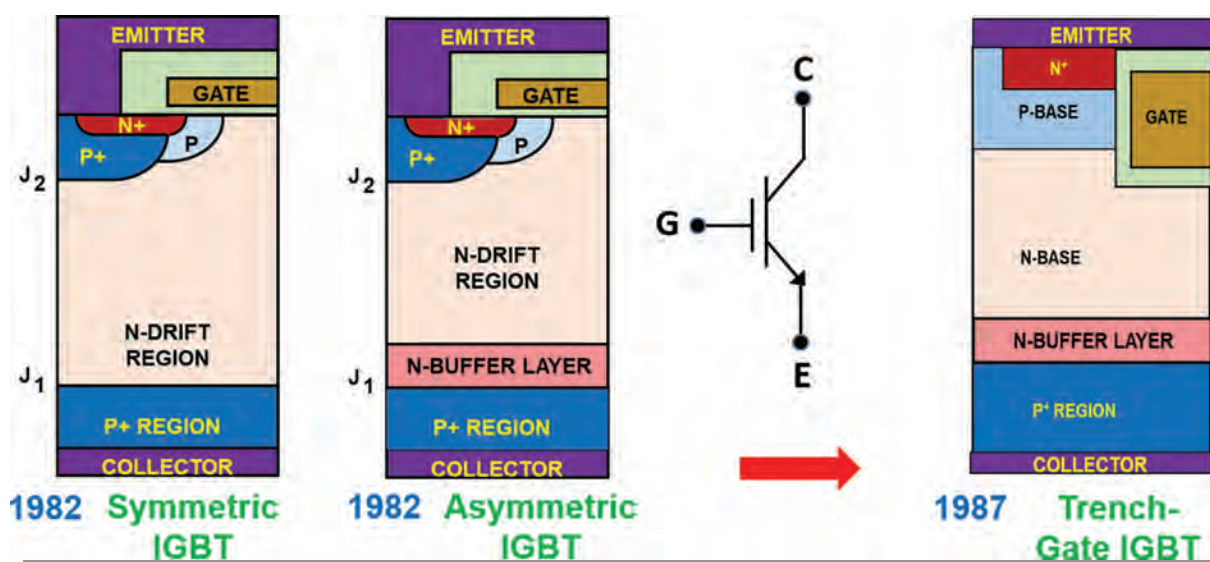


Figure 4. Evolution of Insulated Gate Bipolar Transistors (IGBTs).

This was a critical step in making the IGBT available in large quantities for use at GE to build the first adjustable speed motor drives for heat pumps, and novel lamps that were precursors of the compact fluorescent lamps that became commercially viable in the 1990s. Jack Welch embargoed any publication of information regarding the IGBT due its value to GE applications. This embargo was eventually broken by announcement of an IGBT product D94F4 by the Semiconductor Products Division in June 1983. It's applications were promoted by GE (Baliga and Smith, IEEE APEC, 1983), which resulted in a "Product of the Year" Award. After the release of my publications by GE on the attributes of the IGBT from 1983 to 1985, products were developed and introduced by many companies (Toshiba, Mitsubishi Electric, Fuji Electric) in Japan starting in 1985.

IGBT innovations were also made in Europe (ABB, Siemens) in the 1990s with the transparent emitter design (Fig. 5 left). The P⁺ emitter region was replaced with a thin P-diffusion on the bottom of the wafer with low doping concentration to reduce the injection efficiency. This was found to reduce switching losses for very high voltage

(> 4 kV) devices required to replace gate-turn-off (GTO) thyristors used for electric locomotive drives. This technology was rapidly optimized in Europe and Japan for wide spread use in urban and long distance public transportation.

An improvement to the trade-off between the on-state voltage drop and switching speed for the IGBT was achieved by employment of the trench-gate structure (Chang and Baliga IEEE IEDM, 1987). The trench-gate design (Fig. 4 right) increases channel density, providing more drive current to the internal bipolar transistor, to reduce on-state voltage drop. Another IGBT design innovation that was shown to improve the performance of high voltage IGBT devices was the deep trench structure (Toshiba, IEEE ISPSD, 1998) with a narrow P-base region (Fig. 5). This approach enhanced the conductivity modulation of the drift region resulting in lower on-state voltage drop.

Over the last 4 decades, the IGBT has become very popular for a large variety of applications (Baliga, The IGBT Device, Elsevier, 2015). It is used in all sectors (transportation, lighting, consumer, industrial, medical, etc.) of the economy to enhance the quality

of life for billions of people around the world. The creation of the electronic ignition system using IGBTs for gasoline powered cars and trucks has reduced gasoline consumption by 1.8 trillion gallons from 1990-2020. The development of adjustable speed motor drives using IGBTs has reduced electricity consumption by 73,000 Tera-Watt-Hours from 1990-2020. The deployment of 20 billion compact fluorescent lamps using IGBT electronic ballasts has reduced electricity consumption by 59,900 Tera-Watt-Hours from 1990-2020. These applications of the IGBT have saved consumers \$ 33.6 Trillion while reducing carbon-dioxide emissions by 181 Trillion pounds from 1990-2020 to mitigate global warming.

All solar and wind power generation relies upon using the IGBT to convert the energy into a stable 50 or 60 Hz AC power that can be delivered to the grid. In addition, the IGBT is used for the inverters for driving the motors in electric cars manufactured by all automobile companies. It will therefore play an essential role in the elimination of fossil fuels in the electricity generation and transportation sectors to combat climate change.

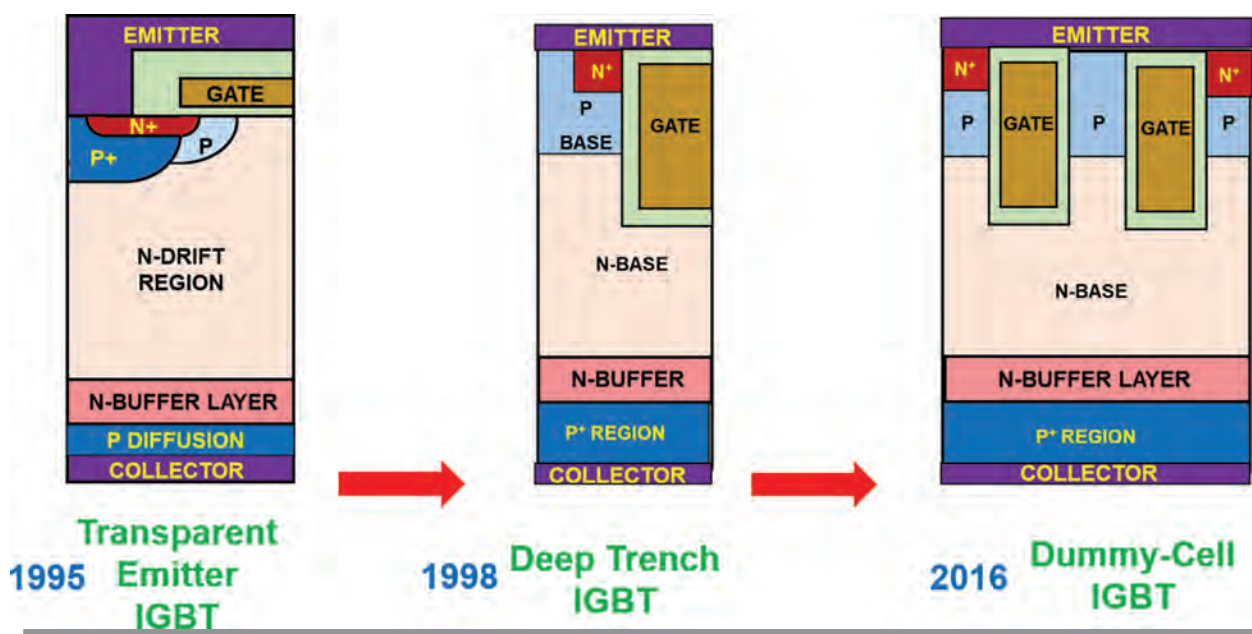


Figure 5. Evolution of Insulated Gate Bipolar Transistors (IGBTs).

The history of evolution of power devices includes a quantum leap in performance that was enabled by wide band gap semiconductor materials. The impact of replacing silicon with wide band gap semiconductors was first recognized by the derivation of an equation relating the drift region resistance in a vertical unipolar power device to the basic material properties, now commonly called Baliga's Figure-of-Merit or BFOM (Baliga, GE, JAP, 1983; IEEE EDL, 1989). This equation predicted 13.7-fold reduction in resistance by using gallium arsenide and more than 100-fold reduction in resistance by using silicon carbide (SiC). The theory was validated in the 1990s, after the availability of 6H-SiC wafers, by fabricating 400 V Schottky rectifiers (Bhatnagar, McLarty and Baliga, IEEE EDL, 1992) and subsequently the first high performance SiC power MOSFETs. (Shenoy and Baliga, IEEE EDL, 1997). This required altering the power MOSFET structure to (a) shield the P-base region to prevent reach-through breakdown; (b) shield the gate oxide from high electric fields; and (c) employing accumulation channels to increase the channel mobility. The 4H-SiC planar-gate MOSFET structures that are now commercially available employ the shielded structures (Baliga, NCSU, U.S. Patent 5,543,637, 1996) with accumulation or inversion channels (Fig. 6).

The D-MOSFET process used for silicon power MOSFETs cannot be used for SiC devices due to insignificant diffusion of dopants in this material even at very high temperatures that lead to sublimation. The channel is therefore formed by staggered ion-implantation of the P and N-type dopants used to form the P-base and N⁺ source regions (Bhatnagar and Baliga, U.S. Patent 5,322,802, 1994; Shenoy, Cooper and Melloch, IEEE EDL, 1997). This requires high resolution photolithography to create the sub-micron channel lengths needed to achieve a low on-state resistance in the power MOSFETs. Commercial SiC planar-gate power MOSFETs are

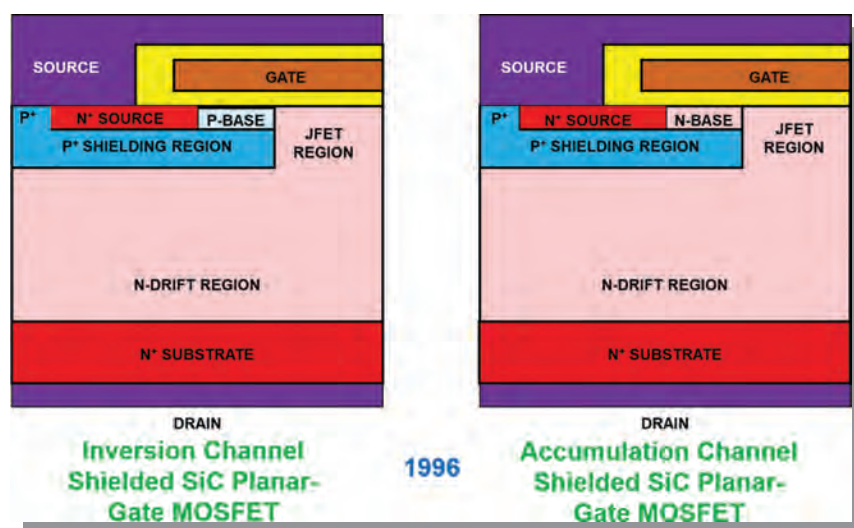


Figure 6. Evolution of Planar-Gate Silicon Carbide Power MOSFETs.

manufactured using this technology.

The reduction in switching power losses in motor drives by replacement of silicon IGBTs with SiC power MOSFETs was projected (Baliga, NCSU, Proceedings IEEE, 1994) and subsequently experimentally demonstrated (Fabre, et al., ALSTHOM, IEEE TPE, 2015). However, the cost of SiC power MOSFETs is at present more than 3-times that for the equivalent rated silicon IGBT, impeding its commercial viability. The strategy undertaken by the industry to overcome the higher cost of this technology is to operate the power electronics at a much higher frequency to reduce the cost of passive elements, such as inductors and filters, to offset the semiconductor cost. The operation of SiC power MOSFETs at higher frequencies requires design innovations to reduce drain current and voltage transient times during switching. Faster drain voltage transient times during switching can be achieved in SiC power MOSFETs by reducing the gate-drain charge.

One innovative design (Fig. 7 left) to achieve this employs a central-implanted P⁺ region inside the JFET region (Zhang, et al., CREE, IEEE ISPSD, 2015). Additional process steps are required to add the P⁺ region and it must be connected to the source electrode orthogonal to the

cross-section. The second innovative approach (Fig. 7 middle) is the split-gate device design (Han, Baliga, and Sung, NCSU, IEEE EDL, 2017) where the width of the gate electrode is shortened over the JFET region. This design reduces the gate-drain charge by a factor of 2.4-times without any additional process steps. The third innovative design approach (Fig. 7 right) is the buffered-gate design (Han, Baliga, and Sung, NCSU, IEEE EDL, 2018) where the edge of the P⁺ shielding region is extended beyond the edge of the split-gate electrode. This design reduces the gate-drain charge by a factor of 6-times but requires an additional process step to include a second JFET region.

In typical voltage source inverters using the H-bridge topology with silicon IGBTs, it is necessary to connect an anti-parallel diode for operation of the adjustable speed drive for motors. In principle, the anti-parallel diode is not required for the SiC power MOSFET due to current flow via the P-N body diode. However, this approach has been found to result in high switching power losses due to the bipolar diode reverse recovery phenomenon at elevated temperatures. In addition, a phenomenon called bipolar degradation of the SiC power MOSFET was discovered where defects are generated in the

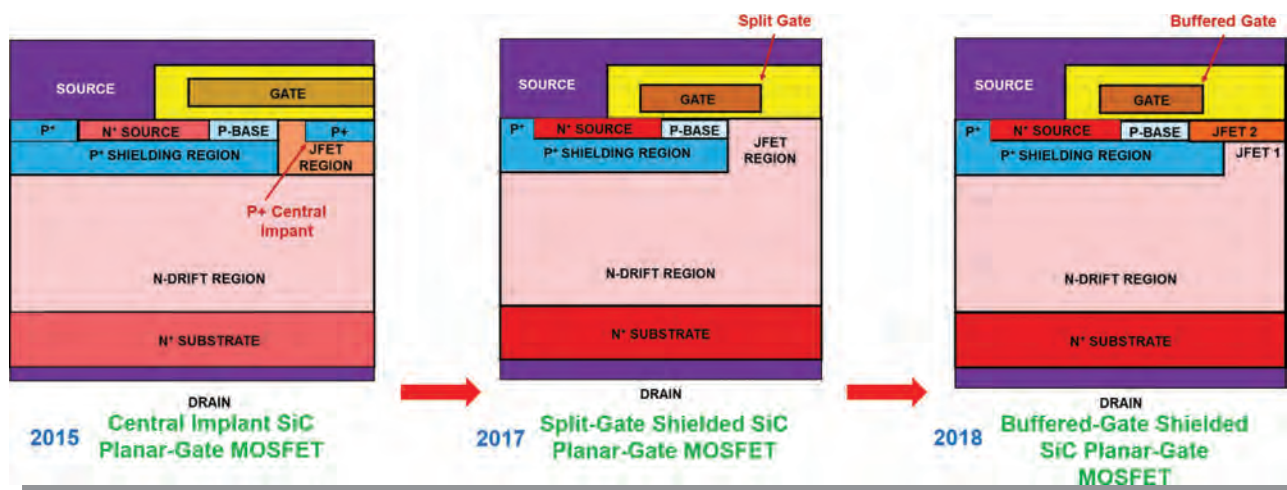


Figure 7. Evolution of Planar-Gate Silicon Carbide Power MOSFETs.

drift region due to the P-N diode bipolar current flow. A discrete junction barrier controlled Schottky (JBS) diode (Baliga, GE, IEEE EDL, 1984; Held, Kaminski, and Niemann, ABB, Material Science Forum, 1998) can be connected across the SiC power MOSFET to prevent current flow via the body diode. This adds another packaged component with significant SiC chip area and cost. An innovative design (Fig. 8) integrates the JBS diode into the SiC power MOSFET cell structure (Sung and Baliga, NCSU, IEEE EDL, 2016). This structure was created by engineering the source contact process to simultaneously

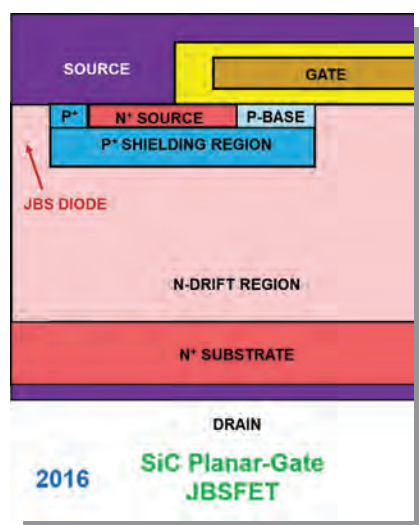


Figure 8. Evolution of Silicon Carbide Power MOSFETs.

make a Schottky barrier contact to the drift region at the JBS diode and ohmic contacts to the N⁺ source and P⁺ shielding regions.

As in the case of silicon power MOSFETs, trench-gate technology can be employed for SiC power MOSFETs to reduce the on-state resistance due to elimination of the JFET region and increase in channel density. The major challenge for this approach is a very high electric field in the gate oxide at the bottom of the trench that can lead to unreliable operation and even catastrophic failure. The first innovative design (Fig. 9 left) to solve this problem utilizes a P⁺ shielding region at the bottom of the trench which is connected to the source electrode orthogonal to the cross-section (Baliga, NCSU, U.S. Patent 5,396,085, 1995; Li, Cooper and Capano, Purdue University, IEEE EDL, 2002). The second approach (Fig. 9 middle) makes use of two trench regions (Harada, et al, Rohm, IEEE ISPSD, 2012), one to form the gate structure and a second deeper one for shielding the gate oxide. The third approach (Fig. 9 right) makes use of a shallow trench to form the gate structure and two deeper trenches to shield the gate oxide (Peters, et al, Infineon, PCIM 2017). In all three designs, a JFET region is created when shielding the gate oxide, which must be adequately doped to reduce the on-state resistance

without degrading the breakdown voltage. Good on-state resistance, breakdown voltage and gate oxide shielding was observed with the first approach, while the lowest gate oxide electric field was observed for the third approach with a higher on-state resistance (Agarwal, Han and Baliga, NCSU, IEEE WIPDA, 2018).

As mentioned in the beginning of this article, the 'holy grail' for the power semiconductor community during the last 60 years has been to create a power switch with symmetric behavior in the first and third quadrants, gate voltage controlled output characteristics with current saturation, low on-state voltage drop, and fast switching capability. Power electronics engineers have used multiple discrete devices to assemble such a switch for use in matrix converters (Baliga and Han, NCSU, GOMACTech, 2018). A compact, monolithic 4-terminal bi-directional power switch, named the BiDFET, has been recently achieved (Baliga, NCSU, U.S. Patent 10,804,393, 2020; Han, et al., NCSU, IEEE ISPSD, 2020) by integration of two JBSFETs (Fig. 10). These devices will enable a new generation of power electronics that is more compact and efficient.

Excellent power devices can also be created using another wide band gap semiconductor, gallium nitride (GaN). The ability to grow device

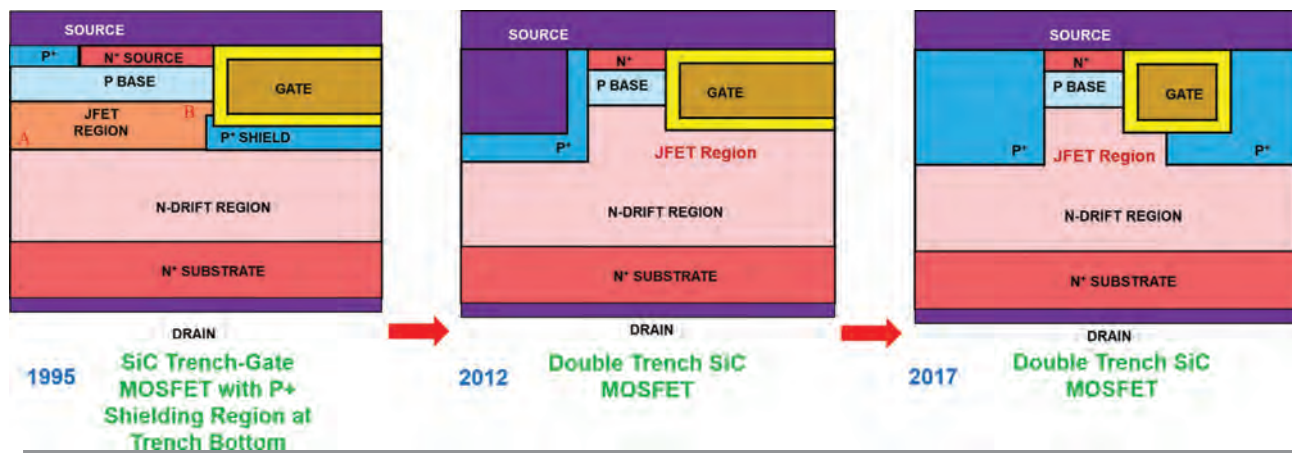


Figure 9. Evolution of Trench-Gate Silicon Carbide Power MOSFETs.

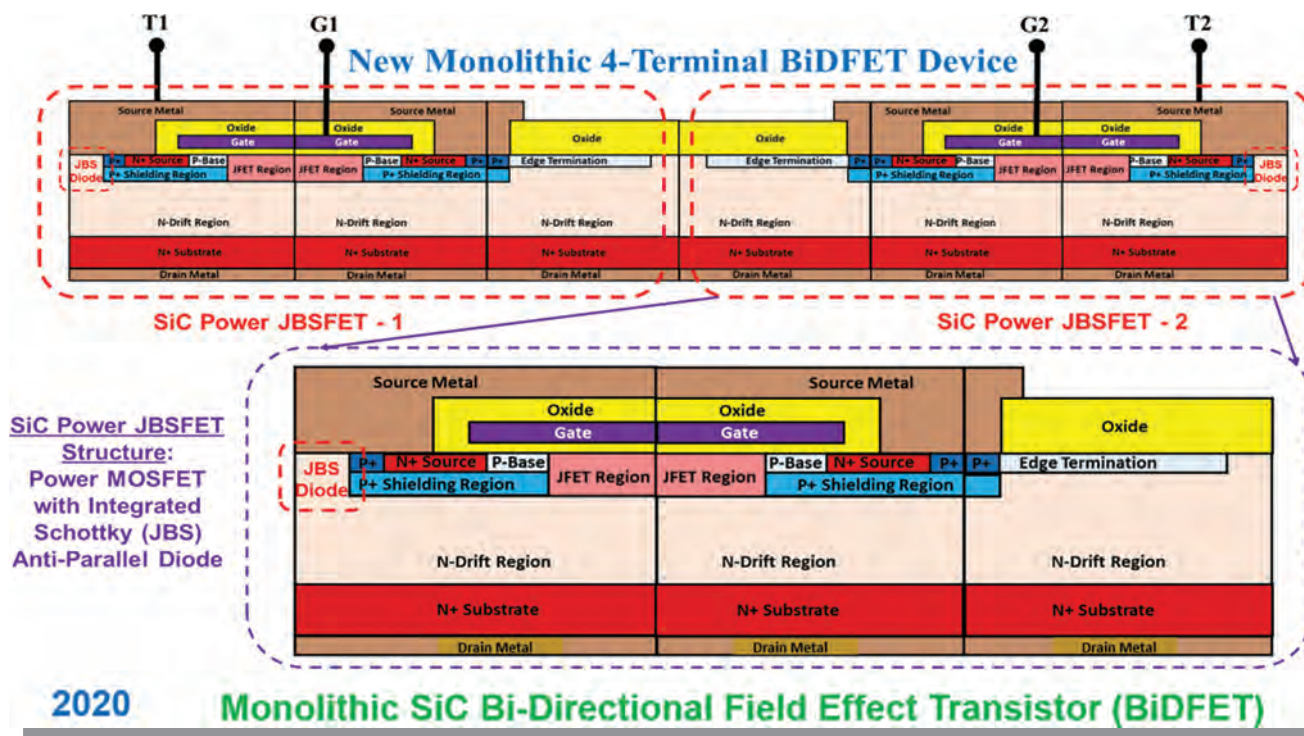


Figure 10. Monolithic SiC Bi-Directional Field Effect Transistor (BiDFET).

quality epitaxial layers of GaN on low cost, large diameter, silicon substrates is a unique attribute of this approach. However, this requires fabrication of lateral high voltage power devices with inter-digitation of the drain, gate, and source electrodes, which can make the chip design challenging due to current crowding and parasitic metal resistances. The formation of a two-dimensional electron gas (commonly referred to as a 2D-gas) at the interface

between GaN and aluminum gallium nitride (AlGaN) creates a layer with low sheet resistance to reduce on-state resistance. The first devices (Fig. 11 left) used a metal-gate (Schottky barrier) contact that produced normally-on behavior in the high-electron-mobility-transistor (HEMT) device. Since this is unacceptable for use in power circuits, this design was combined with a low-voltage silicon MOSFET to form the Baliga-Pair or Cascode

topology (Baliga, NCSU, U.S. Patent 5,396,085, 1995; Transphorm and IRF products). Subsequently, normally-off GaN HEMT devices (Fig. 11 middle and right) were created using the recessed gate design (Saito, et al., IEEE TED, 2006) and P-GaN gate region (Holt, et al., IEEE IPES, 2010). The lateral configuration of these devices allows making multiple power transistors on the same chip to build compact power integrated circuits for applications

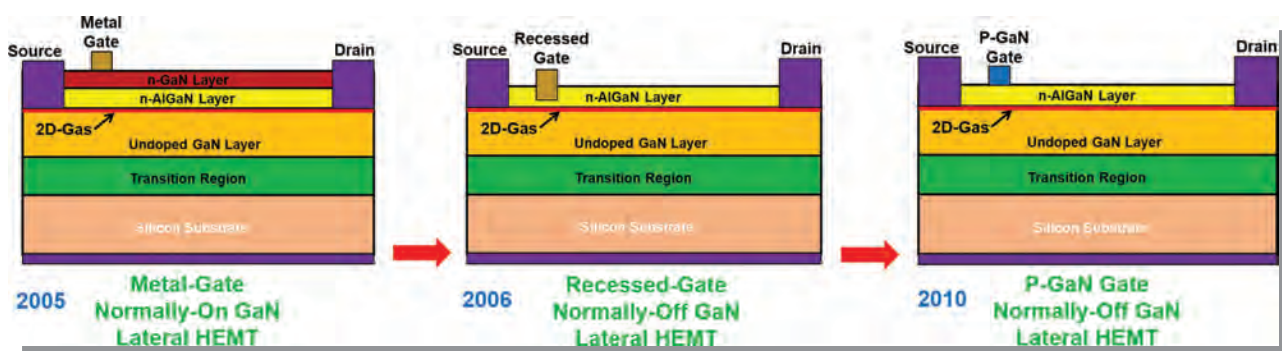


Figure 11. Gallium Nitride Lateral HEMT Power Devices.

such as laptop and cellphone chargers. The devices may be suitable for motor drives for electric vehicles but face a strong competition from the previously discussed SiC power MOSFET in this application space.

Despite 40 years of progress, innovations in power semiconductor devices continue to enhance their performance. They have become essential technology for providing consumers with enhanced comfort, mobility, and quality of life. The transition from fossil fuels to renewable energy for our electricity needs and electric vehicles for our transportation can only be accomplished by utilizing power semiconductor devices.

Acronyms

APEC: Applied power Electronics Conference

EDL: Electron Device Letters

IEDM: International Electron Devices Meeting

IPES: International Conference on Integrated Power Electronic Systems

ISPSD: International Symposium on Power Semiconductor Devices and ICs

JAP: Journal of Applied Physics

PCIM: Power Conversion and Intelligent Motion Conference

TED: Transactions on Electron Devices

TPE: Transactions on Power Electronics

WIPDA: Wide bandgap semiconductor Power Device and Applications Workshop

Biography



ing and a Life Fellow of the IEEE. He spent 15 years at the General Electric Research and Development Center, Schenectady, NY, leading their power device effort and was bestowed the highest scientific rank of Coolidge Fellow. He joined NC State in 1988 as a Full Professor and was promoted to the rank of 'Distinguished University Professor' in 1997. Among his many NCSU honors, he was the recipient of the 1998 O. Max Gardner Award given by the North Carolina University Board of Governors to the one person within the 16 constituent universities who has made 'the greatest contribution to the welfare of the human race'; and the 2011 Alexander Quarles Holladay Medal of Excellence, the highest honor at NCSU from the Board of Trustees. Prof. Baliga has authored/edited 22 books and over 700 scientific articles. He has

Prof. Baliga is an internationally recognized expert on power semiconductor devices. He is a Member of the National Academy of Engineer-

been granted 122 U.S. Patents. The IEEE has recognized him numerous times—most recently with the highest award, the IEEE Medal of Honor. Scientific American magazine included him among the 'Eight Heroes of the Semiconductor Revolution' when commemorating the 50th anniversary of the invention of the transistor. Prof. Baliga invented, developed and commercialized the Insulated Gate Bipolar Transistor (IGBT) at GE. He was inducted into the National Inventors Hall of Fame as the sole inventor of the IGBT. The IGBT is extensively used in the consumer, industrial, lighting, transportation, medical, renewable energy, and other sectors of the economy. It has enabled enormous reduction of gasoline and electrical energy use, resulting in huge cost savings to consumers, and reduction of world-wide carbon dioxide emissions. A detailed description on the applications and social impact of the IGBT is available in one of his books. He received the National Medal of Technology and Innovation, the highest form of recognition given to an engineer by the United States Government, from President Obama in October 2011, at the White House; and the North Carolina Award for Science from Governor Purdue in October 2012, and the Global Energy Prize in 2015.

Transistors at 75—Past, Present, and Future

CHENMING HU

TSMC DISTINGUISHED PROF. EMERITUS, UNIV. OF CALIFORNIA BERKELEY

IEEE LIFE FELLOW, MEDAL OF HONOR RECIPIENT

Early Transistors: Three Bell Labs researchers born on three continents invented the transistor 75 years ago—John Bardeen in America (Madison USA), William Shockley in Europe (Liverpool England), and Walter Brattain in Asia (Xiamen China). Another engineer, John Pierce, suggested the name “transistor” because it connects the new device to the already familiar terms: transconductance, resistor, etc.

Transistor became a household word when SONY introduced a shirt-pocket-size transistor radio using Texas Instruments transistors and a standard 9V battery in 1957 and went on to sell 6 million units of that model. IBM introduced the first mass-produced transistor computer in 1958.

From Ge to Si to Heterogeneous Integration: The early transistors were made with germanium. Around 1960, silicon became the preferred semiconductor because its larger bandgap greatly reduces the transistor leakage current especially when the transistors are hot.

While Si wafers are now entrenched as the substrate material, Ge has returned in the form of $\text{Si}_x\text{Ge}_{1-x}$ alloy thin films added on the Si substrates during IC production. SiGe is playing increasingly critical roles in advanced MOSFETs for enhancing electron and hole mobilities and other benefits. Optical, magnetic, and ferroelectric materials have also been integrated into Si technology. Wide band-gap semiconductors GaN on Si or SiC substrates are used for making high-voltage transistors.

How the Transistor Density Grew and Grew: Jack Kilby of TI received the 2000 Nobel Prize in Physics “for his part in the invention of the integrated circuits.” Robert Noyce of Fairchild Semiconductor is considered the other major contributor and his



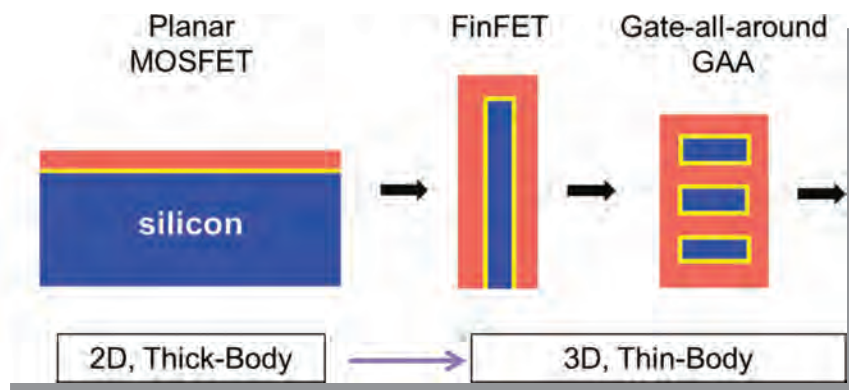
President Barack Obama shakes hands with Dr. Chenming Hu

patent content bears a great resemblance to modern IC technology, but he had died before 2000.

Today, we take for granted that over 100 million silicon wafers are used each year to produce about 10^{20} transistors with the smallest features the size of tens of atoms. But the growth of circuit density could have halted for any one of several reasons long ago but for the ingenuity and hard work of many people and several industries. The semiconductor equipment industry kept improving **lithography** and other production tools. The process engineers in the leading IC fabs delivered **high-yield nano-fabrication** technologies for making tiny intricate structures. The

high **costs of technology development and fabs** were once considered potential showstoppers - until industry consolidation and the foundry model created huge IC manufacturing companies. The EDA industry's design automation tools reduced the barrier to **designing large complex ICs**, and accurate standard transistor models bridged the physical fabs and the digital EDA tools. Ensuring the **long-term reliability** of billions of transistors turned out possible through better materials, manufacturing, understanding of failure mechanisms, and failure rate modeling. But past success does not guarantee future success. The hill gets steeper.

Power Consumption, MOSFET, CMOS, Thin-Body CMOS, 3D Transistor: If we want to cramp a hundred times more transistors into a chip of a certain size, we need to reduce the power consumption per transistor by about a hundred times. Otherwise, heat removal would be a nightmare, not to mention the impact of such energy use on mother earth. A major change that reduced power consumption was the transition from bipolar transistors to MOSFET and then CMOS. **CMOS technology reduced the standby current of circuits to nothing but the transistor leakage current.**



Evolution of transistor structure

The basic MOSFET structure remained unchanged from 1960 for 50 years until reducing MOSFET size further without degrading leakage, speed or switching energy became impossible. In 2011 Intel adopted the first **3D transistor**, **FinFET** for production. FinFET and the **thin-body MOSFET** concept arise from the insight that the leakage current basically cannot flow within several nanometers (nm) of the Si surface because the surface potential is well controlled by the gate voltage. In the figure showing the MOSFET evolution, FinFET has a vertical Si fin (in blue), about 10nm thin, as the transistor body. The body is covered by gate oxide (in yellow) and gate metal (in orange) and leaves no Si outside the range of strong gate control. It reduces the leakage current by orders of magnitude. Furthermore, the FinFET size can be reduced every few years as long as the fin thickness is also reduced. Another thin-body MOSFET demonstrated in the same DARPA research project as FinFET is the ultra-thin-body SOI (UTB-SOI or **FDSOI**). Being a 3D transistor, FinFET has a smaller footprint than the planar MOSFET. It has the same advantage as building tall buildings

instead of single-story buildings in a crowded city.

The fin of FinFET has become thinner and taller with each new technology node. At the 2nm node, it is too hard to make the required thin and tall fin by lithography and etching. The industry is adopting a new 3D thin-body MOSFET structure called NanoSheet or GAA (gate-all-around), where the thin body is made by epitaxial growth and etch-release. The figure above illustrates the evolution from FinFET to GAAFET.

Examples of What May Happen Next

3D transistors and 3D packaging are here to stay. 3D NAND technology is an excellent example of a cost-effective monolithic 3D memory IC. Monolithic 3D logic IC may start with stacking PFET on top of NFET to reduce CMOS-gates' footprints. Future monolithic 3D IC paths may employ transferred single-crystal semiconductor films, self-assembled 2D semiconductors, or amorphous or polycrystalline semiconductor films as the transistor material. 0.6nm MoS2 monolayer has been used to demonstrate 1 nm gate-length thin-body MOSFET. Power supply voltage

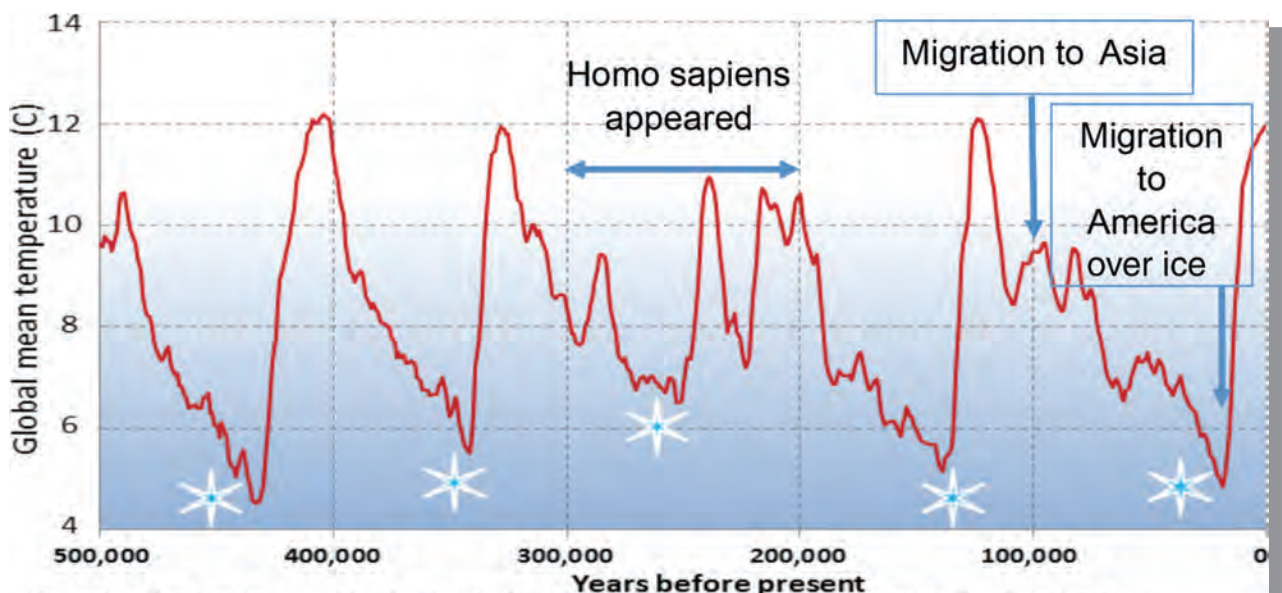
and power consumption may be reduced by many folds with Negative-Capacitance Transistor (NCFET). It requires inserting a thin layer of ferroelectric such as HfZrO in the MOSFET gate stack. Another advantage of adding the thin ferroelectric is its memory property that may be exploited for computing in memory or fast non-volatile memory.

Does the World Need More and Better Transistors?

The enormity of the task of dealing with global warming (see the graph below) is beginning to be realized. What about the task of dealing with the next Ice Age, which is predicted to start in 1500 years based on Earth's orbit? Humans may need order-of-magnitude greater capabilities to deal with future existential challenges.

But how can we possibly get 10x or more problem-solving power? Electronics are the key. While all technological advances bring forth new capabilities, electronics are unique for three reasons.

- 1) Its impact is infectious. High-speed communication and computing, automation, internet, AI, robotics, and



Source of global mean temperature: Panchuk, K. (2019) *Glaciation over Earth's History*.

Variation of global mean temperature

yet-unknown future technologies enabled by better transistors have lifted and will lift up all technologies, industries, and sciences. And they in turn lift each other.

- 2) ICs use relatively small amounts of materials. And the less materials they use (by being made smaller), the faster and more capable they become.
- 3) Theoretically, the energy required for information manipulation can still be reduced by more than a thousand times. Although we have no idea how to get there now, reducing the energy by 10 or 100 times would not violate physical laws. The energy efficiencies of other technologies (transportation, lighting, ...) are mostly already around 50% of their theoretical limits.

Lesson From the Past and Task for the Future

The history of transistors is a journey log of climbing one hill after another. Until we get high enough on one hill, we can not even see the terrain and map a route to reach the next hill. Importantly, with each hill climbed, we accumulate and discover new skills that help us move forward. Deposit and etch materials one atomic layer at a time? Sure. Economically on millions of wafers every week at high yield with billions of transistors on each chip? Sure. Magnetic, ferroelectric, and optical materials too? Sure. Switch the magnetic polarization with an electric field, not current? Sure. Do anything that does not violate physical

laws? Probably. Continuing the hard climbs while diligently scouting for new provisions and possible routes is the best way to create future electronics, which may be very different in devices, materials, and operating mechanisms. The new provisions and route will come from university and industry researchers with deep knowledge in physics, chemistry, biology, and algorithms—and the help of expanding problem-solving capabilities, time, and luck.

Biography



Dr. Hu received his B.S. degree from National Taiwan University, which honored him with its Distinguished Alumni Award, and M.S. and Ph.D. degrees from UC Berkeley. Dr. Chenming Hu is called the Father of 3D Transistors for developing the FinFET in 1999. Intel hailed FinFET as the most radical shift in semiconductor technology in over 50 years. Modern computers, smart phones, and the internet all ran on 3D transistor processors. He received the US National Technology and Innovation Medal from President Obama in 2016. He leads the ongoing development of BSIM, a suite of industry-standard computer models of transistors. University of California provides it royalty free for the global IC industry to design integrated circuits worth well over a trillion US dollars since 1995. IEEE, world's largest technical professional organization, gave him its highest award,

Medal of Honor, in 2020 for helping to "keep Moore's Law going over many decades" after lauding him as "Microelectronics Visionary" for "achievements critical to producing smaller yet more reliable and higher-performance integrated circuits" in 2009. The 2013 Kaufman Award cited his "tremendous career of creativity and innovation that fueled the past four decades of the semiconductor industry". Dr. Hu is TSMC Distinguished Chair Professor Emeritus of the University of California, Berkeley. From 2001 to 2004 he was the Chief Technology Officer of TSMC, now the world's largest semiconductor company. He was the board chairman of the nonprofit Friends of Children with Special Needs and the East Bay Chinese School. He has authored six books and 1000 research papers and received over 100 US patents and honorary doctoral degrees from the University of Hong Kong and NYCU in Taiwan. He is honored with memberships in the US National Academy of Engineering, Chinese Academy of Sciences, US Academy of Inventors, The World Academy of Sciences and Academia Sinica. His other professional honors include Asian American Engineer of the Year; Silicon Valley Engineering Hall of Fame; IEEE Jack Morton Award, Solid State Circuits Award, Nishizawa Medal, and the EDS Education Award for "distinguished contributions to education and inspiration of students, practicing engineers and future educators." He also received UC Berkeley's highest honor for teaching—the Berkeley Distinguished Teaching Award.

TECHNICAL BRIEFS

OUTSIDE SYSTEM CONNECTIVITY ROADMAP

C. MICHAEL GARNER

GARNER NANOTECHNOLOGY SOLUTIONS, CHAIR OUTSIDE SYSTEMS CONNECTIVITY

1. Introduction

The purpose of the Outside System Connectivity (OSC) roadmap is to identify communication requirements for systems in different applications, identify gaps in capabilities, identify critical component and device development needs and monitor developments of capabilities to fill these future gaps.

The Internet of Everything (IoE) is continuing to expand in applications that demand higher volumes of higher performance communication. The IoE was initially defined as a wide range of Internet of Things (IoT) devices communicating with cloud computing that store data and which was analyzed with applications and actions communicated. As IoE was used for a broader range of applications, some applications had unacceptably slow performance due to the latency of communicating with the cloud. To overcome this latency limitation, some applications added local storage and processing close to the IoT devices and network, which is referred to as fog computing.

Most applications will employ RF/microwave wireless communication to connect to the internet which will then connect through high-performance backhaul or fiber optical interconnects to a cloud data center. In the future, millimeter waves (mmWaves), massive multiple-input multiple-output (MIMO) or other 5G media will be implemented for high-speed connection to terminal devices, while low-power wide-area network (LoWAN) communications, such as LoRaWAN, SIGFOX, LTE Cat 0 and NB-IoT, will be utilized to connect and provide enormous data to the cloud and/or fog

computing system from IoT-edge sensor devices. Within the data center, communication to servers is through fiber optical interconnects with signals being routed through multiple routers. Upon arrival at a router, the optical signals are converted to electrical, routed and then converted back to optical signals, which adds to energy consumption and latency. The requested data is then routed out of the data center and returned to the requesting IoT devices through a path similar to the request path.

Applications that require fast communication and decision making, such as autonomous vehicles and traffic control, are adopting edge computing. In this model fast communications are made between the edge and vehicles and traffic flow controls and filtered data is communicated between edge computing and the supporting cloud computing capabilities. Fast communication with low latency is required between the IoT devices and the fog, while fast communication will be required also between elements of the Edge. Computing in the Edge can be performed in a micro data center, which is connected to the network and the internet.

With the rapid growth of high data rate internet applications and IoT, communication rates in data centers need to grow to support high-speed access and provide high-speed low latency communication between servers and memory or other servers. With increased use of high-resolution video, virtual reality, and augmented reality applications, ever higher data rate communication with lower latency is required in data cen-

ters. Communication between racks and switches is carried by optical interconnects; however, the capacity of switches is increasing faster than the capacity of fiber interconnects. Also, the power consumed by the switches in data centers is approximately 30% of the power consumed in the data center. To reduce switching power and overcome the fiber capacity gap, companies are working to integrate silicon photonics into the switch. There are also efforts to extend fiber into the server, into packages and thus reduce power. There are significant technical challenges with developing and implementing single mode fiber with low loss for these applications. These challenges will be highlighted in this article.

Applications that will first drive the development of high-volume component and device development are communication in data centers and mobile handheld devices. Over time new applications, such as quantum computing, may arise that require the development of new component and device capabilities and these are monitored in the roadmap.

2. Application/System Requirements & Challenges

While a broad range of applications are assessed in the OSC roadmap, data centers and mobile smartphones are driving development of higher performance circuits and devices and are described in this article.

Data Center Communication

For data centers, the drivers for communication are the data rate per server unit, which is currently 400 Gbps, as shown in Table 1, and

Table 1: Wavelength Division Multiplexing Module Performance Requirements

	2019	2021	2023	2025	2027	2029	2031	2033	2035	2037
System structure										
Data Rate/ Lane[1] (Gbit/s)	100	100	100/200	200	200/400	200/400	400	400	400	400/800
Data Rate/fiber (Gbit/s)	400	400	800	800	1600	1600	3200	3200	3200	3200
Distance (km)	< 10	< 80	< 80	< 80	< 80	< 80	< 80	< 80	< 80	< 80
# Wavelengths [2]	4	4	4	4	8	8	8	8	8	8
Number of Bits per symbol (HOM) [3]	2	2	2	2	2	2	4	4	4	4
Additional link penalty due to HOM (dB)	3	3	3	3	3	3	9	9	9	9

[1] a lane is for a single data stream with only amplitude modulation in a fiber (per wavelength)

[2] assuming HOM on fully integrated Si Photonics : QPSK/DPQPSK demonstrated with Si-photonics, 16-PSK, 32-PSK not demonstrated

[3] assuming integrated laser on Si after 2019, 40 mW on WDM laser at high temperature not demonstrated yet

HOM: Higher Order Modulation (i.e. PAM4, QPSK, etc.)

PAM: Phase Amplitude Modulation

QPSK: Quadrature Phase-Shift Keying

WDM: Wavelength-Division Multiplexing

<i>Manufacturable solutions exist, and are being optimized</i>	
<i>Manufacturable solutions are known</i>	
<i>Manufacturable solutions are NOT known</i>	

power consumption. Data centers typically upgrade servers approximately every three years and would like to have the data rates increase when they upgrade the servers; however, this would require upgrading the optical interconnect cables with every server upgrade. Power consumed in communication and switching is becoming significant, 30% of data center power in 2013, and signal integrity is being compromised at higher data rate due to RF loss in the metal trace between the switch chip to the faceplate, so Data Centers are requesting that optical I/O be integrated into the switch package by the 51.2 Tbps switch. The Consortium for On-Board Optics (COBO) or Co-packaged Optics (CPO) is driving to have the photonic transmitter and receiver on the board and connecting this to single-mode fiber in the data center. This would enable upgrading the data center communication data rate when the servers are upgraded. At the same time, the routers in data centers are adding

communication capacity and ports that consume considerable power, so the industry is seeking ways to reduce router thermal density and improve energy efficiency.

Mobile Handheld

As smart phones incorporate more functionality, they will need to communicate at higher data rates, as shown in table 2, with the internet, but also detect signals from GPS satellites, cell towers, health monitors, watches, and other RF sources. Thus, they will need to have compact antennas that can receive and transmit to multiple ranges of frequencies with multiple protocols. The RF and AMS (Analog/Mixed-Signal) components will need to support all of the communication with high energy efficiency for multiple applications simultaneously.

A significant challenge for mobile smartphones is to support the data rates required for new multimedia applications such as virtual reality. While future smartphones need to

communicate at higher data rates, they will need to operate with low power consumption. Furthermore, future smartphones will need to have improved security of personal information when communicating with the internet or other devices. An additional challenge is to integrate additional antennas into thin smartphones without causing interference in other communications or integrated circuits.

3. Critical Components

Data Centers

To achieve higher data rates, more wavelengths than 4 in current CWDM4 format and higher order modulation, will be needed in addition to higher data rates per lane. To support pulse amplitude modulation, DAC/ADCs are needed.

Mobile Phones

In the longer term, high frequency mmWave may be used in high population density areas to support high

Table 2: Mobile Device Wireless Cellular Performance Requirements

Year	2021	2022	2023	2024	2025	2026	2027	2028	2029
Cellular Data Rate Gbps (Max.) ⁶	5	5	7	7	7	10	10	10	20
Max. Cell Range ⁷ (km) [unobstructed]	35/0.2-1	35/0.2-1	35/0.2-1	35/0.2-1	35/0.2-1	35/0.2-1	35/0.2-1	35/0.2-1	35/0.2-1
3G Frequency	<4 GHz	<4 GHz	<4 GHz	<4 GHz	<4 GHz	<4 GHz	<4 GHz	<4 GHz	<4 GHz
4G Frequency	<4 GHz	<4 GHz	<4 GHz	<4 GHz	<4 GHz	<4 GHz	<4 GHz	<4 GHz	<4 GHz
5G Maximum Data Rate (Gbps)	5	5	7	7	7	10	10	10	20
6G Maximum Data Rate (Gbps)									
Wireless Power Budget (mW)	200–300	200–300	200–300	200–300	200–300	200–300	200–300	200–300	200–300
Year	2030	2031	2032	2033	2034	2035	2036	2037	
Cellular Data Rate Gbps (Max.) ⁶	20	20	50	50	50	70	70	70	
Max. Cell Range ⁷ (km) [unobstructed]	35/0.2-1	35/0.2-1	35/0.2-1	35/0.2-1	35/0.2-1				
3G Frequency	<4 GHz	<4 GHz	<4 GHz	<4 GHz	<4 GHz				
4G Frequency	<4 GHz	<4 GHz	<4 GHz	<4 GHz	<4 GHz				
5G Maximum Data Rate (Gbps)	20	20	20	20	20	20	20	20	
6G Maximum Data Rate (Gbps)			50	50	50	70	70	70	
Wireless Power Budget (mW)	200–300	200–300	200–300	200–300	200–300	200–300	200–300	200–300	

⁶ Assumes that Massive MIMO will be implemented in 2019 and full 5G performance in 2025.

⁷ Assumes 4G LTE through 2017, Massive MIMO <6 GHz through 2023 and both Massive MIMO <6 GHz and mm Wave beyond 2025.

<i>Manufacturable solutions exist, and are being optimized</i>	
<i>Manufacturable solutions are known</i>	
<i>Manufacturable solutions are NOT known</i>	

data rate applications with a large number of users. A significant challenge is that 28 GHz to 78 GHz signals do not penetrate buildings, so buildings would need to have repeaters in the building or employ massive MIMO or ultra-high data rate Wi-Fi.

If 5G is implemented with mmWave and MIMO, cell phones would need to have multiple antennas to receive and transmit information and each antenna would need to have power amplifier (PA) and an ADC and DAC [1], which would consume considerable power operating with high precision at high frequencies. A critical challenge is to increase the energy efficiency of the PA at mmWave frequencies while maintaining linearity, since the efficiency of the PA decreases with operating frequency. Thus, higher performance

of incumbent process technologies or even new materials may be required to improve energy efficiency. In the transmit mode, the antenna array would operate as an active phased array to focus transmission toward the base station. To overcome the high operating power of the high precision DAC/ADCs, use of hybrid analog/digital preprocessing [2, 3] or lower precision DAC/ADCs (1bit) [1, 2, 4] has been proposed. To compensate for potential blockages [5], multiple antennas would need to be integrated into the cell phone to be connected with multiple base stations.[6]

For >10 Gb/s communication rates, proposals have been made for a single bit zero crossing modulation protocol; however, energy efficiency of all required components need to be investigated.

4. Integrated Circuits

To increase data rates of communication with lower power and lower power, DACs and ADCs need to operate with higher sampling rates and lower power consumption. Also, serializer-deserializer (SERDES) circuits need to operate at higher frequencies with higher efficiency. To achieve higher data rates with improved energy efficiency in these circuits, devices need to operate with lower power at higher frequencies. This may require introduction of new device, gate, contact, or interconnect materials while decreasing circuit cost.

Recently, a 5 nm integrated circuit technology was announced that demonstrated a transmitter test circuit that operated at 130 Gb/s data rates with PAM4 modulation and 0.97 pJ/bit energy consumption [7].

5. Device Requirements, Challenges & Potential Solutions

CMOS Devices

The 2022 roadmap technology plots reflect the RF and analog performance metrics needed to support the technology roadmap developed by the IRDS More Moore IFT in 2017. The RF-AMS performance metrics for CMOS devices have been restricted to peak f_T (Figure 1) and peak g_m (Figure 2) and have been calibrated on recent averaged measured data in the 28 nm, 22 nm, and 16 nm nodes. The 2020 roadmap gives the above performance FoMs for n-channel FDSOI and double-gate FinFET high-performance devices obtained from technology computer aided design (TCAD)-based device modeling methods(a) [8]. These include hydrodynamic transport with thin silicon mobility physics, as well as the estimated resistive and capacitive device parasitics up to the first metal layer, which defines the terminals of a transistor cell in high-frequency analog circuit design. They indicate the degradation in f_T and g_m at gate lengths below 10 nm as a result of mobility degradation caused by surface scattering at the gate oxide in-

terface, and due to the ever-thinner silicon body. As can be observed, the double gate of the FinFET results in higher transconductance but also higher capacitive parasitics compared to the single-gate FDSOI MOSFETs. Note that the displayed f_T (Figure 1) does not include the capacitive parasitics resulting from connecting the transistor cell to the passive devices in the upper metal layers of the back-end. The introduction of new materials, and transistor and gate structures may change the f_T trend of sub 10 nm CMOS devices. Reduction of gate and contact resistance has been demonstrated to improve f_{max} [9, 10], but not impact f_T .

Many of the materials-oriented and structural changes being invoked in the digital roadmap degrade or alter RF and analog device behavior. Complex tradeoffs in optimization for RF, HF, and AMS performance occur as different mechanisms emerge as limiting factors. Examples include series resistances at gate, source and drain, as well as parasitics from interconnecting the transistors to other devices in a circuit that greatly affect the device impedances and the “loaded” figures of merit as measured at the upper metal levels. Fundamental

changes of device structures, e.g., multiple-gates and silicon-on-insulator (SOI), to sustain continued digital performance and density improvements greatly alter RF and AMS characteristics. Such differences, along with the steady reduction in supply voltages, pose significant circuit design challenges and may drive the need to make dramatic changes to existing design structures.

Group IV Bipolar

The roadmap for SiGe heterojunction bipolar transistors (HBTs) and associated benchmark circuits at mm-wave frequencies has been based since 2013 on a seamless set of TCAD device simulation tools in order to obtain consistent compact model parameters for the complete transistor structure used in the respective circuit simulations. All known transport, structural parasitics up to metal 1 (i.e. transistor cell terminals) and temperature effects have been included in the results [11] and calibrated based on experimental data. Furthermore, the TCAD tools and those parameters that cannot be obtained by TCAD have been calibrated on existing prototyping process technologies. Performance

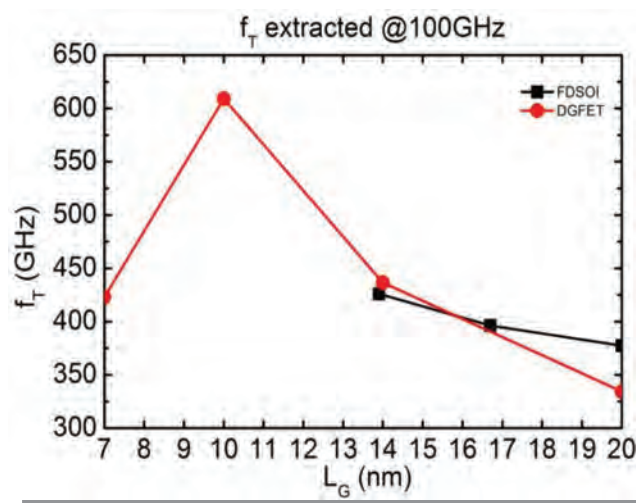


Figure 1. CMOS Roadmap for Peak f_T vs. Physical Gate Length for FDSOI and Double-gate (FinFET) MOSFETs Based on Technology CAD.¹

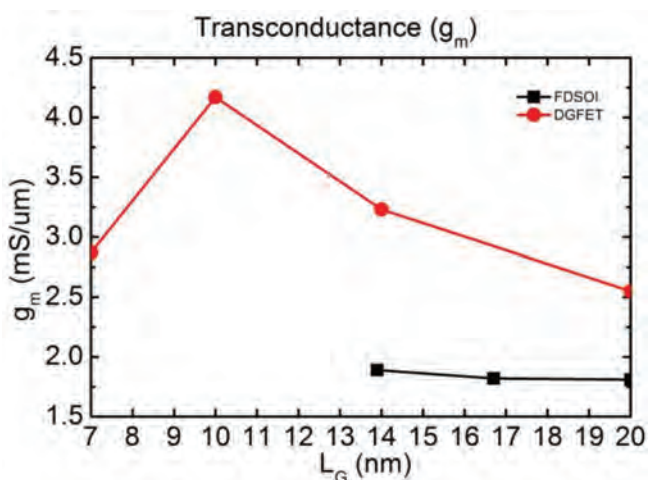


Figure 2. CMOS Roadmap for Transconductance per Unit Gate Width, g_m , vs. Physical Gate Length for FDSOI and Double-gate (FinFET) MOSFETs Based on Technology CAD.

¹TCAD simulations performed by Sorin Voinigescu at the University of Toronto.

plateaus have been assumed to last four years and are linked to applications and the foregoing system drivers. It has been assumed that at least two foundries offering the technology of the respective node for product prototyping are presented. The benchmark circuits for LNA, PA, VCO, and current-mode-logic-based (CML) ring-oscillator (RO) have been manually optimized for each technology node and a variety of commercially relevant frequencies. The most recent result for a prototyping process [12] corresponds closely to the performance predicted for node N3 (Figures 3, 4).

Even though it is a challenge for the HS-NPN to increase the unity current gain cut-off frequency f_T by more aggressive vertical profiles, it is less of a challenge to achieve $f_{MAX} > f_T$. What is unclear today is, how large the ratio f_{MAX}/f_T needs to be for future circuit applications. That is, the challenge is to determine what this ratio should be by using the “plateau technologies” for the next roadmap and appropriate benchmark circuits. Since lateral scaling requirements for HBTs are significantly relaxed compared with those for MOSFETs, vertical profile fabrication under the

constraints of overall process integration appears to be the bigger challenge. The reduction of imperfections and the increase of current carrying capability of the emitter and collector contact metallization are further challenges that need to be met by process engineers on the way to achieving the physical limits of this and any other technology [12].

III-V FET and Bipolar

The FoMs depend on technology and include: f_T , f_{MAX} , g_m , and V_{BD} ; power, gain, and efficiency at 10, 24, 60, 94, 140, and 220 GHz; NF_{MIN} and G_A at 10, 24, 60, and 94 GHz; LNA NF and G_A at 140 and 220 GHz. f_T and associated gain are as shown in Figures 5–6. As mentioned previously, RF and AMS front-end components are a growing part of the semiconductor industry. However, this has divided the III-V technology landscape into two groups, one dominated by the large volume consumer market and the other dominated by low volume specialty markets. Within the III-V technology landscape, the large volume consumer driven market is best represented by GaAs HBT power amplifiers for cellular communications.

The unique challenges for III-V devices are yield (manufacturability), substrate size, thermal management, integration density, dielectric loading, and reliability under high fields. Challenges common with Si-based circuits include improving efficiency and linearity/dynamic range, particularly for power amplifiers. A major challenge is increasing the functionality of power amplifiers in terms of operating frequency and modulation schemes while simultaneously meeting increasingly stringent linearity and efficiency requirements at the same or lower cost.

Photonic Integrated Circuits and Devices

Near-term challenges are to 1) increase the data rate per wavelength and total throughput per fiber, density of optical transceivers while reducing their power and cost, and 2) develop a router/switch package integrated photonic interconnects for data centers. Long-term challenges include 1) processing information in the optical domain, and 2) developing methods for communication between systems with different wavelengths, polarizations, and modulations.

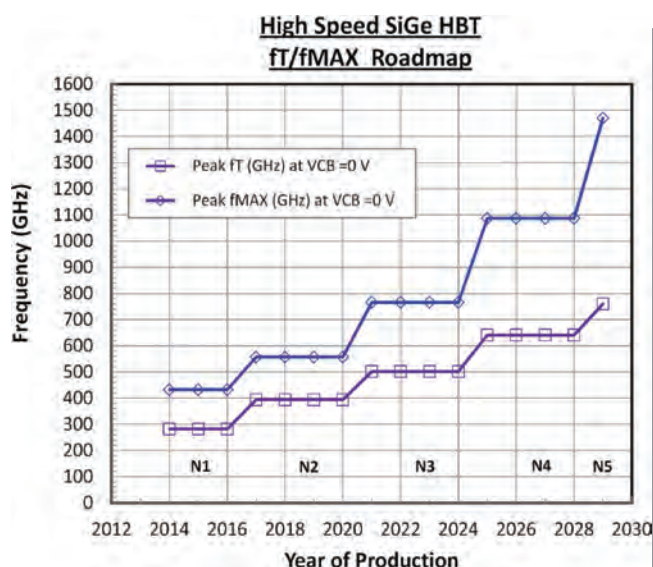


Figure 3. High Speed SiGe HBT f_T and f_{MAX} Roadmap vs. Year of Production.

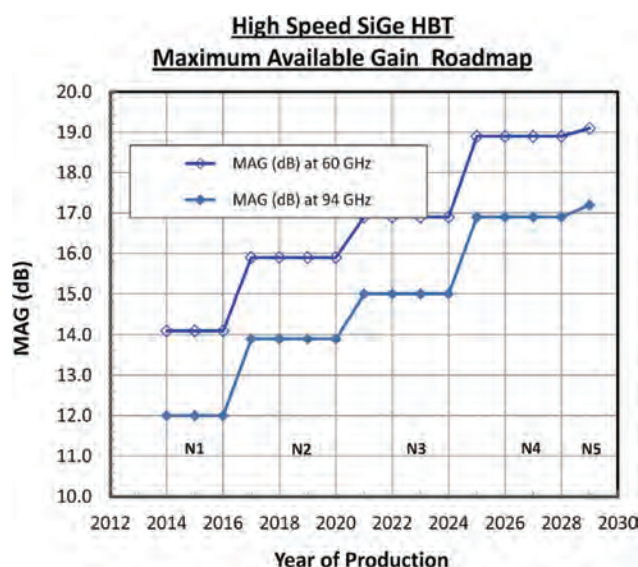


Figure 4. High Speed SiGe HBT Maximum Gain Roadmap vs. Year of Production.

Photonic Integrated Circuits(PIC)

Recently, photonic integrated circuits on silicon, using either hybrid or heterogeneous integration methods, have been introduced into the market by multiple transceiver manufacturers. Currently, some of these products have separate transmitter and receiver chips.

Some of these transmitter circuits have the lasers integrated with the modulators, while some of these have the laser packaged separately from the modulators. In most cases, the modulators and waveguides are fabricated on single-crystal silicon on insulator wafers. Most suppliers are employing Mach Zehnder modulators, while more compact ring modulators are being evaluated in research and moving to product phase in a few years. Since ring modulator operating wavelength is sensitive to temperature, they have been integrated with tuning elements to control the optimal wavelength, which increases power consumption and cross-talk, which must be managed. Many of these transmitter circuits employ multiple wavelengths that either are transmitted over individual fibers or multiplexed into a

single fiber. Mach Zehnder modulators and the (de)multiplexers currently use silicon waveguides and the weak electro-optic effect from free carriers means the foot-print of the PIC is relatively large. Future energy-savings from these circuits, will depend upon improvements to laser wall-plug efficiency and reduction in size and power consumption of electro-optic modulators, thereby having a cascading effect of reduced power consumption and cost for the photonic chip, and supporting integrated circuits.

Low Power High Output Lasers

To reduce the power consumed in communication, there is a need to increase the efficiency of lasers in converting electrical energy to photons. VCSELs and edge-emitting lasers are used for different applications and may be competing in some applications as silicon photonics strives to reduce cost while increasing data rates.

Although VCSELs are more energy efficient than edge emitting lasers, the power to modulate at higher data rates will increase, which can cause reliability issues. So more efficient top emitting lasers are needed in the future. To support high volume manufacturing,

III-V quantum dot VCSELs epitaxially grown and fabricated on (001) silicon [13] with p-doping [14] have been demonstrated with high stability over a wide temperature range.

An emerging technique to increase photonic light source energy dissipation is to introduce nanostructures that increase energy density. This has been used to demonstrate electrically pumped lasers with lasing thresholds of 287 nA at 150 K [15] that is 1000x less than earlier electrically pumped nanocavity lasers.

Some short-distance communication links may also be powered by high-efficiency LEDs (no threshold). However, higher throughput relies on efficient packaging of several thousand spatially multiplexed optical channels.

High-Density Low Power Modulators

For optical interconnects to meet future requirements, all supporting devices must operate with higher performance, lower energy consumption, higher optical efficiency, and have a lower cost. Essential for long-distance communication, Electro-Optic Modulators (EOM) can modulate the amplitude, phase, frequency, or polarization

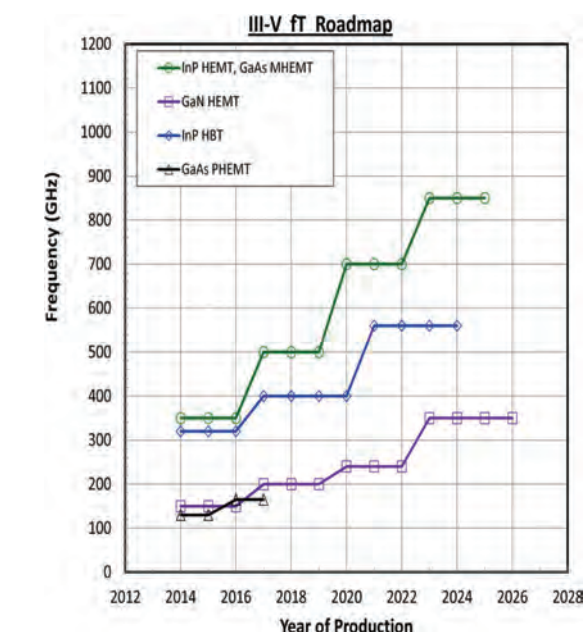


Figure 5. III-V Roadmap for fT

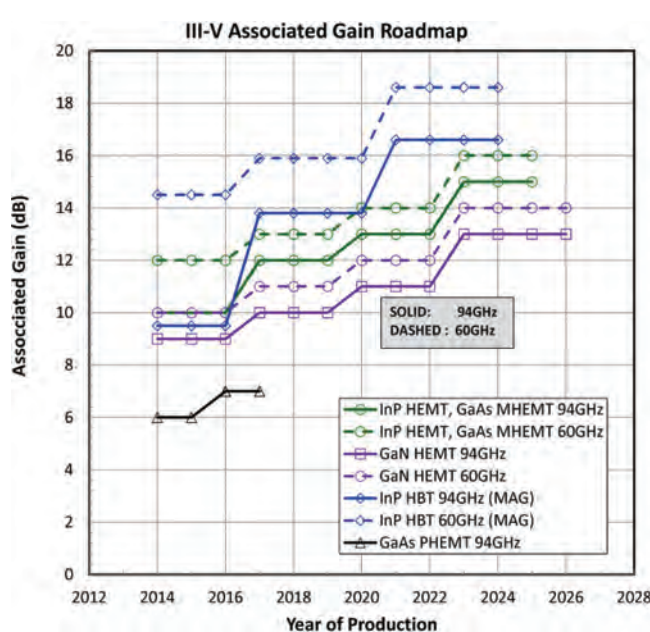


Figure 6. III-V Roadmap for Associated Gain

of the light; however, these devices must become more compact, and operate with lower power consumption. Compact modulator options in the future will likely use the following physical effects: electro-absorption modulation, bulk semiconductor Franz-Keldysh effect (III-V, Ge), plasmonics, Stark Effect, or Wannier-Stark localization.

High Speed, High-Density Photodetectors

A significant challenge for optical detectors is to increase operating frequency to support higher data rates. A limiting factor is the RC time constant of the photodetector. The most logical solution is to reduce the detector size which reduces junction capacitance, but this may not be able to absorb most of the light, i.e., poor responsivity. Ongoing efforts are focused on reducing the junction and contact resistance for the smaller photodetectors, and achieve a good speed-responsivity tradeoff. The most recent research breakthrough has yielded a bandwidth in excess of 250 GHz [16]. If the detector intercepts less light from the waveguide, the amplifier will need to have higher gain that will potentially reduce the signal-to-noise ratio. The best solution to this is to develop techniques to effectively couple light from the waveguide into the detector. Possible solutions include using plasmonic structures above the photodetectors to focus light into the detector. Another option is to include passive periodic or aperiodic nanophotonic structures to focus light onto the photodetector. The temperature dependence of the potential solutions needs to be understood, to design the optimal solution.

Optically Based Switching and Routing

Currently, optical signals are redirected by electrical routers where the light must be converted to electrical signals that are routed to different fi-

ber channels. This significant latency can be added to the transmission of optical signals that go through multiple routers. New technologies are needed to enable optically based switching and routing that do not require the optical-electrical-optical conversion. Hybrid electrical/optical (E/O) routing capabilities have been demonstrated using both MEMS [17–20] and E/O switches including Mach-Zehnder interferometers [21] and ring resonators [22].

If all-optical networks are to be viable, optically based logic will be needed to identify signal stream routing conflicts and determine the correct routing alternative. A number of optical logic devices and functions have been proposed that require local nonlinearity of optical properties [23]. It is proposed that branched waveguides with local nonlinear optical materials could function as AND or OR functions [24].

6. Summary

Future system communication requirements are driving development of new communication architectures, circuits, and devices. The OSC welcomes input on circuit and device requirements and potential solutions.

7. Acknowledgments

The author acknowledges the valuable contributions of the IEEE IRDS members and former ITRS members to the IEEE IRDS Outside System Connectivity Roadmap. Furthermore, valuable improvements were made to this paper by Carlos Augusto, Di Liang, and Sudharsanan Srinivasan.

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UPCOMING TECHNICAL MEETINGS

IEEE International Electron Devices Meeting Announces 2022 Call for Papers

IEDM 2022 will feature special Focus Sessions on the following topics:

- Advanced Heterogeneous Integration: Chiplets and System-in-Packaging
- DNA Digital Data Storage, Transistor-Based DNA Sequencing, and Bio-Computing
- Emerging Implantable-Device Technology
- Quantum Information and Sensing
- Special Topics in Non-Von Neumann Computing

The **Plenary speakers** for this year are Dr. Ann Kelleher (Intel), Dr. Yusuke Oike (Sony) and Dr. Maud Vinet (CEA-Leti)

Short Courses will present exciting opportunities to learn about

- High-Performance Technologies for Datacenter and Graphics to Enable Zetta Scale Computing, Organizer: Ruth Brain, Intel
- Next-Generation High-Speed Memory, Organizer: Yih Wang, TSMC

IEDM 2022 will offer six Tutorials on

- Device Innovations to Extend CMOS Scaling for 2nm Node and Beyond—Tenko Yamashita (IBM)
- Sensors for IoT, Automobile, Health and Other—Carlotta Guiducci (EPFL)
- Resistive Memories-based Concepts for Neuromorphic Computing—Elisa Vianello (CEA-Leti)
- The Era of Advanced Packaging and Hybrid Bonding—Sitaram Arkalgud (Tokyo Electron Ltd.)



- FEOL Reliability: from Essentials to Advanced and Emerging Devices and Circuits—Ben Kaczer (imec)
- Fabrication and Three-Dimensional Integration Technologies—Qiangfei Xia (Univ. of Massachusetts)

Under the theme, “The 75th anniversary of the Transistor, and the Next Transformative Devices to Address Global Challenges,” the 68th annual IEEE International Electron Devices Meeting (IEDM) has issued a Call for Papers seeking the world’s best original work in all areas of microelectronics research and development.

The 2022 IEDM is being planned as an in-person conference 3–7 December 2022 at the Hilton San Francisco Union Square hotel, with on-demand access to recorded presentations after the event for those unable to travel due to COVID-19 restrictions.

The paper submission deadline is Friday, 14 July 2022. Authors are asked to submit four-page camera-ready papers. Accepted papers will be published as-is in the proceedings. A few late-news papers also will be accepted, covering only the most recent and noteworthy developments.

The late-news submission deadline is 22 August 2022.

The IEEE IEDM is the premier forum for technological breakthroughs in semiconductor and related device technology, manufacturing, design, physics and modeling. Each year, the world’s leading technologists gather to participate in a technical program of more than 220 presentations, panels, focus sessions, tutorials, Short Courses, supplier exhibits, IEEE/EDS award presentations and other events highlighting the industry’s best work.

IEDM 2022 encourages submissions in all areas, with special emphasis on:

- Neuromorphic/in-memory computing / AI
- 2.5/3D integration
- Quantum computing devices
- Devices for RF, 5G/6G, THz and mm-wave
- Technologies for advanced memory and logic nodes
- Power distribution network
- Non-charge-based materials, devices and systems
- Advanced power devices, modules and systems
- Sensors, MEMS and bioelectronics
- Devices/circuits/system interaction
- Package-device level interactions
- Electron device simulation and modeling
- Reliability of systems and electronic devices
- Robustness/security of electronic circuits and systems
- Optoelectronics, displays and imaging systems

The IEDM 2022 technical subcommittees are as follows:

- Advanced Logic Technology (ALT)
- Emerging Device and Compute Technology (EDT)
- Memory Technology (MT)
- Microwave, Millimeter Wave and Analog Technology (MAT)
- Modeling and Simulation (MS)
- Optoelectronics, Displays and Imaging Systems (ODI)
- Power Devices and Systems (PDS)
- Reliability of Systems and Devices (RSD)
- Sensors, MEMS and Bioelectronics (SMB)

Further information

For more information, visit the IEDM 2022 home page at www.ieee-iedm.org.

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cated to advancing technology for the benefit of humanity. Through its highly cited publications, conferences, technology standards, and professional and educational activities, IEEE is the trusted voice in a wide variety of areas ranging from aerospace systems, computers, and telecommunications to biomedical engineering, electric power, and consumer electronics. The IEEE Electron Devices Society is dedicated to promoting excellence in the field of electron devices and sponsors the IEDM.

2022 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)



Downtown Phoenix skyline

The 2022 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS) will be taking place in downtown Phoenix, Arizona during 16–19 October, and is the 5th year of the successful merger between the original Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) and the Compound Semiconductor IC Symposium (CSICS). BCICTS is the premier forum for the presentation and discussion of the latest developments in bipolar, BiCMOS, and

compound semiconductor circuits, devices, and technology. Coverage includes all aspects of these technologies, from materials, through device fabrication, device phenomena, TCAD modeling, compact modeling, integrated circuit design, testing, to system applications. A wide range of integrated circuit technologies are covered, including bipolar and field-effect transistors realized in materials such as SiGe, GaAs, GaN, InP, SiC. The latest results in wireless, analog, RF, microwave, high-speed

digital, mixed signal, optoelectronic, millimeter wave, and THz integrated circuits are embraced.

The conference itself will take place at the newly renovated Sheraton Phoenix Downtown, conveniently located to many popular dining, shopping, and entertainment options and near many interesting sites located in downtown Phoenix, including Chase Field, the Arizona Science Center, the Phoenix Art Museum, and the Heard Museum, known for its dedication to American

Indian art. The Phoenix area boasts world-class golf courses as well as numerous options for other outdoor activities, with Papago Park, home of the Phoenix Zoo and the Desert Botanical Garden, located only a 15-minute drive from downtown. Farther afield, the world-famous Red Rocks of Sedona lie only a 2-hour drive north of the downtown area. Two hours north of Sedona lies the Grand Canyon, one of 7 wonders of the Natural World.

The technical committee for BCICTS has lined up an exciting and informative array of speakers for the 2022 conference, which will begin with a series of short courses on Sunday 16 October, “Millimeter-wave and THz sensors—Systems,

circuits, devices, and technologies” including courses on System architectures, Circuit building blocks, SiGe BiCMOS technology, and InP technology for mm-wave and THz applications. These short courses will be taught by internationally renowned experts of their field. Sunday will also include a primer course, “Simulation tools for RF design”, before the Plenary and contributing sessions begin on Monday morning, 17 October. Anchoring the contributing sessions will be more than ten invited talks arranged by the technical subcommittees of BCICTS. These invited talks are representative of the wide range of topics and subject matter experts that the BCICTS conference brings together,

of a diversity and depth of synergistic knowledge covering the latest topics and advances in the rapidly progressing field of semiconductor technology and circuits unmatched by any other conference. For registration and up to date information, including a listing of the researchers who are scheduled to give an invited talk and their respective topics for this year’s conference, please visit the BCICTS website at www.bciets.org. The members of the BCICTS organizing committee cordially invite you to join us there!

*2022 IEEE BCICTS Organizing
Committee
Jay John
2022 BCICTS Publicity Chair*

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SOCIETY NEWS

MESSAGE FROM EDS NEWSLETTER EDITOR-IN-CHIEF



Daniel Tomaszewski
EDS Newsletter
Editor-in-Chief

Dear Readers, Members of the IEEE EDS Community,

Welcome to the IEEE EDS Newsletter issue July 2022.

Let me briefly draw your attention to the content

of a new installment of the newsletter. First of all I recommend two articles written by Prof. Chenming Hu and Prof. B. Jayant Baliga, as the Society's contribution to the celebration of the 75th Anniversary of Transistor. Both eminent Authors share with us reflections on the developments of transistors for integrated circuits and of high power/high voltage devices. Needless to say, both Authors have made tremendous contributions to their fields of interest.

The Technical Briefs section brings us the next article summarizing the current status of the International Roadmap for Devices and Systems (IRDS™), namely C. Michael Garner presents Outside System Connectivity Roadmap. The Upcoming Technical Meetings section includes information about two important conferences: IEEE International Electron Devices Meeting 2022 (IEDM) and 2022 IEEE BiCMOS and Com-

pound Semiconductor Integrated Circuits and Technology Symposium (BCICTS).

In the Women in Engineering section please find the article by Prof. Mona E. Zaghloul, who describes her fascinating adventure of research, teaching and mentoring in integrated circuits, nanoelectronics and sensors. Prof. Zaghloul emphasizes an issue of barriers for women willing to work in engineering. Hard work and persistence are needed to overcome them. She had experienced this herself. In the Young Professionals section we present an interview of Manoj Saxena with Dr. Jiaju Ma, 2021 IEEE EDS Early Career Award Winner.

Further parts of this Newsletter issue include news on technical, societal and humanitarian activities led by the Chapters in Regions 8 and 10. The term "humanitarian activity" brings to my mind a need to help Ukrainian people during and after a terrible and unjust war to which they fell victim.



Larry Larson

After a short introduction to the Newsletter content I would like to introduce to you Larry Larson, who has been appointed as the

new EDS Newsletter Regional Editor for Regions 5 & 6, i.e. Southwestern & Western USA. Dr. Larson is the Retired Professor of Practice, Electrical Engineering. His long professional career included academic and industrial positions in semiconductor technology, electronics, physics, to name a few. We are very glad to welcome Larry in our team and we wish him fruitful work for the EDS Newsletter. In parallel, I would like to thank Muhammad Mustafa Hussain for his service and the time he devoted to the Newsletter. Muhammad, we wish you a lot of success in your further work for the Society.

Dear Readers, if you have any suggestions, comments regarding the Newsletter contents, please do not hesitate to contact us. We will be very glad to receive your feedback. Interesting views will be presented with the consent of the authors, along with our replies in the Letters to Editors section.

Finally, I would like to thank all the Authors and all the members of the Editorial Team. My gratitude goes particularly to Joyce Lombardini and Manoj Saxena for their continuous support in our work.

I sincerely wish you all good summer holidays. Take care of yourself.

Sincerely,
Daniel Tomaszewski

CALL FOR NOMINATIONS—EDS BOARD OF GOVERNORS



Cary Yang
EDS Nominations &
Elections Chair

The IEEE Electron Devices Society invites nominations for election to its Board of Governors – BoG (formerly AdCom) members-at-large. The next election will be held after the BoG meeting

on Sunday, 4 December 2022. This year, seven out of the twenty-two members will be elected for a 3-year term, with a maximum of two terms.

A member can only serve for a maximum of two terms as a BoG member in a lifetime. Therefore, the eligibility will be verified for all nominees who will be voted on by the EDS BoG. All electees begin their term in office on 1 January 2023. The nominees need not be present to run for the election.

Any EDS member who has served for a minimum of one year as an EDS Officer, Vice-President, Standing & Technical Committee Chair/Member, Publication Editor and Chapter Chair is eligible to be nominated, unless otherwise precluded from doing so in the EDS Constitution and Bylaws. The electees are required to attend at least one BoG meeting every year. While the December meeting is organized in conjunction with the IEEE International Electron Devices Meeting, the mid-year meeting is frequently held outside the US. Partial travel support is available to attend BoG meetings.

All nominees must be endorsed by one BoG member, i.e., one of the four officers (President, President-Elect, Treasurer or Secretary), the Jr. or Sr. Past President or one of the 22 current BoG Members-at-Large. It is the

responsibility of the nominators and the endorers to make sure that, if elected, the nominee is willing to actively serve in the position as a BoG member-at-large. Self-nomination is acceptable.

Please submit your EDS BoG nomination by 15 October 2022, using the online nomination form at: (<https://ieeeforms.wufoo.com/forms/k4vnyad0ys3o4z/>).

Also, all endorsements letters should be submitted using the online form: <https://ieeeforms.wufoo.com/forms/q1d5l2jz1pps20g/> by 15 October 2022.

If you have any questions, please feel free to contact Laura Riello (l.riello@ieee.org) with a copy to me at cyang@scu.edu.

Cary Yang
Chair of EDS Nominations & Elections

EDS BOARD OF GOVERNORS (BoG) MEMBERS-AT-LARGE ELECTION PROCESS

The Members-at-Large (MAL) of the EDS Board of Governors (BoG) are elected for staggered 3-year terms. The EDS Constitution and Bylaws mandates the number of elected MAL to be a total of 22 members with at least two members from each of the following geographic areas: Regions 1-7 and 9; Region 8; and Region 10. Our Constitution and Bylaws also require that at least one elected BoG member is a Young Professional. A Young Professional member is defined by IEEE as a member who graduated with his/her first professional degree within the last fifteen years. It is also required that a slate of nominees for members-at-large comprising a minimum of 1.5 times the number of vacancies to occur. We also have a two-term lifetime limit for a volunteer to serve as a BoG Member-at-Large, which must be

considered for nominations. All nominees will be voted on by the EDS BoG in its meeting in December 2022. All electees begin their term in office on 1 January 2023. The nominees need not be present to run for the election. In 2022, seven positions will be filled.

The election procedure begins with the announcement of Call for Nominations in the *EDS Newsletter*. The slate of nominees is developed by the EDS Nominations & Elections Committee. Nominees are asked to submit a two-page biographical resume and an optional 50 word personal statement in a standard format.

Any EDS member who has served for a minimum of one year as an EDS Officer, Vice-President, Standing & Technical Committee Chair/Member, Publication Editor & Chapter Chair is eligible to be nominated, unless oth-

erwise precluded from doing so in the EDS Bylaws. All nominees must be endorsed by one BoG member, i.e., one of the four officers (President, President-Elect, Treasurer or Secretary), the Jr. or Sr. Past President or one of the 22 current BoG MAL. Self-nomination is allowed. Endorsers should submit their online endorsement form by the deadline. Please note that there is no limit to the number of candidates that a full voting BoG member can endorse.

The deadline for Nominations will be 15 October 2022. The biographical resumes and endorsement letters will be distributed to the BoG prior to the December BoG meeting. The election will be held after the conclusion of the BoG meeting on 4 December 2022.

Cary Yang
Chair EDS of Nominations & Elections

IEEE ANNUAL ELECTION

This is a reminder for EDS members to vote in the 2022 IEEE Annual Election for the following positions and candidates. Listed below are the positions and candidates up for election.

The order of candidate names has been pre-determined by lottery and indicates no preference.

In addition, the IEEE Board of Directors voted to place an amendment to the IEEE Constitution on the ballot. View the member discussion Forum in Collabratec.

Position	Candidate
IEEE President-Elect, 2023	<ul style="list-style-type: none"> • Thomas M. Coughlin (Nominated by IEEE Board of Directors) • Maïke Luiken (Nominated by IEEE Board of Directors) • Kazuhiro Kosuge (Nominated by Petition) • Kathleen A. Kramer (Nominated by IEEE Board of Directors)
IEEE Division Delegate-Elect/Director-Elect, 2023 IEEE Division I	<ul style="list-style-type: none"> • Yong Lian (Nominated by IEEE Division I) • Samar K. Saha (Nominated by IEEE Division I)
IEEE Region Delegate-Elect/Director-Elect, 2023–2024 Region 2 (Eastern USA)	<ul style="list-style-type: none"> • Rhonda L. Farrell (Nominated by IEEE Region 2) • Felicia Harlow (Nominated by IEEE Region 2)
Region 4 (Central USA)	<ul style="list-style-type: none"> • Tarek Lahdhiri (Nominated by IEEE Region 4) • Hamid Vakilzadian (Nominated by IEEE Region 4) • Constance A. Kelly (Nominated by IEEE Region 4)
Region 6 (Western USA)	<ul style="list-style-type: none"> • Joseph C. Wei (Nominated by IEEE Region 6) • Gora Datta (Nominated by IEEE Region 6)
Region 8 (Africa, Europe, Middle East)	<ul style="list-style-type: none"> • Michael G. Hinchey (Nominated by IEEE Region 8) • Adeel Sultan (Nominated by IEEE Region 8)
Region 10 (Asia and Pacific)	<ul style="list-style-type: none"> • Byung-Gook Park (Nominated by IEEE Region 10) • Takako Hashimoto (Nominated by IEEE Region 10)
IEEE Standards Association Board of Governors Member-at-Large, 2023–2024 Position 1:	<ul style="list-style-type: none"> • David T. Chen (Nominated by IEEE Standards Association) • Kishik Park (Nominated by IEEE Standards Association)
Position 2:	<ul style="list-style-type: none"> • Sha Wei (Nominated by IEEE Standards Association) • Dorothy V. Stanley (Nominated by IEEE Standards Assoc.)
IEEE Technical Activities Vice President-Elect, 2023	<ul style="list-style-type: none"> • Manfred J. Schindler (Nominated by IEEE Tech. Activities) • Rakesh Kumar (Nominated by IEEE Technical Activities)
IEEE-USA President-Elect, 2021	<ul style="list-style-type: none"> • Keith A. Moore (Nominated by IEEE-USA) • James R. Look (Nominated by IEEE-USA)

Balloting period starts on 17 August 2022 and ends at 12:00 PM, Eastern Time USA (16:00 UTC) on 1 October 2022. All eligible voting members can access their ballot electronically at www.ieee.org/elections. In accordance with their member communication preferences on record on 30 June 2022, voters will receive voting instructions via email and/or a ballot package via postal mail (members can vote electronically or on paper ballots, but only one ballot will be accepted.) For more information on the election and candidates, visit the IEEE Annual Election web page at www.ieee.org/elections, or email election@ieee.org.

ANNOUNCEMENT OF 2023 EDS CHAPTER SUBSIDY PROGRAM



*Murty Polavarapu
EDS Vice President
of Regions/Chapters*

The IEEE Electron Devices Society (EDS) is offering financial support to our chapters for serving local members through the EDS Chapter Subsidy Program for 2023. Chapters interested in obtaining funds need to submit an EDS chapter subsidy request form. The deadline for submission is **1 September 2022**.

Please note that the maximum funding amount for each requesting EDS chapter may vary and is derived based on the total available subsidy

budget and number of requests. But the amount does not exceed \$1,000 for EDS only chapters and \$500 for chapters jointly sponsored by EDS and any other IEEE society(ies).

The subsidy can be used to fund Chapter meeting expenses, membership promotion, travel expenses for invited speakers to chapter events, and support for EDS student activities at local institutions.

Please note that in addition to this Chapter Subsidy Program, other channels of funding available to you include the annual Chapter subsidy from IEEE Member and Geographic Activities, funding for Mini-colloquia and funding for EDS Humanitarian Projects. Final decisions concerning

subsidies will be made in December 2022. Subsidy funds will be issued in January 2023.

For advice in coordinating the activities of your chapter you can contact the members of the Regions/Chapter Committee and/or Sub-Committee for Regions/Chapters (SRC). For additional information on the chapter subsidy program, please visit the EDS website.

On behalf of IEEE and the EDS, I would like to thank you for your time and efforts devoted to the missions of IEEE and EDS.

*Murty Polavarapu
EDS Vice President of Regions/
Chapters
Space Electronics Solutions*

AWARDS AND CALLS FOR NOMINATIONS

2022 IEEE EDS WILLIAM R. CHERRY AWARD WINNER

2022 IEEE William Cherry Award presented at the 49th IEEE PVSC to Stephen R. Forrest

B. A. Physics, 1972, University of California, MSc and PhD Physics in 1974 and 1979, University of Michigan. In 1985, Prof. Forrest joined USC and, in 1992, moved to Princeton University. In 2006, he rejoined the University of Michigan as Vice President for Research, where he is the Peter A. Franken Distinguished University Professor. A Fellow of the APS, IEEE and OSA and a member of the National Academy of Engineering, the National Academy of Sciences, the American Academy of Arts and Sciences, and the National Academy of Inventors, he has received numerous awards and medals for his invention of phosphorescent



*Stephen R. Forrest
Peter A. Franken Distinguished University
Professor of Engineering
Paul G. Goebel Professor of Engineering
Professor of Electrical Engineering, Physics
and Materials Science and Engineering*

OLEDs, innovations in organic LEDs, organic thin films and advances in photodetectors for optical communications. Prof. Forrest has authored ~647 papers in refereed journals and has 365 US patents. He is co-founder or founding participant in several companies, including Sensors Unlimited, Epitaxx, Inc., NanoFlex Power Corp. (OTC: OPVS), Universal Display Corp. (NASDAQ: OLED) and Apogee Photonics, Inc., and is on the Growth Technology Advisory Board of Applied Materials. He is past Chairman of the Board of the University Musical Society and served as Chairman of the Board of Ann Arbor SPARK. He has served on the Board of Governors of the Technion – Israel Institute of Technology

where he is a Distinguished Visiting Professor of Electrical Engineering. He received an honorary doctorate from the Technion in 2018, and the Henry Russel Lectureship at the University of Michigan in 2019. His first book, *Organic Electronics: Foundations to Applications*, was published in September, 2020. Steve has long experienced all the advantages of solar power at his off-grid house which is mostly powered by the sun in the Green Mountains of Vermont.

About the Award

This award is named in honor of William R. Cherry, a founder of the photovoltaic community. In the 1950's, he was instrumental in establishing solar cells as the ideal power source for space satellites and for recognizing, advocating, and nurturing the use of photovoltaic systems for terrestrial applications. The William R. Cherry award was instituted in 1980, shortly after his death. The purpose of the award is to recognize an individual engi-

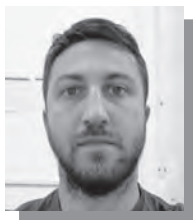
neer or scientist who devoted a part of their professional life to the advancement of the science and technology of photovoltaic energy conversion. The nominee must have made significant contributions to the science and/or technology of PV energy conversion, with dissemination by substantial publications and presentations. Professional society activities, promotional and/or organizational efforts and achievements are not considerations in the election for the award.

2020-2021 EDS Region 9 Outstanding Student Paper Award

The IEEE Electron Devices Society confers its prestigious Region 9 Outstanding Student Paper Award to the best Region 9 student paper published in an internationally recognized IEEE sponsored journal or conference in the field of electron devices related topics.

The winning paper is entitled, "Reliability-Aware Design Space Exploration for Fully Integrated RF CMOS PA". This paper was published in the *IEEE Transactions on Device and Materials Reliability* and was authored by Sebastian Pazos, Fernando Aguirre, Felix Palumbo and Fernando Silveira. The award will be presented at the 2022 IEEE Latin American Electron Devices Conference (LAEDC), which will be held on 4-6 July 2022 in Puebla, Mexico.

The Award consists of a certificate and reimbursement of up to US \$1,500 to cover one author's travel and accommodations to attend the conference. On behalf of the IEEE Electron Devices Society, I would like to congratulate Sebastian Pazos and the remaining authors for this achievement. Brief biographies of all the authors of the paper are given below.



Sebastian Matias Pazos received his degree in Electrical Engineering in 2015 and his PhD in 2021 by Universidad Tecnológica Nacional,

Facultad Regional Buenos Aires (UTN.BA), Argentina. He received fellowships from DAAD, UTN.BA and CONICET and was Interim Professor and TA at UTN.BA. He is currently a Postdoctoral Fellow at King Abdullah University of Science and Technology (KAUST), Saudi Arabia, and member of the EDS Nanotechnology Committee. He co-authored more than 20 articles in international journals and was co-awarded 3 best paper awards in international conferences. His interests include CMOS RF/AMS circuit design, advanced materials integration, device/circuit reliability and neuromorphic hardware.

Fernando L. Aguirre (M. 2022) received the electronics engineering degree in 2016 and his PhD in engineering in 2021, both from the UTN-FRBA



(Argentina). He received the UTN-DAAD, CIN-EVC (undergraduate student) and the CONICET (PhD) grants. He has co-authored almost

50 papers in international journals and conferences and received three best paper awards (PRIME-LA 2017, SBmicro 2019 and IRPS 2019). In 2019 he was a visiting PhD researcher in the UAB (Spain). From 2013-2021 he was Teaching Assistant and Adjunct Professor at UTN-FRBA, teaching CMOS Analog Electronics. His research interests include dielectric reliability, Resistive Switching, memristor-based Neuromorphic computing and CMOS design.



Felix Palumbo received the M.Sc. (2000) and the Ph.D. (2005) both in physics from the University of Buenos Aires (UBA), Argentina.

He is research staff of the National

Council of Science and Technology (CONICET), and Full Professor at National Technological University (UTN) Buenos Aires, Argentina, working in the field of semiconductor device physics and reliability, with experience in academia and industry. He was a fellow of Marie Curie Fellowship Program, Abdus Salam International Center for Theoretical Physics (ICTP, Italy), CONICET (Argentina), and CNR (Italy). He has authored and co-authored more than 50 papers in international conferences and journals.



Ph.D. in Microelectronics from Université Catholique de Louvain, Belgium in 1995 and 2002. He is currently Professor at the Electrical Engineering Department of Universidad de la República. His research interests are in the design of ultra-

Fernando Silveira received the Electrical Engineering degree from Universidad de la República, Uruguay in 1990 and the MSc. and

low-power analog and RF integrated circuits and systems, in particular with biomedical application. He is coauthor of two books and many technical articles. He has had multiple industrial activities, including leading the design of an ASIC for implantable pacemakers and designing modules for implantable devices.

*Navakanta Bhat
EDS Region 9 Award Chair*

2022 EDS CHAPTER OF THE YEAR AWARD CALL FOR NOMINATIONS

The IEEE EDS Chapter of the Year Award is given each year based on the quantity and quality of the activities and programs implemented by the chapters during the prior July 1st–June 30th period (for 2022 awards—activities and programs between July 1, 2021, and June 30, 2022). Virtual events can also be included.

EDS recently revised our Chapter of the Year Award to award one non-student chapter and one student chapter in any geographic location.

Nominations for the awards can only be made by Regions/Chapters Committee Members, SRC Chairs/Vice-Chairs, or self-nominated by Chapter Chairs. Please visit the EDS website to submit your nomination form (<https://eds.ieee.org/awards/chapter-of-the-year-award>).

Each year each winning chapter (maximum 2) will receive a plaque and check for \$500 to be presented at an EDS chapter meeting of their choice. Travel reimbursement will not be provided. A chapter that has previously received the Chapter of the Year Award is eligible for re-nomination only after three years from the year of award.

The schedule for the award process is as follows:

ACTION	DATE
Call for nominations e-mailed to chapter chairs, SRC Chairs, SRC Vice-Chairs and Regions/Chapters Committee	July
Deadline for nominations	September 15th
Regions/Chapters Committee selects winners	October
Award presented to chapter representative at requested chapter meeting	Open

EDS WOMEN IN ENGINEERING

INTEGRATED CIRCUITS, NANOELECTRONICS, SENSORS APPLICATIONS

MONA E. ZAGHLOUL, PROFESSOR, DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING,
SCHOOL OF ENGINEERING AND APPLIED SCIENCE, THE GEORGE WASHINGTON UNIVERSITY,
800 22ND STREET, N.W., RM 5550, WASHINGTON, DC 20052,
ZAGHLOUL@GWU.EDU

Background and Education



I was born in Cairo, Egypt, at a time during which the Royal family still ruled Egypt. My mother and father had obtained their Ph.D. degrees in chemistry from England and were Professors of Chemistry at Cairo University. They often took me with them, and I watched the long hours of hard work they both spent in the chemistry lab. I finished high school with above-average grades in 1960. I was accepted to Cairo University and chose to study electronics there. By the end of my undergraduate career, I met my husband (my

classmate), and we were married soon after graduating. I traveled with my husband to Canada in 1968 and joined the Department of Electrical Engineering at the University of Waterloo as a Research Assistant. I continued my studies there and obtained my master's degree in Electrical Engineering in 1970. After my master's degree, I joined the School of Mathematics at the University of Waterloo to pursue a second master's degree, this one in Applied Mathematics and Computer Science. At that time, the University of Waterloo was a pioneer in studying computer science and programming language. I graduated with my second master's degree in 1971. Towards the end of my degree, I was offered an opportunity

to pursue a Ph.D. with a professor of Electrical Engineering whose work focused on computer-aided design of nonlinear electronics and circuits. CAD tools such as SPICE were first introduced around that time for simulating and designing circuits. My thesis work focused on modeling circuits and electronics. The time that I spent working on my Ph.D. in the early 1970s was unique and exciting. This was the early Internet, and our Waterloo network, called WITS, was one of the first such networks in the world. I was awarded my Ph.D. in 1975.

I was the first woman to graduate with a Ph.D. from the School of Engineering at the University of Waterloo, Canada. I did not know this at the time. But in retrospect, I had noticed that I was often the only woman in attendance in most of my engineering courses. This was very different from my undergraduate experience. Many years later, I was awarded an Honorary Ph.D. degree in 2007 from the University of Waterloo. It is awarded an honorary Ph.D. degree in recognition that I was the first female graduate from their School of Engineering and my career and accomplishments in research and teaching.

Move to the USA and early career

We moved to the United States in 1978. My husband was offered a position at COMSAT, Inc., a communications satellite company in the Washington, DC area. At our move, I



Figure 1. Zaghloul with her students in her Research Laboratory at George Washington University

had two young children – a four-year-old boy and a four-week-old girl. I moved to the DC area with my family and started looking for a job.

I was interested in working in academia because I had seen my mother and the example she had set. It wasn't easy, though, mainly because I was a woman. I did not know that female engineers were rare in the US. I met an individual early in my job search who told me, *"Ma'am, you are a woman, an engineer, and you are a foreigner (thinking I was French Canadian). Do you think you will find a job in this place? This is Washington, DC, the top of the nation."* Many of the recruiters I met told me that it was near impossible for a woman with a Ph.D. in engineering to find a job. My job search was more difficult because I had a husband and two small children and was limited in terms of the geographic area in which I could search for and accept a position.

I was eventually offered a job at the Computer Science Corporation; my first job involved programming using several programming languages I had studied and drew upon my experiences while writing code at Waterloo. Although my Ph.D. was focused on modeling and simulation electronics circuits, I accepted this initial position to work as a computer scientist while I continued my search for an academic job in my major area of expertise. I continued writing papers on my Ph.D. work and submitting them for publication during my free time. It wasn't easy, but after several attempts, I was finally offered a job as an Assistant Professor in the Department of Electrical Engineering and Computer Science (EECS) at George Washington University in Washington, DC. I was the first woman hired in the School of Engineering and Applied Science at GWU. This was a big change for many other faculty members, and many did not accept this change. The Chair of the EECS Department at the time was Professor Ray Pickholtz. He was well known in the field of communica-

tions, and he certainly believed in my ability to work and produce quality research. In addition, he knew that I could teach computer science courses in addition to courses in electrical engineering. His support during this early time was critical. I had experience developing Computer-Aided Design tools (CAD tools) for electrical circuits and developing simulations of circuits with active components. In addition, I was very familiar with circuit theory as a result of the courses I attended during my Ph.D. graduate courses.

I started my teaching position at GWU in 1980 by introducing several new courses on circuit theory, computer-aided tools for circuit simulation, and modelling linear and nonlinear circuits. I also taught optimization, graph theory, and programming courses in different languages. These changes were unique to the graduate curriculum at GW, and the

courses attracted several students. At the time, my courses were introducing new knowledge in computer science, and the students were appreciative. My students were mainly from government agencies around the DC area attending evening classes.

In 1984, I applied for a position at the National Institute of Standards and Technology (NIST), which was called the National Bureau of Standards (NBS) at that time. I was hired by Dr. Ken Galloway, the head of the Semiconductor Electronic Technology Division. I applied for the position because I was interested in pursuing research and was trying to find better facilities than were available at GW. I was trying to create collaborations in the area. I was hired as a "faculty hire" to go to NIST one day a week in addition to my teaching job at GWU. The NIST job was an important step in my career. I was exposed to the best laboratories and the best

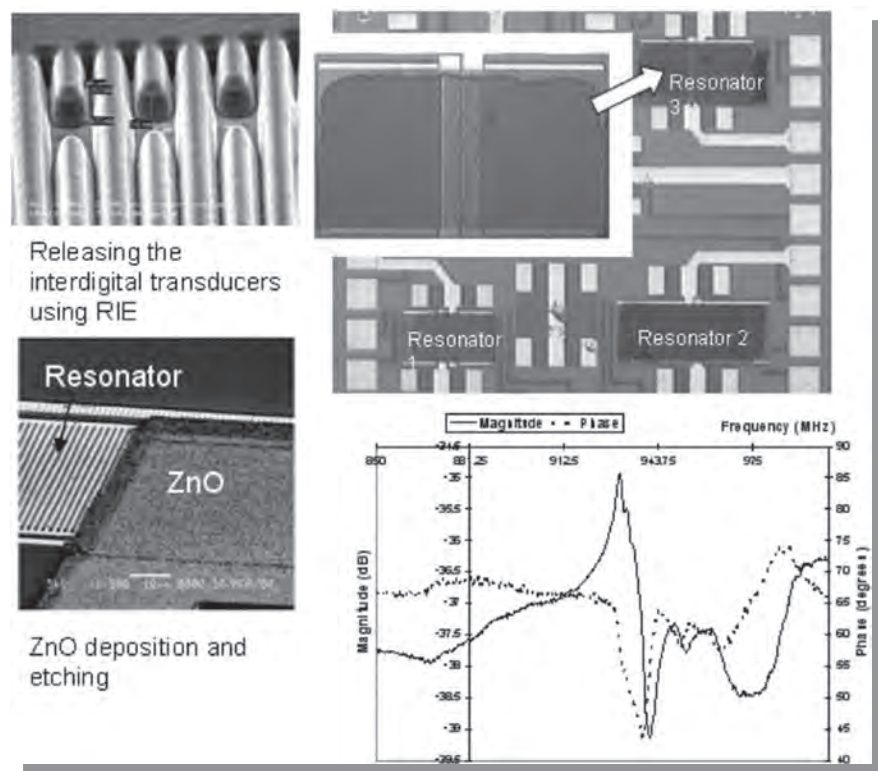


Figure 2. Surface Acoustic wave resonators which are used as Filter for Transmitter/Receiver systems. It was developed using CMOS technology with post-processing steps to obtain the resonators. Reference: Anis N. Nordin, Mona E. Zaghloul, "Modeling and fabrication of CMOS Surface Acoustic Wave Resonators"; IEEE Transactions on Microwave Theory and Techniques, Vol. 55, No.5, May 2007, pp. 992–1002.

research scientists specializing in semiconductor electronics research. I was exposed to extensive techniques for measuring and testing electronic circuits and testing electronic materials, and applying the industry standards. In addition, I learned how to fabricate devices in the cleanroom facility at NIST and the basics of chip designs. In 1984, a course was offered by MOSIS (MOS Integrated Systems) was funded by the US Government) for learning the design of integrated circuit chips. The course was offered by top leading university professors at the time, and the goal of the course was to teach other university professors, and consequently their students, the art of VLSI chip design. Professor Carver Mead from the California Institute of Technology was the lead Professor. The course was offered at the MOSIS building at Marina Del Rey for two weeks. The US government set up this new initiative to motivate academic researchers to begin designing and building integrated circuit chips. I learned many things from this course. I started designing Complementary Metal Oxide Silicon (CMOS) chips for fabrication and testing. This skill was in demand in the Semiconductor Electronics Technology Division at NIST, where I worked. It was essential to design test structures to measure the performance of devices for different technologies. I collaborated with many of my colleagues in the division on these tasks. In addition, I started teaching chip design at GWU and started sending our chips to MOSIS for fabrication. We sent several students' projects using analog and digital integrated circuit designs to MOSIS for fabrication. MOSIS returned the fabricated chips to GWU, where we tested the chips and prepared testing reports for submission back to MOSIS. I added several other courses to the GWU curriculum to reflect the depth of CMOS design. I wanted to carry out several research projects and applications using CADENCE software.

I started a collaboration with University of Maryland Professor Robert Newcomb on designing Neural Networks and trying to implement the neuron with the ability to learn and process data. Several students were trained in building hardware for learning Neural networks, and as a result, several students earned their Ph.D. in this topic. Therefore, several GWU students graduated with knowledge of CMOS chip design, and my NIST knowledge of the industry standard and requirements is reflected in their courses. Many of these students are now part of a productive force in top IC design companies like Intel, Apple, Google, etc. As a result of our knowledge of the theory and design of Neural Networks, we learned about their applications to the classification of data and especially for large data (Big Data). Thus, I was asked by my NIST colleagues to develop a Ma-

chine learning approach for classifying large semiconductor data, and I was asked to write the code and verify it (that was in 1994). In 1996, I was awarded IEEE Fellow for my work on Integrated Circuits chips design and the Circuits we developed for implementing Neural Networks mimicking the firing and the learning of the neuron. In 2017, I was selected as a Fellow of the National Academy of Inventors (NAI), recognizing my patents in microelectronics and MEMS.

In 1990 the NIST team started paying attention to Microelectromechanical Systems (MEMS) design and expanding the scope of the CMOS materials to all possible other materials. I joined this effort at that time. In MEMS work, you have to be very familiar with the different layers of the material. The designer has to add and subtract new materials to construct the MEMS device. To verify

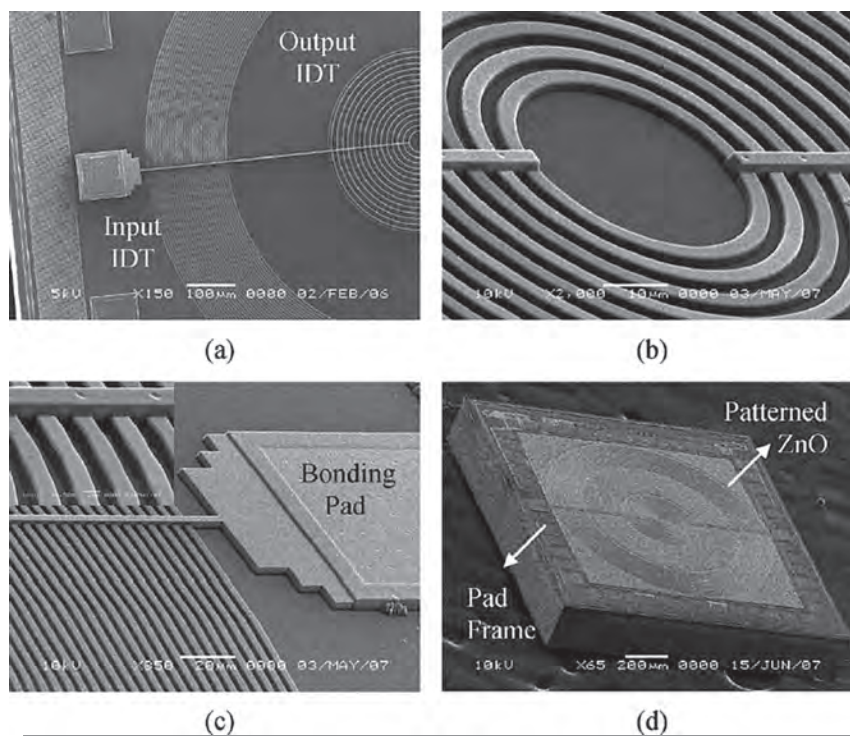


Figure 3. Novel Circular Surface Acoustic wave, which can be used as resonator or biosensor. (a) Top view SEM (Scanning Electron Microscope) of the circular SAW chip after CMOS and before postprocessing. (b) Close-up view of the inner IDT after the RIE step with 90 sidewalls. (c) Close-up view of the outer IDT with the pad after RIE. (d) Top view SEM snapshot of the device after the final step of ZnO patterning. Reference: Onur Tigli, Mona E. Zaghloul; "Design, Modeling, and Characterization of a Novel Circular Surface Acoustic Wave Devices"; IEEE Sensors Journal, Vol.8, Mo. 11, November 2008, pp 1807, 1815.

the designed and fabricated devices, the designer must have extensive knowledge of deposition and etching of different materials, material interaction, cleanroom facility equipment, and imaging equipment. I had a large team of students from GWU help me, try several recipes, and work on developing novel devices for MEMS applications. The applications chosen were to develop sensors. We used most of the available CAD tools to simulate the MEMS devices. Our team designed several novel MEMS devices. The devices were patented and were acquired by the industry. I

had several Ph.D. students working with me at NIST. We used MEMS to implement varieties of novel sensors, and it was an opportunity to add the electronics on the chip to yield smart sensors.

I also used CMOS technology to build novel MEMS devices by adding to the CMOS technology other materials on the surface of the fabricated CMOS device (Surface Micromachining) or by etching layers from the standard CMOS technology (Bulk Micromachining) or possibly using both techniques at the same time. We developed several novel devices and

sensors with integrated electronics. An example was developing a mechanical Surface Acoustic Wave device (SAW) for resonator applications and biosensors.

The work was acknowledged, and several students graduated using these techniques, and many joined the industry for MEMS design with the knowledge of IC design. They were hired as VLSI designers in addition to the skills of MEMS designers. Recently, I joined the material science group at NIST to synthesize 2D materials and start designing electronics circuits using 2D material. I have been working with the Material synthesis group at NIST for more than five years on 2D material. My students and I designed different transistors using different 2D materials and using 2D materials for sensors. For the design of 2D materials, the designers have to know how to build the devices in a clean room and measure the devices and use imaging equipment to have an image of the device. Several devices were fabricated and tested at the NIST laboratory and my GWU laboratory. Recently, GWU added a clean room to its new facility, which allowed our students to use it to build novel devices and use excellent imaging equipment to characterize the fabricated devices.

In 1989 I was promoted to Full Professor at the Department of Electrical and Computer Science. Again, I was the first woman to be appointed Full Professor at the George Washington University School of Engineering and Applied Science. This was a big step, and I think it opened the door for many other women to follow. Several female professors were hired at GWU School of Engineering, and a whole different era started.

The number of women engineers is still small in proportion to all engineers. For example, in the USA and Canada, it is about ~ 11%, and in Australia, it is about 9.6%. Other European countries such as Latvia, 30%, Bulgaria, 29.3%, Cyprus, 28.6%, and Sweden, 25.9%. China: the percentage of

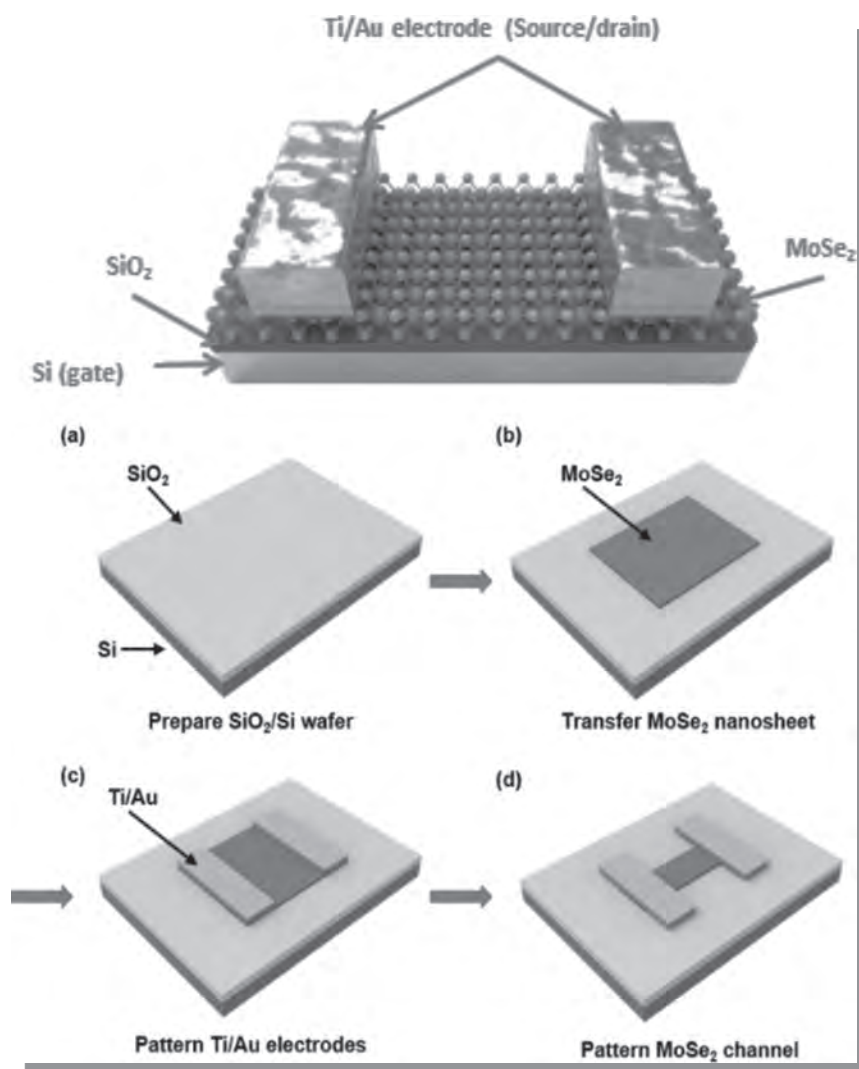


Figure 4b. Fabrication Process of transistor in the Clean Room, Reference: Shiqi Guo; "TMDS-based Soft and Wearable Bioelectronic Toward Precision Health Care"; The George Washington University, Washington, DC, PhD. Thesis, June 2019; Measurements of the transistor characteristics are shown in Figure 5.

women engineers is 40%. The IEEE, Institute of Electrical and Electronics Engineers, an International organization headquartered in New Jersey, USA, created the Women in Engineering Organization (WIE) as an affinity group in 1994. WIE celebrated its 23rd anniversary in 2017, and the estimated number of members is 24,000. WIE is very active in many regions in the US and globally: Asia, Latin America, Europe, and Africa.

Now GWU School of Engineering and Applied science undergraduate classes 2018 is about 25% female students, which is considered one of the highest in the country. Thus, several female undergraduate students are attracted to Engineering, and female engineers are now recognized and respected as productive engineers. I teach several female students in my classes, and I am proud of their accomplishments. Many professional societies recognize women in engineering and encourage women to join the profession. I have been impressed by the progress of female engineers since I started my career, and certainly, it has been a long road since 1970.

Professor experience at The George Washington University: Challenges and Successes

In the early years at GWU, I was repeatedly presented with the most challenging assignments. It seemed to me that my fellow male colleagues were eager to see whether a woman could do what was, at the time, still primarily a man's job. My only choice was to respond to their increasing challenges with increasingly hard work and the tools my education provided me. In 1994 I was elected the Chair of the Electrical and Computer Science Department. I was the First Woman to be Department Chair in the School of Engineering and Applied Science. The EECS department was a large Department with many faculties in the whole university.

I wanted to keep my research work going because I like to do research.

I succeeded in managing the department, and we received accreditations from ABET with no problems for years. I hired several Assistant professors and Associate Professors and tried to increase the Department's research areas. I kept my work with NIST and was at NIST with my students, learning new technologies and directions, producing new devices, and educating my students on the latest technology directions. I was the Chair of the Electrical Engineering and Computer Science Department from 1994-1998. I ended my first period as chair. I went on sabbatical at Delft University in the Netherlands.

In 2000 the EECS department was separated into two departments, the Electrical and Computer Engineering Department and Computer Science Department.

In 2009, my colleagues elected me as Department Chair for the Department of Electrical and Computer Engineering. I worked as Chair from 2009-2014. I kept my research and maintained contact with NIST, and I was always eager to learn new technology and introduce new technology courses to my students. Thus, I spend my time learning nanotechnology and specifically nanoelectronics. I taught a new course on nanoelectronics and introduced the students to nanofabrication. Now with the new cleanroom at GWU, the course is taught with the cleanroom laboratory to teach the students nanofabrication. Currently, I am working with

material scientists at NIST to synthesize 2D materials which we are using for electronics applications as flexible electronics. 2D materials are atom-thick layers of materials, and they became active research areas after the discovery of graphene.

In 2014 I was hired as Program Director at the National Science Foundation in the Division of Electrical, Communication, Cyber, Systems (ECCS). I was responsible for the Circuits, Communications, Sensors, Systems program CCSS. I worked at NSF from January 2014-December 2016. It was a very productive time, and indeed, I learned and met many new researchers in my areas of interest.

In 2017 I returned to George Washington University and concentrated on my research. Currently, I am focused on the following areas of research:

- Research on integrated circuit design as an interface for sensors, complete with fabricating and testing chips (mostly CMOS technology) with emphasis on flexible electronics components and integrating small CMOS components on a flexible substrate.
- Research on MEMS/NEMS design and fabrication to develop novel sensor devices using different materials with emphasis on biosensors for health care systems.
- Program on nanotechnology with emphasis on realizing nanodevices for electronics and sensors applications

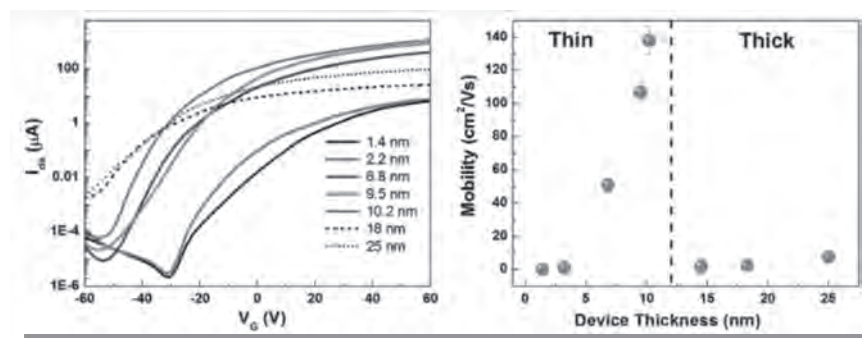


Figure 5. Measurements Characteristics of nanotransistors. Reference: Shiqi Guo; "TMDs-based Soft and Wearable Bioelectronic Toward Precision Health Care"; The George Washington University, Washington, DC, PhD. Thesis, July 2019.

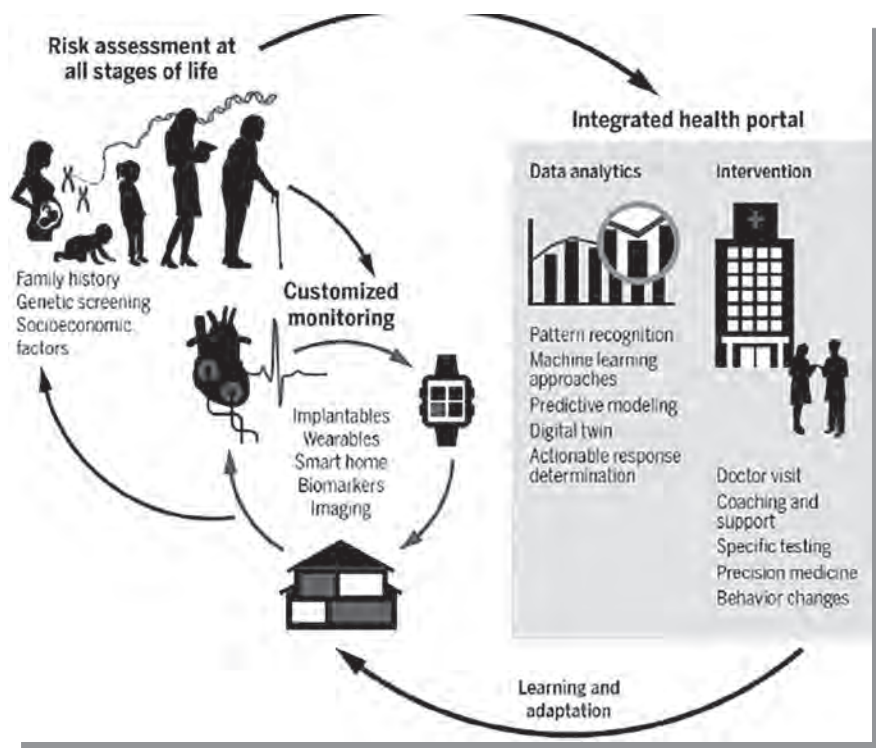


Figure 6. Precision health care overview; after S. S. Gambhir, et al., "Toward achieving precision health," *Sci. Transl. Med.* 10, eaao3612 (2018).

We are currently working on several projects under the above topics.

I promoted women in engineering and encouraged women undergraduates to be active in research. Over my career of 39 years at GWU, out of 38 Ph.D. dissertations completed under my supervision, 8 (21%) were female, and out of 24 Master's theses, 4 (17%) were female. All-female and male graduates are currently working in industry (Silicon Valley, etc.) and in academia (the US and abroad), with several having leading positions. At the GWU School of Engineering and Applied science SEAS, the number of undergraduate female students improved considerably, reaching 39.8% of the total number of students in 2018. For graduate students, the percentage of female students reached 26.7% of total students, above average

nationwide. While this certainly leaves plenty of opportunity for growth, we must recognize and take pride in the gap narrowed in the past 40 years.

Future and Prospective

I introduced several new technical initiatives, several courses, and research areas during my career:

- Program on integrated circuit design, complete with fabricating, and testing chips (mostly CMOS technology)
- Program and Institute on MEMS/NEMS design and fabrication
- Program on nanotechnology which emphasizes realizing nano-devices for electronics and sensor applications.

There are many directions of research with an emphasis on health care; It is true that in the near future,

we will have sensors attached or embedded in our body for complete monitoring of our health care. We are living in a fascinating time. New technologies are being developed around us all the time. We see tiny machines the size of one billionth of a meter. We are building with the individual atoms. This is an era of melding between man and machine. We are at a multidisciplinary time where the boundaries between electrical, mechanical, civil, chemical, and bioengineering are rapidly fading. This is truly the era of science and engineering, and it is an exciting time to be an engineer or a scientist. The possibilities to create novel things appear limitless. For young women engineers, my advice is that opportunities are endless. There are many directions, and being an engineer is an outstanding opportunity. You are the only limit to your achievements; you can achieve whatever you set your mind to with hard work and persistence. It may not have been done before, but that does not mean it can't be done. Education is essential, and it gives you the foundation and the confidence that help shape your career.

In the following, I will briefly give examples of devices developed in our laboratory. Many of the devices we micro/nanofabricated in a clean room, and most are patented.

Recently my research included nanoelectronics material for implementations of nanotransistors, examples of nanomaterial.

Currently, we are working on health care sensors. Precision health care, as shown in the following Figure 6, where sensors are implanted in the body or attached as wearable or distributed in the smart home, generate the health data. The data are analyzed, and the action response is determined.

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Use promotion code **EDSWIE2022**



The image features a woman in the foreground, looking thoughtfully at a complex digital interface. The interface is overlaid with various data visualizations, including a world map with location markers, a line graph, a bar chart, and a waveform. In the top right corner of the interface, the IEEE Women in Engineering (WIE) logo is displayed, consisting of the text "IEEE Women in Engineering" in a sans-serif font and "WIE" in a large, stylized script font. The overall aesthetic is high-tech and professional.

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#IEEEWIElead



EDS YOUNG PROFESSIONALS

JIAJU MA: REFLECTIONS FROM AN EDS YOUNG PROFESSIONAL

2021 IEEE EDS EARLY CAREER AWARD WINNER

The Young Professional guest in this Newsletter issue is Jiaju Ma, IEEE Electron Devices Society's 2021 Early Career Award winner. The discussion reflects his perceptions about EDS and views regarding professional development and career growth. Here are the excerpts of the interview made by Manoj Saxena, the Newsletter Associate Editor-in-Chief, with Jiaju Ma.

Manoj Saxena (MS): What was the specific temptation, if any, which made you join EDS, which is the largest professional organization in the globe, at first?

Jiaju Ma (JM): I have been working on the research and development of novel semiconductor devices since 2012. More specifically, my work is focused on novel image sensor pixel devices that can realize photon-counting capabilities with ultra-low readout noise. IEEE EDS is the largest organization globally in the field of semiconductor devices as well as the field of my research interests. It was a natural decision for me to join EDS, and it has always been the best platform for me to publish my work and learn from other scientists. I am proud to be part of the ED community, and I am excited to make more contributions to the organization in the future.

(MS): You won the prestigious EDS Early Career Award, an honor most of the young professionals aspire to. How do you consider this recognition, and what are your plans to further develop your research career?

(JM): It is a great honor to win the EDS Early Career Award. This pres-



tigious recognition has been very inspiring to me because it came from scientists and experts from the same field. It is a remarkable motivation to continue devoting my career to this field. As the co-founder and CTO of Gigajot Technology, Inc. (Pasadena, CA), I am currently leading the research and development activities in the startup to commercialize the Quanta Image Sensor technologies, which emerged from my Ph.D. research work. We have successfully brought this technology to the market by launching three sensor products for high-performance scientific and professional imaging applications. The plan is to continue the R&D and product development based on this technology and bring its unique capabilities to a broader range of applications, including consumer imaging, and create larger benefits for Society and humanity.

(MS): As a Young Professional, how do you position your interest in your field with the activities and

services you perform as an EDS member/volunteer?

(JM): As an EDS member, I have been actively publishing my own research work in the EDS conferences and journals such as IEDM, TED, EDL, and JEDS. The scopes of these conferences and journals are well aligned with my research interests. Attending the conferences hosted by EDS always allows me to connect with other outstanding researchers globally in my field. I also often get invited to review the papers submitted to the EDS journals.

(MS): What are your thoughts about the EDS membership and its paybacks? Whether the EDS membership benefited you at any time in your career growth? If so, how?

(JM): I have benefited from the ED Society and its membership for more than a decade since my Ph.D. research. Publishing my work in the EDS journals, reading others' research activities in the Society, and attending the EDS conferences are essential for the progress of my research work and irreplaceable for the growth of my career.

(MS): As a YP, how do you consider the Society as a whole, and what are the changes or developments you would like to see in evolving this professional body as a group devoted to humanity and its causes?

(JM): The ED Society has been doing a great job, in my opinion. A good addition can be an online archive for the recorded presentations from the conferences. It will be very valuable for those who cannot attend the events in person.

(MS): What are your suggestions and recommendations for those young professionals who may aspire to join EDS?

(JM): I strongly recommend other young professionals to join EDS. This is a very supportive community that can provide numerous opportunities for them to learn, grow, and make an impact in this field.





(MS): As an EDS Young Professional and a young researcher in the field, how do you consider the prospects of scientific research in this field for the progress of Humanity as a whole?

(JM): Our world is experiencing an unprecedented technological evolution powered by semiconductor devices. The pandemic further speeded up this transition. New technologies like artificial intelligence, autonomous driving, and AR/VR are emerging and changing daily lives. The further development of semiconduc-

tor devices, fabrication processes, and chip integration is at the heart of this technological revolution. As a young professional, I feel it is a very exciting time to work in our field, and there are a lot of opportunities for us to contribute to the progress of humanity as a whole.

Jiaju Ma is a pioneering inventor and entrepreneur in the field of CMOS image sensors and Quanta Image sensors. Ma is the co-inventor and designer of the first CMOS image sensor pixel devices with deep sub-electron read noise that enables photon counting and photon-number resolution without using electron multiplication, generally referred to as a Quanta Image Sensor (QIS). This innovative device can clearly distinguish individual photoelectrons and has a small pitch size that enables megapixel resolution and which is compatible with standard CMOS im-

age sensor manufacturing processes for mass production. The low-noise photon-counting pixel device that Ma co-invented and developed is being commercialized at Gigajot Technology (Pasadena, CA), a startup co-founded by Ma. Ma received his B.S. in Applied Physics from Nankai University, China, and his Ph.D. in Engineering Sciences from Dartmouth College, New Hampshire, USA. At Gigajot, he serves as CTO and leads the engineering work to advance further the performance and readiness of this technology for mass production in both high-performance and consumer applications. Ma has over 50 technical publications and holds over 20 US patents and patent applications. He is one of the two awardees of the 2021 IEEE EDS Early Career Award. He also served as a technical committee member of the International Image Sensor Workshop (IISW) in 2019.

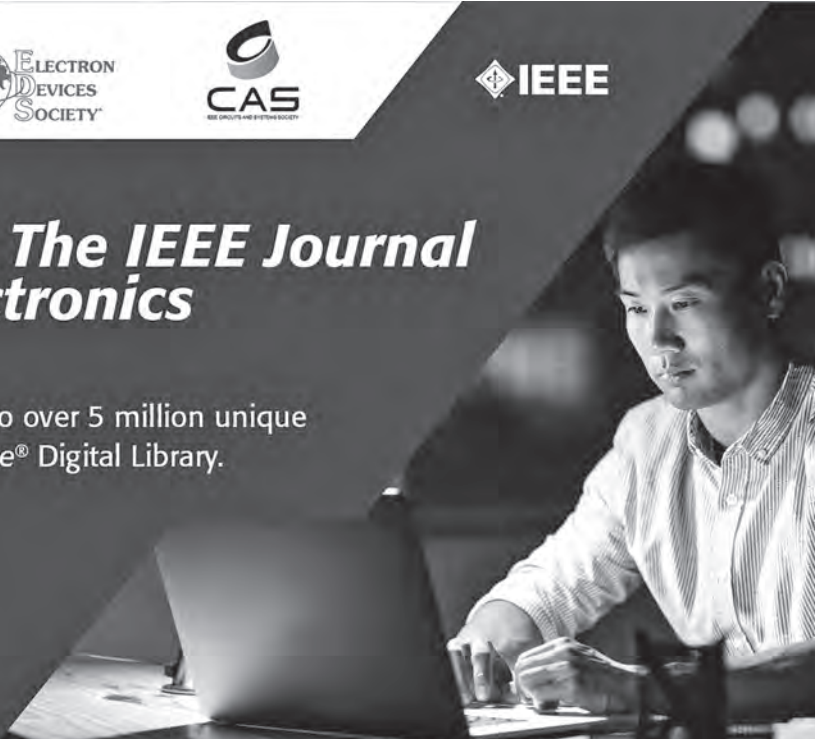


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HUMANITARIAN PROGRAMS

VRIKSHA PHASE-V: A TREE PLANTATION DRIVE

On 13 March 2022, the IEEE ED MSIT Student Branch Chapter in association with the Rotaract Club of Meghnad Saha Institute of Technology as a part of the World Rotaract Week Initiative, organized at MSIT College Campus an event, Vriksha Phase-V: A Tree Plantation Drive.

The motivation of the event was to create an awareness in building a cleaner and a greener Earth for a healthy and balanced life in the ecosystem. Thirty attendees took part in the program, ten of whom were IEEE members and all contributed to the planting of 30 saplings.

An overview of a balanced life in a cleaner and greener environment was given by Prof. Sahana Sengupta, faculty member of Basic Science and Humanities of Meghnad Saha Institute of Technology.

~Soumya Pandit, Editor



Vriksha Phase-V: A Tree Plantation Drive at MSIT College Campus

CHAPTER NEWS

MINI-COLLOQUIUM ON "MEMRISTIVE DEVICES" AND SYMPOSIUM ON SCHOTTKY BARRIER MOS 2022

By MIKE SCHWARZ

The event will be held in hybrid format, onsite and via Zoom, with the R&D event beginning on 7 September 2022 with a mini-colloquium on "Memristive Devices," and the Symposium on SB-MOS scheduled for 8 September.

The following lecturers will present at the MQ:

- Prof. M. Lanza (KAUST, Saudi Arabia)
- Prof. E. Miranda (Universitat Autònoma de Barcelona, Spain)
- Prof. B. Iniguez (Universitat Rovira i Virgili, Spain)

The following speakers are scheduled for the SSBMOS:

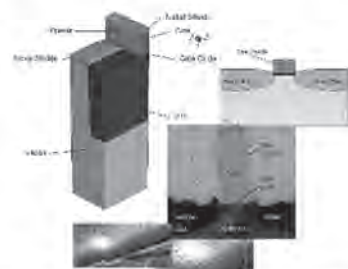
- Dr. Radu Sporea (Advanced Technology Institute, University of Surrey, Guildford, UK)
- Dr. Laurie E. Calvet (C2N, CNRS-Université Paris-Sud, France)
- Dr. Richard Forbes (Advanced Technology Institute, University of Surrey, Guildford, UK)
- Prof. Walter Weber (TU Vienna, Austria)

This year the joint R&D event is sponsored by the THM and the IEEE

EDS Germany Chapter, and organized by Dr. Laurie Calvet (C2N, Palaiseau, France), Prof. Mike Schwarz (NanoP THM, Germany), Prof. Alexander Kloe (NanoP THM, Germany) and the staff at the THM.

Attendees are welcome to participate in our joint R&D event. The attendees are limited in total to 300. Further information and registration is present at <https://meetings.vtools.ieee.org/m/311092>.

~Mike Schwarz, Editor

<p>IEEE Mini-Colloquium (MQ) "Memristive Devices"</p> <p>The MQ will provide an open forum for education and discussion of memristive devices and trends in the evolution of applications for hardware based artificial intelligence. Lectures will cover basics of memristive device materials and introduce promising applications of those.</p> <p>IEEE Distinguished Lecturers:</p> <ul style="list-style-type: none"> - Prof. M. Lanza (KAUST, Saudi Arabia) - Prof. E. Miranda (Universitat Autònoma de Barcelona, Spain) - Prof. B. Iniguez (Universitat Rovira i Virgili, Spain) <p>Symposium on Schottky Barrier MOS Devices</p> <p>The symposium goal is to combine the activities of an enthusiastic group of Schottky barrier researchers worldwide. The topics cover all important aspects of potential applications, simulation and modeling, processing and implementation for CMOS/SOI technologies, Quantum technologies and approaches for neuromorphic applications. The content is targeted for those seeking to learn the current opportunities and challenges of this technology. New aspects and future proposals to make the Schottky barrier into the main stream are welcome.</p> <p>Tentative Speakers:</p> <ul style="list-style-type: none"> - Dr. R. Sporea (University of Surrey, UK) - Dr. R. Forbes (University of Surrey, UK) - Dr. L. Calvet (C2N, France) - Prof. Walter Weber (TU Vienna, Austria) <p>The Event</p> <table border="0"> <tr> <td>IEEE Mini-Colloquium</td> <td>07. September 2022</td> </tr> <tr> <td>Symposium SB MOS Devices</td> <td>08. September 2022</td> </tr> </table> <p>On September 7th a conference dinner is organized and included in the registration.</p> <p>Abstract and Deadlines</p> <p>Intended authors should send an abstract (max. 300 words) to the email (alexander.kloe@el.thm.de) with the event of interest and note the following deadlines:</p> <table border="0"> <tr> <td>Receipt of abstract</td> <td>30. June 2022</td> </tr> <tr> <td>Notification of acceptance</td> <td>31. July 2022</td> </tr> <tr> <td>Registration deadline</td> <td>31. August 2022</td> </tr> </table>	IEEE Mini-Colloquium	07. September 2022	Symposium SB MOS Devices	08. September 2022	Receipt of abstract	30. June 2022	Notification of acceptance	31. July 2022	Registration deadline	31. August 2022	<p>Registration & Price Information</p> <p>The IEEE Mini-Colloquium & Symposium on Schottky Barrier MOS devices is for free, no fees required. The attendance does not include accommodation and transport.</p> <p>The registration takes place by the vTools of IEEE. The following link is provided: https://meetings.vtools.ieee.org/m/311092</p> <p>WWW</p> <p>Further information are present under http://ssbm.blogsport.com</p> <p>The Venue</p> <p>The joint workshop is held at the Competence Center for Nanotechnology and Photonics, TH Mittelhessen - Univ. of Applied Sciences, Giessen, Germany.</p> <p>Giessen, is a small city in the German federal state of Hessen. The population is approximately 86000, with roughly 24000 university students. The name comes from Giezzen, as it was first referred to in 1197, which refers to the position of the town between several rivers, lakes and streams. The largest river in Giessen is the Lahn, which divides the town in two parts (west and east), roughly 65 kilometers (40 miles) north of Frankfurt am Main.</p> <p>Travel Arrangement</p> <p>Air: Giessen is served by Frankfurt Main Airport (FRA), located 70 km south of the city center. From FRA various connections by railway are available.</p> <p>Rail: Direct railway connections from Frankfurt mainstation are available. Connection from Frankfurt airport to mainstation are available by metro and/or intercity connections. Airport to Giessen connection takes approximately 1 hour. Mainstation to Giessen approximately 50 minutes.</p> <p>Road: Giessen can be easily reached by road from major cities in Europe by A5, A45 and A485.</p> <p>Organized by: Prof. Alexander Kloe, NanoP, Germany - Prof. Mike Schwarz, NanoP, Germany - Dr. Laurie Calvet, C2N, Palaiseau, France</p>	<p>Students welcome! Free workshop!</p> <p>ANNOUNCEMENT</p> <p>1st CALL FOR PAPERS</p> <p>Symposium on Schottky Barrier MOS Devices 2022</p> <p>IEEE MQ "Memristive Devices"</p>  <p>THM NanoP</p> <p>IEEE</p> <p>Advancing Technology for Humanity</p> <p>AdMOS</p> <p>Giessen, Germany, 7th Sept. - 8th Sept. 2022</p>
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IEEE EDS MALAYSIA SENIOR MEMBER ELEVATION WORKSHOP 2022

By P SUSTHITHA MENON, AHMAD SABIRIN ZOOLFARKAR, MAIZATUL ZOLKAPLI, ZUHAINA ZAKARIA & MERLYN DE SOUZA

The Chapter hosted a virtual IEEE Senior Membership Elevation Workshop, 10 March 2022 via Google Meet. The event was held in conjunction with International Women's Day 2022 on 8 March, where three prominent women gave their remarks with regards to senior member elevation

in IEEE. The event was moderated by the Chapter Chair, Assoc. Prof. Ir. Ts. Dr Ahmad Sabirin Zoolfakar from UiTM Shah Alam, with opening remarks by the IEEE Malaysia Section Chair 2021-2022, Assoc. Prof. Ir. Dr. Pauzi Abdullah from UTM Johor. The participants were fortunate to

listen to the views of IEEE EDS Vice-President of Membership, Prof. Dr. Merlyne de Souza (University of Sheffield), and Prof. Ir. Dr. Zuhaina Zakaria (UiTM Shah Alam), the Chair of IEEE Admission and Advancement Committee. The speakers gave overviews on the benefits of senior member elevation and the review panel's perspective. Finally, a step-by-step method on documenting the Senior Member application form was given by Assoc. Prof. Dr. P Sushitha Menon, Member, IEEE EDS Board of Governors from IMEN, UKM. During the workshop, Dr. Susi presented an overview of member grade elevation procedures and recognition, requirements for senior membership elevation and case studies. The workshop was attended by 20 people and adjourned at 12 noon.

Women In Engineering Career Talk 2022 for School Students

—by P Sushitha Menon, Bernard Lim, Ahmad Sabirin Zoolfakar, Maizatul Zolkapli, Lim Xiao Xian, Presanna

On 25 March 2022, the Institution of Engineers Malaysia (IEM) Penang Branch in collaboration with IEEE ED Malaysia Chapter, IEEE ED UKM Student Branch, IET Malaysia, TAM, PWDC and Penang STEM, held a Women in Engineering Career Talk for higher secondary school students. The online event was held via Zoom and was attended by 90 school students from all over Malaysia. The Branch Chair, Ir Bernard Lim briefed the students on the motivation of the talk, which was to give students, especially women and girls, an overview of the different career options that an engineering undergraduate will have upon graduation. In this series, Assoc. Prof. Dr. P Sushitha Menon from IMEN,



IEEE EDS MALAYSIA SENIOR MEMBER ELEVATION WORKSHOP

**DATE: 10 MARCH 2022
(THURSDAY)**
TIME: 3PM TO 5PM
PLATFORM: GOOGLE MEET
LINK: <https://meet.google.com/vwp-xinj-zdq>

SPEAKER:
ASSOC PROF. DR.
P SUSTHITHA MENON

Member, IEEE Electron Devices
Society (EDS) Board of Governors



MODERATOR:
ASSOC PROF. IR. DR.
AHMAD SABIRIN ZOOLFARKAR
2021/2022 Chair,
IEEE EDS Malaysia



Organizer: IEEE EDS MALAYSIA

Senior member is the highest grade in IEEE. All members who have been a member of IEEE for at least 5 years can be nominated as a Senior Member. Join us to know more about the promotion procedures. This workshop is open to all IEEE members.


Poster of the IEEE EDS Malaysia Senior Member Elevation Workshop

UKM, Member of IEEE EDS Board of Governors, gave an Introduction to Engineering from the perspective of an academician. The students were briefed on the various career paths

available if they are interested in being an engineering educator or lecturer. The session ended with a Kahoot quiz where winners received e-wallet vouchers sponsored by the ED Malay-

sia Chapter. The students were highly motivated with the engineering field and asked various questions.




~Sharma Rao Balakrishnan, Editor



Women In Engineering


JPN approval ref: JPNPP(UKK) 100-4/4 J1d 52(28)

Monthly Invited Speakers: Listen to our speakers from the industry, academician, consultant and many more in order to understand the different types of engineering discipline as a career.


 <p>Speaker 1: Ir. Catherine Sim Siew Ping The Institution of Engineers, Malaysia (Penang Branch)</p>	<p>Date: 19 February 2022 Time: 10.00am – 12.00pm Topic: Introduction to Engineering: General</p>
 <p>Speaker 2: Assoc. Prof. Dr. P. Susthitha Menon The National University of Malaysia (UKM)</p>	<p>Date: 26 March 2022 Time: 10.00am – 12.00pm Topic: Introduction to Engineering: Academia</p>
 <p>Speaker 3: Ms Soon K. Kuek General Manager, LAMResearch</p>	<p>Date: April 2022 Time: 10.00am – 12.00pm Topic: Introduction to Engineering: Manufacturing</p>

More speakers in the coming months....

Participating organization:



Registration:



event.iempenang.org

Free Admission for Students

Poster of the Women in Engineering Career Talk 2022

REGIONAL NEWS

EUROPE, MIDDLE EAST & AFRICA (REGION 8)

Successful Hiroshi Iwai, IEEE EDS Distinguished Lecture on “Impact, History and Future of Nanoelectronics”

—by Mike Schwarz

An impressive and outstanding lecture took place on 18 February 2022. What was it about? The title of the lecture was “Impact, History and Future of Nanoelectronics”, given by Prof. Hiroshi Iwai, Vice Dean and Distinguished Professor from ICST, NYCU, Taiwan.

The DL was organized by the ED Germany Chapter and co-sponsored by the NanoP from THM - University of Applied Sciences. The DL was attended by 19 IEEE participants and 23 non-IEEE members.

Prof. Iwai gave an outstanding overview and perspective of the next upcoming decade. He started with a historic review of the past and set focus on the performance increase of the last 115 years. He showed the essential KPI parameters of MOSFET

devices and their impact regarding the performance limit of downsizing. Furthermore, Prof. Iwai offered where the physical limit of the real physical gate length will occur and what is the difference regarding the commercial nm technology names. The lecture contained a detailed explanation of the four main impacts, i.e. punch through current, direct tunneling leakage, subthreshold leakage, and gate insulator leakage. Furthermore discussion took place, which effects could be avoided and which limit the physical gate length, e.g. direct tunneling impact.

After the discussion an outlook of the near future (next 15 years) was given, the movement towards nanosheet transistors and 3D stacking of those with experimental data. Approaches, as die to wafer smart bonding and resistivity of narrow metal lines were presented by Prof. Iwai. The presentation continued with a far future outlook and the challenges to be accepted by potential engineers and scientists as the readers of this article. We need you!

Finally, Prof. Iwai referred to the differences between AI and the human brain and where the potentials and advantages of both are and how

to combine and overcome the current bottlenecks. The lecture concluded with a following discussion on certain topics.

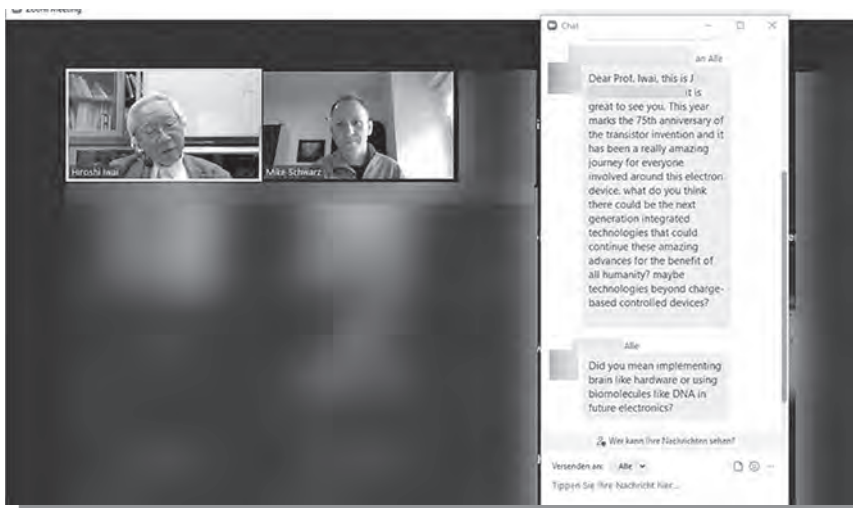
Successful Hybrid—Benjamin Iniguez, IEEE EDS Distinguished Lecturer on “2D Semiconductor FET Modeling”

—by Mike Schwarz

It felt somehow strange entering a lecture room at THM and introducing Prof. Benjamin Iniguez for the IEEE EDS Distinguished Lecture “2D Semiconductor Modeling” in front of students and staff of the Device Modeling Research Group of NanoP from THM – University of Applied Sciences. Shortly announced, 12 IEEE participants and 8 non-IEEE members attended the lecture, where 10 were present at the THM and 10 by Zoom. After almost more than two years of pandemic a portion of normality came back into daily business.

The distinguished lecture was organized by the ED Germany Chapter and co-sponsored by the NanoP from THM—University of Applied Sciences. Prof. Benjamin Iniguez from University Rovira i Virgili, Spain gave an overview of 2D Semiconductors with the focus set on modeling of those devices. He highlighted different technological and physical aspects of those devices in comparison with experimental data of TU Vienna fabricated by Max Lemme’s group at AMO Aachen, Germany.

As said, Prof. Iniguez started with an introduction into the topic and properties of 2D semiconductors. The discussed TMDs (Transition metal dichalcogenide) band structure depending on the layers, gave insights of black phosphorus, and pWSe2 and nMoS2 on Wafer devices. Afterwards, the physical mechanisms related to



Prof. Hiroshi Iwai answering and discussing Q&A of the attendees

also being shared on social media, i.e., the IEEE EDS Malaysia YouTube channel to increase the visibility of IEEE EDS and as an approach for membership promotion.

ED Malaysia's Distinguished Expert Webinar in Conjunction with 75th Anniversary of the Transistor

—by Maizatul Zolkapli, Ahmad Sabirin Zoolfakar, Rosminazuin Ab Rahim, Norhayati Soin, Azrif Manut, Iskandar Yahya, P Susthitha Menon

In conjunction with the 75th Anniversary of the Transistor, the Chapter together with the Institute of Microengineering and Nanoelectronics (IMEN), Universiti Kebangsaan Malaysia (UKM) and IEEE ED UKM Student Branch Chapter held a very prestigious event, a Distinguished Expert Webinar on 1 April 2022, to commemorate the significant roles of Micro and Nanoelectronics in our lives. The title of the talk was "From Micro to Nanoelectronics;" conducted in hybrid mode. About 15 people attended the talk physically while 110 others joined online via the Zoom platform. We were honoured to have Prof. Dato' Dr. Burhanuddin Yeop Majlis, the renowned figure of Mi-



IEEE EDS Malaysia members with Prof. Dato' Dr. Burhanuddin Yeop Majlis (second from left)

croelectronics in Malaysia to share his insights on Micro and Nanoelectronics. His pictorial and nostalgic talk portrayed the evolution of microelectronics during the early years until where we are today and he shared how EDS Malaysia was established in Malaysia. Prof. Burhanuddin must be commended for proliferating the field of Micro and Nanoelectronics in Malaysia and for moulding many experts in this field.

IEEE International Conference on Semiconductor Electronics (ICSE) 2022

—by Maizatul Zolkapli & Ahmad Sabirin Zoolfakar

The ED Malaysia Chapter is pleased to welcome everyone to participate in the 2022 IEEE International Conference on Semiconductor Electronics (ICSE) on 15–17 August 2022. Since 1992, this bi-annual technical

conference has aimed to bring together researchers from industry and academia to gather and explore various issues and trends in the field of semiconductor electronics. This is the 15th ICSE organized by the Electron Devices Chapter of IEEE Malaysia Section and technically co-sponsored by the IEEE Electron Devices Society. Over the last twenty-eight years, the ICSE conference series has become the prominent international forum on semiconductor electronics embracing all aspects of the semiconductor technology from circuit device, modelling and simulation, photonics and sensor technology, MEMS technology, process and fabrication, packaging technology and manufacturing, failure analysis and reliability, material and devices and nanoelectronics. Please visit our website for further details <https://ieeemalaysia-eds.org/icse2022/about-icse/>



Poster of the event



ED Indonesia Chapter

—by Basuki Rachmatul Alam

The Chapter conducted EDS Summer School 2021, as a selected program funded by IEEE EDS and supported by State Polytechnic of Batam. The summer school was held in hybrid mode (in person and online) from 23-25 August 2021. The EDS Summer School titled “IoT System in Package assembly for Humanity application” was a blended education program combining a series of lectures and hands-on manufacturing work of IoT System in Package (SIP) modules in assembly lines of TFME (Teaching Factory Manufacturing Electronics), on the State Polytechnics of Batam campus, in Batam Island, Indonesia. After opening speeches from Director of Polytechnic of Batam, IEEE Indonesia Section Chair, ED Indonesia Chapter Chair and Prof. Navakanta Bhat, EDS Vice-President of Education (recorded speech), the EDS Summer School began 23 August with a 2-day series of lectures on microelectronics and nanotechnology as the main driver of IoT Technology.

The lectures were presented online on Day 1:

- Prof. Mohammad Nizar Hamidon of ITMA-Universiti Putra Malaysia, “Flexible patch Antenna using Ferrimagnetic Materials for IoT”



Lab Session—IOT IC Packaging

- Dr. Manoj Saxena of Universiti New Delhi, “Modeling and Simulation of Robust Ultrasensitive Tunnel Field Effect Transistor Design for Biosensing Applications”
- Two tutorial sessions on microelectronics and IC back-end assembly by TFME staff

The second day events included tutorials and lectures:

- Dr. Basuki Rachmatul Alam, ED Indonesia Chapter, began a tutorial on related MEMS technology on presence IoT Technology
- Prof. Dr. Khairurrijal, Faculty of Mathematic and Natural Sci-

ence of Institute of Technology Bandung (ITB), “Progress of Electrospun Nanofibers-based Electronics and Sensors”

- Prof. Dr. Trio Adiono of Microelectronic Center of ITB, “The SoC Baseband Processor Design for VLC”
- Simon Deleonibus, PhD of CEA LETI and EDS Distinguished Lecturer, “New Routes and Paradigms in Device Engineering for Nanoelectronics and Nanosystems”

The Summer School hybrid session drew 33 registered participants throughout the country and neighbouring country (Malaysia) whose participation consisted of 17 online and 16 in person participants. The number of participants was limited due to compliance to pandemic health protocol and inherent limitation on the number of personnel per unit of assembly manufacturing lines at TFME was restricted.

On the 3rd and 4th day, participants learned hands-on manufacturing of IoT SIP modules from PCB manufacturing processes, PCB Assembly (component assembly on PCB or SMT), and IC Assembly (IC packaging). Two hands-on device Assembly (IC Packaging) of the IoT SIP sessions were taught to the participants subsequently on the 4th day. On the last day (5th), all participants’



Lab Session—IOT PCB Manufacturing



Closing EDS Summer School School Closing Ceremony

cognitive level of knowledge on Summer School subject material were assessed through a short quiz and a group essay project presentation of a certain topic of IoT SIP chosen by all group members on the previous day. Every participant in turn presented his/her part of IoT SIP Module, and was questioned at the end of their presentation by a panel of 3 jurors formed from faculty members. Moreover, all student participants from ITB (Institute of Technology Bandung) are allowed to transfer the learning hours and evaluation grade to credit of regular undergraduate curriculum of study program in SEEI (School of Electrical Engineering and Informatics) of ITB abiding by recently introduced program by General Directorate of Higher Education, Ministry of Education, Culture and Research of Indonesia: Independent Learning based on Independent Curriculum.

~Sharma Rao Balakrishnan, Editor

ED Delhi Section Chapter

—by Harsupreet Kaur and Manoj Saxena

To mark the celebration of 75 Years of the invention of the transistor, the ED Delhi Chapter in association with the

National Academy of Sciences India (NASI)-Delhi Chapter and Deen Dayal Upadhyaya College, organized an “International Symposium on History and Future of Transistors” under the aegis of DBT Star College Program. The event was held 23-30 December 2021, and included 11 talks given by eminent speakers invited from across the world. The distinguished speakers who shared their expertise:

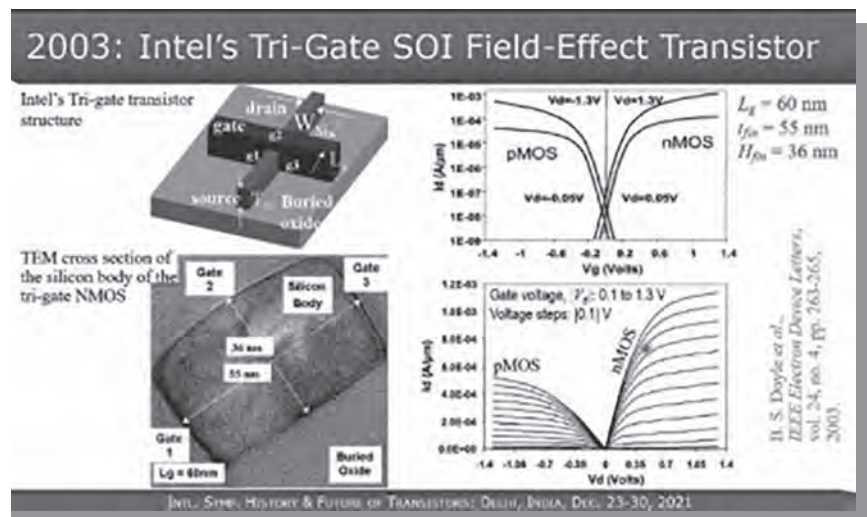
- Prof. R. Muralidharan, IISc Bangalore
- Prof. Sanjay Banerjee, University of Texas

- Dr. Samar Saha, Santa Clara University
- Prof. Amitava DasGupta
- Prof. Shreepad Karmalkar, IIT Madras
- Prof. Kaustav Banerjee, University of California
- Prof. Udayan Ganguly
- Prof. Swaroop Ganguly, IIT Mumbai
- Prof. Renuka P. Jindal, Vanderbilt Institute of Science and Technology
- Prof. Satyabrata Jit, IIT BHU
- Prof. Nihar R. Mohapatra, IIT Gandhinagar

Lectures covered diverse topics in the area of semiconductor devices and microelectronics and laid focus on Silicon MOS devices and their role towards transformation of the digital ecosystem. A large number also covered compound semiconductors, 2D materials, and some emerging areas such as atomistic modeling, nano and super junctions, spintronics etc. More than 230 participants from across the world attended the symposium.

The chapter organized several events in collaboration with major universities in the area:

On 13 January 2022, in association with the Department of Electronic Science, University of Delhi South Campus, organized a technical talk on



the topic “Role of Science and Technology in the Development of Society.” The speaker was Sh. Raj Singh of the Institute for Plasma Research, Gandhinagar. He summarized the evolution of the electronics industry in India over the last few decades. The talk was attended by over 70 participants.

The Department of Electronics, University of Jammu in collaboration with the Chapter, organized a one-day webinar 20 January 2022, on Advanced Semiconductor Devices for Industrial Applications. Prof. Chandan Kumar Sarkar, ex-professor of Electronics and Telecommunication Engineering, Jadavpur University, and Dr. Ajit Kumar Panda, emeritus professor at NIST-Berhampur delivered lectures on “Semiconductor Industry towards Tunnel FET” and “Semiconductor Devices for 2G to 5G Communication Technology,” respectively. The program was attended by more than 70 participants.

In association with the Department of Electronic Science, University of Delhi South Campus, a technical talk on “6G: Testing Next-Generation Sub-Terahertz Applications,” was organized for 21 January 2022. The speaker, Mr. Vishal Gupta, Keysight Technologies, India, provided a brief overview of electromagnetic spectrum by explaining all the dedicated bands from VHF, UHF to Sub terahertz frequencies, and also focused on the WiGig, alternatively known as 60 GHz Wi-Fi. The lecture attracted over 70 participants.

The Department of Instrumentation of Shaheed Rajguru College of Applied Sciences for Women in collaboration the Chapter conducted on 8 February 2022, a Distinguished Lecture on “Heterogeneous Integration for AI Architectures.” The speaker, Dr. Mukta G. Farooq, Distinguished Research Staff Member IBM Research, TJ Watson, Albany, New York, USA, gave a very insightful talk to more than 50 participants. Her lecture covered Artificial Intelligence (AI), Heterogeneous Inte-

gration, Through Silicon Via (TSV) technology and 3D integration.

The Department also organized its annual technical festival, TECHNEX-US on 7-8 February 2022. In addition to the technical activities and competitions enjoyed by 120 students and faculty members, four talks were given. The speakers who shared their expertise were, Mr. Tapes Jain and Mr. Navjot Singh of Sun Pharma, R&D Gurugram; Prof. Mridula Gupta of the Dept of Electronic Science, University of Delhi South Campus; and Dr. Saakshi Dhanekar of IIT Jodhpur.

A Distinguished Lecture on “Spintronics-Perspectives and Challenges” by Prof. Brajesh Kaushik of IIT Roorkee was organized for 10 February 2022. Prof. Kaushik explained that in the post-CMOS era, spintronics shall emerge as a potentially viable interdisciplinary field with credible technological perspectives. The talk was very engaging and was attended by over 55 IEEE and non-IEEE members.

The Department of Electronics of Maharaja Agrasen College in collaboration with the EDS Chapter conducted on 23 February 2022 a technical talk titled, “Development of Automated Characterization Systems for Electronic Devices.” The speaker Prof. Chetan J Panchal, Department

of Applied Physics of M.S. University of Baroda, Vadodara, India, explained the role of automated systems in characterization of electronic devices. This talk was attended by 97 participants including 10 IEEE members.

ED NIT Silchar Student Branch Chapter

—by T.R. Lenka

The Chapter in association with the IEEE Nanotechnology Council Chapter and the Department of Electronics and Communication Engineering, NIT Silchar, organized the International Conference on Micro/Nanoelectronics Devices, Circuits and Systems (MNDCS-2022), which was held 29-31 January.

Five distinguished plenary lectures were arranged with the following speakers:

- Prof. Subramanian S. Iyer of UCLA, USA
- Prof. Lan Fu of Australian National University, Australia
- Prof. Patrick Fay of University of Notre Dame, USA
- Prof. Nowshad Amin of Universiti Tenaga Nasional, Malaysia
- Prof. Merlyne De Souza of University of Sheffield, UK

In addition there were six keynote talks:



Ms. Samadrita Das, Student Chair (from left); Dr. S. K. Tripathy (Treasurer IEEE NTC); Prof. Rakesh Vaid, Speaker (middle); Dr. T. R. Lenka, Chapter Advisor; Mr. Rabin Paul, Student Vice-Chair; Ms. Jenifer Manta (Student Membership Coordinator); and EDS Student Members

- Dr. Jacopo Iannacci of Fondazione Bruno Kessler, Italy
- Prof. Sanket Goel of BITS Pilani Hyderabad campus
- Prof. Neerish Revaprasadu of University of Zululand, South Africa
- Prof. Luisa Petti of Free University of Bozen-Bolzano, Italy
- Prof. Sriram Krishnamoorthy of UCSB, USA
- Prof. P. Susthitha Menon of UKM, Malaysia

There were 47 oral presentations of research articles in the most relevant areas allied to the theme of the conference.

The chapter also organized a membership drive on 18 February 2022 and another technical talk on, "High-K MOS Capacitor: Fabrication and Characterization" by Prof. Rakesh Vaid of the Department of Electronics, University of Jammu, India, on 28 March 2022.

ED Meghand Saha Institute of Technology Student Branch Chapter

—by *Manas Chanda*

The student branch organized the 3rd IEEE International Conference on VLSI Device, Circuit and System during 26–27 February, 2022 (IEEE conference number 53788). The conference had a 43% paper and presentation acceptance rate, with the program providing 12 plenary and keynote talks.

The plenary speakers were:

- Dr. Saptarshi Das, Department of Engineering Science and Mechanics, Pennsylvania State University, USA
- Dr. Writam Banerjee, of Global-Foundries, Germany
- Prof. (Dr.) Benjamin Iñiguez, IEEE Fellow, University Rovira i Virgili, Spain
- Dr. Daniel Tomaszewski, Department of Microsystem Technology, Łukasiewicz Research Network – Institute of Microelectronics and Photonics, Poland

The Keynote Speakers were:

- Prof. (Dr.) Subir Kumar Sarkar of Jadavpur University, Kolkata
- Prof. (Dr.) Debashis De of Maulana Abul Kalam University of Technology
- Dr. Kanad Basu of the Department of Electrical and Computer Engineering, University of Texas at Dallas
- Prof. (Dr.) Ajit Kumar Panda, professor of NIST Berhampur
- Prof. (Dr.) Mridula Gupta of the Department of Electronic Science, University of Delhi South Campus, India
- Prof. (Dr.) Rajnish Sharma, Dean (Academic Affairs) of the Chitkara University Institute of Engineering and Technology
- Dr. Soumya Pandit, of the Institute of Radio Physics and Electronics, University of Calcutta
- Prof. (Dr.) Brajesh Kumar Kaushik of the Department of Electronics and Communication Engineering, IIT Roorkee, India

Michael Ong, Chair, IEEE Region 10 CQM Committee, also gave a small speech regarding the activities of IEEE Region 10 as well as how to maintain the quality and the control of a conference. The conference was a largely successful event, attended by more than 350 people, out of which 60 were IEEE members. All of

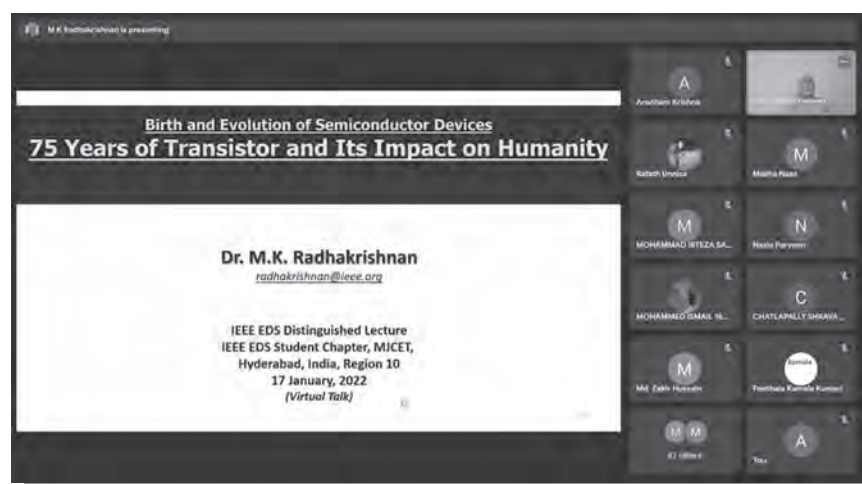
the presented papers were sent to IEEE Xplore for possible inclusion. Dr. Manash Chanda, Chairman, ED Kolkata Chapter, acted as General Chair under the patronage of Techno India Group.

ED Muffakhamjah College of Engineering & Technology Student Branch Chapter

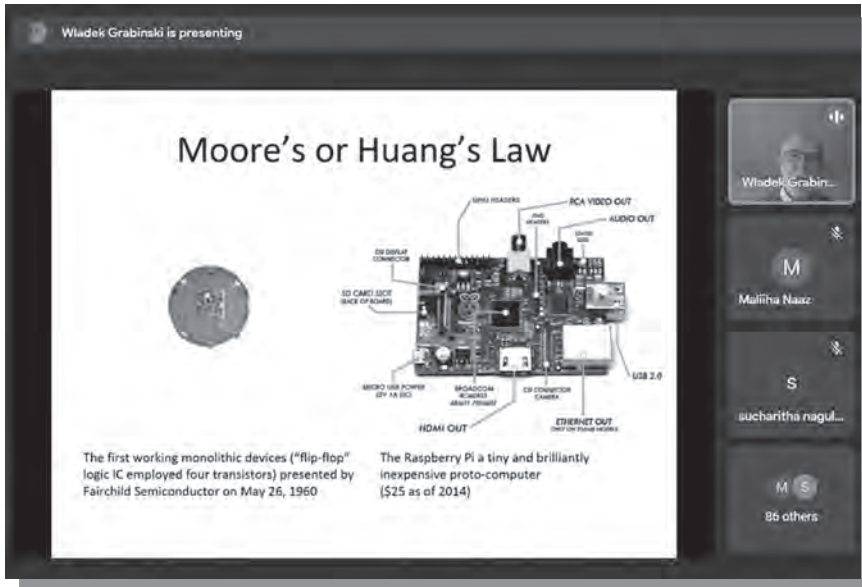
—by *Maliah Naaz*

The Chapter organized a five-day program during 17-21 January 2022, to celebrate the 75 years of the invention of transistors. The first event was a Distinguished Lecture "Birth And Evolution Of Semiconductor Devices: 75 Years of Transistors and Its Impact On Humanity." The speaker, Dr. M.K. Radhakrishnan, also formally inaugurated this newly formed chapter. The DL was attended by 80 participants including 50 IEEE members.

A webinar on the second day on "Preparation Strategies For Jobs In Electronics," was given by Dr. Mohammed Arifuddin Sohel. The webinar was attended by 80 students, of which 50 were IEEE members. On 19 January 2022, a quiz competition was held and based on the technical knowledge disseminated in the earlier lectures. There were 60 participants in the competition.



Dr. Radhakrishnan delivering a Distinguished Lecture "Birth and Evolution of Semiconductor Devices: 75 years of Transistor and its Impact on Humanity"



Dr. Wladek Grabinski presents an overview of Moore's Law



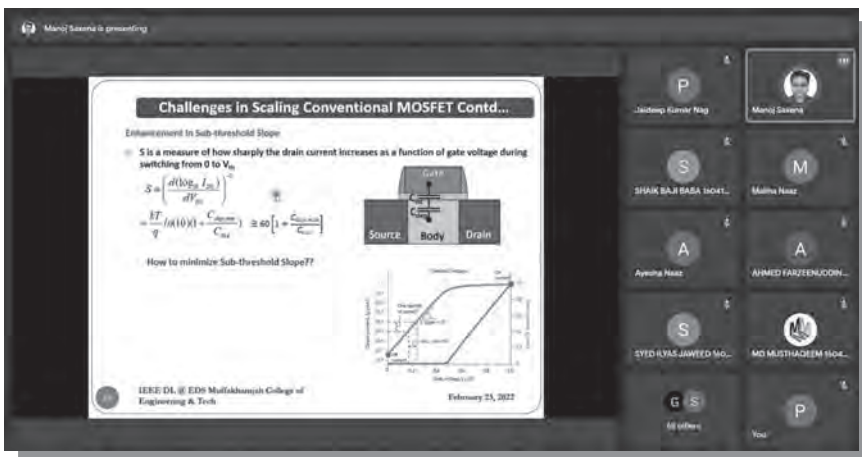
Technical talk on "Recent Trends in Biomedical instruments" by Mr. Suresh Chander Kapali

ED Panimalar Institute of Technology Student Branch Chapter —by Preethi Gandhi G. S.

The student branch chapter in association with the Technology Institution Innovation Council, conducted a technical talk on the topic, "Recent Trends in Biomedical Instrumentation" on 8 December 2021. The speaker was Mr. Suresh Chander Kapali, Assistant Professor of the Biomedical Instrumentation Department.

The chapter organized a "Mini Project Competition" for the students of Electronics and Communication Engineering Department of Panimalar Institute of Technology on 9 December 2021. More than 30 teams presented their ideas and explanations along with their prototypes. All teams targeted bringing solutions to the struggles which were faced in society. Among all the teams, the top 3 were selected as the winners and rewarded with certificates. Jury members gave their ideas and suggestions on how to improve all the projects. Student coordinators, Lohitha, Lakshana and Sowmiya organized the event under the guidance of Dr. Sathyapriya, Dr. Suganthi, Dr. Selvarani and Mrs. Sanjana.

The Chapter conducted a webinar on 14 December regarding "Intellectual Property Rights," to benefit students from various



Dr. Manoj Saxena giving the talk, "Fundamental Insights into Channel and Gate Engineered Double Gate Junction-Less Transistor"

The fourth day program began with a presentation by members of the chapter on the topic, "Understanding the different specifications of hardware devices and how they compare to older devices." The session was then followed by presentations from general students. On the concluding day, a webinar was held on, "Scientific Reading and Analysis," by Dr. Ayesha Naaz.

On 25 January 2022, the chapter organized a distinguished lecture talk on 'SPICE and Verilog-A Model-

ing using Open Source Tools', delivered by Dr. Wladek Grabinski. The speaker narrated the various open source tools for Verilog modeling. The session was interactive and informative.

Another distinguished lecture on, "Fundamental Insights into Channel and Gate Engineered Double Gate Junctionless Transistor," by Dr. Manoj Saxena was held on 23 February. The necessity of scaling, challenges of scaling and various structures of transistors were discussed in detail.



Mini Project Competition

ments. He also shared about NIOT and their motive. More than 100 participants from various educational institutions attended the event.

ED Uttar Pradesh Section Kanpur Chapter

—by Yogesh Chauhan and Shubham Sahay

The chapter organized a distinguished lecture on “Compute-in-Memory Designs: Trends and Prospects,” by Prof. Jaydeep Kulkarni of the University of Texas at Austin, USA.

The IEEE EDS Workshop on Devices and Circuits (WDC 2022) was also organized by the chapter and spanned 4 days, with more than 50 eminent speakers and 75 technical lectures by representatives of academia and industry, with an aim to boost the knowledge, initiate collaboration and expose the members to diverse research areas. Technical topics included, semiconductor material growth, device fabrication, digital, analog, and mixed-signal circuit design, RF circuit design, physics of semiconductors, compact modeling, SPICE and TCAD simulations, IC fabrication,



Webinar: “Virtual visit cum session on opportunity in oceanic engineering for electronics students—NIOT,” by Dr. Tata Sudhakar

institutions. The speaker, Dr. R. Valli gave the talk to create awareness on how to obtain patent rights. The student coordinators, Dasa Saranya and Sowmiya, organized the event under the guidance of Dr. MP. Chitra, and the student branch counselor, Mr. Arun M.

On 24 January, the Chapter conducted a webinar on “Industry 4.0 and Career Prospects,” by Dr. Sugandha Singh, who shared her views on the Internet of Things and cloud computing roles in future.

Another webinar on “Virtual visit cum session on opportunity in oceanic engineering for electronics students — NIOT,” was held 27 January 2022. The speaker, Dr. Tata Sudhakar, Scientist G, National Institute of Ocean Technology, spoke about Marine Instruments and classification of oceanographic instru-



Group Photograph from WDC 2022

atomistic simulations, RF and sub-THz measurements, optoelectronic and flexible electronics, non-invasive sensing techniques, MEMS and biosensors, neuromorphic computing and hardware security. The workshop was attended by more than 100 IEEE members and was perhaps the most successful in-person event hosted post-COVID19 pandemic.

For the complete program and list of speakers, visit the conference website at <https://home.iitk.ac.in/~chauhan/wdc2022.htm>.

ED Uttar Pradesh Section Nepal Chapter

—by *Rajendra Parajuli*

The chapter organized an online seminar on the topic, “Spinto Portronics of M²MⁿXYene Oxides,” on 28 January, 2022. The speaker was Dr. Deependra Parajuli, Research Centre for Applied Science and Technology & Tri-Chandra Multiple Campus, Tribhuvan University, Kathmandu, Nepal.

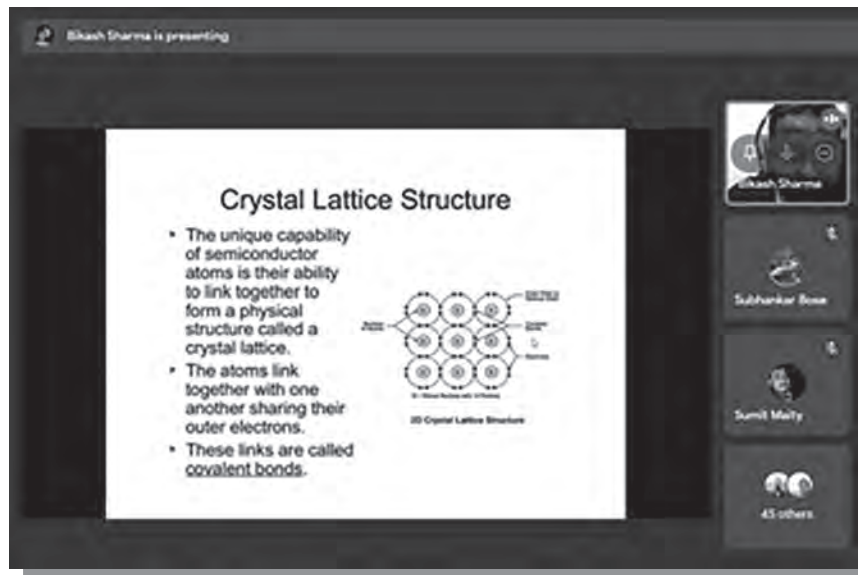
On 28 February, an EDS Distinguished Lecture by Simon Deleonibus, Chief Scientist/Directeur Scientifique Silicon Technologies, on “New routes and paradigms for Device Engineering in the Nanoelectronics and Nanosystems Era.”

An online lecture on “III-nitride nanowire, hetero-structures, molecular beam epitaxial, light-emitting diodes, optoelectronic devices,” was presented by Dr. Hieu P. T. Nguyen, Department of Electrical and Computer Engineering, New Jersey Institute of Technology, USA.

ED Kalyani Government Engineering College Student Branch Chapter

—by *Lokesh Maji and
Angsuman Sarkar*

The chapter in association with the Department of Electronics & Communication Engineering, Kalyani Government Engineering College, celebrated ‘Student’s Week’ as declared by the Govern-



Online presentation by Dr. Bikash Sharma

ment of West Bengal, India. During 1–7 January 2022, two seminars were held and well attended and enjoyed by the students through active participation:

- “Advances in Communication” by Dr. Somak Bhattacharya of IIT Benaras Hindu University on 5 January.
- “Nanoelectronics: The current and future of Electronics,” delivered by Dr. Bikash Sharma of Sikkim Manipal Institute of Technology on 6 January.

In association with the Department of Electronics and Communication Engineering, Kalyani Govt. Engineering College, two Distinguished Lectures were organized on 24 and 26 February, with more than 50 participants who gave positive feedback.

- Dr. Subir Kumar Sarkar, Professor of Jadavpur University lectured on “Microfluidic Biochips and their Applications”
- Dr. Chandan Kumar Sarkar, Retd. Professor of Jadavpur University, gave his talk on “Semiconductor Industry towards Tunnel FET”

~*Soumya Pandit, Editor*

Annual Meeting of the ED Japan Joint Chapter

—by *Toshiro Hiramoto and
Masaharu Kobayashi*

On 8 February 2022, the annual meeting of the Chapter was held via Webex. Prof. Toshiro Hiramoto, Japan Joint Chapter Chair, and Dr.



The Student Award ceremony held via Webex virtual platform on 8 February 2022

Nobuyuki Sugii, Vice Chair, gave a presentation reviewing 2021 activities and 2022 plans of the Chapter. After the meeting, the 2021 EDS Japan Joint Chapter Student Awards (VLSI & IEDM) were presented to three students, who made excellent presentations at the VLSI Symposia 2021 and IEDM 2021. The award win-

ners are posted on the Japan Joint Chapter's webpage; (http://www.ieee-jp.org/japancouncil/chapter/ED-15/ed15_award.htm).

After the annual meeting, the IEDM 2021 Report Session was held continually. Six members of the committee made presentations summarizing research topics and

the latest research trends in IEDM for more than seventy attendees. The session provided a good opportunity for the attendees to learn the latest technology trends, especially for those who were unable to attend the IEDM.

~ Alex Huo, Editor

EDS MEETINGS CALENDAR



THE COMPLETE EDS CALENDAR CAN BE FOUND AT OUR WEB SITE:
[HTTP://EDS.IEEE.ORG](http://eds.ieee.org). PLEASE VISIT.

<u>2022 IEEE Latin American Electron Devices Conference (LAEDC)</u>	04 July – 06 July 2022	Puebla, Mexico
<u>2022 29th International Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD)</u>	06 July – 09 July 2022	Kyoto, Japan
<u>The 29th edition of the IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)</u>	18 July – 20 July 2022	Singapore
<u>2022 IEEE International Flexible Electronics Technology Conference (IFETC)</u>	21 Aug – 25 Aug 2022	Qingdao, China
<u>2022 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)</u>	07 Sept – 09 Sept 2022	Granada, Spain
<u>2022 44th Annual EOS/ESD Symposium (EOS/ESD)</u>	19 Sept – 24 Sept 2022	Reno, NV USA

<u>2022 IEEE 48th European Solid State Circuits Conference (ESSCIRC) and IEEE 52nd European Solid-State Device Research Conference (ESSDERC)</u>	20 Sept – 23 Sept 2022	Milan, Italy
<u>2022 17th European Microwave Integrated Circuits Conference (EuMIC)</u>	26 Sept – 28 Sept 2022	Milan, Italy
<u>2022 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)</u>	16 Oct – 19 Oct 2022	Phoenix, AZ USA
<u>2022 14th International Conference on Advanced Semiconductor Devices and Microsystems (ASDAM)</u>	24 Oct – 27 Oct 2022	Smolenice, Slovakia
<u>2022 International EOS/ESD Symposium on Design and System (IEDS)</u>	09 Nov – 11 Nov 2022	Chengdu, China
<u>2022 International Electron Devices Meeting (IEDM)</u>	03 Dec – 08 Dec 2022	San Francisco, CA USA
<u>2022 IEEE 50th Semiconductor Interface Specialists Conference (SISC)</u>	08 Dec – 11 Dec 2022	San Diego, CA USA



EDS STRATEGIC PLANNING UPDATE

On behalf of your EDS community, EDS leadership and delegates descended upon Hawaii (June 10-11) for a groundbreaking 2-day strategic planning event in prelude to the Mid-Year EDS Board of Governors (BoG) meeting and the IEEE Symposium on VLSI Technology & Circuits. Everyone came with dedication and commitment that even exceeded expectations with a collective burning desire to propel EDS forward in the years to come. Most specific outcomes will be disclosed publicly after vetting through EDS membership that will include two live webinars on July 20th with favorable times to Europe and Asia, respectively. But we can reveal our adopted EDS Core Values that were affirmed by the EDS BoG [trustful, respectful, inclusive, ethical, and open] and which were guiding principles throughout the deliberations and discussions. Key performance indicators (KPI) were proposed and refined that will lead to an EDS Dashboard, tracking our EDS progress, holding our community accountable for positive change. This will be key for an iterative deployment plan, baking in a feedback loop. We hope that our recommitment will attract a new generation of volunteers to get more involved and make EDS the place to be for the field of electron devices benefitting humanity.

Ravi Todi, EDS President

Doug Verret, EDS Strategic Directions Vice President

Paul Berger, EDS Future Directions AdHoc Committee Chair