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Technical Briefs

Marvels of Microelectronic Technology: The 1T-1C Dynamic Random Access Memory, from a Groundbreaking Idea to a Business Benchmark

by Simon Deleonibus, Past Chief Scientist, CEA, LETI

In this issue, we report on one of the flagship Marvels of Microelectronic Technology, which has marked the history of microelectronics in the past 50 years: the 1 Transistor –1 Capacitor Dynamic Random Access Memory (1T1C DRAM). DRAMs have driven and accompanied Moore's Law through Metal Oxide Semiconductor Field Effect Transistor (MOSFET) integrated circuit scaling. They have been and still are a benchmark for the microelectronics industry: they continue to share their leadership with advanced microprocessors, SOCs and nonvolatile memories. DRAM fostered technological progress that was necessary to introduce new materials and revise process integration. In this article, R.H. Dennard, H. Sunami, M. Koyanagi and K. Itoh (Figure 1) accepted to remind us the pioneering times when 1T1C DRAM came out of its cradle.

DRAM Invention and First Developments

The groundbreaking ideas proposed by Robert Dennard, IEEE Fellow, IBM Fellow, to push microelectronics progress thanks to the 1T1C DRAM and MOSFET integrated circuit scaling have already been widely commented and many times awarded. The circumstances giving birth to the idea of MOSFET scaling were reported in the IEEE EDS Newsletter July 2019 issue. In this issue (October 2019), we will report the advent of 1T1C DRAM. Robert Dennard kindly accepted to remind us a few important facts. Some of them were also reported at

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Marvels of Microelectronic Technology: The 1T–1C Dynamic Random Access Memory, from a Groundbreaking Idea to a Business Benchmark

(continued from page 1)

his 2013 Kyoto Prize Award ceremony as well as in journals/magazines papers [1], [2].

In the time period of Dennard's invention (mid-1960s), IBM mainframe computers were equipped with a maximum of 1 MB magnetic-core memory capacity. The access time was in the range of 1–2 microseconds, and power dissipation was about 40 kW. Those features are orders of magnitude larger than the ones we are used to on our today's handheld mobile phones! In 1971, the first semiconductor memory equipped IBM mainframe computers were based on 128 bit/chip bipolar design [2]. The six transistor (6T) memory cell (2 cross coupled flip flops and 2 bitlines access transistors) was the standard benchmark reference [3]. To compensate the lack of performance of 6T MOSFET arrays, Pleshko and Terman proposed to interface them with bipolar support circuits in order to drive large interconnect loads with low impedance devices [4]. n-MOSFET design started to be convincing by its potential lower cost and scalability, coming together with a speed increase and reduced power consumption, which narrowed the gap with bipolar Figures [5]."

Dennard was struck by an unexpected fact, where he states: *"One day in late 1966 an important event in my life occurred. During the day I attended a large IBM Research conference where various projects were presented. … I was very impressed by a description of a proposed thin-film magnetic memory, which was projecting hundreds of thousands of bits in a 25 cm wide memory board… they had a very simple memory cell, just a small square of magnetic material at the intersection of two etched copper lines. I was inspired to find something that simple for the technology we were developing."* [1], [2]

Figure 1 From left to right: (Standing) Hideo Sunami and Mitsumasa Koyanagi (Sitting) Kiyoo Itoh and Robert Dennard at the 2006 IEEE Award Ceremony. Itoh, Sunami, and Koyanagi were honored with the 2006 IEEE Jun-Ichi Nishizawa Medal. (Front cover of IEEE SSC Newsletter, Winter 2008, vol. 13, n°.1)

Such a simple idea has been so powerful in the long term and is still a source of inspiration nowadays to those who build cross bar arrays or are ever looking for the Universal Memory. *"I found that an MOS transistor in series with each capacitor could be used as a switch to connect the capacitor to a data line briefly to charge or discharge it to write a data bit, represented by a positive voltage level, +V, or a zero voltage level on the bit line. The transistor is turned on and off by a control signal on a word line which allows selecting a given capacitor from many others for receiving the data on that bit line."* [1], [2] The basic idea of 1T1C DRAM was born that same day in late 1966. Dennard restlessly kept on working for several weeks on various configurations. He finally realized that the stored charge could be written and read through the same nonlinear device which is the access transistor, that would create a small signal on the bit line: *"The cell had been reduced to a single transistor and a capacitor at the intersection of two access lines* [1], [6]. *I was satisfied that this was as close to my goal as possible, and offered a great reduction in complexity compared to the six-transistor memory cell."* (Figure 2 Left)

Nevertheless, MOSFET technology needed to prove its capability because the mainly used p-channels transistor speed was lower than for the bipolar competitor. Moreover, MOSFETs' characteristics, based on interface inversion, were still not well controlled. In that context, Intel realized the first silicon gate 3 p-channel transistor DRAM in 1970 [7]. The first proposal of 2 kbits "One device RAM chip" design, based on MOSFET technology, was published in 1971 [8]. 4 kbit chips became commercially available in the mid 1970s.

Besides the technology, further development consisted in layout

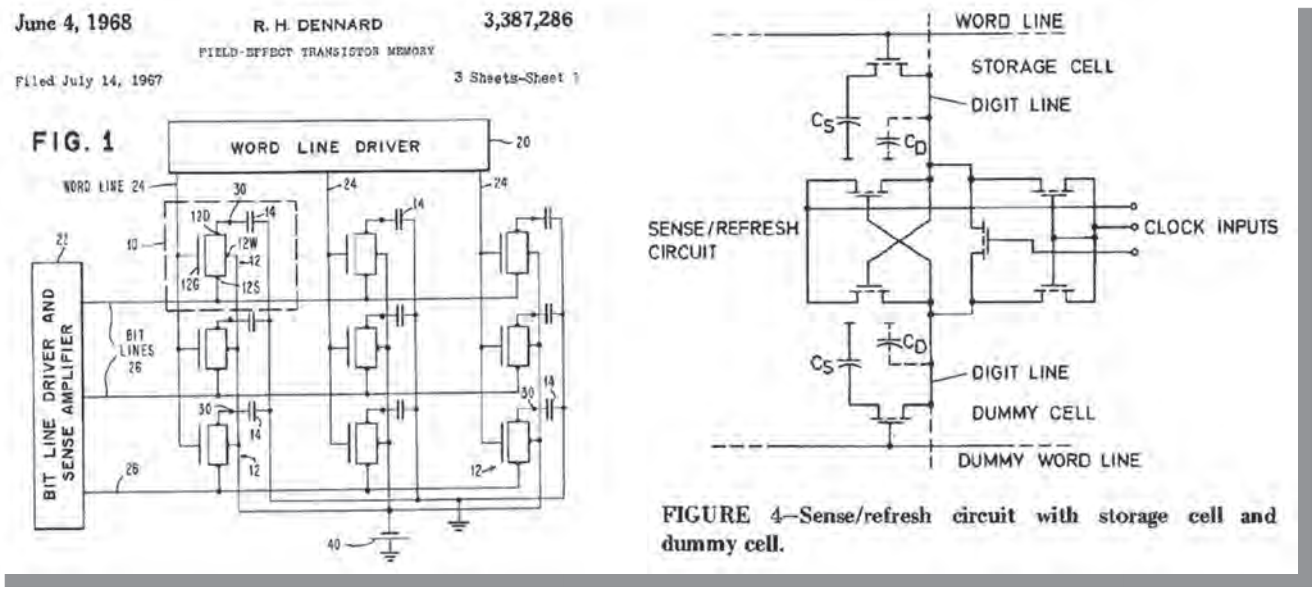

Figure 2 (Left) Detail from R.H. Dennard's 1st Patent of 1T1C DRAM [6] ; (Right) Open Bitline 1T1C DRAM array architecture by K.U. Stein et al. presented at 1972 IEEE ISSCC [11]. The sense-and-refresh circuit is shared by 2 bitlines both connected to a large number of DRAM storage and dummy memory cells (first pair only represented) through two latch nodes

optimization to pack up as much as possible the bit cell, possibly including self-aligned contacts and two poly layers, to realize both a transistor gate and a capacitance plate [9]. At the chip level, innovations were guided by the necessity to match bitlines and wordlines pitches, including the row and column decoders layout, with the bit cell arrays without sacrificing the performance and noise Figures [9]. The small signals delivered by the bitcell and the necessity to restore them requested innovations in the design of the sense amplifiers [2]. Dennard reminds how critical it was to make DRAM products design manufacturable from the first idea of latch based sense amplifier in 1970 [10] and the implementation of the Open Bitline architecture using a cross-coupled differential sense amplifier based on a combination of each bitcell with a dummy cell, first presented at the 1972 ISSCC [11] (Figure 2 Right), refined in its "double cross coupled" version in IBM's 64 kBit DRAM in 1977 [12]. However, the solution to noise problems, potentially introduced by imbalances in the arrays, was brought by the Folded Bitline architecture invented by Itoh [13] in 1974 (see more hereunder "Folded Bitline and revised Open Bitline architectures" section). At this early stage of development, the necessity to introduce redundancy in order to maximize production yield appeared and was reported by IBM and Bell Laboratories [14], [15].

In the early days, Dennard's approach received also criticism, including internally at IBM, despite the fact that the architecture was considered as the simplest for a memory cell. As an example, we report a comment on 1T1C DRAM drawbacks "*The cell has a number of drawbacks… the readout is destructive, the stored charge distributes between the cell and bit line capacitances and the writing speed is limited by the information storage capacitor which must be made large enough to yield a reasonable sense charge*" [5]. However, Dennard explains that such a specific situation can be managed: "*A distinctive characteristic of this memory cell is that a small leakage current from this n-doped region to the p-type silicon substrate discharges the capacitor in a fraction of a second. This gives rise to the name "dynamic" since the data is only stored temporarily. To preserve the data it must be refreshed by reading it out and writing it back into each cell at certain intervals. Fortunately, the speed of this memory scheme allows more than a hundred million read or write operations per second and only a small percentage of these are needed for refreshing the data. Thus, this scheme became known as dynamic RAM, and commonly called DRAM." [1]*

Once the 1T1C concept was proven, competition started raging to scale down the memory devices driven by performance and density increase. At Hitachi, another main frame computer company, two concepts came out almost concomitantly, driven by two talented imaginative engineers, IEEE Fellows and Professors Hideo Sunami and Mitsumasa Koyanagi, as original solutions to respond to the scaling challenge. One was using capacitors embedded into trenches etched in the substrate and the second one stacked a capacitor on top of the addressing (write/refresh, sense/erase,) devices. These approaches were among the first attempts to exploit the 3rd-Dimension to improve microelectronics circuit density and were going to become benchmark circuits

for technology scaling, but their inventors probably were not conscious of it, at the time.

Trench Capacitor DRAM

Hideo Sunami proposed the trench capacitor approach. He was inspired by a combination of Dennard's 1T1C approach, his background on electronic components engineering and his youth passion for radio engineering. He entered Tohoku University in 1963 and joined Hitachi Central Research Laboratory (CRL) in 1969 after his graduation from Prof. Junichi Nishizawa's laboratory in 1969.

Hideo Sunami was very much involved in CCD research at Hitachi and that naturally led him to be interested in the DRAM because CCD were very demanding in terms of silicon engineering and more precisely gettering, doping and materials purity control. He proposed to make the capacitor of the 1T1C DRAM by etching a trench capacitor into silicon. Sunami thought that by adjusting the trench depth the capacitance value could be increased without increasing the capacitor footprint [16] (Figure 3 Left). Sunami told us: *"At an early stage of my junior-high school age I fell in love with two hobbies. One was collecting butterflies and the other was hand making of short-wave radio receivers and transmitters. Then I have made myself to be very familiar to electronic components such as vacuum tubes, transistors, resistors, capacitors, etc. by the time I entered Tohoku University in 1963."*

Hitachi CRL offered him a leave opportunity at Stanford University. His imagination was struck by marvels achieved in a completely different area while he attended a conference: "*In the conference I was awfully shocked by some presentation where truly vertical trench of aspect ratio of almost 5 was formed on (110)-oriented silicon surface. In those days, truly vertical trench could not be formed on silicon surface but spherical crater-like hollow was formed even by using plasma etching.*" He knew from

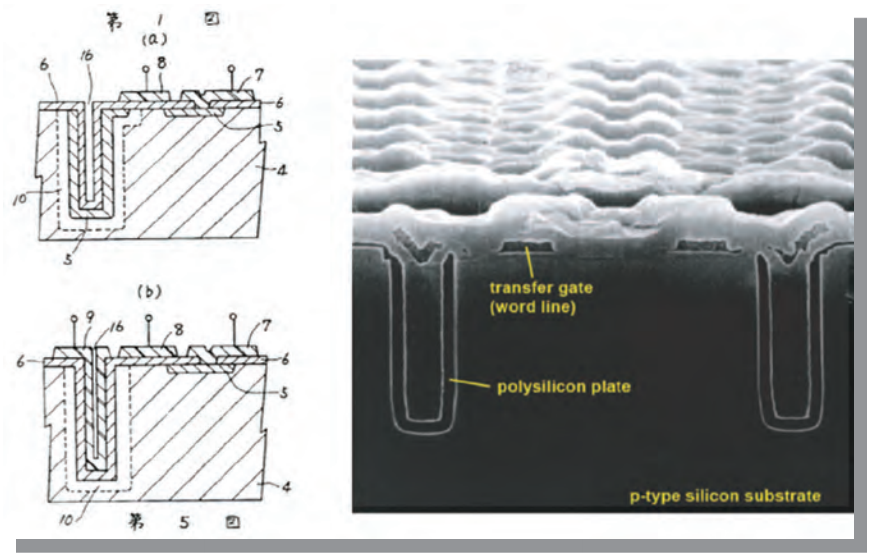

Figure 3 (Left) Trench Capacitor DRAM patent H. Sunami and S. Nishimatsu, Japanese patent application, Tokugansho 50-53883, 1975 [16]; (Right) SEM cross section of first 1-Mbit Trench Capacitor cell DRAM, presented at 1982 IEDM by Sunami et al. [18]

his experience on CCD that surface characterization was a major tool to master the integrity and reliability of silicon devices.

Sunami continues: *"On the other hand, I was hearing that one-device and one-capacitor DRAM cell had been recently invented. Despite the on-going research on surface characterization at Stanford, I got an inspiration of a first trench capacitor cell concept based on a combination of that DRAM cell and a cylindrical trimmer condenser used in radio-frequency transmitter. I requested my department boss at CRL to send me abroad a patent application form. His answer was negative. He told me: "You should concentrate on on-going research." Therefore, the first trench-capacitor cell patent was applied in 1975, several months after I left Stanford. Since the patent was not classified to be excellent, it was not applied to US!"*

In the late 1970s and 1980s, Hitachi became one of the major actors on the DRAM business by first introducing Trench capacitor DRAM. Hitachi's 1-Mb DRAM was first presented at 1984, ISSCC [17] featuring a Corrugated Cell Structure that was first reported at 1982 IEDM [18] (Figure 3 Right) and received the IEEE Paul Rappaport Award in 1984 [19].

Stacked Capacitor DRAM Cell

Another challenging approach to the scaling of DRAMs was the 1T1C cell using a so called "Stacked Capacitor." While the storage capacitance decreases by following their linear scaling, the number of stored charges decreases. The stored charge can thus incur severe variations. Mitsumasa Koyanagi points out: "*The number of signal charges stored in the storage capacitor has to be maintained at almost a constant, or can be only slightly reduced, as the memory cell size is scaled down. However, MOS capacitor value—and hence the amount of signal charges—is significantly reduced as the memory cell size is reduced, even if the capacitor oxide thickness is scaled-down. Therefore, I forecasted in 1975 that the 1-T cell with a two-dimensional (2D) structure using a planar MOS capacitor eventually would encounter a scaling-down limitation because it was not possible to reduce the MOS capacitor area according to the scaling theory.*" [20] The second reason to find an alternative was to reduce the influence of minority carriers generated in the

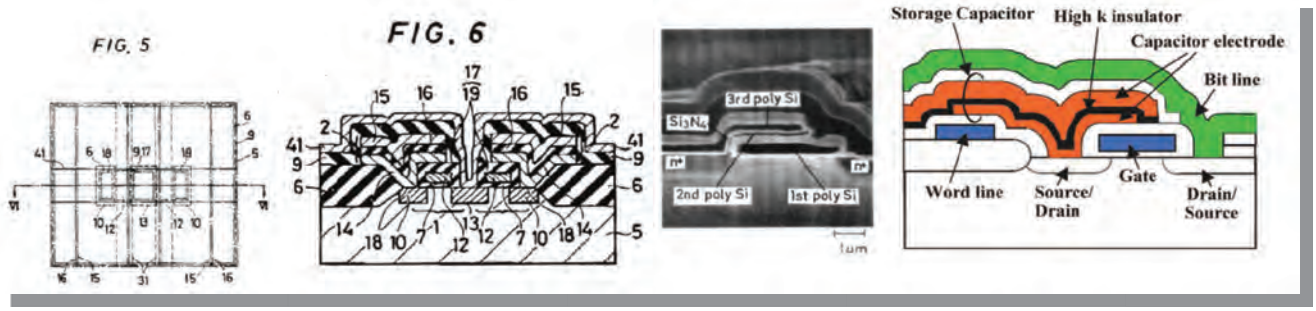

Figure 4 (Left) Capacitor over Bitline Basic principle of stacked capacitor cell DRAM [22]; (Middle) 3 μm NMOS Stacked capacitor DRAM presented by M. Koyanagi et al. at IEDM 1978 [21]; (Right) Schematic cross-section of Capacitor Over Bitline [20]

silicon substrate on the storage node charges, degrading thus retention time and soft error immunity.

Using a vertical capacitor (exploitation of the 3rd-dimension) would give more flexibility to fix the capacitance value. If the vertical capacitor is located far from the silicon substrate, then the degradation of retention and soft errors immunity by the minority carriers is dramatically reduced.

"*An inversion layer capacitance and a depletion layer capacitance are connected with the gate oxide capacitance in series in the MOS capacitor. The charges in the inversion layer and the depletion layer are easily affected by the minority carriers, which are thermally or optically generated or generated by the irradiation of energetic particles in a silicon substrate.*"

Koyanagi had a good knowledge of MOS interface physics. "*In my Ph.D. research during 1971–1974 [3], I had commented on the silicon surface and the inversion layer in MOS structures. To evaluate the electrical properties of the interface states and the inversion layer, I myself built an impedance analyzer with the frequency range of 0.01 Hz to 100 MHz. I examined various kinds of capacitors, including high-k (high dielectric constant) capacitors as a reference capacitor of this impedance analyzer. Eventually, I made a vacuum capacitor for a reference capacitor in which fin-type capacitor electrodes were encapsulated in a vacuum container.*"

Koyanagi also used a Ta_2O_5 film as a capacitor insulator for the first time [21]. Ta_2O_5 has a dielectric constant five or six times larger than that of SiO_2. Therefore, the storage capacitance can greatly be increased, although the leakage current is larger than for SiO_2 or Si_3N_4 (for the same thickness) because of a lower bandgap value.

Koyanagi proposed the Capacitor Over Bitline (COB) concept which laid out the capacitor structure on top of the access transistor [21], [22], [23] (Figure 4). Many ways have been explored to increase the capacitance value per unit area by playing with the actual capacitance area spread in 3D either by wrapping multiple electrodes (Fin type capacitors , 1st publication by Fujitsu in 1988 [24]), increasing the plate electrode area with large hemispherical grains polysilicon(1st publication by NEC in 1990 [25]), or a cylindrical capacitor (1st publication in 1989 by Mitsubishi [26]) which have been extended to Multigigabit DRAMs till nowadays.

The concept of the COB-type stacked capacitor cell—that various kinds of materials can be stacked on the switching transistor using a lower temperature process—has been carried on in new memories with a three-dimensional structure such as Fe-RAM (Ferroelectric RAM), P-RAM (Phase Change RAM), R-RAM (Resistive RAM) and M-RAM (Magnetic RAM). [20]

Further on Koyanagi spent much of his energy on the generalization of 3D stacking. His work with his team at Tohoku University is recognized as a reference in the packaging and 3D community. By intensively using wafer bonding and Through Silicon Vias (TSV), he has been instrumental in creating a way to give a new breath to Moore's law. He did that not only to increase DRAM capacity but also to cointegrate heterogeneously different types of circuits [27].

Soft Errors and the "DRAM Midlife Crisis"

Once the DRAM circuits complexity and production volume increased, stochastic and statistical effects started to appear such as Soft Errors. In 1979, two research groups at Intel [28] and Bell Laboratories [29] revealed that 16kbit DRAMs could suffer from transient error due to bombardment by alpha-particles and subsequent excess minority carrier generation in the substrate. Dennard points out: "*The alpha particles were identified as coming from radioactive impurities in the materials of the hermetically-sealed packages...an analysis of the possible soft-error rate due to cosmic rays showed that this source could be significant. Personally, I felt very responsible because of my early role with dynamic RAM's and because I failed to anticipate the problem.*" [1] A good understanding required building a model based on a Monte Carlo approach developed by G Sai-Halasz. A solution based on a self-aligned buried n-grid to protect against radiation-induced charge collection was proposed [30] (Figure 5 Left): "*It was shown that error rates would rise in response to scaling to smaller dimensions, but that design changes including error-correction*

techniques would contain the problem. The midlife crisis was over."

In our exchanges, Dennard further commented: "*IBM was also careful to replace radioactive lead and other sources of alpha-particle emissions in order to limit soft-error rates (SER). IBM chose trenches to avoid disrupting our back end of line (BEOL) process with a tall stacked capacitor. The designers wanted a big memory-cell capacitor to support large arrays (long bit lines) and we knew how to etch really deep trenches.*"

Within Hitachi, the concern on SER, besides the caution taken on packaging, led to make drastic choices on the architecture. The different approaches of Trench DRAM and Stacked capacitor (STC) were shown to behave quite differently with respect to the soft errors. Sunami comments *"Hitachi was one of the biggest main frame makers in the world at that time, and was as much concerned like IBM, the huge giant. The computer division of Hitachi became very nervous to degraded SER of which home-made DRAM provided."* He considers that DRAM in consumer equipment market did not require main-frame level SER. Consequently, many manufacturers such as NEC, Toshiba, IBM, TI, Siemens shipped 1-Mbit DRAM integrating trench capacitors. "*Some of them applied modified trench capacitors having improved SER.*" The idea was based on the collection of minority carriers through a highly conductive buried electrode. Examples such as the use of self-aligned buried grids [30], p+ substrate or n+ sheath plates under the storage capacitor have been used [31], [32], [33], as well, to control cell to cell leakage current.

Koyanagi showed to the DRAM community in Japan the results that a soft error rate could be dramatically reduced by almost three orders of magnitude by employing a Stacked Capacitor Cell as compared to a planar capacitor cell. This very important result was mentioned in his IEEE TED paper in 1980 [34]. Koyanagi comments: "*My boss in Hitachi at that time cut the Figure of soft error characteristics from the 1980 TED paper. He said that data of STC soft error was very important internally in Hitachi and hence data indicating the superior immunity to soft error of STC should be confidential for outside.*" Koyanagi obtained permission for publication on the evidence of the superiority of STC on soft error immunity only in a Japanese paper [35]. The Figure demonstrating such a superiority appeared in IEEE SSCS News in 2008 [20] (Figure 5 Right). Koyanagi concludes: *"Today, the three major DRAM companies are Samsung, Hynix and Micron. These three DRAM companies have been using the Stacked Capacitor Cell from 4 Mbit DRAM to 8 Gbit DRAM and maybe 16 Gbit DRAM."*

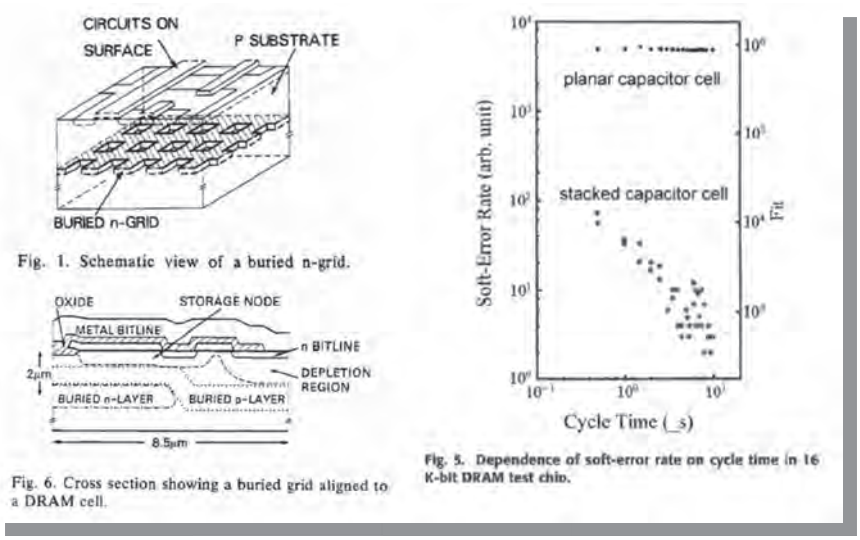

Figure 5 (Left) Self aligned buried n-grid protection for soft error immunity, as proposed by Wordemann et al. [30]; (Right) Dependence of Soft Error Rate on 16 kDRAM cycle time. Comparison of Stacked Capacitor Cell and unprotected Planar Capacitor Cell [20]

Folded Bitline and Revised Open Bitline Architectures

Another benchmark innovation for DRAM success, that had become an industry standard from the 1980s to the mid-2000s, is the invention of the Folded Bitline (Folded BL) arrangement at the end of 1974 by IEEE Fellow Kiyoo Itoh of Hitachi CRL [13]. The first demonstration was made by a presentation of a 64-kb DRAM at ISSCC in Feb. 1980 [36].

The Folded BL uses a pair of balanced BLs running close to one another and are parallel on the same conductor, equalizing and thus cancelling noise voltages coupled to the pair, caused by voltage bounces in an array, with the differential amplifier [37] (Figure 6) . Moreover, a metal BL reduced soft-error noise caused by diffused-BL structures of the Open BL. Although in principle the Open BL realizes a smaller cell size of $6F^2$ (F is feature size) than the Folded BL ($8F^2$), the much larger cell compensates the noise voltages with a larger signal voltage. Itoh comments: "*Unfortunately, a simple single metal-layer 5-μm process available at that time could not suppress the noise voltages sufficiently. Consequently, the 64-kb DRAM enabled stable operations despite a drastic reduction of the operation voltage V_{DD} to a TTL-compatible 5 V from 12 V for the 16-kb DRAM… In the cradle of DRAM, no one knew solutions for stable operations under array noise and soft errors and thus at the beginning I could not convince top managers on the importance of the innovation.*" Since that time until the mid-2000s, the Folded-BL was adopted for nearly all DRAM chips produced. In 2002, however, based on in-depth analysis of array noise,

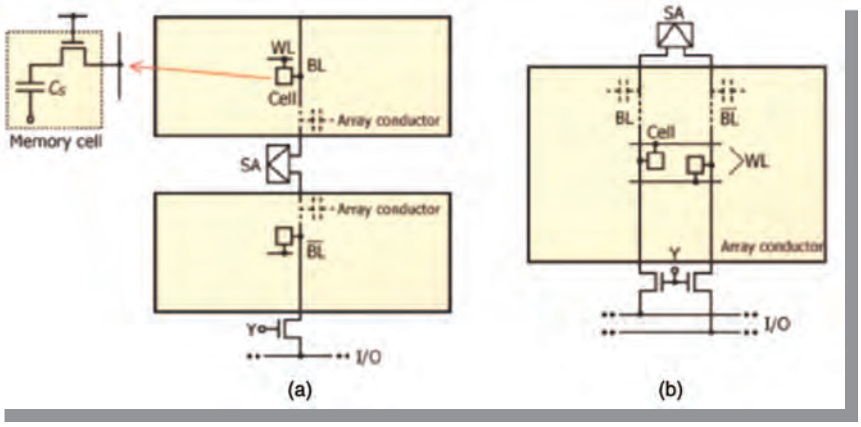

Figure 6 Comparisons of [37]: (a) Open Bitline arrangement and (b) Folded-Bitline arrangement. SA: Sense amplifier; Y; Column select-line; I/O: Common data-in- and data-out-lines-see also [13]

Itoh's team [38] revealed the possible revival of the open-BL with $6F^2$, if an advanced vertical capacitor cell for a larger cell signal voltage and a three-level metal layer process for reduced voltage bounces were used. Triggered by the 2002 JSSC paper [38], major DRAM players such as Samsung, SK Hynix and Micron have gradually changed the cell to the $6F^2$ Open BL, starting with 512-Mb DRAMs in 2005 [39], reaching nowadays 10-nm-class 16-Gb DRAMs [40]. Stacked modules with 8 single-16-Gb-DRAM chips [41] contribute to high density servers and mobile applications. Itoh underlines: "*The addition of an on-chip voltage down-converter to protect internal miniaturized devices [42] and reduction circuits of the ever-larger subthreshold-leakage current [43], are also key contributors to DRAM success.*"

The simplicity of Dennard's 1T-1C DRAM principle has kept it unbeaten by any other solution and certainly qualifies it a Marvel of Microelectronic Technologies. A lot of technical progress has been achieved worldwide, since its invention, year after year: Dennard, Sunami, Koyanagi and Itoh are certainly key persons who made it happen. Future prospect to reach a smallest footprint of $4F^2$ have already been highlighted, thanks to a vertically stacked access transistor and a high aspect ratio capacitor based cell [44], featuring a revised Open BL architecture.

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Highlights of the 2019 IEEE Photovoltaic Specialists Conference

By Ned Ekins-Daukes and Sarah Kurtz

The 46th international 2019 IEEE Photovoltaic Specialists Conference (PVSC-46), was held June 16–21, 2019, at the Sheraton Grand Hotel in Chicago, Illinois. The PVSC is held annually and is the leading international conference on PV science and technology and one of the flagship conferences of IEEE sponsored by the Electron Devices Society. The conference hosted 1,150 attendees from 46 different countries: 56% from the USA, 7% from Japan, 5% from Germany, 4% from Australia, 3% from China and the remaining 25% from other nations. During the conference, 885 presentations were delivered.

The *William R. Cherry Award* is the highest award presented at the conference and was conferred to Harry Atwater (CalTech, USA) in recognition of his creative work since 1988, contributing to world-record GaAs cell efficiencies. His presentation highlighted the importance of the optical design and internal radiative

efficiency of solar cells, introducing a luminescent concentrator GaInP cell integrated above a silicon cell. He co-founded Alta Devices and ETC Solar.

The *Young Professional Award* was renamed this year after the late Stuart R. Wenham. This year the award went to Zachary Holman for his research at Arizona State University. He gave a presentation "Advancements in Silicon Heterojunction Solar Cells," providing a cost analysis of tandem cells. He discussed examples such as III-V on silicon, perovskite on silicon and spectrum splitting configurations.

Best Student Paper Awards and Poster Awards were issued in various categories.

Outreach

The PVSC High School Competition hosted nine teams (32 students). Their solar energy research projects were supported by teacher-facilitators from their local schools as well as mentors from Arizona State University, University of New Mexico, and Purdue. Thanks to a generous grant from the NSF, 12 high school scholars from Arizona were able to travel to the conference to participate in person in the Monday-afternoon poster session with their Chicago-area peers. This cross-age event helped create a sense of belonging for young aspiring engineers, communicating that we are all photovoltaics scholars, different in level, not type; all agreed that the event was a resounding success!

Keynote

The opening keynote was given by Dr. Ron Sinton on "The Path Towards a Major Utility Commitment for 100% Carbon-Free Electricity." Dr. Sinton explained how one of the largest electricity utility companies in the USA, Xcel, has pledged to become carbon-free by 2050. While the transition is motivated by an appetite from consumers for clean electricity, the transition is enabled by the competitive costs of wind and solar electricity; now cheaper than the marginal cost of coal in many locations. Additionally, Xcel makes the case that investment in solar and wind is advantageous for Xcel's investors, suggesting the beginning of a trend where investor-owned utilities may become primary drivers of solar expansion.

Special Session—Understanding the Value of Efficiency in Mainstream PV Markets

Kelsey Horowitz presented a comprehensive argument that solar power conversion efficiency has a premium in space-constrained applications, e.g. rooftop generation in situations with high electrical demand, such as a household with an electric vehicle. Industry representatives shared a range of viewpoints, noting that note everyone is looking for the same product and sharing maps of where Winner technologies, Loser technologies, Niche products and Super Winners exist.

Conference participants, Richard King, Thorsten Trupke and Ron Sinton congratulate the new Cherry Award winner, Harry Atwater, second from right

Conference Highlights

The PVSC-46's Technical Program included 12 areas covering cutting-edge developments in PV technology, ranging from fundamentals to applications, with an emphasis on material science, devices, PV systems, solar resources and policy. At present, the technical program can be easily digitally explored at https://www.ieee-pvsc.org/ePVSC/mobile/ with papers available to conference attendees. The proceedings will be available in September. To give readers insights on the conference's vast program, this Technical Brief provides an overview of the conference highlights by area.

Area 1 *Fundamentals and New Concepts for Future Technologies*

The Area 1 Plenary was given by Tom Markvart from the University of Southampton, UK, who used thermodynamics to explain the operation of a solar cell and the way the chemical potential of emitted photons is recovered through photon recycling. Recognizing that a significant fraction of the incident energy is lost to carrier thermalization, Tom outlined a thermoelectric approach for the implementation of a hot carrier solar cell, in which SQ efficiency could be surpassed. Jeronimo Buencuerpo from NREL presented ultrathin III-V solar cells using photonic crystals, demonstrating that a 2D photonic crystal on front and rear of 300 nm thin III-V cells enables absorption close to the Lambertian limit. Jacob Krich presented a figure

of merit for intermediate band absorbers to predict when it is worthwhile to make devices. The figure of merit well described devices using a new open source device model, Simudo, available at github.com/simudo/simudo. Daisy Xia described research on laser power conversion at 1310 nm, predicting that a 20 junction photonic power converters would achieve 13.7 V with a power conversion efficiency of 60%. Ian Sellers presented exciting results about hot carrier effects in thin bulk systems without nanostructuring. He demonstrated an InGaAs/AlInAs system, with an extrapolated V_{oc} of 1.375 V, limited by the L valley of the conduction band rather than the conduction band minimum. Finally, Rob Patterson presented a computational study to screen new candidate materials for the top cell for a silicon tandem cell, such as CuZnSI, $CuZn_3S_3I$ and $CuZnSI_3$.

Raffi Garabedian gives plenary lecture for Area 2

Area 2 *Chalcogenide Thin Film Solar Cells*

The Area 2 plenary was given by Raffi Garabedian, the CTO of First Solar. He summarized the transformation over the past decade in PV electricity generation, not just achieving grid parity but actually now being the cheapest source of energy; in some locations being cheaper than the marginal cost of a coal power plant. He emphasized that despite concerns from a decade ago, solar plants are now actually adding to grid stability.

Motoshi Nakamura from Solar Frontier presented record breaking results in "Cd-free Cu(In,Ga) $(Se,S)_2$ thin-film solar cell setting a new record efficiency of 23.35%." Key were a CsF treatment and careful optimisation of the bandgap profile obtained by controlling Ga/(Ga+In) and S/(S+Se) ratios. Mahisha Amarasinghe from the University of Illinois reported that high group-V doping > 10^{16} cm^{-3} in CdSeTe thin films could be achieved by vapor transport deposition. An extensive study of KF, K, RbF, and Rb post-deposition treatments on (AgCu)(InGa) Se_2 solar cells by M. Edoff showed a low V_{oc} deficit of 0.4 V. Thomas Fiducia presented 3D imaging of selenium distributions in high efficiency Se-graded CdTe solar cells, combining high-resolution cathodo-luminescence images with elemental distributions to show a selenium deficit at grain boundaries in the regions with high selenium concentrations near the cell top surface and a surplus in bulk regions, induced by the diffusion processes during $CdCl_2$ treatment of CdSeTe/CdTe bilayers. Li et al., Danielson et al., and Yan et al. described innovations in the electron and hole contacts in CdTe solar cells, including air-free $CdCl_2$ treatments that prevent large conduction band offsets at the CdTe/MZO interface, a 30X increase in PL intensity compared to reference cells.

Area 3 *Multijunction and Concentrator Technologies*

Ryan France from NREL announced a 6-junction inverted metamorphic solar cell with a record efficiency of 47.1% at a concentration of 144 suns AM1.5D and 39.2% under the AM1.5G spectrum. Relatedly, Manuel Hinojosa further elucidated the behavior of Zn diffusion at sub-cell interfaces and the role that point defects play in affecting dopant diffusion from tunnel junctions and M. Steiner described improvements made to the AlGaInP top junction. Steve Askins presented a CPV module with planar micro tracking that achieved 29% efficiency at CSTC and up to 25% energy boost with the diffuse contribution. Duanhui Li from MIT presented micro-prism spectrum splitting optics with a 75% optical efficiency. Matt Lumb presented a 5J CPV cell that achieved 35.4% that was assembled into a module using transfer printing. Sodabanlu et al. from AIST presented InGaP growth rate by MOVPE of >30 μm/hr with GaAs grown at 120 μm/hr. Metaferia et al. from NREL presented GaAs solar cells by HVPE with growth rates exceeding 300 μm/hr. Recognizing the competition between perovskite/silicon and III-V / silicon technologies, there were a number of sessions on Hybrid Tandems dubbed "Battle Royale." S. Fan et al. reported on a 20% MBE-grown GaAsP/Si tandem solar cell. T. Grassman improved his group's 2018 record 20.1% epitaxially grown GaAsP/Si tandem cell to 21.8%. Improving the current of the Si cell, improving the GaP nucleation, and reoptimizing the top cell and buffer layer, showed a path to a

30% efficient device. Michael Rienaecker presented how three terminal silicon bottom cells work for tandems that are current mismatched in various configurations.

Area 4 *Silicon Photovoltaic Materials and Devices*

The Area 4 plenary was given by Denis De Ceuster from DDC Solar, providing an overview of passivating contacts for silicon solar cells. Standard Al-BSF technology is limited to 20% efficiency, rising to 23.5% with the emerging PERC architecture. To achieve higher efficiencies (up to 25%) requires passivated contacts. PERC also enables bifacial modules and is free from light-induced degradation. He reviewed three architectures: (1.) the silicon heterojunction cell benefits from a short process flow with no high-temperature processing but may be 2.5x more expensive than the PERC process. (2.) Thin Tunnel Oxide Passivated Contact (TOPCon) is compatible with the PERC process, and adds only a couple of additional process steps to the production line, so is the least expensive of these. The TOPCon layer can be implemented on the rear of the cell with a standard diffusion on the front, or on both sides of the cell. (3) Non-silicon heterojunctions, where the doped amorphous silicon layers in (1) are exchanged with carrier-selective materials, e.g., TiO_2 as an electron contact and MoO_x as a hole contact and has similar disadvantages as the silicon heterojunction approach.

The session on "Innovations in Manufactured Solar Cells" was declared 'simply amazing' by the session chairs since the industry is entering an era of 23% screen printed cells with standard metallization processes. Trina Solar showed passivating contact n-type cell production (TOPCon) with record efficiency of 24.6%. ECN showed several approaches for passivating contacts, including PERC poly p-IBCQ-cells and bifacial PERC devices reaching 22 % (0.1% less than for monofacial PERC) with a bifacial factor of up to 0.77. SERIS is also working on passivating contact approach called monoPoly reaching 23.5% with 0BB. Meyer Burger showed a HJT 2.0 cell with record efficiency of 24.5%. Felix Hasse demonstrated a hybrid IBC structure using n-poly over tunnel oxide for n-contact and local Al-BSF for p-contact and have reached 21.8% on p-type (Ga-doped) on 2×2 cells with screen-printed electrodes. Abhijit Kale presented comprehensive and convincing analysis of the tunnel layer formed by TOPCon and POLO approaches respectively. He showed an increase in recombination at the textured surface is caused by microroughness at the pyramid facets and nonuniformity of the oxides. The issue can be mitigated by an extra acid treatment.

Area 5 *Characterization Methods*

The Area 5 plenary was given by Uwe Rau from Fz. Julich who showed how losses in a solar cell can be determined by either performing a detailed bottom up analysis, or by using reciprocity relationships between absorption and emission it is possible to use top-down methods such as luminescent imaging to extract surprisingly rich data from a solar cell. T. Song from NREL demonstrated the reliability of the asymptotic P_{max} method, as compared to others methods (MPP tracking, SCFC) to measure IV curves of emerging PV devices. An uncertainty of more than 1 percent was estimated to persist. S. Reichmuth presented an overview of measurement issues encountered by calibration laboratories when measuring silicon solar cells with thin or discontinuous busbars. Use of coaxial I-V probes at Fraunhofer ISE shows promise over traditional I-V-I "triplet" configurations. Detailed procedures used for measuring "busbarless" cells were also presented. The ability to measure the voltage on the nanoscale to characterize individual PERC back contacts using photoconductive AFM tips was demonstrated by Bryan Huey. Using luminescence imaging, the temperature coefficient of implied voltages was demonstrated on multi-crystalline wafers from different positions of the ingot by Shuai Nie.

Area 6 *Perovskite and Organic Solar Cells*

The Area 6 plenary was given by David Cahen from the Weizmann Institute, who presented a comprehensive survey of halide perovskite materials and their application to PV. He noted perovskite materials' unusual properties, chiefly as a rare instance of a soft inorganic semiconductor. They also have remarkably low defect densities and in common with CIGS, they have a self-healing ability but with a much shorter time constant, 10 minutes as opposed to 10 years for CIGS. He summarized recent device results including 28% for a perovskite/silicon tandem cell by Oxford PV. C. Bailie presented work from Tandem PV on the complexities of scaling up halide perovskite PV architectures from cells to mini-modules pointing out the relative advantages of laser versus mechanical methods for scribing through the various layers. V. Zardetto described Solliance's progress on scalable fabrication of 100 cm^2 area, semi-transparent halide perovskite PV modules using primarily slot-die coating and S2S ALD. Y. Huang employed a model to study the diffusion of mobile ions in perovskite solar cells and reproduce key characteristics such as hysteresis, etc. He applied 'Big data' analyses to determine key degradation mechanisms and sort them by significance (moisture, inclusion of oxygen, heat, type of CTL etc.) Finally, S. Lee reported on attempts to deposit a perovskite top solar cell on textured Si bottom solar cell by a dry two-step process. The perovskite layers grown on textured Si solar cells show good conformal layers, proven by partial LBIC and spatial

PL. S. Manzoor performed optical modelling of all perovskite tandem PV cells, for the first time providing a complete set of optical constants of low- and wide bandgap perovskites.

Area 7 *Space and Specialty Technologies*

The Area 7 plenary was given by Yannick Combet from Thales, unveiling the concept for the Stratobus airship. Classed as a High Altitude Pseudo Satellite (HAPS) it is 140 m in length, operates at an altitude of 20 km and provides communication, navigation and observation services to civil and military clients. Power will be supplied by 300 kWp of PV with an array voltage of 1200 V. M. Imaizumi presented a novel mechanically stacked 3J cell made by from a top InGaP/GaAs dual-junction (2J) cell and a 1.1 eV CIGS bottom cell designed for very high radiation resistance, with 94% efficiency remaining at EOL. P. Espinet-Gonzalez described the potential of Nanowire based GaAs and InP solar cells in terms of radiation hardness. A world record Nanowire cell with 16.9% efficiency (BOL) was presented. P. Chiu reported the qualification results for the lattice matched triple junction XTE family of cells developed at SpectroLab, including 32% BOL and 27.8% EOL efficiency. M. O'Neill gave a comprehensive overview of the technology development at NASA of space PV concentrators for outer planet missions, and in particular the cost and weight savings achieved from line-focus and point-focus Fresnel lenses. He reported the lightest lenses made to date with 1 gram for 10 cm x 10 cm area.

Area 8 *PV Modules Manufacturing and Applications,*

K. Passow of First Solar analyzed mistracking related losses, which had large implications on a daily basis. K. McIntosh of PV Lighthouse presented a ray-tracing approach to analyze the performance of bifacial systems. He showed how SunSolve software uses cloud-based computation, micron-level tracing of 20 million rays and includes intricate effects such as cell texture, coupled with SPICE simulation of the module circuitry. He was able to quantify the mismatch losses in single-axis tracker systems with bifacial modules. The non-uniform backside irradiance due to edge brightening and torque tube shading can lead to 0.2% cell-to-cell mismatch loss on the modules, the actual value depending on the module position. In addition, A. Wheeler showed that a GaAs module delivered a daily performance ratio (PR) of 98% while silicon modules had a PR of 90-94% on a cool day. B. Newman introduced the concept of dynamic shading; a momentary shading that can interfere with maximum power point tracking. Overall electricity yield losses due to dynamic shading could be >5% with the wrong electronics. At present, there is no specification supplied by a power optimizer manufacturer that could help inform optimizer choice. Finally, N. Shiradkar spoke on the damage to PV plants due to extreme flooding. In some cases the damage was extreme, while in other cases, often when the PV panels were at low inclination, damage to submerged panels was minimal and power output remained the same. The most frequent source of damage was due to flooded inverters that caught fire.

Area 9 *PV Modules and System Reliability*

Chris Deline from NREL gave an inspiring plenary talk on the fact and fiction associated with bifacial modules. The PERC silicon solar cell process lends itself to bifacial cell manufacturing; presently bifacial modules command a premium price in the photovoltaic market of around 5-6c/W. The fractional energy gain over a monofacial module is highest under diffuse irradiance, so the overall gain depends upon overall irradiance conditions as well as ground albedo. Bifacial modules now account for 2 GW cumulative installed capacity. R. Witteck demonstrated improved UV stability of PERC cells through the use of different AR coatings. This is important since UV with wavelength less than 365nm is often transmitted through EVA encapsulation. A graded layer of SiN_x, SiO_y/SiN_x, or a thermal oxide showed the best stability. L. Bruckman provided comparison of field exposed and accelerated exposures of backsheets. Jones provided a comparison of indoor and outdoor tests measured by the change of series resistance. IEC61215 TC200/Qualification Plus TC500 tests were compared with outdoor exposures and clear correlations were observed. Saleh introduced a new analysis method (SSTDR) of PV arrays. Using an injected electrical pulse reflected at impedance discontinuities, disconnection, DH degradation, and PID could be detected. Several presentations addressed soiling of PV panels. M. Mazumder presented how a transparent electrodynamic screen can be used to remove particles from the PV module surfaces without water or moving parts. The scheme requires less than 0.2 Wh to clean a m^2 of PV surface. The overall O&M advantages of electrodynamic film based systems were presented.

Area 10 *Power Electronics and Grid Integration*

Patrick Chapman from Enphase gave the Area 10 plenary describing how Solarbridge was spun out of the University of Illinois to become one of two successful microinverter companies. The business was acquired by SunPower in 2014 and then sold to Enphase last year. The Enphase product has a 97.5% end to end efficiency averaged over load and voltage and a 40-year design life, using a resonant AC link design including MOSFET and ASIC components. A. Haque presented a study of the effect of solar variability (cloud induced) on short-term and long-term flicker severity for distributed and centralized PV across different geographical locations. B. Pierre described the issues caused by momentary cessation in grids with

high PV penetration. A simulation of an actual feeder showed that with high PV penetration can cause over frequency on the feeder during fault with both slow and fast ramp rate. J. Roy spoke about a new multiport PV inverter architecture designed to suppress Idc ripple and thereby minimizing the dc-bus capacitor requirement.

Area 11 *Solar Resource and Forecasting*

R. Perez showed how solar power can provide firm power at relatively low cost if state-of-the-art forecasts are used with over-sized PV power plants and energy storage. N. Engerer described how in Australia solar power forecasting on distribution systems is on the verge of being used operationally by distribution system operators for maintenance scheduling and management/operations. J. Peterson presented on how a disparity between reference-cell performance and pyranometer measurement data motivates a high quality experimental sensor station in Golden, Colorado. The output from the IMT reference cells can be predicted to within -2% for zenith angles less than 85 degrees.

Area 12 *PV Deployment, Policy, and Sustainability*

Andrew Blakers from UNSW made a compelling case for pumped hydroelectric storage in the area 12 plenary, presenting the technology as the key to a 100% renewable energy electricity supply. He argued that PV and Wind have won the energy race, and that pumped hydro can provide the needed storage. His survey of pumped hydro sites has identified 616,000 off-river sites with a storage capacity of 23 million GWh, much more than is required to store renewable energy for the entire planet. An online atlas of pumped hydro sites is available http://re100.eng.anu.edu.au/global/. I. Kaizuka summarized the freshly released annual report from IEA-PVPS on global PV markets. The global cumulative capacity has reached 500 GW and heading towards the terawatt era. At present 2.6% of global electricity generation is derived from PV. A. Jaeger-Waldau summarized the New EU RE directive 2018/2001/EU, describing at least 32% RES share in the EU allowing households and businesses to become clean energy producers. The EU PV market is recovering in many EU countries, possibly totaling around 15GW this year. H. Apostoleris discussed the role of financing in achieving ultra-low electricity prices in the Middle East, finding that the low power purchase agreement prices were the result of factors like low-interest rates and hybrid ownership models.

The authors acknowledge the full Program Committee and the many authors and presenters who chose to present their outstanding work at PVSC-46. Our difficulty in choosing highlights from such a strong field of presentations testifies to the quality of the work presented.

The ITRS and the new IRDS™

By Francesca Iacopi and Terry Hook

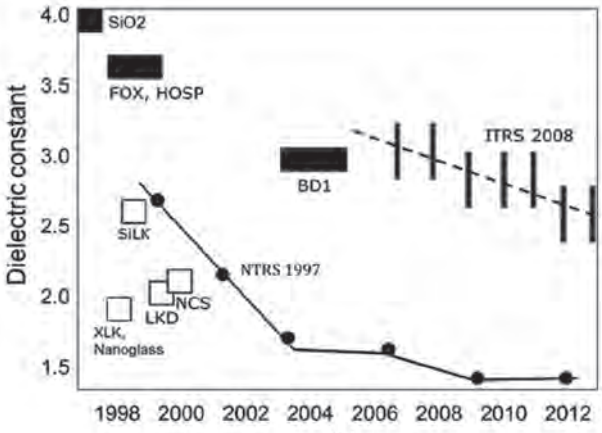
Most of us are probably familiar with the semiconductor industry's roadmaps for the future. For the past four decades, the transistor has been king. Closely assisted by courtiers such as advanced lithography, advanced gate technologies, and the associated plethora of new oxide and contact materials, and supported by increasingly complex interconnects, the transistor has governed the semiconductor roadmap over the last several decades. For many generations, a smaller transistor meant a faster and more powerful processor. These were halcyon years for the Electron Devices Society as well. Devices were in the driver's seat; and the Roadmap was ours. The semiconductor community would do anything necessary to keep on scaling down the channel length. Today's world is far more complex—and interesting—and today's Roadmap reflects that.

Both industry and academia consult the Roadmap to obtain perspective on where to direct their own efforts, even if their underlying purpose is to "beat the Roadmap;" that is, for their own internal plans to reference the Roadmap but to do better. The "old" Roadmap can claim a number of successful predictions. In the mid-90's the Roadmap (then known as the NTRS) sounded the tocsin of doom for gate dielectric scaling, noting that there were then no solutions known to drive below a 1.5 nm effective thickness, which was expected to be required in 2009 (Fig. 1a). Research was accelerated, and, as early as 2007, high-k dielectrics were introduced into high-volume manufacturing, breathing new life into classic Dennard transistor scaling. Similarly, the limitations of conventional photolithography were delineated in Roadmaps through the 1990's, prompting enormous innovations over the following decade such as double -exposure and then immersion lithography, to drive dimensional scaling beyond the diffraction limit in air. Had the Roadmap not articulated a unified

Table 1 1997 NTRS Requirements.

Year of First Product Shipment	1997	1999	2001	2003	2006	2009	2012
Technology Generation (nm)	250	180	150	130	100	70	50
Operating Voltage. Vdd (V)	2.5-1.8	1.8-1.5	1.5-1.2	1.5-1.2	1.2-0.9	0.9-0.6	0.6-0.5
Equivalent Oxide Thickness (nm)	4-5	3-4	2-3	2-3	1.5-2	<1.5	<1.0
Gate Dielectric Thickness Control (%3σ)	±4	±4	±4	±4-6	±4-8	±4-8	±4-8
Maximum Electric Field (MV/cm)	4-5	5	5	5	>5	>5	>5
DRAM GOI (per cm2)	0.06	0.03	0.026	0.014	0.006	0.003	0.001
Logic GOI (per cm2)	0.15	0.15	0.11	0.08	0.05	0.03	0.03
DRAM Particle Defects (per cm2)	0.3	0.15	0.1	0.075	0.03	0.015	0.01
Logic Particle Defects (per cm2)	0.75	0.5	0.45	0.4	0.25	0.2	0.15
Particle Size (nm)	125	90	75	65	50	35	25
Critical Metal (atoms/cm2)	5E(9)	4E(9)	3E(9)	2E(9)	1E(9)	<1E(9)	<1E(9)
Oxide Residue (O atoms/cm2)	1E(14)	7E(13)	6E(13)	5E(13)	3.5E(13)	2.5E(13)	1.8E(13)
Drain Extension Jn Depth (nm)	50-100	70-140	60-130	50-100	40-80	15-30	10-20
Contact Jn Depth (nm)	100-200	70-140	60-120	50-100	40-80	15-30	10-20
Drain Ext. Dopant Conc. (Atoms/cm3)	1E(18)	1E(19)	1E(19)	1E(19)	1E(20)	1E(20)	1E(20)
Contact Silicide Rs(Ω/Sq.)	2	2.7	3.3	3.8	2	2	2
Si/Silicide Max Resistivity (Ω-cm2)	<1E(-6)	<6E(-7)	<4E(-7)	<3E(-7)	<2E(-7)	<8E(-8)	<3E(-8)
Drain Structure	Drain Extension				Elevated Contact - Single Dj		
Sidewall Spacer Thickness (nm)	100-200	72-144	60-120	52-104	20-40	7.5-15	5-10
	No Known Solutions						

(a)



(b)

Figure 1 (a) Excerpt from 1997 NTRS Roadmap [1]. (b) Early optimistic predictions for dielectrics [2]

pre-competitive perspective of those key challenges early on, building consensus and buy-in from the whole semiconductor value chain, would these and other vital innovations have been developed? Perhaps so, but certainly not in such a timely fashion. In the interest of honesty, the Roadmap has also had its share of misses—they could also be described as "unfulfilled challenges" or maybe even "wishful thinking"—either way they have set a goal for the whole community to try and achieve. In one of the most notorious examples, the 1997 version anticipated interconnects insulators with a dielectric constant of less than 1.5 in 2012 (Fig 1b). Despite intense R&D in materials and integration for over a decade, even today's production has never really gone much beyond the integration of materials with k = 2.5. Interconnects have been one of the most underestimated challenges in the history of the semiconductor roadmap. Nevertheless, the Roadmap has successfully brought nanotechnology to mass-scale production, bridging the long valley of death between lab-based conceptual solutions to production-scale technologies from advanced lithography to novel materials for frontend to backend technologies.

The classical CMOS transistor has not really been exclusively preeminent for some time, however. Today's systems need broad diversification. Even within the context of classic Von Neumann computing, hardware-based accelerators, such as intimate CPU/GPU connections like NVlink and CPU/FPGA interfaces such as CAPI, are responsible for much of the recent advances in HP computing [3], [4]. Additionally, while the full potential of digital computing has not yet been exhausted as described in the More Moore chapter. Very different approaches such as analog computing with neuromorphic systems and quantum computing are driving toward on the one hand, intelligent decision-making systems, and maximum computational power on the other hand.

The latest manifestation of the Roadmap extends the scope beyond "how to make a smaller transistor" into the realm of "how to make an improved, miniaturized and tailored system." The mutation of the name ITRS—International Technology Roadmap for Semiconductors—to IRDS™—International Roadmap for Devices and Systems—is much more than window dressing. The latest Roadmap structure connects new system requirements to the technology elements needed and their combinations. Again, IRDS™ is expected to bring pre-competitive consensus across an increasingly more interdisciplinary community (from technologists to designers to quantum and computer scientists) to materialize ground-breaking innovations. Who knows—perhaps in a decade's time we may be writing that "the IRDS™ extrapolation regarding 3D monolithic integration and magnetoresistive neuromorphic synapses was prescient." The IRDS™ has not surrendered its continued role in anticipating the needs of transistors and "classic" wafer-scale semiconductor manufacturing. The new release of the Roadmap still contains chapters on More Moore and Beyond CMOS devices, and Factory Integration, Lithography, Metrology, and Yield, for example. It also emphasizes further the Environmental aspects of semiconductor industry. In addition, IRDS™ includes chapters on Application Benchmarking, Systems and Architectures, and Cryogenic and Quantum Computing. It is beyond the scope of this article to summarize the hundreds of pages contained in the IRDS™ just released; the interested reader is encouraged to locate all the documents at https://IRDS.ieee.org/. Here, the intention is to give some highlights and perspectives regarding the activities, challenges and directions of the International Roadmap for Devices and Systems.

Before delving into the newest esoterica, let's examine the vision for 'traditional' logic transistors in the Roadmap, whose characteristics are largely contained in the More Moore chapter. The mainstream device in the 2025 timeframe is expected to be a lateral GAA structure (Fig. 2). In 2028 pitch scaling is expected to stagnate at a 40 nm gate pitch and 16 nm interconnect pitch; 3D constructs are introduced to improve area scaling. Vdd also stagnates, and power density emerges as the primary challenge, along with containment of parasitics. As the scaling is no longer following the pace of the last few decades, a semantics debate is recurrent in the community, regarding the nomenclature for future technology nodes. The team is discussing the use of a suffix of plusses to indicate fractional node implementation. Silicon Germanium is expected to supplant Si as the pFET channel material. Considerable research investment has been made already in those areas, but though these devices are still basically semiconducting CMOS switches supporting the Von Neumann computing paradigm, absorbing so many key inflections will be challenging to the industry. It is important to note that none of the CMOS-compatible switching devices discussed in the Beyond CMOS chapter such as ferroelectric negative-capacitance FETs, TFETs, III-V, and 2D channel materials are explicitly required to meet the scaling and performance goals as defined in this scenario. It is possible that one or more of these devices may find their way into the stream in the out-years, but LGAA and 3D monolithic integration, which are relatively device-agnostic, form the basis for the improvements in the Roadmap. One important open challenge recently reinforced by the More Moore team, is that there is currently no known solution for achieving a steeper sub-threshold slope. TFETs have so far failed to deliver, partly due to inaccurate band-to-band models and predictions. A potential breakthrough may though come with the implementation of 2D materials.

In addition, further scaling of on-chip interconnects is seeing a "return to the future," with copper interconnects being likely phased out by higher resistivity materials, though more appropriate to scaled performance and reliability. This may lead to a complete rethinking of interconnect technologies, including the notoriously complex copper damascene approach.

Memory has been, and will continue to be a key driver to the overall scaling and performance of systems. While DRAM and Flash are expected to essentially maintain scaling through these years (there is an anticipated difficult transition to the Vertical Channel Transistor cell architecture for DRAM), there are various options in play for non-volatile memories. All forms basically rely on a permanent, reversible change to the impedance of a link. Phase-change, ferroelectric effect, and filamentary resistance are all current options for the storage element. Each has its own challenges, ReRAM density being one of the key pinchpoints for future scaling.

While the Roadmap continues in its important work of anticipating the technological needs of the mainstream semiconductor industry, the new IRDS™ also considers radically different computing paradigms and the underlying technologies required. The rebooted Roadmap aims at "built for purpose" hardware, as opposed to the old approach of "general purpose" computation systems. This is reflected into two widely different "bookend" approaches to complement classic mobile and High Performance computing addressed in the latest IRDS™. On the one extreme are the cryogenic computers, including Quantum Information Processing.

The complex cooling infrastructure demands centralized location of these computers and they would be directed to high-performance computation, the new IRDS™ Chapter on Cryogenic and Quantum computing addresses Superconducting electronics, cryogenic application of semiconductors, and the emerging quantum computing. Cryogenic semiconductors have been considered for many years as cooling can improve performance and leakage of silicon-based CMOS, and is needed for cryogenic environments. Superconducting electronics offers the possibility of very low switching energy, even when cooling power is considered. However, today state of the art superconducting chips have fewer than 1 million junctions and many challenges need to be overcome to achieve the 1 billion range to be comparable to today's conventional CMOS chips. Quantum computing is in its infancy as well, with the largest quantum computers sporting fewer than 100 qubits.

Although the landscape of technological contenders in quantum computing is large, challenges abound in fabricating physical qubits, especially in scaling up their number, ensuring and maintaining their coherence for a useful duration of time, in devising an appropriate error correction strategy to produce adequate logical qubits, and overall in enabling quantum information processing to realize its potential over conventional computing. There will be a critical need for developing fault-tolerant computation approaches, and a need for early co-design with quantum software is anticipated. A dedicated working group on Quantum Computing has spun off in 2018 in IRDS™, testimony to the vast and specific challenges of this field.

At the other extreme lies edge, or frontend, distributed computing. This approach promises to be a solution to the computational problems where complex classification and decision making (thus artificial intelligence) need an enormous amount of data transmission back and forth between the logic unit and the memory. Currently, the limited data transmission rates between the different partitions are the bottleneck to the further progress of artificial intelligence in Von

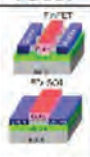
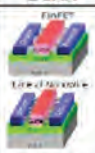
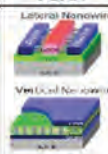
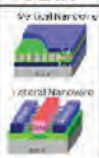
YEAR OF PRODUCTION	2018	2020	2022	2025	2028	2031	2034
	G54M36	G48M30	G45M24	G42M21	G40M16	G40M16T2	G40M16T4
Logic industry "Node Range" Labeling (nm)	"7"	"5"	"3"	"2.1"	"1.5"	"1.5"	"1.5"
IDM-Foundry node labeling	i10-f7	i7-f5	i5-f3	i3-f2.1	i2.1-f1.5	i2.1-f1.5	i2.1-f1.5
Logic device structure options	finFET FDSOI	finFET	finFET LGAA	LGAA VGAA	LGAA VGAA	3DVLSI VGAA	3DVLSI VGAA
							
Mainstream device for logic	finFET	finFET	finFET	LGAA	LGAA	LGAA	LGAA
Vdd (V)	0.75	0.70	0.70	0.65	0.65	0.60	0.60
Gate length (nm)	20	18	16	14	12	12	12
Number of stacked tiers	1	1	1	1	1	2	4
Number of stacked devices	1	1	1	3	3	4	4
Digital block area scaling - node-to-node	-	0.60	0.75	0.82	0.79	0.57	0.50
Cell height limitation - high-density	device	M0	M0	M0	M0	M0	M0
SoC area scalling (stacked) - node-to-node	-	0.70	0.79	0.84	0.83	0.60	0.60
CPU frequency (GHz)	2.90	3.13	3.32	3.80	4.09	3.59	3.33
Frequency scaling - node-to-node	-	0.08	0.06	0.15	0.08	-0.12	-0.07
CPU frequency at constant power density (GHz)	2.90	1.92	1.69	2.10	2.01	1.26	0.73
Power at iso frequency - node-to-node	-	-0.23	-0.14	-0.35	-0.24	-0.10	-0.14
Power density - relative	1.00	1.64	1.96	1.81	2.04	2.86	4.53

Figure 2 excerpt from IRDS™ [5]

Neumann architectures, where logic hardware is separated from memory, making GPUs underutilized. The minimum memory needed for image learning is at least 1GB, and needs very fast access times, with no less than 1 month retention time. New technologies that could ease this bottleneck are going to be carefully considered.

While this will take many forms, including conventional computing enabled by More Moore scaling, some of the most exciting elements of this involve brain-inspired models such as neuromorphic computing hardware. The latter, with all of its different potential approaches, potentially spiking neural networks is expected to become key for AI implementation at the edge, offering a more efficient interaction with the analog world, and in addition, could dramatically reduce computing energy consumption. Vital for image recognition, matrices of tunable elements are programmed based on a learning phase and then used in very rapid analog calculations to identify patterns during the inference operation. Various means of fabricating these artificial synapses are under development, such as ferrolelectric tuning, magnetic moment manipulation, and modulation of resistance. Networks can also be formed with coupled oscillators, which in some ways more closely mimics brain function, and fabrication of VO_2-based structures is known, The Beyond CMOS chapter of the IRDS™ contains an extensive assessment of neuromorphic computing technologies and other approaches that are not replacements for CMOS switches, but are rather entirely new means of doing computations.

As was the case for ITRS, new materials and their integration and reliability will be still underpinning the novel advances over the next 20 years for all of the areas of the IDRS™. 2D materials, as already mentioned, may bring the long—sought breakthrough in TFETs, although the major challenge here will be how to deal with materials that are made 100% by surfaces/interfaces. A plethora of advanced oxides are being considered as materials for "memristors," which could be the basic hardware components for neuromorphic computing.

In addition, among the different ideas brewing in the Beyond CMOS working group, there is another one that could represent another paradigm shift: fully reversible computing. One would argue that the second law of thermodynamics cannot be broken, however there could be ways to substantially limit entropy, and this would be underpinned by yet another radically different way of doing computing, from the device level, to the computation principles and software. Novel materials such as topological insulator, or older solutions like adiabatic CMOS switches or superconducting electronics may hold the promise to address such problem at a device level, however, this hardware will have to be complemented by a truly reversible computing approach. Many of the Beyond CMOS solutions indicate the need for early co-design of hardware and computing/software approaches.

The connectivity and communications area is spread across a few different work packages in IRDS™, and covers a very broad range of technical areas. While more specific information can be found in the particular Roadmap documents, it is probably useful to briefly mention a couple of major items. For example, one flagrant bottleneck we have already discussed is given by the increasing need for high rate data transmission within the electronic system as well

as towards the outside world. Photonics transmissions are thus a high priority. However, the handshake between electronics and photonics is shifting levels, and one of the most important questions becomes where and how best to make the electron/photon conversion happen.

When mentioning communications, 5G is clearly one of the big items of the Roadmap, and particularly 5G versus how to approach 6G. The switch to the 5G paradigm will likely not be able to go to the planned extent, so some indicate that 6G will achieve the full 5G expectations. 6G will require terahertz electronics, another area of growing R&D. During one of the recent debates at the IEEE Rebooting Computing conference in Grenoble, it was pointed out that mobile communications will have to be increasingly cooperative with local WiFi systems, as the next targeted communications bands will not efficiently penetrate buildings. In the same discussion, a "sharing economy" of communication bands and computing, where all mobile devices in the vicinity would cooperate to optimize usage, was also discussed. Although clearly this is an appealing proposition, there is an elephant in the room to be addressed, called Cybersecurity, in particular, how trust between different systems will be implemented. This is one more opportunity given by IRDS™ to bring hardware, communications and software scientists closer together at an early stage.

The NTRS, and subsequently ITRS, have been a very powerful instrument guiding the intensive R&D semiconductor efforts over the last decades. As the semiconductor community has finally come to terms with the fact that pure dimensional scaling will not be able to drive electronics for another 20 years, now more than ever, we are facing an exciting set of solutions and challenges regarding how this industry is going to evolve in the coming decades. The IRDS™ goal of "building for purpose" opens up many more different directions for the community to pursue in a pre-competitive stage, as compared to pure scaling with Von Neumann architectures. As the more challenging new solutions will require a lead time of likely up 10 years or more, during which the technologies are thoroughly developed, reliably produced and scaled up, and the corresponding semiconductor supply chain (materials, metrology, equipment suppliers with multiple trusted sources) will have to be developed. The IRDS™ will be needed to gain early visibility and insights on feasibility of such solutions, assess whether they can be or become fit for purpose, and steer the increasingly complex ecosystem to make implementation happen efficiently within a reasonable amount of time. Academia is expected to continue looking up to the roadmap for guidance as to the types of problems and corresponding solutions needed, the specs to be reached, etc. Indeed, a key aspect of the Roadmap are the "roadmap tables" like those in Figure 1 and 2 that have been produced by NTRS and ITRS in the past. Those tables are likely to become even more complex in the IRDS™ era, as totally new metrics—as well as new *standards*—will have to be developed for new computing paradigms, from Quantum to Neuromorphic.

In addition, in this second age of the Roadmap, the ecosystems are becoming ever more complex and interdisciplinary, and the needed solutions, as explained, will need to encompass materials/device manufacturing technologies, design, computing, software. Early co-design across traditionally distant disciplines will be primordial, as attempts at retrofitting technologies as an afterthought exercise in this context will likely lead to a vast amount of wasted efforts (hence the "Systems" part in the IRDS™ acronym). IRDS™ will have to play the "glue" for the whole community at large—across disciplines, across academia and industry, and again across geography—to come together and devise the new Roadmap. From an industrial point of view, the challenge will be to get enough momentum across all of the vertical levels of the value chain but also across the new leaders of electronic systems, which include several "fabless" players (Google, Apple, Microsoft, just to name a few), which makes today's industry a much more fragmented landscape as compared to the ITRS era. Geographically speaking, the challenge will be to effectively bring together representatives from all of the major regions of the world where Electronics R&D is substantial. The international aspect of the IRDS™ is apparent in the close relationship with the European SiNANO Institute and its recently completed three-year NEREID Roadmap project, and exemplified by the location of the latest IRDS™ Workshop in Grenoble, France. Next year, the Spring workshop is expected to be in Japan, thanks to the Japan Society of Applied Physics, and SDRJ, the System Device Roadmap Committee of Japan.

This is a particularly exciting time to be involved in computing technology, and the new IRDS™ offers new opportunities to learn about and participate in all aspects, driving, evolving and converging to common goals from basic materials to manufacturing and entirely new computing paradigms.

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[1] The National Technology Roadmap for Semiconductors, Semiconductor Industry Association 1997.

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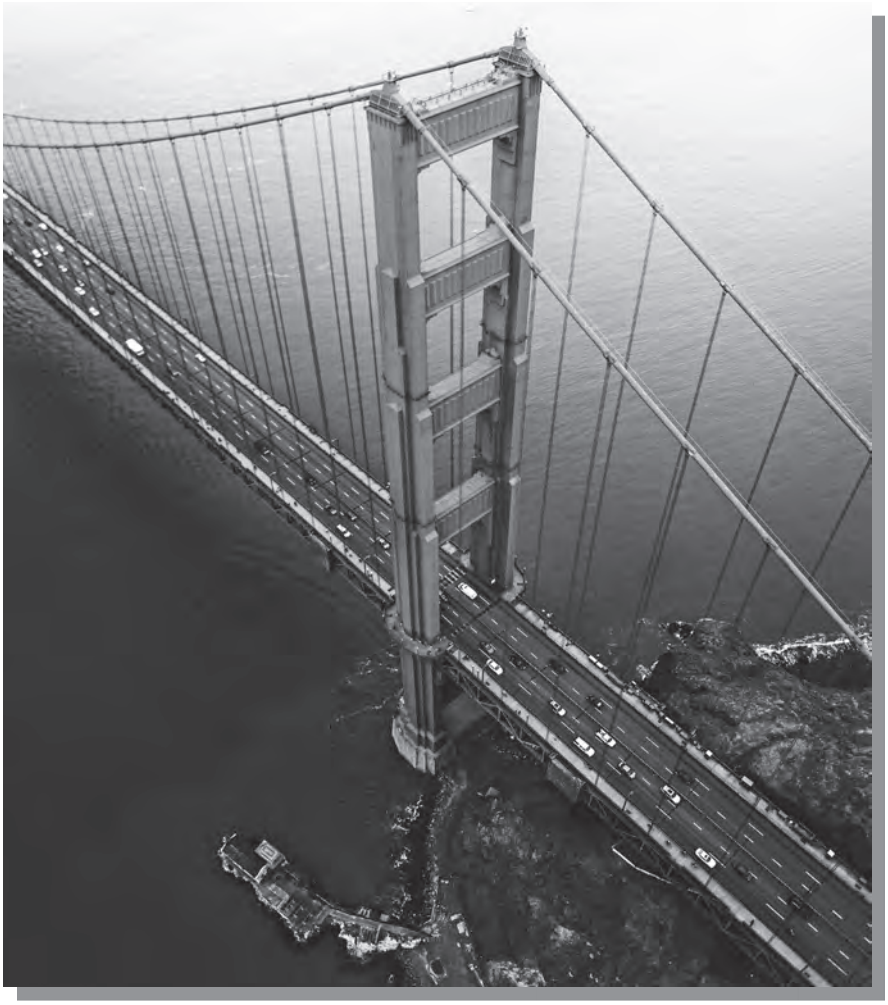
[5] IRDS™ https://irds.ieee.org/

2019 IEEE International Electron Devices Meeting
to Highlight Innovative Devices for an Era of Connected Intelligence

IEDM 65th International Electron Devices Meeting



The upcoming 65th annual IEEE International Electron Devices Meeting (IEDM), to be held December 7–11, 2019 at the Hilton San Francisco Union Square hotel, will once again feature the latest and most important research taking place in electron devices, but this year the focus will be different.

Under the theme "Innovative Devices for an Era of Connected Intelligence," IEDM 2019 will turn a brighter spotlight on new types of processors, memories, accelerators, 3D architectures, power devices, quantum computing concepts and other novel devices and materials needed for evolving and fast-growing applications like artificial intelligence, mmWave/5G communications, automotive electronics, the Internet of Things and others, in addition to talks that describe breakthroughs in traditional CMOS scaling.

The conference will offer attendees more than 220 scheduled presentations and an extensive slate of tutorials, short courses, focus sessions, panels, poster sessions from affiliated groups, and supplier exhibits to complement the technical program, along with a luncheon talk and many networking opportunities designed to support the continuing educational needs of today's students, engineers and scientists.

Also, this year the IEDM once again will feature special sessions of invited papers focused on some of today's most important areas of research. This year's Focus Session topics are AI technologies, the human-machine interface, quantum computing infrastructure, and reliability for circuits and systems.

Here are details of the 2019 IEDM:

90-Minute Tutorials—Saturday, December 7

The 90-minute Saturday tutorial sessions on emerging technologies have become a hugely popular part of IEDM. These are presented by experts in the fields, the goal being to bridge the gap between textbook-level knowledge and leading-edge current research. The topics for 2019 are:

- *Oxide Semiconductors and TFTs: What is different from conventional semiconductors?* Hideo Hosono, Tokyo Institute of Technology
- *Cryogenic MOSFET Modeling,* Christian Enz, EPFL

- *FEFE Memory (FRAM, FTJ and NCFETs)*, Johannes Mueller, GLOBALFOUNDRIES
- *In-Memory Computing for AI,* Abu Sebastian, IBM
- *3D-Monolithic Integration,* Perrine Batude, Leti
- *Magnetic Sensors*, Keith Green, TI

Short Courses—Sunday, December 8

Register early for the full-day Sunday Short Courses , as they are often sold out. They offer the opportunity to learn about important areas and developments, and to network with global experts.

- **Technology Scaling in the EUV Era and Beyond**, organized by Wook-Hyun Kwon, Samsung
  - *Future of Computing: From Core to Edge Computing,* Karim Arabi, Qualcomm
  - *Logic Transistor Options for 3 nm Node and Beyond*, Jin Cai, TSMC
  - *Advanced Processes for Technology Scaling Beyond 3 nm,* HooChur Kim, Samsung
  - *Design Technology Co-Optimization for Advanced Scaling,* Lars Liebmann, TEL
  - *Novel Interconnect Techniques for CMOS Technologies in the EUV Era,* Intel
  - *Low-Power Device Solutions for Ultra-Low-Power Computing,* Arokia Nathan, Univ. of Cambridge
- **Technologies for Memory-Centric Computing**, organized by Ali Keshavarzi, Stanford University
  - *Emerging Memories on Advanced Technology Nodes,* Oleg Golonzka, Intel
  - *Advanced DRAM, 3D-stacked SDRAM and HBM Technologies,* Kyomin Sohn, Samsung
  - *Novel 3D NAND, Lower Latency NAND and Persistent Memory Technologies,* Jian Chen, Western Digital
  - *Emerging Memory and AI Technologies,* Edith Beigne, Facebook
  - *Requirements of Advanced Memory Devices,* Alessandro Calderoni, Micron Technology
  - *Advanced Memory-Centric Computing: A Device, Circuit and System Perspective,* Arijit Raychowdhury, Georgia Tech.

Plenary Presentations—Monday, December 9

- Robert Chau, Intel
- Kazu Ishimaru, Toshiba
- Martin van den Brink, ASML

Luncheon—Tuesday, December 11

IEDM will have a career-focused luncheon this year featuring industry and scientific leaders talking about their personal experiences in the context of career growth. It will be moderated by Jungwoo Joh, TI, and this year's speakers will be Ramune Nagisetty from Intel and Linda Sommerville from Micron.

Evening Panel Session—Tuesday evening, December 11

IEDM 2019 will offer attendees an evening session where experts will give their views on important industry topics in a fun, engaging format. Audience participation is encouraged to foster an open and vigorous exchange of ideas. The title of this year's evening panel is "**Rest in Peace Moore's Law, Long Live Artificial Intelligence,**" organized by Dr. Vijay Narayanan, IBM Fellow and Manager, Materials Research.

Vendor Exhibition/Poster Sessions

- A vendor exhibition will be held once again.
- This year two poster sessions will be held, one on MRAM technology organized by the IEEE Magnetics Society, the other a student research showcase hosted by the Semiconductor Research Corporation.

Further Information about IEDM

For registration and other information, visit www.ieee-iedm.org.

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Tohoku University

Dina Triyoso
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TEL Technology Center America

4th Electron Devices Technology and Manufacturing (EDTM) Conference 2020

March 16–18, 2020, Hotel Equatorial, Penang, Malaysia

https://ewh.ieee.org/conf/edtm/2020

The **IEEE Electron Devices Technology and Manufacturing (EDTM) Conference 2020** is a three-day meeting to be held at the ***Hotel Equatorial***, Penang, Malaysia from **March 16–18, 2020**. The IEEE *Electron Devices Society* (EDS) sponsored EDTM is a premier conference for the electron devices community. The EDTM provides a unique forum for the electron devices community to discuss and collaborate on broad range of device/manufacturing-related topical areas including materials, processes, devices, packaging, modeling, reliability, and manufacturing and yield. The **EDTM 2020** will provide the following formats.

Technical Sessions

The EDTM 2020 solicits papers in all areas of materials, processes, devices, packaging, modeling, reliability, and manufacturing and yield. Papers on devices and systems for Internet of Things (IoT) include all areas of **sensing**, **connectivity**, and **computing** to enabling smart environments and integrated ecosystems. Topical areas for papers, not limited to, are low-power/smart-power devices, wearables, advanced memories, sensors, actuators, MEMS, bio-chips, artificial intelligence and machine learning, passive devices, and all types of (exploratory) device concepts within the following broad technical areas:

- Materials
- Process and Tools for Manufacturing
- Devices and Smart Systems for Internet of Things (IoT)
- Smart Power and Renewable Energy Devices
- Modeling and Simulation
- Reliability
- Packaging and Heterogeneous Integration
- Manufacturing Yield
- Emerging Photonics, Bio-photonics, Optoelectronics Technologies, and Novel photovoltaic devices
- Artificial Intelligence (AI) and Machine Learning

Authors should indicate a technical area based on the broad topical areas shown above during online paper submission. The conference will also include poster presentations. Authors should indicate their preference for oral or poster presentation format when submitting their abstracts.

Publications

The EDTM 2020 papers will be subjected to IEEE-EDS standard review processes and IEEE conference publishing guidelines. The accepted papers presented at the meeting will be published in the EDTM 2020 proceedings and may be available on *IEEE Xplore*. Besides, the authors of a selected number of *high-impact* presented papers will be invited to submit an extended version of the same for the consideration of publication in the *IEEE Journal of Electron Devices Society* (J-EDS). All such submissions must comply with J-EDS author-guidelines and will be subjected to the standard IEEE and J-EDS review and publication policy.

Short Courses and Tutorials

The EDTM 2020 will be preceded by several short courses on March 15, 2020, encompassing the latest advancements in niche application areas of interest, which include hardware security, sensors for IoT, flexible and wearable electronics, artificial intelligence (AI) and machine learning, and heterogeneous integration of different device technologies.

The EDTM 2020 will, also, be preceded by several tutorial sessions on topics ranging from front-end to back-end-of-line CMOS process, packaging and emerging memory technology.

Important Dates

October 14, 2019: Final *four-page* extended abstract submission including Text, Figures, Tables, and References

December 14, 2019: Notification of acceptance

Arjun Kantimahanti
Silterra, Malaysia

Samar Saha
Prospicient Devices, USA
EDTM 2020 General Chairs

2019 IEEE International Integrated Reliability Workshop (IIRW)

The 2019 IEEE International Integrated Reliability Workshop (IIRW), sponsored by the IEEE Reliability Society and the IEEE Electron Devices Society, will be held at the Stanford Sierra Conference Center on the shores of Fallen Leaf Lake near South Lake Tahoe, California, October 13–17, 2019. This workshop provides a unique forum for open, lively discussions of all areas of reliability research and technology for present and future semiconductor applications.

Reliability topics for the workshop include: emerging memory technologies (ReRAM, FeRAM, MRAM, etc.), FinFET on bulk and SOI, high-*k* and nitrided SiO_2 gate dielectrics, reliability assessment of novel devices, power devices and wideband gap material reliability, organic electronics, transistor reliability including hot carriers and NBTI/PBTI, MOL and BEOL interconnects and low-k dielectrics, product reliability, impact of transistor degradation on circuit reliability, reliability modeling and simulation, optoelectronics, single event upsets, array testing and others. Special focus this year will be on BEOL and emerging memory reliability.

IIRW is quite different from a typical technical conference. Located 6400 feet above sea level in the California Sierra Nevada, the Stanford Sierra Conference Center provides an ideal atmosphere for a relaxing yet informative workshop. All aspects of the workshop, including the physical isolation of the location, the absence of distractions such as in-room phone/television, and the format of the technical program, encourages extensive interaction among the workshop attendees. You feel yourself drawn into technical discussions from the start.

The conference traditionally begins Sunday evening after the majority of attendees arrive. The single Sunday night talk includes refreshments, and is designed for the weary traveler, being a technically toned-down presentation on an interesting topic either peripherally related to reliability, or simply an interesting hobby or business from one of the attendees. This year we are delighted to announce this Sunday night talk will be given by Jason Ryan from NIST and devoted to his hobby—Antique trucks restoration.

The keynote will be given by Dr. Eduard Cartier (IBM research) who will talk about Analog devices for Artificial Intelligence. Additionally, the list of Invited speakers will include Clemens Ostermaier (Infineon) on GaN device reliability, Sofie Beyne (*imec*/ KU Leuven) on electromigration, Jason Ryan (NIST) on the frequency-modulated charge pumping technique, Michael Waltl (TU Vienna) on FEOL reliability characterization techniques, Cristiano Capasso (GlobalFoundries) on automotive reliability, Gennadi Bersuker (Aerospace corporation) on emerging memory reliability, Luca Larcher (Advanced Materials) on RRAM and emerging memory reliability modeling, Sonia Ben Dhia (Univ. Toulouse) on electromagnetic compatibility, and Barry O'Sullivan (imec) on logic for memory and related reliability issues.

At the IIRW 2018, "Reliability Experts Forum" was introduced to the conference. It was an attempt to bring top reliability experts in the transistor reliability to one platform leading to very invigorating discussions. Building on the success of the forum, this year, the topic of the forum will be "Memory technology and Reliability." The event is expected to be participated by world experts as panelists and researchers as participants. It aims to have discussion on Memory Architecture, Technology and Reliability risks for current as well as emerging technologies.

Another advantage of attending IIRW is the collection of tutorials, presented by leading experts and included at no additional cost. This year program includes two tutorials in FEOL reliability in advanced nodes given by Andreas Kerber and Adrian Chasin (*imec*) and on BEOL TDDB by Tian Shen (IBM).

One other advantage of IIRW is the moderated discussion groups that are held in the evenings. Following up on the discussion groups are the Special Interest Groups, which are composed of small groups of attendees who want to continue their discussions on a particular topic of interest, which often continue even after the workshop.

One unique aspect of the workshop is the opportunity for any attendee to present a walk-in poster of their latest work. Finally, attendees have Wednesday afternoon off to enjoy a variety of outdoor activities such as hiking, volleyball, sailing or kayaking, biking, walking, or simply continuing that intriguing conversation from the night before. This free afternoon is a great way to not only network, but also to build long-lasting friendships.

Additional information about the workshop is available on the IIRW website at www.iirw.org, or by contacting Zakariae Chbili, 2019 IIRW General Chair, (gc.iirw@gmail.com). Information on the Stanford Camp is available at stanfordsierra.org.

On behalf of the 2019 IIRW Management Committee, I look forward to meeting you in Lake Tahoe!

Stanislav Tyaginov
2019 IIRW TPC Chair
imec, Leuven, Belgium

Society News

Message from EDS President-Elect

Greetings to the EDS community.

Meyya Meyyappan
EDS President-Elect

As I am writing this on August 1st, I am very much looking forward to an EDS event in two weeks, IEEE International Flexible Electronics Technology Conference (IFETC) to be held in Vancouver on August 11–14, 2019. This is a new EDS conference that was started last year and is being held only for the second time. Flexible electronics is a rapidly growing field, particularly fueled by the emerging Internet of Things (*IoT*). The anticipated market for printable and flexible electronics is expected to reach $250 billion by 2025 due to numerous applications under development and on commercialization path all across the globe. The conference provides a forum to discuss all electronics that are flexible, wearable and printed including chemical, bio and physical sensors, RFIDs, antennas, actuators, transducers, thin film transistors, memory devices, energy harvesting and storage devices, displays and many others. The organizers have worked very hard to put together an excellent program including tutorials (https://attend.ieee.org/ifetc-2019/). Hope you get to attend this conference in Vancouver or at least follow the developments. Venues to hold the conference in 2020 and 2021 have already been lined up as enthusiastic volunteers from both sides of the Pacific started bidding early.

As you realize, this emerging field is entirely within the EDS field of interest: fabrication of flexible and printed devices, testing and characterization, application development, materials and processes enabling the flexible devices, modeling and simulation of devices and processes, and system integration. This is why EDS is proposing a new journal on flexible electronics and currently working through the IEEE system. We have several other IEEE Societies and Councils expressing interest in joining EDS to launch this new periodical. We need your support as authors, readers, reviewers and volunteers. Stay tuned to learn more about EDS efforts in this new and exciting field, and join us and lend a hand.

Meyya Meyyappan
EDS President-Elect
NASA

Message from the Editor-in-Chief

Dear Reader,

Carmen M. Lilley
EDS Newsletter
Editor-in-Chief

Welcome to the October 2019 issue of the EDS newsletter. I want to send a warm greeting to all of the readers who have reached out to express their enthusiasm for the celebratory July 2019 issue. In addition, I have been very pleased with the avid interest and at times passionate discussion by readers on the series of historical reviews in Marvels of Microelectronics. In this issue, I include an excerpt of one such discussion I received in a Letter to the Editor for the July 2019 article along with the response by the author Joachim Burghartz.

Sincerely,
Carmen M. Lilley

Dr. Cary Y. Yang, Professor of Electrical Engineering at Santa Clara University and former EDS President, stated:
"While the article provides an informative historical narrative of Si-based devices, it contains some unfortunate factual omission and misleading information. In particular, PSP was portrayed in the article as the only surface-potential-based compact model for MOSFET. Such portrayal is not only false, it is misleading to the reader as PSP is no longer the industry standard. As you can see on the CMC website, https://projects.si2.org/?page=1685, the current industry-standard compact models for MOSFET are BSIM and HiSIM, but such fact was not acknowledged in the article."

In response, Joachim Burghartz stated:
"we were fully aware that the list of topics we could bring up could never be comprehensive…However, with respect to compact modeling in particular, I was fully aware that I will be stepping into a political minefield… For that reason, I decided to have experts in the field decide and comment on what they believe could be

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2018 EDS Paul Rappaport Award

A high priority of the Electron Devices Society (EDS) is to recognize and enhance the quality of papers published in EDS archival literature. Every year, the Society confers its prestigious Paul Rappaport Award to the best paper published in the *IEEE Transactions on Electron Devices*. Among other criteria including technical excellence, an important metric for selection for the award is comprehensive and impartial referencing of prior art.

The winning paper was selected from over 790 articles that were published in 2018. The winning paper is entitled *"Local 2DEG Density Control in Heterostructures of Piezoelectric Materials and Its Application in GaN HEMT Fabrication Technology."* This paper was published in the August 2018 issue of the *IEEE Transactions on Electron Devices*, and was authored by Konstantin Osipov, Joachim Wuerfl, Ina Ostermay, Frank Brunner, Günther Tränkle and Maniteja Bodduluri.

The award will be presented at the plenary session of the IEEE International Electron Devices Meeting to be held on December 9, 2019, in San Francisco, California. In addition to the award certificate, the authors will receive a check for $2,500 to be shared equally among all authors. On behalf of the Electron Devices Society, I would like to congratulate the authors for this achievement. Brief biographies of some of the authors follow.

Konstantin Osipov received the master's degree in electrical engineering from Tomsk State University of Control Systems and Radio Electronics, Tomsk, Russia, in 2008. In 2012, he joined the Ferdinand-Braun-Institut, Berlin, Germany, as a DAAD student. Since 2013, he continued this work as a Ph.D. student, with a focus on high frequency, highly reliable GaN MMICs for space applications.

Ina Ostermay received the Ph.D. degree from TU Dresden, Dresden, Germany. She joined the Ferdinand-Braun-Institute in 2011, where since 2013, she focuses on process technology. She is the Group Leader for thin film deposition, and her main interest is the improvement of semiconductor processing including e-beam evaporation, sputtering, ALD, plasma-enhanced chemical vapor deposition, and annealing processes.

Maniteja Bodduluri was born in Ramakrishnapur, India, in 1992. He received the B.Tech. degree in Electronics and Communication Engineering from Jawaharlal Nehru Technological University Kakinada, Kakinada, India, in 2013, and the M.Sc. degree in micro and nano systems from the TU Chemnitz, Chemnitz, Germany, in 2017. From 2016 to 2017, he completed his master's thesis at the Ferdinand-Braun-Institut, Berlin, Germany, entitled Monolithically Integrated Strain Sensors in GaN Technology.

Frank Brunner received the Ph.D. degree in electrical engineering from the University of Karlsruhe, Karlsruhe, Germany, in 2002. Since 2005, he has been responsible for epitaxy of GaN-based microwave transistors at the Ferdinand-Braun-Institut, Berlin, Germany. He is in charge of design and development of (Al,Ga)N-related optoelectronic device structures.

Günter Tränkle received the Ph.D. degree in physics from the University of Stuttgart, Stuttgart, Germany, in 1988. In 1996, he became the Head of the Ferdinand-Braun-Institute, Berlin, Germany. He has been the Chair of microwaves and optoelectronics at Technical University Berlin, Berlin, since 2002. His current research interests include III/V-semiconductor technology, micro- and mm-wave devices, and high-power diode lasers.

Joachim Würfl received the Ph.D. degree in electrical engineering from the Technical University of Darmstadt, Darmstadt, Germany, in 1989. He has been with the Ferdinand-Braun-Institute Berlin since 1992. In 2007, he was appointed Head of the newly implemented business field GaN electronics. He has been the CEO of the spin-off company Berlin Microwave Technologies AG (BeMiTec) since 2008.

Tsu-Jae King Liu
EDS Vice-President of
Publications and Products
tking@eecs.berkeley.edu

2018 EDS George E. Smith Award

A high priority of the Electron Devices Society (EDS) is to recognize and enhance the quality of papers published in EDS archival literature. The George E. Smith Award was established in 2002 to recognize the best paper appearing in a fast turnaround archival publication of EDS, targeted to the *IEEE Electron Device Letters*. Among other criteria including technical excellence, an important metric for selection for the award is comprehensive and impartial referencing of prior art.

The paper winning the 2018 George E. Smith Award was selected from over 400 articles that were published in 2018. The paper is entitled, "Improved Subthreshold Swing and Short Channel Effect in FDSOI n-Channel Negative Capacitance Field Effect Transistors." This paper appeared in the February 2018 issue of the *IEEE Electron Device Letters* and authored by Daewoong Kwon, Korok Chatterjee, Ava J. Tan, Ajay K. Yadav, Hong Zhou, Angada B. Sachid, Roberto Dos Reis, Chenming Hu and Sayeef Salahuddin.

The award will be presented at the plenary session of the International Electron Devices Meeting to be held on December 9, 2019 in San Francisco, CA. In addition to the award certificate, the authors will receive a check for $2,500 to be shared equally among all authors. On behalf of the Electron Devices Society, I would like to congratulate the authors for this achievement. Brief biographies of some of the authors follow.

Chenming Hu is a Professor at UC Berkeley and formerly the Chief Technology Officer of TSMC. He led the development of FinFET–the 3D transistor which enabled scaling beyond 20nm, and the industry-standard transistor model (BSIM) used in the design of over one trillion dollars worth of ICs. He has received the IEEE Nishizawa Medal, Solid State Circuits Award and Jack Morton Award; the EDA industry's Phil Kaufman Award and UC Berkeley's highest honor for teaching—the Berkeley Distinguished Teaching Award. He is a member of the US National Academy of Engineering and the Chinese Academy of Sciences. In 2016, President Obama presented to him the US National Medal of Technology and Innovation.

Dae Woong Kwon received Ph.D. degrees in Electrical Engineering at Seoul National University, Korea, in 2017. He designed NAND flash memory from 2005 to 2014 at Samsung Electronics, Korea. He joined UC Berkeley from 2017 to 2019, as a Post-Doctoral Fellow. He joined Intel, Folsom, USA, in 2009.

Roberto dos Reis is specialized in advanced structural characterization of using TEM techniques. As Research Assistant Professor at Northwestern University, he focuses in developing and applying experimental TEM-based methods to convey a direct relationship between properties and atomic structure by combining high spatial resolution, precision, and chemical sensitivity.

Korok Chatterjee received the B.S. and Ph.D. degrees in electrical engineering and computer sciences from the University of California Berkeley, Berkeley, CA, USA, in 2011 and 2018, respectively, where he is currently a postdoctoral researcher. His current research interests include the use of ferroelectric phenomena in the design of novel electron devices.

Angada B. Sachid (PhD – IIT Bombay 2010; Postdoc/Scientist – UC Berkeley 2018) is currently the Director and Distinguished Member of Technical Staff in the Design Technology Group at Applied Materials, USA. His research interests include ultra-low power FETs, DTCO, materials-to-systems connectivity, bio sensors, emerging memories and neural-inspired computing.

S. Salahuddin is a professor of Electrical Engineering and Computer Sciences at the University of California Berkeley. His work has focused mostly on conceptualization and exploration of novel device physics for low power electronic and spintronic devices. Salahuddin has received the Presidential Early Career Award for Scientist and Engineers (PECASE). Salahuddin also received a number of other awards including the NSF CAREER award, the IEEE Nanotechnology Early Career Award, the Young Investigator Awards from the Air Force Office of Scientific Research (AFOSR) and the Army Research Office (ARO) and best paper awards from IEEE Transactions on VLSI Systems and from the VLSI-TSA conference. In 2012, Applied Physics Letters (APL) highlighted two of his papers among 50 most notable papers among all areas published in APL within 2009–2012. Salahuddin is a co-director of the Berkeley Device Modeling Center (BDMC) and Berkeley Center for Negative Capacitance Transistors (BCNCT). Salahuddin is also a co-director of ASCENT, one of the six centers of the JUMP initiative sponsored by SRC/DARPA. He served on the editorial board of IEEE Electron Devices Letters (2013–16) and was the chair the IEEE Electron Devices Society

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2020 IEEE EDS William R. Cherry Award Call For Nominations

The IEEE Electron Devices Society invites the submission of nominations for the 2020 William R. Cherry Award.

This award is named in honor of William R. Cherry, a founder of the photovoltaic community. In the 1950's, he was instrumental in establishing solar cells as the ideal power source for space satellites and for recognizing, advocating, and nurturing the use of photovoltaic systems for terrestrial applications. The William R. Cherry award was instituted in 1980, shortly after his death. The purpose of the award is to recognize an individual engineer or scientist who devoted a part of their professional life to the advancement of the science and technology of photovoltaic energy conversion.

The award consists of a plaque, monetary award, recognition and a dedicated Cherry Award Talk during the Photovoltaic Specialists Conference.

Nominate: William R. Cherry Award online nomination form: https:// **Get updated web address

Submission Deadline: January 15, 2020

For more information: http://www.ieee-pvsc.org/PVSC47/awards-cherry.php

Electron Devices Society Members Named Recipients Of 2019 IEEE Medals

Two EDS members were named 2019 IEEE Medal award winners. Please be sure to visit IEEE.tv http://ieeetv.ieee.org/ to view the award presentations and acceptance speeches.

2019 IEEE Medal of Honor

Kurt E. Petersen

Kurt E. Petersen, has been named as the recipient of the 2019 IEEE Medal of Honor. The citation states, *"For contributions to and leadership in the development and commercialization of innovative technologies in the field of MEMS."*

Kurt E. Petersen's foundational work on microelectromechanical systems (MEMS) helped unify and provide direction for the field, and his commercialization of MEMS technologies has continued to transform the field to realize the many applications we take for granted today. MEMS involve miniature mechanical and electromechanical elements, such as sensors, actuators, and other microelectronics, merged onto a common silicon substrate along with integrated circuits. MEMS-based devices provide important functionality in today's smart phones, medical devices, and smart automotive and smart human-machine interface applications. It was Petersen's 1982 seminal review paper "Silicon as a Mechanical Material" that helped lay the foundation for future MEMS research. It summarized all the mechanical properties of silicon as well as mechanical devices made on silicon chips at that time and also anticipated future devices. Prior to this work, MEMS research consisted of many unconnected and unrelated efforts. Petersen's paper provided the diverse group of MEMS researchers with a unified vision and

a sense of community in which to develop the MEMS industry as we know it today. Petersen was also instrumental in establishing forums for the MEMS academic, industrial, and government communities to share and discuss their work. In 1984, he served as the first program chairperson for the biennial Solid-State Sensors, Actuators, and Microsystems regional workshop. In 1987, he was the first co-chairperson of the yearly International Conference on MEMS.

Petersen has played a significant role in developing innovative MEMS tools, co-founding six companies to commercialize his ideas. At NovaSensor (co-founded in 1985), Petersen led the development of a disposable pressure sensor for blood pressure monitoring during and after surgical operations. NovaSensor was also the first to commercialize the revolutionary silicon fusion bonding (SFB) and deep reactive ion etching (DRIE) fabrication processes. Practically all of today's MEMS high-volume products use a variation of these processes. In 1996, he co-founded Cepheid, where he developed a totally automated, microfluidic system to test for anthrax in the U.S. mail system. Other MEMS diagnostic tests commercialized by Cepheid have transformed the molecular diagnostics industry using microfluidics and the polymerase chain reaction. Petersen became the founding chief executive officer of SiTime in 2004. SiTime commercialized MEMS devices that outperform quartz crystal oscillators for timing applications, and its products can be found in many consumer mobile devices. Petersen co-founded both Profusa and Verreon in 2008. Profusa's small, flexible hydrogel implant for glucose sensing is causing the medical industry to change how it thinks about measuring chemicals in the body. Projects at Verreon were focused on the development of MEMS sensors and actuators on glass substrates instead of silicon to take advantage of cost efficiencies and the potential for use in the flat-panel display industry. In 2011, Petersen joined the Silicon Valley Band of Angels, which is an investment group comprised of former and current high-tech executives that funds and mentors early stage, high-tech start-up companies. Today, he spends most of his time helping and mentoring such companies, and he gives many invited talks around the world on MEMS and on entrepreneurial trends.

An IEEE Life Fellow and member of the U.S. National Academy of Engineering, Petersen is currently a member of the Silicon Valley Band of Angels and resides in Milpitas, CA, USA.

2019 IEEE Jun-Ichi Nishizawa Medal

Pallab Bhattacharya

Pallab Bhattacharya, has been named as a co-recipient of the 2019 IEEE Jun-Ichi Nishizawa Medal. The citation states, "For contributions to the development and commercialization of quantum dot lasers."

The pioneering and continued efforts of Yasuhiko Arakawa, Pallab Bhattacharya, and Dieter Bimberg enabled the scientific and technological marvel known as the quantum dot (QD) laser, which is replacing semiconductor lasers in a growing range of areas including optical communications, medical and industrial applications, and silicon photonics. Their contributions provide the basis for the development of advanced systems for data- and telecommunications and quantum cryptography. The successful operation of the QD laser depended on the realization of nanostructured atom-like quantum dots in the gain region, but the technology for this did not exist. Arakawa, Bhattacharya, and Bimberg's groups solved this problem by creating a laser that has vastly superior characteristics compared to traditional semiconductor lasers, including those on silicon substrates by the first two. In 1982, Arakawa proposed the concept of the QD laser and theoretically showed temperature insensitivity of threshold current in the device. He experimentally demonstrated the reduced temperature dependence of threshold current using high magnetic fields and also forecasted theoretically enhanced modulation dynamics and reduced spectral linewidth. He then worked on developing high-performance QD lasers, demonstrating temperature-insensitive QD lasers, and contributed to their first commercialization. Bhattacharya turned his attention to QD lasers in the 1980s when his group accidently observed the formation of self-organized QDs in the strained channel region of high-speed modulation doped transistors. His group was one of the first to report a room-temperature QD laser, and he also demonstrated the laser's temperature-invariant operation, near-zero chirp, and high-speed modulation, as well as the first III-nitride-based QD lasers and LEDs with emission in the entire R-B-G wavelength range for displays. Bimberg demonstrated the first low- and room-temperature injection lasers based on self-organized quantum dots. He pioneered the general effective mass, 8-band k.p and many particle theories of quantum dots presenting the basis to understand the electronic, optical, and transport properties of QDs and QD devices. His fundamental discovery of the relevance of strain for self-organized growth, established novel growth technologies for devices with properties superior to those of quantum-well structures.

An IEEE Life Fellow and foreign member of the U.S. National Academy of Engineering, Arakawa is a Specially Appointed Professor and Professor Emeritus with The University of Tokyo, Tokyo, Japan.

An IEEE Life Fellow, a member of the U.S. National Academy of Engineering and a Fellow of the National Academy of Inventors, Bhattacharya is the Charles M. Vest Distinguished University Professor and James R. Mellor Professor of Engineering with the University of Michigan, Ann Arbor, MI, USA.

An IEEE Life Fellow, member of the German and Russian Academies of Sciences, and foreign member of the U.S. National Academies of Engineering and Inventors, Bimberg is executive director of the "Bimberg Chinese-German Center for Green Photonics" of the Chinese Academy of Sciences at CIOMP, Changchun, China.

Samar Saha
EDS Awards Chair
Prospicient Devices
Milpitas, CA, USA

EDS Members Recently Elected to IEEE Senior Member Grade

The IEEE Electron Devices Society would like to recognize the excellence of its valued members, especially when they have performed for a long time at a particularly high-quality level.

Congratulations to the following EDS members who have recently become IEEE Senior Members.

Andreas Aal
Zlatan Aksamija
German Alvarez-Botero
Kristoffer Andersson
N.B. Balamurugan
Andreas Bett
Harish Bhaskaran
Ronald Birkhahn
Sindhu Preetham Burugupally
Adilson Cardoso
Youngcheol Chae
Premjeet Chahal
Kimara Chin
Daniel Durini
Lisa Edge
Dina El-Damak
Shahrokh Farhangi
Vasilis Fthenakis
Takafumi Fukushima
Manel Gasulla
Salvador Gimenez
Michele Goano
Edward Greer
Koushik Guha
Qiang Guo
Mina Hanna
Hashimah Hashim
Bahman Hekmatshoar
Geert Hellings
Masataka Higashiwaki
Tsuyoshi Horikawa
Wen Huang
Amit Jha
Jungwoo Joh
Andrew Kelly
Dylan Kelly
Pranita Kerber
Chang-Jin Kim
Kazutoshi Kobayashi
Gilles S. C. Lamant
Yan Li
Chih-Ting Lin
Shibing Long
Josef Lutz
W. Gregory Lyons
Negin Manavizadeh
Alessandro Marchioro
William Martino
Hideaki Matsuzaki
Arnan Mitchell
Sushanta Mohapatra
Youichi Momiyama
Jay Morreale
Tanya Nigam
Nikolaos Papandreou
Adam Payne
Yuriy Prokopenko
Enrique
Quiroga Gonzalez
Vishwanath Ramachandran
Stephen Ramey
S. Rathod
Cristian Ravariu
Carlos Sampedro Matarin
Berardi Sensale
Guneet Sethi
Aditya Shah
Bikash Sharma
Zhou Shudong
Radu Sporea
Derek Stewart
Anders Sunesson
Akil Sutton
Fazal Talukdar
Chuan Seng Tan
Ioannis Tigelis
Suman Tripathi
Christos Tsamis
Tetsuzo Ueda
Jan Vandenbussche
Han Wang
Seamus Whiston
Donald Whitney
Bingxi Wood
Feng Yan
Zhuoqing Yang
Kiyokazu Yasuda
Chunhua Zhou
Wenjuan Zhu

Do you know an outstanding IEEE member who is not yet an IEEE Senior Member?

Do you feel that you are qualified for such recognition?

Are you interested in becoming a Senior Member or nominating a fellow IEEE Member?

Visit the IEEE website for an application and for qualification requirements: https://www.ieee.org/membership/senior/

Please designate the IEEE Electron Devices Society as your nominating entity!

IEEE YP GERMANY—ELECTIONS

BY MIKE SCHWARZ

The IEEE Young Professionals Germany affinity group has elected new ExCom members. An exciting new leadership team has been built to establish YP activities in Germany.

The new ExCom consists of:

- Chair-Ali Aboosaidi (in-tech GmbH)
- Vice Chair-Mike Schwarz (Robert Bosch GmbH)
- Treasurer-Ahmed Hussein (IAV GmbH)
- MAG Lead-Siwei Bai (TU München)
- Secretary-Sevda Abadpour (Karlsruhe Institute of Technology (KIT))
- Activities Lead-Alan Blumenstein (AKKA Technologies)

Further information available at https://www.ieee.de/affinity-groups/young-professionals.html

Here are some brief infos of the new ExCom:

Ali Aboosaidi received his Bachelor of Science Degree in Electrical Engineering, from Western Washington University, Washington United States in 2017. During the years in his University, he held multiple leadership positions in the IEEE student chapter, was inducted into the honors society HKNEta Kappa Nu Mu Zeta chapter where he also held a leadership role, and organized the first ever student field trip to the CES tradeshow taking place in Las Vegas, NV. Ali is currently a consulting engineer in the mobile power solutions industry in Munich, Germany. Ali is also actively involved in organizing professional conferences such as the IEEE Rising Stars Conference, taking place in Las Vegas, Nevada. Ali has a background in establishing organizations such as Project EVA, entrepreneurship, and building teams.He enjoys influencing tomorrows cutting edge technologies, bringing people together and public speaking.

Mike Schwarz received the Diploma degree from the University of Applied Sciences Giessen-Friedberg, Giessen, Germany, in 2008 and the M.S. degree in electrical engineering from the Universitat Rovira i Virgili, Tarragona, Spain, in 2009. During 2008-2013, he was Research Assistant—Ph.D. student at Device Modeling Research Group, Competence Center for Nanotechnology and Photonics, Technische Hochschule Mittelhessen, Giessen, Germany. He received his Ph.D. degree with honors from the Universitat Rovira i Virgili in October 2012 on the subjectof compact modeling of Schottky barrier multiple-gate FETs.

Mike was the recipient of the Friedrich Dessauer Prize for the best diploma thesis about multiclass support vector machines in 2008 and the URV Graduated Student Meeting on Electronic Engineering Award for the best oral presentation for a paper about an analytical model for the electric field in Schottky barrier double-gate MOSFETs in 2010. Since 2013 Mike is with the Robert Bosch GmbH, working in the research and development department on design, modeling and simulation of MEMS sensors and systems. Mike has at present 116 publications, 59 conference papers, 18 journal articles, and 39 patents.

He is committed to volunteering work within IEEE, as he is Member of the IEEE Young Professionals, Vice-Chair of the IEEE Young Professionals Germany Section, Editor Western Europe EDS newsletter, TPC MIXDES, TPC QCIT.

His current research interests are simulation and compact modeling of Schottky Barrier MOSFET devices and simulation and compact modeling of neuromorphic applications and devices as well as development of simulation methodologies for MEMS sensor devices.

Ahmed Hussein has received his Bachelor of Science Degree in Mechatronics Engineering from the German University in Cairo (GUC), Egypt, in June 2012; followed by his Master of Science Degree in Mechatronics Engineering from the German University in Cairo (GUC), Berlin campus, Germany, working on optimization of multiple robot systems cooperation in May 2013. In September 2018, he received his PhD Degree in Electrical Engineering, Electronics and Automation from Universidad Carlos III de Madrid (UC3M), Spain. During the doctoral degree period, he was working with the Intelligent Systems Lab (LSI) research group, where he was one of the team leaders of the Intelligent Campus Automobile (iCab) project, working on the development and implementation of localization, mapping, planning, control,

communication and cooperative driving techniques for multiple self-driving vehicles. Currently he is a Senior Development Engineer in the Department of Perception & Camera Functions at IAV GmbH in Berlin, Germany.

His research interests are focused on intelligent transportation systems fields, mainly on sensors data fusion, autonomous systems control, optimization techniques, computational intelligence and cooperative vehicles systems. Recently, his research interests also include computer vision, deep learning and development of perception systems based on camera and lidar data for object detection, recognition and classification.

Siwei Bai is a biomedical engineer with a multidisciplinary background, and an early-career researcher with an emerging track record in the research and development of medical devices and computational modelling of biological systems. He received his PhD on biomedical engineering at the University of New South Wales in Australia, focusing on developing computer models of transcranial electrical stimulation. Currently, he is working as Postdoctoral Research Fellow at the Technical University of Munich in Germany, and at the same time Adjunct Associate Lecturer at the University of New South Wales. His project involves developing computational models of the human cochlea for refining the design of cochlear implants. He has been awarded several prestigious grants from various grant bodies, including a Postdoctoral Research Fellowship from the Alexander von Humboldt Foundation, and a Marie Skłodowska-Curie Individual Fellowship from the European Commission. In addition, he is a co-investigator in two Project Grants offered by the Australian National Health & Medical Research Council, as well as in a D-A-CH Project Grant offered by the German Research Foundation.

Sevda Abadpour received the M.Sc. degree from Amirkabir university of Technology (AUT) Tehran, Iran, in 2011 in Electrical Engineering. Her research fields in Bachelor and Masterwere circuit design and Electromagnetic Compatibility (EMC), respectively. From 2011 to 2013, she was with Iran Telecommunication Research Center (Research Institute for Information and Communication Technology (ICT)), Tehran, Iran as a research assistant in Satellite Communications Group. Then she was Technical Manager in MizanGostar-Rayaneh, Tehran, Iran from 2013–2014. From 2014 to 2017, she was Quality Manager in Institute of Telecommunication and Applied Electromagnetics in Amirkabir University of Technology (AUT), Tehran, Iran. The research study of Institute of Telecommunication and Applied Electromagnetics is the EMC tests for the device under design. In September 2017, she became a research assistant in Institute of Radio Frequency Engineering and Electronics (IHE), KIT, Karlsruhe, Germany. Her research filed is Automotive Radar and especially wave propagation in automotive radar communication.

S. Abadpour's research interests are in the broad area of high-frequency integrated circuits and systems and she has authored six publications in this field. She is a student member of IEEE from 2005 and student member of Antenna wave propagation, also. Her main areas of specialization are: Wave propagation, Mathematical Modeling and Computational and Numerical Electromagnetics, RF/Microwave and Millimeter-Wave Circuits and Devices.

Alan Blumenstein made his bachelor degree in the Universidad Nacional De Asuncion, Paraguay in the area of Mechatronics and his master degree in Universidad de Oviedo and the Karlsruhe University of Applied Sciences in the area of Mechatronics and Micro-Mechatronics Systems. During his bachelor he was involved in the creation of the first student branch of Paraguay, (Universidad Nacional de Asuncion), he was vice president and president of it, he helped with the organization of National Branch reunion of Argentina and the third National Sumo Robot competition and beside that he represented the students of mechatronics as president of them and also as career coordinator and also as a Assistant Professor in several subjects, after that he got involved on the creation of the Paraguayan section, he helped on the creation of the section, he was also in charge of the awards in the section and also in charge of the first ever National Robotic Competition and also the first edition of the National congress of Paraguay, Aranducon. During his master degree he was shortly involved with the student branch of Universidad de Oviedo. As a professional Alan was in charge of the robotic laboratory of the Universidad Nacional de Asuncion, and started his own company Dedalo that worked mostly in the area of non-conventional marketing. Today Alan works in AKKA DSW as an embedded software developer in areas such as automotive, IoT and Medicine. He is an appassionato in robotics and Astrophysics, he enjoys learning about new technologies such as quantum computer and Artificial Intelligence.

CALL FOR NOMINATIONS
2018-2019 IEEE Electron Devices Society
Region 9 Biennial Outstanding Student Paper Award

Description: Awarded to promote, recognize, and support meritorious research achievement on the part of Region 9 (Latin America and the Caribbean) students, and their advisors, through the public recognition of their published work, within the Electron Devices Society's field of interest: All aspects of the physics, engineering, theory and phenomena of electron and ion devices such as elemental and compound semiconductor devices, organic and other emerging materials based devices, quantum effect devices, optical devices, displays and imaging devices, photovoltaics, solid-state sensors and actuators, solid-state power devices, high frequency devices, micromechanics, tubes and other vacuum devices. The society is concerned with research, development, design, and manufacture related to the materials, processing, technology, and applications of such devices, and the scientific, technical and other activities that contribute to the advancement of this field.

Prize: A distinction will be conferred in the form of an Award certificate bestowed upon the most outstanding Student Paper nominated for the two-year period. The prize will be presented at either the Latin American Electron Devices Conference (LAEDC) or the Symposium on Microelectronics Technology and Devices (SBMicro). In addition to the recognition certificate, the recipient will receive a subsidy of up to $1,500 to attend the conference, where the award is to be presented. There will be a formal announcement of the winner in a future issue of the EDS Newsletter. The winner will also receive up to three years of complimentary IEEE and EDS student membership, as long as winner remains eligible for student membership.

Eligibility: Nominee must be enrolled at a higher education institution located in Region 9. In the case of a co-authored paper, only eligible co-authors may be nominated. Papers should be written in English on an electron devices related topic. Papers should have been published, in full-feature form, during 2018-2019 in an internationally recognized IEEE sponsored journal or conference in the field of electron devices related topics. Statements by the student and by the faculty advisor should accompany the nomination. Nominator must be an IEEE EDS member. Previous winners of this award are ineligible. There must be a minimum of five nominations submitted in order for the award to be administered for that year.

Basis for Judging: Demonstration of Nominee's significant ability to perform outstanding research and report its results in the field of electron devices. Papers will be judged on: technical content merit, originality, structure, clarity of composition, writing skills, overall presentation. These criteria will be weighted by the assessment of the nominee's personal contribution and the linkage of the nominated work to the nominee's career plans.

Nomination Package:
- Nominating letter by an EDS member (it may be the faculty advisor)
- A brief one-page (maximum) biographical sketch of the student
- 1000 words (maximum) statement by the nominated student describing the significance and repercussion of the nominated work within the wider scope of the nominee's career plans
- 400 words (maximum) statement by the faculty advisor under whose guidance the nominated work was carried out. It should unmistakably state the faculty advisor's support of the nomination, and clearly explain the extent of the nominated student's contribution, as well as its relevance for the overall success of the reported work.
- A copy of the published paper

Timetable:
- Nomination packages are due at the EDS Executive Office no later than **15 February 2020.**
- Nomination packages can be submitted by mail, fax or e-mail, but a hard copy must be received at the EDS Office
- Winners will be notified by 15 March 2020.
- Recipients may choose to have the formal presentation of the award at either one of the conferences: LAEDC 2020 or SBMicro 2020

Send completed package to:
IEEE Operations Center
EDS Executive Office
EDS R9 Outstanding Student Paper Award
445 Hoes Lane, Piscataway, NJ 08854 USA

For more information contact:
Laura Riello, EDS Executive Office
l.riello@ieee.org or 732-562-3927

SOLID-STATE CIRCUITS SOCIETY
Where ICs are in IEEE

IEEE SSCS International Student Circuits Video Contest

Submission Deadline: December 15, 2019

WHAT: Create fun short (5-minute to 10-minute) videos that explain circuits

AUDIENCE: High school students

HOW: Tell a story that uses drawings, cartoons, and analogies to connect a circuits topic to a real-world application.

This **example video** about Machine Learning shows the style of video: https://youtu.be/ZmBUnJ7lGvQ

STORY TEMPLATE:

Think about telling a story to connect your audience to the circuits concept you chose in a way that they can understand. The template below is a suggested approach for formulating your story, but creative alternatives are encouraged:

1. Students pick a circuits topic (e.g., ADC, Low power digital, RF TX ...)
2. Begin your video by describing a compelling application (link to the real world)
3. Define a step-by-step connection from the application to the circuit
4. Explain how the circuit works, at an appropriate level for the audience
5. Revisit the impact at the application level

The objective of this contest is to excite students about circuit design and its impact on important applications. Submissions are solicited by both undergraduate and graduate students who are currently enrolled in a college or university.

SUBMISSION GUIDELINES:

The submission deadline is December 15, 2019.

All video submissions must be posted online (e.g., on YouTube or a similar site) and then submitted using the form at this link: https://app.smartsheet.com/b/form/df8d23562694492381af4f8224e875e9

Video submissions should:

- Motivate a real-world application of circuits
- Give clear step-by-step explanations with animated figures
- Be clear and appealing to high-school students
- Be about ~5 minutes in length (10 minutes maximum)

A committee will post selected videos to an SSCS channel, where SSCS members and the public can vote on their favorites by "liking" the video. Three videos will receive awards and the voting results will be one of the criteria to win the awards. Voting will conclude by March 2020.

Students who submit videos that are selected for voting will receive one year of free SSCS membership.

ELIGIBILITY:

This contest is open to undergraduate and graduate students who are currently enrolled in a college or university. IEEE and/or SSCS membership is NOT a requirement to enter this contest.

AWARDS:

Up to three contestants will receive US$2K each towards attending an SSCS-sponsored conference (ISSCC, CICC, ESSCIRC, VLSI Symp., A-SSCC). The number of "Likes" will be one of the criteria for selecting the awardees so make sure your video has broad appeal and catches the attention of the public. This award is paid either as a reimbursement following the attended conference or will be paid directly to the conference for registration and to the hotel for accommodations. Winners will have their names highlighted in the Solid-State Circuits Magazine.

RULES AND REGULATIONS:

Please be sure to read the contest guidelines, rules, and regulations - Click here to access.

If you have any questions, please email sscs_contest@ieee.org.

START YOUR SUBMISSION NOW!

Enter Now

SSCS and EDS Student and Young Professionals Mentoring Event at VLSI 2019

By Abira Altvater

The Young Professional (YP) members of the IEEE Solid-State Circuits Society (SSCS) and the IEEE Electron Devices Society (EDS) enjoyed food, drink, and friendly conversation at the Young Professionals, Faculty, and Students Micro-Mentoring Session at the 2019 Symposia on VLSI Technology and Circuits on 10 June in Kyoto, Japan.

The event was kicked off with a welcome and presentation about the numerous benefits of SSCS membership by Emre Ayranci, SSCS Secretary. SSCS and EDS Leaders—who acted as the mentors—went around the room and described their academic and career journeys and how being an SSCS, EDS, and IEEE member has benefited them and shaped them.

Since there were people at all different stages in their careers at the event, the YP's and mentors had a lot to discuss. Mentors gave mentees advice on topics such as entrepreneurship, going into academia vs. industry, work/life balance, journal authorship, and much more.

For details on the next SSCS mentoring event, check the SSCS website.

SSCS and EDS Students, Young Professionals, and Mentors at the Mentoring Event at VLSI 2019

Diversity Luncheon at VLSI 2019

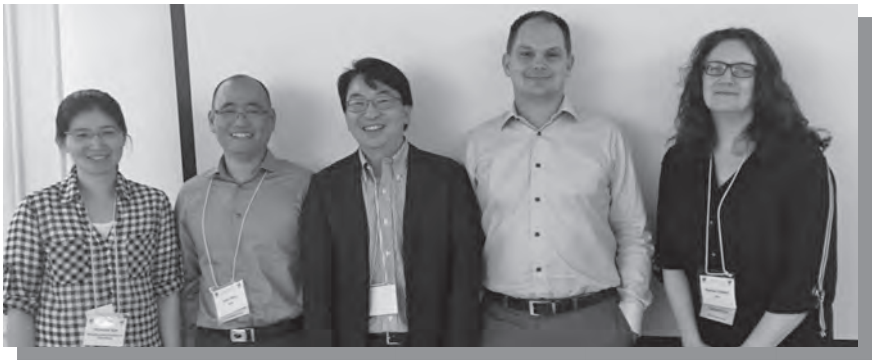
By Danielle Griffith

The IEEE Solid-State Circuits Society (SSCS) and the IEEE Electron Devices Society (EDS) hosted a diversity luncheon at the 2019 Symposium on Very Large Scale Integration (VLSI) Technology and Circuits in Kyoto, Japan. Seventy people attended a networking lunch followed by a panel discussion. The focus of the event was to examine ways to increase diversity within the devices and circuits community. Nadine Collaert of IMEC moderated the event. The first guest speaker was Professor Makoto Nagata from Kobe University who discussed how the university used different methods to increase female enrollment in the engineering program. These methods included emphasizing the end-use case of products being developed instead of concentrating on just the integrated circuit design itself. Vivienne Sze, associate professor in the Electrical Engineering and Computer Science Department at MIT, spoke next. Professor Sze outlined the problems of implicit bias for women and minorities in engineering. She also discussed issues associated with impostor syndrome, whereby individuals perceive themselves as undeserving of their accomplishments, and are filled with fear and doubt about their abilities, regardless of actual demonstrated competence. The next invited speaker was John Wuu, a Fellow at AMD who described a program he led while at Hewlett-Packard that worked with local high schools to increase interest in engineering careers by providing practical work experience. The last invited speaker was Dr. Todd Waterman, Director at Texas Instruments who described the increased focus that TI has been directing towards improving diversity, particularly in the last few years.

Numerous excellent suggestions were proposed in the question and answer session following the talks by the panelists. These included developing a system of formalized mentors who could ensure that underserved groups could turn to a dedicated advocate for assistance, using software

to rewrite job descriptions to be more inclusive and welcoming to all people, and ensuring diversity in interviewers during the recruitment process. One point that was stressed was that support from first line managers is critical to ensuring a successful diversity program. Improving diversity is seen not as an action taken by a human resources department, but rather as a priority within all business units.

The diversity luncheon was well attended and participants were fully engaged on the topic of ways of increasing diversity in the devices and circuits community. The four guest speakers contributed valuable insight into not only the challenges but also the benefits of improving diversity in their respective organizations. All agreed that maintaining an open dialog in the form of future events like these will help to bring about a much better engineering environment for everyone.



The Diversity Luncheon panelists and moderator: From left to right, Panelists Vivienne Sze, John Wuu, Makoto Nagata, and Todd Waterman with Moderator Nadine Collaert

A full house at the Diversity Luncheon at VLSI 2019 in Kyoto, Japan

Message from the Editor-in-Chief

(continued from page 23)

considered a marvel. See in that respect the cited comments by Colin McAndrew (Page 8, third column) and by Larry Nagel (page 9, first column), two colleagues who had no personal stakes in MOS compact modeling but had been involved in the field throughout their career. I hope that this explains our approach and can help clarify your concerns."

Both Dr. Burghartz and Professor Yang subsequently agreed that an excerpted summary of their comments by the EIC be published in the next issue of the Newsletter.

2018 EDS George E. Smith Award

(continued from page 25)

committee on Nanotechnology (2014–16). Salahuddin is a Fellow of IEEE.

Ava J. Tan is a PhD student at the University of California, Berkeley. She received her B.S. from Cornell University in 2016. Her research focuses on the development of CMOS compatible ferroelectrics for novel nonvolatile memories and hardware to support emerging computing paradigms.

Ajay K. Yadav received his Ph.D. from the University of California, Berkeley. He completed his B.S. from Indian Institute of Technology Kanpur (India) in 2009. His research focuses on developing materials for different applications such as non-volatile memories.

Tsu-Jae King Liu
EDS Vice-President of Publications and Products
tking@eecs.berkeley.edu

Chapter News

IEEE EDS Mini-Colloquium on Photovoltaics

by Susthitha Menon

Two EDS technical committee sponsored mini-colloquiums on photovoltaics were held in Malaysia in April 2019. The lectures were delivered by EDS Distinguished Lecturers; Dr. Lawrence L. Kazmerski, an IEEE Fellow and an Emeritus Research Staff Member from the National Renewable Energy Laboratory (NREL), Colorado, and a research professor at the University of Colorado, Boulder, with the Renewable and Sustainable Energy Institute (RASEI) with his talk on Photovoltaics History, Technology, and Progress: The Future is Now…; Dr. Anil Kottantharayil from the Centre of Research in Nanotechnology and Science, Indian Institute of Technology (IIT) Bomba,y with his talk on PV Module Performance Loss due to Degradation and Soiling; and Dr. Vikram Dalal, an IEEE Fellow and Distinguished Professor from the Electrical and Computer Engineering, Iowa State University, USA, with his talk, Perovskite solar cells: The new frontier for photovoltaic device.

The first MQ was held on April 9, 2019 at Universiti Kebangsaan Malaysia (UKM) Bangi, Selangor. and was organized by the ED Malaysia (Kuala Lumpur) Chapter and was co-organized by IMEN, UKM and the IEEE ED UKM Student Branch. The MQ was officiated by the ED Malaysia chapter advisor, Professor Dato' Dr. Burhanuddin Yeop Majlis and the EDS Vice President of Regions and Chapter, Dr. M.K. Radhakrishnan. The MQ in Kuala Lumpur also included talks by four esteemed local academics, Associate Dr. Azrul Azlan Hamzah, Dr. Norhayati Soin, Professor Nowshad Amin, and Associate Professor Mohd Nizar Hamidon. All speakers shared their research expertise on applications of photovoltaics and nanoelectronics. A total of 66 participants attended the MQ. Research posters by participants were also exhibited during the event. The chapter also had a booth at the event to promote IEEE membership.

Meanwhile, the ED/MTT/SSC Penang Chapter successfully organized a similar MQ at the Penang Skills Development Center (PSDC) on April 11, 2019, in collaboration with the electronic engineering technical division (eETD) of The Institution of Engineers, Malaysia (IEM), also with support from the ED Malaysia Chapter. The mini-colloquium was attended by 31 engineers, technologists and researchers and was moderated by Dr. Jagadheswaran Rajendran, Vice Chair of IEEE Penang Chapter. It was an informative talk where the DL speakers depicted the road map, status of R&D, markets, manufacturing, and investments of photovoltaic technology. The MQ adjourned with interactive Q&A as some participants are practicing engineers involved in the PV business. The Penang Chapter Chair, Ir. Bernard Lim, also presented certificates of appreciation to speakers.

EDS chapters would like to thank EDS photovoltaics technical committee chair, Prof. Juzer Vasi, for providing the opportunity for the MQs to be held in Malaysia for the benefit of EDS members here.

TC-sponsored MQ by EDS Penang Joint Chapter

TC-sponsored MQ by EDS Malaysia Kuala Lumpur and EDS UKM Student Branch

26th International Conference "Mixed Design of Integrated Circuits and Systems"—MIXDES 2019

By Marcin Janicki

On June 27–29, 2019, Rzeszów, Poland, the International Conference MIXDES 2019 took place. The event was organized by the Lodz University of Technology together with the Warsaw University of Technology. The conference was co-sponsored by Poland Section IEEE ED & CAS Societies, Polish Academy of Sciences (Section of Microelectronics and Electron Technology), and Commission of Electronics and Photonics of Polish National Committee of International Union of Radio Science—URSI.

The 3-day conference program included 97 presentations from 28 countries. The following six general invited talks were presented during the conference plenary sessions:

- *Advanced MOS Device Technology for Low Power Logic LSI*
  Shinichi Takagi (The University of Tokyo, Japan)
- *Quantum Bits and Quantum Computing Architecture*
  Farzan Jazaeri (EPFL, Switzerland)

Prof. Shinici Takagi giving invited talk

- *Towards Energy-Autonomous Integrated Systems Through Ultra-low Voltage Analog IC Design*
  Viera Stopjaková (Slovak University of Technology in Bratislava, Slovakia)
- *THz Technologies and Applications*
  Thomas Skotnicki (Institute of High Pressure Physics PAS, Poland)
- *What is Killing Moore's Law? Challenges in Advanced FinFET Technology Integration*
  Arkadiusz Malinowski (GLOBALFOUNDRIES, USA)
- *Yield and Reliability Challenges at 7nm and Below*
  Andrzej Strojwąs (Carnegie Mellon University, USA)

The sessions also included presentations in the frame of four special sessions:

- *Compact Modeling for Nanoelectronics*
  organized by D. Tomaszewski (Institute of Electron Technology, Poland) and W. Grabiński (GMC, Switzerland)
- *Intelligent Distributed Systems*
  organized by M. Drozd (LTC Sp. z o.o., Poland), R. Sztoch, P. Sztoch (FINN Sp. z o.o., Poland), B. Sakowicz and D. Makowski (Lodz University of Technology, Poland)

Tourist activities (Łańcut Castle)

- *Large Scale Research Facilities* organized by A. Napieralski, W. Cichalewski (Lodz University of Technology, Poland)
- *Thermonuclear Fusion Projects* organized by S. Simrock (ITER, France), D. Makowski (Lodz University of Technology, Poland), D. Bocian and M. Scholz (Institute of Nuclear Physics, Poland)

The next MIXDES 2020 Conference will take place in Wrocław, Poland. The Preliminary Call for Papers is available at http://www.mixdes.org/downloads/call2020.pdf. More information about the past and next MIXDES Conferences can be found at http://www.mixdes.org.

Edited by Mariusz Orlikowski
MIXDES 2019 Conference Secretary

2019 IEEE Electronic Endeavor Match

by Yang Chai

On April 27, 2019, the ED/SSC Hong Kong Chapter held the 3rd IEEE Electronic Endeavor Match. The year the match was hosted at the Hong Kong University of Science and Technology (HKUST) and co-organized by the Academy of Bright Future Young Engineers of HKUST. The IEEE Electronic Endeavor Match is aimed to recognize primary and secondary school students who have developed their interest and skill in constructing electronic circuits.

A total of 98 participants, from different elementary and middle schools in Hong Kong, were divided into 3 different groups according to their age. This year, contestants from Shenzhen, a nearby city also participated in the match, expanding it from a local event to a regional event. After competing in two different phases, the committee selected 3 awardees and the best design award from each group. The students exhibited their interest in electronic circuits and provided positive feedback on this event. More information about the match can be found on http://www.ieee-elex.org/eem.

During the competition

~Ming Liu, Editor

26th International Symposium on Nano Device Technology (SNDT)

by Wen-Kuan Yeh

The ED Tainan Chapter organized the 26th International Symposium on Nano Device Technology (SNDT) at Taiwan Semiconductor Research Institute (TSRI), HsinChu, Taiwan on April 26, 2019. This year's SNDT focused on "The trend for nano device and material." The following two keynote speakers were invited to give Distinguished Lectures: "IC Technology—The Roadmap Going Forward," by Dr. Philip Wong, Vice President of Taiwan Semiconductor

Manufacturing Company; and "Challenges and opportunities of ferroelectric-HfO2 based transistor and memory technologies," by Masaharu Kobayashi, Professor, University of Tokyo.

Another 12 invited speakers from Taiwan, Japan, and Europe were invited to give excellent speeches. There were more than 200 attendees, including professors, IEEE members, students and local professionals in Taiwan attended SNDT 2019. For more information on the program, please visit the website at http://sndt.ndl.narl.org.tw/.

~Ming Liu, Editor

Opening Ceremony of SNDT 2019
From front left to right: Dr. Wen-Fa Wu, Prof. Masaharu Kobayashi (University of Tokyo), Dr. Philip Wong (Vice President of tsmc), Prof. Wen-Kuan Yeh (Chair of ED Tainan Chapter), Prof. Min-Hung Lee (National Taiwan Normal University), Prof. Pi-Ho Hu (National Central University) and some attendees.

IEEE EDS Mini-Colloquium held at Universitat Rovira i Virgili in Tarragona, Spain

by Benjamin Iniguez, Lluis Marsal, and Mike Schwarz

A Mini-Colloquium at the Universitat Rovira i Virgili (URV) took place on May 24th in Tarragona, Spain. The MQ was hosted and organized by the DEEEA department of the URV under the supervision of Prof. Benjamin Iniguez and Prof. Lluis Marsal.

Invited Distinguished Lecturers of the MQ were Dr. Fernando Guarin, Prof. Hiroshi Iwai, Dr. Mukta Farook, Prof. Durga Misra, Prof. Simon Deleonibus and Prof. Yogesh Chauhan.

Dr. Guarín held an inspiring lecture on the topic of *"Leveraging semiconductor technology for the benefit of society."* He discussed how semiconductor technology and electron devices have benefited society and the world in which we live, and how the multiple advances in devices and materials have provided us with unprecedented amounts of solutions and information at continually decreasing costs. Dr. Guarín is an IEEE Fellow, Distinguished Lecturer for the IEEE Electron Devices Society (EDS), a long-time member of the EDS Board of Governors, and current President of the Society (2018 and 2019).

Next, Prof. Hiroshi Iwai from Tokyo University shared his opinion on the end of *"Moore's Law" by a lecture on "End of CMOS miniaturization and technology development after that."* The lecture contained the limit of the CMOS miniaturization and the semiconductor device technology development after reaching the scaling limit. Prof. Hiroshi Iwai is a Professor Emeritus, IEEE Life Fellow, and has served as EDS President and IEEE Division I Director, as well as being an IEEE EDS Distinguished Lecturer for 25 years since 1994.

After a break, the lecture *"Heterogeneous Integration"* by Dr. Mukta Farook followed. The lecture discussed the question why silicon scaling reached astonishing levels over the last half century, while it has not been a corresponding level of scaling in electronic packaging technology, with a view to shedding light on the reasons behind the paradigm shifts, and the methods by which these are achieved. Dr. Mukta Farooq is an IEEE Fellow, an IEEE EDS Distinguished Lecturer, a Distinguished Alumna of IIT-Bombay (India), an RPI Mercer Distinguished Lecturer, and a member of the IEEE EDS Board of Governors.

The fourth lecture was given by Prof. Durga Misra on the topic of *"Self-Heating in FinFETs: Characterization, Reliability and Impact on Logic Circuits."* The lecture outlined the self-heating (SH) in FinFETs and its characterization. E. g. local self-heating potentially affect device performance and exacerbate the effects of some reliability mechanisms. Furthermore, three different measurement methodologies for the electrical characterization of FinFET self-heating at wafer-level were presented. Prof. Durga Misra is currently an

Invited Distinguished Lecturers and participants of the EDS MQ in Tarragona, Spain

IEEE EDS Distinguished Lecturer and serving on the EDS Board of Governors. He is a Fellow of the Electrochemical Society (ECS). He received the Thomas Collinan Award from the Dielectric Science & Technology Division of ECS. He is also the winner of the Electronic and Photonic Division Award from ECS.

The afternoon session was opened by Prof. Simon Deleonibus with the lecture *"New routes and paradigms in Device Engineering for Nanoelectronics and Nanosystems."* His lecture concentrated on the future of nanoelectronics and how it will face the major concerns of being energy and variability efficient (E.V.E.). Simon Deleonibus is distinguished CEA Research Director (2002), IEEE Distinguished Lecturer (2004), Fellow of the IEEE (2006), Fellow of the Electrochemical Society (2015). He was awarded the titles of Chevalier de l'Ordre National du Mérite (2004) and Chevalier de l'Ordre des Palmes Académiques (2011), the 2005 Grand Prix de l'Académie des Technologies. He was Associate Editor of *IEEE Transactions on Electron Devices* (2008–2014) and Member of the EDS Board of Governors (2009–2014) and reelected (2016–2018); Chair of IEEE EDS Region 8 SRC (2015–2016); and EDS Secretary (2016–2017).

The MQ was closed by the lecture of Prof. Yogesh Chauhan on "*Fundamentals and Recent Progress in Negative Capacitance Transistors.*" The lecture focused on the physics and modeling of various "negative capacitance transistor (NCFET)" structures and impact of this new transistor on circuits including processors. Dr. Yogesh Chauhan is an associate professor at IIT Kanpur and he is the Editor of *IEEE Transactions on Electron Devices* and IEEE EDS Distinguished Lecturer. He is a member of the EDS Compact Modeling Technical Committee. He is the founding chairperson of the IEEE Electron Devices Society U.P. Chapter and Vice-chair person of IEEE U.P. Section.

~ Mike Schwarz, Editor

How to Plan an EDS Distinguished Lecture Event

When planning your upcoming chapter meetings, workshops, etc., please remember to visit the EDS website for a recent list of EDS Distinguished Lecturers (DLs) and lecture topics.

✓ DL Checklist

- ☐ Chapter contacts EDS DL to check availability, confirm date/location of lecture, discuss DL funding needs and determine chapter funding
- ☐ EDS DL completes EDS DL Activity Log & Funding Request Form
- ☐ If applicable, obtain EDS funding approval
- ☐ Chapter publicizes lecture via web, email, etc. and can obtain chapter members list via IEEE OU Analytics.
  - ○ Do not forget to publicize EDS Membership Offers!
- ☐ If applicable, DL submits their expense report via IEEE Concur to receive reimbursement
- ☐ Chapter Chair/DL Coordinator submits EDS DL/MQ Feedback Form

Thank you for your continued support of the Society.

Europe, Middle East & Africa (Region 8)

ED Poland Chapter
—by Krzysztof Górecki and Daniel Tomaszewski

EDS Distinguished Lecturer, Mansun Chan gave gave a talk titled "Simulation and Modeling of Dynamic Systems with Time Varying Device Characteristic" on May 21, 2019, at Łukasiewicz Research Network—Institute of Electron Technology (Łukasiewicz ITE), Warsaw, Poland. Approximately 15 persons from ITE and from abroad, traveled to Warsaw for the ESSDERC paper selection meeting and to attend the lecture.

The abstract of the Distinguished Lecture: The existing circuit simulation methodologies are based on time-invariant device models, electrical characteristics and parameters of which do not change over time. However, more recently, many new applications such as neuromorphic computing or artificial neural-network circuits require the use of devices with history dependent behavior. Due to such a behavior different from traditional transistors, which are the focus for the compact modeling community, a new approach to monitor the time dependent characteristics of these devices is necessary. In addition, a new simulation methodology is also required to predict the behavior of such system efficiently. In the presentation, a new approach to simulate dynamic systems was introduced. The proposed approach combined with the modification of simulation flow and compact model construction was introduced. The approach is very general and can be used to cover a wide class of devices with dynamic behavior such as memory function or device performance degradation during a prolonged operation.

Prof. Mansun Chan giving a Distinguished Lecture in ITE, Warsaw, May 21, 2019

Some attendees of the EDS Distinguished Lecturer Mini-Colloquium "Nanoelectronics—Technology, Design, Modeling" in Rzeszów, June 26, 2019

A Mini-Colloquium was organized by the ED Poland Chapter in cooperation with: Gdynia Maritime University, Gdynia, Poland, Łukasiewicz Research Network—Instytut Technologii Elektronowej (Łukasiewicz-ITE), Warsaw, Poland, and a Department of Microelectronics and Computer Science, Lodz University of Technology, Lodz, Poland. Approximately 20 persons attended the full-day event. Nine interesting talks were presented by internationally recognized experts in the area of nanoelectronics, including three EDS Distinguished Lecturers (DLs).

Prof. Shinichi Takagi (The University of Tokyo) presented a talk "Tunneling FET technology for ultra-low power logic applications" addressing critical issues, technical challenges and viable technologies of TFETs using a variety of semiconductors such as Si, Ge and oxide semiconductors. Device engineering indispensable in improving the performance of TFETs were summarized with emphasis on

the source junction formation technology and the optimal material design. The electrical characteristics of TFETs using Si and Ge homo junctions, Ge/strained SOI hetero-junctions and ZnO/(Si, Ge) hetero-junctions were presented as the viable examples.

Prof. Andrzej Strójwąs (PDF Solutions, and Carnegie Mellon University) had a talk "New Product Introduction Challenges in the Bleeding Edge Technology Nodes," presenting a comprehensive methodology and a full suite of process-design design interaction characterization techniques to enable cost-effective introduction of new products in the 7 nm and below technologies.

Dr. Arkadiusz Malinowski (GlobalFoundries) gave a talk "Will FinFET era last only for 10 years? FinFET scaling challenges for next CMOS technology nodes," in which challenges related to FinFET metrology/inspection, lithography/overlay, integration/variability, cycle time and cost were addressed.

Dr. Rajiv V. Joshi (DL, IBM Research Division Yorktown Heights) presented a lecture "Variability aware design in nm era." He highlighted predictive analytical technique based on statistical analysis methodology targeting both memory and custom logic design applications is highlighted. Design case studies both in planar and non-planar technologies were discussed. Finally, the speaker discussed an efficient statistical methodology based on simulation and modeling to evaluate and minimize the aging of memory chips.

Prof. Henryk M. Przewłocki (DL, Łukasiewicz Research Network—Instytut Technologii Elektronowej) presented a talk "Expanding the horizon of photoelectric investigations of the MIS system properties," in which he discussed an extended theory of the photocurrent vs. gate voltage characteristics, at different wavelengths of light illuminating the structure under test, with diffusion currents taken into account. The theory is in agreement with the relevant experimental characteristics. This opens the possibilities of developing new measurement methods of the MIS system crucial parameters.

Prof. Marcelo Pavanello (DL, Centro Universitario FEI) presented a talk "Performance and modeling of Nanowire-based MOSFETs." He discussed differences between double-gate, triple-gate and nanowire-based MOSFETs and their characteristics. Also junctionless nanowire transistors (JNTs) were introduced as one of the interesting alternatives for downscaling because of their relative process simplicity compared with inversion-mode nanowires. Different aspects of modeling of the JNT steady-state and dynamic operation was interestingly presented.

Dr. Farzan Jazaeri (EPFL) presented a talk "Cryogenic Electronics and Quantum Computing Architecture." He made an interesting review of topics of a quantum computation that holds the promise to solve problems that are intractable even for the most powerful supercomputers. Quantum computers process the information stored in quantum bits (qubits). The information in the qubits is fragile, so the qubits must be typically cooled to cryogenic temperature. Spin qubits in silicon were reported that have already been proposed and experimentally demonstrated in academic research laboratories.

Prof. Mike Brinson (London Metropolitan University) presented a talk "Equation-Defined template and synthesis driven compact modelling of semiconductor devices." He reported current research that links Equation-Defined Device modelling with Verilog-A modules, driven by code templates and synthesis, which in turn result in an improved interactive modelling techniques. Throughout the talk a series of compact device models were introduced to demonstrate the fundamentals and application of the new approach to compact device modelling.

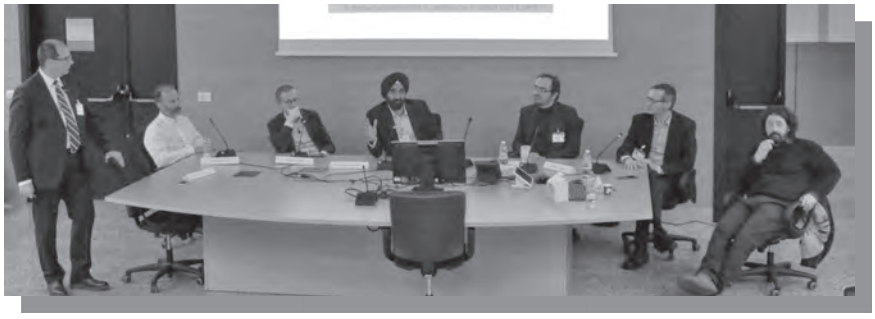
Dr. Władek Grabiński (DL, MOSAK and GMC) presented a talk "FOSS tools for support of IC modeling and design with special emphasis on Verilog-A standardization." He discussed selected FOSS CAD tools along complete technology/design tool chain from nanoscaled technology processes. The talk was illustrated by application examples of the FOSS TCAD tools, like Cogenda TCAD and DEVSIM. Compact modeling was related to the parameter extraction and standardization of the experimental and measurement data exchange formats. Finally, present FOSS CAD simulation and design tools: ngspice, Qucs, GnuCap, Xyce were presented.

~ Marcin Janicki, Editor

Workshop on Advances in Analog Circuit Design (AACD)

—by Andrea Baschirotto

On April 1–3, 2019 University of Milan-Bicocca hosted the 28th edition of the Workshop on Advances in Analog Circuit Design (AACD). The Workshop is arranged in three one-day sessions, each one dealing with



In the picture, the panel coordinated by Andrea Baschirotto (on the left) with the participation of (from the left) A. Laville (TriaxisTechnical Leader, Melexis), A. Onetti (MEMS Sensor Division General Manager, STMicroelectronics), B. Chandhoke (Senior Product Manager, GlobalFoundries), C. Calligaro (CEO, RedCat Devices), M. Pagani (Group Manager, Huawei, Italy), and M. De Matteis (Professor, Univ. of Milano-Bicocca)

a specific topic by means of 6 invited speakers and a final panel. The formula allows great interaction with the audience in interesting scientific discussions. This year the topics for the three sessions were: "Next-Generation ADCs" (organized and chaired by Kofi Makinwa), "High-Performance Power Management" (organized and chaired by Pieter Harpe), and "Technology Considerations for Advanced IC" (organized and chaired by Andrea Baschirotto). About 150 participants (from both industries and research institutes) attended the sessions and contributed to interesting discussions. The event has been supported by several companies (Huawei, Infineon, Maxim, Melexis, RedCat Devices, STMicroelectronics, TDK-Invensene), INFN (National Institute for Nuclear Physics), and by the IEEE-SSCS Italian Chapter. Two social events contributed to increaseinteractionsbetween the participants: the visit and the Welcome Reception at the Leonardo da Vinci exhibition (within the celebration for Leonardo death 500 years ago), and the Gala Dinner at the Luciano Pavarotti (famous opera singer) museum restaurant.

Further information's are available at the website innotechevents.com/aacd2019.

Distinguished Lecture in Madrid and Valencia

—by Benjamin Iniguez, Lluis Marsal, and Mike Schwarz

Prof. Albert Wang, from the Dept. of Electrical and Computer Engineering of the University of California (USA), gave a Distinguished Lecturer at Institute on Nanotechnology and Semiconductor Nanodevices (ISOM) of the Polytechnical University of Madrid (Madrid, Spain), on May 20, 2019. It was organized by Prof. Miguel Angel Sánchez, who is Professor at the Polytechnical University of Madrid. The title of his seminar was "LED-Based Visible Light Communications Systems-on-Chip."

Prof. Albert Wang, from the Dept. of Electrical and Computer Engineering of the University of California (USA)

On May 22, 2019, Prof. Wang also gave a Distinguished Lecturer at the University of Valencia (Valencia, Spain). It was organized by Prof. Enrique Maset. The title of Prof. Wang's seminar was "On-Chip ESD Protection Designs for Integrated Circuits."

IEEE EDS Distinguished Lecture at University Rovira i Virgili

—by Benjamin Iniguez, Lluis Marsal, and Mike Schwarz

Prof. Joao Martino, from the University of Sao Paolo (Brazil), gave a a Distinguished Lecturer at the University Rovira i Virgili (Tarragona, Spain), on April 4, 2019. He was invited by the ED Spain Chapter, chaired by Prof. Benjamin Iñiguez.

The title of his seminar was "Field-Effect Transistors: From MOSFETs to Tunnel FETs." This talk was a review of Si FET technologies starting from the first MOSFET process, up to Tunnel FETs; SOI MOSFETs and FinFETs were also addressed.

Prof. Lluis Marsal, Prof. Benjamin Iñiguez and Prof. Joao Martino

Prof. Joao Martino during his Distinguished Lecture

19th HICUM Workshop

—by Christoph Weimer

The 19th HICUM Workshop, a forum for the presentation and discussion of recent advances and issues related to heterojunction bipolar transistor modeling with focus on the industry standard compact model HICUM, was held May 12–13, 2019, at the facilities of Infineon AG in Neubiberg, Germany. HICUM stands for HIghCURrent Model and targets the design of bipolar transistor circuits at high frequencies using Si, SiGe or III-V based process technologies.

Professor Michael Schröter, the author of HICUM and head of the Chair for Electron Devices and Integrated Circuits (CEDIC) at the TU Dresden, opened the workshop. Following the traditional schedule of the previous HICUM workshops, first an overview on the latest HICUM/L2 and L0 developments and releases were presented by Prof. Schröter. Examples of recent developments include improvements of the formulations for the collector avalanche current and the critical current.

Didier Céli from ST Microelectronics reviewed geometry scaling laws of the base-collector depletion capacitance and proposed a very accurate scaling scheme. Markus Müller from CEDIC presented a parameter extraction tool, which is based on open-source software. This object-oriented, scalable framework is written in the language Python and is currently being developed by the modeling engineers at CEDIC. It targets the fast and efficient extraction of compact model parameters, simulation of compact models using an interchangeable interface to a multitude of circuit simulators and evaluation of a large amount of measurement data. W. Grabinski concluded the first workshop day by providing an overview of different open-source compact modeling tools. Wrapping up the first workshop day, most of the participants had dinner together in the center of Munich.

The second workshop day was opened by Prof. Schröter with a review of different approaches for collector avalanche effect compact modeling in Si BJTs and SiGe HBTs. C. Weimer from CEDIC presented first results of his experimental study related to the degradation of the small-signal transistor behavior as a result of static stress, such as reverse-bias stress and extreme forward-active bias stress, and examined relevant aspects of reproducible, long-term S-Parameter measurements.

The circuit-oriented part of the workshop was commenced by M. van Delden from the Ruhr-University Bochum, who discussed the advantages of HICUM for designing high-speed fully programmable frequency dividers. Subsequently, Y. Zhang from CEDIC provided comparisons between simulation and measurement of various mm-wave circuits for device characterization and model verification. Additional sensitivity studies provide insight into the impact of physical and parasitic effects in HBTs on circuit performance.

Prof. Schröter concluded the 19th HICUM Workshop by presenting future development plans for HICUM. As usual, the workshop provided plenty of time for discussions and gave all participants the opportunity of valuable information exchange.

5th joint EUROSOI—ULIS 2019 Conference

—by Maryline Bawedin and Mike Schwarz

The 5th joint EUROSOI—ULIS 2019 conference was held from April 1–3 in Grenoble, France. The conference was hosted by the Maison Minatec conference center. This year it was sponsored by IEEE, IMEP-LAHC, CEA-LETI, SOITEC, Solid-State-Electronics Journal, SINANO Institute, CNRS, Grenoble INP, Université Grenoble Alpes and AirFrance/KLM.

The local organizing committee Dr. Maryline Bawedin (IMEP-LAHC, Conference General Chair), Dr. Joris Lacord (CEA-LETI, Conference Co-Chair), Prof. Jean-Pierre Colinge (CEA-LETI, Technical Program Chair), Dr. Claire Fenouillet-Beranger

Participants of the 5th joint EUROSOI—ULIS 2019 conference

(CEA-LETI, Editorial Manager), Dr. François Tcheme-Wakam (UGA, Local Arrangement Chair), and Mrs. Dalhila Alouani (IMEP-LAHC, Treasurer) Participants from 21 countries attended the conference: France (30), South Korea (15), Germany (11), Belgium (8), Spain (8), Russia (6), Italy (5), Switzerland (4), India (3), Brazil (2), Canada (2), Japan (2), Mexico (2), Netherlands (2), UK (2), Australia (2), Austria (1), USA (1), Ireland (1), Taiwan (1), Ukraine (1). There were also representatives from 5 major companies: Globalfoundries (2), IBM (1), STMicroelectronics (4), Huawei Technologies (2), and SK Hynix (4).

The best paper award was given to Dr. Gilles Scheen (UCLouvain, Belgium) for his contribution "Post-process porous silicon for 5G applications."

The conference hosted various presentations and posters in six sessions on these topics:

- Advanced transistor architectures
- Advanced materials
- Characterization techniques and reliability assessment techniques
- Novel devices
- III-V semiconductors and memory-oriented materials

Additionally the program hosted keynotes by:

- Nanowire/sheet-FETs for ultra-scaled, high-density logic and memory applications—Anabela Veloso, IMEC
- SOI Technology: From Niche to Mainstream Applications—Ionut Radu, SOITEC
- Effects in Innovative Devices—Marc Gaillardin, CEA-DIF
- Steep-Slope Devices for Ultra-Low-Power Applications—Ru Huang, Peking University

The conference contained as well some satellite events:

- FDSOI RF technology for 5G Workshop
- REMINDER Industrial Workshop on 1T-eDRAM
- IEEE International Nanodevices and Computing Conference *(see separate article)*

~ Mike Schwarz, Editor

ED/AP/MTT/COM/EMC Tomsk Chapter

—by Oleg Stukach

The 14th International Siberian Conference on Control and Communications (SIBCON-2019), organized by the ED/AP/MTT/COM/EMC Tomsk Chapter and Tomsk State University of Control Systems and Radioelectronics (TUSUR), and co-sponsored by National Instruments Rus R&D, was held in Tomsk TUSUR facility "Dom Uchenykh," Russia, on April 18–20, 2019. This biennial conference was formed in 1995 to bring together engineers and scientists to discuss state-of-the-art technologies and devices for control and communications.

This year's topics were: fundamental directions of communication and control theory, robots and automation, computer measurement technologies, sensors and systems, with a focus on the development of microwave electron devices, which are the main field of R&D activities at TUSUR. Nowadays, it is not conceivable to design a new device or rather technological process, or even to study a physical structure without simulation and characterization methods. They have become important tools in semiconductor technology research and development.

The conference had 212 registrants, and 106 selected papers were presented at 12 sessions, including keynote papers. The papers were selected by peer review from 180 papers received. The number of contributions has not increased from year to year but good quality of papers has been achieved. Our sponsor, National Instruments Rus R&D provided the attendees with bags containing promo materials and many technical presentations.

The SIBCON Conference triggered a lot of fruitful discussions and was held in a very friendly atmosphere. Social events were arranged, including a reception, a get together party, the conference banquet, as well as technical and sightseeing tours. Several possibilities for further increase in participation in chapter activities and EDS membership were identified and pursued.

My sincere congratulations must go to the TUSUR Scientific Council staff and personally to Inna Yarimova, who did an excellent job of organizing this successful event. We trust this conference will continue in the future, increasing the number of participants as well as inviting lecturers and growing contributions from other countries. We hope to meet you at the next SIBCON in Kazan in 2021. More data on the SIBCON Conference is available at http://tomsk.chapters.comsoc.org/sibcon/.

About TUSUR (https://tusur.ru/en): Tomsk State University of Control Systems and Radioelectronics is a modern, dynamically developing university, one of the leaders in a system of Russian higher education on electronics included in QS World University Rankings EECA. TUSUR Innovative Complex project provides about 80% scientific and research results in the Tomsk Region.

~ Daniel Tomaszewski, Editor

The National Instruments Session at SIBCON-2019

Asia & Pacific (Region 10)

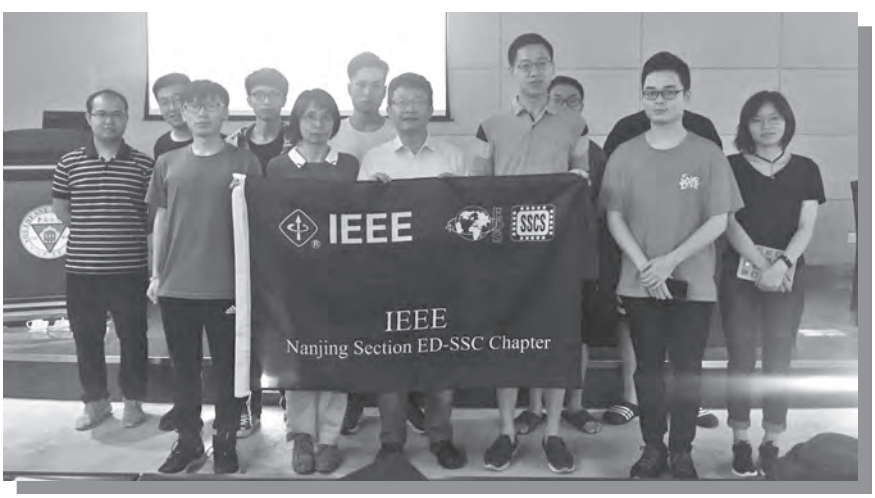
ED/SSC Nanjing Chapter

—by Weifung Sun

The EDS/SSCS Nanjing Chapter held a Distinguished Lecture, containing two interesting topics, on June 20, 2019, at Southeast University Wuxi, China. The event was hosted by Prof. Weifeng Sun. There were two speakers from the Department of Electronics Engineering of the National Chiao Tung University, Prof. H. C. Lin and Prof. P. W. Li. Their talks are briefly introduced below.

Prof. H. C. Lin gave a talk entitled "Three-Dimensional ZnO Inverter Technology." A new "film profile engineering" (FPE) scheme is conceived and established to fabricate sub-micron, high-performance metal-oxide thin-film transistors (MO TFTs) and logic gates. In the scheme, a bridge is first constructed to suspend right over the gate electrode with an attempt to shadow the deposited species. Then, various apparatuses with specific deposition conditions are employed to prepare the major thin films, i.e. gate dielectric, channel and source/drain (S/D) electrodes, with tailored and desirable film profiles to fabricate MO TFTs displaying superb performance. Based on the above scheme, an innovative, 3-dimensional (3D) sub-micron ZnO inverter technology is further developed. Three patterned, stacked and separated TiN layers are built at first in this technology as the hardmask, load gate and drive gate, respectively. By utilization of the FPE scheme, the load TFT stacked on the drive one can be fabricated simultaneously. VTH of the two devices can be properly tuned through controlling the geometric parameters of the three TiN layers. The 3D ZnO inverters fabricated with the new technology demonstrate excellent performance in voltage transfer characteristics (VTC) including full-swing switching, moderate noise margin, high voltage gain, good uniformity and superior immunity to light-induced instability.

Prof. P. W. Li gave a talk entitled, "Self-organized heterostructures of Ge nanosphere/SiO2/Si1-xGex-recess channel enables monolithically-integrated electronics and photonics on Si platform." Seamless integration of Si-based EPICs in CMOS technology promises cost-effective data transfer, IoT, and quantum computing applications. While it is a formidable task for Si itself to implement EPICs, recently Ge emerges as the savior thanks to its pseudo-direct bandgap, high carrier mobility, and CMOS compatibility. Discrete Ge MOSFETs and photodetectors were demonstrated, however, monolithically-integrated Ge receivers on Si for optical/electrical signal conversion and amplification, is challenging due to the size incompatibility for μm-scale PDs versus nm-scale MOSFETs. Prof. Li shared recent advances in a single-fabrication-step growth of Ge nanodot/SiO2/SiGe-recess channel heterostructures, which is a key enabler for realizing Ge MOS devices supporting the Si nanoelectronics (MOSFETs) as well as Si nanophotonics (photodetectors). We report the first-of-its-kind, self-organized gate stack of Ge nanosphere gate/SiO2/Si1-xGex channel fabricated in a single oxidation step. Process-controlled tunability of the Ge NP size, SiO2 thickness, and Ge content and strain engineering of the Si1-xGex are achieved. We demonstrated Ge junctionless (JL) n-FETs and photoMOSFETs (PTs) as amplifier and photodetector, respectively, for Ge receivers. Our gate stack of Ge NP/SiO2/Si1-xGex enables a practically achievable building block for monolithically-integrated Ge electronic and photonic ICs (EPICs) on Si. We sincerely believe that our discoveries on the formation of Ge Nanosphere/SiO2/SiGe heterostructures have only scratched the "tip of the iceberg" in terms of the myriad, exciting device possibilities. We envisage further scientific exploration of our MOS heterostructures toward the ultimate goal of demonstrating advanced Ge-based MOS nanoelectronic and nanophotonic devices. The DL had good attendance with approximately 20 PhD students, postgraduate students and 2 faculty members.



ED/SSC Nanjing, DL on June 20, 2019, (Row 1 from left) Speaker (Prof. P. W. Li, 2nd and Prof. H. C. Lin, 3rd), and seminar chair (Prof. Weifung Sun, 4th) with audience

ED Taipei Chapter

—by Steve Chung

The ED Taipei Chapter together with the EDS NCTU Student Chapter held two invited talks in the second quarter of 2019. The first event was given on April 26th, in which Dr. Hsinyu Tsai, IBM Research, was invited to give a talk entitled, "Analog Memory-based Accelerators for Deep

ED Taipei, Invited Talk on April 26th, (Row 1, from left) (Prof. H. M Chen, 6th), Speaker (Dr. Hsinyu Tsai, 7th), seminar chair (Prof. Steve Chung, 8th) with audience

ED Taipei, Invited DL on May 27th, (left) Group photo (the speaker and audience), (right) Speaker (Ajit Kumar Panda) and seminar chair (Steve Chung)

Learning." Dr. Tsai gave a review on the current status of computing advances and requirements of neuromorphic computing, especially on the hardware implementation and/or acceleration of deep neural networks (DNN), which demonstrated near-human capabilities on tasks of image recognition, understanding speech, playing games, and translations between languages. This progress ranges from systems that combine conventional CMOS devices in different and unconventional ways to systems built around emerging NVM devices. She discussed how the strengths and weaknesses of analog memory-based accelerators match well to the weakness and strengths of digital accelerators, and attempt to identify future hardware opportunities. One example she gave is their recent enormous progress on the use of phase change memory devices for the analog-based DNN. This talk was attended by around 50 graduate students and professors.

The second talk, given by Prof. Ajit Kumar Panda of National Institute of Science and Technology, India on May 27, 2019, was entitled "HEM: A Prospective Device for High Frequency Communication Circuit." Prof. Panda's talk started from Semiconductor to 2DEG formation technique using his own philosophy and developed program to HEMT device determining different power and different structures. He showed the potential of HEMT device. Finally he presented how HEMT can be used in Circuit. He also showed how they have designed, model, fabricated and put on in circuit to see the potential of HEMT to use as an amplifier. This talk was attended by around 40 graduate students, professors, and several industry leaders.

One major event is a premier event on VLSI in the region as well as a leading technology conference worldwide for over 30 years, 2020 VLSI-TSA and VLSI-DAT, April 20–23, 2019, Hsinchu, Taiwan, https://expo.itri.org.tw/2020VLSITSA. Both are mainly technically sponsored by the IEEE EDS and SSCS, which attracts more than 900 attendees each year. The paper submission due date is: October. 31, 2019. For further information and inquiries, please contact Miss Caroline Huang, vlsitsa@itri.org.tw.

ED Tainan Chapter

—by Wen-Kuan Yeh

The ED Tainan Chapter held one Distinguished Lecture in Tainan, Taiwan on May 10, 2019. Dr. Seji Samukawa (Professor, Institute of fluid science, Tohoku University, Sendai, Japan) gave his talk at National Cheng-Kung University (NCKU), titled "Creating Green Nanostructures and Nanomaterials for Advanced Energy Nano Devices." His talk focused on new material and structure of nano-devices for related applications. About 50 attendees and several professors from local universities attended.

ED Beijing Chapter

—by Kangwei Zhang

The ED Beijing Chapter held one Distinguished Lecture in Beijing, China on April 29, 2019. Dr. Hiroshi Iwai (Professor Emeritus, Institute of Innovative Research, Tokyo Institute of Technology, Yokohama, Japan) gave a talk at the Institute of Microelectronics of Chinese Academy of Sciences. The talk "End of CMOS miniaturization and technology development after

ED Tainan, DL talk on May 10th, (First row, left second) Prof. M. H. Chiang, Prof. W. K. Chung (Chair, Institute of Microelectronics, NCKU), Prof. Wen-Kuan Yeh (Chair of ED Tainan Chapter), Prof. Dr. Seji Samukawa (DL speaker), and some of attendees

ED Beijing Distinguished Lecture at on April 29th, (Row 1 from left) Speaker (Dr. Hiroshi Iwai, 4th), seminar chair (Prof. Ming Liu, 5th) with audience

that," explained the limit of CMOS miniaturization and discussion on semiconductor device technology development after reaching the scaling limit. About 30 attendees and several professors attended Dr. Iwai's talk.

~Ming Liu, Editor

ED Malaysia Kuala Lumpur Chapter

—by S.N. Ibrahim, S. Fatmadiana, Z. Yusoff, and R.A. Rahim

EDS Malaysia Chapter Receives 2018 Region 10 Chapter of the Year Award

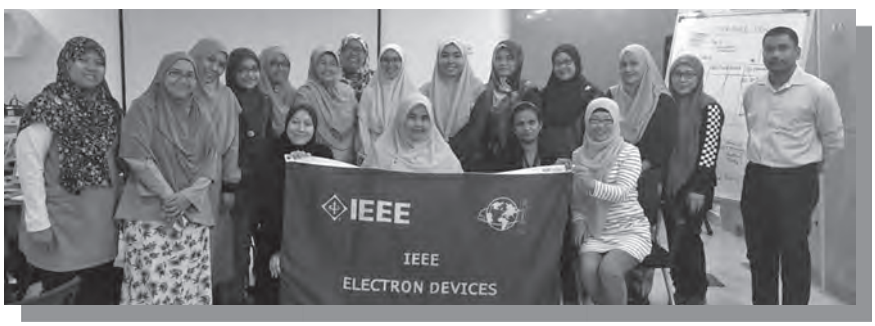
The EDS Malaysian Chapter was presented with the 2018 IEEE Electron Devices Society Region 10 Chapter of the Year Award during the TC-sponsored Mini Colloquium on Photovoltaics on 9th April 2019 at Meeting Room, Level 4, Administrative Building FKAB, Universiti Kebangsaan Malaysia (UKM) Bangi, Selangor. The event commenced with a welcoming speech by the EDS Malaysia chapter advisor, Professor Dato' Dr Burhanuddin Yeop Majlis and the Vice President of IEEE Electron Devices Society, Dr M.K. Radhakrishnan. The award was received by the Past Chair of EDS Malaysia, Assoc Prof Dr P Susthitha Menon and the current chair, Prof Dr Norhayati Soin.

Workshop on Effective Research Skills at Universiti Malaya (UM)

EDS in collaboration with the Centre of Printable Electronics of University of Malaya, had conducted a workshop on Effective Research Skills on 3rd to 4th of April 2010. The aim of the workshop is to expose newly registered postgraduates with valuable skills on how to conduct research whilst gaining clarity on their research objectives. The workshop was held at The Cube at level 4 of KPPI Building in University of Malaya. 17 participants from various universities participated in the workshop. EDS Chair Prof Ir Dr Norhayati Soin, was the main speaker for the workshop. Dr Sharifah Fatmadiana, and Dr Ma Li Ya also facilitated Prof Norhayati for the one-to-one session. With this, participants had gained insights of practical methods of structuring literature reviews, to develop an impactful research statement, to develop strong research objectives and to design a coherent research methodology. At the end of the session, there was a presentation session from participants, and from their presentations, it was apparent that the objectives of the workshop had been fulfilled as at the end of the workshop, the participants were able to produce satisfactory presentations of their respective research topics.

EDS Malaysia Instilling Innovative Mindset at EE Makerthon

The Department of Electrical Engineering at University of Malaya, in collaboration with IEEE EDS, had conducted an EE Makerthon event from 26th April to 28th April 2019. The EE Makerthon 2019: Smart Drone Challenge was a 3-day design competition event during which, participants were required to build physical prototypes in line with the theme, within a specific amount of time. This year the theme was a smart drone challenge in drone delivery management whereby the participants need to proposed drone-based solutions for pick up and drop off package in specific condition and location, while at the same time maintain communications with the station. The participants, who were of 2nd year Electrical Engineering students, were expected to provide solutions in combination of technical ability, engineering design and some level of complexity. There were three challenges, challenge 1—object lifting, challenge 2—recognizing the place to drop the object, challenge 3—drone's battery wireless charging. There were eight awards given to the participants—top three best Instagram pictures award, special award by Head of Department Electrical Engineering, best design award and top three drone challenge winners. Judging panels from the industry had also attended the event to evaluate the design and performances of the drones.



Participants of the Effective Research Skills Workshop

EDS-ETC Event for Full Residential School International Symposium (FRSIS) at IIUM

An educational program with 38 participants of 8th Fully Residential School International Symposium (FRSIS) 2019 from Malaysia (33), Japan (1), Vietnam (1) and Philippines (3) was successfully conducted on 14th June 2019. Officiated by Dean of Kulliyah of Engineering, IIUM, Prof Ahmad Faris Ismail, the program is divided into two sessions: Arduino Coding and EDS-ETC Electronics. In EDS-ETC Electronics session, the Form 4 students are divided into 4 groups and they were introduced to Electronics concepts through hands-on activities at 4 stations: FM Radio, Automatic Street Lamp, Solar Battery and Sand Water Detector. This session certainly has helped them in seeing the real application of electronics and it is hoped it will stimulate their interests in this field.

Participants of the EE Makerthon at Universiti of Malaya

Group photo session with lecturers of Kulliyyah of Engineering, IIUM

IEEE EDS Technical Talk— Seminar on Biosensors at IIUM

IEEE EDS Malaysia Chapter and VLSI and MEMS Research Unit, Department of Electrical and Computer Engineering, Kulliyyah of Engineering has organized a technical talk session on biosensors seminar on 20th June 2019 at Kulliyyah of Engineering, International Islamic University Malaysia. The title of the seminar is Point of Care biosensors for healthcare management in developing countries. Officiated by Dean of Kulliyah of Engineering, IIUM, Prof Ahmad Faris Ismail, the seminar was delivered by an eminent researcher in the biosensing field, Prof. Anthony Turner, Emeritus Professor of Biotechnology from Cranfield University, United Kingdom, who is also the Editor-in-Chief, Biosensors and Bioelectronics Journal, Elsevier. The title of his talk is Biosensors based on soft materials. In addition, the seminar also has featured another three invited speakers such as Prof Uda Hashim, Vice Chancellor, Universiti Malaysia Perlis with his talk on IoT based Biosensor for medical diagnostic application and Prof Norhayati Soin, Head of Center of Printable Electronics, University Malaysia with her talk on Printable Internet of Things pH Sensors and Their Potential Application for Palm Based Biodiesel. Finally, Prof Anis Nurashikin Nordin Head of VLSI & MEMS Research unit, IIUM delivered her talk on BioMEMS for Non-Pervasive and Personalised Healthcare Sensors. All the invited speakers shared their research expertise on the biosensor. The seminar successfully attracted 38 participants from various universities in Malaysia.

Participants and invited speakers at IIUM Seminar on Biosensors

~P Susthitha Menon, Editor

EDS MEETINGS CALENDAR

The complete EDS Calendar can be found at our web site: http://eds.ieee.org. Please visit.

2019 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)	04 Sept – 06 Sept 2019	UDINE, Italy
2019 Joint International Symposium on e-Manufacturing & Design Collaboration(eMDC) & Semiconductor Manufacturing (ISSM)	06 Sept 2019	Taiwan
2019 16th International Conference on Electrical Engineering, Computing Science and Automatic Control (CCE)	11 Sept – 13 Sept 2019	Ukraine
2019 XXIVth International Seminar/Workshop on Direct and Inverse Problems of Electromagnetic and Acoustic Wave Theory (DIPED)	12 Sept – 14 Sept 2019	Ukraine
2019 41st Annual EOS/ESD Symposium (EOS/ESD)	15 Sept – 20 Sept 2019	Riverside, CA, USA
2019 IEEE 31st International Conference on Microelectronics (MIEL)	16 Sept – 18 Sept 2019	Nis, Serbia
ESSCIRC 2019 - IEEE 45th European Solid State Circuits Conference (ESSCIRC)	23 Sept – 26 Sept 2019	Cracow, Poland
ESSDERC 2019 - 49th European Solid-State Device Research Conference (ESSDERC)	23 Sept – 26 Sept 2019	Cracow, Poland
2019 8th International Symposium on Next Generation Electronics (ISNE)	09 Oct – 11 Oct 2019	Zhengzhou, China

2019 International Semiconductor Conference (CAS)	09 Oct – 11 Oct 2019	Sinaia, Romania
2019 IEEE International Integrated Reliability Workshop (IIRW)	13 Oct – 17 Oct 2019	South Lake Tahoe, CA
2019 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)	14 Oct – 17 Oct 2019	San Jose, CA, USA
2019 19th Non-Volatile Memory Technology Symposium (NVMTS)	28 Oct – 30 Oct 2019	Durham, NC, USA
2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)	29 Oct – 31 Oct 2019	NC, USA
2019 IEEE BiCMOS and Compound semiconductor Integrated Circuits and Technology Symposium (BCICTS)	03 Nov – 06 Nov 2019	Nashville, TN USA
2019 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)	04 Nov – 07 Nov 2019	Westminster, CO
2019 IEEE International Electron Devices Meeting (IEDM)	09 Dec – 11 Dec 2019	San Francisco, CA
2019 IEEE 50th Semiconductor Interface Specialists Conference (SISC)	11 Dec – 14 Dec 2019	San Diego, CA
2020 IEEE Electron Devices Technology & Manufacturing Conference (EDTM)	15 Mar – 18 Mar 2020	Malaysia
2020 IEEE International Reliability Physics Symposium (IRPS)	29 Mar – 03 April 2020	TX, USA

EDS Vision, Mission and Field of Interest Statements

Vision Statement
Promoting excellence in the field of electron devices for the benefit of humanity.

Mission Statement
To foster professional growth of its members by satisfying their needs for easy access to and exchange of technical information, publishing, education, and technical recognition and enhancing public visibility in the field of Electron Devices.

EDS Field of Interest
The EDS field-of-interest includes all electron and ion based devices, in their classical or quantum states, using environments and materials in their lowest to highest conducting phase, in simple or engineered assembly, interacting with and delivering photo-electronic, electro-magnetic, electromechanical, electro-thermal, and bio-electronic signals. The Society sponsors and reports on education, research, development and manufacturing aspects and is involved in science, theory, engineering, experimentation, simulation, modeling, design, fabrication, interconnection, reliability of such devices and their applications.