IEEE
ELECTRON DEVICES SOCIETY
Newsletter

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Technical Briefs

Micro-Transfer Printing Technology Enables Heterogeneous Integration for 3D ICs

Bob Conner, Johann Weinhändler

3D heterogeneous integration of many diverse ultra-thin components improves the power, performance, area, cost, time-to-market, and security of high-performance computing, communications, mobile, automotive, industrial, medical, and defense systems. These diverse components include high electron mobility transistors (HEMTs), heterojunction bipolar transistors (HBTs), power transistors, gate drivers, photonics, sensors, hardware assurance devices, capacitors, inductors, filters, and antennas manufactured using many different process nodes and technologies, including SOI, GaAs, GaN, InP, and SiGe.

Micro-transfer printing (MTP) technology, a patented process developed by X-Celeprint, employs a massively parallel pick-and-place process to stack large arrays of ultra-thin (1–20 micron) diverse components, called x-chips, from one or more separately manufactured wafers on a variety of destination substrates to improve heterogeneous integration to create a 3D IC with the following improvements in:

- **Performance**—by re-partitioning, disaggregating, and re-integrating by stacking separately manufactured components
- **Power**—by reducing parasitics and resulting power losses by using ultra short interconnects
- **Area**—by using the z-dimension for integration rather than growing x- and y-dimensions and producing ultra-thin 3D ICs for embedding in substrates and organic interposers
- **Cost**—by separately manufacturing each component using the optimal material and technology node, reducing die size,

(continued on page 3)

Your Comments Solicited

Your comments are most welcome. Please write directly to the Editor-in-Chief of the Newsletter at daniel.tomaszewski@imif.lukasiewicz.gov.pl

ELECTRON DEVICES SOCIETY

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NEWSLETTER DEADLINES

Issue	Due Date
October	July 1st
January	October 1st
April	January 1st
July	April 1st

The EDS Newsletter archive can be found on the Society web site at http://eds.ieee.org/eds-newsletters.html. The archive contains issues from July 1994 to the present.

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Micro-Transfer Printing Technology Enables Heterogeneous Integration for 3D ICs

(continued from page 1)

increasing utilization of expensive semiconductor wafers, using low-cost, massively parallel manufacturing processes and relaxing manufacturing thermal constraints

- **Time-to-market**—by combining x-chips produced in different fabs and re-using them in multiple designs by stacking them in different configurations to manufacture many different 3D ICs
- **Security**—by integrating multiple hardware authentication and sensor x-chips

MTP technology supplements other conventional and advanced packaging technologies, providing 3D IC manufacturers with a unique "tool-in-the-toolbox" optimized for heterogeneous integration of large arrays of ultra-thin, diverse components. An MTP-based 3D IC (Figure 1) is manufactured using the following steps: 1) Source wafer fabrication; 2) Destination wafer or substrate fabrication; 3) MTP stamp fabrication; 4) MTP pick-and-place; and 5) Thin film interconnects.

1) Source Wafer

Tightly packed x-chips are fabricated on source wafers made using the optimal process node and technology (such as SOI, GaN, GaAs, InP and SiGe) for each component. A sacrificial layer is formed underneath the x-chips using different techniques depending upon the source wafer technology, such as:

- For SOI x-chips on silicon wafers with <100> or <111> crystal plane orientation, a standard tetramethylammonium hydroxide (TMAH) or potassium hydroxide (KOH) etch removes the silicon under the x-chips with the oxide beneath the x-chips serving as a barrier against etch of x-chips above.
- For compound semiconductors grown on silicon wafers with <100> or <111> crystal plane orientation, a TMAH etch removes the silicon under the x-chips while not removing the compound semiconductor x-chips.
- For compound semiconductors grown on native substrates, various lattice matched sacrificial layers can be used to undercut the x-chips.

A tether/anchor system (Figures 2 and 3) holds the x-chips aloft after the source wafer is anisotropically etched to remove the sacrificial layer everywhere but underneath the anchor.

2) Destination Substrate

There are many options for the destination substrate, including silicon wafers with integrated CMOS ICs, silicon, glass, or ceramic interposer wafers, and large-area glass, ceramic, or plastic panels. The substrate's surface may be planar or non-planar and be smooth or rough.

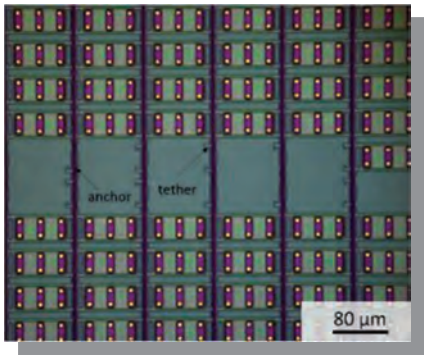


Figure 2. X-chips on source wafer after partial x-chip pick-up.

3) MTP Stamp Fabrication

A low-cost, reusable mold is used to make the MTP stamp (Figure 4) which consists of an array of soft posts composed of a compliant elastomer material, polydimethylsiloxane (PDMS), on a stiff glass substrate. The stamp is stiff in the x-y dimensions, providing high placement accuracy, and compliant in the z-dimension, accommodating non-planar and rough destination

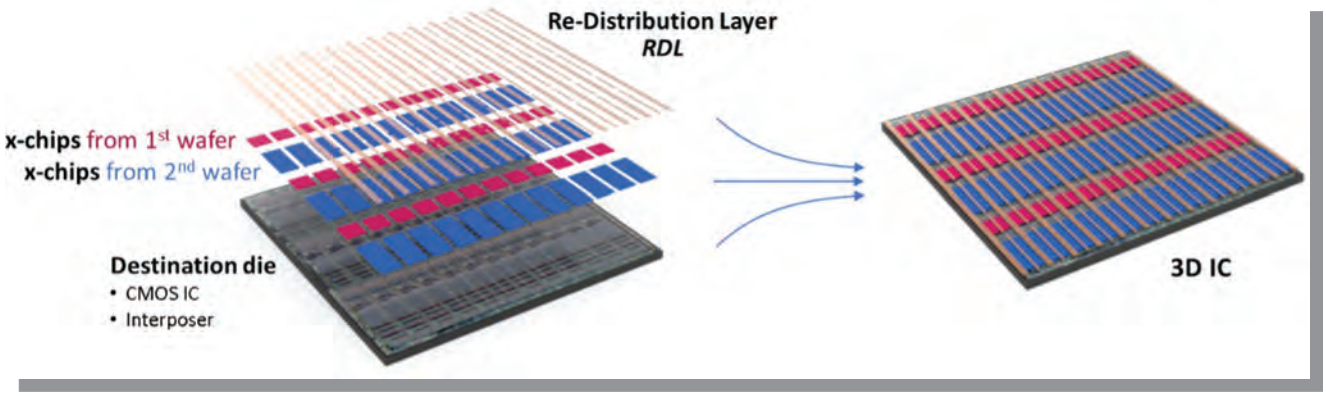
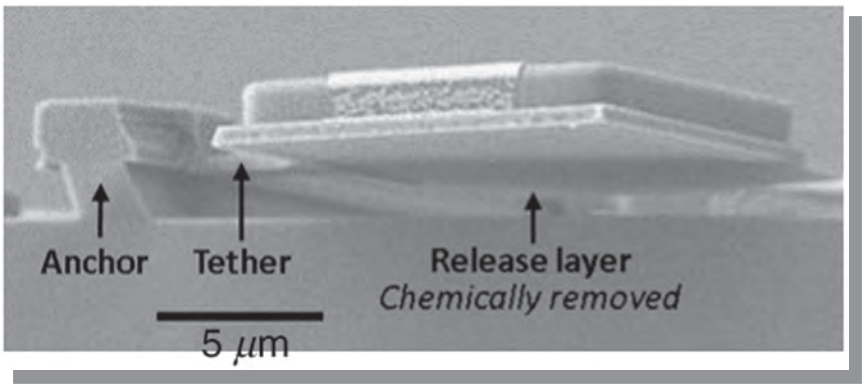


Figure 1. 3D IC made with MTP Technology.



`Figure 3. X-chip after chemical etch.

substrates. The post array on the stamp (Figure 5) is customized to match the desired destination substrate locations for massively parallel, selective pick-and-place of thousands of x-chips.

The stamp's posts adhere to the x-chips via van der Waals force. The stamp's viscoelastic behavior uses fast separation speed during pick-up to break the tethers and remove the x-chips, and slow separation speed to place the x-chips on the destination substrate. Using a "step and repeat" process, the entire destination substrate is populated with x-chips. The stamp can pick-and-place x-chips from smaller to larger wafers (Figure 6) with high wafer utilization, as the stamp readily handles x-chips at the wafer's edge.

The x-chips may be transferred from multiple source wafers to different locations within the same die on the destination wafer to combine components made using multiple process technologies (Figure 7). By adjusting the pattern and spacing of the small posts on the transfer stamp, the x-chips may be tightly-packed on the source wafer, reducing cost via high wafer utilization, and either tightly- or loosely-packed on the destination wafer.

4) MTP Pick-and-Place

An ultra-high precision pick and place tool developed by AMS Amicra is used to implement MTP technology via a high throughput, fully automatic ISO clean room class 10 system employing a 50 × 50 mm MTP stamp for massively parallel pick-and-place of x-chips from source wafers, which can be up to 300 mm, to destination substrates, which can be up to 300 mm wafers or 450 × 450 mm panels. Placement accuracy is plus-or-minus 1.5-microns

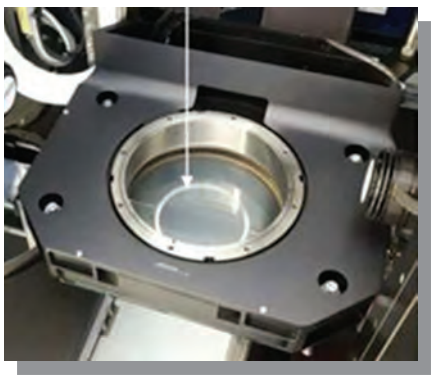


Figure 4. MTP stamp.

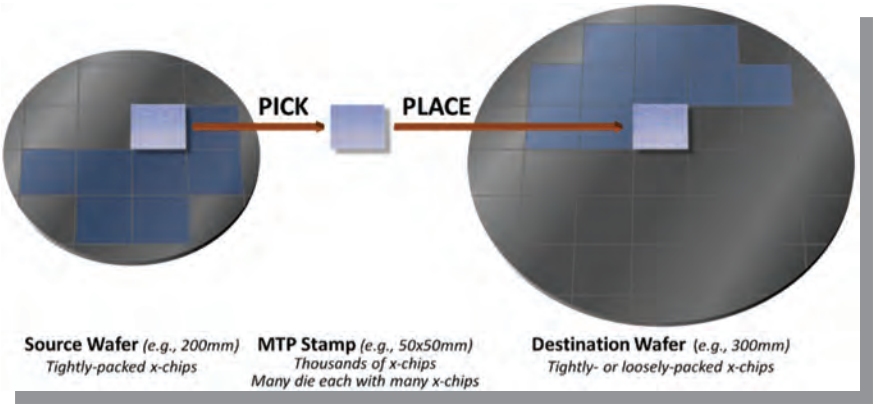


Figure 6. Transfer from smaller source wafer to larger destination wafer.

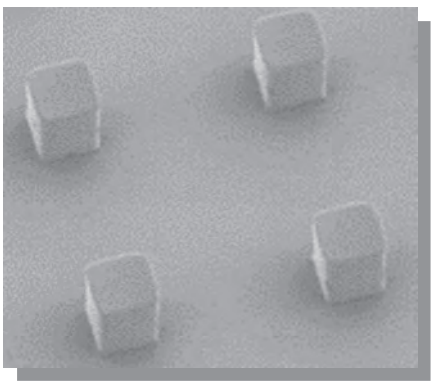


Figure 5. Close-up of MTP stamp's posts.

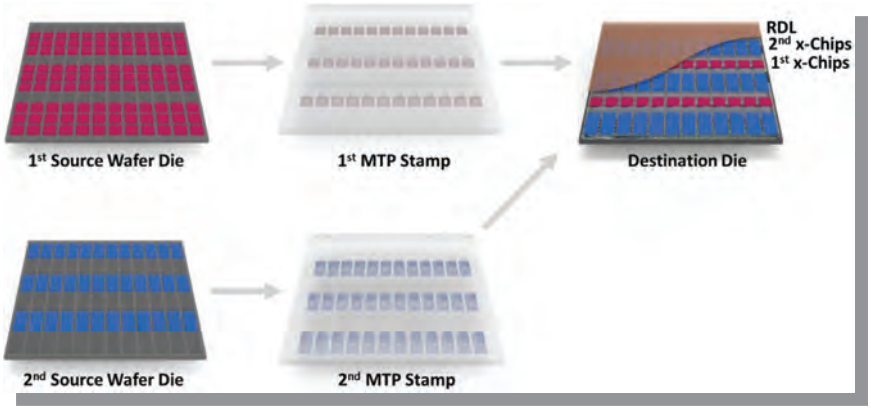


Figure 7. Single die close-up of transfer from two source wafers to a destination wafer.

Figure 8. High volume MTP manufacturing system developed by AMS Amicra; for details of inset see Fig. 12 caption.

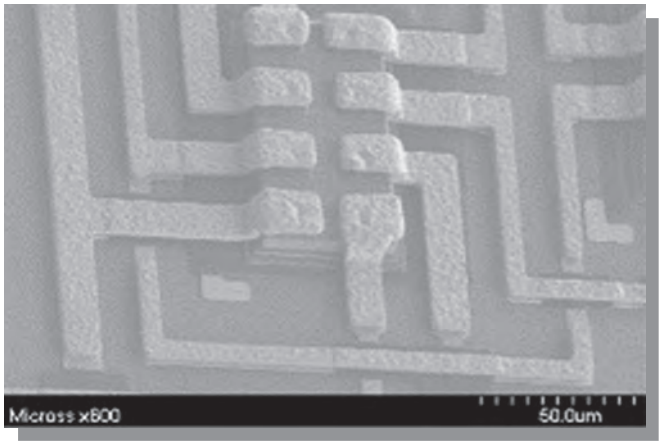


Figure 9. X-chip with RDL top view.

with a 40 second cycle time. Other implementations of the MTP technology include systems with higher placement accuracy (plus-or-minus 0.5-micron) and a low-volume system to serve R&D and specialized manufacturing markets.

5) Thin Film Interconnects

Since the x-chips are ultra-thin (1–20 micron), thin film interconnects may be readily used to connect the x-chips and destination die, resulting in very short path lengths, since both are active side up. Figures 9 and 10 show the top and cross section views of x-chips interconnected with a copper redistribution layer (RDL). The RDL provides a low electrical and thermal resistance path and enables use of multiple conventional and advanced packaging options.

Examples

Figures 11–16 show a wide variety of prototypes manufactured using MTP:

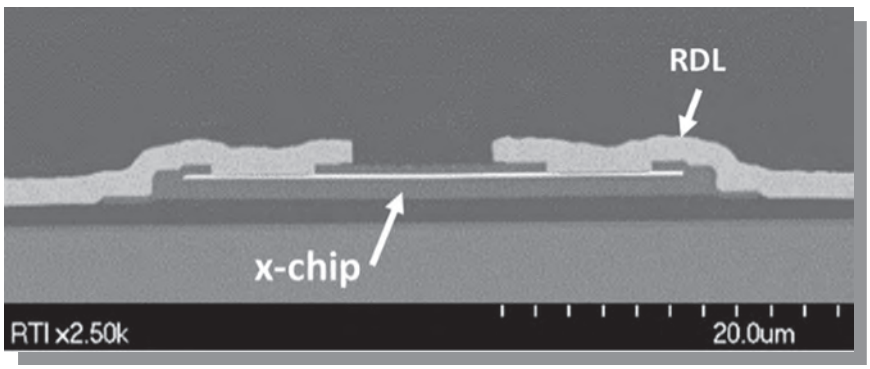


Figure 10. X-chip with RDL cross-section view.

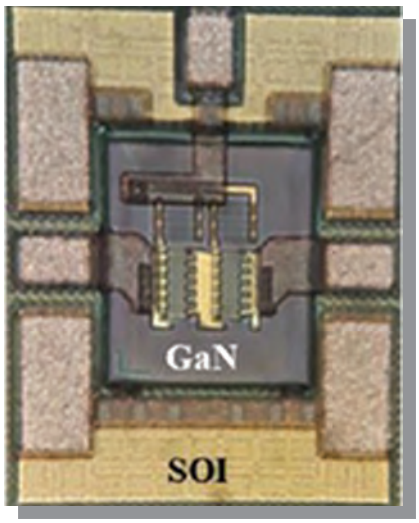


Figure 12. Drillet, F., Loraine, J., Saleh, H., … U'Ren, G. (2021). RF Small and large signal characterization of a 3D integrated GaN/RF-SOI SPST switch. Int. J. Microwave and Wireless Technol., 13(6), 517-522. doi:10.1017/S1759078721000076.

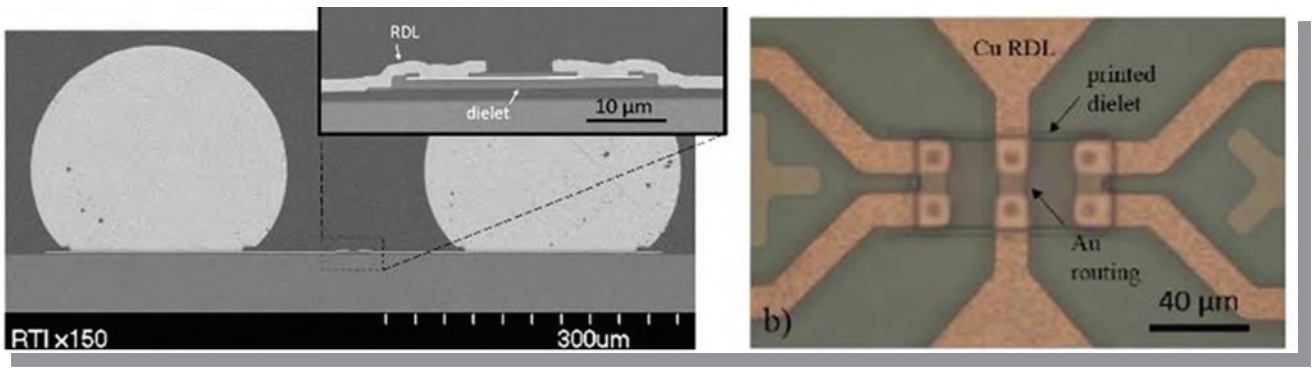


Figure 11. Fan-Out Packaging of Microdevices Assembled Using Micro-Transfer Printing (https://doi.org/10.1109/ECTC.2016.269).

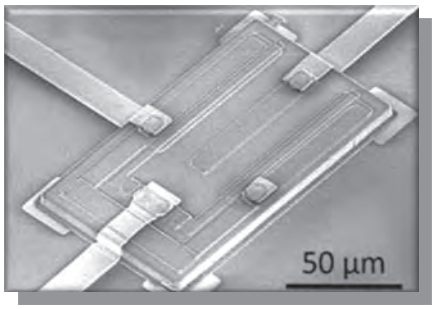


Figure 13. Integration of GaN HEMTs onto Silicon CMOS by Micro Transfer Printing (https://doi.org/10.1109/ISPSD.2016.7520875).

Figure 14. Mathews, I., Quinn, D., Justice, J., … Corbett, B., Microtransfer Printing High-Efficiency GaAs Photovoltaic Cells onto Silicon for Wireless Power Applications. Adv. Mater. Technol. 2020, 5, 2000048. https://doi.org/10.1002/admt.202000048. Copyright Wiley-VCH GmbH. Reproduced with permission.

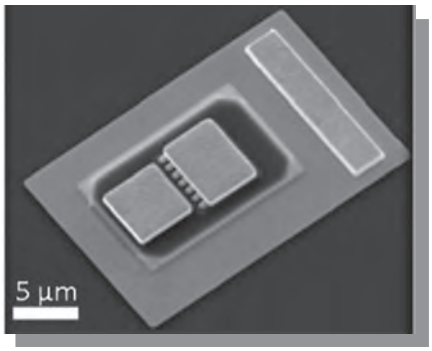


Figure 15. Microtransfer-Printed InGaAs/InP HBTs Utilizing a Vertical Metal Sub-Collector Contact (https://doi.org/10.1109/DRC46940.2019.9046426).

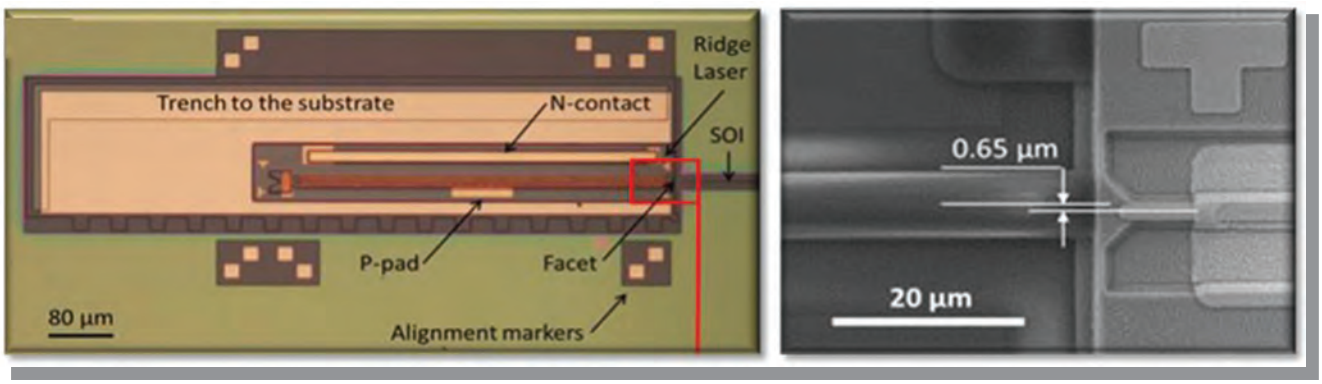
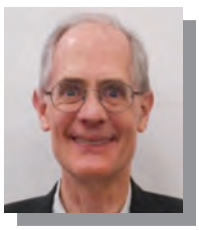


Figure 16. Edge-coupling of O-band InP etched-facet lasers to polymer waveguides on SOI by micro-transfer-printing (https://doi.org/10.1109/JQE.2019.2958365).

About the Authors



Bob Conner is VP of Business Development at X-Celeprint. Previously, he was CEO of Sarda Technologies and Symmorphix. Bob has held VP positions at Semprius, Nextreme, and Cirrus Logic and worked for Applied Materials, Intel, and GE. Bob earned his MBA at University of Chicago and BSME at Duke University.

Dr. Johann Weinhändler is Managing Director at ASM AMICRA. Previously, he has held different management positions at Oerlikon Systems, Datacon/Besi, and Lam Research.

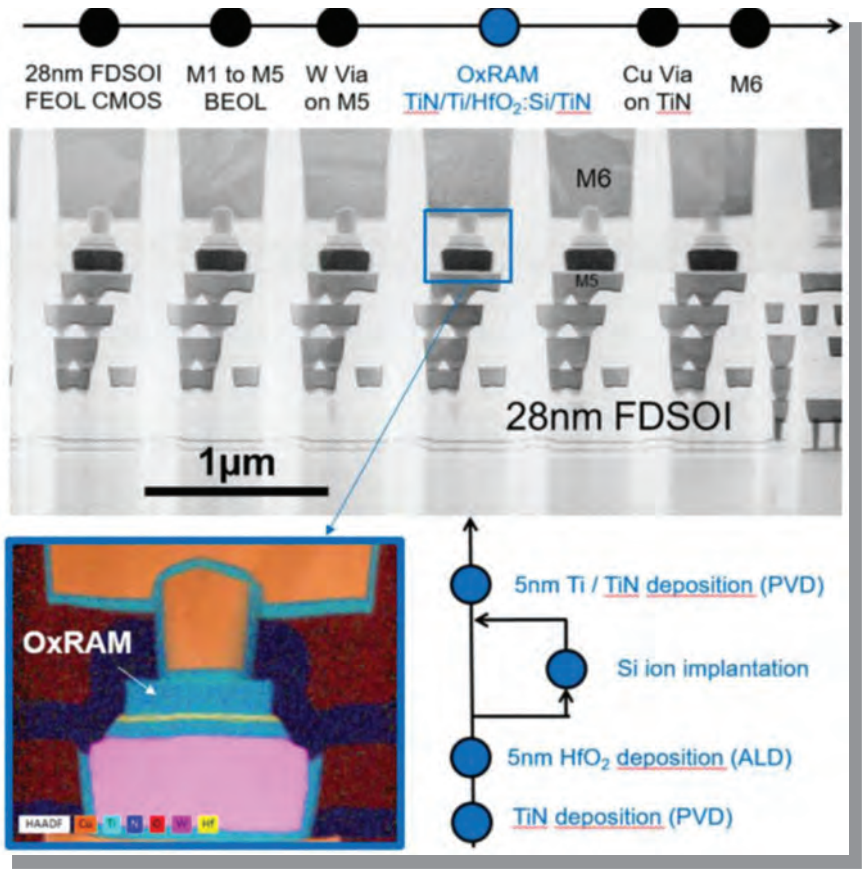
Johann earned his Ph.D at the Trinity Colleges Dublin and an MBA from the Open University Business School in the UK.

2021 IEEE International Memory Workshop (IMW)

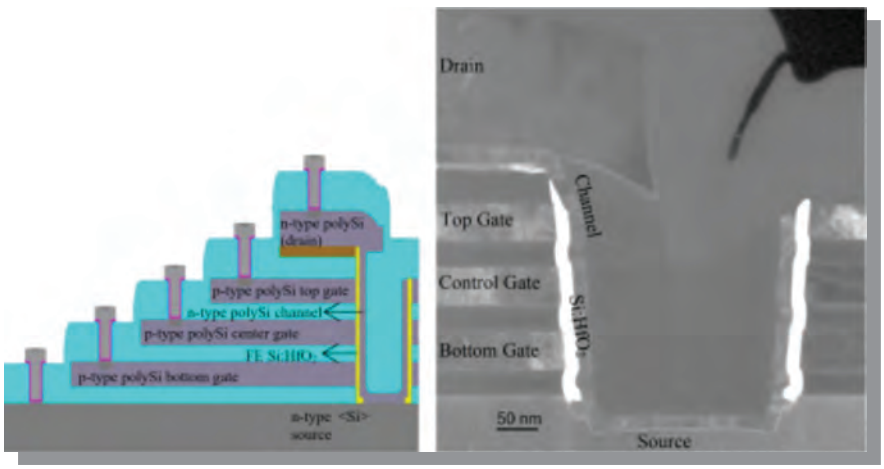
The Thirteenth IEEE International Memory Workshop (IMW) was held as a virtual event from 16–19 May 2021, due to the outbreak of COVID-19. The IMW is sponsored by the IEEE Electron Devices Society and meets annually in May. The workshop is a unique forum for specialists in all aspects of semiconductor memories (non-volatile & volatile). The target audience covers specialists from different areas of microelectronics and people with different backgrounds who wish to gain a better understanding of the field. More than 280 people took part in our virtual meeting this year. The technical sessions were organized in a manner of presentations and live Q&A that provided ample time for informal exchanges amongst presenters and attendees.

This year's program included a one-day short course chaired by Srivardhan Gowda from Intel and Tomoya Sanuki from Kioxia, with lectures on the New computing paradigms with memories and 3D memories-beyond Flash.

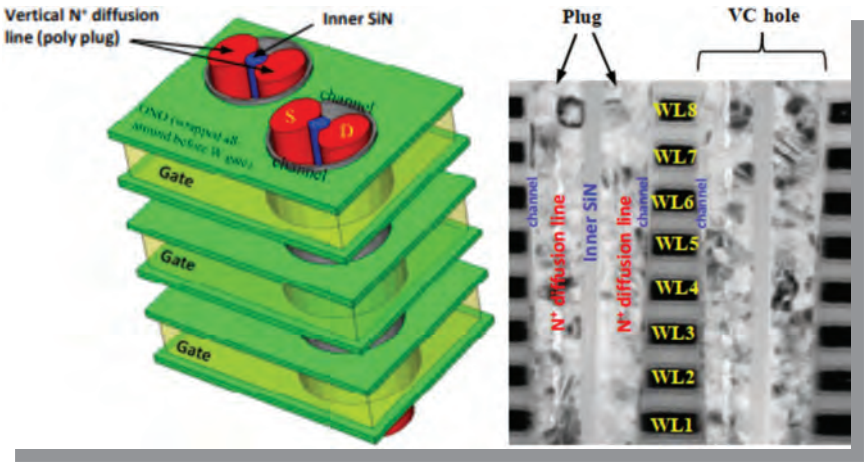
The single-track conference spanned three days, including a couple of invited talks given by experts in the memory field—X. Xu (Chinese Academy of Sciences), J. Okuno (Sony), D.H. Kim (Samsung), F. Schanovsky (Global TCAD Solutions), and J. J . Sun (Everspin)-providing an exciting overview of the main trends for memory technologies and applications. The IMW is also an excellent forum to present new and original technical works. This year's technical program comprised 28 excellent papers selected by the technical committee among more than 50 papers submitted and covering the major categories of memory technologies (NAND, DRAM, SRAM, ReRAM, FeRAM, MRAM, emerging technologies) and applications (Automotive, In memory computing). Among the most exciting news presented at the conference were, an



Embedded ReRAM compatible with 28 nm FDSOI technology (after: L. Grenouillet, et al., "16kbit 1T1R OxRAM arrays embedded in 28 nm FDSOI technology demonstrating low BER, high endurance, and compatibility with core logic transistors," DOI: 10.1109/IMW51353.2021.9439607).



Draft and cross-sectional view of 3D FE-FET with trench architecture (after: K.Banerjee, et al., "First demonstration of ferroelectric Si:HfO2 based 3D FE-FET with trench architecture for dense nonvolatile memory application", DOI: 10.1109/IMW51353.2021.9439620).



Draft and cross-sectional view of 3D AND-type flash memory cell (after: H.-T. Lue, et al., "Write-In-Place Operation and It's Advantages to Upgrade the 3D AND-type Flash Memory Performances", DOI: 10.1109/IMW51353.2021.9439621).

embedded ReRAM array compatible with 28 nm FDSOI technology, a 3D FE-FET with trench architecture for dense nonvolatile memory application, a 3D AND-type flash memory with the in-place page write time around 110 µsec.

The next IMW will be held in May 2022 in Dresden, Germany. For more details on the IMW conference please visit the IMW website (http://www.ewh. ieee.org/soc/eds/imw/). IMW technical proceedings are available on the IEEE Xplore database https://ieeexplore.ieee.org/xpl/conhome/9439548/proceeding.

Zhiqiang Wei
2021 IMW Publicity Chair
Avalanche

2021 IEEE International Electron Devices Meeting Highlights Educational Opportunities in Leading-Edge Semiconductor Technologies

At IEDM each year, the world's best scientists and engineers in nano/microelectronics gather to participate in a technical program consisting of more than 220 presentations, along with a variety of panels, focus sessions, Tutorials, Short Courses, a supplier exhibit, IEEE/EDS award presentations and other events highlighting leading work in more areas of the field than any other conference. The 67th IEDM is scheduled for 11–15 December 2021, under the theme "*Devices for a New Era of Electronics: From 2D Materials to 3D Architectures*."

While the comprehensive technical program for the 2021 IEEE International Electron Devices Meeting (IEDM) will be finalized soon, the popular IEDM Tutorials and Short Courses are already set. The broad reach, interdisciplinary nature and technical depth of the topics that will be discussed in these educational events can serve as a "crystal ball" of sorts to show where the industry is headed. For those who wish to get a jump on learning about the 67th IEDM, this news release provides descriptions of these educational offerings.

"As the COVID-19 pandemic has demonstrated, the world is becoming increasingly reliant on electronic technologies. The good news is that the IEDM Tutorials and Short Courses will provide attendees with the invaluable knowledge and information needed to advance the state-of-the-art in critical areas of the field," said Meng-Fan (Marvin) Chang, IEDM 2021 Publicity Chair, IEEE Fellow, Distinguished Professor of Electrical Engineering at National Tsing Hua University, and Director of Corporate Research at TSMC. "The opportunity to engage with the world's technical leaders in these highly specialized areas is one of the hallmarks of the IEDM conference."

"New, fast-growing electronics applications often require novel semiconductor solutions," said Srabanti Chowdhury, IEDM 2021 Publicity Vice Chair and Associate Professor of Electrical Engineering at Stanford University. "The IEDM Tutorials and Short Courses represent a great opportunity to explore evolving areas of the field, with topics that include novel materials and device types; advances in process and packaging technologies; new design approaches; and much more."

IEDM Tutorials—Saturday, December 11

Now in their 12th year, the 90-minute Saturday tutorial sessions on emerging technologies and specialized topics have become a hugely popular part of IEDM. They are presented by experts in the respective areas, the goal being to bridge the gap between textbook-level knowledge and leading-edge current research. The topics for 2021 are:

2:45 p.m.–4:15 p.m.

- *Beyond the FinFET Era: Challenges and Opportunities for CMOS Technology*, Kai Zhao, IBM
- *TCAD-Based DTCO and STCO*, Asen Asenov, University of Glasgow
- *6G Technology Challenges from Devices to Wireless Systems*, Aarno Pärssinen, Oulu University

4:30 p.m.–6:00 p.m.

- *Selective and Atomic-Scale Processes for Advanced Semiconductor Manufacturing*, Robert Clark, TEL
- *Machine Learning for Semiconductor Device and Circuit Modeling*, Elyse Rosenbaum, University of Illinois, Urbana-Champaign
- *GaN Power Device Technology and Reliability*, Dong Seup Lee, Texas Instruments

IEDM Short Courses—Sunday, December 12

In contrast to the Tutorials, the full-day IEDM Sunday Short Courses are focused on a single technical topic. Early registration is recommended, as they are often sold out. They offer the opportunity to learn about important areas and developments, and to network with global experts.

- **Future Scaling and Integration Technology**, organized by Dechao Guo, IBM Research
  - *Processes and Materials Engineering Innovations for Advanced Logic Transistor Scaling*, Benjamin Colombeau, Applied Materials
  - *Interconnect Resistivity: New Materials*, Daniel Gall, Rensselaer Polytechnic Institute
  - *Metrology and Material Characterization for the Era of 3D Logic and Memory*, Roy Koret, Nova Ltd.

- *Beyond FinFET Devices: GAA, CFET, 2D Material FET*, Chung-Hsun Lin, Intel
- *Heterogeneous Integration Using Chiplets & Advanced Packaging*, Madhavan Swaminathan, Georgia Tech
- *Design-Technology Co-Optimization/System-Technology Co-Optimization*, Victor Moroz, Synopsys

- **Emerging Technologies for Low-Power Edge Computing,** organized by Huaqiang Wu, Tsinghua University and John Paul Strachan, Forschungszentrum Jülich
  - *Mobile NPUs for Intelligent Human/Computer Interaction*, Hoi-Jun Yoo, KAIST
  - *Brain-Inspired Strategies for Optimizing the Design of Neuromorphic Sensory-Processing Systems*, Giacomo Indiveri, University of Zurich
  - *Memory-Based AI & Data Analytics Solutions*, Euicheol Lim, SK hynix
  - *Material Strategies for Memristor-Based AI Hardware and their Heterointegration*, Jeehwan Kim, MIT
  - *RRAM Devices for Data Storage and In-Memory Computing*, Wei Lu, University of Michigan
  - *Practical Implementation of Wireless Power Transfer*, Hubregt Visser, IMEC

Vendor Exhibition/Poster Sessions

- A vendor exhibition will be held once again in conjunction with the technical program.

Further information about IEDM

For registration and other information, visit www.ieee-iedm.org.

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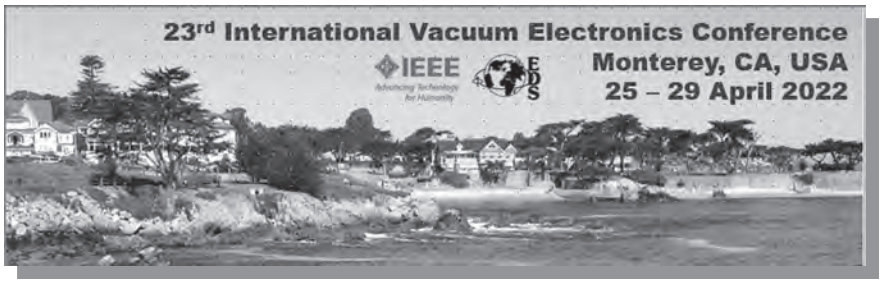
Gary Dagastine
Dagastine & Co. PR
gdagastine@nycap.rr.com

Chris Burke
BtB Marketing Communications
chris.burke@btbmarketing.com

23rd International Vacuum Electronics Conference (IVEC 2022)



On behalf of the IVEC 2022 Organizing Committee, we are pleased to announce that the Twenty-Third International Vacuum Electronics Conference (IVEC) will be held in Monterey, California, from 25–28 April 2022. In addition to the traditional in-person conference format, virtual access will be available for presenters and attendees who cannot travel to Monterey.

Plenary talks will provide insights into the history, emerging technology, and future directions of vacuum electronics. The conference will include invited and contributed papers and posters on topics ranging from the fundamental physics of electron emission and modulated electron beams to the design and operation of advanced devices at UHF to THz frequencies. In addition, presentations on the development of computational tools for vacuum electron device (VED) design, supporting technologies, and VED-based systems will be made. IVEC provides a unique snapshot of the current state-of-the-art of VEDs, devices that continue to produce unmatched power and performance at frequencies up to and including the THz band.

A one-day minicourse, with tutorials offered by international vacuum electronics experts, will be held on 25 April 2022. The mini-course will also be accessible to remote participants. The John R. Pierce Award for Excellence in Vacuum Electronics, the Vacuum Electronics Young Scientist Award, and a Student Paper Award will be presented at the conference.

The most up-to-date information about the conference can be found at ieeeivec.org.

We invite you to submit papers on your work and experiences in vacuum electronics and electron sources, and we hope to see you all in Monterey or online for IVEC 2022.

Jack Tucek
2022 IVEC General Chair

IEEE International Reliability Physics Symposium 2022

Mohsen Alavi
Corporate VP and GM of Quality & Reliability, Intel

Shankar Krishnamoorthy
GM, Digital Design Group, Corporate Staff, Synopsys

Nagasubramaniyan Chandrasekaran
Senior VP, Technology Development, Micron

Jun He
VP Corporate Quality & Reliability, TSMC

The IEEE International Reliability Physics Symposium (IRPS) is the world's premier forum for leading-edge research addressing developments in the Reliability Physics of devices, materials, circuits, and products used in the electronics industry. IRPS is the conference where **emerging reliability physics challenges and practical solutions** to achieve realistic **end-of-life projections and mitigation** are first discussed.

In 2022, the IRPS will be held **27–31 March at the Hilton, Dallas, Texas**. Over the course of the conference, IRPS will offer a blended mix of keynote talks, tutorials, year-in-reviews, workshops, vendor exhibits, and technical presentations. **Abstracts are due by 23 October 2021. Late breaking news submissions are welcome by 23 January 2022**.

The IRPS draws presentations and attendees from industry, academia and governmental agencies worldwide. No other meeting presents as much leading work in so many different areas of reliability of electronic devices, encompassing silicon device, non-silicon device, process technology, nanotechnology, optoelectronics, photovoltaic, MEMS technology, circuits and systems reliability including packaging. IRPS 2022 is **soliciting increased participation** in the following areas: **Circuit Reliability and Aging, Reliability of RF/mmW/5G Devices, System Electronics Reliability, and Neuromorphic Computing Specific Reliability Issues**.

IRPS 2022 will be kicked off by keynote presentations from reliability experts at Intel, Synopsys, Micron, and TSMC, covering the latest reliability trends and mitigation approaches from various industry perspectives.

Further opportunities at the symposium include:

- **Tutorial Program**. The IRPS tutorial program is a comprehensive event designed to help both the new engineers and experienced researchers. The program contains both beginner and expert tracks and is broken down into topic areas that allow the attendee to participate in tutorials relevant to their work with minimal conflicts between subject areas.
- **Year-in-Review Session**. These seminars provide a summary of the most significant developments in the reliability community over the past year. This serves as a convenient, single-source of information for attendees to keep current with the recent reliability literature. Industry and academic experts serve as the "tour guides" and save you time by collecting and summarizing this information to bring you up to date in a particular area as efficiently as possible.
- **Poster Reception**. The poster session provides an additional opportunity for authors to present their original research. The setting is informal and allows for easy discussion between authors and other attendees.
- **Workshops**. These workshops enhance the symposium by providing the attendees an opportunity to meet in informal groups to discuss key reliability physics topics with the guidance of experienced moderators. Some of the workshop topics are directly coupled to the technical program to provide a venue for more discussion on the topic.
- **Vendor Exhibits**. Held in parallel with the technical sessions, the equipment demonstrations provide a forum for manufacturers of state-of-the-art laboratory equipment to present their products. Attendees are encouraged to visit the manufacturers' booths for information and demonstrations.
- **IRPS Paper Awards**. IRPS bestows awards for Best Paper, Best Student Paper, Best Posters, and People's Choice.
- **IEW Co-Location**. This year the IRPS will be co-located with the International ESD Workshop (IEW). Now in its 16th year, the IEW provides a relaxed, invigorating atmosphere to present new work and engage in discussions about the latest issues confronting the ElectroStatic Discharge (ESD) and Electrostatic OverStress (EOS) communities.

For the call for papers and other information, visit the IRPS 2022 home page at www.irps.org or join the IRPS linked-in group.

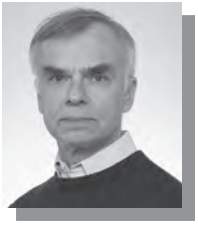
The IRPS committee members look forward to seeing you in Dallas, Texas!

Charlie Slayman
2022 IRPS General Chair
Cisco Systems

Chris Kim
2022 IRPS Publicity Chair
University of Minnesota

Society News

Message from EDS Newsletter Editor-in-Chief



Daniel Tomaszewski
EDS Newsletter
Editor-in-Chief

Dear Readers, Members of the IEEE EDS Community, Welcome to the IEEE EDS Newsletter issue October 2021. I am very glad to introduce this issue to you.

First, I would like to draw your attention to the Tribute to Prof. T.P. Ma who passed away on 6 April 2021.

In the *Technical Briefs* section we continue the presentation of articles on emerging technologies and devices, which, I believe, may be of interest to you. This time you can read an interesting material introducing the Micro-Transfer Printing (MTP) technology, which employs a massively parallel pick-and-place process to stack large arrays of ultra-thin (1–20 micron) diverse components from one or more separately manufactured wafers on a variety of destination substrates to improve heterogeneous integration to create 3D ICs. Except for the material on MTP, we also present a brief report on 2021 IEEE International Memory Workshop (IMW).

In this issue we share with you further details of the IEDM 2021 program and announce two technical conferences that will be held next year, namely IRPS 2022, and IVEC 2022.

In the sections *EDS Women in Engineering (EDS WiE)* and *EDS Young Professionals* (EDS YP) we continue to present outstanding female researchers. I believe that their impressive achievements in different domains, and their thoughts and suggestions may be inspiring, in particular to the young members of EDS. In this issue the WiE section includes two articles presenting Prof. Elyse Rosenbaum and Prof. Deblina Sarkar, whereas the YP section includes excerpts of the interview that Manoj Saxena made with Dr. Pragya Kushwaha.

The *Regional News* and *Chapter News* sections bring information about continuous daily activities of numerous EDS chapters from most of the parts of Regions 8, 9, 10. I deeply appreciate the efforts of all those chapters that delivered materials for the issue. It is worth mentioning that the *Chapter News* section includes this time four articles concerning two aspects: a help of EDS members and student-members to communities touched by COVID-19 pandemic, and efforts of researchers and engineers involved in the state of the art technologies, to cope with a progressing climate destruction and its effects. Undoubtedly, these plagues are great threats for our ecosystem.

Dear Readers, in May and June, 2021 we carried out a series of four WebEx meetings with the Regional Editors responsible for the Newsletter cooperation with different Regions. Therefore, the Vice President of Regions & Chapters, representatives of the Regions & Chapters Committee and Subcommittee for Regions & Chapters were also present. The meetings were organized by Joyce Lombardini, who coordinates the Editorial Team work. A goal of the meetings was to get to know each other better, recognize the needs of the Editors, answer their questions, and share with them expectations concerning both cooperation with the assigned chapters and cooperation with the Editor-in-Chief, Associate Editor-in-Chief, and the Team coordinator. I believe that the meetings were fruitful. We were able to discuss and improve recommendations for the Editorial Team, in particular for the Regional Editors. I am very grateful to them for their efforts. I am happy that the recently appointed Regional Editors do also an excellent job.

Dear Readers, if you have any suggestions, comments regarding the Newsletter contents, please do not hesitate to contact me or Manoj Saxena. We will be very glad to receive your feedback. As you can see, in this issue a rubric *Letters to the Editor* has appeared. Your questions and our answers will be presented there.

Finally, I would like to express again my thanks to all the article Authors and to all the members of the Editorial Team. I hope that the Readers will find the issue interesting.

Sincerely,
Daniel Tomaszewski

In Memory of Prof. T.P. Ma

By Mukesh Khare, Huiming Bu, Dechao Guo, and Terry Hook, IBM Research

Tso-Ping (T.P.) Ma, the Raymond J. Wean Professor of Electrical Engineering and Applied Physics at Yale University for 44 years, passed away peacefully on April 6, 2021, at the age of 75, after a brief illness. He left behind his wife of 49 years, Dr. Pin-Fang Ma, his children Mahau Ma and Jasmine Ma, and a legacy of mentoring countless students, of which many have become prominent and groundbreaking leaders in the semiconductor industry. Although Ma spent a relatively short time at IBM, his former Yale students make up a talented and appreciative cohort within IBM Research.

Terry Hook, Senior Technologist at IBM, fondly recalls a time at Yale when he accidentally spent more than $20,000 in computer time in one month. "I don't know how they solved that problem, but TP shielded me from the consequences. He forever loved that story and enjoyed roasting me when we encountered one another at conferences around the world in the following years. He even defined a new metric of computer usage: one "Hook" is $20,000 worth of CPU time."

Ma was born on November 13, 1945, in Lanzhou, China and graduated from National Taiwan University in 1968. He completed his Ph.D. degree at Yale University in 1974, then joined IBM for a few years before returning to Yale as a faculty member in 1977. He focused his research and teaching on semiconductors, CMOS technology, and nanoelectronics, and over the years received numerous awards and honorary degrees for his achievements, including election to the US National Academy of Engineering, a Foreign Member of the Chinese Academy of Sciences, an Academician of the Academia Sinica in Taiwan, and a life Fellow of the Institute for Electrical and Electronic Engineering (IEEE). He also received the 2008 Connecticut Medal of Technology, the 2006 Semiconductor Industry Association University Researcher Award, the 2005 IEEE Andrew S. Grove Award, and a 2005 Pan Wen-Yuan Research Award.

Prof. Tso-Ping Ma
(November 13, 1945–April 6, 2021)

One notable story from his time at IBM was recounted by Huiming Bu, Vice President Semiconductor Technology Research and Director Albany Lab. "Ma and one of his IBM colleagues discovered the ionizing radiation effects in MOS devices, after failing many times to cure defects by trying all kinds of furnace annealing techniques. One day he decided to put the silicon wafer in a microwave, and surprisingly it worked. "Of course, nowadays you can't put a 12" wafer in a microwave as the size doesn't fit," Ma would add."

Ma was an internationally recognized pioneer for his contributions to semiconductor science and technology—in particular, breakthroughs in advanced gate dielectrics, which paved the path for high-k dielectrics and extended the scaling of CMOS technology. His research also generated fundamental and lasting impacts on many other applied physics fields, notably ferroelectrics and ionizing radiation sciences.

"As the father of high-k gate dielectrics, Professor T.P Ma will be deeply remembered as an influencer, a mentor, and a friend by the semiconductor world", said Dechao Guo, Director Advanced Logic Technology Research. "At conferences, workshops and seminars, Ma was always surrounded by friends from the industry and academia. People always enjoyed interactions with him, for his view on technology, his stories of the semiconductor industry, his sense of humor, and his inspiring advice."

Mukesh Khare, Vice President of Semiconductor, Systems, and Cloud, credits Ma with "inspiring me to take challenges, and coaching me all the way to the finish line, with his trademark humility and humor. He would take students to "Naples Pizza" to celebrate every occasion, and I would attempt to speak in a Chinese dialect. This became a tradition, and TP would burst out laughing every time. "Nǐ yǒngyuǎn shì wǒ xīnzhōng de yīngxióng" (You will always be my hero)."

For many of us who had the opportunity to interact with him in person, Ma was a scholar with a sharp mind, a mentor with great wisdom, and a person with a kind heart. He will be dearly missed by the semiconductor community, and all who benefitted from his humanity.

Letters to the Editor

Dear Dr. Tomaszewski,
I was reading the Technical Briefs: Beyond CMOS, and I was wondering why technology, devices and circuits for THz electronics (>100 GHz) were not even mentioned (this part felt during the IRTS in the More than Moore section). Is this topic out of scope within the International Roadmap for Devices and Systems (IRDS)?

With kind regards
Thomas Zimmer
(University Bordeaux)

Dear Prof. Thomas Zimmer,
I am very glad that the recent article in the series based on IRDS International Focus Team (IFT) reports has drawn your attention and triggered your comment with some criticism.

The THz electronics topic appeared in two IRDS IFT reports, namely "Cryogenic Electronics and Quantum Information Processing" (e.g. for astronomy applications), and "Outside System Connectivity" (for communication at very high frequencies).

It is the intention of the IRDS teams led by Dr. Paolo Gargini to present all their reports in the Newsletter. The EDS Newsletter team is also very interested in introducing IRDS reports to the EDS community. So, I believe you will be able to read Technical Briefs including THz electronics in the future Newsletter issues.

With kind regards,
Daniel Tomaszewski (Newsletter EiC)

A Message from Vice President of Publications and Products

Dear Fellow EDS Members:

Joachim N. Burhartz
EDS Vice President of Publications and Products

It is my great pleasure to update you on the status and the ongoing activities around our EDS publications. Our flagship journals, the *IEEE Transactions on Electron Devices* (T-ED), the *IEEE Electron Devices Letters* (ED-L), and the *IEEE Journal of the Electron Devices Society* (J-EDS), continue to do very well under the outstanding leadership of the respective Editor-in-Chiefs (EiCs), Giovanni Ghione for T-ED, Jesus del Alamo for ED-L and Enrico Sangiorgi for J-EDS. ED-L has been steadily increasing its impact factor to 4.187 now (5-year average is 3.967), and T-ED and J-EDS have maintained their impact factors of 2.9 and 2.5, respectively. The real strength of our flagship journals, however, are their superior turn-around times, which are a great value to authors. ED-L, aiming particularly at rapid publication of letters, forwards accepted manuscripts to ePublication after only 3.9 weeks from submission, while T-ED and J-EDS have constant figures of 13.4 and 11.8 weeks, respectively, which are well in line with their 5-year averages. Our publications also perform very well in terms of usage. When considering PDF downloads and HTML views in Xplore, ED-L, T-ED and J-EDS are ranking at positions 24, 10, and 102, respectively, out of 383 IEEE publications overall (2019 figures).

Also, our co-sponsored journals do very well, having ranks between 28 and 125. In cases where the journal's performance declined during past years, though the scope and industrial relevance is high, we started new initiatives. This applies to the Transactions on Display Technology (T-DT) which are intended to succeed the Journal of Display Technology (J-DT), formerly owned by the Photonics Society. An LOI has been approved by the EDS Board of Governors (BoG) and was submitted recently. Launching a co-sponsored publication can be a major effort, as seen with the new IEEE Journal on Flexible Electronics (J-FLEX). It took more than two years of planning, negotiations and approval by the IEEE Periodicals Review and Advisory Committee (PRAC) to finally launch this new and very timely publication which is co-sponsored by EDS, the Sensors Council (SC), and the Circuits and Systems Society (CAS). The two founding editors are Ravinder Dahiya from SC and Paul Berger from EDS; the journal's steering committee is chaired by Sandro Carrara from CAS. We are now looking forward to a highly successful new journal that can well be associated with the two IEEE conferences IFETC and FLEPS.

Another topic that currently receives a lot of our attention is the consideration of an EDS Magazine. Numerous IEEE societies offer such magazines to their members as a society benefit, meaning that electronic subscription is free to them and that printed copies can be purchased

with a substantial discount. Some societies offer both a magazine and a newsletter, while others prefer to merge those contents into a magazine only. Yet quite a few societies just offer a newsletter, such as we do at EDS. Our newsletter has emerged from a communication media to a publication that is enriched by technical articles and historical reviews, such as the series on 'marvels of microelectronic engineering' from July 2018 through January 2020. The key difference between a newsletter and a magazine is that a magazine is to be treated as an IEEE publication with access through Xplore, while a newsletter is owned by the society. That means that a magazine can achieve an impact factor due to technical and review articles published. In some cases, IEEE magazines have reached impact factors beyond 10. A magazine also offers opportunities to publish articles of practical value to industry, articles about celebrated society members, and on many more topics that are not covered by our flagship publications or by our newsletter. It should be pointed out that the new EDS Magazine should not be compared to the former Circuit & Devices Magazine which was co-sponsored by the IEEE societies EDS, CAS, LEOS, and CPMT. This was a magazine of IEEE Division-I rather than a society magazine as we target now. The current plan is to take the steps towards launching the EDS Magazine, which has been approved by BoG and will be prepared for PRAC approval, in coexistence with our successful EDS Newsletter. This will be a major effort but we will look forward to providing the EDS Magazine as a benefit to our existing members and help attracting other IEEE members to join EDS.

Finally, I want to take the opportunity to thank the Editors-in-Chief of our flagship journals and of our co-sponsored publications, as well as the associate editors and peer reviewers involved, for their outstanding service to our society. I would like to acknowledge the EDS staff and the IEEE publications staff for their excellent support.

I would very much welcome comments and suggestions related to our EDS publications.

Joachim N. Burghartz
EDS Vice President of Publications and Products
e-mail: burghartz@ims-chips.de

Message from EDS Vice President of Membership and Services

Patrick Fay
EDS Vice President of Membership and Services

As I write this, we are more than a year into the pandemic and many aspects of our lives—both personal and professional—have been disrupted in many ways. It is my sincere hope that the members of our "EDS family" find the support and care they need to persevere in challenging times. While of course the health and safety of all our members and their families, friends, and colleagues are at the forefront of our thoughts, EDS members have continued to work to advance the state of the art in electron devices through research and industrial efforts. In that same spirit, EDS members and volunteers have also ramped up their efforts to continue to serve you, our members, despite the challenges we collectively face. Recognizing that some of our traditional venues for education and interaction have been disrupted, EDS has significantly expanded our educational webinar series (https://eds.ieee.org/education/webinars). Featuring a wide range of topics of interest to EDS members and presented by leading practitioners and researchers, these webinars offer our members unique educational opportunities. Our podcast series (https://eds.ieee.org/education/podcasts) is another excellent way to gain insights and perspective from leaders in the electron devices field. While we all look forward to the time when we can resume in-person conferences, symposia, and workshops, in the interim EDS members and volunteers have made tremendous efforts to host high-quality conferences; while the circumstances have required that these be hosted on-line or in hybrid formats, they continue to provide opportunities for networking, learning, and stimulating new ideas for participants. I encourage everyone to check out EDS's social media feeds (Facebook, Twitter, LinkedIn, and Instagram) for the latest news, opportunities, and initiatives.

Speaking of new initiatives, I would like to call your attention to two new programs that may be of interest. For students, the "EDS Awarded Student Membership" program is designed to recognize students that contribute to the IEEE and EDS missions. Students involved/engaged in EDS activities, and studying topics within the EDS areas of interest, can be nominated for these awards. I encourage you to nominate worthy candidates for these recognitions; the details can be found online (https://eds.ieee.org/members/eds-awarded-student-membership-program). A second initiative focuses

on supporting our chapters to grow, try new things, and flourish. This "EDS Special Membership Growth" program is intended to fund new, experimental activities by groups or chapters that will help to enhance the participation of students, young professionals, women, and under-represented communities (i.e., ethnic, social, or economic groups that are under-represented in EDS membership). These can be one-time or multi-year initiatives but must be creative and new ideas that can expand the appeal of EDS and help our society grow. The details are available online (https://eds.ieee.org/members/eds-chapter-membership-growth-program). Finally, while not a new initiative, I would like to encourage eligible members to consider applying for Senior Member status. If you have been in professional practice for 10 years or more (including credit for college-level education), you may be eligible. Senior member status is the highest grade of membership for which an individual can apply and is a mark of distinction that is widely recognized professionally. EDS chapters may also wish to coordinate Senior Member recruiting events to strengthen their local chapter profile. Please see https://eds.ieee.org/members/eds-senior-member-program for full program details.

Finally, I'd like to take this opportunity to note that since our goal as a society is to serve you, our members, I hope you will let me, or other members of the membership committee know if you have thoughts or ideas that would improve the value of the society for you. EDS is well-established and very active in providing high-quality publication venues (including Electron Device Letters, Transactions on Electron Devices, the Journal of the Electron Devices Society, Transactions on Semiconductor Manufacturing, the Journal of Microelectromechanical Systems, Transactions on Device and Materials Reliability, and the Journal of Photovoltaics), as well as premier electron-device focused technical conferences, educational opportunities such as the distinguished lecture series and webinars, and outreach and service opportunities. But we are very interested in expanding the services and benefits that we can provide to our members, and we very much value any suggestions you have. The current membership committee consists of Shuji Ikeda, Benjamin Iniguez, Carmen Lilley, Durga Misra, Angele H. M. E. Reinders, Mike Schwarz, and Bin Zhao. I hope you will pass along your thoughts or suggestions directly to me or to any of us on the committee (https://eds.ieee.org/about-eds/governance/standing-committees/membership-committee).

Patrick Fay
EDS Vice President of Membership and Services
University of Notre Dame
Indiana, USA
e-mail: pfay@nd.edu

EDS Optoelectronic Devices Technical Committee Report

Can Bayram
Chair of the EDS Optoelectronic Devices Committee

Optoelectronic Devices Technical Committee serves the society in the areas of light and light—matter interactions through organizing webinars, creating special invited issues in the EDS journals, and contributing to the conferences through organizing special sessions. In the wake of the COVID-19 pandemic, we witnessed increased responsibilities in teaching, research, and at home. The TC continues to support the IEEE and EDS Missions through newsletter contributions and webinar organizations. Recent topics covered include photovoltaics, opto-electro-mechanics, detectors, and emitters and (recently archived 7+) webinars are available for viewing at your convenience. On a path towards (re) normalization, the TC will benefit from the pandemic era learning and continue to build its online content as traditional in-person engagement mechanisms are being (re)vitalized. Recent needs in photonic disinfection and the continuous goal of going carbon-neutral reassures the value of fundamental and applied research in optoelectronics to enable energy-efficient and scalable solutions to the grand challenges in energy, communication, and health.

Can Bayram
Chair of the EDS Optoelectronic Devices Committee
e-mail: cbayram@illinois.edu

2020 EDS George E. Smith Award

A high priority of the IEEE Electron Devices Society (EDS) is to recognize and enhance the quality of papers published in EDS archival literature. The George E. Smith Award was established in 2002 to recognize the best paper appearing in a fast turnaround archival publication of EDS, targeted to the *IEEE Electron Device Letters*. Among other criteria including technical excellence, an important metric for selection for the Award is comprehensive and impartial referencing of prior art.

The paper winning the 2020 George E. Smith Award was selected from over 420 articles that were published in 2020. The paper is entitled, "***Theoretical Limit of Low Temperature Subthreshold Swing in Field-Effect Transistors***." This paper appeared in the February 2020 issue of the *IEEE Electron Device Letters* and authored by Arnout Beckers, Farzan Jazaeri and Christian C. Enz.

The Award will be presented during the IEEE International Electron Devices Meeting to be held in December 2021. In addition to the Award certificate, the authors will receive a check for $2,500 to be shared equally among all authors. On behalf of the IEEE Electron Devices Society, I would like to congratulate the authors for this achievement.

Joachim Burghartz
EDS Vice-President of Publications and Products

2020 EDS Paul Rappaport Award

A high priority of the Electron Devices Society (EDS) is to recognize and enhance the quality of papers published in EDS archival literature. Every year, the Society confers its prestigious Paul Rappaport Award to the best paper published in the *IEEE Transactions on Electron Devices*. Among other criteria including technical excellence, an important metric for selection for the Award is comprehensive and impartial referencing of prior art.

The winning paper was selected from over 850 articles that were published in 2020. The winning paper is entitled "*Improved Air Spacer for Highly Scaled CMOS Technology*". This paper was published in the December 2020 issue of the *IEEE Transactions on Electron Devices*, and was authored by Kangguo Cheng, Chanro Park, Heng Wu, Juntao Li, Son Nguyen, Jingyun Zhang, Miaomiao Wang, Sanjay Mehta, Zuoguang Liu, Richard Conti, Nicholas J. Loubet, Julien Frougier, Andrew Greene, Tenko Yamashita, Balasubramanian Haran and Rama Divakaruni.

The Award will be presented during the IEEE International Electron Devices Meeting to be held in December 2021. In addition to the award certificate, the authors will receive a check for $2,500 to be shared equally among all authors. On behalf of the Electron Devices Society, I would like to congratulate the authors for this achievement. Brief biographies of some of the authors follow.

Joachim N. Burghartz
EDS Vice-President of Publications and Products

2020 EDS Leo Esaki Award

The Leo Esaki Award was established in 2019 to recognize the best paper appearing in a fast turn around archival publication of the IEEE Electron Devices Society, targeted to the *IEEE Journal of Electron Devices Society*. Among other criteria including technical excellence.

The paper winning the 2020 Leo Esaki Award was selected from over 199 articles that were published in 2020. The paper is entitled, ***"A New 8T Hybrid Nonvolatile SRAM with Ferroelectric FET."*** This paper appeared in the February 2020 issue of the *IEEE Journal of the Electron Devices Society* and authored by Wei-Xiang You, Pin Su and Chenming Hu.

The Award will be presented during the IEEE International Electron Devices Meeting to be held in December 2021. In addition to the Award certificate, the authors will receive a check for $2,500 to be shared equally among all authors. On behalf of the IEEE Electron Devices Society, I would like to congratulate the authors for this achievement.

Joachim Burghartz
EDS Vice-President of Publications and Products

Electron Devices Society Members Named Recipients Of 2021 IEEE Medals

Two EDS members were named 2021 IEEE Medal recipients. Please be sure to visit the IEEE website at https://corporate-awards.ieee.org/recipients/current-recipients/ to view all of the award recipients.

2021 IEEE James H. Mulligan, Jr. Education Medal

John D. Cressler, has been named as the recipient of the 2021 IEEE James H. Mulligan, Jr. Education Medal. The citation states, *"For inspirational teaching and mentoring of undergraduate and graduate students".*

A world-renowned researcher in nanoscale-engineered silicon-germanium (SiGe) electronics, John D. Cressler's vocation in life has been educating and mentoring young people, and he has excelled at that as one of Georgia Tech's most decorated professors. Silicon-germanium alloys are a lower-cost alternative to expensive compound semiconductor components but can still provide the performance necessary to enable the higher-frequency requirements of today's and the future's wireless and wired communications devices. As leader of one of the largest and most visible SiGe-focused research teams in the world, Cressler and his students at Georgia Tech have helped pioneer this emerging field that is providing the infrastructure to fuel the global communications revolution. During his tenure there, Cressler has introduced very popular courses. His "Introduction to the Microelectronics and Nanotechnology Revolution" is open to all majors/years, and he started the graduate-level "Silicon-based Heterostructure Devices and Circuits." Both courses utilize textbooks that Cressler wrote, and they

have been adopted at other universities. He also teaches his "Science, Engineering, and Religion: An Interfaith Dialogue" course within Georgia Tech's Ivan Allen Liberal Arts College. This course is open to undergraduate students of all years and majors. Mentoring students is Cressler's great passion, and he feels that his greatest accomplishments are measured by the success of his students. His graduate students have become leaders in the most prominent electronics companies of the world, including IBM, Intel, Texas Instruments, and National Semiconductor; many have received fellowships; and others have become professors and started their own businesses. He also has been asked on many occasions to share his thoughts on teaching, mentoring, and work-life balance with incoming Georgia Tech faculty, staff, and students.

An IEEE Fellow and recipient of the 2013 Georgia Tech Class of 1934 Distinguished Professor Award, Cressler is the Schlumberger Chair Professor in Electronics in the School of Electrical and Computer Engineering and the Ken Byers Teaching Fellow in Science and Religion at the Georgia Institute of Technology, Atlanta, Georgia, USA.

2021 IEEE Jun-Ichi Nishizawa Medal

James J. Coleman, has been named the recipient of the 2021 IEEE

Jun-Ichi Nishizawa Medal. The citation states, "*For contributions to the development of strained-layer semiconductor lasers*".

Ushering in a new era of laser design, James J. Coleman's work on strained-layer semiconductor lasers has enabled high-power lasers for all-optical telecommunications systems and technologies we take for granted today such as DVD players and laser pointers. Coleman recognized early the importance of strained layer lasers as efficient sources in the 980-nm pump band of erbium-doped fibers and was the first to systematically study and demonstrate reliable strained-layer semiconductor layers operating in the 900-1100-nm range using indium gallium arsenide quantum wells. His pioneering studies were the first to relate strain, performance, and reliability in this system and confirmed earlier predictions that threshold current densities are lower for these devices compared to unstrained lasers. These lasers are now widely used in fiber-optic telecommunications networks as pump sources for optical amplifiers. The simple, all-optical erbium-doped optical-fiber amplifier has replaced more complex, more costly, and less reliable optical-electrical-optical regeneration circuitry. Prior

to Coleman's work there had been theoretical predictions of the potential advantages of strained quantum-well lasers in the 980-nm band; however, his experimental work established their commercial viability, which was crucial for the acceptance of this technology. Today, virtually all semiconductor lasers routinely use strain-reduced valence band (hole) effective mass as a design variable. In his early career, Coleman contributed to the development of long wavelength telecommunication diode lasers grown by liquid phase epitaxy, and he was involved in early demonstrations of the effectiveness of metalorganic chemical vapor deposition (MOCVD) to make quantum well lasers, solar cells, and photodetectors with better performance characteristics. His more recent work includes high-performance lasers, integrated lasers, and other photonic devices produced through selective-area epitaxy and novel growth processes for quantum-dot lasers and other three-dimensional nanostructures. Other commercial products also utilize his laser designs for applications in displays and information storage and retrieval.

An IEEE Fellow and member of the U.S. National Academy of Engineering, Coleman is the Presidential Distinguished Professor of Photonics at the University of Texas at Arlington, Arlington, Texas, USA.

Fernando Guarin
EDS Awards Chair
Global Foundries

IEEE

ELECTRON DEVICES SOCIETY

CALL FOR NOMINATIONS
IEEE EDS William R. Cherry Award

The IEEE Electron Devices Society invites the submission of nominations for the 2022 William R. Cherry Award.

This Award is named in honor of William R. Cherry, a founder of the photovoltaic community. In the 1950's, he was instrumental in establishing solar cells as the ideal power source for space satellites and for recognizing, advocating, and nurturing the use of photovoltaic systems for terrestrial applications. The William R. Cherry Award was instituted in 1980, shortly after his death. The purpose of the Award is to recognize an individual engineer or scientist who devoted a part of their professional life to the advancement of the science and technology of photovoltaic energy conversion. The nominee must have made significant contributions to the science and/or technology of PV energy conversion, with dissemination by substantial publications and presentations. Professional society activities, promotional and/or organizational efforts and achievements are not considerations in the election for the Award.

The Award consists of a plaque, monetary award, recognition and a dedicated Cherry Award Talk during the Photovoltaic Specialists Conference.

Nominate:
William R. Cherry Award online nomination form:
https://ieeeforms.wufoo.com/forms/eds-william-r-cherry-award-nomination-form/

Submission Deadline:
15 January 2022

For more information:
https://ieee-pvsc.org/PVSC49/awards-cherry.php#

EDS Young Professionals

Pragya Kushwaha: Reflections of an EDS Young Professional

The Young Professional guest in this issue of the Newsletter is Pragya Kushwaha, Electron Devices Society's 2019 Early Career Award winner and a scientist at Space Application Centre (SAC), Ahmedabad, India, which is one of the centers of Indian Space Research Organization (ISRO). Her perceptions about EDS and views regarding professional development and career growth are reflected in the discussion. Here are the excerpts of the interview with Pragya Kushwaha made by Manoj Saxena, the Newsletter Associate Editor-in-Chief.

Manoj Saxena: My first question is what was the specific temptation, if any, which made you join EDS which is a part of the largest professional organization in the globe?

Pragya Kushwaha: Most of the universities/institutes have subscription of IEEE journals/conferences. However, students seldom realize this opportunity and the importance of IEEE membership. During my masters I came to know that I can access IEEE research papers even from my home. That was the tipping point which tempted me to take IEEE membership for the first time. Eventually I realized that being a researcher in the field of electron devices, it is the need of the hour to stay tuned with cutting edge technologies. IEEE EDS serves this purpose by facilitating an access for young professionals to a knowledge sharing platform.

MS: You won the prestigious EDS Early Career Award, an honor most of the young professionals aspire to. How do you consider this recognition and what are your plans to further develop your research career ?

PK: I am honored to have this prestigious award as it not only recognizes my work internationally but has also made me India's first woman scientist a recipient of this award. This award encourages me to carry out my future research work with more enthusiasm. Till date my contributions in the field of electron devices revolve around the characterization techniques and industry standard compact model development for a betterment of the state-of-the-art CMOS devices, i.e. FinFETs, FDSOI MOSFETs, NCFETs. We are witnessing an era where the semiconductor industry is facing radical changes due to the emergence of several new computing techniques such as quantum computing, neuromorphic computing and artificial intelligence. My vision is to make these emerging computing techniques compatible with the state-of-the art CMOS devices to facilitate more and more functionality from a single chip at low cost.

MS: As a Young Professional, how do you position your interest in your own field with the activities and services you perform as an EDS member/volunteer?

PK: IEEE EDS is an umbrella entity which runs numerous technical and non-technical activities under which it serves our society. The Society not only facilitates access to the research platform for sharing knowledge but also connects young professionals with their peer groups. I am fortunate enough to be a part of technical as well as non-technical activities running under the Society such as EDS Compact Modeling Committee, EDS Women in Engineering (WIE) and EDS Young Professionals (YP) Committee. The IEEE VLSI Symposia is one of the events where EDS YP are present every year. During my doctorate, I felt that these kinds of networking platforms provided me the opportunity to explore new areas of interest and to meet experts of my field. Having a specialization in the very-large-scale integrated circuits (VLSI) field, I was invited to organize the online mentoring event for VLSI Symposia 2020 where I invited my colleagues and senior experts from Academia/Industry to make this event successful. Many young researchers joined this event to get answers for their queries and to get guidance from experts. I will be happy to give my services to EDS technical/non-technical activities also in future.

MS: What are your thoughts about the EDS membership and its paybacks? Whether the EDS membership benefited you at any time in your career growth? If so, how?

PK: I have been an active member of IEEE EDS since 2016. Online subscription of EDS Newsletter and IEEE Spectrum keeps me aware of the latest technology and its R&D efforts worldwide. As an IEEE EDS member, I regularly receive information about upcoming IEEE events and conferences. These international conferences organized by the Society provide a platform where academia and industry representatives meet and share their visions on future technologies.

As a young professional, it has always been a great opportunity for me to attend EDS conferences (i.e. IEDM, S3S) where I got a chance to meet academia/industry partners. This is one of the reasons that my research is recognized as state-of-the-art work and the developed compact models are still appreciated by companies like Globalfoundries and Qualcomm. Today I am serving Society as a reviewer of many reputed EDS journals (i.e., IEEE TED, MTT and EDL) and the only woman member of EDS compact modeling technical committee which I believe are the paybacks for me.

MS: As an YP, how do you consider the ED Society as a whole and what are the changes or developments you would like to see in evolving this professional body as a group devoted to humanity and its causes?

PK: EDS as a professional body has a vision to nurture good quality research work worldwide for the betterment of humankind. EDS not only provides technical platforms to the young professionals but also recognizes professors/ industry experts for their contributions in the field of education and research. I feel this kind of recognition of hard work by the IEEE EDS will definitely motivate young engineers to contribute in the field of electron devices.

MS: What are your suggestions and recommendations for those young professionals who may aspire to join EDS?

PK: I still remember those happy student life moments when I benefited from IEEE EDS student member discounts while registering for IEEE conferences. These are schemes which show that EDS has a vision to motivate young engineers to attend conferences and to get benefited technically. During the COVID pandemic, IEEE continued its services by providing free access to many e-books and even conducted free online webinars for its members on state-of-the art topics which shows dedication of the Society towards technology development. EDS membership has helped me a lot in growing professionally in my career. I would strongly recommend young professionals to join this prestigious community for their bright future.

MS: As an EDS Young Professional and a young researcher in the field, how do you consider the prospects of scientific research in this field for the progress of Humanity as a whole?

PK: We are born in the era when technology changes every day. Researchers are trying their best to make human life simpler than before. I am thankful to EDS for providing a common platform to the academia as well industry to collaborate. I believe these kinds of efforts will definitely improve scientific research and serve humanity.

Biography

Pragya Kushwaha received her Ph.D. degree in microelectronics specialization from Indian Institute of Technology Kanpur in 2017. She completed her postdoctoral fellowship (2017-2020) in the University of California Berkeley, USA. Dr. Kushwaha is the first Indian woman scientist to receive IEEE EDS Early Career Award in 2019. Dr. Kushwaha has been selected for INSPIRE faculty fellowship 2019 and a prestigious Ramanujan fellowship 2020 by Department of Science and Technology, India. She joined Space Applications Centre (SAC) Ahmedabad, India, a center of ISRO, in July 2020 as SD scientist in the microelectronics group. Dr. Kushwaha has over 55 publications in international journals and conferences and two book chapters on her name. She is reviewer of many reputed EDS journals (i.e., IEEE TED, MTT and EDL). Dr. Kushwaha is the only woman member of EDS compact modeling technical committee since July 2020.

NEW!

EDS Podcasts Available to Everyone!

EDS is pleased to announce our new podcast series. Join us as we host interviews with some of the most successful members of our Society sharing their lives and careers. Their insight and wisdom will be invaluable inspiration and knowledge for those in the engineering field. Stay tuned to our social media channels and website for future announcements on upcoming events.

Women in Engineering

Elyse Rosenbaum—A Career in Academia—Impressions and Hints

My intended audience for this article is early-career engineers, especially those still engaged in university studies. I, too, spend much of my time on a university campus, but as a faculty member rather than a student. I am the Hasselbrock Professor in Electrical and Computer Engineering at the University of Illinois at Urbana-Champaign. Some of you may be considering a career in academia. This article will shed a bit of light on what it is that professors do when we are not lecturing in the classroom or reviewing our graduate students' research results. I will also provide focused advice for the woman readers.

I was asked to contribute a nontechnical article for the Women in EDS series. Why did I agree? Many readers may be unaware that professors are evaluated annually for their contributions in three spheres: teaching, research, and professional service. Those evaluations determine our next year's salary and eligibility for promotion in rank. My authorship of this article constitutes professional service, and that was one of my motivations for doing it. That brings me to my first piece of advice for young engineers: Look for service opportunities that fit your interests and are not overly burdensome (i.e., very time consuming). Do not reflexively say yes to all requests.

If you had asked me to make predictions about the year 2021 back when I was a student in electrical engineering, I would not have projected that the EDS Newsletter would contain a series of articles on Women in EDS. I could not have imagined that there would be anything noteworthy about women in our profession. Indeed sadly, the engineering workforce of 2021 doesn't have significantly higher female representation than that of 1991. Perhaps the young women reading this article will be the ones to finally achieve parity. There are no good reasons for you not to do so! Engineering competency and engineering brilliance are found in equal measures among male and female students. My perception is that historically, more young men entered the university with confidence in their hands-on technical skills, perhaps having developed them by participating in a robotics club or an Eagle Scout project. Today, we find that more and more young women participate in "tech" activities during their high school years. However, even if a student did not participate in youth engineering activities, it is not an impediment to successful completion of an engineering degree or to a long, productive career as an engineer.

Since the engineering workplace will be majority male for at least the next decade, how is a woman to cope with her minority status? You should strive to rapidly establish a reputation for excellence and reliability, so work hard starting day one. Advocate for yourself; ask to be assigned to high-excitement, high-visibility new projects. Choose your battles carefully for maximum impact; if you refrain from objecting every time a male coworker says something a bit offensive or you detect implicit bias, people will take notice when you do call out an inequity or an inappropriate statement. In the words of the late, great U.S. Supreme Court Justice Ruth Bader Ginsburg, "It helps sometimes to be a little deaf in every workplace." Observe which of your co-workers are competitive and which ones have your best interests at heart. Treat the latter as your informal mentors; go to them for career advice—it doesn't matter if they are male or female. And now I want to address the men specifically: please make an effort not to be jerks! Don't comment on your female coworkers' appearance; don't make assumptions about what kinds of skills they have; don't exclude them from lunchtime and after-work socializing, since that is how a lot of professional relationships are built.

Those of us in academia may not have work-life balance—many of us are workaholics—but it is an ideal profession for people who also want to be parents. Professors work many hours per week, but those hours are flexible. You can arrange your schedule so that you are free to pick up the children from daycare or school each afternoon or you are home in time to prepare dinner each night; also, you can work from home if a child is ill. University communities are great places to raise children. Most universities offer educational and cultural programs that are open to persons in the community, and the local schools tend to be very good. Academia is a highly suitable career for parents, moms and dads alike, but I recognize that historically, childcare has been the mother's special responsibility.

How did I succeed as a female professor? First, I devoted a lot of time to planning and practicing my external presentations, especially in the early part of my career. Conference talks

are the primary way one becomes known in the EDS community, and being known translates to getting approached for research collaboration and research funding opportunities. As a graduate student, I received the Roger A. Haken Best Student Paper Award for the 1991 IEDM, in part because my presentation was clear and engaging. As a professor, I received an Industry Pioneer Recognition Award from the EOS/ESD Association, in recognition of my research group's sustained contributions to the field. Researchers within the ESD discipline were aware of those contributions as a result of the carefully constructed and well-practiced presentations my students and I have given at the annual EOS/ESD Symposium.

Second, as a nontenured assistant professor, I proposed research projects that would leverage my academic training and that I could easily argue I was well qualified to lead. Only after becoming better known—and receiving tenure—did I step further outside my comfort zone. At that point, I had established that I was highly capable of leading research projects and I knew that proposal reviewers would be less skeptical of me than of a junior professor. Today, I lead a research center that focuses on machine learning, which is a far cry from my doctoral research on gate oxide reliability!

In closing, I want to mention that my favorite research projects still are those that focus on reliability of individual semiconductor devices. I am an EDS girl at heart.

Elyse Rosenbaum is the Melvin and Anne Louise Hassebrock Professor in Electrical and Computer Engineering at the University of Illinois at Urbana-Champaign. She received the Ph.D. degree in electrical engineering from University of California, Berkeley. She is the director of the NSF-supported Center for Advanced Electronics through Machine Learning (CAEML), a joint project of the University of Illinois, Georgia Tech and North Carolina State University. Her current research interests include machine-learning aided behavioral modeling of microelectronic components and systems, compact models, circuit reliability simulation, component and system-level ESD reliability, and ESD-robust high-speed I/O circuit design. Dr. Rosenbaum has authored or co-authored about 200 technical papers; she has been an editor for IEEE Transactions on Device and Materials Reliability and IEEE Transactions on Electron Devices. She was the recipient of a Best Student Paper Award from the IEDM, Outstanding and Best Paper Awards from the EOS/ESD Symposium, a Technical Excellence Award from the SRC, an NSF CAREER award, an IBM Faculty Award, and the ESD Association's Industry Pioneer Recognition Award. She is a Fellow of the IEEE.

Deblina Sarkar—Research Journey

As a child, my interest in science grew as I saw my father working on small projects at home which are of great practical use in our daily lives. He had developed for example a washing machine that can be operated without electricity, a system of pulleys for lifting heavy loads easily, amongst many others. These sparked my interest in science and engineering early on which grew stronger as I began to read books specifically on physics. Looking at a concept which might seem unfathomable at first glance but when we think more about it, unfolds beautifully, gives me the greatest joy in pursuing science. Then the ability to employ these concepts to build something unique and impactful is my inspiration behind pursuing engineering. I received my BSc Tech. from Indian institute of Technology, Dhanbad in electronics engineering. I had started research early on during my first year as an undergraduate student. At that time my research was fully theoretical in nature due to lack of access to any experimental facilities. I was fascinated by the field of nanoelectronics and started reading papers related to that, and thinking what kind of devices I could make which could overcome the existing challenges. I developed a physics based model for a double gate transistor to estimate the leakage currents with technology scaling. I also proposed a novel gating scheme for power reduction in semiconductor devices. Furthermore, I explored novel spin based devices to achieve energy efficiency. Based on my undergraduate work, I had one journal and 5 conference publications.

After my bachelors I joined University of California, Santa Barbara as an MSc/PhD student. During my doctoral research, I invented the world's thinnest channel (6 atoms thick) quantum mechanical transistor involving band-to-band-tunneling, which overcomes the fundamental thermal limitations in subthreshold swing and leads to record energy reduction by more than 75% [D. Sarkar et.al., *Nature*, 526(7571), 91–95, (2015)] [*Nature* (News and Views) 526, 51–52 (2015)]. This atomically thin and layered semiconducting-channel tunnel FET (ATLAS-TFET), is

based on the idea, that I conceived, of a unique tunneling heterojunction combining the best attributes of 3D (matured doping technology) and 2D (excellent electrostatics and ultra-low tunneling barrier) materials to achieve extremely efficient and controllable electron wave propagation through the energy barrier. This device is the first tunneling-transistor, in any architecture and any material platform, to achieve ITRS prescription of sub-thermal subthreshold swing over four decades of current at an ultra-low power-supply voltage of 0.1 V (thus, allowing voltage scalability). Moreover, the atomically-thin 2D channel provides near-ideal device electrostatics, which allows dimensional scalability beyond Silicon scaling era (sub 5 nm). Thus, this device has potential to crack the long-standing issue of simultaneous dimensional and power-supply voltage scalability.

Apart from experimental work, I also developed physics based analytical models for transistors as well as built a quantum-mechanical numerical simulator based on Non-Equilibrium Green's Function Formalism for designing and optimizing nanodevices [D. Sarkar et.al., *Appl. Phys. Lett.*, 100, 143108 (2012)]. Moreover, I developed the first detailed impedance model for graphene, which provides insights into the physics of on-chip 2D interconnects and inductors and revealed for the first-time anomalous skin effect in graphene [D. Sarkar et.al., *IEEE Trans. Elec. Dev.*, 58, 843–852 (2011)] [D. Sarkar et.al., *IEEE Trans. Elec. Dev.*, 58, 853-859 (2011)] [D. Sarkar et.al., *IEEE Intl. Interconnect Tech. Conf.* (2010)]. This model is critical for building of "all 2D" integrated circuits, which can lead to flexible/conformable computers and prosthetic devices.

My research also showed for the first time, that employment of quantum mechanical transistors and atomically-thin flexible 2D-materials can lead to electrical biosensors with extremely high sensitivity and potential for single-molecular detectability, in addition to they being extremely small and low-power, which can revolutionize wearable/implantable medical devices as well as point-of-care applications [*Nature Nano.* Research Highlights 2012] [*Appl. Phys. Lett.* 2012] [*ACS Nano* 2014] [*Nano Lett.* 2014].

I received the EDS PhD Student Fellowship Award in 2011. My PhD dissertation was honored as one of the top three dissertations throughout USA and Canada in the field of Mathematics, Physical Sciences and all departments of Engineering by the Council of Graduate Schools, and at the end of my PhD, I got job offer from Intel corporation and invitations to apply for faculty positions from Caltech, Princeton University, University of Pennsylvania and University of Southern California. However, while developing energy-efficient electronic devices during my PhD, I became passionately curious about understanding the brain, which can be thought of as an ultimate example of a low-power computational system. Driven by my curiosity, passion and adventurous nature allowing me to enjoy academic risks as well as the belief that truly disruptive technologies emerge by fusing dissimilar scientific realms, I decided to completely diversify my research field and transitioned to neuroscience in order to develop technologies for better understanding the brain.

As a postdoctoral researcher, I leveraged my extensive background in physics, engineering and biosensors, and helped in the design of an optical probe, for multiplexed recording of neural activity [S. G. Rodriques et. al., *Jnl. Biomed. Optics* 2016]. I have also shown that while highly dense and intricate 3D nanoarchitectures enable critical biological functions, such nanostructures may remain invisible to super-resolution imaging due to the inaccessibility of recognition labels. To overcome this challenge, I developed a technology called expansion revealing (ExR) [D. Sarkar et.al., bioRxiv, 2020; doi:10.1101/2020.08.29.273540] which decrowds the complex biomolecular environment. I demonstrated that ExR enables the discovery of fundamentally new nanostructures within biological specimens. As examples of capabilities of this technology, I revealed for the first time, a nanoscale trans-synaptic alignment in brain tissue and discovered intriguing nanodomains of amyloid-β arranged in periodic patterns associated with Alzheimer's disease. I shared this technology with researchers around the globe even before publication, who are currently employing it to answer fundamental questions in neuroscience and to understand neurological disorders.

Recently, I joined Massachusetts Institute of Technology as an assistant professor and started my own lab. I named my lab the Nano-Cybernetic Biotrek (NCB). Breaking down our group name, Nano: as we are working with nanoscale devices and materials, Cybernetic: as it means use of technology to control systems and in our case it could mean use of technology to develop novel nanoelectronics devices or to control biological systems, Bio: stands for biology, trek: signifies adventure and research to us is an adventurous scientific journey. In our lab we are merging engineering, applied physics, and biology with two main research directions: a) to build novel technologies for energy efficient computers, and b) to fuse such nanoscale devices with living-matter to create new nanoelectronics-bio hybrids that can create unprecedented opportunities for probing and modulating our biological system for therapeutics.

There are multiple open positions in my group in fields related to nanoelectronics, electromagnetism, antenna design, and brain recording. Overall, I am open to students from any academic field who are passionate and are willing to learn. I specifically encourage women and students from minority communities to apply.

Deblina Sarkar is an assistant professor at MIT and AT&T Career Development Chair Professor at MIT Media Lab. She heads the Nano-Cybernetic Biotrek research group. Her group carries out trans-disciplinary research fusing engineering, applied physics, and biology, aiming to bridge the gap between nanotechnology and synthetic biology to develop disruptive technologies for nanoelectronic devices and create new paradigms for life-machine symbiosis. Her inventions include, among others, a 6-atom thick channel quantum-mechanical transistor overcoming fundamental power limitations, an ultra-sensitive label-free biosensor and technology for nanoscale deciphering of biological building blocks of the brain. Her PhD dissertation was honored as one of the top 3 dissertations throughout USA and Canada in the field of Mathematics, Physical sciences and all departments of Engineering. She is the recipient of numerous other awards and recognitions, including the Lancaster Award, Technology Review's one of the Top 10 Innovators Under 35 from India, NIH K99/R00 Pathway to Independence Award.

Chapter News

Opportunity to Grow Your Chapter Membership

Applications Now Being Accepted for the EDS Membership Fee Subsidy Program

***UPDATE**—Program Expanded for all EDS Chapters in 2022!*

Our society continually works to increase the value of EDS membership and our colleagues enjoy an incredible array of members-only benefits. One EDS initiative to encourage newcomers and assist EDS chapters to stay strong and vibrant is the EDS Membership Fee Subsidy Program (MFSP). EDS MFSP offers the generous incentive of one-year complimentary IEEE and EDS memberships (sponsored by EDS), to help launch new chapters or assist existing chapters in low-income geographical areas to grow their memberships.

This special offer is available to students currently enrolled in an accredited course of study, and to engineering professionals who would normally qualify for reduced IEEE membership fees (i.e., unemployed, retired, or meet a minimum income threshold).

Please review the EDS Membership Fee Subsidy Program policy carefully:

- EDS will cover the cost of IEEE and EDS membership for up to **15** applicants per chapter. Please note that this is a one-time benefit, per applicant. Past recipients of the EDS membership fee subsidy benefit cannot apply again.
- **Five** of the fifteen applicants must be first-time IEEE members.

EDS has Chapters around the world that organize events to benefit your professional development

- Applicants must contact their local EDS chapter to apply. To find an EDS chapter near you: https://eds.ieee.org/chapters/global-chapters-list
- Each professional applicant must indicate their income situation in their IEEE account prior to applying for EDS Membership Fee Subsidies to show eligibility for the IEEE membership fee special circumstances discount. NOTE: This requirement does not apply to Student applicants.
- For a complete list of special circumstances eligible for reduced IEEE membership fees: https://www.ieee.org/membership/special-circumstances.html.
- Professional applicants will be enrolled in IEEE Electronic Membership. For details on this IEEE membership option: https://www.ieee.org/membership/join/emember-countries.html

If you wish to apply for EDS Membership Fee Subsidy but are not eligible because of receiving this benefit in the past, we encourage you to try the IEEE Electronic Membership option. IEEE Electronic Membership is open to new and renewing members who reside in countries where the per capita Gross National Income (GNI) is US$15,000 or less. Please visit the IEEE website for more details on this membership option: https://www.ieee.org/membership/join/emember-countries.html

EDS Chapter Chairs: Please contact Joyce Lombardini (j.lombardini@ieee.org) in the EDS Executive Office, to receive enrollment instructions.

ED NIT Silchar Student Branch Chapter organizes COVID-19 Awareness Program

By T. R. Lenka

On 19 April 2021 the NIT Silchar ED Student Branch Chapter organized a COVID-19 Awareness Program for the rural and semi-urban citizens of the city of Silchar. The disease symptoms and various precautionary measures were explained by the student volunteers through presentations and demonstrations of the correct use of face masks, keeping a correct distance of minimum 2 yards between two or more persons in a gathering etc. The informative part of the program was followed by distribution of face masks and sanitizers to the participants as well as to the local people. It is worthwhile to mention that the program organized by the Chapter was in line with many undertakings arranged by governmental, professional and local organizations in India to stem the tide of the pandemic spreading and secure the people's living conditions in this crisis situation.

~ Soumya Pandit, Editor

IEEE EDS Malaysia Humanitarian COVID19 students' necessity parcel support for engineering students

On behalf of IEEE EDS Malaysia, Dr. Nurul Ezaila Alias from Universiti Teknologi Malaysia (UTM) Johor Bahru organized a humanitarian program to provide stationery parcels for students from School of Electrical Engineering during the lockdown period under Enhanced Movement Control Order (EMCO) in UTM.

During the EMCO period from 21 May 2021 until 3 June 2021, students and resident staff were not allowed to

EDS members volunteering during the COVID-19 pandemic

leave the campus thus making it difficult for them to obtain essential supplies and food due to a closure of the on campus cafeterias and shops. Concerning the students' needs and welfare, a donation drive was conducted amongst EDS members to hand out stationeries for students who were staying for their examinations. In total, 270 parcels containing A4 papers and pens were channeled through the office of the UTM Alumni to students from School of Electrical Engineering. During this challenging time, IEEE EDS Malaysia Chapter appreciates the generosity and commitment of the ExCom members towards the welfare of the engineering student community.

EDS Malaysia Chapter Received COVID-19 Response Project Grant from IEEE HAC/SIGHT

A project entitled 'Bridging Digital Inequalities Amongst the Urban Poor Communities in Malaysia' received US $5,000.00 funding from IEEE HAC/SIGHT. This is part of IEEE's effort in mobilizing member grassroots' humanitarian technology for sustainable development projects that addresses local challenges of the COVID-19 situation in the members' communities. The team was led by Dr. Maizatul Zolkapli. He with two other members Assoc. Prof. Dr. Ahmad Sabirin Zoolfakar and Dr. Aliza 'Aini Md Ralib aim to equip selected urban poor category families from Sekolah Menengah Kebangsaan Seksyen 18, Shah Alam with a device and digital application literacy to ensure that these students can participate in online learning in preparation for Malaysian Certificate of Education examination in March 2022. During this 6 month project, the students and their parents will be guided and trained to use the devices and related applications. Training modules, step-by-step manuals and handouts will be developed by the team to assist the students in their digital learning experience. The team hopes that this initiative will help to bridge a digital gap between privileged and disadvantaged communities.

Did You Know?

IEEE and EDS provide temporary Open Access to top papers from the IEEE Electron Device Letters (*EDL*) and the *IEEE Journal on Microelectromechanial Systems* (*J-MEMS*).

Every month, EDL Editors select a small number of particularly remarkable articles as **Editors' Picks**. These are highlighted on the issue cover and enjoy temporary (one month) Open Access. One of these articles is further selected as Cover Article and prominently featured in its main cover graphics. Visit the EDS website for links to the current EDL Editors' Picks.

Stay up to date with the latest developments in the MEMS areas with **IEEE RightNow Access for J-MEMS**. Enjoy temporary Open Access (3 months) to select featured papers from the latest J-MEMS edition. New selections are available quarterly.

Join us on social media to receive release announcements.

Regional News

North America (Regions 1–7)

1st EDS R9 ASIC Design Contest

—by Edmundo Gutiérrez

In March 2020 EDS launched the Call for the first R9 EDS/IEEE Student ASIC Design Fabrication contest. A total of 13 applications from 6 different countries were received: Brazil, Mexico, Chile, Colombia, Ecuador, and Uruguay. Out of those 13 applications, 9 were finally selected and passed the design rule checks (DRC). They were fabricated in a TSMC 0.18 µm CMOS technology through the Europractice program. All 9 designs were contained in a 2.5 × 2.5 mm^2 MPW chip. According to the schedule of the program a shipment and delivery of the fabricated chips was planned to be completed by mid-September 2021. We expect the final tests to be ready by January 2022. The 9 designs under consideration are listed below:

1) "Conditioning system and digital biomedical signal processor," by INAOE, Mexico,
2) "Receiver for Internet of Medical Things (IoMT) and ADC converters," by UNAM, Mexico,
3) "Low power circuits for biomedical applications," by FEI, Brazil,
4) "Delay-based temperature sensor for IoT applications," by USFQ, Ecuador,
5) "Project FEI2020: a device test structures for modeling purposes," by FEI, Brazil,
6) "Low power analog and mixed-signal blocks for IoT interfaces," by UFRGS, Brazil,
7) "ELAPSE Electronics for particle physics experiments," by PUC, Chile,
8) "CLaN- A current limiter circuit with GaN power switch for payloads protection," by UNICAMP, Brazil, and
9) "Passive UHF RFID tag for vital signs measurements using UWB communication," by UnB, Brazil.

The second issue of the ASIC Design Contest was approved and launched in August 2021.

ED South Brazil Chapter

—by Paula Agopian

The XV Workshop on Semiconductors and Micro & Nano Technology (SEMINATEC 2021) was held virtually on 13–14 May 2021. It was organized by Sao Paulo State University (UNESP), University of Sao Paulo (USP) and EDS South Brazil Chapter, and co-organized by Integrated Systems Laboratory at the University of São Paulo, EDS Student Branch of Campinas, EDS Student Chapter of FEI and IEEE Solid-State Circuits Society.

The SEMINATEC is focused on technology trends in the areas of micro and nanotechnology promoting the interaction among industry, academy, research & development centers, government and students. More than 120 participants, including EDS members, attended SEMINATEC 2021.

SEMINATEC's program included 10 invited speakers (5 Distinguished Lectures—DLs of EDS and one DL from IEEE SSCS), and 28 regular papers.

1) "Evolution of semiconductor devices from its conception to our present." by Prof. Adelmo Ortiz Conde, Universidad Simon Bolivar, Venezuela, (DL invited by EDS South Brazil Chapter/USP);
2) "Unifying the Modeling of Charge Trapping in RTN, 1/f Noise and BTI." by Prof. Gilson Wirth, UFRGS, Brazil (DL invited by EDS South Brazil Chapter/USP);
3) "Compact modeling of organic and amorphous oxide TFTs from 150 to 350 K" by Prof. Benjamin Iniguez, Universitat Rovira i Virgili, Spain (DL invited by EDS Student Branch of FEI);
4) "Impact of Using Non-standard Layout Styles for MOSFETs"

SEMINATEC 2021 Distinguished Lecturers, Invited talks and organization (Paula Agopian—General Chair and Joao Martino—Program Chair)

by Prof. Salvador Pinillos Gimenez, FEI, Brazil (Invited talk);

5) "Analog IC design in scaled CMOS technology" by Prof. Hugo Daniel Hernandez Herrera, UFMG, Brazil (Invited talk);
6) "High Resolution Radar Imaging for Breast Cancer Detection: Trends and Challenges" by Prof. Andrea Bevilacqua, University of Padova, Italy (DL invited by SSCS/USP);
7) "Thermoresistive Sensors, Applications and Electrical Equivalence Principle." by Prof. Sebastian Yuri Cavalcanti Catunda, UFRN, Brazil (Invited talk);
8) "Chemical Sensors for Detection of Hydrogen and Acetylene" by Prof. Sebastião Gomes dos Santos Filho, USP, Brazil (Invited talk);
9) "Adaptable Electronics" by Prof. Muhammad Mustafa Hussain, University of California, Berkeley, USA (DL invited by EDS Student Branch of Campinas/UNICAMP);
10) "MOSFET evolution: From planar to gate all around devices and Bio-FET" by Prof. João Martino, USP, Brazil (DL invited by EDS South Brazil Chapter/USP).

Additional information about the Workshop is available at http://www.psi.poli.usp.br/seminatec2021.

ED South Brazil Chapter—Webinar 2020

—by Joao Martino, Chapter Chair

The Electron Device Society of South Brazil Chapter organized the 2020 IEEE EDS South Brazil Chapter Webinar on Micro & Nanodevices (EDS/South Brazil Webinar 2020) held virtually on 13–29 October 2020.

The ED South Brazil Webinar 2020 program included 4 invited talks (3 Distinguished Lectures—DLs of IEEE EDS) as shown below:

ED South Brazil Webinar 2020

1) "Electron Devices Evolution: Past-Present-Future" by Prof. Dr. Cor Claeys, KULeuven, Belgium, Fellow and DL of IEEE EDS, that was on 13 October 2020;
2) "Dielectric Science on Today´s Devices" by Prof. Durga Misra, New Jersey Institute of Technology (NJIT), USA, Fellow and DL of IEEE EDS, that was on 15 October 2020;
3) "Electrical Characterization: From Micro to Nano Era" by Prof. Adelmo Ortiz-Conde, Universidad Simón Bolívar, Venezuela, DL of IEEE EDS, that was on 22 October 2020;
4) "Advanced Transistors for High Frequency Applications" by Dr. Bertrand Parvais, Imec, Belgium, that was on 29 October 2020.

All lectures were presented (and 3 of them are still available) on the Youtube channel. For those interested in a link to the channel is given: https://youtube.com/channel/UCejDJawSk2kKOveZ6bwzFlg.

We had about 250 attendees on average among 4 talks, including many EDS members from around the world.

~Paula Agopian, Editor

Mexican Humanitarian Technology Conference (MHTC 2021)

—by Roberto S. Murphy

On 21–22 April 2021, the third edition of the Mexican Humanitarian Technology Conference (MHTC 2021) was held, virtually but based in the city of Puebla, Mexico. The objective of the conference is to highlight the technological developments proposed by students and professionals of the region which have a direct application to the well-being of humans. As such, diverse topics spanning healthcare, education, potable water procurement, 5G, the Internet of Things, and green energies generation and use were presented in 13 papers written by a total of 57 authors from Brazil, Ecuador, El Salvador, Guatemala, Mexico, Spain, Sweden and the United States of America. Besides the presentation of these papers, we had five keynote speeches. The first one was by Mario Aleman, from Nicaragua, who spoke of ways of empowering

Latin American countries by instituting better practices and more financial opportunities to make a better world. Jenifer Castillo talked about the relief efforts headed by IEEE, through the Brillo project, after a hurricane Maria hit Puerto Rico. Pritpal Singh, from the US, outlined his activities aimed at preparing students and young professionals to participate in humanitarian technology projects. Eros Pasero, from Italy, detailed the actions being taken worldwide to incorporate new technologies and artificial intelligence in medicine, what is now termed the Fourth Industrial Revolution. On a similar basis, Ricardo Anaya of Mexico, spoke about the 5G network and the future of healthcare.

The conference was organized, as the previous editions, by the Puebla Section of IEEE, with the participation of the most important universities of the city and the only public research center based on the state, the INAOE. All the IEEE Chapters and affinity groups registered in the Puebla Section participated as well, resulting in many people volunteering their time and knowledge to make MHTC 2021 a very successful conference, even online, having an average participation of 110 attendees.

~ Joel Molina, Editor

Europe, Middle East & Africa (Region 8)

ED/AP/MTT/COM/EMC Tomsk Joint Chapter

Siberian Conference on Control and Communications SIBCON

—by Oleg Stukach

The 15th Siberian Conference on Control and Communications (SIBCON) co-sponsored by IEEE Electron Devices Society and organized by Tomsk Joint Chapter took place in Kazan, Russia, on 13–15 May 2021.

During a regular session of the 2021 SIBCON conference

This in-person biannual meeting was held between the second and third waves of the COVID-19 pandemic. The technical program consisted of keynote speeches, contributed paper presentations in oral sessions, and a selected session for participants who could not visit Kazan. In this case, SIBCON confirmed its role as a platform for personal contact and direct information exchange.

Various problems related to sensors, electron devices, communication, and control theory, with emphasis on both theory and applications, were considered. The major goal of the conference was to bring together researchers to present accomplishments in Communications, Control Theory and Technology. The conference demonstrated a continuing interest in analysis and control methods for the considered problems. We were honored to have many distinguished speakers who gave their talks on relevant and important topics in the areas covered by SIBCON. Thus, Professor Max Talanov from Kazan Federal University delivered a talk "Neurotechnologies to Manage a Robotic System" where the AI and brain-computer interface technologies overview in the context of integration with robotic and biological systems was discussed. Also, Yuri Choni in his talk "Stabilizing the Beams of a Large-Sized Satellite Antenna within the Frame of an Engineering Approach to Antenna Synthesis" presented an engineering approach to antenna synthesis and its role in the antennas theory and practice. The conference proceedings were published in the IEEE Xplore. We thank all authors who submitted and presented papers at the conference.

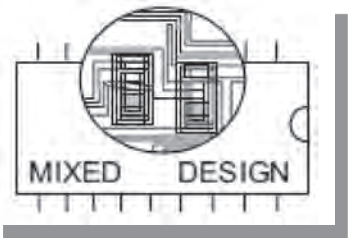
Modern but forevermore ancient Kazan witnessed many exciting events in Russian history and still plays a very important role in its scientific and cultural life. The weather was perfect, and the sightseeing tour provided an excellent opportunity to enjoy the historical sites, as well as the beauties of the city. It was a special time for attendees to relax during the conference, to enjoy refreshments, and to make plans for future joint investigations.

We are very pleased that SIBCON has yet again confirmed the status of the flagship and well-known event. My sincere congratulations must go to the Kazan Federal University and personally to Prof. Evgeni Magid who had done an excellent job of organizing such a successful event. We hope you might consider participating at the next SIBCON, please join us in Tomsk.

~Kateryna Arkhypova, Editor

28th International Conference "Mixed Design of Integrated Circuits and Systems" — MIXDES 2021

—by Mariusz Orlikowski



The 28th MIXDES conference took place on 24–26 June 2021. Due to the COVID-19 pandemic, for the second time the event was organized fully on-line jointly by the Lodz University of Technology and the Warsaw

University of Technology, Poland. The conference was co-sponsored by Poland Section IEEE ED & CAS Societies, Polish Academy of Sciences (Section of Microelectronics and Electron Technology), and Commission of Electronics and Photonics of Polish National Committee of International Union of Radio Science—URSI.

The conference program included 60 presentations given by authors affiliated in 21 countries. The following three general invited talks were presented during the conference plenary sessions:

- *ASCENT+ European Infrastructure for Nanoelectronics: a Deep Dive to All-GaN IC Technology for Power Electronics* Urmimala Chatterjee (IMEC, Belgium) and Giorgos Fagas (University College Cork, Ireland)
- *Modeling and Simulation of Charge Trapping in 1/f Noise, RTN and BTI: from Devices to Circuits* Gilson I. Wirth (UFRGS, Brazil)
- *Modeling Passive Devices for CMOS RF Circuits* José Valdés, Reydezel Torres and Roberto S. Murphy Arteaga (INAOE, Mexico)

Except for regular sessions, two special sessions were held:

- *Compact Modeling for Semiconductor Device, Sensor and IC Design* organised by Dr. Daniel Tomaszewski (Łukasiewicz-IMiF, Poland) and Dr. Władysław Grabiński (GMC, Switzerland)
- *Fusion Diagnostics I&C Workshop* organised by Dr. Stefan Simrock (ITER, France), Dr. Axel Winter (Max Planck Institut für Plasmaphysik, Germany) and Dr. Dariusz Makowski (Lodz University of Technology, Poland)

During the plenary session the participants of MIXDES conference commemorated two members of the Programme Committee who had passed away recently: Prof. Ninoslav Stojadinović and Prof. Andrzej Jakubowski. A special editorial in memory of Prof. Stojadinović was already included in the April 2021 EDS Newsletter issue. The passing away of Prof. Jakubowski on 9 March 2021 after a long illness was a great loss for the microelectronics community in Poland. He was a visionary highly respected in Europe among the researchers and engineers working in the field of electron device modeling and characterization. Prof. Jakubowski contributed significantly to the development of electronic devices and integrated circuit technology. For over 50 years of his scientific activity he served as a teacher and a mentor for many generations of Polish electronic engineers. More information about his life and career is available at https://sedemos.blogspot.com/2021/03/rip-prof-dr-hab-inz-andrzej-jakubowski.html.

The next MIXDES conference hopefully will take place in 2022, as it was originally planned, in Wrocław, Poland. The preliminary Call for Papers is available at http://www.mixdes.org/downloads/call2022.pdf. More information about the past and next MIXDES conferences can be found at http://www.mixdes.org.

~ Marcin Janicki, Editor

Mina Rais-Zadeh DL on Miniaturized Sensors for Space Applications

—by Mike Schwarz

The distinguished lecture on "Miniaturized Sensors for Space Applications" was held 12 April 2021. It was organized by the EDS Germany Chapter and co-sponsored by the NanoP from THM—University of Applied Sciences. The DL was attended by 14 IEEE participants and 22 non IEEE members.

The distinguished lecture of Dr. Rais-Zadeh from NASA JPL, California Institute of Technology, USA, started with an overview in various domains which are under investigation by JPL. The talk was focused on advanced sensors and micromechanical systems.

The content of the DL had a scope on upcoming NASA missions to Venus and Mercury with their harsh environments, i.e. temperature, radiation, low or high pressures and atmosphere with its gaseous environment. Dr. Rais-Zadeh set the focus on high costs, a short mission time and many other challenges occurring during the mission development. The requirements of the sensors are huge to avoid a mission failure. Dr. Rais-Zadeh offered various hot planet mission concepts, especially for Venus, and emphasized requirements for a successful mission.

After the introduction and scope Dr. Rais-Zadeh went forward and presented GaN for MEMS Applications. An overview of the properties of the second most popular semiconductor was given, including high mobility, strong piezoelectric properties enabling sensors and actuators, high power handling capability, and many

Dr. Mina Rais-Zadeh during the presentation of the hot planet mission concepts

more. Focus on GaN for sensing applications in space was followed by a discussion of devices with 2DEG made of GaN with its extremely stable temperature properties. Furthermore, GaN electromechanical properties were presented in comparison to other semiconductors.

Various applications as ovenized MEMS oscillators with a bench of examples and results followed. Afterwards, Dr. Rais-Zadeh switched the focus on GaN for sensing applications. Here, the focus was set on IR applications for the Venus mission and on the realization of piezo/pyroelectric resonant devices based on GaN. An example of a hot IR detector for Venus was presented as well, with its constraints on design of the device and the absorber. The last topic was related to diffraction gratings for planetary imaging spectrometers including visual and infrared mapping.

Mario Lanza DL on Hexagonal Boron Nitride Based Electronic Devices and Circuits: Status and Prospects

—by Mike Schwarz

The distinguished lecture on "Hexagonal boron nitride based electronic devices and circuits: status and prospects" was held on 20 May 2021. It was organized by the EDS Germany Chapter and co-sponsored by the NanoP from THM—University of Applied Sciences. The DL was attended by 14 IEEE participants, as well as other non-IEEE members.

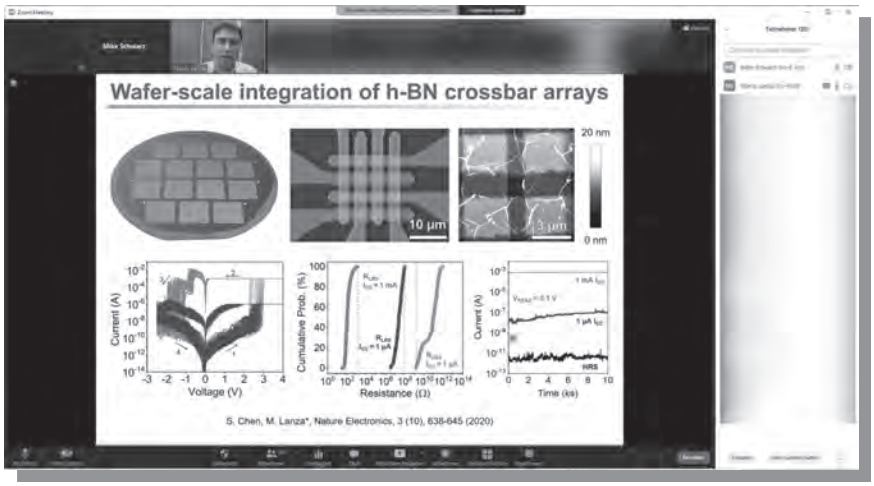
The distinguished lecture of Prof. Lanza from KAUST, Saudi Arabia gave an outstanding overview of the status and prospects of hexagonal boron nitride (h-BN) based electronics devices and circuits. The main conclusion of Prof. Lanza's talk is that, while hexagonal boron nitride grown by scalable methods still contains too many defects that hinder its application as reliable gate dielectric in transistors, it exhibits superior resistive switching properties that allows employing it to fabricate reliable memristors for multiple applications, including electronic synapses and neurons for neural networks and/or artificial intelligence.

The DL started with discussing fabrication of 2D material based circuits, where the challenges are that often circuits and devices suffer from the process's huge variability. Prof. Lanza went through materials and methods, e.g. synthesis methods, and methods for transferring 2D material. Here, exfoliation vs. CVD growth was discussed with their advantages and challenges. Key points as degradation and breakdown of thin dielectrics in a context of memristors were highlighted. Morphology and local electrical properties influence essentially the memristor behavior. As a solution Prof. Lanza proposed 2D material based memristors, where 2D materials offer better control, because fewer atoms are involved in the "filament" generation. Further properties as high thermal conductivity, higher chemical stability and simple fabrication and high integration were highlighted.

The DL went through electrical properties as bipolar and threshold resistive switching, which allows for synapse and neuron emulation by one device in an electronic circuit. It is obvious that this allows for a higher integration with less effort compared to other solutions.

Prof. Lanza showed initial solution of memristive synapses and neurons, showed wafer-scale integration of h-BN crossbar arrays, yield of Au/h-BN/Au synapses and their variability. Furthermore, results for artificial neuronal networks with h-BN memristors in terms of emulated/simulated multilayer perceptron networks were demonstrated. A 98% yield of the hardware realization was achieved.

~Mike Schwarz, Editor



Prof. Mario Lanza showing examples of wafer-scale integration of h-BN crossbar arrays

Asia & Pacific (Region 10)

ED/SSC Hong Kong Chapter—IEEE EDS Invited Lectures

—by Qiming Shao

On 24 May 2021, the IEEE Hong Kong Joint Chapter of Electron Devices and Solid-State Circuits (ED/SSC) organized a hybrid-mode seminar given by Prof. Lain-Jong (Lance) Li, Chair Professor of Department of Mechanical Engineering at The University of Hong Kong. The title of his talk was "Materials Innovation for Future Electronics." On May 28, HK ED/SSC Joint Chapter organized another online seminar given by Prof. Yufei Ding, Assistant Professor of Computer Science and Electrical & Computer Engineering at University of California, Santa Barbara. Her

seminar was titled "Quantum Computing Engineering: Challenges and Opportunities." These two events were co-organized by HKUST-Academy for Continuing Education (ACE). They are briefly reported below.

Beyond CMOS is a booming direction in the EDS community. Two major directions are two-dimensional devices and quantum devices. Prof. Li discussed in his talk two possible approaches for advancing IC fabrication for future electronics: (1) Continue the transistor scaling (Moore's Law). With the scaling for future technology nodes, the transistor body thickness needs to be reduced to ensure efficient electrostatic control. Professor Li presented his recent works on thin materials with perfect surfaces such as transition metal dichalcogenide (TMD) monolayers. (2) Construct 3D integrated circuits with a monolithic approach. Few examples included adding sensor functionalities, constructing upper-layer logic circuits or memory devices on CMOS Si wafers, and stacking logic with memory devices. Professor Li presented his works on adding carbon nanotube transistors on TSMC 28 nm CMOS technology wafers to save the footprint and power consumption.

The second quantum revolution, the transition from quantum theory to quantum engineering, leads us towards practical quantum computing. Professor Ding reviewed in her talk the challenges and research opportunities in the state-of-the-art technological hierarchy of quantum computing, including quantum computing devices, peripherals control architecture, compiler design/optimization, programming language design, etc. Then she introduced her recent works to tackle some of these challenges, i.e. works on efficient qubit mapping, on superconducting quantum processor architecture design, and on quantum program assertions.

In total, over one hundred participants, including over 50 IEEE members/student members, attended these two seminars. The audience exhibited their interests by asking many questions. Readers can find more information about these seminars on the IEEE HK ED/SSC Chapter website: https://r10.ieee.org/hk-edssc/.

ED/SSC Shenzhen Chapter—IEEE EDS Distinguished Lecture

—by Shengdong Zhang

On 27 May, the ED/SSC Shenzhen Chapter hosted the IEEE EDS Distinguished Lecture given by Prof. Yogesh Singh Chauhan of Indian Institute of Technology Kanpur, India. The lecture was performed as a webinar due to the COVID-19 pandemic. Prof. Chauhan's lecture was titled "Modeling and Simulation of Negative Capacitance Transistors," and covered a wide range of topics around negative capacitance device modeling and simulations. The lecture attracted many audiences including the graduate students in the chapter. After the lecture there was a warm discussion on ferroelectric devices, the physics and modeling, and also on the application of modeling and simulation in the development of device technology. The lecture was invited and hosted by Dr. Paul Lining Zhang, Assistant Professor of School of Electronic and Computer Engineering, Peking University, Shenzhen.

Prof. Lain-Jong (Lance) Li from the University of Hong Kong gave invited seminar for HK ED/SSC Joint Chapter

Prof. Yogesh Singh Chauhan giving the Virtual DL

ED Xi'an Chapter—The National Semiconductor Physics Conference

—by Hongliang Lu

The National Semiconductor Physics Conference is a conference which was initiated by the late academician Huang Kun, a world-renowned physicist and the winner of the State Preeminent Science and Technology Award, in 1978. The conference is held every two years (convened in odd-numbered years) and combined with the biennial International Semiconductor Physics Conference (convened in even-numbered years). The purpose of the conference is to promote academic exchanges in the field of semiconductor physics research, grasp the development trends of major international frontier fields, and enhance the international influence of domestic semiconductor physics and related disciplines. So far, this conference has received enthusiastic support, including 8 conference reports and over 300 invited reports from experts and scholars.

This conference was hosted on 8–11 July 2021 by the School of Microelectronics of Xidian University and the Shaanxi Advanced Semiconductor Technology Center in Xi'an, Shaanxi. The themes of this conference included semiconductor quantum computing, semiconductor spin physics, semiconductor surface physics, quantum information, wide-bandgap semiconductor physics, etc. The purpose of the topic selection was to support and lead the development of multi-disciplinary information, energy, life, and materials. During the conference, the winners of the

2020–2021 Huang Kun Physics Prize (biennial) and their awarded works were announced. In order to promote the integration of industry, education and research, and provide young students and postdoctoral fellows with more employment information, this conference also specially set up a "job opportunity exchange venue".

ED Taipei Chapter—IEEE EDS Distinguished Lecture

—by Steve Chung

The ED Taipei Chapter together with the EDS NCTU Student Chapter held on 25 May 2021 the invited DL talk by Prof. Mansun Chan from Hong Kong University of Science and Technology. The Lecture title was "CMOS Interconnect Technology Beyond Copper and Low-k Dielectrics". The Lecture was arranged in a virtual format. Prof. Chan started the seminar introducing himself to the audience via a video on Youtube, https://www.youtube.com/watch?v=FZ83A6iDJak, to learn more about his background. First, the speaker then made a statement that there are two major hurdles to the scaling following Moore's law, which are interconnects and low-k dielectrics. New materials such as carbon nanotubes (CNTs) and graphene have been extensively studied to extend the scaling roadmap for interconnects. However, many barriers have to be overcome before these materials can enter mainstream manufacturing. In his talk, Professor Chan presented some solutions illustrating the recent progress in using CNT as a contact plug as well as an agent to form very low k-value interlayer dielectrics. In particular, he demonstrated a successful use of CNT to the graphene contact and interlayer capacitance reduction through air-gap technology by 2D materials. This talk was attended by more than 90 graduate students and professors.

ED Taipei Chapter—The 2021 International Symposium on VLSI Technology, Systems and Applications

—by Steve Chung and Chih-I Wu

The 2021 International Symposium on VLSI Technology Systems and Applications (VLSI-TSA 2021) was held on 19–22 April 2021 at the Ambassador Hotel Hsinchu, Taiwan. It was organized by Industrial Technology Research Institute (ITRI) and technically co-sponsored by IEEE Electron Devices Society and IEEE Solid-State Circuits Society. Prof. Steve Chung served as the General Chair of the Conference.

The Symposium was kicked-off in 1983. It is a premiere VLSI conference in Taiwan and receives up to 1,000 participants every year. The Conference venue, Ambassador Hotel is next to Hsinchu Science Park, the well-known "Taiwan's Silicon Valley," with clusters of world-class high-tech IC manufacturers and design houses.

Due to COVID-19 concerns, the VLSI-TSA 2021 was held in a hybrid format, in which an on-site meeting was provided for local participants while online access was for overseas participants. Though the pandemic was under control in Taiwan, there were travel restrictions for overseas attendees. The event featured a virtual platform with live sessions, live Q&A sessions, and chat rooms, creating valuable networking opportunities. Right after the physical event, the virtual platform also provided pre-recorded presentations for on-demand viewing, lasting for one month.

The meeting consisted of two half-day short course sessions, three-day technical presentations of contributed papers, as well as special sessions including "Heterogeneous Integration", "Low Temperature Electronics", "Low Dimensional Materials and Devices", "Hardware Security", and "Biomedical Sensors and Devices".

The three-day conference started with a joint plenary session with three distinguished keynotes from Dr. Lipen Yuan (TSMC) on "Logic Technology Scaling: Present and Future", Prof. Evan Reed (Stanford University) on "Finding a Needle in a Haystack: Success Stories of Data Mining and Machine Learning for Electronic Materials Selection", and Dr. Masanao Yamaoka (Hitachi) on "Domain-specific In-memory Computing Architecture: CMOS Annealing Machine to Solve Combinatorial Optimization Problems". Together with a concurrent VLSI-DAT symposium, there were two joint special sessions, "In-Memory Computing" and "Design-Technology Co-Optimization and Advanced Packaging".

ED Taipei, Invited DL talk 25 May 2021 via virtual presentation

(Left) VLSI-TSA 2021 Symposium; (Right) Prof. Takao Someya from the University of Tokyo joined the live Q&A in the conference

The next VLSI-TSA will be back in Taiwan, 18–21 April 2022 at the Ambassador Hotel Hsinchu. The paper submission due date is: 31 October 2021. The attendees from industry may take this opportunity to visit Science Park business units, whereas the attendees from academia may visit major universities/Research Institutes of Taiwan. For more details, please visit: https://expo.itri.org.tw/2022vlsitsa

ED Tainan Chapter—IEEE EDS Distinguished Lecture

—by Wen-Kuan Yeh

The ED Tainan Chapter held one Distinguished Lecturer presentation on `5 April 2021. Professor Cher-Ming Tan (Director, Center for Reliability Science and Technologies, Professor in Department of Electronics, Chang-Gung University) gave a talk in Cheng-Kung University, Tainan, Taiwan. The topic was "Reliability and failure physics modeling of electronic components and systems." This talk focused on the modeling of reliability and failure physics in electronic components and systems. Several aspects discussed include the finite element modeling of materials degradation, the reliability of Li-ion batteries and high power LEDs, and the statistical modeling of reliability in engineering systems, nano-materials and devices. About 45 attendees including students, professors of universities and engineers from south Taiwan attended this DL.

First row from left: Prof. C. H. Huang (NCKU), Dr. Y. J. Lee (TSRI), Y. H. Wang (NCKU). Prof. Cher-Ming Tan (DL speaker), Wen-Kuan Yeh (Chair of EDS Tainan Chapter) with attendees in the background

EDS Kansai Chapter—Technical Online Meeting

—by Yuichi Ando

EDS Kansai Chapter hosted the Technical online meeting on 14 June 2021. The meeting organizers invited two famous speakers to give the speeches. Dr. Toshihiro Ohki from Fujitsu Limited was invited to talk about "High-Frequency Device and Material Technologies for the Progress of 5G and 6G Mobile Telecommunications". Prof. Tsuyoshi Sekitani from Osaka University gave a speech on "R&D and social implementation of stretchable flexible electronics." The meeting had 149 attendees, including 17 EDS members and students enjoying two distinguished talks.

We would also like to announce the 2021 International Meeting for Future of Electron Devices, Kansai (IMFEDK), sponsored by IEEE EDS Kansai Chapter, which will be organized on 17–19 November 2021. The meeting will be held either online (Zoom) or in a hybrid mode (Avanti Kyoto Hall, Kyoto, Japan), in accordance with the pandemic status. The IMFEDK 2021 webpage is https://www.ieee-jp.org/section/kansai/chapter/eds/imfedk/

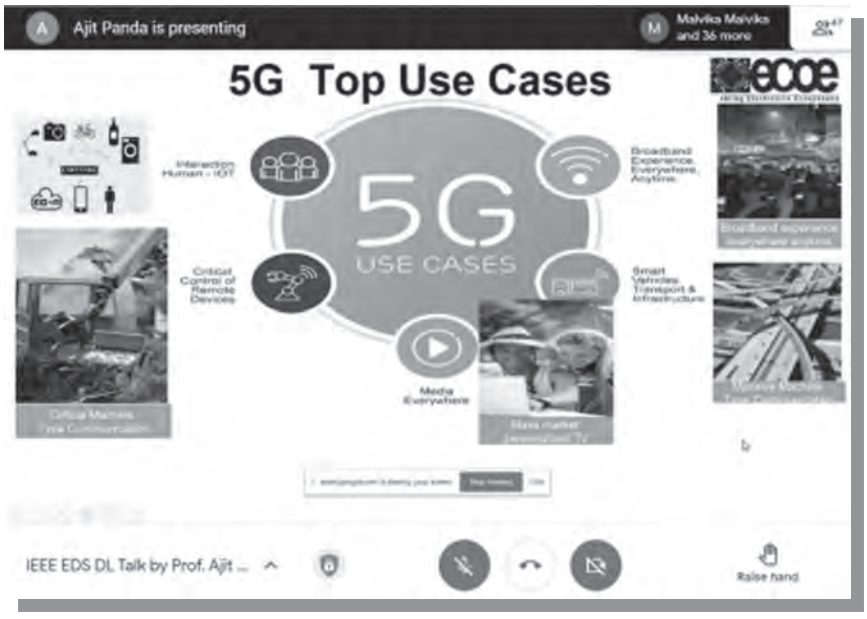
Dr. Toshihiro Ohki of Fujitsu Limited talked about "High-Frequency Device and Material Technologies for the Progress of 5G and 6G Mobile Telecommunications"

~Alex Hou, Editor

ED NIT Silchar Student Branch Chapter

—by T.R. Lenka

The ED National Institute of Technology (NIT) Silchar Student Branch Chapter, Assam, India, in association with IEEE Nanotechnology Council Chapter and Department of Electronics and Communication Engineering, NIT Silchar organized a series of three distinguished lectures in a virtual mode. The first one, held on 22 May, 2021, was delivered by Prof. Ajit Kumar Panda on the topic "Semiconductor Devices for 5G Communication Technology." The speaker discussed in an elegant manner the evolution of semiconductor devices



Virtual mode of presentation by Prof. Ajit Kumar Panda (DL); Prof. F. A. Talukdar (Branch Counselor), Dr. T. R. Lenka (Chapter Advisor), Dr. Koushik Guha (Secretary) were present online

from simple transistors to state-of-the-art HEMT devices. The second lecture was given on 29 June 2021 by Prof. Jesús A. del Alamo of Microsystems Technology Laboratories, Massachusetts Institute of Technology, USA. The topic was "3D Integration: Above and Beyond Moore's Law." The recent developments on the complexities of integrating multi-million gates in integrated circuits and approaches for mitigating such challenges using 3D techniques were discussed in a manner well understood by a large number of participants. The last lecture was given on 30 June 2021 by Prof. Patrick Fay of the Department of Electrical Engineering, University of Notre Dame, IN, USA. The title was "Advances in III-N Devices for 5G and Beyond". The lecturer introduced modern high speed circuits and devices.

Meghnad Saha Institute of Technology ED Student Branch Chapter

—by M.Chanda

Meghnad Saha Institute of Technology (MSIT), ED Student Branch Chapter (SBC) in association with IEEE Student Branch of the Institute and the Department of Electronics and Communication Engineering (ECE) organized a series of three technical seminars given by the alumni of the Institute. The first was given on 22 May 2021 by Ms. Anwesha Lahiri, (ECE batch 2015–19) currently at Open Silicon. She delivered her talk titled "Journey from MSIT to Open Silicon". The second seminar was given on 29 May 2021 by Mr. Bitan Mallik (ECE batch 2009–13) currently working as a research associate in Fraunhofer, Germany. The title of the seminar was "Journey from MSIT to Fraunhofer IIS". The last talk was given by the alumnus Mr. Samrat Manna who is currently an associate consultant in TCS, Southampton-UK. He gave his talk on 5 June 2021 on the topic "Journey from MSIT to TCS, Southampton-UK". All the seminar presentations were well attended by the students of the department. They motivated them for a bright career ahead.

The Chapter also organized on 19 June 2021 another technical seminar in a virtual mode. The speaker was Mr. Sumilak Chaudhury, Design Engineer II, Cadence Design Systems India Pvt Ltd. The topic was "Visualizing Transient Response in Passive Circuit Components", which is a useful topic for the undergraduate students. About 83 participants comprising undergraduate students of the departments including 18 IEEE Student Members, and a few professors were present during the seminar.

Netaji Subhash Engineering College ED Student Branch Chapter

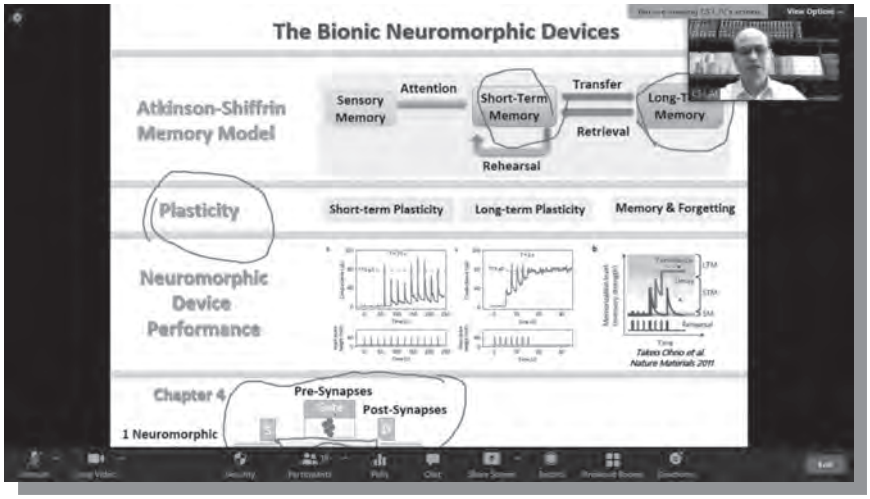
—by Sweta Sarkar and Dr. Saheli Sarkhel

The Chapter organized a membership drive program held virtually on 20 April 2021. The office representatives and members of the Chapter executive committee met with around 45 students of the 1st year course. The new students were motivated through an online presentation to join the Student Branch Chapter. The benefits of being an EDS student member in their career were explained in detail. The meeting aroused a deep interest among the students, which is reflected in their interactions with the Chapter members.

Uttar Pradesh Section Chapter, ED Kanpur Chapter

—by Y.S.Chauhan

The chapter organized a series of three distinguished lectures. The first lecture was delivered by Prof. Marcelo Antonio Pavanello (Full Professor at Department of Electrical Engineering at Centro Universitário da FEI, Brazil) on "Compact Continuous Model of Drain Current and Trans-capacitances of Junctionless Nano-wire Transistors." The second lecture was given by Prof. Chao-Sung Lai (Professor and Institute Dean of Engineering, Department of Electronic Engineering, Chang Gung University, Taiwan) on "Nitrided and Fluorinated Graphene and MoS2 for Transistors, Memristors and Optical Neuromorphic Computing". The last one was delivered by Prof. Yang Chai (Associate Professor, Department



Virtual mode of presentation by Prof. Chao-Sung Lai

of Applied Physics, The Hong Kong Polytechnic University, Hong Kong) on "Near-/in-sensor Computing for Neuromorphic Machine Vision." Apart from this, three technical seminars were also organized with eminent speakers from academia. They were Dr. Chithra Jayaraj of IIT Madras, Dr. Rituraj of Stanford University, USA, and Dr. Mahitosh Biswas of IIT Bombay. The lectures boosted the knowledge and exposed the members to diverse research areas including time-to-digital converter chip for neutrino observatory, nanophotonics for quantum light manipulation and III-V semiconductor nano-structures.

ED Kalyani Government Engineering College Student Branch Chapter

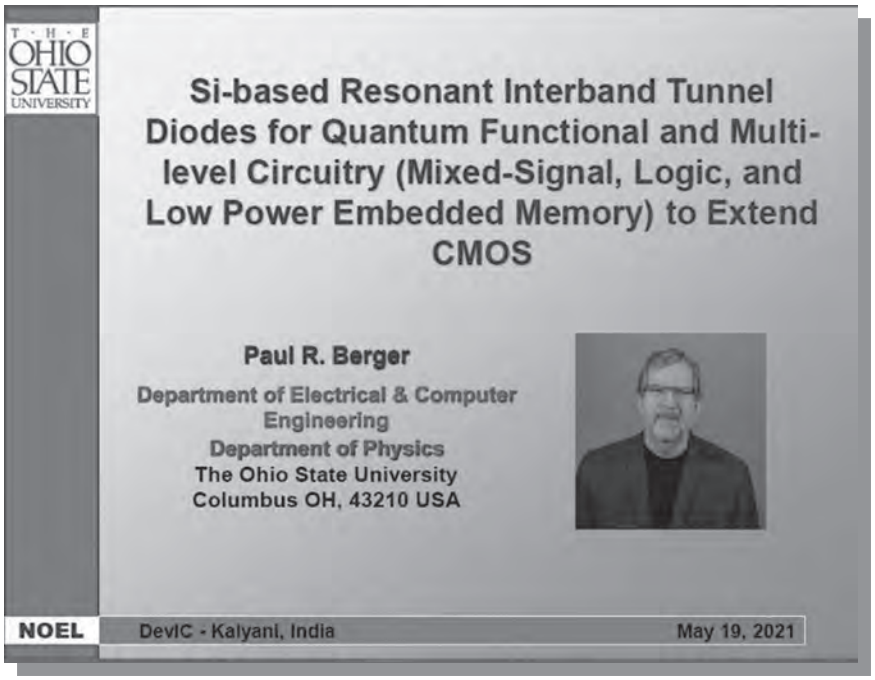
—by Angsuman Sarkar and Arpan Deyasi

The Kalyani Govt. Engineering College (KGEC) Student Branch Chapter in association with the Department of Electronics and Communication Engineering, KGEC organized the 4th International Conference on "Devices for Integrated Circuit (DevIC 2021)" in virtual mode during 19–20 May 2021. The conference was technically co-sponsored by the ED Kolkata Chapter. This year 395 participants from 4 continents [Europe (10 from 4 countries), Asia (380 from 4 countries), Africa (2 from 1 country) and North America (3 from USA)] attended the conference. The program schedule included 6 plenary talks and 144 regular contributions. The plenary talks and regular presentations were streamed live.

The first plenary talk entitled "Graphene-Based Quantum Dot for Biomedical Applications: Current Scenario and Future Prospects" was delivered by Prof. Subhankar Paul from NIT Rourkela, India. The speaker introduced the participants to the Graphene-based quantum dots and its role in many biomedical applications.

The second plenary talk entitled "Compact/SPICE Modeling from a FOSS TCAD/EDA perspective" was delivered by Dr. Wladek Grabinski. The speaker discussed the importance of compact/SPICE models for use in advanced IC design using nano-scaled semiconductor technologies in order to facilitate communication between the semiconductor companies and fabless IC design teams. Application examples of the FOSS TCAD 3D numerical simulators have been illustrated.

The third plenary talk entitled "Si-based Resonant Interband Tunnel Diodes for Quantum Functional and Multi-level Circuitry (Mixed-Signal, Logic, and Low Power Embedded Memory) to Extend CMOS" was delivered by the EDS Distinguished Lecturer Prof. Paul R. Berger from Ohio State University, USA. Prof. Berger introduced the background on Si-based tunnel diode devices and circuits. The Si-based RITD device



Plenary talk "Si-based Resonant Interband Tunnel Diodes for Quantum Functional and Multi-level Circuitry (Mixed-Signal, Logic, and Low Power Embedded Memory) to Extend CMOS" by Prof. Paul R. Berger from Ohio State University, USA

optimization and their monolithic integration with Si-based transistors were highlighted.

The fourth plenary talk entitled "Compact modeling of semiconductor devices in micro- and nanoelectronics" was delivered by Dr. Daniel Tomaszewski of the Institute of Microelectronics and Photonics, Warsaw, Poland. The speaker explained the importance of sophisticated computational models of technological processes and advanced models of semiconductor structures in the TCAD tools. The trend of semiconductor device models in the state-of-the art scaled devices was also elaborated out.

The fifth plenary talk entitled "Polymeric and three-dimensional biochips for biological investigations through microfluidics" was delivered by Dr. Maria Serena Chiriacò of the CNR NANOTEC Institute of Nanotechnology, Italy. Dr. Chiriacò introduced Labs-on-a-chip (LoCs) and the design and fabrication of polymeric lab on chips.

The final plenary talk, entitled "THM-TFET: A Physics-Based Verilog-A Compact Model of Tunnel-FETs for DC/AC Exploration of New Circuit Concepts" was delivered by Prof. Alexander Kloes of the Technische Hochschule Mittelhessen, Germany. In his visionary presentation, Prof. Kloes introduced Verilog-A compact model of Tunneling field-effect transistor (Tunnel-FET) and corresponding DC, AC and transient simulations in standard circuit simulators. The plenary talks were attended by nearly 350 participants on both of the two days.

Distinguished experts chaired various parallel sessions of the technical papers and ranked the works presented. Based upon the rank, two paper presenters; Ms. Sumedha Gupta from Delhi Technological University, Delhi, India and Dr. Rupam Goswami from Tezpur University, Assam, India was jointly awarded as winner of "DevIC 2021 Best Paper Award". The conference had benevolently exhibited their humanitarian activity when Prof. Angsuman Sarkar, General Chair- DevIC 2021, donated a token amount of Rs. fifty thousand to the West Bengal State Emergency Relief Fund for prevention and control of situations arising out of COVID-19.

ED Delhi Section Chapter

—by Harsupreet Kaur

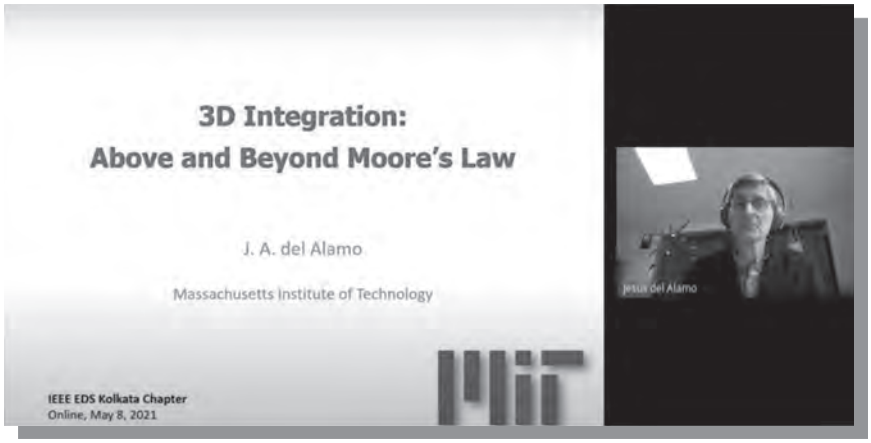
The Department of Electronics and Communication Engineering, Maharaja Agrasen Institute of Technology, Rohini, New Delhi in association with ED Delhi Chapter jointly organized a national seminar on "Latest Trends in LASER Technology and Fiber-Optics Communication," on 25–26 March, 2021. Several eminent speakers delivered lectures during the seminar. Dr. Fahim Durani of Solid State Physics Laboratory, Defence Research and Development Organisation (DRDO) delivered a lecture on "Laser Communication for Underwater Strategic Applications." It was followed by the lecture on the topic "Many Facets of Optical Fibres," by Prof. Anurag Sharma, Indian Institute of Technology, Delhi. The use of laser technology and optical fibres in various applications including defence and communication was discussed. Prof. Enakshi Sharma of the University of Delhi, Delhi, delivered a very insightful talk on "Laser and Optical Amplifiers," while Dr. Abhishek Sharma of the Solid State Physics Laboratory, DRDO shared insightful ideas about "Laser and Optical Communication." The concluding talk "Miniature Atomic Clocks" was delivered by Dr. Poorandu Chaturvedi of the Solid State Physics Laboratory, DRDO. The program was attended by over 50 participants.

ED Kolkata Section Chapter

—by Mousiki Kar

The Chapter organized a series of three distinguished lectures. Prof. Jesús A. del Alamo, of the Massachusetts Institute of Technology (MIT) spoke on 8 May 2021 on the topic "3D Integration: Above and Beyond Moore's Law." Prof. Supriyo Datta of the Purdue University, USA delivered on 29 May 2021 the lecture on the topic "Computing with p-Bits: Between a Bit and a q-Bit". Prof. Ioannis (John) Kymissis, of the Columbia University, New York, USA delivered his lecture on 19 June 2021 on the topic "Electronics on Anything: How Thin Film Electronics can Instrument the World". Except for the distinguished lectures mentioned above technical talks were also held. Prof. Prasanta Kumar Basu, of the Institute

A group of participants of the National Seminar "Latest Trends in LASER Technology and Fibre-Optics Communication"



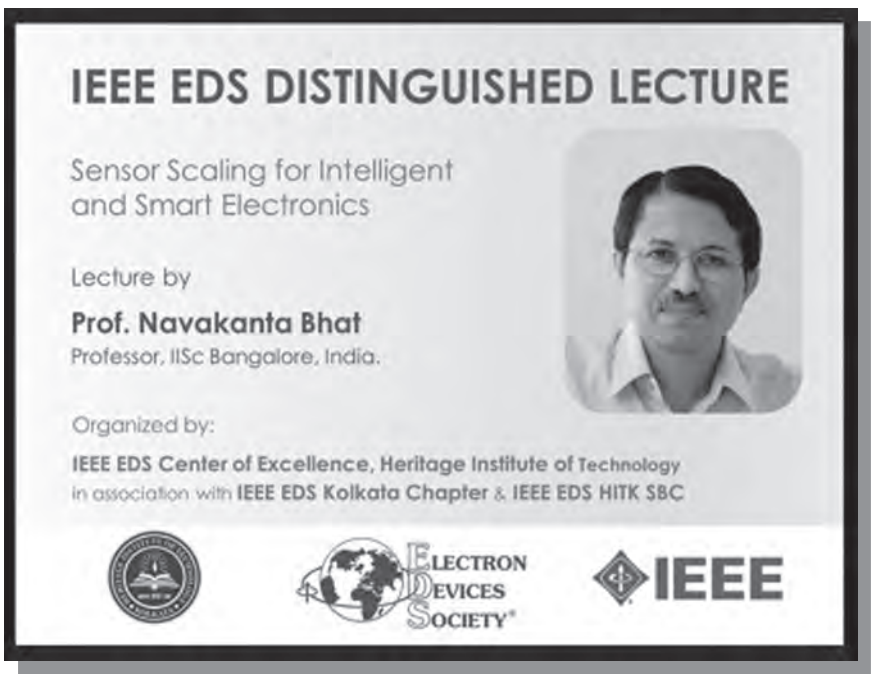
Distinguished Lecture "3D Integration: Above and Beyond Moore's Law" by Prof. J.A.del Alamo

of Radio Physics and Electronics, University of Calcutta gave a technical lecture on 5 June 2021 The topic was "Network-on-Chip: A Journey from Electronic to Electronic—Photonic to Future Plasmonic Systems." The seminar was attended by 97 participants. In addition to these, the Chapter organized jointly with IEEE Joint CSS-IMS Kolkata Chapter a membership drive program, which was held on 12 June 2021. In this program, Dr. Mousiki Kar delivered a talk on the "Benefits of IEEE Membership."

ED Centre of Excellence, Heritage Institute of Technology

—by Mousiki Kar

The Centre organized a series of three distinguished lectures. Prof. Subramanian S. Iyer, Distinguished Professor and Charles P. Reames Endowed Chair in the Electrical Engineering Department at the University of California at Los Angeles delivered a talk on "Flexible Hybrid Electronics 2.0", which was held on 17 April 2021. He spoke about the significant impact that Flexible Hybrid Electronics (FHE) is making in the area of medical and wellness electronics. 89 enthusiastic participants took part actively in the lecture session. The event was organized in association with ED HIT SBC and IEEE Kolkata Section. Prof. Navakanta Bhat of the Indian Institute of Science, Bengaluru gave his virtual lecture on 20 April 2021. The topic was "Sensor Scaling for Intelligent and Smart Electronics." The possibility of constructing an on-chip electronic nose was discussed and some other applications were presented in the lecture. The session was attended by 50 participants. The event was organized in association with IEEE EDS Kolkata Chapter and ED HIT-K, SBC. Prof. Kaushik Roy of Purdue University gave a distinguished lecture on 1 May 2021. He spoke on the topic "Re-Thinking Computing with Neuro-Inspired Learning: Devices, Circuits, and Systems." The speaker described his recent works on neuromorphic computing with spike based learning and the design of underlying hardware that can lead to quantum improvements in energy efficiency with good accuracy. The lecture was attended by 95 participants. The event was organized in association with ED HIT-K SBC and IEEE Kolkata Section.



Distinguished Lecture "Sensor Scaling for Intelligent and Smart Electronics" by Prof. Navakanta Bhat

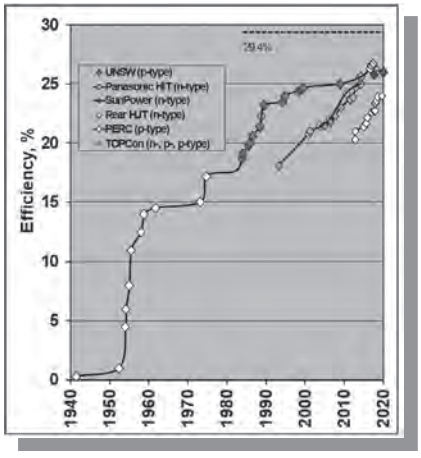
~ Soumya Pandit, Editor

ED Australia New South Wales Chapter

—by Bram Hoex

ED NSW Online Webinar on Solar Cell Technology Evolution and Future Trajectories

On 23 June 2021, the ED NSW Chapter held a webinar entitled "Solar Cell Technology Evolution and Future Trajectories" by EDS Celebrated Member Scientia Professor Martin Green from the University of New South Wales (UNSW) Sydney. The webinar had over 50 registered participants predominantly from Asia and North America. Prof Green pre-



The efficiency chart of solar cells.

sented an excellent overview of the history of the direct conversion of sunlight to electricity by solar cells.

Solar energy is now the cheapest source of electricity in most countries. It offers the lowest cost electricity the world has ever seen, with power purchase agreements (PPA) of 0.01 USD/kWh in a recent auction in Saudi Arabia. This tremendous reduction in the cost of solar electricity, particularly in the last two decades, resulted from the significant development of the solar industry in China, often by UNSW-trained entrepreneurs. In the last five years, the price reduction has been largely enabled by introducing the PERC (passivated emitter and rear contact) solar cell in industry, a higher efficiency silicon solar cell architecture that Prof Green invented at UNSW in the early 1980s. In addition to a new solar cell architecture, the industry has been reducing costs at every part of the value chain enabled by technological advancements such as continuous Czochralski pulling, diamond wire sawing, increasing the solar cell size, and shingling the solar cells to increase the fraction of the solar module that is covered with semiconductor.

The solar industry will still be able to increase the performance of silicon solar cells in the next few years until they reach the practical industrial limit of the single-junction silicon solar cell. After that, Prof Green believes that the industry will move to so-called tandem solar cells in which two solar cells with different band gaps are stacked on top of each other. Stacking solar cells reduces the fundamental losses of the solar cell and consequently allows for higher energy conversion efficiencies. Prof. Green explained that initially one up to two higher band gap thin film solar cells would be stacked on top of a silicon bottom cell extending the life of silicon in solar energy even further. Ultimately, the industry might move to a complete thin film tandem solar cell based on their experience on the first few generations of silicon-based tandem solar cells. As the candidate for the top cell in the first silicon-based tandem is not yet decided, let alone the materials for the subsequent generations, Prof Green is confident that there is still a strong need for academic research in the area of solar energy.

ED Malaysia Kuala Lumpur Chapter

—by Maizatul Zolkapli, Nurul Ezaila Alias, Aliza 'Aini Md Ralib, Rosminazuin Ab Rahim, and Norhayati Soin

EDS Malaysia Chapter Received Educational Project Grants From IEEE R10 EAC

Three EDS members had received the R10 EA grants under the 2021 Reaching Local Initiatives and New Innovation Challenge Under Educational Activities. The Reaching Local Initiatives project aims to encourage and support local Operational Units (OUs) such as Councils, Sections, Sub-sections, Chapters, Student Branches, WIE, YP, Life members and Affinity Groups to conduct activities and/or produce resources to reach out to the community using local languages. The New Innovation Challenge Under Educational Activities is focusing on the creative and new innovative programs which will provide values to the IEEE community, in alignment with MGA/EAB goals and 2020–2025 IEEE Strategic focus on Lifelong Learning. Congratulations to the following recipients: Dr. Aliza 'Aini Md Ralib, the leader of the project "Let's code with Microbit" (category: "Reaching Local Initiatives") was granted USD 400, Dr. Maizatul Zolkapli, the leader of the project "Enriching orphans through curiosity with graphite" (category: "Reaching Local Initiatives") was granted USD 150, and Assoc. Prof. Dr. Rosminazuin Ab Rahim, the leader of the projects "Let's Play Robot with TryEngineering" (category: "Reaching Local Initiatives") and "Do-Your-Bit Nature Challenge" (category: "New Innovation Challenge Under Educational Activities") was granted USD 175, and USD 200 respectively.

EDS Malaysia Chapter Membership Drive and Technical Talk

The ED Malaysia Chapter organized a membership drive in conjunction with the technical talk on Sustainable Flexible Electronics in e-Waste Management organized by Malaysian Polytechnic and Community College. During the talk Prof. Dr. Norhayati Soin had introduced IEEE EDS to the 290 participants who were mostly polytechnic and community college lecturers and students throughout Malaysia. The activity was held virtually on 30th June 2021 and received positive feedback from the participants.

13th 2021 IEEE Regional Symposium on Micro and Nanoelectronics (RSM)

The ED Malaysia Chapter is pleased to welcome everyone to participate in the 2021 IEEE Regional Symposium on Micro and Nanoelectronics (RSM) on 2–4 August 2021. Since 1997, this bi-annual technical conference aims to bring together researchers from industry and academia to gather and explore various issues and trends in the field of semiconductor electronics. This will be the 13th RSM organized by the Electron Devices Chapter of IEEE Malaysia Section and technically

2021 IEEE Regional Symposium on Micro and Nanoelectronics (RSM) on 2–4 August 2021

co-sponsored by the IEEE Electron Devices Society. Over the last twenty-four years, RSM conference series has become the prominent international forum on semiconductor electronics embracing numerous aspects of the semiconductor technology including circuit and device modelling and simulation, photonics and sensor technology, MEMS technology, packaging technology, failure analysis and reliability, materials and devices for nanoelectronics. Please visit the website for further details https://ieeemalaysia-eds.org/rsm2021.

~Sharma Rao Balakrishnan, Editor

New Sources for Electron Device Content

EDS Resource Center—electron device educational content. The place to find short courses, technical panels, workshops, and more. Make this your first stop to find electron device technical training. New offerings added as they become available.

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EDS MEETINGS CALENDAR

THE COMPLETE EDS CALENDAR CAN BE FOUND AT OUR WEB SITE: HTTP://EDS.IEEE.ORG. PLEASE VISIT.

2021 International Semiconductor Conference (CAS)	06 Oct – 08 Oct 2021	Virtual Event
2021 16th European Microwave Integrated Circuits Conference (EuMIC)	~~10 Oct – 11 Oct 2021~~	POSTPONED to 13-18 February 2022
2021 IEEE/ACM International Conference On Computer Aided Design (ICCAD)	01 Nov – 05 Nov 2021	Munich, Germany Hybrid Event
2021 IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)	06 Nov – 08 Nov 2021	Redondo Beach, CA
2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)	06 Dec – 09 Dec 2021	Monterey, CA Virtual
2021 IEEE 52nd Semiconductor Interface Specialists Conference (SISC)	08 Dec – 11 Dec 2021	San Diego, CA
2021 IEEE International Electron Devices Meeting (IEDM)	11 Dec – 16 Dec 2021	San Francisco, CA Hybrid Event
2022 16th European Microwave Integrated Circuits Conference (EuMIC)	13 Feb -18 Feb 2022	London, United Kingdom
2022 IEEE 34th International Conference on Microelectronic Test Structures (ICMTS)	20 Mar – 23 Mar 2022	Cleveland, OH
2022 IEEE International Reliability Physics Symposium (IRPS)	27 Mar – 31 Mar 2022	Dallas Texas

2022 23rd International Vacuum Electronics Conference (IVEC)	25 April – 28 April 2022	Monterey, CA
2022 IEEE International Memory Workshop (IMW)	15 May – 18 May 2022	Dresden, Germany
2022 34th IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD)	22 May – 26 May 2022	Vancouver, BC, Canada
2022 IEEE Symposium on VLSI Circuits	08 June – 18 June 2022	Honolulu, HI
2022 IEEE Symposium on VLSI Technology	08 June – 18 June 2022	Honolulu, HI
2022 IEEE International Interconnect Technology Conference (IITC)	27 June – 30 June 2022	San Jose, CA
2022 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)	16 Oct – 20 Oct 2022	Phoenix, AZ
2022 International Electron Devices Meeting (IEDM)	02 Dec – 08 Dec 2022	San Francisco, CA
2022 IEEE 50th Semiconductor Interface Specialists Conference (SISC)	08 Dec – 10 Dec 2022	San Diego, CA

EDS Vision, Mission and Field of Interest Statements

Vision Statement
Promoting excellence in the field of electron devices for the benefit of humanity.

Mission Statement
To foster professional growth of its members by satisfying their needs for easy access to and exchange of technical information, publishing, education, and technical recognition and enhancing public visibility in the field of Electron Devices.

EDS Field of Interest
The EDS field-of-interest includes all electron and ion based devices, in their classical or quantum states, using environments and materials in their lowest to highest conducting phase, in simple or engineered assembly, interacting with and delivering photo-electronic, electro-magnetic, electromechanical, electro-thermal, and bio-electronic signals. The Society sponsors and reports on education, research, development and manufacturing aspects and is involved in science, theory, engineering, experimentation, simulation, modeling, design, fabrication, interconnection, reliability of such devices and their applications.