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Newsletter

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IEEE

Morris Chang Recognized as the 2022 IEEE EDS Celebrated Member of the Institute of Electrical and Electronics Engineers (IEEE)

The Institute of Electrical and Electronics Engineers (IEEE) named Dr. Morris Chang, TSMC, as the "IEEE EDS Celebrated Member" of 2022. This recognition will take place during the 2022 IEEE International Electron Devices Meeting (IEDM) in San Francisco, California, U.S.A. EDS takes pride in the accomplishments of our Celebrated Members and draw from the inspiration to advance our field and to achieve more because it is not only their work but ours as well, that can help transform the world around us.

Dr. Morris Chang founded Taiwan Semiconductor Manufacturing Company Ltd. (TSMC) in 1987, served as its Chairman for 31 years, and its CEO for many of those 31 years. Dr. Chang retired from TSMC in June 2018. TSMC pioneered the dedicated silicon foundry business model and has served as a powerful force of innovation in the information industry.

Prior to his career in Taiwan, Dr. Chang's career was in the United States. He served at Texas Instruments for 25 years (1958–1983), where he was Group Vice President responsible for worldwide semiconductor business for six years.

Dr. Chang received his B.S. and M.S. degrees in Mechanical Engineering from M.I.T. in 1952 and 1953, and his Ph.D. in Electrical Engineering from Stanford in 1964. He has received honorary doctorates from eight universities worldwide.

Dr. Chang received many honors and awards in his career. Among them were: the "Exemplary Leadership Award" of the Global Semiconductor Alliance (GSA) (1999), the IEEE Robert N. Noyce Medal for Exceptional Contributions to Microelectronics Industry (2000), Nikkei Asia Prize (2005), and the highest honor of the Semiconductor Industry Association (U.S.), its Robert N. Noyce Award (2008). He received the IEEE Medal of Honor (2011), the R.O.C. Order of the Brilliant Star (2011), the SEMI Akira Inoue award for green

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CONTRIBUTIONS WELCOME

Readers are encouraged to submit news items concerning the Society and its members. Please send your ideas/articles directly to either Editor-in-Chief or the Regional Editor for your region. The email addresses of all Regional Editors are listed on this page. Email is the preferred form of submission.

NEWSLETTER DEADLINES

ISSUE	DUE DATE
October	July 1st
January	October 1st
April	January 1st
July	April 1st

The EDS Newsletter archive can be found on the Society web site at http://eds.ieee.org/eds-newsletters.html. The archive contains issues from July 1994 to the present.

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Moore's Law Scaling and Radiation Effects in MOS Devices

By Dan Fleetwood, Vanderbilt University

Microelectronic devices and ICs experience high radiation levels in space, defense, and particle accelerator environments. After the invention of the transistor in 1947 [1], radiation effects research focused primarily on defect creation in semiconductor materials and displacement damage in bipolar junction transistors [2]–[5]. The sensitivity of MOS transistors to total ionizing dose (TID) effects was discovered by Hughes and Giroux in 1964 [6], just one year before Moore's law was postulated [7], [8]. An early and influential study of TID effects in MOS devices was co-authored in 1967 by a young Andy Grove, while still at Fairchild Semiconductor [9], [10]. The modern era of radiation-tolerant MOS electronics began in 1971 with the development of radiation-hardened *p*MOS technology by Hughes Aircraft Company [8], [11].

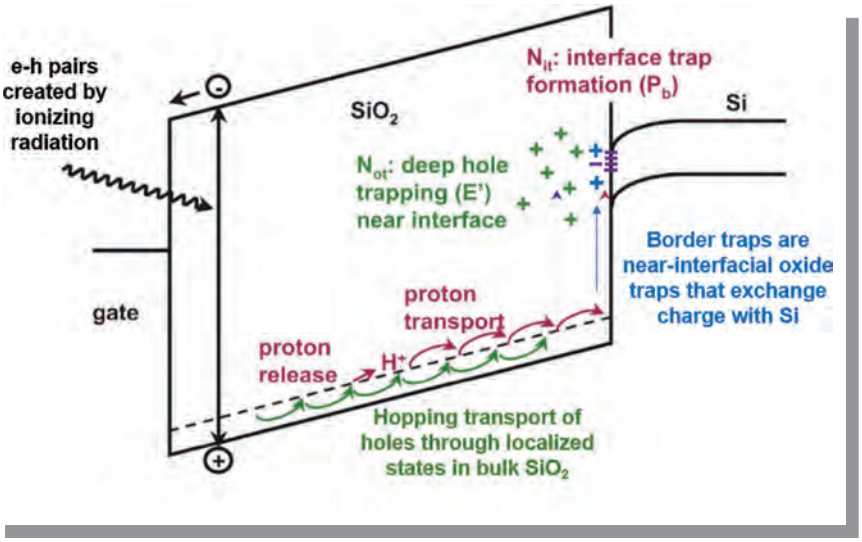

Figure 1. Schematic illustration of electron-hole pair generation, charge transport, and trapping in irradiated MOS devices. (After [8], [12], [13].)

Fig. 1 illustrates the chain of events that occur during and after TID-irradiation of MOS devices [8], [12], [13]. Primary effects include hole transport and trapping in gate and isolation oxides and buildup of interface and border traps at or near gate-dielectric/semiconductor boundaries. Proton (H^+) release during hole transport and field-induced H^+ transport to the Si/SiO_2 interface play critical roles in interface and border-trap formation [8], [12], [13].

Moore's Law scaling and changes in device architecture significantly affect MOS radiation response [10], [14]–[17]. Progressively thinner gate and isolation oxides in highly scaled devices (Fig. 2) generally lead to enhanced TID tolerance (Fig. 3). However, in current and future generation FinFETs (Fig. 2(c)), gate-all-around, and nanosheet or forksheet devices, the thickness and quality of the gate insulator and isolation oxides, transistor channel/edge doping levels, and strength of gate control all strongly affect charge trapping [10], [14]–[17]. Thus, significant variations are expected and observed in the TID response of MOS devices and ICs [10], [16].

As MOS technologies have evolved and device dimensions and operating voltages have decreased, single-event effects (SEE) due to cosmic rays and/or high-energy protons have become an increasing concern. When a single high-energy charged particle deposits a sufficient amount of energy per unit path length to generate a densely ionized track, soft or hard errors can result, with probabilities determined by the amount of collected charge and resulting device/IC response [10], [16], [18]–[20]. Until the ~130 nm technology node, SEE in electronics in space environments typically increased with decreasing feature size, as seen in Figs. 4 and 5. This is due primarily to reductions in operating voltage and critical charge to upset [10], [16], [18]–[20]. Fortunately, Moore's Law scaling greatly enhances design, layout, modeling, and simulation capabilities, which are increasingly necessary to understand and mitigate the resulting effects [14], [16], [18].

By the mid-1990s, device scaling made terrestrial electronics sensitive to soft errors caused by reactions of atmospheric neutrons in silicon and surrounding materials [21], [22]. Removing B_{10} from processing and changing to FinFET/Tri-Gate

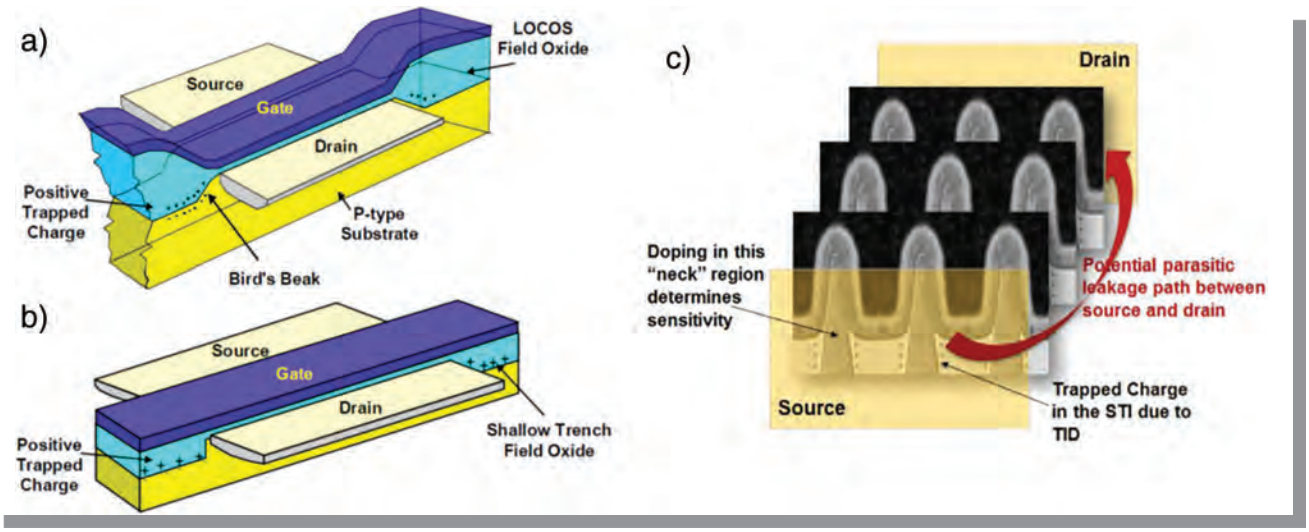

Figure 2. MOS devices with (a) LOCOS (local oxidation of silicon) or (b) shallow-trench isolation, STI [15]. (c) Bulk FinFETs [17].

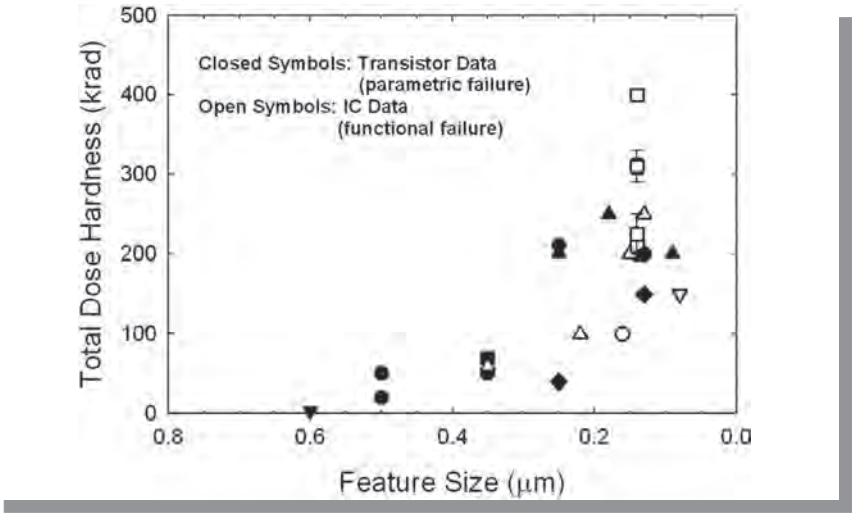

Figure 3. Hardness of MOS ICs to TID vs. feature size. (After [16].)

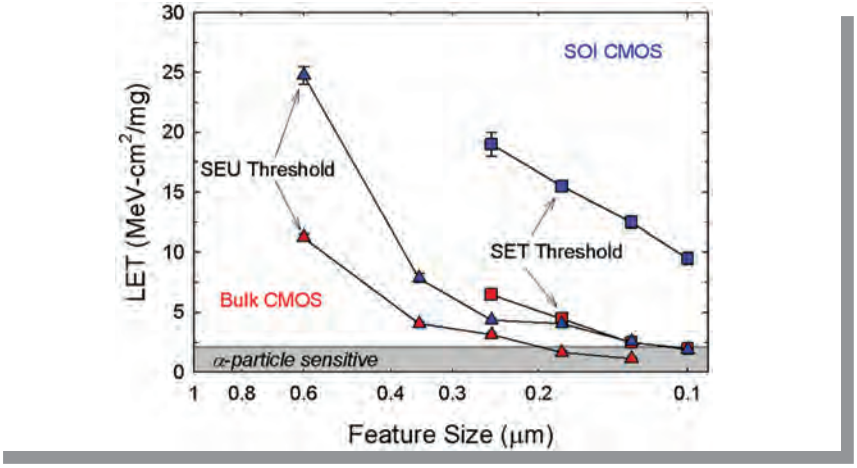

Figure 4. Critical ion LET (linear energy transfer) to failure vs. feature size for planar bulk and SOI (silicon on insulator) CMOS ICs. The buried oxide layer makes SOI devices less sensitive to SEE. (After [16].)

architecture (Fig. 5, inset) can greatly reduce SERs in ICs [19], [22]. However, as transistor sensitive volumes become smaller than ion tracks and transistor packing densities continue to increase, multiple-bit errors and "charge sharing" among adjacent devices become more significant [10], [16], [18]. ICs now are more three-dimensional, and nanoscale MOS devices can be sensitive to single-particle displacement damage [10], [23]. Thus, each new IC technology generation continues to present new radiation-effects challenges.

Biography

Dan Fleetwood received his Ph.D. from Purdue University in 1984. He joined Sandia National Laboratories in 1984 and was named a Distinguished Member of Technical Staff in 1990. Dan joined Vanderbilt University as a Professor of Electrical Engineering in 1999. From 2003–2020 he chaired Vanderbilt's EECS Department; since 2009 he has been appointed Olin H. Landreth Chair in Engineering. He received the 2009 IEEE Nuclear and Plasma Sciences Merit Award, and is a Fellow of IEEE, AAAS, and the American Physical

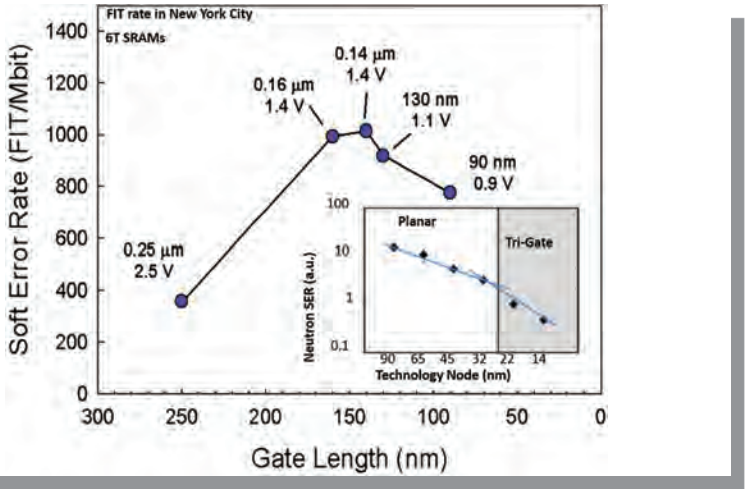

Figure 5. Feature size dependence of terrestrial-neutron soft-error rates (SER) in bulk planar six-transistor static RAMs and (inset) tri-gate (FinFET) CMOS ICs. One FIT = one failure in 10^9 h. (After [16], [22].)

Society. His research interests include radiation effects on microelectronics, low-frequency noise, and defects in microelectronic materials and devices.

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The Silicon-Germanium Heterojunction Bipolar Transistor

John D. Cressler
Regents Professor and Schlumberger Chair Professor in Electronics
School of Electrical and Computer Engineering
Georgia Tech

Seventy-five years of the transistor (shortened from "transresistance amplifier" to "transresistor" to "transistor"). Time flies. A remarkable little piece of quantum physics in action. In 2022, transistors are viral-sized, nearly as fast as a speed of light, and importantly, cleverly possess that unique golden attribute of amplification, making tiny voltages and currents larger. There are over 10^{24} transistors on Earth in 2022, made possible by the jaw-dropping exponential growth patterns embodied in Moore's law. Transistors are ubiquitous to modern life, whether seen or unseen by both purveyors and consumers of technology. Surely the word "transistor" should be added to the vocabulary of every single person on Earth. In sort, all of modern technology, without exception, from smartphones to automobiles to planes to internet to GPS, would instantly cease to function if they were subtracted from the planet. In fact, in terms of its impact on the trajectory of human civilization, one could fairly argue that the invention of the transistor is the single most important discovery in human history. Bold words, but defensible [1].

Transistor action was first observed by Bardeen and Brattain at Bell Labs in late 1947 using a point contact device. This demonstration of a solid-state amplifying object is also unique in the historical record for the precision with which we can locate it—December 23, 1947, at around 5:00 pm. The precise moment the world changed irrevocably. Snow was falling in Murray Hill, NJ. Not to be outdone, by February of 1948, Shockley, the third member of the "transistor three," developed the theory for how this clever little object did its remarkable thing, and importantly, could be further improved, leading three years later to the first bipolar junction transistor (BJT) on April 12, 1950. That first BJT was made, ironically, from Ge, not Si.

The concept of the heterojunction (a junction built from two different semiconductors) bipolar transistor (HBT) is a surprisingly old one, dating in fact to the fundamental BJT patent filed by Shockley in 1948. Given that the first bipolar transistor was built from Ge, and III-V semiconductors were not yet on the scene, it seems clear that Shockley envisioned the combination of Si (wider bandgap emitter) and Ge (narrower bandgap base) to form a SiGe HBT that would yield useful properties. The basic formulation and operational theory of the HBT, for both the traditional wide bandgap emitter plus narrow bandgap base approach found in most modern III-V HBTs, as well as the drift-base (graded) approach used in SiGe HBTs today, was pioneered by Kroemer, and was largely in place by 1957. It is noteworthy that Kroemer in fact worked hard early on to realize a SiGe HBT, without success, ultimately pushing him towards the III-V material systems for his heterostructure studies, a path that proved, in the end, to be quite fruitful for him, since he shared the Nobel Prize in physics in 2000 for his work in (III-V) bandgap engineering for electronic and photonic applications. While III-V HBTs (e.g., AlGaAs/GaAs) began appearing in the 1970s, driven largely by the needs for active microwave components in the defense industry, reducing the SiGe/Si HBT to practical reality took 30 years after the basic theory was in place, due primarily to material growth limitations.

The achievement of practical SiGe/Si heterostructures, the key to building SiGe HBTs, solidly rests on the shoulders of material scientists and crystal growers, those purveyors of the semiconductor "black arts" associated with the deposition of pristine SiGe alloys of nanoscale dimensionality onto enormous Si wafers, with near-infinite precision. Once device-quality SiGe alloys were finally achieved in the mid-1980s, progress was quite rapid.

The first functional SiGe HBT was demonstrated in December of 1987, 40 years, nearly to the day, after the first transistor. That pioneering result showed a SiGe HBT with functional, albeit leaky, DC I-V characteristics; but it was a SiGe HBT, it worked, and it was the first. It is an often-overlooked historical point, however, that at least four independent groups were simultaneously racing to demonstrate the first functional SiGe HBT. Worldwide attention became squarely focused on SiGe HBT technology in June of 1990, with the eyebrow-lifting demonstration of a SiGe HBT with a peak cutoff frequency of 75 GHz by IBM, at the time twice the performance of state-of-the-art Si BJTs, clearly demonstrating the future potential of the Si-processing-compatible SiGe technology. The pursuit of SiGe HBTs for practical circuit applications began in earnest at a large number of industrial and university laboratories around the world, a trend that has not let up since and likely never will [2]–[3].

While it may be tempting to assume that CMOS is the only transistor game in town, SiGe HBTs are alive and well, and growing rapidly in both sophistication and diversity of utilization. SiGe HBT (Fig. 1) frequency response since

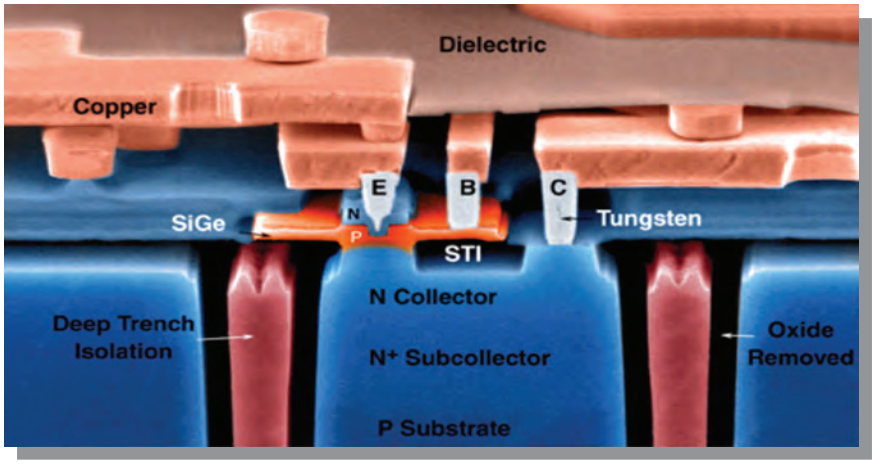

Figure 1. Decorated cross-sectional scanning electron micrograph of a SiGe HBT. The epitaxial SiGe alloy is shown in orange. (Courtesy of IBM Corporation.)

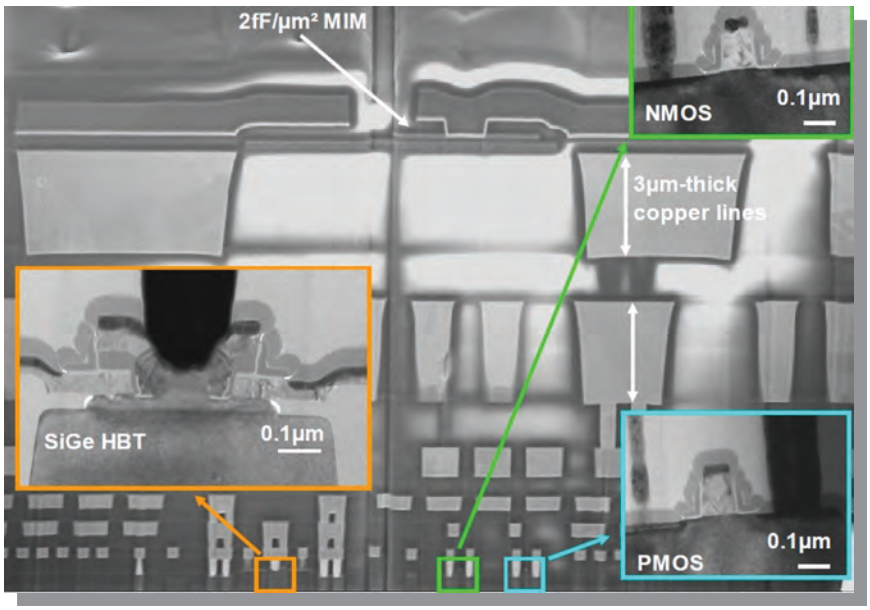

Figure 2. Cross-sectional scanning electron micrograph of a modern SiGe BiCMOS platform, showing SiGe HBT, CMOS devices (n-channel and p-channel), and the back-end-of-the-line metallization layers and passive elements. (Courtesy of P. Chevalier and ST Microelectronics.)

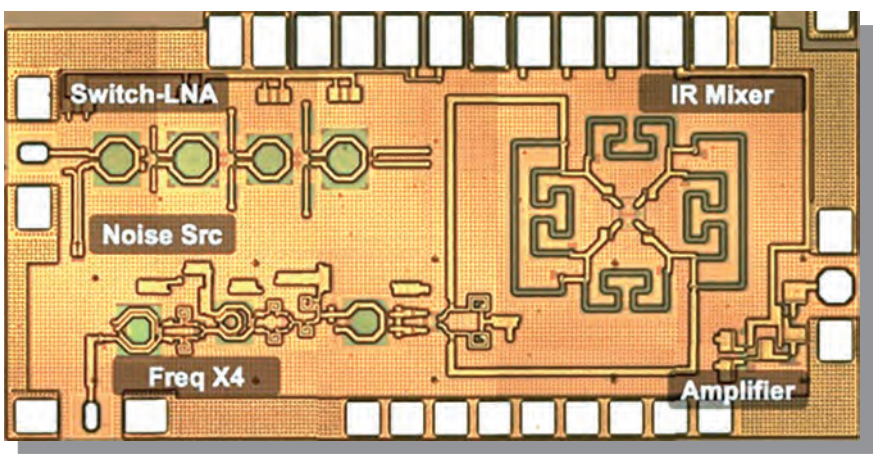

Figure 3. Example of a SiGe BiCMOS mm-wave integrated circuit, a 60 GHz SiGe radiometer for space-based remote sensing designed for use on a CubeSat. The die size is less than 2 mm².

that pivotal 1990 unveiling has grown by 10x in only thirty years! Quite a feat. SiGe HBTs are now approaching THz levels of performance in 100% Si manufacturing compatible commercial platforms (>700 GHz and counting at 300K in 2022), something unimaginable at the field's inception.

Now universally practiced as a BiCMOS technology platform (SiGe HBT + CMOS together on die), SiGe technology (Fig. 2) offers an ideal division of labor between bipolars and FETs, which each have their own respective attributes, clearly, and remains in wide use globally in performance-constrained analog, RF through mm-wave, and even digital applications (Fig. 3). SiGe HBTs also possess a natural affinity for robust operation in so-called "extreme environments," which include exposure to intense space radiation and at deep cryogenic temperatures [4].

There you have it—the SiGe HBT. A remarkable product of human ingenuity and hard work. Happy anniversary to the transistor, and its remarkable SiGe HBT progeny!

Biography

John D. Cressler received his B.S. from Georgia Tech in 1984, and his Ph.D. from Columbia University in 1990. From 1984 to 1992, he was on the research staff at the IBM Thomas J. Watson Research Center, and from 1992 to 2002 he served on the faculty at Auburn University. In 2002, he joined the faculty at Georgia Tech, and is currently Regents Professor and Schlumberger Chair Professor in Electronics in the School of Electrical and Computer Engineering, as well as the Ken Byers Teaching Fellow in Science and Religion. The basic thrust of Cressler's research is to develop Si/SiGe-based micro/nanoelectronic and photonic devices, circuits, and systems for next-generation applications within the global terrestrial and space-based electronics/

photonics infrastructure. His research interests include: Si-based (SiGe/strained-Si) heterostructure devices and technology, mixed-signal circuits (analog, digital, RF to mm-wave) built from these devices, integrated Si/SiGe photonic devices and circuits, novel scientific instruments for space-systems, radiation effects in electronic and photonic devices and circuits, cryogenic electronics for quantum systems, device-to-circuit interactions, reliability physics, device-level simulation (TCAD), and compact circuit modeling. He and his students have published over 750 scientific papers in this field, and he has graduated 66 Ph.D. students during his 30-year academic career. He was elected Fellow of the Institute of Electrical and Electronics Engineers (IEEE) in 2001 for his research contributions, and was awarded the 2010 *Class of 1940 W. Howard Ector Outstanding Teacher Award* (Georgia Tech's top teaching award), the 2011 *IEEE Leon Kirchmayer Graduate Teaching Award* (the IEEE's top graduate teaching award), the *Class of 1934 Distinguished Professor Award* (the highest honor Georgia Tech bestows on its faculty), and the 2021 *IEEE James H. Mulligan, Jr. Education Medal* (the highest award IEEE gives in teaching and mentoring). He has served the Electron Devices Society in a number of roles, including as Editor-in-Chief of *IEEE Transactions on Electron Devices*, from 2012-2015. Cressler's books include *Silicon-Germanium Heterojunction Bipolar Transistors*, *Reinventing Teenagers: the Gentle Art of Instilling Character in Our Young People*, *Silicon Heterostructure Handbook*, *Silicon Earth: Introduction to Microelectronics and Nanotechnology*, *Extreme Environment Electronics*, and the historical novels *Emeralds of the Alhambra*, *Shadows in the Shining City*, and *Fortune's Lament*, love stories set in medieval Muslim Spain.

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Morris Chang Recognized as the 2022 IEEE EDS Celebrated Member of the Institute of Electrical and Electronics Engineers (IEEE)

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management (2011), Businessman of the Year by Forbes Asia magazine (2012), the Visionary Award from SPIE (the international society for optics and photonics) (2014), and the R.O.C. Order of Propitious Clouds with Special Grand Cordon (2018).

Dr. Chang is a Member of National Academy of Engineering (U.S.A.), a Laureate of the Industrial Technology Research Institute (Taiwan), a Life Member Emeritus of MIT Corporation (U.S.A.), and Fellow of the Computer History Museum (U.S.A.).

IEEE is the world's largest association of technical professionals, and the Celebrated Member distinction honors and recognizes esteemed alumni whose accomplishments inspire young scholars and researchers and take the field to new heights.

For more information, please visit https://eds.ieee.org/members/celebrated-members.

Ravi Todi, EDS President

The 2022 IEEE VLSI Symposium on Technology & Circuits, Now Fully Combined As A Single Event

The 2022 Symposium on VLSI Technology & Circuits, completing its 42nd year of delivering a unique convergence of technology and circuits for the microelectronics industry, was held as a five-day hybrid event from 12–17 June 2022 in Honolulu, Hawaii, combining both live sessions onsite at the Hilton Hawaiian Village, as well as on-demand access to selected presentations. Newly merged as a single event, the Symposium featured the theme: "Technology & Circuits for the Critical Infrastructure of the Future." More than 1,293 people attended the Symposium, with a nearly equal split between those attending in person, and those participating virtually.

The weeklong Symposium continued its reputation as the microelectronics industry's premiere international conference integrating technology, circuits, and systems with a range and scope unlike any other conference, including advanced VLSI technology developments, innovative circuit design, and the applications they enable, such as artificial intelligence, machine learning, IoT, wearable/implantable biomedical applications, big data, cloud/edge computing, virtual reality (VR)/augmented reality (AR), robotics, and autonomous vehicles.

The main Symposium technical program featured 270 technical papers. In addition to the technical presentations, the Symposium program featured a demonstration session, evening panel discussions, joint focus sessions, short courses, workshops, and a special forum session on Friday following the Symposium main program.

Plenary Sessions

- **"Holistic Patterning to Advance Semiconductor Manufacturing for the 2020s and Beyond," by Martin Van den Brink, President & CTO, ASML**—Presented via video, this plenary session discussed the convergence of 5G, artificial intelligence, and the billions of connected devices that promise to start a new wave of innovation, bringing advanced computing power to massive amounts of data. The key enabler continues to be affordable scaling, driven by advanced EUV lithography, computational capabilities, fast metrology and inspection. Key developments in these areas included ASML's EUV roadmap for 0.33 NA (low-NA), and the next-generation 0.55 NA (high-NA), as well as a DUV roadmap to deliver cutting edge immersive lithography.
- **"Semiconductor Innovations, from Device to System," by Yuh-Jier Mii, Senior Vice President for R&D TSMC** –This year's Symposium coincides with the 75th anniversary of the invention of the transistor and of the semiconductor industry's profound impact on the world and society at large. Technology scaling has been the key driving force behind the numerous innovations that ushered in the Information Age. As the fast-expanding new applications in 5G, AI, ADAS, AR/VR and robotics continue to propel demand for data-centric products and services, future generations of semiconductor technology will require innovations across the entire stack—from material and device to design infrastructure, architecture and system—including 3D stacking technologies to extend scaling and enable more energy-efficient computing.
- **"From System-on-Chip (SoC) to System-on Multichip (SoMC) Architectures: Scaling Integrated Systems Beyond the Limitations of Deep-Submicron Single Chip Technologies," by Chris Patrick, Senior Vice-President and General Manager, Mobile Handsets, Qualcomm Technologies, Inc.**—Relying on IP integration platforms and processes that allow rapid innovation and integration of new IP such as 5G, the mobile wireless revolution has achieved low power and low cost by quickly leveraging new technology nodes. Complex systems have been integrated in SoCs and enhanced every year as technology shrinks. However, current trends in SOCs for diverse markets like mobile, compute, automotive and AI servers will lead to impractical die sizes due to diminishing percentage area shrinkage

with future deep sub-micron technology nodes, highlighting the need for to transition to a System-on-Multichip (SoMC) approach. Partitioning the SoC into multiple die (also called chiplets) in a multichip configuration may help, but this also brings new challenges.

- **"The Rise of Memory in the Ever-Changing AI Era—From Memory to More-Than-Memory," by Seok-Hee Lee, Executive Chairman, Solidgm**—Innovation in the field of semiconductor memory has provided one of the key solutions to address the challenges of ever-changing, data-driven computing. It is no longer only important that memory technologies deliver their traditional metrics such as high performance, lower power, lower cost, and higher capacity. They also have to deliver smarter and more functionality in or near memory to minimize data movement, and break down the barrier between compute and memory.

Focus Sessions: As part of the Symposium's program integration, a series of joint focus sessions presented papers with both circuits and technology topics from BEOL processes, new concepts for transistor scaling, 6G, compute-in-memory, biomedical technology, and 3D heterogeneous integration.

Short Courses on Key VLSI Topics

Three full-day short courses were presented prior to the Symposium technical program:

- The Technology Short Course *"Monolithic & Heterogeneous Integration"* focused on advanced monolithic and heterogeneous integration with coverage of logic and memory scaling in monolithic 3D integration, chiplet-based technologies and systems, and silicon photonics.
- The Joint Short Course *"Advances in Application-Specific Computing Systems & Technologies"* explored advances in application-specific computing systems and technologies, examining the latest developments in augmented reality, quantum and photonic computing, in- and near-memory computing, and computing in stretchable electronics.
- Finally, the Circuits Short Course *"Electronics That Drive the Next Generation Smart Car"* examined the electronics that will enable the next-generation smart vehicle with presentations spanning hardware and software architecture, auto computing and infotainment systems, connectivity, sensors, and battery management.

Forum Session: The Symposium program also featured a multi-speaker full day Forum Session on "VLSI for Infrastructure and Infrastructure for VLSI," held on Friday following the technical program sessions.

- The VLSI Forum is devoted to a single topic that extends the scope of the current Symposia program, or explores emerging cutting-edge applications of VLSI. This year's forum focused on green mobility and smart semiconductor manufacturing, covering energy efficiency, security, communication, and big data, as well as technologies serving infrastructure.

In addition, three **Evening Panel Sessions** were held during the Symposium:

- *"What Will It Take To Bring New Material From Lab To Manufacturing?"*
  - Robert Clark from Tokyo Electron moderated a panel of distinguished guests from across industry and academia to provide their valuable insights and thoughts, and share their experiences on this important topic. Questions included: How can we make sure the thousands of newly explored materials in academic, government, and industry labs are relevant to manufacturing technologies? What are the fundamental factors to convert a success story to a technology transfer? Is there anything to be learned from history?
- *"Building The 2030 WorkForce: How to Attract Great Students And What to Teach Them"*
  - Prof. Boris Murmann from Stanford University moderated a panel of experts from industry and academia to offer their insights and explore a critical challenge facing the semiconductor industry. With declining university enrollment in the semiconductor fields, and a shortage of skilled engineers across the industry, what can universities do to reverse the trend and ensure a robust workforce heading into 2030? What should the students learn to best prepare them for the industry's emerging needs?
- *"Supply…Unchained? Will the Chip Shortage Continue?"*
  - This panel, moderated by Joe Macri from AMD, brought together industry experts representing viewpoints from leading foundries/IDMs, OSATs, fabless designers, materials suppliers, and equipment makers for a discussion on how the industry can come together to overcome the supply chain shortages. In addition, they addressed the topic of how the semiconductor industry landed in the current supply shortage, and what it will take to return to a healthy supply chain.

Demonstration Session

The popular in-person demonstration session was once again part of the Symposium program, after two years of virtual demonstrations. The session provided participants an

opportunity for in-depth interaction with authors of selected papers from both Technology and Circuits sessions. These demonstrations, through table-top presentations, showcased device characterization, chip operational results, and potential applications for circuit-level innovations.

Workshops
A series of workshop sessions were held during the Symposium program to provide additional learning opportunities for participants. This year's program included six workshops:

Technology Workshops
- Heterogeneous Integration—The Next Scaling Frontier: Material & Process Challenges
- Machine Learning Applications in Semiconductor Processes and Equipment Development

Circuit Workshops
- The Emerging Ecosystem of Open-Source Chip Design
- Analog/RF Circuits for IoT
- Recent Advances in Radar, mmWave, and Sub-THz: Technology, Packaging, & Circuits

Joint Workshop
- Cryogenic Electronics for Quantum Computing: covering scalable and reliable cryogenic electronics for quantum computing using a large number of qubits.

Special events at the Symposium included mentoring events for Women in Engineering and Young Professionals, sponsored by the IEEE Electron Devices Society and the Solid-State Circuits Society. The popular Joint Banquet/Luau was held on Wednesday evening, featuring Hawaiian music and dancing.

Best Student Paper Awards for each track Symposium are chosen each year based on the quality of the papers and presentations. The recipients receive a monetary award, travel cost support, and a certificate. For a paper to be reviewed for this award, the lead author and presenter of the paper must be enrolled as a full-time student at the time of submission, and must indicate on the web submission form that the paper is a student paper.

Further information about the Symposium is available at: http://www.vlsisymposium.org.

Sponsoring Organizations
The IEEE VLSI Symposium on Technology & Circuits is sponsored by the IEEE Electron Devices Society, in cooperation with the IEEE Solid-State-Circuits Society, and Japan Society of Applied Physics, in cooperation with the Institute of Electronics, Information and Communication Engineers.

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EDS is Celebrating the 75th Anniversary of the Transistor
Are you an EDS Forum Member or Chapter Chair and would like to hold an event to celebrate the 75th anniversary of the transistor? The IEEE Electron Devices Society is providing 75th-anniversary banners to any IEEE/EDS Forum Member or Chapter Chair that is holding an event to celebrate this important anniversary. Please submit the banner order form and we will ship a banner to you to display during your event. We ask that you also consider sending event photos/videos to eds@ieee.org for posting on EDS website, newsletter, and social media sites. A prize will be given for the best photo!

Order Form: https://ieeeforms.wufoo.com/forms/s92tddv1kgbs7k/

2022 IEEE International Electron Devices Meeting (IEDM) to Showcase Breakthroughs in Semiconductors and Related Technologies

- The 2022 IEDM is planned as an in-person conference 3–7 December 2022 at the Hilton San Francisco Union Square Hotel, with on-demand access afterward for those unable to travel due to COVID-19 restrictions.
- The theme is "The 75th anniversary of the Transistor, and the Next Transformative Devices to Address Global Challenges," chosen to honor the industry's historic achievements while unveiling and exploring today's breakthroughs.
- IEDM 2022 will feature tutorials, short courses, focus sessions, an evening panel session, supplier exhibits, and a career-focused luncheon to complement the technical program.
- There will be three tracks of the increasingly popular tutorials this year, not just two.

"IEDM began shortly after the transistor was invented, in recognition of its revolutionary potential," said Srabanti Chowdhury, IEDM 2022 Publicity Chair, and Associate Professor of Electrical Engineering at Stanford University. "The breakthroughs described at the IEDM since then have pushed transistors and related technologies forward. This year, for example, many of the accepted papers indicate a growing interest in the use of 2D material systems for advanced devices."

"The broad reach, interdisciplinary nature and technical depth of the topics featured at the IEDM serve as a kind of crystal ball, because they show where the industry is placing its focus," said Jungwoo Joh, IEDM 2022 Publicity Vice Chair and Process Development Manager at Texas Instruments. "Many papers this year also deal with electrothermal considerations in extremely scaled devices, because reliability and thermal management go hand-in-hand."

IEDM 68th International Electron Devices Meeting

Plenary Talks

IEDM 2022 will feature three Plenary talks on Monday, 5 December given by notable industry experts addressing some of the industry's most pressing issues. They are:

- *Celebrating 75 Years of Transistor Innovation by Looking Ahead to the Next Set of Industry Grand Challenges*, by Anne Kelleher, Executive Vice President/General Manager of Technology Development, Intel
- *Expanding Human Potential through Imaging and Sensing Technologies*, by Yusuke Oike, General Manager, Sony Semiconductor Solutions
- *Enabling Full Fault-Tolerant Quantum Computing with Silicon-Based VLSI Technologies*, by Maud Vinet, Quantum Hardware Program Manager, CEA-Leti

Evening Panel Session

On Tuesday, 6 December there will be an evening panel session on the topic, *75 Years of Transistor Technology—(No) Time for Retirement?* It will be moderated by Stefan De Gendt, Scientific Director at IMEC, and Suman Datta, Professor at Georgia Institute of Technology.

Career Luncheon

There also will be a career-focused luncheon on 6 December, featuring industry and scientific leaders talking about their personal experiences in the context of career growth. The speakers will be:

- Myung-hee Na, Vice President of SK Hynix's Revolutionary Technology Center
- Lisa Rutherford, Director of Research Science at Meta Reality Labs Research

Focus Sessions

Among this year's technical highlights are five special Focus Sessions on key emerging technologies. They are:

Advanced Heterogeneous Integration: Chiplets and System-in-Packaging

Leading-edge integrated circuits have become so complex that it's difficult to add new features and achieve higher performance. Heterogeneous integration—where separately manufactured chips and chiplets (sub-processing units) are assembled into a single package in various ways—is an alternative.

Components having different functions can be built and optimized using the most appropriate technologies, and then combined into a unified circuit.

- *Heterogeneous and Chiplet Integration Using Organic Interposer*, S-P. Jeng et al, TSMC
- *Hybrid Substrates for Chiplet Design and Heterogeneous Integration Packaging*, J. Lau et al, Unimicron Technology
- *Advanced System-in-Package Enabled by Wafer-Level Heterogeneous Integration of Chiplets*, S. Bhattacharya et al, A*Star
- *Advanced Package FAB Solutions (APFS) for Chiplet Integration*, S.W. Yoon, Samsung
- *Advanced Substrate Packaging Technologies for Enabling Heterogeneous Integration (HI) Applications*, G. Duan et al, Intel
- *Advanced Packaging Technology Platforms for Chiplets and Heterogeneous Integration*, L. Cao, ASE

DNA Digital Data Storage, Transistor-Based DNA Sequencing, and Bio-Computing

This Focus Session will feature papers at the intersection of computer science and biology. Some will explore the intriguing possibility of using DNA molecules as a potential data storage medium, because of DNA's extremely high density. Others will describe experimental nano-scale biosensors and related devices, which may lead to novel life-science technologies.

- *Bacterial Nanopores Open the Future of Data Storage*, M. Dal Peraro et al, EPFL
- *DNA Storage: Synthesis and Sequencing Semiconductor Technologies*, D. Lavenier, Univ. Rennes
- *Wafer-Scale Biologically Sensitive Carbon Nanotube FETs: from Fabrication to Clinical Applications*, Z, Zhang et al, Peking University
- *System Design Considerations for Automated Digital Data Storage in DNA*, C. Takahashi, Univ. Washington
- *Single-Molecule Field-Effect Transistors: Carbon Nanotube Devices for Temporally Encoded Biosensing*, K. Shepard et al, Columbia Univ.
- *Advances in Electronic Nano-Biosensors and New Frontiers in Bioengineering*, R. Bashir et al, Univ. Illinois Urbana-Champaign/Gachon Univ./Korea Univ./ Univ. California Irvine/Univ. Texas Austin
- *The Nanopore-FET as a High-Throughput Barcode Molecule Reader for Single-Molecule Omics and Read-Out of DNA Digital Data Storage*, P. Van Dorpe et al, IMEC/KU Leuven

Emerging Implantable-Device Technology

Researchers are investigating the use of advanced electronic technologies for new and improved implantable medical devices, in order to monitor and predict brain activity, to biodegrade after use, and for other purposes.

- *Soft Wireless Optogenetic and Hybrid Implants for Advanced Neural Interfacing*, J-W Jeong, KAIST
- *Biodegradable Implantable Microsystems*, J. Brugger et al, EPFL
- *Bilayer-Nanomesh Transparent Neuroelectrodes on 10μm-Thick PDMS*, J. Ryu et al, Dartmouth College/Northeastern Univ.
- *Channels, Layout and Size Scalability of Implantable CMOS-Based Multielectrode Array Probes*, L. Berdondini et al, Italian Institute of Technology
- *The Future of Holistic Neural Interfaces: 2D Materials, Neuromorphic Computing, and Computational Co-Design*, D. Kuzum et al, Univ. California San Diego
- *Optogenetic Neural Probes: Fiberless, High-Density, Artifact-Free Neuromodulation,* E. Yoon, Univ. Michigan
- *A Transient, Closed-Loop Network of Wireless, Body-Integrated Devices for Autonomous Electrotherapy*, J. Rogers, Northwestern Univ.
- *Increasing the Lifetime of Implantable Neural Devices*, S. Negi et al, Blackrock NeuroTech/Univ. Texas Dallas

Quantum Information and Sensing

Quantum sensing is the idea that sensors based on the properties of quantum mechanics (e.g., entanglement, coherence, tunneling, etc.) could be used to measure physical, electrical, magnetic, light and other quantities in ways that aren't possible otherwise. This may enable new technologies and ways of doing things, and papers in this Focus Session will discuss the fundamental work taking place to make various types of quantum sensors possible.

- *Hybrid-Magnon Quantum Devices: Strategies and Approaches*, A. Hoffmann, Univ. Illinois Urbana-Champaign
- *Josephson Parametric Amplifiers for Rapid, High-Fidelity Measurement of Solid-State Qubits*, S. Shankar, Univ. Texas at Austin
- *Potential of Diamond Solid-State Quantum Sensors*, M. Hatano et al, Tokyo Institute of Technology
- *Rare Earth-Based Solid-State Qubit Platforms*, S. Guha et al, Univ. Chicago/Argonne National Laboratory/MIT
- *Spin Qubits in Silicon FinFET Devices*, S. Paredes et al, IBM/Univ. Basel
- *Towards Topological Superconducting Qubits*, J. Shabani et al, New York Univ.

Special Topics in Non-von Neumann Computing

Most computers are based on a so-called von Neumann architecture, named after computer pioneer John von Neumann, where a processor stores and fetches data from separate memory circuits, accessed with various input/output interfaces.

With today's much faster processing speeds and denser chips, the inability of a processor to access memory quickly enough and at low power is becoming a serious limitation. Papers in this Focus Session will explore various ways to get around the "von Neumann bottleneck."

- *Analog Compute-in-Memory For AI Edge Inference*, D. Fick, Mythic
- *Subthreshold Operation of SONOS Analog Memory to Enable Accurate Low-Power Neural Network Inference*, S. Agrawal et al, Infineon/Sandia National Labs
- *Multistable Neuromorphic Computing: Controlling Attractor Switches Using Waveforms*, J. Chang et al, Univ. Texas at Austin
- *Life is Probabilistic - Why Should All Our Computers Be Deterministic? Computing with p-Bits: Ising Solvers and Beyond*, B. Behin-Aein et al, Ludwig Computing
- *Energy-Efficient Activity-Driven Computing Architectures for Edge Intelligence*, S-C Liu et al, Univ. Zurich
- *Training-to-Learn with Memristive Devices*, E. Neftci et al, Peter Grunberg Institute
- *Ferroelectric FET Configurable Memory Arrays and Their Applications*, S. X. Hu et al, Notre Dame/ De La Salle Univ. /Univ. South Florida
- *Scalable In-Memory Computing Architectures for Sparse Matrix Multiplication*, J. Kendall et al, Rain Neuromorphics/Univ. Florida/Sandia National Laboratory

Visit https://www.ieee-iedm.org/registration-overview to register for IEDM 2022. The deadline for early registration rates is 22 November 2022.

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7th IEEE Electron Devices Technology and Manufacturing (EDTM) Conference

7–10 March 2023/COEX, Seoul, Korea
https://ewh.ieee.org/conf/edtm/2023/

The 7th IEEE Electron Devices Technology and Manufacturing Conference (EDTM 2023) is a full four-day conference to be held in Seoul, Korea. EDTM is a premium conference sponsored by the IEEE Electron Devices Society that provides a unique forum to discuss and collaborate on a broad range of device/manufacturing—related topical areas including materials, processes, devices, packaging, modeling, reliability, and manufacturing and yield. The 7th EDTM will be held with the main theme: "Strengthen the global semiconductor research collaboration beyond the COVID-19 pandemic era."

The **Plenary** speakers include Dr. Suman Datta (Georgia Tech), Dr. Seon Yong Cha (SK Hynix), Dr. Jong Myeong Lee (Samsung Electronics), and Dr. Michael Lercel (ASML).

Technical Sessions

The EDTM 2023 solicits papers in all types of exploratory device concepts within the following broad technical areas:

- Materials
- Process, Tools, Yield, and Manufacturing
- Semiconductor Devices
- Memory Technologies
- Photonics, Imaging and Display
- Power and Energy Devices
- Modeling and Simulation
- Reliability
- Packaging and Heterogeneous Integration
- Sensor, MEMS, Bio-Electronics
- Flexible and Wearable Electronics
- Nanotechnologies
- Disruptive Technologies - IoT, AI/ML, Neuromorphic & Quantum Computing

Publications

Submitted papers will be subjected to IEEE standard review processes and publishing guidelines, as well as EDTM 2023 review criteria. The accepted and presented papers will be included in the EDTM 2023 Proceedings (Camera-Ready at submission and to be published AS IS if accepted), which will be published in IEEE Xplore. The authors of selected high-impact papers will be invited to submit extended versions for possible publication in the Special Issue on EDTM 2023 in *IEEE Journal of Electron Devices Society* (J-EDS), subjected to J-EDS author guidelines, and standard IEEE review and publication policy.

Short Courses and Tutorials

EDTM 2023 will start with a set of short courses and tutorials on 7 March 2023. Tutorials teach selected topics from the basics to the state-of-the-art, allowing the attendees to catch up on a topic quickly. Short Courses discuss the latest research and challenges on hot and advanced topics encompassing the EDTM 2023 theme. EDTM 2023 will offer 3 Short Courses on advances in manufacturing and processing

technologies, CMOS Image Sensor technology, power and energy devices, and 3 Tutorials on innovation technology for advanced semiconductor manufacturing, a new paradigm for high-efficiency computing, packaging, and heterogeneous integration.

Important Dates
Paper Submission Deadline:
24 October 2022
Notification of Acceptance:
23 December 2022 (tentative)
Early Registration Deadline:
10 February 2023 (tentative)

On behalf of the EDTM 2023 Organizing Committee, we invite you to join us in Seoul.

Miso Kim
EDTM 2023 Publicity Chair

2023 IEEE International Reliability Physics Symposium (IRPS)

The IEEE International Reliability Physics Symposium (IRPS) is the world's premier forum for leading-edge research addressing developments in the Reliability Physics of devices, materials, circuits, and products used in the electronics industry. IRPS is the conference where emerging reliability physics challenges and practical solutions to achieve realistic end-of-life projections and mitigation are first discussed.

In 2023, the IRPS will be held on 26-30 March at the Hilton, Monterey, California. Over the course of the conference, IRPS will offer a blended mix of keynote talks, tutorials, year-in-reviews, workshops, vendor exhibits, and technical presentations. **Abstracts are due by 24 October 2022. Late breaking news submissions are welcome by 23 January 2023.**

The IRPS draws presentations and attendees from industry, academia and governmental agencies worldwide. No other meeting presents as much leading work in so many different areas of reliability of electronic devices, encompassing silicon device, non-silicon device, process technology, nanotechnology, optoelectronics, photovoltaic, MEMS technology, circuits and systems reliability including packaging. IRPS 2023 is soliciting increased participation in the following areas: Embedded/In-product memory/neuromorphic compute, GAA, nanosheet, RibbonFET™ , Forksheets, 3D IC advanced packaging.

IRPS 2023 will be kicked off by keynote presentations from reliability experts at Intel, AMD, and Ampere covering the latest reliability trends and mitigation approaches from various industry perspectives.

Further opportunities at the symposium include:

- **Tutorial Program**. The IRPS tutorial program is a comprehensive event designed to help both the new engineers and experienced researchers. The program contains both beginner and expert tracks and is broken down into topic areas that allow the attendee to participate in tutorials relevant to their work with minimal conflicts between subject areas.
- **Year-in-Review Session**. These seminars provide a summary of the most significant developments in the reliability community over the past year. This serves as a convenient, single-source of information for attendees to keep current with the recent reliability literature. Industry and academic experts serve as the "tour guides" and save you time by collecting and summarizing this information to bring you up to

Ann Kelleher
Executive Vice President and General Manager of Technology Development, Intel

Mark Fuselier
Senior Vice President, Technology & Product Engineering, AMD

Rohit Vidwans
Executive Vice President and Chief Engineering & Manufacturing Officer, Ampere

date in a particular area as efficiently as possible.

- **Poster Reception**. The poster session provides an additional opportunity for authors to present their original research. The setting is informal and allows for easy discussion between authors and other attendees.
- **Workshops**. These workshops enhance the symposium by providing the attendees an opportunity to meet in informal groups to discuss key reliability physics topics with the guidance of experienced moderators. Some of the workshop topics are directly coupled to the technical program to provide a venue for more discussion on the topic.
- **Vendor Exhibits**. Held in parallel with the technical sessions, the equipment demonstrations provide a forum for manufacturers of state-of-the-art laboratory equipment to present their products. Attendees are encouraged to visit the manufacturers' booths for information and demonstrations.
- **IRPS Paper Awards**. IRPS bestows awards for Best Paper, Best Student Paper, Best Posters, and People's Choice.
- **IEW Co-Location**. In 2023, the IRPS will be co-located with the International ESD Workshop (IEW). Now in its 16th year, the IEW provides a relaxed, invigorating atmosphere to present new work and engage in discussions about the latest issues confronting the ElectroStatic Discharge (ESD) and Electrostatic OverStress (EOS) communities.

For the call for papers and other information, visit the IRPS 2023 home page at www.irps.org or join the IRPS linked-in group.

The IRPS committee members look forward to seeing you in Monterey, California!

Chris Conner
2023 IRPS General Chair
Intel

Paula Chen
2023 IRPS Publicity Chair
AMD

24th International Vacuum Electronics Conference (IVEC 2023)

On behalf of the IVEC 2023 Organizing Committee, we are pleased to announce that the Twenty-Fourth International Vacuum Electronics Conference (IVEC 2023), organized and sponsored by the University of Electronic Science and Technology of China (UESTC) with the technical co-sponsorship of the IEEE Electron Devices Society (EDS), will be held on-site in Chengdu, Sichuan Province, China, on 25–28 April 2023. Chengdu is known as the hometown of pandas, and we sincerely expect all attendees to fully interact with each other while immersing themselves in the natural beauty of Southwest China.

IVEC 2023 aims at being an international forum of information and technical discussion among various players in the fields of vacuum electronics: designers, researchers, young and experienced engineers, scientists, device users, manufacturers, operators, government/institutions, academics and of course, our valuable students.

We invite you to submit papers with the results of your latest work and experiences in the field of vacuum electronics. Submissions from all groups are highly encouraged and appreciated. IVEC 2023 strives to provide a unique platform for exchanging scientific and technical information and foster collaboration and cooperation in the vacuum electronics domain at Asian and global levels.

IVEC 2023 will focus on the Development of Vacuum Electronics for Requirements of the 21st Century as the conference theme. A special highlight of IVEC 2023 will be the introduction of Generalized Vacuum Electronics, which will try to extend the electron radiation from traditional vacuum to solid-state materials, as well as combine vacuum technology with the semiconductor technology. IVEC 2023 is the ideal forum to present and discuss the promising research from this field with the wider vacuum electronics community.

The John R. Pierce Award for Excellence in Vacuum Electronics, the Vacuum Electronics Young Scientist Award and the Best Student Paper Award will be presented.

For more details and the most up-to-date information, please visit the conference website at https://ivec2023.org.

We hope to see you all in Chengdu or online for IVEC 2023.

Yubin Gong
IVEC 2023 Chair
University of Electronic Science and Technology of China
ivec2023@ivec2023.org

Society News

EDS Strategic Planning

As you may know, the Strategic Planning Workshop was completed in June and I am very pleased to announce that it successfully completed its charter. There is now a Strategic Plan proposal which will be presented to the EDS Board of Governors and Forum for adoption. The Plan has five major components. In this article I would like to share the first three components with you. The Mission and Vision are the ones with which you are familiar. They have been on EDS website for quite some time. The Workshop delegates affirmed these with no major changes.

Mission
To foster professional growth of its members by satisfying their needs for easy access to and exchange of technical information, publishing, education, and technical recognition while enhancing public visibility in the field of Electron Devices.

Vision
Promoting excellence in the field of electron devices for the benefit of humanity.

The third component consists of five adjectives which describe the EDS Core Values. It was proposed by the EDS Executive Committee and adopted by the delegates. They articulate the human values of the Society as lived today and endure but which are distinct from what it aspires to be. They describe what anyone should expect who interacts with us and when we interact with each other.

Core Values
- trustworthy.....we are honest and transparent; we keep our word
- respectful.....we are civil, courteous and polite in our actions and discourse
- inclusive.....we seek full engagement from all members; we exclude no one; there are no ranks
- ethical.....we do nothing to harm individuals or the environment; we follow the law
- open.....we are listen to new ideas; we are aware of and adapt to change

The Strategic Plan is a dynamic plan which thrives when all members live its core values and participate in the realization of its vision and mission. Your role in this is vital. That is why I am calling on you to exemplify our core values in your professional life and to engage in a dialog with us about what the Society can do for you and what you can do to make our vision and mission come to life.

We need your feedback. You are the important ingredient for making this successful. Please go to: https://ieee-collabratec.ieee.org/app/workspaces/8209/Electron-Devices-Society-Strategic-Plan/activities. You can log on with your IEEE credentials or simply register as a Collabratec user at no cost. Do it today.

Doug Verret
Strategic Directions Committee
Vice President

Message from EDS Newsletter Editor-in-Chief

Daniel Tomaszewski
EDS Newsletter
Editor-in-Chief

Dear Readers, Members of the IEEE EDS Community,

Welcome to the IEEE EDS Newsletter issue October 2022. Let me briefly introduce to you the contents.

The Society News section brings you this time an interesting report by Monica Blank, Chair of EDS Vacuum Electronics Technical Committee. The article is illustrated by an exceptional picture of just how large electron devices are in the field of interest of the Society.

We continue the series of articles celebrating the 75th Anniversary of Transistor. In this issue, Prof. John D. Cressler overviews developments of the SiGe HBTs, and Prof. Dan Fleetwood highlights Radiation Effects in scaled MOS Devices.

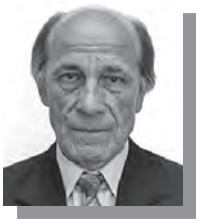
In the Technical Briefs section we offer a summary of the 2022 IEEE VLSI Symposium on Technology & Circuits, fully combined as a single event. Moreover, in Regional News we present short reports on recent editions of the International Memory

Workshop and Latin America Electron Devices Conference. What concerns the future, we present in the Upcoming Technical Meetings section the last update on IEEE International Electron Devices Meeting, and the advertisements of IEEE Electron Devices Technology and Manufacturing Conference, International Vacuum Electronics Conference, and International Reliability Physics Symposium. The upcoming editions of IEEE Workshop on Wide Bandgap Power Devices & Applications, International Memory Workshop, International Symposium on Power Semiconductor Devices and ICs are announced in Regional News.

In the Women in Engineering section, please find the article by Prof. Dragica Vasileska who presents her career as a researcher and teacher in the area of computational electronics. The Young Professionals section contains an interesting article by Prof. Paul Berger who tells us how he has used the IEEE Collabratec platform for mentoring young people starting or willing to start their professional careers in the Electron Devices discipline. Based on his own positive experience, Paul encourages experienced members of the Society to try sharing their own experience and expertise with young people. It is a key message of this article.

Further parts of this Newsletter issue include news on technical, societal and humanitarian activities led by the Chapters in Regions 2, 8, 9, and 10. At this point, I would like to welcome in our Newsletter the IIITDM-Kancheepuram, ED15 Student Branch Chapter. This SBC was established very recently and now reports its first activities. Congratulations to the Chapter members, the Branch Advisor Dr. Pradhan and Chair Mr. Chandrasekar!

Mykhaylo Andriychuk



After a short presentation of the Newsletter content I would like to introduce to you Mykhaylo Andriychuk (IEEE M'95, SM'03) who has been appointed as the EDS Newsletter Regional Editor for Region 8 - Eastern Europe after Kateryna Arkhypova's stepping down from this position. We, the whole EDS Newsletter Editorial Team, are grateful to her for dedication in voluntary work for EDS and wish her dreams come true. Dr. Andriychuk has been employed by the Pidstryhach Institute for Applied Problems of Mechanics and Mathematics (IAPMM), Lviv, Ukraine, for more than 40 years. Currently, he is the Head of Department of the Numerical Methods in Mathematical Physics. He also holds a position of professor at the National University "Lviv Polytechnic", Lviv, Ukraine. His professional performance includes more than 180 papers in the scientific journals and international conference proceedings, which concern the diffraction and antenna synthesis theory, optimization methods and nonlinear integral and matrix equations. Dr. Andriychuk served for a long time as the IEEE Ukraine Section (West) MTT/ED/AP/EP/SSC Societies Joint Chapter Chairman. That time, the Chapter won the IEEE Antennas and Propagation, Electron Devices, and Microwave Theory and Techniques Societies Outstanding Chapter of the Year Awards. We are very glad to welcome Mykhaylo in our team and we wish him fruitful work for the EDS Newsletter.

Dear Readers, if you have any suggestions, comments regarding the Newsletter contents, please do not hesitate to contact us. We will be very glad to receive your feedback. Interesting views will be presented with the consent of the authors, along with our replies in the Letters to Editors section.

Sincerely,
Daniel Tomaszewski

EDS Vacuum Electronics Technical Committee Report

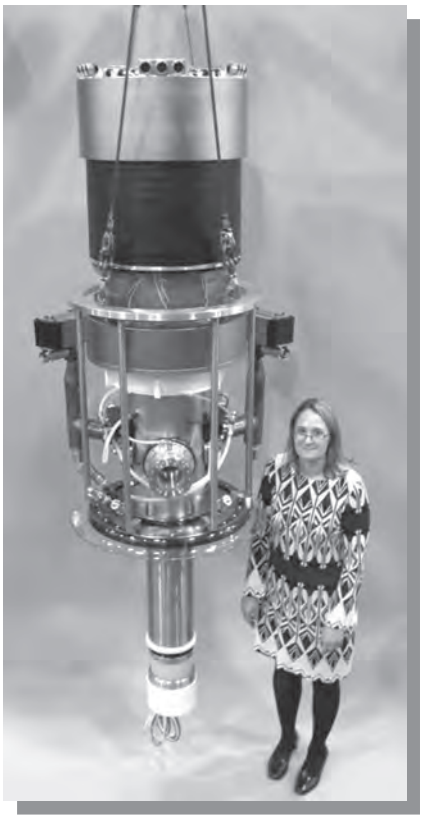
The EDS Vacuum Electronics Technical Committee (VETC) was formed more than 20 years ago to represent the vacuum electron device community within EDS. The Committee has 11 members and 15 corresponding members, all of whom are world-recognized experts in one or more technical disciplines related to vacuum electronics. In addition to overseeing the International Vacuum Electronics Conference (IVEC) and supporting EDS journals, the Committee works to promote and foster emerging technologies, new applications, and cutting-edge research in the broad field of vacuum electronics. With the Committee members from the academia, industry, and government labs in Asia, Europe, and North America, the VETC seeks to represent and advocate for the worldwide vacuum electronics community.

The dynamic, challenging, multidisciplinary field of vacuum electronics represented by the Committee continues to advance, evolve, and grow. Scientists and engineers working in the field of vacuum electronics seek to develop and exploit the most up-to-date technology, design tools, and design techniques to continuously advance the state-of-the-art. As applications require vacuum electronic devices with progressively

better performance, including higher power, higher frequencies, broader bandwidths, higher gains, and longer lifetimes, the Committee actively promotes the research and development to ensure that the technology continues to meet ever growing application demands.

The VETC is also responsible for selecting yearly winners of the John R. Pierce Award for Excellence in Vacuum Electronics as well as the Vacuum Electronics Young Scientist (VEYS) Award. Each year, these two awards are presented at IVEC, where the winners have the opportunity to deliver plenary addresses. The 2022 Pierce Award Winner, Dr. Keishi Sakamoto from Kyoto Fusioneering, gave at IVEC 2022 an enthusiastic and inspiring plenary address on how the continuous wave gyrotrons performance improvements at the megawatt power level, have moved electron cyclotron resonance heating from a lesser role to the main heating method for ITER and other groundbreaking fusion machines. The 2022 VEYS Award winner, Dr. Diana Gamzina from SLAC and Elve, delivered a career retrospective talk highlighting the most impressive of her numerous technical accomplishments as well as her establishment and oversight of the SLAC Accelerating Girls' Engagement in STEM (SAGE-S) program. Please join the VETC in congratulating Dr. Sakamoto and Dr. Gamzina, two extremely accomplished and deserving award winners, who represent the best our field has to offer.

Last year, the Committee's main areas of focus were the successfully concluded IVEC 2022, the upcoming IVEC 2023, a special issue of the IEEE Transactions on Electron Devices, and an updated technical Committee website. IVEC 2022, the first hybrid in-person and online meeting in the IVEC series, was held in Monterey, CA, in April under the guidance of Dr. Jack Tucek of Northrop Grumman Corporation, the General Chair, and Technical Program Chair Dr. Max Mankin of Modern Electron Corporation. The meeting was comprised of 257 invited and contributed papers, 6 plenary and award talks, and a very well-received mini course with lectures on the basics of TWT amplifiers, additive manufacturing for vacuum electronics, thermionic converters, as well as ultrafast and ultra-small scale electron emission. Despite the inherent challenges of a hybrid meeting, the 23rd IVEC, along with the mini course, was a huge success, with higher than typical attendance and outstanding technical content.



Monica Blank, Chair of VETC, standing next to a 170 GHz, 1 MW power level gyrotron oscillator

Prof. Yubin Gong of UESTC, the general chair of IVEC 2023, and his co-chairs, Prof. Yirong Wu of AIR-CAS, Prof. Detian Li of LIP-CAST, and Prof. Jinjun Feng from BVERI, are well ahead in the planning process for next year's IVEC. The hybrid conference will take place from 25–28 April 2023, with the in-person component held in Chengdu, China. Details about the conference can be found at https://ivec2023.org. Please visit the conference website for the latest information about this exciting upcoming meeting. We hope to see all of you in Chengdu or online for IVEC 2023.

The VETC has also been focused on the upcoming Special Issue in the *IEEE Transactions on Electron Devices*, entitled "From Mega to Nano: Beyond One Century of Vacuum Electronics." The submission deadline for the Special Issue is October 31, 2022 and publication is planned for June 2023. All are invited to submit manuscripts to this timely and relevant Special Issue.

Details about the Special Issue of TED, the 2023 IVEC, the John R. Pierce and VEYS awards, and much more can be found at the newly updated Committee website, https://vacuumelectronics.org. We invite everyone to visit the website for all the latest news and information about the vibrant and exciting vacuum electronics community.

Monica Blank
Chair of EDS Vacuum Electronics Technical Committee

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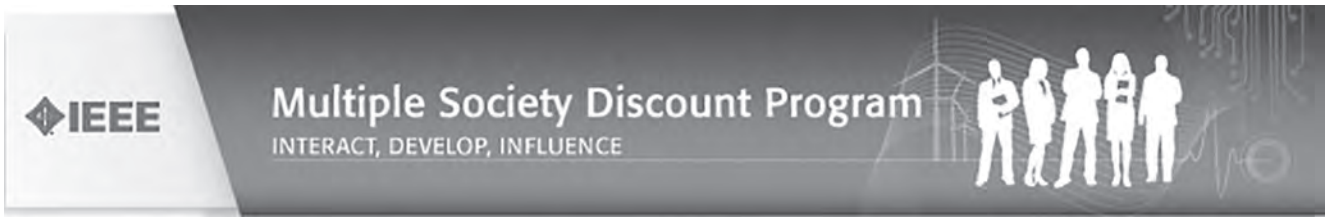
The IEEE Societies that complement the IEEE Electron Devices Society include IEEE Solid-State Circuits Society, IEEE Circuits and Systems Society, IEEE Photonics Society and IEEE Reliability Society.



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New lower student dues in developing nations and low-income economies will make undergraduate student membership more affordable and will be automatically priced for eligible students in these countries. NO promotion code is needed, but also, no other discounts or promotions can be applied in combination with the new lower dues. In developing nations, undergraduate student dues will be US$14. In low-income economies, dues will be US$5.

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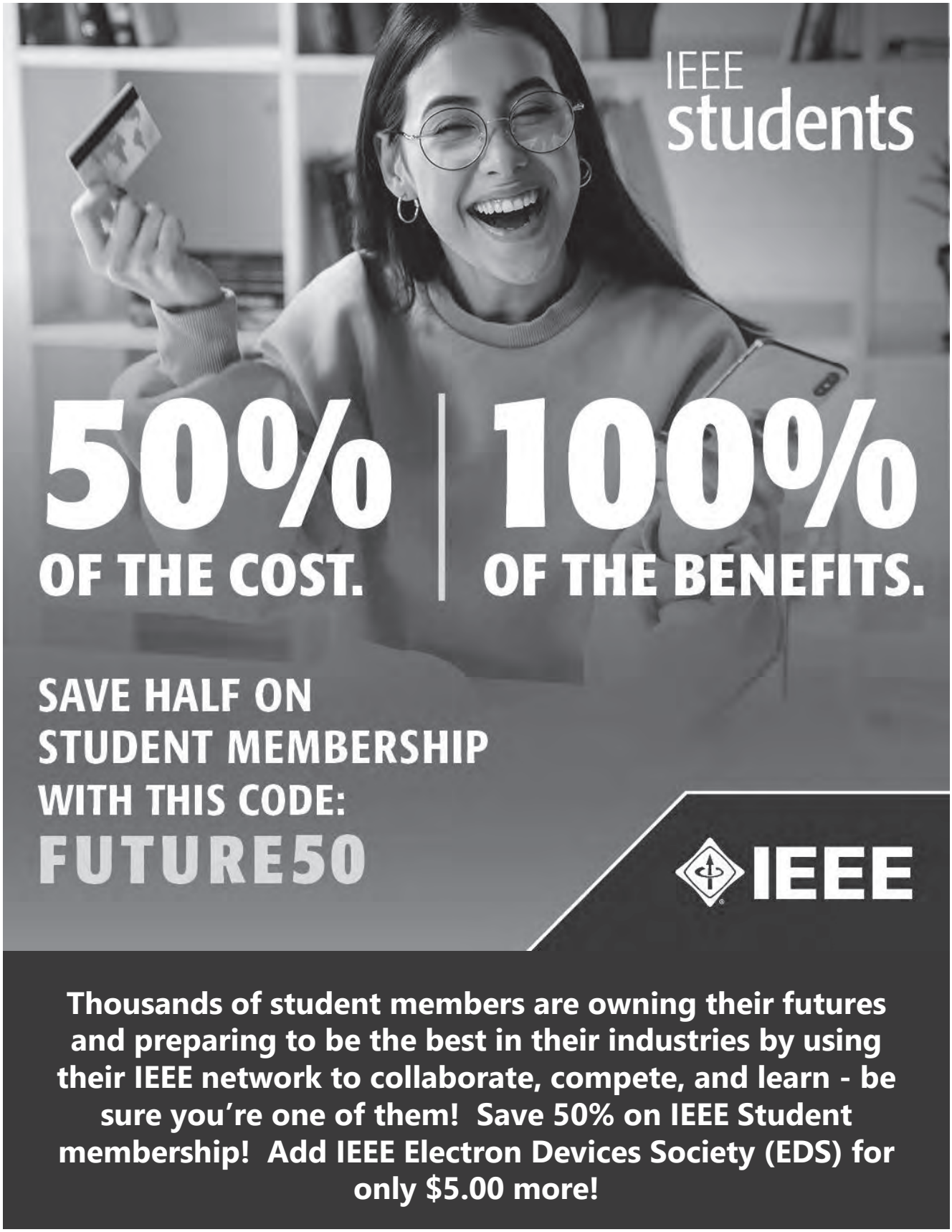
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2021 EDS Paul Rappaport Award

A high priority of the IEEE Electron Devices Society (EDS) is to recognize and enhance the quality of papers published in EDS archival literature. Every year, the Society confers its prestigious Paul Rappaport Award to the best paper published in the *IEEE Transactions on Electron Devices*. Among other criteria including technical excellence, an important metric for selection for the award is comprehensive and impartial referencing of prior art.

The winning paper was selected from over 1,027 articles that were published in 2021. The winning paper is entitled *"Monolithic Integration of Oxide Semiconductor FET and Ferroelectric Capacitor Enabled by Sn-Doped InGaZnO for 3-D Embedded RAM Application."* This paper was published in the December 2021 issue of the *IEEE Transactions on Electron Devices*, and was authored by Jixuan Wu, Fei Mo, Takuya Saraya, Toshiro Hiramoto, Hiroshi Goto and Masaharu Kobayashi.

The award will be presented during the IEEE International Electron Devices Meeting to be held in December 2022. In addition to the award certificate, the authors will receive a check for $2,500 to be shared equally among all authors. On behalf of the IEEE Electron Devices Society, I would like to congratulate the authors for this achievement. Brief biographies of some of the authors follow.

Arokia Nathan
EDS Vice-President of Publications and Products

2021 EDS Leo Esaki Award

The EDS Leo Esaki Award was established in 2019 to recognize the best paper appearing in a fast turn around archival publication of the IEEE Electron Devices Society, targeted to the *IEEE Journal of the Electron Devices Society*.

The paper winning the 2021 Leo Esaki Award was selected from over 195 articles that were published in 2021. The paper is entitled, "*Utilization of Unsigned Inputs for NAND Flash Based Parallel and High-Density Synaptic Architecture in Binary Neural Networks*." This paper appeared in the November 2021 issue of the *IEEE Journal of the Electron Devices Society* and authored by Sung-Tae Lee, Gyuho Yeom, Joon Hwang, Hyeongsu Kim, Honam Yoo, Byung-Gook Park, and Jong-Ho Lee.

The award will be presented during the IEEE International Electron Devices Meeting to be held in December 2022. In addition to the award certificate, the authors will receive a check for $2,500 to be shared equally among all authors. On behalf of the IEEE Electron Devices Society, I would like to congratulate the authors for this achievement.

Arokia Nathan
EDS Vice-President of Publications and Products

2021 EDS George E. Smith Award

A high priority of the IEEE Electron Devices Society (EDS) is to recognize and enhance the quality of papers published in EDS archival literature. The EDS George E. Smith Award was established in 2002 to recognize the best paper appearing in a fast turnaround archival publication of EDS, targeted to the *IEEE Electron Device Letters*. Among other criteria including technical excellence, an important metric for selection for the award is comprehensive and impartial referencing of prior art.

The paper winning the 2021 EDS George E. Smith Award was selected from over 447 articles that were published in 2021. The paper is entitled, "*Demonstration of a p-type Ferroelectric FET with immediate read-after-write capability*." This paper appeared in the December 2021 issue of the *IEEE Electron Device Letters* and authored by Dominik Kleimaier, Halid Mulaosmanovic, Stefan Dunkel, Sven Beyer, Steven Soss, Stefan Slesazeck and Thomas Mikolajick.

The award will be presented during the IEEE International Electron Devices Meeting to be held in December 2022. In addition to the award certificate, the authors

will receive a check for $2,500 to be shared equally among all authors. On behalf of the IEEE Electron Devices Society, I would like to congratulate the authors for this achievement.

Arokia Nathan
EDS Vice-President of Publications and Products

EDS Members Named Recipients of 2022 IEEE Medals

Four EDS members were named 2022 IEEE Medal recipients. Please be sure to visit the IEEE website at https://corporate-awards.ieee.org/recipients/current-recipients/ to view all the award recipients.

Asad M. Madni
2022 IEEE Medal of Honor
"For pioneering contributions to the development and commercialization of innovative sensing and systems technologies, and for distinguished research leadership."

Anantha Chandrakasan
2022 IEEE Mildred Dresselhaus Medal
"For contributions to ultralow-power circuits and systems, and for leadership in academia and advancing diversity in the profession."

Ingo Wolff
2022 IEEE/RSE James Clerk Maxwell Medal
"For the development of numerical electromagnetic field analysis techniques to design advanced mobile and satellite communication systems."

Umesh K. Mishra
2022 IEEE Jun-ichi Nishizawa Medal
"For contributions to the development of gallium nitride-based electronics."

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Mentoring

By Paul R. Berger, EDS Board of Governors ('19–'24)

Our EDS community is nearly 9000 strong, but our membership is drifting downwards each year as EDS members retire and are not being replaced by enough younger members, who are retained over their full career. Mentoring is a valuable tool for the most senior 3000 members to reach out to the most junior 3000 in order to mentor and life coach.

During my tenure as the seminal VP for Strategic Directions for EDS ('20–'21), we conducted a survey through IEEE Strategic Research of current and recently non-renewed EDS members of their opinions about EDS. One message that resonated with me is that younger members joined with high hopes and enthusiasm, but were met with a relatively quiet response of a self-administered, self-selected menu of choices. Granted our publications and conferences are extremely healthy and well run, but in 2022, this is not enough. I recall vividly that one member articulated in the comments section of that survey that they wanted to volunteer and get involved, but no one asked them.

Mentoring is a natural human trait. In our nuclear family, we may call it parenting, and in a former world where you begin and end your career at the same company, one may call it training. And in academia, we call it advising. But in 2022, engineers are likely to change jobs and move cities much more frequently. IEEE can play a significant role to mentor and recruit EDS members through mentoring, regardless of geolocation.

IEEE's Collabratec is an underutilized, but yet valuable tool. Many of us have a multitude of webpage profiles to maintain and monitor, such as LinkedIn, Google Scholar, Research Gate, Publons, as well as the social media of Facebook, Twitter, Instagram, etc. It can be overwhelming. So, adding yet another profile can be taxing in a hyper busy world. But IEEE Collabratec is a way to reach across time zones and borders to others in our community.

IEEE Collabratec has a mentoring feature, whereby any IEEE member can list themselves as a mentor. I personally have done this and responded to requests in two waves so far. The first wave, I tested the water with one student, who was from Chile. I was very pleasantly surprised to discover a very worldly, ambitious and aware individual, who simply needed to talk with someone senior to validate their career plans and goals. We probably spent more time trying to find a suitable time slot than we spent on the actual Zoom call. But they simply needed a lifeline and a life coach.

My experience was quite pleasant, so I accepted a second tranche of mentees. Some are still trying to connect up, but through this tranche, I also met with another student, currently in the Philippines. Again, I was gob smacked by their maturity and self-awareness. It was another very pleasant experience and only cost me a 1-hour Zoom call. In fact, anecdotally, I feel that the Collabratec platform has also imparted a filter that only the more enterprising students and YPs actually utilize this request, thereby shielding more senior members from wasted time and effort. I came away fulfilled and I believe each student has gained self-assurance as well as a connectivity to the IEEE community.

So, I call upon us all to establish your IEEE Collabratec profiles and reach out to our EDS Young Professionals and EDS Student Members to give them a lifeline to their future, and our future.

IEEE Collabratec USER GUIDE

About IEEE Collabratec, https://ieee-collabratec.ieee.org/

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Women in EDS and Computational Electronics

Dragica Vasileska, Professor of Electrical Engineering and IEEE Fellow
School of Electrical, Computer, and Energy Engineering
Arizona State University, Tempe, AZ, USA

Since I was a child, I have been interested in electrical circuits. I made my circuits successfully many times but also blew up several fuses in my parent's house. My favorite subject in primary and high school was physics. I was fascinated with nuclear physics and initially wanted it to be my major and professional focus in life. By the end of high school, I became more interested in practical applications of physics and decided to apply to the Faculty of Electrical Engineering and Information Technologies (FEEIT), University Ss Cyril and Methodius, Skopje, Republic of North Macedonia. I was extremely excited and motivated to become an engineer. I graduated in 1985 with the highest honors and the highest GPA ever since FEEIT was founded. After graduation, I was offered a Lecturer position. As the first woman ever hired in the FEEIT Electronics group, I accepted without reservation. I wanted to be a professor, to teach students how electrical circuits work, and to encourage young women to choose electrical engineering as a career.

In December 1990, I moved with my husband to the United States, where we were accepted into the Ph.D. program at Arizona State University (ASU). To me, the concept of a centralized campus was fascinatingly different from how most universities are situated in Europe. For example, while working on my master's degree in North Macedonia, I often struggled to get a publication that I really needed for my research. It was those times before the internet revolution, so access to literature was very difficult. In contrast, at ASU, I could spend days and nights at Noble Science Library. Everything was within reach: books, periodicals, journal papers…. It was like Disneyland to me. Once my Mom asked me why I wanted to stay in the United States, I pointed her to the Noble Science Library.

I was fortunate to have Prof. David Ferry as a Ph.D. advisor. I learned from him about semiclassical and quantum transport. I also developed an interest in modeling and simulation, which nowadays is recognized as a third mode of investigation, in addition to theory and experiments. The greatest joy of anybody developing simulation software is when you discover a bug in your program, sometimes while asleep. I was fascinated with Richard Feynman's contributions to quantum physics and carefully read his lectures on physics. I was also fascinated with his charisma and read numerous non-scientific books authored by him, such as "The pleasure of finding things out." I decided to make my Ph.D. dissertation work in quantum field theory. I was among the first to apply the near-equilibrium Green's function formalism to modeling low-dimensional systems such as silicon inversion layers and to investigate the impact of collisional broadening of the states on the electron density of states function and electron mobility [1]. Prof. David Ferry made it possible that, while being a poor Ph.D. student at ASU, I attended many scientific conferences and met scientists that I admire, such as Karl Hess from the University of Illinois at Urbana Champaign (UIUC).

After graduation, I spent two years as a post-doc at the Center for Solid-State Electronics Research at ASU (1995–1997). The focus of my research was modeling discrete impurity effects in nanoscale transistors that gave rise to fluctuations in device parameters, such as the threshold voltage (Figure 1), of devices fabricated on the same wafer. Our group pioneered the real-space molecular dynamics treatment of electron-electron and electron-ion interactions within particle-based device simulators in 1999 [2]. We were also among the first to develop a 3D Schrödinger-Poisson solver to model electrostatics in quantum dots.

After being a post-doc for two years, it was time for a real job, and my heart was set on academia. Although there were a lot of research opportunities in industry and in the national research laboratories, they all lacked one key component: the rewarding interaction with students. I strongly believe that helping students to think clearly, to reason logically, to be both imaginative and curious, regardless of their level of knowledge, is essential to society's and our own future development. In August 1997, I was offered an Assistant Professor position at ASU, which became my permanent home. I still enjoy being in Arizona and teaching and doing research at ASU. It was difficult at times to be a young faculty, teach new subjects, prepare lecture notes for classes, guide graduate and undergraduate students, and at the same

time work on research projects and proposals to secure funding, but it was worth the effort. Seeing students start from knowing virtually nothing and grow into successful researchers is a privilege, and I enjoy it. The hard work paid off, and in 1998 I won the National Science Foundation (NSF) CAREER award, which strengthened my position at ASU. Afterward, I won many grants from NSF, Office of Naval Research (ONR), Semiconductor Research Corporation (SRC), and others related to semiconductor device modeling.

It was at the Computational Electronics Conference in Osaka, Japan (1998), when Prof. Mark Lundstrom (Purdue University) and Prof. Umberto Ravioli (UIUC) introduced the idea of developing a platform for dissemination of tools to non-experts in modeling and simulation. I immediately bought-in to their idea and suggested my Schred [3] tool. Schred is a tool to calculate quantum-mechanically the electron density and the subband energies in silicon inversion layers (MOS Capacitors). It considers the quantum-mechanical size quantization effects that manifest as bandgap widening and an increase in the average displacement of the carriers from the semiconductor oxide interface. This, in turn, degrades the device transconductance of a MOSFET. In 1999 Schred was deployed on the Purdue University Network Computing Hubs (PUNCH), sponsored by NSF. PUNCH is the predecessor of nanoHub, an NSF-sponsored multi-institution science gateway for the dissemination of tools and educational materials worldwide. One of the firsts on nanoHUB, Schred remains among the most cited tools on the platform.

During my first sabbatical (Dec. 2005–Aug. 2006), in collaboration with Prof. Gerhard Klimeck's group, I ported the PN-junction lab based on the PADRE simulation software. MOSCAP, MOSFET, BJT, and MESFET labs followed in the same way. As a multi-institutional group, we introduced on nanoHub the concept of "tool-based curricula": a collection of tools and educational materials on a particular subject. Soon after, ABACUS (Assembly of Basic Applications for Coordinated Understanding of Semiconductors), AQME (Advancing Quantum Mechanics for Engineers), and ACUTE (Assembly for Computational Electronics) were released. Currently, I am the 3rd largest contributor to nanoHUB from over 2600 contributors from all over the world, and my educational materials served more than 7,000 users in 480 courses from 47 institutions. The usage statistics of my tools deployed on nanoHUB are shown in Figure 2.

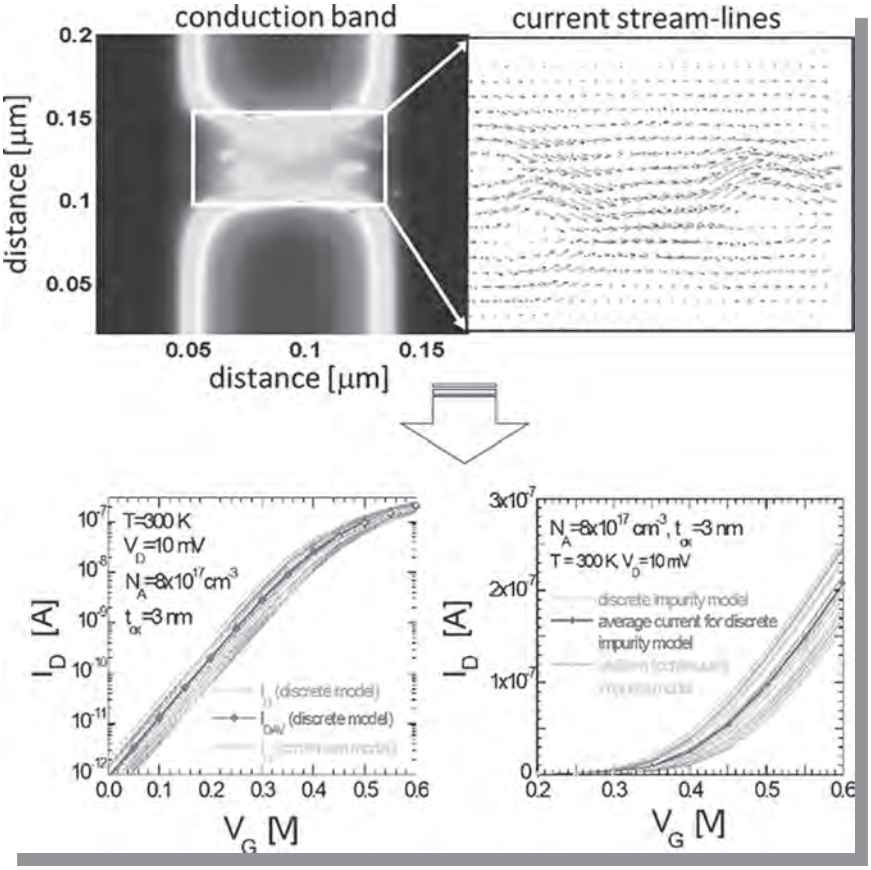

Figure 1. Fluctuations in the confining potential due to the discrete nature of the impurity atoms in the active channel region of the device (top left) that lead to non-uniform current flow (top right). The discrete nature and the different number and distribution of impurities in devices fabricated on the same wafer give rise to threshold voltage fluctuations (bottom).

At ASU, I continue to initiate collaborations with colleagues on topics related to semi-classical and quantum transport modeling. For example, in 2000, based on Feynman's and Kleinert's idea, Prof. David Ferry, introduced the concept of effective potential approach, which mimics the quantum-mechanical space-quantization effects in classical device simulators. The idea was immediately implemented in our in-house 2D Monte Carlo device simulator [4]. In 2008 my PhD student Katerina Raleva (now Professor at FEEIT) was the first to couple particle-based device simulators with energy balance solvers for the acoustic and the optical phonon baths [5], to study self-heating effects in nanoscale transistors as shown in Figure 3. (This work was done in collaboration with Prof. Stephen Goodnick from ASU). My long-time friend and colleague Mary Jo Rack (at that time Intel employee) used to say: "Our transistors are frying!" My postdoc Denis Mamaluy (now at Sandia National Lab) together with my

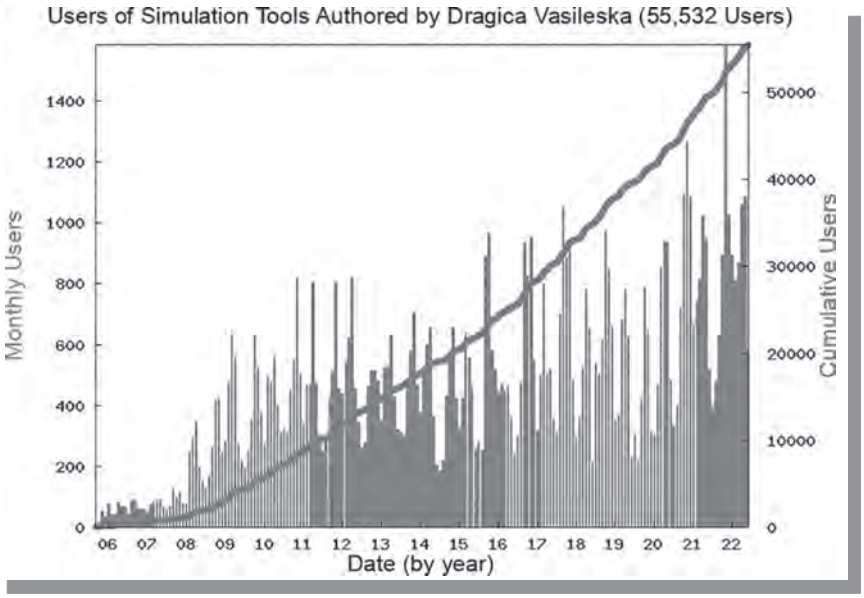

Figure 2. Cumulative User of tools authored by Prof. Vasileska residing on nanoHUB.org.

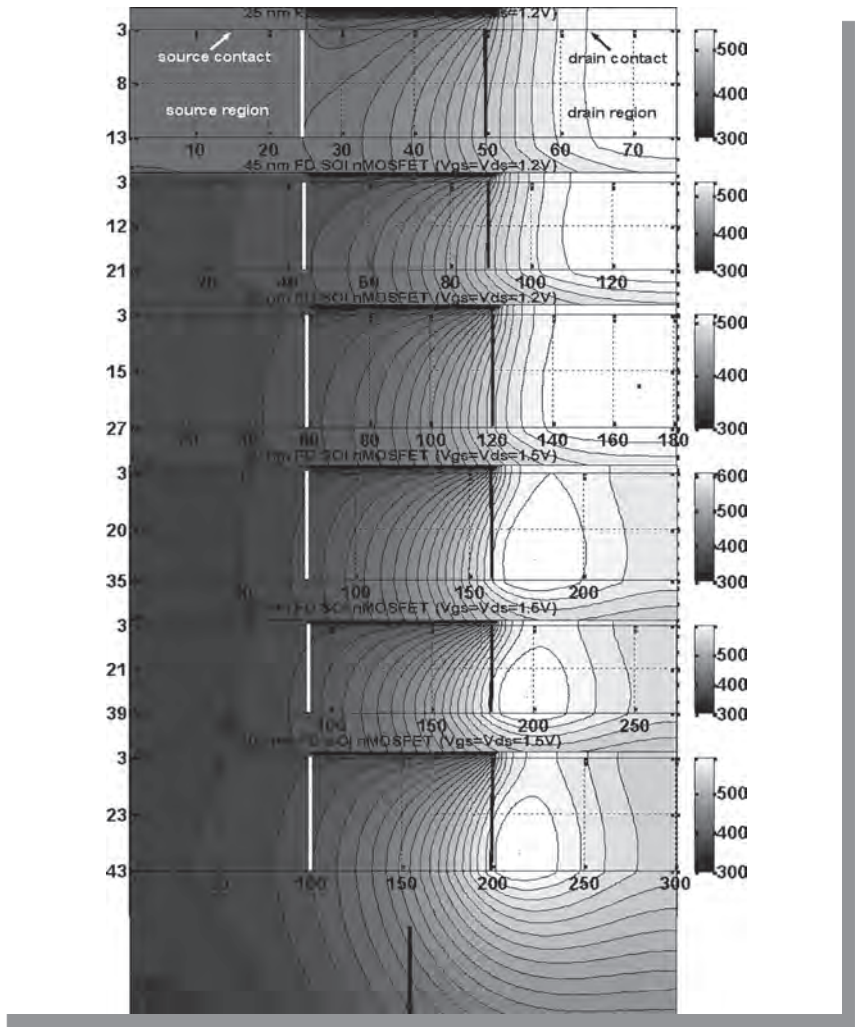

Figure 3. Self-heating in fully-depleted (FD) SOI devices. Here are the lattice temperature profiles for different technology generations in the thin silicon film of the device [6].

PhD student Hasanur Rahman Khan (now at Intel) developed the 3D Contact Block Reduction method in 2006 [6], which was the first tool to study ballistic transport in FinFETs. Several of my Ph.D. students chose careers in academia and the others chose in industry. They are all successful scientists and professionals, and I am proud of them.

I have many collaborations outside of ASU as well: the group of Prof. Peter Vogl at the Walter Schottky Institute in Munich; the group of Prof. Siegfried Selberrher at the Technical University in Vienna (including Prof. Hans Kosina and Mihail Nedjalkov) where I spent my second sabbatical (Sep. 2012 to Dec. 2012); Prof. Asen Asenov's and Prof. John Barker's groups at Glasgow University; and many others. In collaboration with Ben Kaczer and Eric Bury at IMEC, Katerina Raleva and I contributed to the extraction of test device hot-spot temperature using the heater-sensor approach [7] via numerical simulation and comparison with experiments. This collaboration spawned a focus on global thermal modeling in my group. Global thermal modeling is extremely important because the mean free path of phonons is much larger than the mean free path of electrons in silicon. This difference necessitates the use of a global thermal solver that accounts for heat dissipation through the interconnects and the package. My collaboration with Prof. Gilson Wirth and his team at Universidade Federal do Rio Grande do Sul (UFRGS), Porto Alegre, Brazil, spans years, working on random dopant and random telegraph noise fluctuations in nanoscale transistors.

A few years back, my research interests also included modeling the reliability and metastability of CdTe solar cells. This project was initiated by researchers from First Solar and was sponsored by two multi-university research grants from the U.S. Department of Energy (DOE), in which ASU was the lead. PVRD-FASP [8], a tool currently used at

First Solar, was developed by my Ph.D. student Abdul Rawoof Shaik (now at Samsung).

To me, there are many components to success in teaching. For example, a primary goal should be to bring students to a level of understanding that will allow them to independently analyze complicated physical problems. In today's world, engineers require not only technical expertise, but also self-confidence and maturity to implement their ideas and the ideas of others. I believe that it is our obligation to educate rather than train students, give them a strong mathematical foundation, introduce them to state of the art technology, and teach them to be effective team members. Since the designs of the future will need even greater use of computer tools for product development, I also think that we need to:

- Include this new mode of investigation in the undergraduate electrical engineering curricula along with the traditional theoretical and experimental methods, and
- Train graduate students to develop and use such tools with thorough understanding of the physical phenomena involved, so they can interpret the results of the computational simulations realistically and critically.

I equally enjoy teaching specialized graduate-level classes and undergraduate classes. Throughout my time at ASU, I have co/developed and taught numerous courses at undergraduate and graduate level. Sharing knowledge is, in my opinion, most important for the future development of science and technology. I have aggregated selections of my lecture notes, my research work, and the work of my students into three textbooks: *Computational Electronics* (with S. M. Goodnick, Morgan & Claypool publisher), *Computational Electronics: Semi-Classical and Quantum Transport Modeling* (with S. M. Goodnick and G. Klimeck, CRC Press), and *Modeling Self-Heating Effects in Nanoscale Devices* (with K. Raleva, A. Shaik, and S. M. Goodnick, Institute of Physics Publishing, Morgan & Claypool).

While at FEEIT and ASU, I have promoted the inclusion of women in engineering disciplines. For example, I was part of the WISE (Women in Science and Engineering) initiative at ASU for many years, teaching young girls (middle-school and high-school) Boolean algebra and how to make a motor using wire, a battery, magnets, and rubber bands. I enjoyed every moment spent with these young and enthusiastic girls and hoped they became motivated to choose electrical engineering. Women CAN succeed in male-dominated disciplines and become successful professionals in their respective fields. I will continue to introduce women to computational electronics at the undergraduate and graduate levels. I will recruit women into my research activities. Of my 19 PhD and 30 MS students, 4 were women.

I hope that many young women will follow my example and be more successful in the electrical engineering discipline.

Dragica Vasileska ('F2019) is a Professor of Electrical Engineering at Arizona State University She received B.S.E.E. and M.S.E.E. Degree from the University Ss. Cyril and Methodius (Skopje, Republic of North Macedonia) in 1985 and 1991, respectively, and a Ph.D. Degree from Arizona State University in 1995. Her research interests include semiconductor device physics and semiconductor device modeling, with strong emphasis on quantum transport and Monte Carlo device simulations. Recently, her research interests also include modeling metastability and reliability of solar cells. Prof. Vasileska published in prestigious scientific journals, and conference proceedings, has given numerous invited talks and is a co-author of three books and an editor of two books. Prof. Vasileska is a recipient of the 1998 NSF CAREER Award. Her students have won numerous awards at prestigious international scientific conferences.

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IEEE EDS SHE in ECE Event

A report by Prof. Durga Misra

On 22 July 2022, a "One-Day Summer Camp for Female High School Students", was hosted at NJIT from 8:30 AM to 3:30 PM, to encourage female students to join engineering, especially in electrical engineering and computer engineering. The theme was "Soaring High-powered Excellence" i.e., SHE in IEEE and SHE in Electrical and Computer Engineering (ECE).

More than 75 girls entering 9th to 12th grades from the local high schools attended the event, which included several minority students. Students were welcomed by Prof. Durga Misra, Chapter Chair of EDS/CASS Chapter of North Jersey Section. He emphasized the financial sponsorship of IEEE Electron Devices Society and IEEE Circuits and Systems Society.

The morning panel session included the faculty panel, industry panel and student panel, in addition to a hands-on activity by the girls. The faculty panelists were Prof. Xuan Liu of ECE, Prof. Ratna Raj of ECE and Prof. Janice Daniels, Associate Dean for Research in Newark College of Engineering. The faculty panel moderated by Ms. Ryoko Mathes advised the students on Career Development.

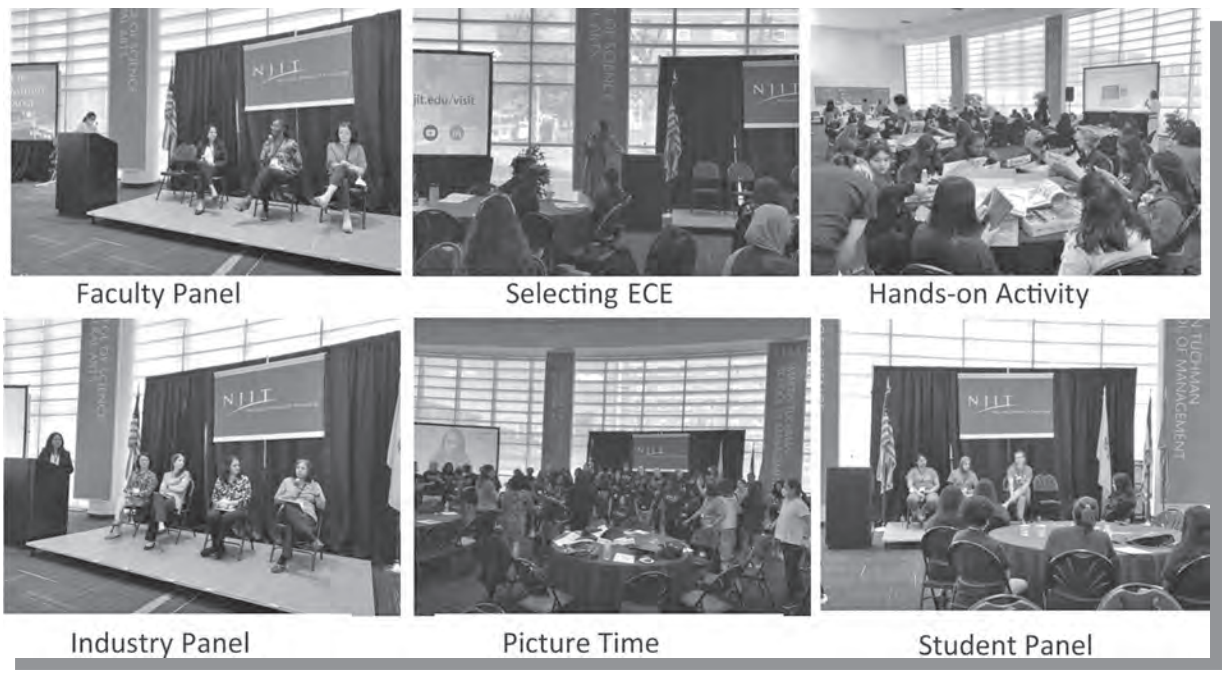
The industry panelists were Ms. Chitra Venkatraman, retired Telecommunications Engineer from Nokia; IEEE North Jersey Section Pre-University chair, WIE co-chair, Dr. Reena Dahle, Senior RF Scientist of Metamagnetics Inc; IEEE North Jersey Section WIE Co-Chair, Dr. Anisha Apte, Sr. Design Engineer at Synergy Microwave Corporation; IEEE AP-S AdCom member, AP-S COPE Committee Vice-chair-2, IEEE North Jersey section AP/MTT Vice-chair and SIGHT group Co-chair, and Dr. Charlotte Blair, Technical Manager, Ansys, IEEE Region-1 coordinator. The industry panel was moderated by Prof. Ratna Raj. The panelists described the IEEE Women in Engineering and IEEE TRY Engineering programs in addition to how female engineers make highly positive impacts at industrial workspaces.

Ms. Dimana Kornegay of NJIT's admission guided the senior students for the application process. The hands-on activity was guided by Dr. Byron Chen, Director of Labs of ECE Department. During the break and lunch time, videos of former female students of ECE describing their student and work experiences were presented.

The students were given the *Snap Circuits MyHome Plus* from Elenco Electronics and a multimeter to set up the activity. After lunch the students were divided into four groups for visit to MakerSpace, ECE Research Labs, Campus Tours and "Ask Anything" to the student panel, which was managed by current students Ms. Anushreya Ghosh, Ms. Jehan Salabi and Ms. Cori Frockowiak.

An excellent breakfast and a stupendous lunch were served to the attendees. The entire project was managed by Ms. Teri Bass and Ms. Ryoko Mathes of the ECE Department of NJIT. Joyce Lombardini of the EDS office publicized the event on social media and helped to secure the Snap Circuits kits from Elenco Electronics.

The news brief about this event can also be found on the NJIT website: https://news.njit.edu/campus-event-inspires-high-school-girls-study-electrical-engineering



Humanitarian Programs

VED National Institute of Technology—Silchar Student Branch Chapter Aids Flood Ravaged Villages

By T.R. Lenka

The Silchar town of Cachar district was submerged by a devastating flood due to heavy rain and excess water flow beyond the danger level in the Barak River for the period of 17–27 June 2022. The entire district was very badly affected by the flood situation. On 28 June 2022, the IEEE EDS/NTC/WIE members reached out to 230 flood affected families covering five nearby villages of NIT Silchar and distributed food and grocery items. It gave immense happiness to the IEEE members to help their local communities.

Silchar Flood Relief Distribution on 28 June 2022—Dr. Koushik Guha, Secretary, NTC (left), Dr. T. R. Lenka, Chapter Advisor, Prof. F. A. Talukdar, Branch Counselor, Dr. Arnab Nandi, Dr. Banani Basu, Faculty Advisor, WIE, Dr. M. Kavicharan, Dr. G. S. Baghel, Dr. D. S. Gurjar and Student Members

Awarded Student Membership Program

EDS is pleased to announce a new student award program. This new "Awarded Student Membership" program will provide up to 100 students with complimentary EDS and IEEE membership. Two tiers of award are available: Silver membership is available for students that have not previously been a member of IEEE and EDS, while Gold membership is available for students that are current members of IEEE and EDS. Preference is given to students that are active participants in IEEE and EDS events or activities. Students must be nominated by their chapter chair or student chapter advisor using an online form. Additional program information and links to nomination forms can be found here: https://eds.ieee.org/members/eds-awarded-student-membership-program.

ED Malaysia Kuala Lumpur Chapter STEM for all: Inspiring Malaysia Indigenous Students Through EDS-ETC

By Maizatul Zolkapli, Aliza Aini Md Ralib, and Rosminazuin Ab Rahim

In the spirit of promoting the advancement of technology to the school teachers and students, an educational and a community service event has been organized by IEEE Electron Devices Society (EDS) Malaysia Chapter in collaboration with student and staff volunteers from International Islamic University Malaysia. The program has been sponsored by EDS-ETC (EDHAC21-1) in response to the IEEE Electron Devices Society (EDS) and IEEE HAC Special Call for Proposals: *EDS-Relevant Technology for Local Community Challenges*. In the spirit of leveraging technology for a better tomorrow, the event is aimed at sharing the beautiful world of electronics with the students. The project targets 50 indigenous students aged 13 to 19 who are staying at Asrama Darul Falah PERKIM (ASDAF) hostel. This hostel was founded by Tuan Haji Yaakob bin Lazim and established on 19 August 1995 to accommodate Orang Asli (indigenous) children in the secondary school level. They originate from villages in the interior of the peninsular Malaysia to be given academic and religious education in Kuala Lumpur.

ASDAF students who attended the STEM workshop used Elenco Discover Coding kits donated by the EDS-ETC Program.

Since Malaysia has moved to endemic due to Covid-19, two series of face to face training program were conducted with 15 students and 4 staff volunteers from International Islamic University Malaysia under one common course name 'Usrah in Action' that addressed the issues from community through community services. A detailed community profiling survey was conducted during the course to identify the students' interest and awareness towards STEM education. It was a very crucial step before moving on to identifying the needs and providing assistance to help the students overcome all of their problems. Based on the data from the survey, it was discovered that the majority of the students found learning science and mathematics difficult. Therefore, we organized a half-day face-to-face STEM workshop conducted by EDS-ETC to introduce students to basic engineering sciences such as electrical circuits and their components. A total of 50 students participated in this workshop. Using the STEM module, the students learnt on assembling a circuit using the components provided in the kit.

The STEM modules were divided into two parts i) Snap Circuits Coding ii) Paper circuit. Among the selected projects there are *Flying Saucer, Fun Circuit* and *Fan Coding*. In the *Flying Saucer* project the students learnt the kinetic movement and the aerodynamics of a fan with a circuit. The shape of the designed fan blades will determine whether the fan will

fly or not by simply changing the positive negative position of the motor before demonstrating the circuit. As for the *Fun Circuit*, it focuses on sound with the use of speakers in the circuit. The speaker sound strength will be controlled by changing the value of the resistor in the circuit. As for *Fan Coding*, which involves coding, students write a code in the Snap Circuits® application that has been installed in the tablet and control the circuit with it. In response to the IEEE Electron Devices Society (EDS) and IEEE HAC Special Call for Proposals: *EDS-Relevant Technology for Local Community Challenges*, 6 tablets sponsored by EDS-ETC (EDHAC21-1) were given to the ASDAF management to assist the students on hands-on STEM learning using Snap circuit coding. This session certainly helped them in seeing the real application of electronics and it is hoped it will stimulate their interests in this field. The program's primary purpose is to improve in a series of workshops the science and electrical engineering understanding of ASDAF high school students. In addition, students quickly comprehended STEM related instruction over a series of modules since it was delivered practically. As a result, students will quickly grasp these STEM-related disciplines, and online learning will be facilitated as a result of tablet contributions. This may be ascribed to SDG 4 (Quality Education) and SDG 17 (Partnerships for the Goals) since both are concerned with education-related science and technology.

~Sharma Rao Balakrishnan, Editor

ED Kansai Chapter

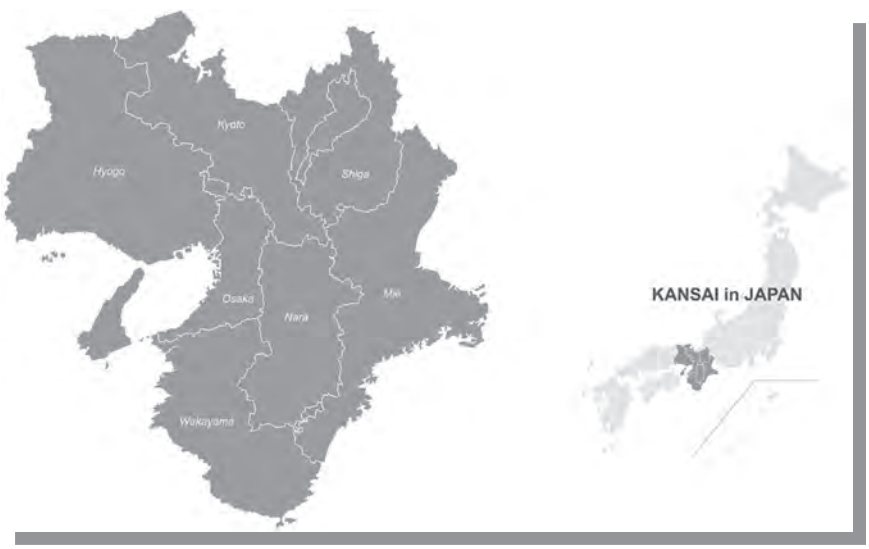
By Yuichi Ando

Annual General Meeting

The annual general meeting of EDS Kansai Chapter (EDSK) was held on 17 January 2022. At the meeting, in addition to reviewing chapter activity results of 2021, we also discussed the activity plan of 2022. There were a total 28 EDSK members who joined this online meeting.

Round Table Meeting

On 28 April 2022, the Chapter held the round table meeting and we discussed technical, industrial, educational, and business interests/concerns widely. Three speakers, Professor Uraoka, Dr. Okada, and Dr. Seki, members of EDSK, were invited to share their experiences, with 15 attendees enjoying the discussion.



~Alex Hou, Editor

ED Panimalar Institute of Technology—Chennai Student Branch Chapter

By Preethi Gandhi G S

The Chapter organized various academic programs for the benefit of the students of the institute, with several departments cooperating to organize activities. Three webinars were held during the months of April and May:

- "Higher Studies Opportunities in Abroad," by Premkumar Kora, Managing Director & Founder Kora Study Abroad Consultants. This event had nearly 30 attendees from various educational institutions. Special thanks to students Dhanalakshmi, Sushmitha and Reshma, for coordinating this successful webinar.
- "Key Insights of Student Volunteering," by Chaitanya F, Quality

Assurance Engineer, Perficient, Communication lead, who explained how his commitment to volunteering developed. He described the help received from the IEEE due to volunteering in many IEEE programs. The speaker also presented his survey results showing the significance of IEEE volunteering.

Snapshot of slide presentation held on 24 April 2022.

- "Soft skills – A core skill," by Dr. Supriya Kumaravelan, an international speaker, Toastmaster Communication & Leadership Coach, and soft skill Trainer. She spoke on the techniques of soft skills and their significance by explaining the differences between soft skills and hard skills. Nearly 40 participants from various educational institutions benefited from her talk.

IBM IEEE—AI Compute Symposium 2022—A Free Hybrid Research Event

Dear Researcher,

Together with the IEEE Circuits and Systems Society and the IEEE Electron Devices Society, IBM Research is hosting the 5th AI Compute Symposium. The Symposium will be held in-person on 12–13 October 2022 at the IBM T. J. Watson Research Center, Yorktown Heights, New York. Virtual attendance via livestream is also an option.

The IBM and IEEE sponsored Symposium will bring together dreamers, thinkers, and innovators in cutting-edge research for a two-day hybrid forum to explore AI Compute challenges and future research directions. This symposium is free of charge, but may limit the maximum number of virtual attendees, with the first registrants having priority.

This event features eminent distinguished speakers from academia and industry, a panel, as well as a student poster session. An award will be given to the best poster.

Distinguished speakers include:

- Stefanie Chiras, Red Hat
- Jason Cong, UC Los Angeles
- Tamar Eilam, IBM Research
- Tsu-Jae King Liu, UC Berkeley
- Robert Muchsel, ADI
- Steve Teig, Perceive
- Aaron Voon-Yew Thean, National University of Singapore
- Susan Trolier-McKinstry, Pennsylvania State University
- Arun Venkatachar, Synopsys
- Marian Verhelst, KU Leuven

See the Symposium website for registration and more details. A registration confirmation email will be sent about a day after registering.

https://www.zurich.ibm.com/thinklab/AIcomputesymposium.html

Contact Information:

Please send questions to the following symposium email address, or contact aics.ibm.ieee@gmail.com

Please consider attending the 5th IBM/IEEE AI Compute Symposium.

Rajiv Joshi
General Chair,
rvjoshi@us.ibm.com

Regional News

North America (Regions 1–7)

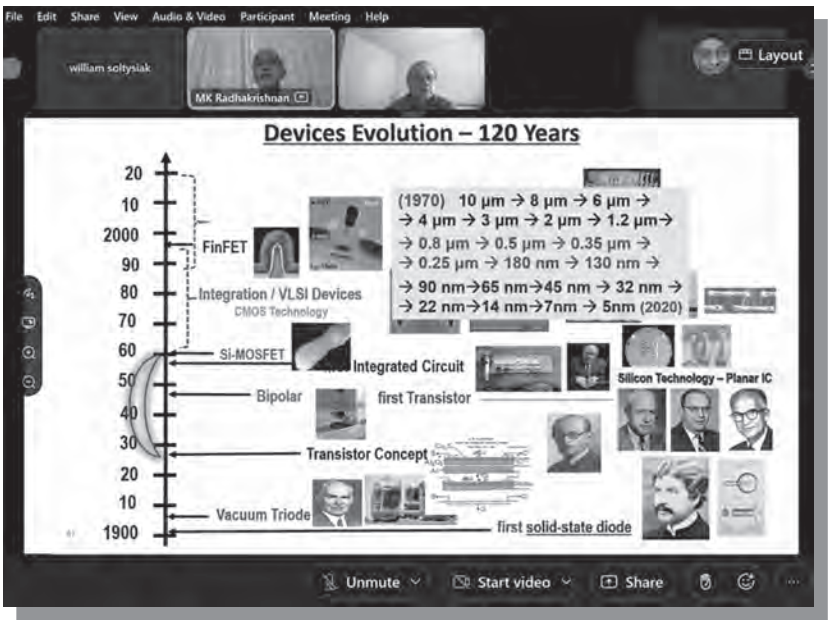
Northern Virginia/Washington DC Chapter Hosts Distinguished Lecture on 75 Years of Transistor and Its Impact on Humanity by Dr. M.K. Radhakrishnan

—by Xiangyi "Tony" Guo

The EDS Northern Virginia/Washington DC Chapter hosted on 22 March 2022 an IEEE EDS Distinguished Lecture (DL) on "75 Years of Transistor and Its Impact on Humanity" by Dr. M.K. Radhakrishnan, the Founder of NanoRel (Singapore) and Vice President of IEEE EDS (2016–2019). The DL was co-sponsored by local Chapters of Society on Social Implications of Technology, Nuclear and Plasma Sciences Society, Nanotechnology Council and Women In Engineering as well as the Baltimore Chapter of EDS.

Dr. M.K. Radhakrishnan began a lecture with the first study of a semiconductor device, according to a patent awarded 120 years ago, continuing to vacuum triode, to transistor concept, BJT, IC, Si-MOSFET, and to recent FinFET, with well-prepared materials and images. Later he covered technology impacts to society and humanity. He stated the benefits to humanity are immense from all the transistor and integrated circuit scaling but cautioned the audience to be aware of how technology is affecting the human thought process and behavioral pattern. One Q&A highlight is the sharing of our local member's involvement in Intel 4001-4004 development work back in 1970. The lecture presentation slides can be accessed through the vTools event (ID: 307058) Media section. The DL was attended by 87 participants. This event hit the highest attendee count in the last one year.

~Rinus Lee, Editor



M.K.Radhakrishnan Distinguished Lecture "75 Years of Transistor and Its Impact on Humanity"

The 9th IEEE Workshop on Wide Bandgap Power Devices & Applications 7–9 November 2022

The organizing committee for the 9th Annual IEEE/PMSA Workshop on Wide Bandgap Power Devices and Applications (WiPDA) [www.wipda.org] is looking forward to returning to an in-person event from 7-9 November 2022 at the Sonesta Redondo Beach and Marina in Redondo Beach, California.

The workshop is brought to you by the IEEE Power Electronics Society (PELS), the Power Supply Manufacturer's Association (PMSA), and the IEEE Electron Devices Society (EDS) and provides engineers and scientists with opportunities to share their expertise in wide bandgap (WBG) semiconductor technology.

The workshop will feature tutorials as well as keynote sessions, panel sessions, technical sessions, and a poster session that covers multiple technical tracks including silicon carbide (SiC) power devices, SiC applications, gallium nitride (GaN) power devices, GaN applications, Gallium Nitride (GaN) RF devices and applications and International Technology Roadmap for Wide Bandgap Power Semiconductors) (ITRW). Topics in emerging WBG materials will also be solicited.

Areas of Interest

WiPDA 2022 will feature papers within the following areas of interest:

- Heteroepitaxial & Bulk Materials Growth
- Gate Dielectrics & Surface Passivation
- Device Structures & Fabrication Techniques
- Device Characterization & Modeling
- Very-High Efficiency or Compact Converters
- Safe Operating Areas of Wide Bandgap Devices, including Short Circuit, Spike, & Transient Tolerance

- Harsh Environment (High Temperature) Operation & Reliability
- Packaging Power Modules & ICs
- Gate Drive & Other Auxiliary Circuits
- High-Performance Passive Components
- Hard-Switched & Soft-Switched Application Analysis
- Applications in Renewable Energy & Energy Storage, Transportation, Industrial Drives, Grid Power Systems, Space and Aerospace
- Wide Bandgap System Design Philosophies & Strategies
- Radio Frequency (RF) GaN
- Technology Roadmap of Wide Bandgap Including Devices, Applications and Packaging

To stay informed of the latest news and receive deadline reminders for WiPDA 2022, please subscribe. For sponsorship opportunities contact exhibitsatwipdaus@gmail.com.

Renee Yawger
WiPDA 2022 Publicity Chair
Renee.yawger@epc-co.com

Europe, Middle East & Africa (Region 8)

MIXDES 2022 Conference

—by Mariusz Orlikowski

On 23–24 June 2022, the 29th International Conference "Mixed Design of Integrated Circuits and Systems" MIXDES 2022 was held. After 2 years of the COVID-19 pandemic restrictions the conference participants had again an opportunity to meet in person in the beautiful city of Wrocław, Poland. The event was organized by the Lodz University of Technology together with the Warsaw University of Technology and co-sponsored by the Poland Section IEEE ED and CAS Societies, the Polish Academy of Sciences (Section of Microelectronics and Electron Technology), and the Commission of Electronics and Photonics of Polish National Committee of International Union of Radio Science—URSI.

Dr. Mariusz Niewczas (Design2Silicon Inc., USA) giving the lecture "IC Masks—The Challenges of the Newest Technologies"

The conference two-day program included 44 oral presentations coming from 19 countries. The following three general invited talks were presented during the conference plenary sessions:

- *IC Masks - The Challenges of the Newest Technologies*—Mariusz Niewczas (Design2Silicon Inc., USA),
- *Nanoelectronic Challenges and Opportunities for Cyberphysical Systems*—Maria Helena Fino (Nova School of Science & Technology, Portugal),
- *Ultralow Power Stretchable TFT Electronics*—Arokia Nathan (University of Cambridge, UK).

The Conference included also presentations in the frame of two special sessions:

- *Compact Modeling of Heterogeneous Devices and Systems* organized by Dr. Daniel Tomaszewski (Institute of Electron Technology, Poland) and Dr. Władysław Grabiński (GMC, Switzerland),
- *Special Session in Memory of Professor Wojciech P. Maly* organized by Prof. Wiesław Kuźmicz and Prof. Andrzej Pfitzner (Warsaw University of Technology, Poland).

The second of the sessions was dedicated to memory of the late Prof. Wojciech P. Mały, an outstanding academic teacher at the Warsaw University of Technology, Poland, and at the Carnegie Mellon University in Pittsburgh, USA, and a world-class scientist in the field of microelectronics. He passed away in December 2021.

The MIXDES Conference organizers hope to meet all together next year in Kraków, Poland (29 June–1 July 2023), one of the oldest cities and a former capital of Poland. There will also be an opportunity to celebrate the 30th anniversary of the conference. The MIXDES 2023 Preliminary Call for Papers is available at http://www.mixdes.org/downloads/call2023.pdf. More information about the past and next MIXDES Conferences can be found at http://www.mixdes.org.

IEEE EDS Distinguished Lecturer Session and ED Poland Chapter Meeting

—by Kalina Detka

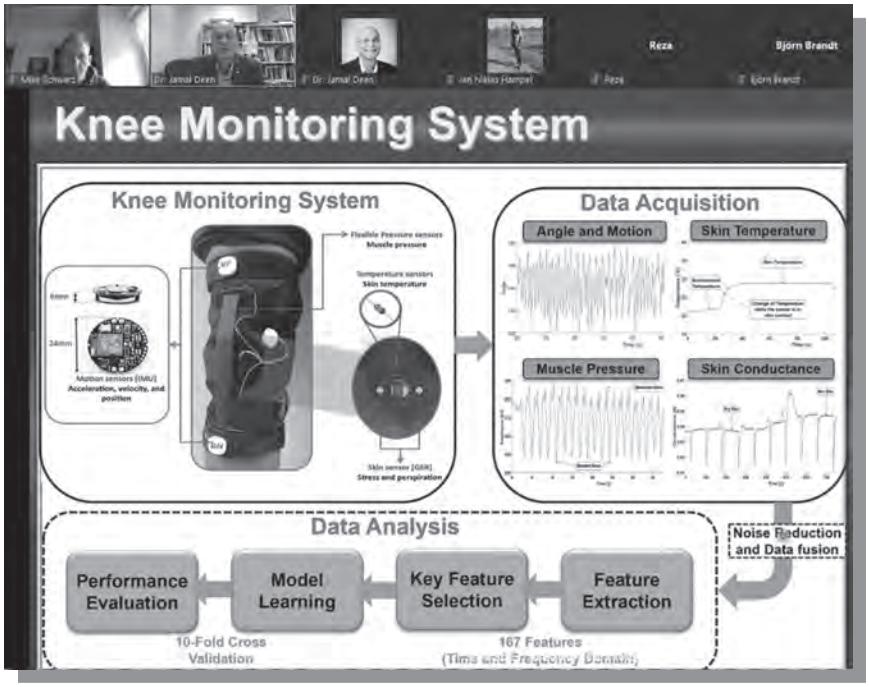
On 23 July 2022, an IEEE EDS Distinguished Lecturer Session was organized by the IEEE Poland Section Chapter, ED/EP Joint Chapter with

technical support from MIXDES 2022 organizers. Four lectures were delivered during the seminar:

- *Power Flexible Electronics*, EDS Distinguished Lecture (on-line) by A. Nathan (University of Cambridge, UK)
- *On the Need for Non-conventional Nanoelectronics Devices Characterization in Engineering Graduate Courses: Modeling Needs and Design Challenges* by M.-H. Fino (Nova School of Science & Technology, Portugal)
- *Compact Modeling and Free Open Source PDKs in FOSS TCAD/EDA Perspective* EDS Distinguished Lecture (on-line) by W. Grabiński (GMC, Switzerland)
- *FETs as Detectors of THz Radiation* by D. Tomaszewski (Ł-Inst. of Microelectronics and Photonics, Poland)

Immediately after the seminar, a meeting of the IEEE Poland Section Chapter, ED/EP Joint Chapter took place, which included a lecture on electrothermal simulations in electronic power devices by Dr. Paweł Górecki (Gdynia Maritime University). The last point of the meeting was a discussion on organizational matters moderated by Prof. Krzysztof Górecki (Gdynia Maritime University), the Chapter Chair.

~Marcin Janicki, Editor



Prof. Deen presenting a Knee Monitoring System

Successful Jamal Deen Distinguished Lecture on "Smart Sensors and Smart Homes for Ubiquitous-Healthcare – AI is a Key Enabler"

—by Mike Schwarz

We are delighted to report on the IEEE EDS Distinguished Lecture from the ED Germany Chapter that took place on 22 April 2022. The lecture was organized by the ED Germany Chapter and co-sponsored by the NanoP from THM – University of Applied Sciences. There were numerous IEEE participants and many non-IEEE members who attended the lecture.

Distinguished University Prof. Jamal Deen started with a motivation, setting the focus on the increased life expectancy and resulting aspects of this changing boundary with respect to social, economic and health conditions. Afterwards, he introduced Smart Sensors and Smart Homes, giving several important advantages they possess to address the immense challenges for our aging society and Ubiquitous Healthcare. To reinforce his arguments, he also discussed business trends and opportunities. Dr. Deen offered a lot of use cases and the needs to enhance quality of life. One particular focus was set on human body mobility (walking, movement) as a use case. Dr. Deen offered several mobility parameters and metrics, and how they are monitored and used. Examples of mobility (walking) degradation and its root causes were discussed.

Afterwards, the Lecturer started with various aspects regarding the sensor system requirements and design and needs in terms of processing with artificial intelligence. Examples for data clustering and findings were presented. Then, Dr. Deen introduced applications of artificial intelligence (AI) in healthcare. He discussed and offered his thoughts on how to extract features from processed data and use them with different machine learning algorithms for classification and diagnostics. Finally, he gave a perspective of upcoming enhancements caused by artificial intelligence and how healthcare and humanity will benefit from this type of research and technology development. In particular, he emphasized that computing and engineering offers viable solutions to help overcome the challenging issues of an aging world.

"The Future of Computing and Storage" Workshop

—by Pascale Caulier, Francis Balestra, and Mike Schwarz

"The Future of Computing and Storage" Workshop, supported by IEEE EDS, was held 17 May 2022 in Udine, Italy, and was devoted to the update of the European contribution to the IRDS Roadmap in the field of More Moore advances and Cryogenic electronics & Quantum information processing (CEQIP). The

Heike Riehl and Francis Balestra during discussion of European and International Roadmaps

main challenges, most promising technologies, needed research efforts and possible applications were presented in the following sessions by renowned EU experts.

During an initial Session devoted to the Overview of European and International Perspectives, Francis Balestra CNRS-G_INP, Director of the SINANO Institute, Chair of EDS France, gave in introduction some information on the European and International Roadmaps. Then Paolo Gargini, IRDS Chairman presented the IRDS Roadmap and Francisco Ibañez, DG Connect, Deputy Head of Unit- European Commission, gave an overview of the European Chips Act.

A first session, devoted to More Moore Advances, started with the overview of the IRDS More Moore Roadmap and Implications for System Scaling. The presenter was Dr. Mustafa Badaroglu—Qualcomm & IRDS More Moore Team leader. Five valuable presentations gave the European views on: Two-dimensional materials as a platform for SOT-based memories (by Dr. Jose Hugo Garcia—ICN2),The role of Non-Volatile Memories in novel computing architectures (by Konrad Seidel—Fraunhofer IPMS), Ferroelectric memristors and memcapacitors as a CMOS compatible physical substrate for bio-inspired neuromorphic computing (by Dr. David Esseni—IUNET—University of Udine), Opportunities and challenges using 2D materials in Nanodevices (by Inge Asselberghs—imec), and Heterogeneous Integration of 2D Materials (by Eros Reato—AMO GmbH).

A second session dedicated to Cryogenic Electronics & Quantum Information Processing, started with the Summary of the IRDS Cryogenic Electronics and Quantum Information Processing (CEQIP) Roadmap by Dr. Scott Holmes—IRDS CEQIP International Focus Team Chair. It was followed by six captivating presentations on this area by European experts:

- Cryogenic CMOS with FD SOI and Si Nanowires (by Dr. Qing-Tai Zhao—JARA Institute/FZJ & RWTH)
- Challenges and possible solutions in the field of alternative Computing Architectures (by Dr. Heike Riel—IBM)
- The potential and global outlook of Integrated Photonics for Quantum Technologies (by Dr. Emanuele Pelucchi & Dr. Giorgos Fagas—Tyndall)
- Challenges for the semiconductor industry to enable Silicon based quantum computing challenges (by Dr. Maud Vinet—CEA-LETI)
- Cryo-CMOS circuits and systems: an enabling technology for large-scale quantum computers (by. Dr Fabio Sebastiano—TU Delft / QuTech)
- Quantum transport in Nano-electronics devices (by Dr. Vihar Georgiev – University of Glasgow & SemiWise)

The presentations are available on the SINANO Institute website: https://www.sinano.eu/the-future-of-computing-and-storage-workshop-may-17-2022/

~Mike Schwarz, Editor

imw 2022 International Memory Workshop

2022 IEEE International Memory Workshop (IMW)

The 14th International Memory Workshop (IMW) was held at Taschenbergpalais Kempinski hotel in Dresden, Germany, from 15–18 May 2022. The last two editions of the event were virtual due to the Covid pandemic. IMW returned after the break as an on-site workshop in a hybrid format, which was the first case for IMW. The Workshop had a mix of on-site and live virtual presentations, with live streaming of the event and interactive Q&A sessions allowing the remote participants to interact live with the presenters. The recordings of all the events were made available to the registered participants for a month for on-demand viewing.

The IMW is sponsored by the IEEE Electron Devices Society and meets annually in May. The workshop is a unique forum for specialists in all aspects of semiconductor memories (non-volatile & volatile). The scope of workshop content ranges from new memory concepts in early research to the technology drivers currently in volume production as well as emerging technologies in development. The technical sessions are organized in a manner that provides ample time for informal exchanges amongst presenters and attendees. More than 200 people took part in our meeting this year with around half of the

Poster presenters in Q&A discussions. Poster papers were presented as short talks to make it compatible with live streaming and recording

participants attending in-person and the other half participating online.

This year's program included a one-day short course, with tutorials on Ferroelectric Memories and Security Aspects of 3D Memories, delivered by experts on the topics from both the industry and the academia. The technical program for single-track conference spanned three days and opened with keynote talks by Lars Heineck (Micron) on NAND Flash trends, Johannes Müller (GlobalFoundries) on Embedded STT-MRAM status and outlook, and Giuseppe Croce (STMicroelectronics) on Non-volatile memory in Smart Power technology applications. The program included invited talks given by experts in memory field—Gabriel Molas (Weebit Nano), Stuart Parkin (MPI Halle), Munehiro Tada (NanoBridge), Daniel Worledge (IBM), and Maarten Rosmeulen (imec)—providing an exciting overview of the main trends for memory technologies and applications.

The IMW is also an excellent forum to present new and original technical works and this year's technical program comprised 27 excellent papers, which included 16 oral (full-length) presentations and 11 posters (short talk). The papers were selected by the technical committee among more than 45 papers submitted. They covered the major categories of memory technologies (Flash, Ferroelectric, MRAM, RRAM, PCM, DRAM, SRAM, emerging technologies) and NVM applications (Automotive, In-memory computing). Among the exciting news presented at the conference, the paper titled "Reliability of 28nm embedded RRAM for consumer and industrial products" presented by Christian Peters (Infineon) won the Best Paper Award, and the paper "Performance Benchmarking of Spin-Orbit Torque Magnetic RAM (SOT-MRAM) for Deep Neural Network (DNN) Accelerators" by Yandong Luo (Georgia Institute of Technology) received the Best Student Paper Award. Another highlight of the event was a stirring panel discussion "Are Emerging Memories Finally Emerging?" hosted by Tomoya Sanuki (Kioxia).

Next IMW will be held May 2023 in Monterey, California, United States. For more details on the IMW conference please visit the IMW website: http://www.ewh.ieee.org/soc/eds/imw/. IMW technical proceedings are available on the IEEE Xplore database: https://ieeexplore.ieee.org/xpl/conhome/9779263/proceeding.

Srivardhan Gowda
IMW 2022 Publicity Chair
Intel

Latin America (Region 9)

ED South Brazil Chapter

—by Joao Martino

The Chapter organized the Mini-Colloquium 2022 on "Micro and Nanodevices" which was held virtually on 20 June 2022. The Mini-Colloquium included four Distinguished Lectures of EDS/IEEE as listed below:

1) Prof. Hiroshi Iwai from National Yang Ming Chiao Tung University, Taiwan, presented a lecture entitled "Impact, History and Future of Nanoelectronics." The main message of his talk was the meaning and impact of the transistor invention on micro- and nanoelectronics.
2) Prof. Manoj Saxena from Deen Dayal Upadhyaya College University of Delhi, India, presented the lecture entitled "Tunnel Field Effect Transistor and its Application as Highly Sensitive and Fast Biosensor." The speaker focused on Non-classical MOSFETs architectures and Emerging architectures of Tunnel-FETs.
3) Profa. Elena Gnani from University of Bologna, Italy, presented the lecture entitled "Trends and Challenges in Nanoelectronics for the Next Decade." Professor Elena talked about the Beyond CMOS devices presenting several alternative devices.
4) Prof. Cor Claeys from KU Leuven, Belgium, presented the lecture entitled "Past, Present and Future of microelectronics: 75 Years of Material and Device Challenges." The speaker talked about the technological evolution during the 75 years since the invention of the transistor. He presented market trends looking at different applications as nanosheets and fork transistors for nanoelectronics and GaN based devices for power electronics.
5) We had an official registration of 101 attendees, where 34 were IEEE members and

IEEE/EDS South Brazil Chapter 2022 Mini Colloquium on "Micro and Nanodevices" on 20 June 2022

15 were Electron Device Society members.

~Paula Agopian, Editor

LAEDC 2022 and Accompanying Events

—by Pablo Moliterno

EDS Summer School

The EDS Summer School themed "Design, characterization and reliability of sensors and integrated circuits", was held on 1–3 July 2022, in Puebla, Mexico. It was organized by the EDS Puebla Chapter and the National Institute of Astrophysics, Optics and Electronics (INAOE). The event was a great success. Out of 345 enrolled students, 114 participated in the School in person, and 231 virtually. The session was attended by students from EDS chapters throughout Latin America: Guatemala, El Salvador, Honduras, Nicaragua, Costa Rica, Brazil, Chile, Colombia, Ecuador, Argentina, Mexico, Peru, Panama, plus 18 from Ghana and 1 form India.

During three days, there were 12 presentations. On the first day, under the general topic "Semiconductor materials, devices, and fabrication": Fernando Guarin, "Opening remarks and overview of the semiconductor industry", Edmundo Gutiérrez, "Introduction to the Physics of Semiconductor Materials and Devices", Alfonso Torres, "Manufacturing process of semiconductor devices", Alba Avila,

Students from EDS Chapters in INAOE, Cholula, Puebla, Mexico

Group photo of the attendees and speakers of the EDS Summer School

"Practical aspects of clean room and operation." The first day was concluded by a virtual visit to the INAOE 0.8 µm manufacturing laboratory. On the second day, under the general topic "Design and applications": Edmundo Gutiérrez, "Cryogenic operation of semiconductor devices, Elkim Roa, "Digital Design: From transistors to computing," Maria Teresa Sanz, "Design of analog integrated circuits", Claudia Reyes, "Design and fabrication of bio-chemical sensors," Alejandro Bautista, "Overview of the first Latin-American IC Design Contest." On the third day under the general topic "Systems, characterization, and reliability: Daniel Durini, "Radiation sensors, theory and practice," Fernando Guarin, "Semiconductor Reliability Overview including RF/mmW/5G," Wilfrido Moreno, "Model-Based Systems Engineering (MBSE)."

EDS Mini-Colloquium

On Sunday, 3 July 2022, a Mini-Colloquium (MQ) was held the day before the start of the 4th LAEDC. Four invited speakers, all of them EDS Distinguished Lecturers, delivered talks ranging from advanced materials and semiconductor device technologies to design, compact modeling and reliability.

Dr. Lluis F. Marsal, from the University Rovira i Virgili, Spain delivered a presentation entitled "Efficient and Stable Organic Solar Cells for Versatile Applications." Dr. Edmundo A. Gutiérrez D., from the National Institute of Astrophysics, Optics and Electronics (INAOE) in Puebla, Mexico gave his lecture entitled "Cryogenic Energy Efficiency and reliability of 65 nm and 14nm FinFETs for Quantum Computing Applications". Dr. Subramanian S. Iyer, from the University of California at Los Angeles delivered a talk titled "Analog in-memory computing using the charge trap transistor." Finally, Dr. Felix Palumbo from the National Council of Science and Technology (CONICET) and a full professor at National Technological University (UTN) in Buenos Aires, Argentina, gave a talk entitled "Dielectric breakdown in thin dielectrics. From silicon dioxide to layered dielectrics." The MQ was attended by around 80 researchers and students including IEEE EDS members.

MOS-AK Workshop

Afterwards, also on 3 July, the 4th Latin American edition of the MOS-AK Workshop on Compact Modeling was held. It was chaired by Prof. Benjamin Iñiguez (Universitat Rovira i Virgili,Tarragona, Spain). It included seven talks. Dr. Daniel Tomaszewski, IMiF, Warsaw (PL) presented a talk "FETs as detectors of THz radiation". Prof. Nagaditya Poluri, Uni. Sheffield (UK) addressed a topic "Capacitance modeling of a transistor for RF Power Amplifiers in 5G applications." Prof. Juan Brito, IMPINJ (BR) gave a talk "MOSFET mismatch characterization made easier: a 2-Transistor test array structure for a voltage-only measurement approach". Prof. Roberto Murphy, INAOE, Puebla (MX) presented a work "Further considerations for RF CMOS compact modeling". Prof. Benjamin Iñiguez addressed a topic "Compact modeling for TMD FETs". Prof. Antonio Cerdeira, CINESTAV (MX) presented a talk "On the Compact Modelling of Si Nanowire and Si Nanosheet MOSFETs." Finally, Prof. Gilson Wirth, UFRGS (BR) gave a talk "Towards Unified Compact Modeling of RTN (time domain), 1/f Noise (frequency domain) and BTI." Over 50 academics, professionals and students attended the Workshop and enjoyed the discussions with the speakers.

LAEDC 2022

The IEEE Latin America Electron Devices Conference (LAEDC 2022) sponsored by the IEEE Electron Devices Society (EDS) was held on 4-6 July 2022 in the Hotel Presidente Intercontinental, Puebla, Mexico. The main topics of interest were: All electron based devices, Semiconductors, MEMS, and Nanotechnologies, Packaging, 3D integration, Sensors and Actuators, Display technology, Modeling and Simulation, Reliability and Yield, Device Characterization, Energy Harvesting, Biomedical Devices, Circuit Device Interaction, Novel Materials and Process Modules, Technology Roadmaps, Electron Device Engineering Education, Electron Device Outreach, Optoelectronics, 5G, Quantum Computing, Photovoltaic and Photonic Devices and Systems.

The Organizing Committee included Edmundo Gutierrez (General Chair), Mario Aleman (Financial Chair), Esteban Arias (Program Chair), Benjamin Iñiguez (MOS-AK Chair), Jean-Michelle Sallese (Publication

Dr. Edmundo Gutiérrez at the Mini-Colloquium

Chair), Pablo Moliterno (Webmaster/Publicity), Danny Xie Li and Julio Bello Pavón (Technical support), and Lluis F. Marsal (Technical co-Chair).

We received contributions from authors of the Americas, Europe, Oceania and Asia: Spain, Mexico, USA, Germany, France, Switzerland, Austria, Japan, China, India, Argentina, Costa Rica, Colombia, Ecuador, Brazil, Canada, and Greece. Eighty-one professional leaders and volunteers attended the Conference in person, whereas 80 people attended it virtually. Scholarships were provided to 35 EDS student members from the summer school who received full support to attend the Conference. Many volunteers actively participated in the Conference delivering presentations during the poster session as a part of the Conference technical program. Most of these volunteers stated that this was the first time attending an international conference of the IEEE technical society.

During LAEDC, a SIGHT (Special Interest Group on Humanitarian Technology) workshop was also organized. It was sponsored by the IEEE Humanitarian Activities Committee (HAC). The attendees learned about funding opportunities and benefits, and best practices in the deployment of technology projects in underserved communities. The workshop was delivered by Dr. Pritpal Singh (SIGHT Assessment Sub-committee Chair), Dr. Luis Kun (SSIT Chair), Dr. Sampathkumar Veeraraghavan (HAC Chair) and Morgan Kiani.

There was also a very successful Women in Engineering and Young Professionals Session with the subject "The role of women in STEAM fields" delivered by Jenna Ward Brennan (Senior Director, Product Management, GE Healthcare), Magaly Sandoval Pichardo (Senior Analog & Mixed Signal Methodology Engineer and Project Manager at the Solutions Group, Synopsys), Jeewika Ranaweera (Principal Hardware Engineer, Oracle) and Morgan Kiani, Ph.D. (Associate Professor, TCU University) hosted by Dr. Alba Avila of the Universidad de los Andes, Bogota, Colombia.

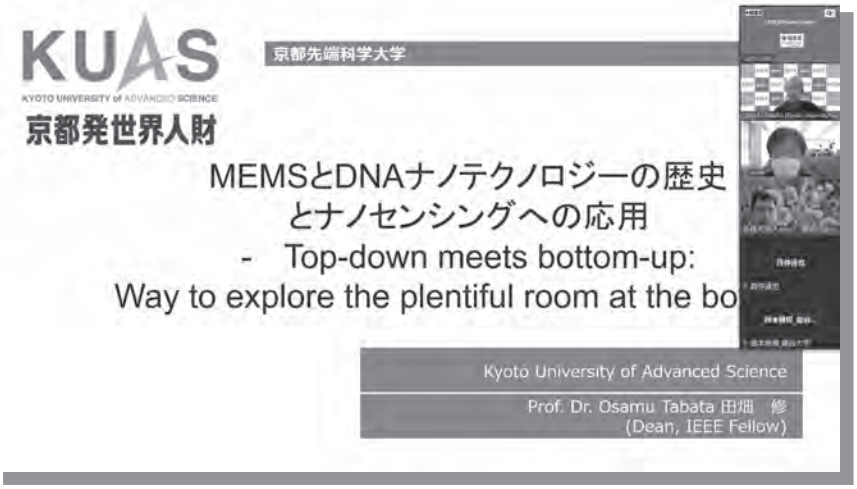
This year the technical program of the Conference included 120 papers presented in nine sessions grouped by specific themes. Three Keynote speakers made magistral presentations: Dr. Hiroshi Iwai, "Invention of the Transistor 75 years ago, The Origin of Device Miniaturization towards Super-Intelligent Society," Dr. Martin A. Green, "Recent Developments and Future Trends in Solar Photovoltaics," and Dr. Subramanian S. Iyer, "Chips, dies, chiplets and dielets and heterogeneous integration." There were seventeen invited speakers: Dr. Laurie E. Calvet, "OTFT neuro-inspired circuits for classification tasks," Dr. Theresia Knobloch, "Scalable and Reliable Gate Insulators for 2D Material-Based FETs," Dr. Dragica Vasileska, "Computational Electronics: An Overview," Dr. Fernando Guarin, "Practical Considerations and methodology for the reliability evaluation of 5G SOI Technologies," Dr. Eugenio Cantatore, "Flexible sensing surfaces based on printed electronics," Dr. Gilson Wirth, "The role of the observation window on the intra- and inter-device variability of RTN," Dr. Luis Kun, "Disparities 2022 and the Global Citizen Safety and Security. A Transformational opportunity for Engineers as Systems Conductors of Society Critical Thinking," Dr. Allan Granados, "System modeling using GO and KPN networks," Dr. Ricardo Donaton, "Integrating new technology elements to enable a 4000+ qubit quantum computer," Prof. Dr. Stefan van Waasen, "How to build a universal quantum computer?—The scaling challenge," Dr. David Hughes, "Hunting a supermassive black-hole in the center of the Milky Way with the Event Horizon Telescope," Dr. Fernando Silveira, "Reliability aware design of RF circuits," Dr. Sebastian Matias Pazos, "Reliability-Aware Design Space

Humanitarian Session

Women in Engineering and Young Professionals Panel

Exploration for Fully Integrated RF CMOS PA," Dr. Pascal Xavier, "RF printed electronic devices using bio-sourced materials: risks and opportunities," Dr. Sourabh Khandelwal, "ASM-ESD—A comprehensive physics-based compact model for ESD Diodes," Dr. Christoph Jungemann, "Device Simulation of the Dyakonov-Shur Plasma Instability for THz Wave Generation," Dr. Hans Kleemann, "Vertical Organic Transistors – Approaching the GHz-Threshold with Organic Devices," and Dr. François Danneville, "Challenges to measure RF noise and intermodulation performances of mmW/THz devices."

The Conference participants enjoyed a very friendly atmosphere that was conducive to many fruitful discussions, most of them while enjoying the wonderful local coffee. Various social events were held like the welcome reception, the well-attended Young Professionals/Women in Engineering mixer, and the conference banquet where the local flavors were mixed with music and a performance by a Mariachi band. Several activities were also conducted to further increase participation in EDS chapter activities and increase membership in the society. We also celebrated the 75th anniversary of the transistor with a large cake that was shared with the audience.



Prof. Osamu Obata from Kyoto University of Advanced Science gave his speech on "Top-down meets bottom-up: Way to explore the plentiful room at the bottom"

Asia & Pacific (Region 10)

ED Kansai Chapter

—by Yuichi Ando

Distinguished Lectures

The ED Kansai Chapter DLs were held virtually on 15 May 2022. Two distinguished speakers were invited to share the topics of MEMS technology and ferroelectric devices. Professor Osamu Obata from Kyoto University of Advanced Science gave a speech on "Top-down meets bottom-up: Way to explore the plentiful room at the bottom." Professor Shinichi Takagi from the University of Tokyo gave a speech on "Physical reservoir computing using ferroelectric devices." A total of 100 attendees, including 19 EDS members and students, joined this meeting. Everyone was interested in it and enjoyed the advanced topics.

Upcoming Events

EDS Kansai Chapter will hold two events in the next half of the year. The first one, Kansai Colloquium, Electron Devices Workshop, will be held on 7 October, 2022. The second one is IMFEDK 2022 (The 2022 International Meeting for Future of Electron Devices, Kansai), which will be on 28–30 November 2022.

(https://www.ieee-jp.org/section/kansai/chapter/eds/imfedk/)

EDTM-2022 (IEEE Electron Devices Technology and Manufacturing) Report Session—IEEE EDS Japan Joint Chapter

—by Nobuyuki Sugii and Naoki Watanabe

On 12 May 2022, the report session of IEEE 6th Electron Devices Technology and Manufacturing (EDTM) Conference 2022 (https://ewh.ieee.org/conf/edtm/2022/) was held as a hybrid format at Suzukakedai Campus, Tokyo Institute of Technology. Dr. Kazunari Ishimaru, General Chair of EDTM 2022, presented EDTM-2022 activities and the future EDTM-2023 plans. Dr. Masumi Saitoh, Technical Program Committee Chair of EDTM-2022, introduced program topics of EDTM-2022. At the report session, the subcommittee members reported the trends of the respective technical sessions.

The program and announcement of this report session have been posted on the EDS Japan Joint Chapter's webpage (https://www.ieee-jp.org/section/tokyo/chapter/ED-15/2022/EDTM2022report/EDTM2022_ReportSession_en.pdf).

The report session of EDTM-2022 (IEEE Electron Devices Technology and Manufacturing) attendees (in-person and online) on 12 May 2022, Kanagawa

The next EDTM (IEEE EDTM-2023) is planned as an in-person event in Seoul, Korea, on 7–10 March 2023. (https://ewh.ieee.org/conf/edtm/2023/index.html).

ED/SSC Hong Kong Chapter

—by Yansong Yang

Distinguished Lecture

On 3 March 2022, the IEEE Hong Kong Joint Chapter of Electron Devices and Solid-State Circuits (ED/SSC) participated in hosting the HKU BME distinguished lecture given by Prof. George Malliaras, the Prince Phillip Professor of Technology at the University of Cambridge. The title of his lecture was "Technology for Bioelectronic Medicine." Bioelectronic medicine provides a new means of addressing disease via the electrical stimulation of tissues. Deep brain stimulation, for example, has shown exceptional promise in the treatment of neurological and neuropsychiatric disorders, while stimulation of peripheral nerves is being explored to treat autoimmune disorders. To bring these technologies to patients at scale, however, significant challenges remain to be addressed. Prof. Malliaras discussed that the key is our ability to establish stable and efficient interfaces between electronics and the human body. Prof. Malliaras presented several examples of using new organic electronic materials and devices engineered to communicate with the body and evolve with it.

On 26-28 April 2022, the Chapter participated in organizing the International Symposium on 3D IC and Heterogeneous Integration. Twelve world-renowned speakers were invited to give lectures covering several popular topics, including system architecture & design in the Era of 3D IC, 3D IC & M3D, and System-in-Package & Heterogeneous Integration. In total, over one hundred participants, including over 40 IEEE members/student members, attended these two activities.

Upcoming TENCON 2022 on 1–4 November 2022

TENCON 2022 and ISPSD 2023

The Chapter is working on organizing two conferences. The first one is the IEEE Region 10 conference (TENCON), which is a premier IEEE international technical conference conducted in Region 10 to bring exciting discoveries, knowledge & understanding. TENCON 2022 will be held on 1–4 November 2022. More information on: https://www.tencon2022.org/.

The second one is the 35th International Symposium on Power Semiconductor Devices and ICs (ISPSD 2023), which is the premier forum for technical discussions in all areas of power semiconductor devices and power integrated circuits. ISPSD 2023 will be held in the city of Hong Kong physically from 28 May to 1 June 2023. The Readers can find more information on: https://www.ispsd2023.com/.

ED NCTU Student Branch Chapter

—by Ming-Chun Hong

An invited hybrid seminar "*Encounter with the Digital Age*" was co-organized by the Department of Electrical Engineering, National Yang Ming Chiao Tung University (NYCU) and EDS NCTU Student Branch Chapter on 24 June 2022. Prof. Simon Sze was invited to share his reflections on the history of semiconductor technology development, personal research experience, and invaluable philosophy of life. Prof. Sze is the NYCU honorary Chair Professor and the IEEE celebrated member. He is best known for his invention of floating-gate memory and the most popular textbook in the field of semiconductor device physics, *Physics of Semiconductor Devices*. He shared his five personal journeys and reflections, including his earlier research on the dielectric constant extraction of silicon in Schottky barriers, his world-renown textbooks, his founding of the first semiconductor company in Taiwan, the humble origin of the powerhouse of the Taiwan semiconductor industry, and finally his epoch-making invention of floating-gate memory. It is a rare opportunity to have a true semiconductor guru sharing his life-long experience with our young students and faculty,

The invited hybrid seminar "Encounter with the Digital Age" by Prof. Simon Sze

including 50 who attended in person and dozens of others who joined on-line. We all enjoyed Prof. Sze's inspiring talk very much.

ED Taipei Chapter
—by Steve Chung

The ED Taipei Chapter held a Distinguished Lecture on 28 June 2022, given by Prof. Hei Wong from the City University of Hong Kong. The Lecture "On the CMOS Device Downsizing, More Moore, More than Moore, and More-than-Moore for More Moore," was arranged in a virtual format. Prof. Hei Wong began with introducing the concept of CMOS devices downsizing, either by shortening the gate-length/half-pitch spacing or by folding the channel width, which might be ended in a couple of generations. However, Moore's Law will continue to grow for at least another decade by using 3D stacking in IC manufacturing or time scaling in device operations. This talk addressed the issue that "More Moore" will no longer rely on the smaller size of transistors or higher density of individual chips. It will be powered by More-than-Moore. So, he advocated the concept of a 3D version of More-than-Moore by adding the third dimension which is attributed to "software, application, and architecture." The hyperspace scaling via the high-speed network interconnection and the new computation architecture could be the most viable way to boost the computing power of ordinary digital terminals to a new level. There were more than 45 graduate students and professors who attended this precious talk.

~Alex Hou, Editor

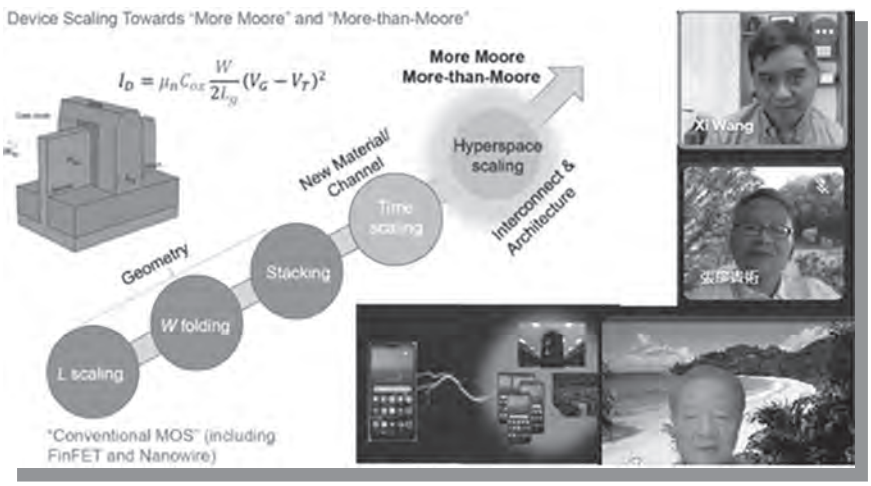
Distinguished Lecture by Prof. S. Deleonibus

ED Malaysia, Kuala Lumpur Chapter

ED Malaysia's Virtual Distinguished Lecture: New Routes and Paradigms for Device Engineering in the Nanoelectronics and Nanosystems Era
—by Maizatul Zolkapli, Hazian Mamat, Suhana Mohamed Sultan, and Ahmad Sabirin Zoolfakar

The ED Malaysia Chapter successfully organized the second Distinguished Lecture in 2022. Prof S. Deleonibus, the CEA Research Director and Past Chief Scientist, Université Grenoble Alpes, France gave an on-line talk on 30 May 2022, titled "New routes and paradigms for Device Engineering in the Nanoelectronics and Nanosystems Era." The lecture was attended by 30 participants.

The main topic of the presentation was a major power consumption reduction that will drive future design of technologies and architectures requesting less energy-greedy devices and interconnect systems. The electronic market will be able to face exponential growth thanks to the availability and feasibility of autonomous and mobile systems necessary to meet societal needs. The increasing complexity of high volume fabricated systems will be possible if we aim at zero intrinsic variability, and generalize 3-dimensional integration of hybrid, heterogeneous technologies at the device, functional and system



ED Taipei Distinguished Lecture on June 18, 2022 (virtual presentation) Top right (H. Wong-speaker, K. S. Chang-Liao, Steve Chung-seminar chair)

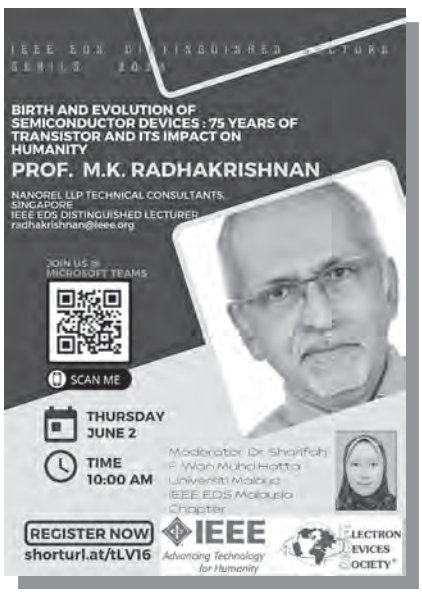
levels. Weighing on the world energy saving balance will be possible and realistic by maximizing the energy efficiency of co-integrated Low Power and High Performance Logic, Memory devices and Nanosystems to serve data computing and storage, functional diversification and communication. Thanks to the new technological opportunities, alternative neuromorphic and quantum based computing are showing up. The future of Nanoelectronics will face the major concerns of being Energy and Variability Efficient (E.V.E.).

IEEE EDS Malaysia's Virtual Distinguished Lecture: Birth And Evolution Of Semiconductor Devices

—by Maizatul Zolkapli, Hazian Mamat, Suhana Mohamed Sultan, and Ahmad Sabirin Zoolfakar

IEEE EDS Malaysia Chapter successfully organized the third Distinguished Lecture in 2022. Dr. M.K. Radhakrishnan, the Founder Director of NanoRel LLP -Technical Consultants Singapore gave an on-line talk on 2 June 2022, titled "Birth and Evolution of Semiconductor Devices: 75 Years Of Transistor And Its Impact On Humanity." The presenter shared views on the progression of device technology and its transformation from micro- to nanoelectronics including the present stage. The benefits to humanity are immense from all these, but seem to challenge fundamentals of the human thought process and behavioral pattern. A major pattern change is already happening. Reflections from various corners are alarming and a short discussion about such observations was also part of this talk. The event catched attention of about 80 participants from Malaysia and other countries. The footage of the presentation is also being shared on social media i.e. YouTube channel *IEEE EDS Malaysia* which has been set-up to increase the visibility of IEEE EDS and as an approach for membership promotion.

~Sharma Rao Balakrishnan, Editor



Distinguished Lecturer by Dr. M.K. Radhakrishnan

ED Delhi Section Chapter

—by Harsupreet Kaur and Manoj Saxena

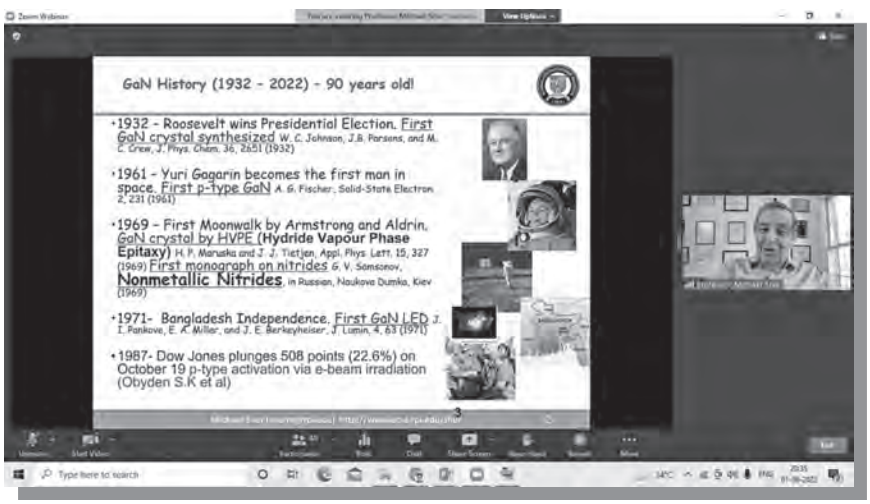
The Chapter organized several events during the first half of the year:

A Distinguished Lecture on the topic "Landscape of Synaptic Weight Memories," which was organized on 2 February 2022 in association with the Department of Electronics of Maharaja Agrasen College. The speaker, Prof. Shimeng Yu, Georgia Institute of Technology, explained the fundamentals of synaptic devices and their role in emerging fields like Artificial Intelligence and Machine Learning. The lecture was very insightful and attended by over 72 participants including 14 IEEE members.

In collaboration with the Department of Electronic Science, University of Delhi South Campus and the Center for India-Canada Studies, University of Delhi, organized on 30 March 2022, a Distinguished Lecture on the topic, "Artificial Intelligence and Brain Biofields Quantum Computing." The speaker, Prof. Adam W. Skorek, University of Quebec at Trois-Rivières, Canada, shared interesting and useful insights into the area of artificial intelligence and brain biofields. The talk was attended by over 35 participants.

In association with the Department of Electronics, University of Jammu, a one-day webinar on "Next Generation Electronic Devices," was held 22 March 2022. The event included the following talks, which were attended by more than 70 participants including faculty members, research scholars and post graduate students from various institutions across India.

- "Next Generation Miniaturized, Integrated, Self-Powered and



Prof. Michael S. Shur delivering the inaugural talk during the MQ

Deployable Smart Sensors," by Dr. Sanket Goel, Birla Institute of Technology and Science (BITS), Pilani

- "Design techniques and Technologies for Green Electronics," by Dr. Arvind Shaligram, CEO, SPPU Research Park Foundation and Professor Emeritus, Savitribai Phule Pune University, Pune

On 7 April 2022, the Chapter in association with the Department of Electronic Science, University of Delhi South Campus organized a Distinguished Lecture on the topic "Compute-in-Memory Designs: Trends and Prospects," by Prof. Jaydeep P. Kulkarni, University of Texas. The speaker discussed trends in recent compute-in-memory designs and also talked about various trade-offs among bit precision, data converter overheads and computational accuracies. The talk was very insightful and over 62 participants attended it.

In association with the Department of Instrumentation, Shaheed Rajguru College of Applied Sciences for Women, University of Delhi, the chapter organized a virtual training session on "Synopsys TCAD solutions." The training was held on 25 May 2022 and was delivered by Vyom Sharma, Application Engineer, Eigen Technologies Pvt. Ltd. Around 50 participants including undergraduate and postgraduate students, research scholars, and faculty members attended the training session. Mr. Vyom explained the importance of the Sentaurus TCAD tool in the semiconductor industry.

In collaboration with Shaheed Rajguru College of Applied Sciences for Women and IEEE Delhi Section SIGHT, the chapter organized an eight-day hands-on workshop for Saraswati Bal Mandir Senior Secondary School (SBM) students on "Basic and Applied Science." The workshop was held from 31 May to 7 June 2022. Over 32 students of class XI and class XII of the School along with their teachers attended the workshop. The students were given hands-on exposure to the various laboratory equipment and techniques.

A virtual Mini-Colloquium (MQ) on "Advances in III-N Devices and Systems," was held 1–6 June 2022, with a total of 130 participants from India, USA, Bangladesh, and Indonesia.

- An IEEE EDS Distinguished Lecture on "Physics of III-N-based Field-Effect Transistors," by Prof. Michael S. Shur, Rensselaer Polytechnic Institute, Troy, USA
- "Industry Standard ASM-GaN Model for Power and RF Circuit Design," by Prof. Yogesh S. Chauhan, IIT Kanpur, India
- Prof. Xing Zhou, Nanyang Technological University, Singapore, spoke on "Monolithic Co-integration of III-V Materials into Foundry Si-CMOS in a Single Chip for Novel Integrated Circuits"
- "GaN Materials and Devices Technologies for High frequency and High power electronics Applications," Prof. Edward-Yi Chang, NYCU, Taiwan
- The concluding talk on "Directions in III-N Devices and Integration for Wireless Communications" was delivered by Prof. Patrick Fay, University of Notre Dame, USA

The Chapter in association with the Center for Extension and Field Outreach, Delhi Technological University organized a six-day program titled, "Exploring Engineering," which was open to the students of Class-X, XI, XII of Private and Government Schools. This was an initiative to create awareness, passion and interest of the students towards engineering by giving them practical sessions on real life basic engineering applications. The program was aimed at promoting community service and proved to be an excellent step towards social responsibility of academic institutions.

ED Indian Institute of Technology – Roorkee Student Branch Chapter

—by Abhishek Kumar & Ankit Gaurav

The Chapter in association with the Department of Electronics and Communication Engineering, IIT Roorkee, organized a technical seminar on "A low-jitter 2.46–4.92 GHz Two-stage Clock Multiplier in TSMC 65nm CMOS." The distinguished lecture was given by Dr. Saurabh Saxena, Department of Electrical Engineering, IIT Madras. In the talk, a low power and low jitter two-stage 2.46–4.92 GHz clock multiplier using a 38.4 MHz reference clock was proposed. The clock multiplier implements an 8X clock multiplication with a delay-locked loop and an edge

Technical talk at IIT Roorkee on 23 May 2022

combiner in the first stage. Fabricated in a 65 nm CMOS process, the first-stage clock multiplier achieves an integrated jitter 761 fs rms at 307.2MHz while consuming 2.5mW. About 29 students, including 20 IEEE members attended the lecture, along with professors and staff members. The session ended with the presentation of souvenirs to the speaker.

ED Muffakhamjah College of Engineering & Technology Student Branch Chapter

—by Maliah Naaz

The Chapter in collaboration with IEEE CAS MJCET Student Branch organized on 23 June 2022, a technical seminar on "Embedded SIM (ESIM)." The speaker was Syed Hamza Hydri, Senior Manager, Software Development, Core OEM Development Engineering, T-Mobile USA. The session was attended by the undergraduate students of the institution which included 65 IEEE members and 28 non-IEEE member students.

The Chapter also organized a professional development event for the students, which was focused on Career Guidance and Mentoring. The program was held on 13 May 2022. The session was attended by 150 participants, which included 80 IEEE members.

Mr. Syed Hamza Hydri delivering a Technical Talk on "Embedded SIM (ESIM)"

ED IIITDM—Kancheepuram Student Branch Chapter

—by Kumar Prasannajit Pradhan

The Chapter in association with the Department of Electronics and Communication Engineering, Indian Institute of Information Technology Design and Manufacturing (IIITDM) Kancheepuram, organized on 23 March 2022 an IEEE EDS Distinguished Lecture (DL) by Dr. M K Radhakrishnan, Secretary of IEEE Electron Devices Society. The topic was "75 Years of Transistors and Its Impact on Humanity (Birth and Evolution of Semiconductor Devices)." Apart from this, the Chapter organized on 19 April 2022 a technical talk by Prof. Chetan Singh Solanki, IIT Bombay, and Founder of Energy Swaraj Foundation. The topic of the talk was "Climate Change, Energy Swaraj & I."

Another IEEE EDS Distinguished Lecture was organized on 5 May 2022. Prof. Benjamin Iniguez, URV, Tarragona, Spain, addressed the topic "Physics and modeling of Organic and Amorphous Oxide Semiconductor Thin Film Transistors."

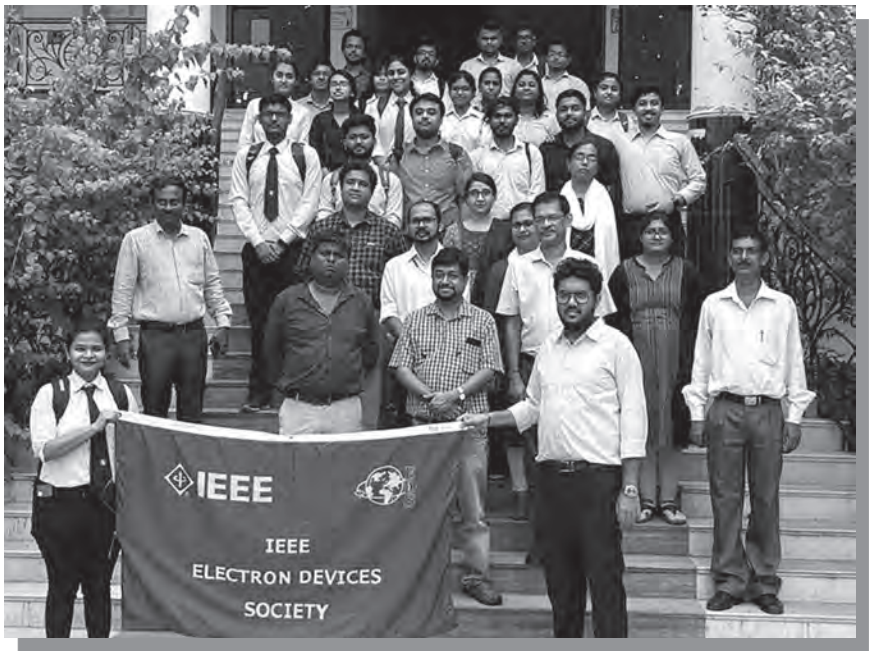
ED Meghnad Saha Institute of Technology Student Branch Chapter

—by Manas Chanda

The Chapter in association with the IEEE Student Branch, IEEE Solid-State Circuits Society, Kolkata Chapter and

Technical talk by Prof. Chetan Singh Solanki delivered on 19 April 2022

EDS student branch chapter student members including Branch Advisor Dr. K P Pradhan and Chair, Mr. L Chandrasekar



Student project contest titled "Project Contest on VLSI Circuits"

the Department of Electronics and Communication Engineering, organized a technical session on the topic, "Prospects of FET-based Neuromorphic Computing". The speaker was Dipanjan Sen, PhD candidate and Graduate Teaching Assistant, Penn State University, USA. A total of 65 attendees participated in the program, out of which 17 were IEEE members.

Another talk was conducted by the Chapter on the topic "Process of Gateway to Intel." Ankita Roy, the alumnus of the Institute, delivered the talk on 21 May 2022. She is currently working as a Platform Architect at Intel.

On 22 May 2022, the Chapter organized a talk on the topic, ''Intel Internship Preparation and Prospects," by Subhendu Manna, RF Software Engineer at Qualcomm, India. About 72 participants (20 IEEE members) were present during the session.

The Chapter organized on 13 June 2022 a student project contest titled "Project Contest on VLSI Circuits." Fifteen project groups, each consisting of two members, participated in the event. The program was attended by 70 students and 11 faculty members.

On 13 June 2022, the Chapter organized a student project contest titled "Project Contest on Device Modeling and Simulation." Seventeen project groups participated in the event. Each team consisted of two or three members from between the final year undergraduate students of ECE, MSIT. The team works were judged by four most senior members of MSIT, who have excelled in this field. The program was attended by 80 students and 11 faculty members.

ED Heritage Institute of Technology Student Branch Chapter and IEEE EDS Center of Excellence

—by Atanu Kundu

The Chapter and the EDS Center of Excellence, in association with the Department of Electronics and Communication Engineering, Heritage Institute of Technology, organized on 13 April 2022 an IEEE EDS Distinguished Lecture by Prof. Durga Misra, Department of Electrical and Computer Engineering, New Jersey Institute of Technology, Newark, USA. The lecture was on the topic "Electron Devices - World of Nanoelectronics 75th Year of Transistors." Prof. Misra discussed the transformation of transistors from planar devices to a three-dimensional device, FinFET. The reliability issues like self-heating and integration of new channel materials like germanium, gate stack formation and scaling of memory devices were also discussed. The talk was attended by 88 participants

Lecture Session by Prof. Souvik Mahapatra

among which 29 were IEEE EDS members.

A technical lecture program by Prof. Souvik Mahapatra, Department of Electrical Engineering, IIT Bombay, India, was organized on 18 April 2022. Prof. Mahapatra delivered the lecture on the topic, "Moore's law - past, present, and future." The talk was attended by 174 participants among which 37 were IEEE EDS members.

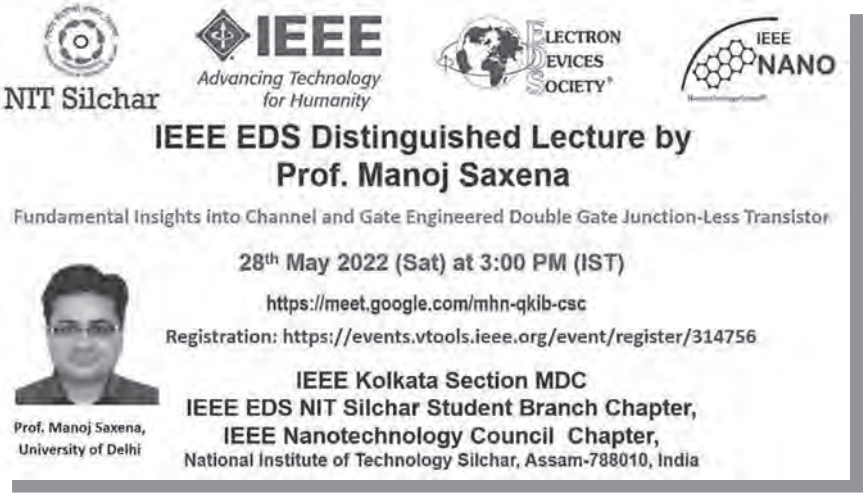
A talk titled "Impact, History and Future of Nanoelectronics" by Prof. Hiroshi Iwai, Prof. Emeritus, Tokyo Institute of Technology, Japan, was organized on 20 May 2022. Prof. Iwai talked about the impact and history of micro/nanoelectronics, and explained the causes of the limit. He also predicted the near future of nanoelectronics in the next 15 years and finally discussed nanoelectronics development for the far future towards the 22nd century and beyond. The webinar was attended by 97 participants among which 29 were IEEE EDS members.

ED National Institute of Technology—Silchar Student Branch Chapter

—by T.R. Lenka

The Chapter organized a distinguished lecture program on "Fundamental Insights into Channel and Gate Engineered Double Gate Junctionless Transistor," by Dr. Manoj Saxena, Department of Electronics, Deen Dayal Upadhyaya College, University of Delhi. This program was also an initiative of IEEE Kolkata Section Membership Development Committee (MDC). Around 50 people including IEEE EDS members attended the talk and interacted with the lecturer.

~Soumya Pandit, Editor



Title slide of the DL by Prof. Manoj Saxena

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EDS MEETINGS CALENDAR

THE COMPLETE EDS CALENDAR CAN BE FOUND AT OUR WEB SITE: HTTP://EDS.IEEE.ORG. PLEASE VISIT.

2022 IEEE International Integrated Reliability Workshop (IIRW)	09 Oct – 14 Oct 2022	South Lake Tahoe, CA
2022 International Semiconductor Conference (CAS)	12 Oct – 14 Oct 2022	Poiana Brasov, Romania
2022 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)	16 Oct – 19 Oct 2022	Phoenix, AZ USA
2022 15th UK-Europe-China Workshop on Millimetre-Waves and Terahertz Technologies (UCMMT)	17 Oct – 19 Oct	Tønsberg, Norway
2022 10th International Symposium on Next-Generation Electronics (ISNE)	22 Oct – 23 Oct 2022	Wuxi, China
2022 14th International Conference on Advanced Semiconductor Devices and Microsystems (ASDAM)	23 Oct – 26 Oct 2022	Smolenice, Slovakia
2022 Symposium on Internet of Things (SIoT)	24 Oct – 28 Oct 2022	Sao Paulo, Brazil
2022 IEEE/ACM International Conference On Computer Aided Design (ICCAD)	29 Oct – 03 Nov 2022	San Diego, CA
2022 IEEE 9th Workshop on Wide Bandgap Power Devices & Applications (WiPDA)	07 Nov – 09 Nov 2022	Redondo Beach, CA

2022 19th International Conference on Electrical Engineering, Computing Science and Automatic Control (CCE)	09 Nov – 11 Nov 2022	Mexico City, Mexico
2022 International EOS/ESD Symposium on Design and System (IEDS)	09 Nov – 11 Nov 2022	Virtual Event
2022 International Siberian Conference on Control and Communications (SIBCON)	17 Nov – 19 Nov 2022	Tomsk, Russia
2022 International Electron Devices Meeting (IEDM)	03 Dec – 07 Dec 2022	San Francisco, CA USA
2022 IEEE 50th Semiconductor Interface Specialists Conference (SISC)	07 Dec – 10 Dec 2022	San Diego, CA USA
2022 IEEE International Conference on Emerging Electronics (ICEE)	11 Dec – 14 Dec 2022	Bangalore, India
2022 International Symposium on Semiconductor Manufacturing (ISSM)	12 Dec – 13 Dec 2022	Tokyo, Japan
2023 Middle East and North Africa Solar Conference (MENA-SC)	05 Feb – 09 Feb 2023	Dubai, United Arab Emirates
2023 7th IEEE Electron Devices Technology & Manufacturing Conference (EDTM)	07 Mar – 10 Mar 2023	Seoul, Korea (South)
2023 IEEE International Reliability Physics Symposium (IRPS)	26 Mar – 30 Mar 2023	Monterey, CA
2023 35th International Conference on Microelectronic Test Structure (ICMTS)	27 Mar – 30 Mar 2023	Tokyo, Japan

Call for Papers
for a Special Issue of
IEEE Transactions on Electron Devices
on

"Wide and Ultrawide Band Gap Semiconductor Devices for RF and Power Applications"

World economy is currently facing two epochal challenges calling for key technological contributions from the RF and power electronic industry: first, a rapid digitalization of industry, jobs and daily life, for which advanced and efficient RF communication systems are required; second, the strive for decarbonization of human activities and the strong fluctuations in the cost of energy, making energy efficiency of electrical power conversion a primary concern.

Both challenges can be addressed through the development of advanced electronic devices, relying on wide and ultrawide bandgap semiconductor materials. In this context, fast RF transistors are being developed to address the challenges of 5G and future 6G networks, where high ft, fmax and high efficiency are needed. In addition, fast and high-breakdown voltage transistors are being developed, for operation in the power conversion field, in the growing markets of electric/hybrid cars, datacenters, renewable energy generation and conversion, and smart grids.

Several materials are currently being explored, from the more mature SiC and GaN, to the more novel ultrawide bandgap semiconductors as Ga_2O_3, Al(Ga)N, BN, and diamond. Despite the impressive development achieved in the past years, several scientific issues still need to be solved, to make these technologies readily available. Challenges include: a) the definition of low-defect growth methods; b) the optimization of device processing and passivation, with the aim of maximizing device performance; c) understanding of the role of defects in limiting the performance (breakdown voltage, leakage current, switching behavior, …) of the devices; d) study of the reliability-limiting mechanisms, that can lead to short-term (e.g. Ron increase, Vth instability) and long-term (e.g. time-dependent breakdown, parametric drift of parameters, …) degradation; e) advanced methodologies for driving and thermal management; f) integration at both circuit and system levels.

This Special Issue of the IEEE Transactions on Electron Devices will report the most advanced and recent results in the field of wide and ultrawide bandgap semiconductor materials and devices, including papers focused on material fabrication, device processing, reliability investigation, device modeling, thermal aspects, and system-related results. Papers must be new and present original material that has not been copyrighted, published or accepted in any other archival publications, that is not currently being considered for publications elsewhere, and that will not be submitted elsewhere while under considerations by the Transactions on Electron Devices.

Topics of interest include, but are not limited to:

Advanced material structures and growth: fundamental material figures of merit; advanced techniques for low-defect material fabrication; link between material properties and device performance; material enhancement techniques to improve quality; new epitaxial structures (e.g. quaternary, Ga2O3, AlNP, …); new substrates (e.g. bulk GaN, AlN, diamond);

Advanced device processing: advanced methodologies for RF and power device processing;

approaches for high-performance lateral and vertical devices; properties and deposition of gate dielectrics and passivation; link between device performance and processing parameters;

RF devices: advanced devices; scaling approaches; dynamic performance optimization; charge trapping and reliability investigation; modeling and simulation;

Power Devices: Vertical and lateral architectures for MOSFETs, HEMTs and MIS-HEMTs, Schottky and pn junction rectifiers, and other device concepts; fabrication and device characterization; designs and device structures for controlling field profiles, edge termination;

Thermal optimization: Thermal characterization and properties of materials and devices; novel approaches to mitigate self-heating in RF and power devices by using wide and ultrawide band gap materials;

Integration: approaches for monolithic and heterogenous integration; integrated circuits based on GaN and other wide band gap materials; integration with Si or other semiconductors for system-on-chip and system-in-package implementations; system level considerations for integrated circuits;

System level aspects: performance of devices based on wide bandgap semiconductors in circuits and systems; thermal and reliability aspects at circuit and system level;

Reliability: reliability-limiting mechanisms; breakdown and TDDB in wide and ultrawide bandgap semiconductors; parametric drift; methodologies for lifetime extrapolation; acceleration factors and parametric drift; models for device degradation.

Submission instructions: Manuscripts should be submitted in a double column format using an IEEE style file. Please visit the following link to download the templates: http://www.ieee.org/publications_standards/publications/authors/author_templates.html In your cover letter, please indicate that your submission is for this special issue.

Submission deadline: August 31, 2023 **Publication date: February 2024**

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EDS Vision, Mission and Field of Interest Statements

Vision Statement
Promoting excellence in the field of electron devices for the benefit of humanity.

Mission Statement
To foster professional growth of its members by satisfying their needs for easy access to and exchange of technical information, publishing, education, and technical recognition and enhancing public visibility in the field of Electron Devices.

EDS Field of Interest
The EDS field-of-interest includes all electron and ion based devices, in their classical or quantum states, using environments and materials in their lowest to highest conducting phase, in simple or engineered assembly, interacting with and delivering photo-electronic, electro-magnetic, electromechanical, electro-thermal, and bio-electronic signals. The Society sponsors and reports on education, research, development and manufacturing aspects and is involved in science, theory, engineering, experimentation, simulation, modeling, design, fabrication, interconnection, reliability of such devices and their applications.