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Contributions Welcome

Readers are encouraged to submit news items concerning the Society and its members. Please send your ideas/articles directly to either the Editor-in-Chief or appropriate Editor. All contact information is listed on the back cover page. Whenever possible, e-mail is the preferred form of submission.

Newsletter Deadlines

<u>Issue</u>	<u>Due Date</u>
January	October 1st
April	January 1st
July	April 1st
October	July 1st

IEEE Electron Devices Society Newsletter

2002 IEEE Bipolar/BiCMOS Circuits and Technology Meeting



Wireless communications is a burgeoning market area and a major driver behind the semiconductor industry, and SiGe BiCMOS and III-V technologies have emerged as the manufacturing processes of choice for many wireless ICs. If you work or are interested in this exciting area, then the IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) is a conference you want to attend.

BCTM has historically been held in Minneapolis, MN. However, due to popular demand the conference is now on the road. In 2002 it will be held 30 September – 1 October at the Doubletree Hotel in Monterey, CA, and in 2003 it will be in Europe, in Toulouse, France. The Doubletree Hotel in Monterey is just a few steps from Fisherman's Wharf, a pleasant stroll from Cannery Row and sandy beaches, and the area is widely known through the works of John Steinbeck. So Monterey is not just a new and exciting place for BCTM; it's a great place to bring the family as well.

The technical program for BCTM consists of one day of short courses (Sunday Sep. 29) given by noted industry experts, and two days of invited and contributed technical presentations. Also for 2002, we will follow a tradition established in 2001 of having a Conference Banquet on the Monday evening. For 2002, this will be at the Monterey Bay Aquarium, a world famous marine institute. The Banquet will actually be a strolling dinner, where you can wander among the exhibits, munch on Californian gourmet specialties, and socialize with other conference attendees.

For the Short Courses this year, we have three noted experts who will present 2-hour courses on various aspects of bipolar devices and technology. Dr. Peter Zampardi of Conexant Systems, Inc., will present a designer's

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Your Comments Solicited

Your comments are most welcome. Please write directly to the Editor-in-Chief of the Newsletter at the address given on the back cover page.

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A Message from the Editor-in-Chief



Ninoslav D. Stojadinovic

It is my privilege to start serving as the Editor-in-Chief (EIC) of the EDS Newsletter in 2002 when we are celebrating the 50th Anniversary of our Society. As the incoming EIC, I would like to address you for the first time and update you on the status of our Newsletter. As you may recall, our new EDS Newsletter was founded in 1994 and Krishna Shenai has served as the founding EIC since then. Over the past seven years, the Newsletter improved dramatically with increased coverage of chapters and reporting of EDS activity all over the world, making it the premier publication for members to keep abreast with society news and events.

After many distinguished years of service, Krishna Shenai has stepped down because of other commitments, leaving me a difficult task to maintain the level of the Newsletter and try improving it further, if that is at all possible. Besides Krishna, Mikael Ostling, Stephen Parke, S.C. Sun, Chuck Yarlning, and Paul Yu have also departed from the Editorial Board this year. On behalf of Editorial Board, I wish them the best, and our gratitude for a job well done. On the other hand, I look forward to working with the current members of the Editorial Board, including four newly appointed regional editors (Alexander Gridchin, Andrzej Napieralski, Murty Polavarapu, and Sunit Tyagi), whose bios follow.



Alexander V. Gridchin

Alexander V. Gridchin was born in Novosibirsk, Russia, in 1969. He received the M.Sc. and Ph.D. degrees in electrical engineering from the Novosibirsk State Technical University (NSTU) in 1991 and 1999, respectively. His Ph.D. thesis was devoted to the developing of theoretical base for the designing of the four-terminal silicon piezotransducers with special form of the current spread region. In 1996 he joined the Department of Applied and Theoretical Physics at NSTU, where he is currently holding a position of an associate professor. He was a co-recipient of the President of the Russian Federation annual grant in 1996.

In 1999, he founded the IEEE NSTU Student Branch, and

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EDS ADCOM ELECTED MEMBERS-AT-LARGE

Term Expires:

2002

C. L. Claeys (1)
J. A. Dayton, Jr. (1)
M. Fukuma (1)
K. M. Lau (1)
K. Lee (1)
M. L. Ostling (1)
D. L. Pulfrey (1)
K. Shenai (2)

2003

I. Adesida (2)
T. Hiramoto (1)
L. Lunardi (1)
A. A. Santos (2)
S. C. Sun (2)
H. S. P. Wong (1)
P. K. L. Yu (2)

*2004

M. Estrada del Cueto (1)
K. F. Galloway (2)
S. J. Hillenius (2)
C. Jagadish (2)
J. K. O. Sin (1)
R. Singh (2)
N.D. Stojadinovic (1)

Number in parenthesis represents term.

* Members elected 12/01

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Upcoming Technical Meetings

IEEE Bipolar/BiCMOS

(continued from page 1)

practical view of Si/SiGe, GaAs, and InP bipolar junction transistor (BJT) device technologies. This will include analysis of the device physics of BJTs in various technologies and the impact on the practical realizations of commercial power amplifiers. Prof. Torkel Arnborg of Ericsson Microelectronics will present a course on linearity modeling and simulation for BiCMOS devices. The need for linearity modeling is increasing, as more RF/analog circuit applications become suitable for implementation in semiconductor technology. Prof. Arnborg will focus on how distortion is created due to non-linearity, how it differs in bipolar vs. MOS devices, and what is required for a successful modeling and simulation. The third course, by Prof. Lode Vandamme of T. U. Delft, will cover noise in BJTs, a topic critical to wireless communications.

The technical part of the conference opens on Monday Sep. 30, with a keynote address by Professor Herbert Kroemer of the University of California, Santa Barbara. Prof. Kroemer, 2000 Nobel Physics Laureate, is the founding father of semiconductor heterostructures, and he will present a fascinating discourse on the history and technical achievements of heterostructure devices.

Dr. Michael Marcus of the US Federal Communications Commission will present the luncheon speech, always a conference favorite, "The Search for Captain Midnight." In April 1986, HBO viewers were surprised to see the programming interrupted by a text message criticizing HBO's recent price change. The message was a result of the first deliberate satellite jamming in history. The only evidence this crime left was a few feet of consumer grade videotape. Yet within a month FCC investigators, using what Time magazine called "high-tech, Holmesian detective work" unmasked the perpetrator. About a year later there was a similar jamming incident on the Playboy Channel where the source was also identified with a month. (Whether or not one approves of the content Playboy was sending, satellite jamming can damage

the satellite transponder and Congress made such action a felony.) Since the "Playboy perp" didn't confess as in the first case, it was necessary to prepare an ironclad technical analysis for the ultimate successful prosecution. This talk will describe the unprecedented analysis that led to the conclusion of both cases, including G-rated versions of the actual incidents.

The technical program includes sessions on bipolar/BiCMOS process technology, power devices, device physics, modeling and simulation, analog circuit design, and RF circuit design. Each technical content area includes a double-length invited talk on an area of present interest. Dr. Chih-Hsien Lin of the Taiwan Semiconductor Manufacturing Corporation will present "State-of-the-Art RF/Analog Foundry Technology." Dr. Richard Williams of Analogic Technologies will talk about simulation of power devices. Prof. Achim Burghartz of the Delft University of Technology will present "Substrate Options and Add-On Process Modules for Monolithic RF Silicon Technology." Dr. Pat Drennan of Motorola, Inc., will talk about accurate modeling of parametric mismatch, a leading cause of yield loss in analog/RF ICs. Dr. Roy Gosser of Analog Devices, Inc., will address relating device parameters and figures-of-merit to real performance of high speed circuits, a topic that will undoubtedly trigger much discussion. And Dr. Tallis Blalack of Simplex Solutions will address

substrate and cross talk modeling a simulation, which is an area of critical concern for analog and RF ICs.

On the morning of Tuesday, October 1, there will be a Special Session on Emerging Technologies. There will be four invited presentations in this session. Dr. Jamal Ramdani from Motorola Inc. will describe their recently announced GaAs-on-Si technology. Dr. Eugenio Cantatore from Philips Natlab will give a talk on circuit and technology developments in polymer electronics, a relatively new and exciting field, with applications from photonics to displays. Dr. Berinder Brar from Rockwell Scientific will outline the present state-of-the-art and project future trends in InP bipolar technology. Also, Dr. Dieter Knoll from Germany's IHP will describe the advantages of carbon-doped SiGe HBTs within the context of a BiCMOS technology for RF applications.

So between the locations, the banquet at the Monterey Bay Aquarium, and the technical presentations BCTM2002 is a must for those working in bipolar/BiCMOS technologies. For more information contact Jan Jopke, CCS Associates, Conference Manager, E-mail: CCS@mn.rr.com 6611 Countryside Drive, Eden Prairie, MN 55346, USA, TEL 612-934-5082, FAX 612-934-6741

See you there

Colin McAndrew
Technical Program Chair
Motorola
Tempe, AZ, USA

2002 IEEE Intersociety Energy Conversion Engineering Conference (IECEC)

Sponsored by the IEEE Electron Devices Society (EDS), the 37th Annual IEEE Intersociety Energy Conversion Engineering Conference (IECEC 2002) is being held in Washington, DC. The dates are July 28 through August 1, 2002, and the location is the Omni Shoreham Hotel. Mark your calendars

and plan to attend this unique, interdisciplinary energy forum where interactive presentations and discussions span the gamut of energy technology, systems, environmental issues, and policy.

The decade of the nineties was a period when energy issues were relegated to a relatively low profile status, but recent

international events have sounded a warning that this attitude cannot continue. The program for IECEC 2002 is a call to action in the energy field, and through plenary sessions, panels, and contributed papers will give attendees a broad and up-to-date exposure to energy issues, as well as reporting the latest developments in energy technology and systems.

This broad scope results from the technical co-sponsorship with IEEE-EDS by five leading societies: The American Institute of Chemical Engineers (AIChE); the American Nuclear Society (ANS); the Society of Automotive Engineers (SAE); the American Institute of Aeronautics and Astronautics (AIAA); and the American Society of Mechanical Engineers (ASME). The international aspects are well represented through overseas coordinators, and by the Japan Engineering Society as a Cooperating Society.

Each year the IECEC has chosen a subtitle to establish a theme; this year the tradition is continued with *Powering the World and Beyond*. This was selected in recognition of the power needs of both terrestrial and aerospace systems, the energy resources available to realize them, and the environmental consequences of their realization. The basic premise on which the IECEC series was founded nearly forty years ago was then, and remains even more applicable today, that the physical, chemical, and engineering principles on which power systems are based are not the prerogative of any single society. The IECEC "Founding Fathers" set out to create a truly interdisciplinary forum to present and discuss all aspects of energy conversion advanced power systems and technology, and related policy and environmental issues.

The IECEC 2002 technical program extends over the four days commencing Monday July 29th and will comprise three major elements. The first is a series of three stand-alone Plenary Sessions, one each day beginning July 29th. The topics will be: The Impact of 9-11 on Energy Availability and Utilization; The Electric Utility Industry in Technical and Structural Transition; and Whither Aerospace Power in the 21st Century?

The second element, panels on current



high visibility topics is, as is to expected, still in the formative process. Tentative examples include: Can Truly Clean Combustion be achieved?; Realizing Power Generation from Nuclear Fission; Looking Back - It Seemed to be a Good Idea at the Time! and The Hydrogen Economy and Fuel Cells.

A wide-ranging list of approximately 50 sessions of contributed papers will complete the program. They will be arranged in sequences drawn from the following topical areas:

Aerospace Power:

Overall Systems and Performance;
Power Systems; Arrays; Storage;
Technology; Analysis and Simulation;
Terrestrial Applications;

Thermal Management

Conversion Technologies:

Combustion, Thermodynamic Converters; Fuel Cells; Photovoltaics;
Wave and Tidal Power, CFD Analysis

Systems and Renewable Sources:

Primary Systems; Biomass; Electrical Generation, Transmission and Distribution; Simulation and Modeling;

Environmental and Policy Impacts:

Electric Vehicles; Energy Efficiency and the Environment; Deregulation; Developing Countries; Public Policy.

Space does not permit a full listing of the specific session topics. Visit the Conference website www.iecec2002.com and click on Program to get full details which will be updated until IECEC 2002 opens. The conference proceedings, given on a CD to all registrants, will contain all papers (except as stated below).

For authors who would like to con-

tribute papers, please refer to the instructions on the web site. Although the official deadline has passed, late abstracts will be evaluated and, if acceptable, may be presented provided that the final manuscript is received by June 1 for inclusion in the proceedings or multiple copies are brought to the conference.

The highlight of the Conference will be the Keynote Address by a prominent player in the energy world. Again, visit the website to learn who has accepted this role and the speaker's topic.

Associated with IECEC 2002 will be a Workshop on Aerospace Power organized by AIAA and held on Saturday, July 27th. The website has full information, including the registration procedure.

The social program will open with a reception on Sunday, July 28th, and will organize or arrange visits to the many cultural and tourist attractions in the Washington, DC area. The Omni Shoreham Hotel overlooks Rock Creek Park (a secluded river in downtown Washington), and has excellent facilities for relaxation and recreation. The Woodley Park - Zoo Metro station is immediately adjacent, so that travel connections to all three area airports, as well as metropolitan Washington, are easy and convenient, as described on the website. The website has online Conference Registration and the full Omni Shoreham Hotel reservation procedure.

As a major center of energy activities and the site of past IECECs, Washington, DC needs no introduction as a great venue for the IECEC. All concerned with putting together the 37th IECEC look forward to welcoming you on July 28th to this unique annual energy event. For any assistance that you may need to make this happen, please feel free to contact the Conference Manager, Ms Eleanor B. Dicks, at iecec2002ebdicks@aol.com.

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Edward S. Pierson
Program Chair
Purdue University
Hammond, IN, USA

2002 IEEE Lester Eastman Conference on High Performance Devices



The IEEE Lester Eastman Conference on High Performance Devices will be held August 6-8 (Tuesday-Thursday), 2002 in

Newark, Delaware. This biennial conference, previously called the IEEE/Cornell University Conference on High Performance Devices, will continue its tradition of highlighting important developments in high-speed semiconductor devices, optoelectronics and novel concepts. This year the venue for the conference is the University of Delaware campus, located in Newark, Delaware. Newark is a classic college town in northwestern New Castle County, an area of beautiful rolling hills tucked away in the urban Eastern corridor, for outstanding cultural and recreational opportunities. It is easily accessible by air, bus and train, and is a drive of a half-day or less from most major cities in the Northeast.

The following three topical areas comprise the scope of the Conference and papers:

- Microwave and millimeter wave devices and circuits
- Optoelectronic devices and circuits
- Speculative materials, devices, and circuits concepts

Topics of interest within these areas include, but are not restricted to:

- Novel materials technologies and devices
- Wide bandgap materials and devices
- High speed and microwave optoelectronics
- Light sources and detectors
- Si-based heterostructures
- Terahertz sources and detectors
- High speed measurement techniques
- Sb-based devices and circuits
- High power and high speed packaging
- Speculative concepts
- Heterogeneous integration for increased functionality
- Microwave and millimeter wave integrated circuits

- Nanometer fabrication and self-assembly techniques
- Molecular Electronics
- Nanoelectronics
- RF MEMS technology for >1 GHz

This year the conference will have the theme of "Over 30 years of Compound Semiconductor Device History". Celebrating the new conference name, a plenary session is planned in honor of Professor Lester Eastman, a seminal figure for this conference and the field of compound semiconductor devices. Technical thrust areas will include: wide bandgap materials and devices; narrow bandgap, low power materials and devices; and heterogeneous integration of dissimilar materials and devices. Papers are solicited covering the physics and performance of devices and circuits for high speed/frequency, high and low power devices, and optoelectronics. There will be invited papers in the key areas. Papers that emphasize innovative device concepts and physical phenomena leading to new devices are particularly encouraged. The proceedings of the conference will be published.

In order to encourage student participation, limited financial assistance for travel is available to first-named student authors who are presenting papers. This assistance should be requested when the

abstract is submitted. Prospective authors are invited to submit a 300-word abstract plus one page of accompanying figures by May 1, 2002. The conference is sponsored by: the Electron Device Society (EDS) of the IEEE, in cooperation with the Microwave Theory And Techniques Society of the IEEE.

The planned dinner/social activity will be held at the Hagley, a renowned outdoor museum located along the Brandywine River on the site of the first du Pont powder works. The Hagley includes the first du Pont family home and garden in America, built by E. I. du Pont in 1803, a Blacksmith Hill workers' community, powder yards, and a nineteenth-century machine shop.

The University of Delaware campus in Newark, Delaware is conveniently located, a 1-hour drive from Philadelphia and 2 hours from Washington, DC (see <http://www.udel.edu>). Both individual and family accommodations will be available in area motels. Dormitory rooms are also available. For more information, see the conference web page at: <http://nina.ecse.rpi.edu/shur/Eastman-Conference/>

*James Kolodzey
University of Delaware
Newark, DE, USA*



2002 IEEE International SOI Conference (SOI)

The 28th Annual IEEE International SOI Conference, the premier conference dedicated to current trends in Silicon-on-Insulator technology, will be held October 7-10, 2002 at the Williamsburg Lodge, Williamsburg, Virginia. A one-day Tutorial Short Course will precede the conference on Monday, October 7th 2002.

The SOI conference was established with the support of IEEE to provide a forum for open discussion in all areas of silicon-on-insulator technologies and their applications. Interest on SOI technology is currently increasing rapidly and most major semiconductor companies are already using and/or developing SOI based processes for high performance and low power chips. The increasing demand for this technology brings the industry together to discuss new accomplishments, gains, and future directions. Original papers presenting new developments in the industry will be presented at the conference.

The 2002 SOI International Conference will begin with a half-day plenary session followed by two days of oral sessions, a poster session and a closing recent news session on Thursday. Session topics will focus on basic materials research, device research, circuit development (both special to SOI and improvements to bulk designs fabricated on SOI) and applications and uses. Rump sessions will be held on Wednesday evening, October 9. These sessions encourage attendees to share their opinions and expertise on the chosen topics of discussion.

Additionally, a materials and equipment exhibition relating to SOI technology will be held concurrently with the conference. Participants will have the opportunity to visit the exhibit area to see what's new in SOI. Overall, the 2002 SOI International Conference offers attendees a broad spectrum of information, opportunities for discussion with one's peers, and is a must for engineers both experts and those seeking a comprehensive introduction in SOI technology.

The 2002 SOI Conference seeks papers on a wide range of SOI technology including:



- SOI material science/modification, material characterization, and manufacture
- SOI device physics and modeling
- SOI circuit applications (high-performance microprocessors, SRAM, ASIC, low-power, high-voltage, RF, analog, Mixed Mode, etc.)
- Double Gate/Vertical Channel Structures; Other Novel Structures
- New SOI structures, Circuits, and applications (3D integration, displays, micro actuators - MEMS, micro sensors, Drop-in RAM, etc.)
- SOI reliability issues (hot-carrier effects, radiation effects, high-temperature effects, etc.)
- Manufacturability and process integration of SOI devices and circuits
- Alternate silicon-on-insulator material.

At the conclusion of the Conference, a Best Paper Award will be presented. Abstracts for SOI 2002 Conference should be submitted electronically to www.soiconference.org by May 10, 2002. Late newspapers with exceptional merit will be considered for the Late News session if submitted on or before August 15, 2002.

Once again, the popular One-Day Tutorial Short Course will be offered preceding the 2002 SOI International Conference. Tutorial Short Course instructors have many years experience in the field of silicon-on-insulator technology. The course is intended to educate attendees in detail about current trends and issues in the SOI industry. The SOI 2002 Tutorial Short Course will focus on circuit design issues, circuit design tools and device models. Participants will receive copies of all visual presentations.

The SOI Conference is held annually throughout the United States. This year's conference is being held at Williamsburg Lodge, Williamsburg, Virginia. The conference is guided by an international steering committee and a technical committee comprised of members of the society throughout the world. The 2002 conference is organized by: General Chair, Dimitris E. Ioannou (George Mason University); Technical Program Chair, Mike Liu (Honeywell Solid State Electronics Ctr.); Local Arrangements Chair, Mike Mendicino (Motorola); Treasurer and Registration Chair, James A. Burns (MIT/Lincoln Lab); Rump and Poster Chair, Olivier Fainot (CEA-LETI); and Short Course Chair, Christophe Tretz (AMD).

The Williamsburg Lodge is designed to allow the perfect blend of work, rest and recreation. Work in meeting facilities designed to compliment any conference, rest in comfortable guestrooms decorated with an American folk art theme, and enjoy an amazing array of recreational opportunities in the immediate area. The Williamsburg Lodge offers a complete fitness center, indoor and outdoors pools, and massages therapy. The award-winning Golden Horseshoe Golf Courses offer 45 holes of championship golf. There are tennis courts with resident tennis professionals who offer complimentary clinics to guests. There is lawn bowling, badminton, table tennis, a putting green, horseshoes, miniature golf, biking, jogging courses, and much more.

If this is not enough, step out of the Lodge and into Historic Williamsburg, 173 acres of "Living History". This recreated 18th century town of Williamsburg has homes and trade sites restored or rebuilt as accurately as possible, using existing foundations and appropriate materials. From 1699 to 1780 Williamsburg was the capital of the colony of Virginia. Here Thomas Jefferson studied law, and later he, George Washington and Patrick Henry plotted America's freedom. Visit with trades' people and town folk as they go about their 18th century day making shoes, furniture, buckets and clothes while catching up on the latest

gossip or political news. You could bump into Thomas Jefferson, Martha Washington or Patrick Henry and get to know them. Watch as the British army marches through town or fall into ranks and see what it's like to drill with the American militia. Even the animals are true to the 18th century. Spend the day walking through the pages of an American history book.

For more information about the area

you can call the Williamsburg Visitors Bureau at (800) 368-6511 or visit their web site: www.visitwilliamsburg.com. You can fax them at (757) 253-1397 or write to them at P.O. Box 3585, Williamsburg, VA 23187.

You may contact the 2002 IEEE International SOI Conference for additional information as follows: c/o BACM, 520 Washington Blvd., #350, Marina del Rey, CA 90292, Tel: 310-305-7885; Fax:

310-305-1038; Email: bacm@attbi.com or on the World Wide Web at <http://www.soiconference.org>.

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Message from the Editor

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since then has been serving as its Counselor. In the period 1999-2001, he served as a member of the IEEE R8 EDS Regions/Chapters subcommittee. He is founder and Vice-chair of the Siberian Russian Workshops and Tutorials on Electron Devices and Materials (EDM), which are being held annually since 2000. He has contributed considerably to the founding of the LEOS Novosibirsk Chapter and four NSTU Student Branch chapters (EDS, SSCS, LEOS, and PELS). He is also assisting in managing the MTT/ED/CPMT/COM/SSC Novosibirsk Chapter. He is a Distinguished Lecturer of EDS.



Andrzej Napieralski

Andrzej Napieralski was born in Lodz, Poland, in 1950. He received the M.Sc. and Ph.D. degrees from the Technical University of Lodz in 1973 and 1977, respectively. He also received the D.Sc. degree in electronics from the Warsaw University of Technology (Poland), and in microelectronics from the Université de Paul Sabatié (France), both in 1989. From 1973 to 1978, he was with the Institute of Electronics, Technical University of Lodz. In

1983, he joined LAAS-CNRS in Toulouse, France, where he worked on gold doping influence on the parameters of high-power semiconductor devices. In the period 1985-1991, he was a member of the research team on power devices at LAAS-CNRS, Toulouse and Visiting Professor at the Institut National des Sciences Appliquées de Toulouse. Since October 1991, he has been a Professor at the Technical University of Lodz. From 1992 to 1996, he was the Vice-Director of the Institute of Electronics, and since 1996 he has been Director of the Department of Microelectronics and Computer Science.

He authored over 440 publications: 4 books, 20 textbooks for students, 14 chapters in books, 46 papers in scientific journals, 279 papers in conference proceedings, two patents, six expertise and 70 scientific reports. He was the editor of 9 conference proceedings and one scientific journal. He supervised 14 Ph.D. and 108 M.Sc. theses.

He participated in seven TEMPUS programs (in three as the coordinator and contractor), two INCO-COPERNICUS, one ESPRIT, two NATO projects, and 27 National Research Grants (in 14 as the head of the project). Currently, he participates in two projects of the fifth European Program for Research and Technological Development. He is a member of many Scientific Committees of National and International Conferences, and for the last nine years he has been the General Chairman of the

International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES). He is the member of the Electronic and Telecommunication Committee of the Polish Academy of Sciences and the Vice-Chairmen of Microelectronics section of this Committee. He is a Senior Member of IEEE and the Chair of IEEE ED Poland Chapter.



Murty S. Polavarapu

Murty S. Polavarapu is the Manager of Technology Integration at Dominion Semiconductor in Manassas, VA. He is a Senior Member of IEEE and is also the Chair of Northern Virginia Section ED Chapter. He is also the Treasurer of IEEE Northern Virginia Section and Vice Chair of the Northern Virginia Chapter of Society for Social Implications of Technology. Over the last nineteen years, he has worked on all facets of semiconductor technology with a special focus on

developing and manufacturing advanced CMOS memories and logic products. His current activities are focused on introducing advanced DRAM products into manufacturing. He holds M.Sc. degrees in physics from India, electrical engineering from Howard University, and management of technology from the University of Pennsylvania. Mr. Polavarapu is a recipient of the IEEE Third Millennium Medal. He has also received Outstanding Technical Achievement and Invention Awards from IBM and President's Award from Dominion Semiconductor.



Sunit Tyagi

Sunit Tyagi received his B. Tech. degree in electrical engineering from IIT, Mumbai, India, in 1984. He worked for a year with Schlumberger Wire line Services. He received his M.Sc. and Ph.D. degrees from ECSE department at Rensselaer in 1987 and 1991, respectively. His work there focused on II-VI and III-V compound semiconductor growth using MOCVD and characterization of electrical properties for use in solar cell devices. Since 1991, he has been with

Intel Corp. working on development of high performance logic CMOS processes. He has been active in IEEE since 1980, and was the Chair of the IIT Mumbai student chapter in the period 1983-1984. Dr. Tyagi has been active member of EDS Ad-Com Regions/Chapters Committee and EDS Educational Committee since 2000.

Ninoslav Stojadinovic
EDS Newsletter Editor-in-Chief
University of Nis
Nis, Yugoslavia

Society News

Announcement of Newly Elected Officers and AdCom Members

On December 2, 2001, the EDS AdCom held its annual election of officers and members-at-large. The following are the results of the election and brief biographies of the individuals elected.

Officers

The following individuals were elected as officers for a one-year term beginning 1/1/2002:



Steven J. Hillenius

Steven J. Hillenius (*President*) is the Director of a research and development department at Agere Systems formerly Bell Laboratories/Lucent Technologies. His department's research is in the ultimate device limitations of silicon technology and new device structures and applications. Dr. Hillenius has nine patents in the area of semiconductor device structures. He has published over 60 articles on semiconductor devices and processing. In 1996, he was elected to the grade of IEEE Fellow. He has held many responsibilities within the IEEE Electron Devices Society, most recently including President for 2002-2003. He was the IEEE Electron Devices Society Publications Chair from 1992-2000; and in 1996, he was General Chairman of the International Electron Devices Meeting (IEDM). He received the Ph.D. degree from the University of Virginia, Charlottesville, Va. in 1979, in physics. He was an Assistant Professor of physics at the University of Virginia from 1978 to 1981, where his research involved low temperature solid-state physics. In January of 1981

until present, he has worked for Bell Laboratories/Agere Systems.



Hiroshi Iwai

Hiroshi Iwai (*Vice President*) is a professor of Frontier Collaborative Research Center, Tokyo Institute of

Technology (TIT). Before joining TIT, he worked at Toshiba Corporation for 26 years, having developed advanced Si device technologies. He was also a visiting scholar at Stanford in 1983 and 84. He received the B.E. and Ph.D. degrees in electrical engineering from the University of Tokyo, Japan in 1972 and 1992, respectively.

He is currently the EDS Regions/Chapters Committee Chair. He has served for many years with IEEE/EDS, as an Elected AdCom member, an editor of the EDS Newsletter, and the chair of a number of EDS conferences.



Paul K. L. Yu

Paul K. L. Yu (*Treasurer*) received his Ph.D. from the California Institute of Technology in 1983. In 1983, he joined the faculty of the Department of Electrical and Computer Engineering at the University of California at San Diego (UCSD) where he has been a professor since 1993. At UCSD, he conducts research in materials and device for fiber optics and optoelectronics applications. He is a Senior Member of IEEE, a Distinguished Lecturer of the EDS and a member of OSA. Currently, his research focus is in solving problems for microwave photonics systems. He has published more than 100 papers in the area of photonics.



John K. Lowell

John K. Lowell (*Secretary*) received the Ph.D. degree in Applied Physics from the University of London. He has held technical and managerial assignments for United Technologies, Northern Telecom, Mostek, Texas Instruments, British Telecom/Dupont, AMD, Applied Materials, Oracle and most recently PDF Solutions. He has also been a Professor at Texas Tech University and in the University of Texas system,

and held Consulting Professorships at other universities in addition to being a Visiting Scholar at the NSF Center for the Synthesis, Growth and Characterization of Electronic Materials at the University of Texas at Austin.

Dr. Lowell is a Senior Member of the IEEE, a Distinguished Lecturer of the EDS and has held AdCom-level positions previously within the LEO and CAS societies. For fifteen years, he was also the Associate Editor-in-Chief of the IEEE Division I Circuits & Devices Magazine, and was its Guest Editor twice.

AdCom Members-at-Large

A total of seven persons were elected to three-year terms (2002-2004) as members-at-large of the EDS AdCom. Four of the seven individuals were re-elected for a second term, while the other three were first-time electees. The backgrounds of the electees span a wide range of professional and technical interests.

Second Term Electees



Kenneth F. Galloway

Kenneth F. Galloway is Dean of the School of Engineering and a Professor of Electrical Engineering at Vanderbilt University. His research and teaching activities at Vanderbilt center on solid-state devices and semiconductor technology with an emphasis on radiation effects in solid-state devices.

Dr. Galloway earned his Ph.D. from the University of South Carolina and has held professional appointments with Indiana University, the U.S. Navy, the National Institute of Standards and Technology, the University of Maryland, and the University of Arizona. He came to Vanderbilt as Dean in 1996.

He is a Fellow of the American Association for the Advancement of Science (AAAS) and a Fellow of the Institute for Electrical and Electronics Engineers (IEEE).

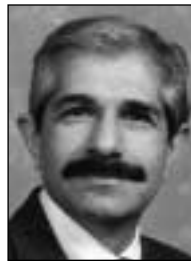
Steven J. Hillenius (See photo and biography in Officers Section of this article)

Chennupati Jagadish is a Professor and Head of the Semiconductor Optoelectronics and Nanotechnology Group in the Research School of Physical Sciences and Engineering at the Australian National University. He received the Ph.D. degree from the University of Delhi in Semiconductor Physics in 1986. He was a Lecturer in Electronics and Physics at S.V. College, New Delhi during 1985-88 and a Research Associate at Queen's University, Canada during 1988-90. In 1990, he joined the Australian National University where he is a Professor. He is a Fellow of the IEEE, a Distinguished Lecturer of EDS and a winner of the IEEE Third Millennium Medal. His research interests are in semiconductor optoelectronics and nanotechnology. He has published more than 220 journal papers and about 120 conference papers, co-authored a book and edited 3 conference proceedings. He is also Chair of IEEE Optoelectronic Device Technical Committee of EDS.



Chennupati Jagadish

Rajendra Singh is D. Houser Banks Professor in the Department of Electrical and Computer Engineering and the Director of the Center for Silicon Nanoelectronics at Clemson University. He is editor of *IEEE Transactions on Electron Devices*, member of the Steering Committee of *IEEE Transactions of Semiconductor Manufacturing*,



Rajendra Singh

chair of IEEE EDS Semiconductor Manufacturing Technical committee and member of IEEE EDS Nanotechnology Technical committee. He is the author of over 250 papers in the field of rapid thermal processing, semiconductor manufacturing, solar cells and nanotechnology. He is a Fellow of IEEE, the Society of Optical Science and Engineering (SPIE), American Association of Advancement of Science (AAAS) and ASM International, the materials information society.

First-Time Electees

Magali Estrada Del Cueto is a Titular Professor at the Section of Solid State Electronics of the Department of Electrical Engineering at CINVESTAV-IPN, Mexico, D.F. She received the Ph. D. at NW Leningrad Polytechnic Institute in 1977. Since 1966, she is engaged with research and development in the field of microelectronics. She was a Titular Professor at the University of Havana until 1994, holds 3 patents, author of one textbook and over 50 published articles. She has received several awards, serves as an EDS Distinguished Lecturer and is chair of the Region 9 EDS Regions/ Chapters Subcommittee.



Magali Estrada Del Cueto



Johnny K.O. Sin

Johnny K.O. Sin received his PhD degree in electrical engineering from the University of Toronto, Canada, in 1988. He joined Philips Laboratories, New York, upon the completion

of his PhD studies, and was a senior member of the research staff there from 1988-1991. Dr. Sin joined the Department of Electrical and Electronic Engineering, the Hong Kong University of Science and Technology, Hong Kong, in August 1991, and is currently a professor. His research interests lie in the general area of devices and technology for system-on-a-chip applications. He has published over 170 journal and conference papers and holds seven patents.

Prof. Sin is an Editor of *IEEE Electron Device Letters*. He served as technical committee member of the International Symposium on Power Semiconductor Devices and IC's (ISPSD) and the International Conference on Microelectronics Test Structures (ICMTS). He is a senior member of IEEE.

Ninoslav D. Stojadinovic is the head of the Department of Microelectronics, Faculty of Electronic Engineering, University of Nis, Yugoslavia. He received the Ph.D. degree in electrical engineering from the University of Nis in 1980. His current research interest involves physics, modeling, characterization, and reliability of MOS devices and circuits. He is author of 58 papers in international journals and 120 conference papers.

Dr. Stojadinovic is Editor-in-Chief of *Microelectronics Reliability* journal and the *IEEE EDS Newsletter*. He is a distinguished lecturer of the IEEE EDS, Chairman of the IEEE International Conference on Microelectronics (MIEL), President of the Yugoslavia IEEE Section and Chair of the Yugoslavia IEEE ED/SSC Chapter.



Ninoslav D. Stojadinovic

EDS Chapter Subsidies for 2003

Requests for subsidies from EDS chapters are due on 1 September 2002. Last year, the EDS AdCom awarded funding to 58 chapters, with most amounts primarily ranging from US\$250 to US\$1,000. In June, Chapter Chairs were sent an e-mail notifying them of the current funding cycle. A list of guidelines

was included with each e-mail. In general, activities which are considered fundable include, but are not limited to, membership promotion travel allowances for invited speakers to chapter events, and support for student activities at local institutions. Subsidy requests should be sent via e-mail, fax or mail to the EDS Administrator, Laura J. Riello. Her contact information is the same as W.F. Van Der Vorst's, included on page 2. Prior to the submission of the subsidy request, the

Chapter Chair must submit a chapter activity report to its respective SRC Chair and EDS Newsletter Editor by July 1. This report should include a general summary of chapter activities (one to two pages) for the prior July 1st – June 30th period. You must also attach a copy of the activity report to your chapter subsidy request. Final decisions concerning subsidies will be made by the EDS Regions/Chapters Committee in early November. Subsidy checks will be issued by late January.

Call For Nominations — EDS AdCom

The Electron Devices Society of the IEEE invites the submission of nominations for election to its Administrative Committee (AdCom). Presently, the AdCom meets twice per year and is composed of 22 members. Eight members will be elected this year for a term of three years, and a maximum of two consecutive terms is allowed. In 2002, the election will be held after the AdCom meeting on Sunday, 8 December. Electees begin their term in office on 1 January 2003.

Nominees are being sought to fill

the slate of candidates. Nominees may be self-nominated, or may be nominated by another person; in the latter case, the nominee must have been contacted and have agreed to serve if elected. Any member of EDS in good standing is eligible to be nominated. As another condition for nomination and election, a nominee must be willing to attend the two annual AdCom meetings.

Please send your nominee's name, address, and supporting information to the EDS Executive Office Administrator, Laura J. Riello

in time to be received by the deadline of **15 October 2002**. Her contact information is the same as W.F. Van Der Vort's, included on page 2. It is very desirable that submissions include a biographical summary in a standard two-page format. The EDS Executive Office can provide you with an example of the format. If you have any questions regarding the nomination requirements or process, feel free to contact the Nominations and Elections Chair, Cary Y. Yang (see page 2 for contact information).

EDS Compact Modeling Technical Committee Report

Narain Arora



The IEEE Compact Modeling Technical Committee, as a part of the Electron Device Society (EDS), was first set up in February 2001, with the aim to objectively identify, examine, and evaluate current models for active and passive components used for circuit simulation. The emphasis is on models for the components/interconnects required for chip design, and therefore this committee will attempt to work closely with the Solid-State Circuits Society.

Dr. Narain Arora chairs the committee. It is a non-voting Ex-Officio AdCom member position with a two-year renewable term. The committee, with diversified membership representing a variety of views, has 22 members from Europe, Japan, and North America. There are two EDS AdCom meetings a year, with one meeting always being held in conjunction with IEDM. The other AdCom meeting is normally held sometime in the April-June time period in conjunction with another EDS sponsored conference.

The first meeting of the committee was held in June 2001 in Singapore and was attended by five committee members. The main topic of the discussion was how to promote interaction among compact model (CM) developers, technology developers, and circuit designers. For developing best compact models for chip design, researchers in all the three areas are required to interact. It was decided that this committee needs to reach out to industry and the chip design community, so that model development is not done in isolation. Dr. Xing Zhou, one of the committee members, graciously agreed to establish a web site for the committee. The web site established in July 2001, is located at <http://www.ntu.edu.sg/home/exzhou/CM> and included the names of all committee members. In addition, it has links to many important societies of interest to model developers and users. Any comments/ideas/suggestions related to the field of VLSI device/circuit/interconnect compact modeling are welcome!

The second meeting was held last December (2001) during IEDM at Washington DC. Though only nine committee members attended the meeting, it was fairly good attendance judging from the overall attendance of the IEDM. There was lengthy discussion on standardization of the model versus how new model developments should be encouraged. To achieve the goals, the following points were discussed:

Arranging a workshop on compact models. In fact this year (2002) two workshops are being held on MOSFET compact models: the first one is being held, as a part of 5th International Conference on Modeling and Simulation of Microsystems (MSM), in Puerto-Rico, April 22-25, 2002. At this workshop, there are nine invited speakers covering different MOS models such as BSIM4, HISiM, EKV, MOS11, SP2000, SOI and more. A panel session on compact models is also arranged. This workshop on MOS models will be the first of its kind and is largely the effort of MSM committee member Prof. Zhou, who is also a CM committee member. Another workshop on compact modeling of device and interconnect will be held September 9-10, as a part of Fabless Semiconductor Association (FSA) Modeling committee being chaired by Dr Dan Foty, who is also a CM committee member. This two-day workshop will cover both MOS and bipolar devices, in addition to interconnects.

Online Journal on Compact Modeling: It was felt that there is a need to start an online journal on compact modeling where compact modelers could share their views and experience and write articles, which need not be original research work, but should be useful for practicing engineers. Examples are methodologies for parameter extraction, technology impact on modeling, etc.

Special issue on compact modeling. It should cover topics such as Comparison of MOS vs. bipolar, flash memory, RF, nano devices, etc.

The locations and dates for the next two committee meetings for the year 2002 will be held at the following places.

Date: 9 June 2002
Meeting: VLSI Symposia
Location: Hilton Hawaiian Village, Honolulu, HI, USA

Date: 8 Dec 2002
Meeting: IEDM
Location: San Francisco Hilton & Towers Hotel, San Francisco, CA

In the first year of existence, the modeling committee has defined its goal and set up the necessary infrastructure to achieve this goal. However, more strategic discussion will follow in the coming

year regarding collaboration with designers, and foundries. We all are aware of the fact that an important aspect of modeling is data, so how to get this data is an issue. An effort should be made to contact foundries and IDMs to get data for research work. The committee will explore on this issue towards achieving its goal.

Narian Arora
Simplex Solutions, Inc.
Sunnyvale, CA, USA

Call for Nominations for the EDS Chapter of the Year Award

The EDS Chapter of the Year Award is given each year based on the quantity and quality of the activities and programs implemented by the chapters during the prior July 1st – June 30th period. Nominations for the award can only be made by Chapter Partners, SRC Chairs/Vice-Chairs, or self-

nominated by Chapter Chairs.

The winning chapter will receive a certificate and check for \$1,000 to be presented at the International Electron Devices Meeting (IEDM).

The schedule for the award process is as follows:

Action	Date
Call for Nominations E-Mailed to Chapter Chairs, Chapter Partners, SRC Chairs & SRC Vice-Chairs	6/1
Deadline for Nominations	9/15
Regions/Chapters Committee Selects Winner	Early-October
Award given to Chapter Representative at IEDM	First week of December

DL Report from the ED/SSC Bangalore Chapter

The formal inauguration of the IEEE ED/SSC society Bangalore chapter was held on March 16th 2002 at the Indian Institute of Science Bangalore. The event was co-sponsored by the ECE Department, IISc Bangalore. On this occasion a one day workshop titled "Future Challenges in the Deep Sub-Micron Era" was also conducted. The workshop had five invited seminars by the experts in devices and circuits. Prof. Hiroshi Iwai from Tokyo Institute of Technology gave an excellent introduction on "Silicon technology scaling trend from millimeter to nanometer". The other seminar topics were "Impact of Advanced Process Modules on Low Frequency Noise in CMOS Technology" by Prof. Cor Claeys IMEC Belgium; "Silicon On Insulator Devices for Analog Applications" by Prof. J. Vasi, IIT Bombay; "Designing Reset Systems for Mixed Signal VLSI" by Mr. Rajat Gupta, Cypress Semiconductors Bangalore; "Building in Reliability for Deep Sub-Micron Devices" by Dr. Radhakrishnan, Phillips, Singapore. The workshop received an extremely good response with about 130 individuals from both industry and academia.



J.Vasi, C.Claeys, N. Bhat, H.Iwai, M.K.Radhakrishnan, K.Rajagopal and Mahesh Patil at the one day workshop organized by ED/SSC Bangalore chapter on March 16th

Earlier this year, the chapter had arranged three technical talks. The first two lectures were conducted by Dr. Vishwani Agrawal, Agere Systems, USA on January 16th. The topics were "Delay Testing in Digital Circuits" and "High Speed VLSI Testing with Slow Test Equip-

ment". These two talks were co-sponsored by Texas Instruments Bangalore. On March 1st, Prof. Q.J. Zhang, Carleton University, Canada gave a lecture on "High Frequency Electronics Design: Towards Next Generation".

Status Report from the 2001 Graduate Student Fellowship Winners

In 2000, the IEEE approved the establishment of the Electron Devices Society Graduate Student Fellowship Program. The Program is designed to promote, recognize, and support graduate level study and research within the Electron Devices Society's fields of interest: which include: Compact Modeling, Compound Semiconductor Devices and Circuits, Device Reliability Physics, Displays, Electronic Materials, Microelectromechanical Systems, Nanotechnology, Optoelectronic Devices, Photovoltaic Devices, Power Devices and ICs, Semiconductor Manufacturing, Technology Computer-Aided Design, Vacuum Devices, and VLSI Technology and Circuits. In deference to the increasing globalization of our Society, at least one fellowship is to be awarded to students in each of three geographical regions: Americas, Europe/Mid-East/Africa, and Asia-Pacific.

In July 2001, EDS announced the first winners of the Fellowship awards. The three winners are: T.K. Ghosh of Lancaster University in the United Kingdom, Sergei Kucheyev of the Australian National University, and Yee-Chia Yeo of the University of California, Berkeley. The winners are pursuing distinctly different research topics for their doctoral degrees. The following are brief progress reports on the activities of the winners.



Yee-Chia Yeo

Yee-Chia Yeo is a student in the Department of Electrical and Computer Engineering at the University of California, Berkeley and his supervisor is Professor Chenming Hu.

Yee-Chia Yeo's research interests are related to semiconductor devices and electronic materials, with focus on front-end issues in complementary metal-oxide-semiconductor (CMOS) device technology. He has previously conducted research on solid-state physics and optoelectronic devices. Currently, he works on the design, fabrication, characterization, and modeling of CMOS transistors, with specific engagement on the diverse challenges faced in device scaling for improved performance and density of integrated circuits. Issues addressed in his recent projects include: channel engineering using novel materials such as silicon-germanium (SiGe), novel device structures such as the ultra-thin-body transistor, alternative gate dielectrics for reduction of direct tunneling gate leakage current, and CMOS process integration involving a dual-metal gate technology. His research encompasses experimental device fabrication and process development, as well as theoretical modeling of materials interfaces and device simulation.

In his work on strained-channel transistors, he developed a simple and novel bulk CMOS process that integrates a

pseudomorphically-strained SiGe channel layer for transistor performance enhancement. He has also worked on the integration of the SiGe heterostructure channel in a novel device structure, the ultra-thin-body MOS transistor. The ultra-thin-body transistor relies on a body thickness of 20 nm or thinner to suppress short-channel effects. Some highlights of this project were the demonstration of the first ultra-thin-body MOS transistor incorporating a SiGe heterostructure channel, and the report of the smallest heterostructure MOS transistor to date. The ultra-thin-body was formed by a novel solid-phase epitaxy technique. From June 2001 – January 2002, he was with the Exploratory Technology Department of Taiwan Semiconductor Manufacturing Company, Taiwan, where he led a team of engineers on strained-channel MOS transistors research and development.

Another area of his research relates to alternative gate dielectrics and metal gates, their process integration issues and impact on device performance. The direct tunneling gate current in transistors with alternative gate dielectrics is investigated, and important material parameters such as the tunneling effective masses are extracted. He recently explored the scaling limits of alternative gate dielectrics based on their direct tunneling figures-of-merit and gate leakage requirements for future CMOS technology generations. Guidelines are provided for the selection of gate dielectrics to satisfy the off-state leakage current requirements of future

high-performance, low operating power, and low standby power technologies. He has also worked on the integration of two different metal gates in a CMOS process in an attempt to eliminate the problems of poly-silicon gate depletion, high gate resistance, and dopant penetration. This work resulted in the first demonstration of a dual-metal gate CMOS technology using titanium and molybdenum gate electrodes. He also employed the interface dipole theory to explain the experimental observation that metal workfunctions on high-k dielectrics differ appreciably from their values on SiO₂ or in vacuum, and provided additional guidelines on the choice of gate materials for future CMOS technology incorporating high-k gate dielectrics.

He has authored or co-authored more than 30 journal and conference papers, and has written a book chapter on MOS transistor gate oxide reliability with Professor Chenming Hu.



Sergei Kucheyev

Sergei Kucheyev is a student in the Department of Electronics Engineering at the Australian National University in Canberra and his supervisor is Professor Chennupati Jagadish.

Sergei Kucheyev's research has focused mainly on ion-beam processing of group-III-nitride and ZnO

semiconductor devices. Ion-beam-produced defects can severely alter all material properties. Hence, an understanding of ion-irradiation-produced defects is essential if potential applications of ion implantation for the fabrication of III-nitride- and ZnO-based electronic devices are to be fully exploited. Emphasis of Sergei's project has been on an understanding of (i) the evolution of defect structures in III-nitrides and ZnO during ion irradiation and (ii) the influence of ion irradiation on structural, mechanical, optical, and electrical properties of these materials. In addition to ion-beam processes, Sergei's current research interests include the deformation behavior of brittle semiconductors (in particular, GaN and ZnO) and basic properties of defects in wide band gap semiconductors.

His project has resulted in the identification of a range of new and technologically important phenomena in group-III-nitrides and ZnO during ion implantation. These phenomena include (i) an unexpected and rather complex behavior of damage accumulation during ion irradiation, (ii) ion-beam-induced phase transformations in III-nitrides, (iii) local stoichiometric imbalance and associated material decomposition during ion implantation as well as during post-implantation thermal annealing, (iv) an intriguing microstructure of defects in ion-irradiated III-nitrides and ZnO, and (v) the evolution of implantation-produced defects during thermal annealing. An understanding of these phenomena is important for a successful application of ion implantation in the fabrication of electronic devices. Sergei's research on mechanical properties has led to a significantly improved understanding of the plastic deformation behavior of GaN and ZnO, which is crucial for the estimation and control of contact-induced damage in GaN- and ZnO-based electronic devices. During his Ph.D. work, Sergei has published more than thirty papers in prime journals in the field.

He has recently been awarded a highly prestigious postdoctoral fellowship at Lawrence Livermore National Laboratory (LLNL) in the U.S.A. Only up to two Fellowships in all fields of research are awarded each year with typically several hundred applicants from all over the world for the three-year program. Sergei is planning to start his appointment as a Distinguished Lawrence Fellow at LLNL in the latter part of 2002.



TK Ghosh

T. K. Ghosh is a student in the Engineering Department at Lancaster University, Lancaster, UK and his supervisor is Professor R. G. Carter.

T. K. Ghosh's research interest is on 3-D simulation and design optimisation of multistage depressed collectors for high efficiency travelling wave tubes. Travelling wave tube (TWT) is a linear beam microwave device and it is an important part of any satellite and air-borne communication system. Multistage depressed collector (MDC) is one of its major components; other two are electron gun and slow-wave structure. A dc beam, generated from the electron gun, transfers some its energy to the input rf wave through a complex process and the rf gets amplified during its travel through the length of the slow-wave structure which is then taken out from the interaction region. The purpose of a collector is to recover most of the remaining power from the spent beam and thereby increase the collector and the overall efficiency. A well-designed multistage collector sorts electrons in the spent beam according to their energy and allow them landing softly which otherwise hit the electrode surface with sufficient energy to generate heat and knock out secondary electrons. Secondary electrons play the detrimental role in collector efficiency if they are collected at a lower depressed electrode from where they were generated. They introduce noise to the amplified signal if stream back towards the interaction region, which is highly undesirable. Experimental results have shown that graphite and carbon, which have low secondary electron emission properties, can be used as electrode materials to suppress the secondary electron emission successfully to a significant level. Use of asymmetric collector geometries and the application of magnetic field in the collector region have proved to be effective in recapturing the secondaries. A fully 3-D simulator LKOBRA (MF) – mainframe version of Lancaster KOBRA has been developed at Lancaster University, UK, which is capable of simulating the multistage collectors including the effects of secondaries and the magnetic field. It is based on KOBRA3 (originally developed for the simulation of ion

sources) that has been modified and the pre- and post-processors of the package have been included.

Efficiency is a prime concern in space applications; TWT is no exception. It is always desirable to optimise the collector performance to maximise the overall amplifier efficiency. At first the potentials at different electrodes are optimised to achieve maximum possible theoretical efficiency. The number of collector stages is restricted due to the compromise among efficiency, weight and complexity in fabrication and power supply. A computer code based on the well-known hill climbing technique has been developed where all possible combinations of the electrode potentials are considered in such a way that the area under the spent beam curve covered by the electrodes is maximum for maximum power recovery. This makes the algorithm robust and reliable. It is also simple to implement. In the next step the geometry of the collector electrodes is optimised using an automated design package that is based on the 3-D simulator LKOBRA (MF). This package has been developed using a genetic algorithm. A genetic algorithm creates a new geometry through a search procedure that works from a population simultaneously. New set of geometries is generated using three basic operators, namely reproduction, crossover and mutation. The efficiency is used as the fitness parameter in the genetic algorithm that produces a new population of geometries. It acts as the deciding parameter for the changes in the collector geometry to be made. This package has been used to optimise the efficiency of a 4-stage symmetric collector to about 90% and for a 3-stage asymmetric collector to nearly 84%. In both cases the effect of secondary electron emission has not been considered which will be included in the future work.

As our current winners finish their Fellowship terms, we wish them success in their research and future endeavors. The competition for 2002 EDS Fellowship Awards is ongoing; the winners will be announced in July 2002.

Ilesanmi Adesida
EDS Educational Activities Chair
University of Illinois
Urbana, IL, USA

IEDM Short Courses on Videotape

The 2001 IEEE International Electron Devices Meeting was held this past year in Washington, DC. The two short courses that were offered at this meeting were titled, "Process and Device Technology for Sub-70 nm CMOS" and "Advanced Memory Technology and Architecture." These short courses are now available on videotape to purchase through IEEE Customer Service.

Process and Device Technology for Sub-70 nm CMOS

Presented by Suresh Venkatesan, Motorola; Yuan Taur, IBM; Dr. Luc Van den Hove, IMEC; Dr. Hsing-Huang Tseng, Motorola; Liang-Kai (Kevin) Han, TSMC; Chris J. McDonald, Intel Corporation

Moore's Law inexorably drives the density, size and performance of semiconductors. The feature size of modern silicon technology is at the 130nm node and will soon move to the 100nm node. Prognostications of fundamental limits notwithstanding, device gate lengths will shrink down to 50nm in the 100nm node and equivalent gate oxide thickness will scale below 15Å. Further shrinking to the 70nm CMOS technology node in many ways places us at crossroads, and each path is fraught with significant challenges. Maintaining performance trends in sub-50 nm devices will drive novel device architectures such as SOI, SiGe, and vertical devices. Increasing gate leakage currents accompanying the aggressive scaling of gate dielectrics coupled with the low power requirements of mobile products will require new gate dielectrics. The wavelength of light will need to be dialed back another notch to keep up with pattern resolution requirements. This course will provide insight into these challenges in the front-end-of-the-line, and discuss potential solutions in the areas of device design, lithography, gate stack, process integration and manufacturing trends.

The first lecture will cover device scaling trends for both low power and high performance applications. It will further cover the device requirements and architectures for the 70nm node including a glimpse at novel structures. The second lecture will cover lithography requirements and trends including a discussion of 157nm lithography systems and

beyond. The third lecture will present an overview of the materials under consideration to replace the conventional polysilicon/SiO₂ (SiON) system and the process integration challenges spawned by this transition. New materials and process integration challenges for device isolation, shallow junction formation and the silicide technology required for contacting the shallow junctions will be discussed in detail in the fourth lecture. Finally, not all trends are benefited by the performance and cost driven scaling paradigm. Yield enhancement in particular is made more challenging by the shrinking dimensions. Requirements and trends for efficient manufacturing and yield management will be the topic of the final lecture.

Order information:

Title: **Process and Device Technology for Sub-70 nm CMOS**

NTSC Order No. EV6983

NTSC ISBN 0-7803-6836-3

PAL Order No. EV6984 PAL ISBN

0-7803-6837-1

IEEE Member Price: \$380.00

List Price: \$450.00

Advanced Memory Technology and Architecture

Presented by Kunio Nakamura, NEC Corporation; Clair Webb, Intel Corporation; Won-Seong Lee, Samsung Electronics; Kenji Noda, NEC Corporation; Raffaele Zambrano, STMicroelectronics; Saied Tehrani, Motorola Inc.

The explosive evolution of digital information technologies requires innovation not only in logic devices but also in the semiconductor memory systems. For example, next generation cellular phones will need much larger memory capacity for digital signal processing than present systems, the use of DRAM cache can reduce MPU power, and, in the distant future, main memory may be substituted by high density non-volatile memory.

Under these IT market needs, continuing efforts in process and circuit technologies have led to realization of commercially available Giga-bits DRAM within a few years. Performance improvement towards higher bandwidth also continues in SDRAM or RDRAM, adopting the novel system architectures to cope

with aggressively increasing MPU operation frequency. Embedded DRAM with high bandwidth and low latency has already been introduced for graphic applications. In SRAM, high speed cache with the operating speed over 1 GHz has been developed with deep sub-micron technology. Power management is also an important issue, especially for the SRAM used in mobile applications.

Recently, the non-volatile memory market has been growing much more rapidly than other fields, thanks to the growth of portable multimedia devices. The NAND flash memory for mass data storage, the NOR flash memory for stand-alone and embedded applications, and the EEPROM for the smart card have been leading the market. These devices, however, have programming speed and endurance limitation. To overcome these drawbacks, development of the emerging technologies such as FeRAM or non-volatile magnetoresistive RAM (MRAM) is in progress.

This course starts with an overview of the MPU architecture evolution and its influence on memory architecture. The second lecture presents the leading edge process and device technologies for Giga-bits DRAM. The third lecture describes state-of-the-art SRAM device and circuit technologies. The fourth lecture deals with non-volatile memory, and the appropriate device solution for each application will be discussed. The final lecture shows potential of MRAM device as a promising candidate of the future non-volatile memory.

Order information:

Title: **Advanced Memory Technology and Architecture**

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Regional and Chapter News

USA, Canada and Latin America (Regions 1-6, 7 & 9)

ED Washington/Northern Virginia

The February and March 2002 meetings for the Washington/Northern Virginia Chapter were co-sponsored with the Microwave Theory and Techniques (MTT) Chapter.

On February 21, 2002 Dr. Michael B. Steer of North Carolina State University delivered a lecture entitled "Technology Choices for Multifunctional Adaptive Radio, Radar, and Sensors". Dr. Steer, currently a Professor of Electrical and Computer Engineering at North Carolina State University, has been very active in research tied to solving fundamental problems in modeling and implementing RF and microwave circuits and systems. He is a Fellow of IEEE.

Dr. Steer noted that while the commercial investments in RF technology since 1990 led to innovations that began the transition to a tether less Society, the prior military RF technology investments were very significant and can legitimately claim to have sparked the commercial RF revolution. With the cost of military systems now being a critical factor in determining whether they are fielded, there is great interest in applying commercial tools, techniques and technologies to military RF systems. Dr. Steer explored the relationship between military and commercial RF with an emphasis on what must be done to achieve cost effective military RF front ends. He described multiple evolving technologies applicable to multifunctional systems.

On March 14, 2002, Mr. Joseph F. Jensen of HRL Laboratories spoke on "High Speed Analog-to-Digital Conversion for RF and Digital Receiver Applications". Mr. Jensen is currently a Principal Research Scientist and Department Head of the Ultra-High Speed IC Department in the Microelectronics Laboratory at HRL and has been actively involved with the development of GaAs MESFET's, AlInAs/GaInAs HEMT's, AlInAs/GaInAs

HBT device technologies.

Mr. Jensen noted the desire of system designers for modern communications and radar systems to move the analog-to-digital interface as far forward in the signal path as possible toward the antenna or sensor. This movement of the digital interface forward in the signal path eliminates stages of down conversion and analog filtering that are bulky, expensive, drift with temperature, and requires calibration. He discussed the role of ultra-fast device technologies such as SiGe, GaAs, and InP HBT in this context. Mr. Jensen also described techniques for A/D conversion at the RF or IF of a receiver such as noise cancellation in wideband ADCs and high sample rate bandpass delta-sigma ADCs for narrowband.

The EDS Chapter expresses its appreciation to the MTT Chapter for making possible the sponsorship of these talks.

ED Mid-Hudson Valley

The IEEE Mid-Hudson Valley (*Region 1*) Electron Devices Chapter co-sponsored a meeting on November 29, 2001, with the local IEEE Section, on OLED Microdisplays. The guest speaker was Dr. Webster Howard of eMagin Corporation, Hopewell Junction, NY. Dr. Webster discussed the advantages of using organic light emitting diodes (OLEDs) on silicon active matrix substrates as a replacement for liquid crystal-based microdisplays for camera viewfinders, DVD players, and wearable computers. The meeting was attended by approximately 50 people, including local experts in the field of microdisplay technology. The next Electron Devices Chapter meeting was held on 25 April 2002. The guest speaker was Dr. Lili Deligianni of IBM Research who discussed Microelectromechanical Systems for Wireless Communications.

Murty S. Polavarapu —Editor

Summary of Activities in Regions 5 & 6

-by Sunit Tyagi

In the past few months and ones coming ahead, the IEEE EDS members in

Regions 5 and 6 have been very active participating in many technical workshops and conferences which include: the International Symposium on Quality Electronics, held in San Jose, CA from 18-20 March 2002; the IEEE International Reliability Physics Symposium from 7-11 April 2002, in Dallas, TX; and the International Vacuum Electronics Conference, held in Monterey, CA from 23-25 April 2002.

There will be many conferences during the month of June, starting with the Radio Frequency Integrated Circuits Symposium in Seattle, WA, 2-4 June; the International Symposium on Power Devices and Integrated Circuits will be held in Santa Fe, NM, 3-7 June; the International Interconnect Technology Conference will take place in San Francisco, CA, 3-5 June. Many conferences will take place in balmy Hawaii, during the period of 5-15 June. There is the: IEEE Workshop on Silicon Nanoelectronics, 9-10 June; the IEEE Symposium on VLSI Technology 11-13 June; and the IEEE Symposium on VLSI Circuits 13-15 June. This year the Device Research Conference will be held in Santa Barbara, CA from 24-26 June.

ED Boise

- by Fernando Gonzalez

The ED Boise Chapter held a Distinguished Lecturer presentation at the Micron's Leading Edge Program on 1 March 2002. The speaker, Dr. Albert Wang, is an assistant professor in ECE department of the Illinois Institute of Technology and a distinguished lecturer for the ED/SSC societies. He discussed in detail the topic of on-chip Electrostatic Protection Circuit Design and Process. As many as 60 people attended, including employees from Micron and Zilog, and other EDS members such as students and faculty members from Boise State University.

Dr. Wang is the EDS mentor and advisor to the ED Boise Chapter. He met with the Boise Chapter officers, discussing broad EDS related issues, including better use of EDS resource, activities, increasing member participation, and



Albert Wang, IEEE EDS/SSCS
Distinguished Lecturer

enhancing the relationships with other chapters and universities.

In May and June, two IEDM tutorial courses on "Reliability for the Logic and Memory Technologies" and "Advanced Interconnects: Design, Process and Integration" were offered by the ED Boise Chapter at Micron Site. The courses were open to Micron employees and local IEEE members.

ED Seattle

- by Tom Raschko

The Seattle Chapter held a very successful meeting in the form of a symposium. This "Wireless Symposium" was open to the public at minimal cost of \$125 per person. This event netted \$10K for the Seattle Chapter. EDS held this symposium jointly with the Communications, Computer, and Engineering in Medicine and Biology societies, and shared the resources and the load. The chapter, along with MTT, is now focusing its energy to ensure the success of IMS2002 which will be held in June 2002 in Seattle, WA.

Sunit Tyagi — Editor

Europe, Middle East & Africa (Region 8)

ED/SSC Novosibirsk State Technical University Student Branch

- by Alexander V. Gridchin

The 2nd Siberian Russian Student Workshop and Tutorial on Electron Devices and Materials EDM' 2001 was successfully held in Novosibirsk State Technical University (NSTU), Novosibirsk,

Russia, July 3-7, 2001. The Workshop and Tutorial was organized by ED/SSC NSTU Student Branch in co-operation with the Dept. of Semiconductor Devices and Microelectronics of NSTU. The Workshop and Tutorial was technically co-sponsored by the ED and SSC societies and financially supported by the Governmental Program 'The Federal Support of Integration of Fundamental Science and High Education for 2001 Year'.

The total number of attendees of EDM'2001 was more than 70. Twelve Russian cities have been represented by reports in the Workshop. Two famous professors were invited to make a presentation for the participants of the Workshop: Prof. Kwyro Lee, KAIST, Korea, and Prof. Biswaijt A. Das, West Virginia University, USA. Besides, Prof. Lee also visited our Workshop as an official Chapter partner for the establishing of the partner's connections between the chapters. 'I enjoyed it, thank you very much for Your efforts', said Prof. Lee in the International Airport of Novosibirsk city.

The EDM'2001 Workshop and Tutorial covered the wide spectrum of problems connected with electronics, microelectronics and nanoscale electronics. All reports were grouped into 4 Sessions. As a result of the Workshop and Tutorial, the volume of Proceedings were issued and full text of papers are available via IEEE Xplore. A CD-ROM version was issued as well.

The EDM'2001 Workshop and Tutori-



Professor Victor A. Gridchin in making of his presentation in the EDM'2001, NSTU, Russia

al is a unique event for students to receive knowledge from the outstanding specialists and the excellent possibility for professors to give their scientific experience to a young generation of researchers. The idea to hold Workshops, Tutorials and Conferences outside the city has been very effective for estab-

lishing the aura of free communication and for attracting quests.

As a result, co-operation with other Student Branches can provide the interaction between students also. Two student branches have been established since the holding of the EDM'2001 and this interaction can be realized in other scientific and social events.

Thus, the EDM'2001 Workshop and Tutorial is a step for the establishing of the scientific environment in Siberia.

The ED/SSC NSTU Student Branch is very grateful to the ED Society for the financial support of the visit of Prof. Kwyro Lee.

AP/ED/EMC/MTT/COM Tomsk Chapter & Student Branch

- by Oleg V. Stoukach, Eugene I. Golovin

With great pleasure we can report that the IEEE-Siberian workshop of students, post-graduate students and young researchers in modern communication technologies SIBCOM-2001 was successfully held November 28-29, 2001 in Tomsk, Russia. The SIBCOM Workshop was organized by the Tomsk Chapter and Student Branch with the support and assistance of the Russian Foundation for Basic Research and technical co-sponsorship from IEEE and the Communications Society.

This Workshop is the continuation of the best traditions introduced by the International Symposium SIBCONVERS. Different levels and types of presentations were accepted, they are: the presentation of research and scientific results, new ideas, valuable conclusions from experience, the state of the art and instructive survey communications.

The first plenary meeting was opened by the corresponding member of the International Academy of High School Sciences, professor Alexander A. Shelupanov. His workshop on the modern advances in the information protection and other fields was very successfully presented. After that, a lot of reports on software cryptography, modern data transfer technologies, etc., were done at the Workshop. A small seminar for the post-graduate students was organized after the sessions.

Our event allows us to achieve the further increasing of academic exchanges and cooperation between the Siberian specialists in radio engineering and their colleagues in other countries. The best affirming of that is the participation of foreign scientists in SIBCOM-2001. We

thank Mr. Tomasz Orzechowski from Poland for his very interesting report on his work in the global European project.

As a result of the SIBCOM Workshop we have the volume of Proceedings as the collection of full reports in English. We've received great experience in contacts with foreign colleagues. We thank all participants and Prof. Shelupanov for the organization of the SIBCOM-2001 Workshop. We are looking forward to seeing you at the SIBCOM-2003 Workshop.

Alexander V. Gridchin — Editor

9th International Conference: MIXED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS - MIXDES 2002

This conference will be held 20-22 of June 2002 in Wroclaw, Poland. The conference is an annual event and gathers each year around 150 scientists from over 20 countries. During the conference, more than 100 papers will be presented at oral and poster sessions. The papers cover areas of design, analysis, simulation and testing of microelectronic circuits and microsystems as well as power devices. This year, the following nine main topics will be discussed:

Design of integrated circuits and microsystems (design methodologies, digital and analog synthesis, hardware-software co-design, hardware description languages, intellectual property-based design, design reuse).

Thermal issues in microelectronics (thermal and electro-thermal modeling, simulation methods and tools, thermal mapping, thermal protection circuits).

Analysis and modeling of IC and microsystems (simulation methods and algorithms, behavioral modeling with VHDL-AMS and other advanced modeling languages, microsystems modeling, models reduction, parameters identification).

Microelectronics technology and packaging (new microelectronic technologies, packaging, sensors and actuators).

Testing and reliability (design for testability and manufacturability, measurement instruments and techniques).

Power electronics (design, manufacturing and simulation of power semiconductor devices, hybrid and monolithic Smart Power circuits).

Signal processing (digital and analogue filters, telecommunication circuits, neural networks, artificial intelligence, fuzzy logic, low voltage and low power solutions).



Dr. Oleg Stoukach is presenting his lecture 'The IEEE: Networking the World'

Interdisciplinary applications (medical, space technology, industrial and others, reconfigurable hardware).

Education (education methodology, software and tools, web-based teaching).

Beside the regular papers, the following Invited Presentations are being planned:

"Recent advances and future trends in RF power FET technologies" by Prof. Krishna Shenai (Distinguished IEEE Lecturer), The University of Illinois at Chicago, Power Electronics Research Center, USA

"Deep-submicron CMOS scaling challenges" by Dr. Gonçal Badenes, Silicon Technology and Device Integration Division, IMEC, Belgium

"Optimal/Robust Design of Nonlinear Multi-Physics Systems — MOEMS & Biochips Examples" by Michael J. Saran, OES, Inc. & Case Western Reserve University, USA

"CMOS Vision Chips" by Prof. Angel Rodriguez-Vazquez, High-Performance Mixed-Signal VLSI ICs, Instituto de Microelectronica de Sevilla-CNM/CSIC, Sevilla, Spain

"Mixed-Signal Multi-Level Circuit Simulation: An Implicit Mixed-Mode Solution" by Prof. Xing Zhou (Distinguished IEEE Lecturer), School of Electrical & Electronic Engineering, Nanyang Technological University, Singapore

Also, the following Special Session presentations are being planned:

I. "MOS Modeling and Modern Mixed-Mode Design" (from CMOS technology developments through MOS modeling to system simulations) organized by Wladyslaw Grabinski, Motorola

- "CMOS technology and Compact models" by T. Skotnicki
- "EKV2.6 selfheating" by C. Lallement
- "EKV3" by M. Bucher
- "gm/Id-Based MOSFET Modeling and Modern Analog Design" by D. Foty
- "Compact model standardization"

by L. Lemaitre

- "Advanced RF Calibration Techniques" by A. Lord
- "NNMS: nonlinear large signal measurements" by E. Vandamme

II. "Interdisciplinary Design: Models and Methods" organized by Władysław Grabinski, MOS-AK Group

- "From continuous field modeling to MEMS macro models" by G. Wachutka
- "Multi-Level Modeling of Deep-Submicron MOSFETs and ULSI Circuits" by X. Zhou

- "MOS Transistor Modeling for HV Processes" by E. Seebacher
- "A unified environment for MOS modeling inside Agilent's IC-CAP" by T. Gneiting
- "SOI 1T DRAM Compact Model" by J-M. Sallese
- "Behavioral models in analog IC design"
- "Application of LTCC ceramics in microwaves" by L. Golonka

III. "Research and Training Action for System on Chip Design, the FP5 European project" organized by Prof. Wiesław Kuzmicz, Warsaw University of Technology, Poland

IV. "System for European Water Monitoring, the FP5 European project" organized by Prof. Andrzej Filipkowski, Warsaw University of Technology, Poland

ED Sweden

- by Mikael Östling

The Sweden ED Chapter arranged several technical seminars/presentations during the fall and winter. Prof. Gijs Bosman, University of Florida, Gainesville, USA, presented a lecture on Simulation of Low-Frequency Noise in MOS Devices. He was also engaged in a summer school for PhD students on wireless systems and technology where he lectured on noise aspects in high frequency silicon devices.

In November, we arranged a Chapter Symposium on Device Modeling. This was a half-day symposium where newly graduated PhDs or PhD students (close to finishing) presented fresh results on device modeling from their own research. The Symposium was well received and attracted more than 35 persons from universities and industry. In total, 8 presentations were made. The Symposium was arranged by Professor Torkel Arnborg and



All speakers at the ED Sweden Chapter Symposium on Device Modeling, From left, Prof. T. Arnborg, J. Sjöström, T. Ewert, J. Anckarcrona, B. Wilén, E. Danielsson, M. Domeij and M. Sandén

Chapter Chair, Professor Mikael Östling.

In December, the chapter was visited by Dr. John Torvik, Astralux Inc., and University of Colorado, Boulder, USA. He presented a very interesting seminar on SiC materials and devices for RF power.

In March, we had a presentation on SiGe HBT high-speed circuits for communication applications by Dr. Toru Masuda from Hitachi Central Research Lab, Japan.

During the spring we plan further technical seminars and some video screening sessions.

Andrzej Napieralski — Editor

MTT/ED/AP/LEO UK&RI

-by Terry Oxley

The current 2002 activities programme includes wide ranging events, for example; Chapter AdCom meetings; lectures by invited speakers; short courses, workshops, symposia and colloquia, many of international interest. The 3rd European MIDAS Workshop-Topical meeting on mixed signal simulation for communication systems, planned for 1-2 July 2002 in The Netherlands, will be reported in the October Issue of EDS Newsletter. The Chapter would, however, like to remind readers of two forthcoming major events within its programme:-

1. The 7th IEEE High Frequency Post-graduate Student Colloquium is planned for 9 September 2002 at the Imperial London Hotel, London, UK. Jointly organised by The Imperial College of Science, Technology & Medicine and the UK&RI Chapter with support by EDS and MTT-S; the aim of the event is to provide an opportunity for student researchers in the field of high frequency engineering to present their work, gain experience in the art of professional presentation, and to interact with students from other universities. Student participation from outside the UK&RI is encouraged. For further details, contact Stepan Lusyszyn at Imper-

al College, E-mail: s.lucyszyn@ic.ac.uk.

2. The 10th IEEE International Symposium on Electron Devices for Microwave & Optoelectronic Applications (EDMO) Symposium is planned for 18 -19 November at The University of Manchester Institute of Science & Technology (UMIST), Manchester, UK. The symposium is jointly organised by UMIST and the UK&RI Chapter with the support of IEEE EDS, MTT-S, LEOS, APS and UK IEE. The aim of the event is to provide a forum for microwave and optoelectronic device designers, technologists and end-users to discuss advances in device performance and system requirements. The Call-For-Papers deadline for abstract submissions is 10th September 2002. For further information, please e-mail the EDMO Symposium Secretary at enquiries@edmo-symposium.org, or see <http://www.edmo-symposium.org>. For information on Chapter activities, please contact the Chapter Chairman: Dr Ali Rezaadeh, Department of Electronic Engineering, King's College, University of London, Strand, London WC2R 2LS, UK. Tel/Fax: +44 20 7848 2879. E-Mail: ali.rezaadeh@kcl.ac.uk.

ED Israel

-by Prof. Nathan Croitoru, Chapter Chair and Dr. Gady Golan; Secretary

1. On Sunday, December 23rd 2001, at the Holon Inst. of Technology (HAIT) - Holon. Subject of meeting: "Robust control of uncertain feedback systems", Guest lecturer was Dr. Marcel Sidi from HAIT. Chairmen of the meeting: Prof. Nathan Croitoru and Dr. Gady Golan -

20 people (most of them were students and academic staff) attended the meeting in Holon.

2. On Wednesday, January 16th 2002, at the Holon Inst. of Technology (HAIT) - Holon. Subject of meeting: "Bleaching Processes And Their Reaction Rates In Photo-Excited Chlorophyll Solu-

tions", Guest lecturer was Dr. Nina Mirchin from HAIT. Chairmen of the meeting: Prof. Nathan Croitoru and Dr. Gady Golan - 40 people (most of them were students and academic staff) attended the meeting in Holon.

3. On Wednesday, February 13th 2002, at the Holon Inst. of Technology (HAIT) - Holon. Subject of meeting: "Optical Thin Films", Guest lecturer was Dr. Reuben Dahan from HAIT. Chairmen of the meeting: Prof. Nathan Croitoru and Dr. Gady Golan - 25 people (most of them were students and academic staff) attended the meeting in Holon.

4. On Sunday, March 3rd 2002, at the Holon Inst. of Technology (HAIT) - Holon. Subject of meeting: "Electric load estimation in IEC Israel", Guest lecturer was Eng. Uri Barenbaum. Chairmen of the meeting: Prof. Nathan Croitoru and Dr. Gady Golan - 35 people (most of them were students and academic staff) attended the meeting in Holon.

5. On Friday, March 9th 2002, at Kings College London (KCL), Distinguish Lecturer seminar, Subject of meeting: "Thermal Chip Technology - A Novel Concept in Self-Regulated Heating", Guest lecturer was Prof. Tony Davies - KCL. Chairmen of the meeting: Dr. Ali Rezaadeh - KCL. 20 people attended the meeting in London.

Gady Golan — Editor

ED Central/South Italy

-by Salvatore Bellone and Heinz-Christoph Neitzert

During the last year, our chapter organized a series of seminars at the University of Salerno:

In particular, in December 2001, Prof. Veljko Milutinovic from the University of Belgrade (Yugoslavia) gave a presentation, titled: "Advances in VLSI Design" and in March 2002 Prof. Wolfgang Fahrner from the University of Hagen (Germany) gave lectures on "Ion Implantation - Technology and Applications".

Another event sponsored and co-organized by our chapter was a 3 day seminar cycle regarding photovoltaic energy conversion from the 10-12 December. The lecturers were Dr. Regis Vanderghehen from the Ecole Polytechnique (France), Dott. Francesco Roca, Ing. Angelo Sarno, Ing. Giorgio Graditi and Ing. Apicella from ENEA (Portici) and Dott. Guerriero from the Campania regional administration. The seminars covered a wide range of aspects of photovoltaic energy conversion, ranging from material research through cell and system

design to economic aspects of photovoltaic energy implementation and brought together specialists and more than 200 students interested in this matter. Information about our chapter distributed during this event resulted in the enrollment of more than 25 new student members to the EDS for the year 2002.

From 6-8 March 2002 our chapter – represented in this occasion by the University La Sapienza of Roma, by the University Federico II of Napoli and by the University of Salerno – has been organizing in Salerno together with the Italian Solar Energy Research Institute (ENEA) the “8th Euroregional Workshop on Thin Silicon Devices”, gathering more than 130 specialists in this field coming from more than 15 countries.

Christian Zardini — Editor

Asia & Pacific

ED/LEO Australia

-by C. Jagadish

The Chapter and its executive committee are actively involved in the organisation of the 2002 Conference on Optoelectronic and Microelectronic Materials and Devices (COMMAD) to be held in the University of New South Wales, Sydney December 11-13, 2002. Short courses will be held on Photovoltaics, Semiconductor Diode Lasers and Silicon based Quantum Computers on December 9-10, 2002. Abstracts on the following topics are due 1 August 2002: Growth and Advanced Processing of semiconductors, Material Properties and Characterisation, Electron Devices and Systems, Optical Devices and Systems, Nanostructure Physics and Device Possibilities.

Further information can be obtained from the COMMAD Web Page: www.commad.unsw.edu.au or by contacting Prof. Michael Gal, School of Physics, University of New South Wales, Sydney, NSW 2052, Australia, Fax: +61-2-9385-6060, Email: COMMAD@phys.unsw.edu.au

For more information, please contact Prof. Chennupati Jagadish, Tel: 61-2-6125-0363, Fax: 61-2-6125-0511, Email: c.jagadish@ieeee.org.

ED/MTT India

- by KS Chari

Under the EDS STAR program, a one day science fair was organized at Haritha Ecological Institute (Paloncha, Andhra Pradesh) held on 5 January 2002. The Chapter Chair also visited the Haritha Institute to review the STAR efforts.

The Chapter co-sponsored the CPM-PONEX Electronics India 2002 International Conference and Exhibition of Electronic Components, Materials and Production Equipment held at Bangalore from 29 January to 1 February 2002. The event was attended by over 500 participants from industry, research community and government agencies.

A two-day National Symposium on Electronics Technology (NASET 2K2) was organized by the Chapter in conjunction with the Electronics Society on 15-16 March 2002. It focused on developments in the fields of Electronics, Information Technology, Computers and Engineering disciplines. Over 200 students from 10 Universities/Engineering Colleges attended the event. A major attraction was the paper presentation session whereby 30 papers were presented covering a wide spectrum of activities in the field of semiconductor devices and computers. The Chapter has given out 20 awards for various NASET events and certificates of attendance for all participants.

AP/ED Bombay

-by V. Ramgopal Rao

On 3 January 2002, Prof. Vijay Arora, EDS Distinguished Lecturer, delivered a lecture titled “Hot Electrons: A Myth or Reality?” at IIT Bombay. Prof. Arora also conducted a half-day ‘Workshop on entrepreneurial Spirit’ on 4 January. The workshop attracted over 120 people from all over the Bombay region.

On 6 January, the Chapter arranged a video show of the short course given by Prof. Asad Abidi (University of California, Los Angeles) on “Circuit Designs and Technology for RF-CMOS”. Over 100 graduate level students attended this video show.

On 7 February, the Chapter invited Prof. W.S. Khokle, ex-Director of CEERI (Pilani, India) to give a lecture on “Electronic Design Towards Consciousness”. The talk was extremely well received.

On 25 February, Prof. Q.J. Zhang of Carleton University (Canada) delivered a lecture on “High-Frequency Electronics Design: Towards Next Generation”.

Prof. Hiroshi Iwai of the Tokyo Institute of Technology and Prof. Cor Claeys of IMEC, were invited by the Chapter to meet the EDS members in the Bombay region. Prof. Iwai also gave a talk on “Silicon Technology Trends from Past to Future: Downsizing from Millimeter to Nanometer” on 25 March.

For more information, please contact

Prof. V. Ramgopal Rao, Tel: 91-22-5767456 OR 91-22-5722545 Ext.7456, Fax: 91-22-5723707, Email: rao@ee.iitb.ac.in.

ED Malaysia

-by Burhanuddin Yeop Majlis

The Chapter organized a short course on Advanced Surface Analysis Techniques at the Faculty of Engineering, Universiti Kebangsaan Malaysia on 5 May 2002. More than forty participants attended the course from local semiconductor industries and universities.

The ED Malaysia chapter is also organizing the 2002 IEEE International Conference on Semiconductor Electronics (ICSE2002) on 19 -21 December 2002 at The Gurney Resort Hotel & Residences, Penang. The scope of the conference covers all fields of microelectronics, such as device physics, process technologies, VLSI and MMIC circuits’ design, optoelectronics, MEMS and sensors, packaging and test.

For more information, please contact Prof. Burhanuddin Yeop Majlis, Tel: 603-89265861, Fax: 603-89259080, Email: burhan@vlsi.eng.ukm.my.

REL/CPMT/ED Singapore

-by Y.C. Ng

The Chapter organized one technical talk on 12 March 2002 in association with the School of EEE of Nanyang Technological University. The speaker was Dr. M. Natarajan of IMEC and the topic was “ESD Issues and Challenges in Deep Sub-Micron Technology – Present and Future”. More than 70 participants attended the talk from a number of industries as well as universities.

The Chapter’s major conference, IPFA (International Symposium for Physical and Failure Analysis of Integrated Circuits), is in its 15th year and the Advance Program for IPFA 2002 has been finalized. IPFA 2002 will be held at Raffles City Convention Centre from 8-12 July 2002. The program includes 4 Tutorials as well as 52 oral papers, including 6 invited papers and two Best Paper exchanges from ESREF and ISTFA. (web-site for IPFA <http://www.ieee.org/ipfa>)

The IEEE TAB (Technical Activities Board) visited the Singapore Section along with the IEEE President on 26 March 2002. The Chapter committee participated in hosting them and had discussions with the team, and TAB appreciated our activities and interaction with the members.

For more information, please contact Y.C. Ng, email: yc.ng@ieee.org.

Wee Kiong Choi — Editor

ED Japan

-by Naoki Yokoyama

The chair and secretary of the ED Japan Chapter, Prof. Kazuo Tsubouchi (Tohoku University), Chair, and Prof. Kazuya Masu (NEC), Secretary, retired at the termination of their 2-year term. For 2002-2003, the chapter has a new chair and its staffs: Dr. Naoki Yokoyama (Fujitsu Laboratories Ltd.); Chair, Prof. Hiroshi Ishiwa (Tokyo Institute of Technology); Vice-Chair, Dr. Yuu Watanabe (Fujitsu Laboratories Ltd.) Secretary; and Prof. Kazuo Tsutsui (Tokyo Institute of Technology) Treasurer. We would like to thank Prof. Tsubouchi and Masu for their great contribution to the ED Japan Chapter and welcome the new officers. On January 21st, an annual Briefing Session for the 2001 IEDM was held in Tokyo, where five speakers were invited to deliver summary talks on the highlights of the 2001 IEDM. Topics covered were Integrated Circuit, CMOS Devices, CMOS Interconnects/Process, Modeling/Simulation, and Compound/Quantum Devices. This was a good opportunity for most of the Japanese engineers, who did not have chance to attend the last IEDM, to get the latest information presented at the largest meeting in the IEEE Electron Devices Society.

The meeting was very successful and attracted about 120 participants. After the IEDM Briefing Session, the committee meeting of the ED Japan chapter was held and the 2002 activity plan was discussed. It was concluded that the chapter technically support several domestic Workshops, and fund a chapter award "ED Japan Student Award" to encourage students who actively contribute to the research of electron devices. The chapter will promote the Senior Member Program and DL Program to enhance the EDS activity in Japan.

ED Kansai

-by Hiroshi Nozawa

A year past since the ED Kansai Chapter was established. The Kansai Chapter has a newly created Message from Spirited Kansai (MFSK) Award to encourage ED Kansai Chapter members in technical activity. The ED Kansai Chapter Award Committee (Chair: T. Nishimura) has evaluated and selected a winner of the award based on sixteen papers presented at the Kansai Colloquia Electron Devices Workshop that was held by the ED Kansai Chapter, 16 January 2002, in Kyoto, Japan. The Executive Committee has agreed to the selection of the award winner after critical examination.

The winner's name and affiliation are S. Maeda of Mitsubishi Electric Corporation and the title of the paper is:

An Artificial Fingerprint Devices (AFD) Module using poly-Si Thin Film Transistors with Logic LSI Compatible Process for Built-in Security. The winner will be honored at the next Workshop, 11 July 2002, Osaka, Japan, presented with a memorial plate.

— Hisayo S. Momose, Editor



S. Maeda of Mitsubishi Electric Corp, the first winner of MFSK Award.

ED Hong Kong

-by Mansun Chan

With the 30th Anniversary of the IEEE Hong Kong Section, the Hong Kong Electron Devices Chapter also entered its 10th year. As the Chair of the ED Hong Kong Chapter, I am glad to see the members in the ED Society have grown steadily in Hong Kong to about 80.

The Hong Kong Electron Device Meeting (HKEDM) has become an important annual event of the region. The number of papers presented in the meeting has also increased steadily from 14, when the meeting was first founded in 1994, to more than 36 papers this year. Participants are attracted from all around the world. HKEDM will remain as one of the major annual events sponsored by the ED Hong Kong Chapter in the years to come. Besides HKEDM, the chapter has also been continuously sponsoring and supporting many local activities including distinguished seminars and conferences. In the coming year, we have planned to sponsor 4 distinguished lectures and a new FPGA conference in addition to the HKEDM. We hope the activities in the ED HK Chapter will continually grow in number, quality and number of participation.



Prof. Hiroshi Iwai and Prof. Cor Claeys with members of IEEE AP/ED Bombay Chapter and students at IIT Bombay

Report on Advanced CMOS Device and Technology Process Workshop

A one-day workshop on Advanced CMOS Device and Process Technology was held at the National Chiao Tung University, Hsinchu, Taiwan, on 30 January. The purpose of this workshop is to give those industrial engineers, university faculties, and students, who did not attend the VLSI Technology Symposium and the IEDM last year, the opportunity to learn the most recent advances in Silicon-based VLSI devices and technologies. This workshop attracted more than 180 partici-

pants and attendees included both IEEE members and nonmembers.

The workshop was organized into 5 different areas and 5 invited experts gave the presentation. These include – Nano-Scale CMOS Technology (Dr. H.C. Lin, NDL), High-k Gate Dielectric and Metal Gate Technology (Dr. C. H. Chien, NDL), CMOS Process Integration (Dr. Kevin L. K. Han, Tsmc), SoC Technologies (Dr. C. C. Wu, Tsmc), and Non-volatile Memory Technology (Dr. C. M. Liu, Winbond USA). These presentations was given with the most updated tech-

nologies and a review of selected papers from the above two conferences. For each topic, tutorial materials were also included such that the attendees may understand the fundamentals of each area. In other words, the lecture is given in a way similar to a short course but also includes leading technologies for state-of-the-art VLSI devices. This is the second time that the Taipei Chapter held this activity and it was very successful in terms of the number of attendees including EDS members and nonmembers.

—Tahui Wang, Editor

Congratulations to the EDS Members Recently Elected to IEEE Senior Member Grade!

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* = Individual designated EDS as nominating entity

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EDS Meetings Calendar

(As of 7 May 2002)

The complete EDS Calendar can be found at our web site:
<http://www.ieee.org/organizations/society/eds/EDSCal.html>. Please visit!

July 5 - 9, 2002, T **Siberian Russian Workshop and Tutorial on Electron Devices and Materials** Location: Novosibirsk State Technical University, Novosibirsk, Russia Contact: Alexander Gridchin, Novosibirsk State Technical University, 20 Karl Marx Prospect, Dept. of Applied & Theoretical Physics, Novosibirsk, Russia 630092 Tel: +7 3832 46 0877 Fax: +7 3832 46 0209 E-Mail: algrid@ref.nstu.ru Deadline: Not Available www: <http://ref.nstu.ru/ieeesb/edm>

July 7 - 11, 2002, @ **International Vacuum Microelectronics Conference** Location: University Lyon 1, Lyon, France Contact: Vu Thien Binh, Universite Claude Bernard Lyon 1, Departemnt de Physique des Materiaux, UMR-CNRS, 69622, Villeurbanne, France Tel: +33 0 4 7244 8070 Fax: +33 0 4 7244 8245 E-Mail: vuthien@dpm.univ-lyon1.fr Deadline: 4/1/02 www: <http://ivmc2002.univ-lyon1.fr>

July 8 - 12, 2002, T **IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits** Location: Raffles City Convention Centre, Raffles City, Singapore Contact: Jasmine Leong, Kent Ridge Post Office, PO Box 1129, Singapore 911105 Tel: +65 743 2523 Fax: +65 746 1095 E-Mail: ipfa@pacific.net.sg Deadline: 1/31/02 www: <http://www.ieee.org/ipfa>

July 8 - 12, 2002, @ **International Vacuum Electron Sources Conference** Location: Saratov State University, Saratov, Russia Contact: Raouf Bakhitizin, Bashkir State University, 32 Frunze Street, Ufa 450074, Russia Tel: +7 3472 236 574 Fax: +7 3472 503 085 E-Mail: raouf@bsu.bashedu.ru Deadline: 4/30/02 www: <http://www.ivesc.sgu.ru>

July 28 - August 1, 2002, @ **IEEE Intersociety Energy Conversion Engineering Conference** Location: Omni Shoreham Hotel, Washington, DC, USA Contact: Eleanor Dicks, 1140 Rockville Place, #138, Rockville, MD, USA 20723 Tel: +1 301 219 8139 Fax: +1 301 946 4374 E-Mail: iecec2002ebdicks@aol.com Deadline: 3/17/02 www: <http://www.iecec2002.com>

August 6 - 8, 2002, * **IEEE Lester Eastman Biennial Conference on High Performance Devices** Location: University of Delaware, Newark, DE, USA Contact: Kimberley Brown, University of Delaware, 140 Evans Hall, Newark, DE, USA 19716 Tel: +1 302 831 3142 Fax: +1 703 696 2206 E-Mail: kibrown@ee.udel.edu Deadline: 4/14/02 www: <http://nina.ecse.rpi.edu/shur/EastmanConference/>

August 12 - 14, 2002, T **International Symposium on Low Power Electronics and Design** Location: The Monterey Beach Hotel, Monterey, CA, USA Contact: Mary Irwin, Penn State University, 227 Pond Laboratory, University Park, PA, USA 16802 Tel: +1 814 865 1802 Fax: +1 814 865 3176 E-Mail: mji@cse.psu.edu Deadline: Not Available www: Not Available

August 17 - 19, 2002, T **International Conference on Microwave and Millimeter Wave Technology** Location: Beijing International Convention Center, Beijing, China Contact: Fang Min, Chinese Institute of Electronics, Secretary, ICMMT 2002, PO Box 165, Beijing, China 100036 Tel: +86 10 6828 3463 Fax: +86 10 6828 3458 E-Mail: Not Available Deadline: 3/31/02 www: <http://www.cie-china.org/icmmt2002>

August 26 - 28, 2002, T **IEEE Conference on Nanotechnology** Location: Hilton Crystal City at National Airport, Arlington, VA, USA Contact: Clifford Lau, Office of Naval Research, Code 363, 800 North Quincy Street, Arlington, VA, USA 22217 Tel: +1 703 696 0431 Fax: +1 703 588 1013 E-Mail: lauc@onr.navy.mil Deadline: 3/31/02 www: <http://ewh.ieee.org/tc/nanotech/nano2002>

September 2, 2002, T **High Frequency Post-graduate Student Colloquium** Location: Imperial College of Science, Technology & Medicine, London, United Kingdom Contact: S Lucyszyn, Imperial College of Science, Technology & Medicine, Exhibition Road, London, SW7 2BT, United Kingdom Tel: +44 (0) 20 7594 6167 Fax: +44 (0) 20 7594 6308 E-Mail: s.lucyszyn@ic.ac.uk Deadline: Not Available www: Not Available

September 2 - 6, 2002, T **International Conference on Unsolved Problems of Noise** Location: National Institute of Health Campus, Washington, DC, USA Contact: Sergey Bezrukov, , Tel: Not Available Fax: Not Available E-Mail: bezrukov@helix.nih.gov Deadline: Not Available www: Not Available

September 3 - 6, 2002, T **IEEE Conference on Intelligent Transportation Systems** Location: Westin Stamford Hotel, Singapore Contact: Fwa Fang, National University of Singapore, Singapore 119260 Tel: +65 874 6851 Fax: Not Available E-Mail: cvehead@nus.edu.sg Deadline: Not Available www: Not Available

September 4 - 6, 2002, @ **International Conference on Simulation of Semiconductor Processes and Devices** Location: International Conference Center Kobe, Kobe 6500046, Japan Contact: Toru Toyabe, Department of Computational Science and Engineering, Toyo University, 2100 Kujirai, Kawagoe, Saitama, 350, Japan Tel: +81 492 39 1439 Fax: +81 492 33 9788 E-Mail: t.toya@cs.toyo.ac.jp Deadline: 3/1/02 www: <http://www6.eie.eng.osaka-u.ac.jp/sispad>

September 9 - 14, 2002, T **Symposium on Microelectronics Technology & Devices** Location: Chip in the Pampa, Porto Alegre, RS, Brazil Contact: Jacobus Swart, State University of Campinas, PO Box 6061, R.Pandia Calogeras, 90 13 083-970 Campinas-SP, Brazil Tel: +55 19 3788 7282 Fax: +55 19 3788 4873 E-Mail: jacobus@led.unicamp.br Deadline: 4/15/02 www: <http://www.sbmicro.org.br/sbmicro/xvisb-micro.html>

September 9 - 13, 2002, T **International Crimean Microwave Conference "Microwave & Telecommunication Technology"** Location: Sevastopol Center of Business & Culture, Sevastopol, Ukraine Contact: Pavel Yermolov, P.O. Box 240, Sevastopol, Crimea, Ukraine 99057 Tel: Not Available Fax: +38 0692 555768 E-Mail: weber@execs.com Deadline: 3/13/02 www: <http://ieee.orbita.ru/aps/crim02e.htm>

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September 10 - 13, 2002, T **International Conference on Mathematical Methods in Electromagnetic Theory** Location: National Technical Univ.-Kiev Polytechnic Institute, Kiev, Ukraine Contact: Eldar Veliev, IRE NASU, ul, Peoskury 12, Kharkov 61085, Ukraine Tel: +380 572 140748 Fax: +380 572 140749 E-Mail: veliev@kharkov.ua Deadline: 5/5/02 www: Not Available

September 11 - 14, 2002, T **International Semiconductor Technology Conference** Location: Diamond Hotel, Tokyo, Japan Contact: Ming Yang, Texas Instruments, Inc., 13570 North Central Expressway, Dallas, TX, USA 75243 Tel: +1 972 995 8289 Fax: Not Available E-Mail: myang@ti.com Deadline: 5/3/02 www: <http://www.y-tech.net/ISTC.htm>

September 18 - 20, 2002, T **International Conference on Actual Problems of Electron Device & Engineering** Location: Saratov State Technical University, Saratov, Russia Contact: A Zakharov, Saratov State Technical University, Saratov, Russia Tel: +7 8452 525697 Fax: +7 8452 507563 E-Mail: aaz@star.sstu.runnet.ru Deadline: 3/30/02 www: <http://www.sstu.runnet.ru/apede>

September 22 - 27, 2002, T **International Conference on Ion Implantation Technology** Location: Sagebrush Conference Center, Taos, NM, USA Contact: Bob Brown, ATMI Incorporated, 7 Commerce Drive, Danbury, CT, USA 06810-4169 Tel: +1 505 758 5120 Fax: +1 505 758 5120 E-Mail: bbrown@atmi.com Deadline: 3/1/02 www: <http://www.iit2002.com>

September 23 - 24, 2002, T **European Gallium Arsenide and Related Compound Applications Symposium** Location: Conference Center, Fiera di Milano, Milano, Italy Contact: Giovanni Ghione, Politecnico di Torino, Corso Duca degli Abruzzi 24, 10129 Torino, Italy Tel: +39 011 564 4064 Fax: +39 011 564 4099 E-Mail: ghione@polito.it Deadline: 3/8/02 www: <http://www.eumw.com/gaas.html>

September 23 - 26, 2002, T **International Conference on Actual Problems of Electronic Instrument Engineering** Location: Novosibirsk State Technical University, Novosibirsk, Russia Contact: Alexander Gridchin, Novosibirsk State Technical University, 20 Karl Marx Prospect, Dept. of Applied & Theoretical Physics, Novosibirsk, Russia 630092 Tel: +7 3832 46 0877 Fax: +7 3832 46 0209 E-Mail: algrid@ref.nstu.ru Deadline: 4/15/02 www: <http://www.nstu.ru>

September 24 - 26, 2002, T **European Solid-State Device Research Conference** Location: Florence Conference Center, Florence, Italy Contact: Giorgio Baccarani, University of Bologna, Viale Risorgimento 2, 40136 Bologna, Italy Tel: +39 051 209 3012 Fax: +39 051 209 3074 E-Mail: gbaccarani@deis.unibo.it Deadline: Not Available www: <http://www.essdrc2002.deis.unibo.it>

September 24 - 27, 2002, T **International Conference on Advanced Thermal Processing of Semiconductors** Location: The Coast Plaza Hotel & Suites, Vancouver, Canada Contact: Bo Lojek, 4830 Langdale Way, Colorado Springs, CO, USA 80906 Tel: +1 719 579 8050 Fax: +1 719 579 8082 E-Mail: blojek@atmel.com Deadline: 5/31/02 www: www.rtp-conference.org

September 30 - October 2, 2002, @ **IEEE Bipolar/BiCMOS Circuits and Technology Meeting** Location: Doubletree Hotel, Monterey, CA, USA Contact: Janice Jopke, CCS Associates, 6611 Countryside Drive, Eden Prairie, MN, USA 55346 Tel: +1 612 934 5082 Fax: +1 612 934 6741 E-Mail: jjopke@aol.com Deadline: 3/22/02 www: <http://www.ieee-bctm.org>

October 6 - 10, 2002, T **Electrical Overstress/Electrostatic Discharge Symposium** Location: Charlotte Convention Center, Charlotte, NC, USA Contact: Steven Voldman, IBM Microelectronics, 1000 River Street, MS 972 F, Essex Junction, VT, USA 05452 Tel: +1 802 769 8368 Fax: +1 802 769 9659 E-Mail: a108501@us.ibm.com Deadline: 1/14/02 www: <http://www.esda.org>

October 7 - 10, 2002, * **IEEE International SOI Conference** Location: Colonial Williamsburg Lodge, Williamsburg, VA, USA Contact: Bobbi Armbruster, BACM, 520 Washington Blvd. Suite 350, Marina Del Rey, CA, USA 90292 Tel: +1 310 305 7885 Fax: +1 310 305 1038 E-Mail: bacm@mediaone.net Deadline: 5/10/02 www: <http://www.soiconference.org>

October 7 - 11, 2002, T **European Symposium on Reliability of Electron Devices, Failure Physics and Analysis** Location: Centro Congressi, Rimini, Italy Contact: Ing Fantini, Università degli Studi di Modena e Reggio Emilia, Via Vignolese 905, 41100 Modena, Italy Tel: +39 059 2056 165 Fax: +39 059 2056 129 E-Mail: fantini@dsi.unimo.it Deadline: 4/12/02 www:

October 8 - 12, 2002, * **International Semiconductor Conference** Location: Sinaia Hotel, Sinaia, Romania Contact: Doina Vancu, IMT-Bucharest, CAS Office, PO Box 38-160, Bucharest, Romania 72225 Tel: +40 1 490 82 36 Fax: +40 1 490 82 38 E-Mail: CAS@imt.ro Deadline: 4/15/02 www: <http://www.imt.ro/CAS>

October 10 - 13, 2002, T **International Seminar/Workshop on Direct and Inverse Problems of Electromagnetic and Acoustic Wave Theory** Location: Tbilisi State University, Tbilisi, Georgia, Ukraine Contact: Mykhalyo Andriychuk, Inst. of Applied Problems of Mech. & Math. Of NASU, 3"b" Naukova str, 79601 Lviv, Ukraine Tel: +380 322 651944 Fax: +380 322 637088 E-Mail: andr@iapmm.lviv.ua Deadline: Not Available www: Not Available

October 14 - 16, 2002, T **International Conference on Advanced Semiconductor Devices and Microsystems** Location: The Castle of Smolenice, Bratislava, Slovak Republic Contact: Juraj Breza, Slovak University of Technology, Ikkovicova Street 3, 812 19 Bratislava, Slovak Republic Tel: +421 2 60291328 Fax: +421 2 65423480 E-Mail: breza@elf.stuba.sk Deadline: 4/15/02 www: <http://www.elf.stuba.sk/~asdam>

October 15 - 17, 2002, @ **International Symposium on Semiconductor Manufacturing** Location: Nihon Toshi Center, Tokyo, Japan Contact: Naoji Yamamoto, Cosmos Hongo Building, 8F, 4-1-4, Hongo, Bunkyo-ku, Tokyo 113-0033, Japan Tel: +81 3 3815 8775 Fax: +81 3 3815 8529 E-Mail: issm@rlz.co.jp Deadline: 4/26/02 www: <http://www.issm.com>

October 20 - 23, 2002, * **IEEE Gallium Arsenide Integrated Circuits Symposium** Location: Doubletree Hotel, Monterey, CA, USA Contact: Tim Henderson, 13510 N. Central Expressway M/S 404, Dallas, Texas, USA 75243 Tel: +1 972 994 8538 Fax: +1 972 994 8505 E-Mail: thenderson@tqtx.com Deadline: 4/18/02 www: <http://www.gaasic.org/>

October 20, 2002, T **Gallium Arsenide Reliability Workshop** Location: Doubletree Hotel, Monterey, CA, USA Contact: Anthony Immorlica, BAE Systems, 65 Spit Brook Road, Nashua, NH, USA 03061-0868 Tel: +1 603 885 1100 Fax: +1 603 885 6061 E-Mail: anthony.a.immorlica@baesystems.com Deadline: Not Available www: <http://www.jedec.org/home/gaas>

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