

TABLE OF CONTENTS

TECHNICAL BRIEFS	1
• Marvels in Materials Thin Films—Breakthroughs Thanks to Heterostructures	
UPCOMING TECHNICAL MEETINGS	9
• 2018 IEEE International Electron Devices Meeting (IEDM)	
• 2019 IEEE International Reliability Physics Symposium (IRPS)	
SOCIETY NEWS	13
• Message from EDS President-Elect	
• Report on the Board of Governors Meeting in Cartagena, Colombia	
• Message from Editor-in-Chief	
• 2017 EDS Paul Rappaport Award	
• Latin-American EDS Chapters Meeting in Cartagena	
• 2017 EDS George Smith Award	
• 2019 William R. Cherry Award—Call for Nominations	
• Electron Devices Society Members Named Recipients of 2018 IEEE Medals	
• Congratulations to EDS Members Recently Elected to IEEE Senior Member Grade	
YOUNG PROFESSIONALS	22
• Innovating the Way of Training Future Engineers	
• Young Professionals say “Aloha” at Mentoring Event in Hawaii	
• Women in Engineering Mentoring Event at VLSI 2018	
• Student Members from ED Tsinghua University Student Branch Chapter Present at 2018 Chinese National Science and Technology Week	
• ED NIST Student Branch Chapter organizes EDS Mini-Colloquium on “Quantum Electronics”	
• New Webinars Available in the EDS Collection	
CHAPTER NEWS	28
MQs, DLs and Conference Reports	
• 2018 IEEE Silicon Nanoelectronics Workshop (SNW)	
• New Award at the IEEE International Vacuum Electronics Conference	
• EDS Distinguished Lecturer Mini-Colloquium SiC: Technology, Devices, Modeling	
• Tools Available to Make it Easier to be on Brand	
• SINANO Modelling Summer School and IEEE EDS MQ on Semiconductor Device Modelling	
• EDS Distinguished Lecture—“Nanoelectronics: Towards End of Scaling and Beyond”	
• 2018 International Meeting for Future of Electron Devices (IMFED)	
• Dr. Rajiv Joshi, EDS Distinguished Lecturer presents Variability and Reliability of VLSI Circuits	
• AP/ED Bombay Chapter’s IEEE EDS Mini-Colloquium on “Solar Photovoltaics”	
• 25th International Conference “Mixed Design of Integrated Circuits and Systems”—MIXDES 2018	
• 16th MOS-AK Workshop at ESSDERC/ESSCIRC, Dresden	
• IEEE 2018 Workshop on Microelectronics and Electron Devices	
REGIONAL NEWS	39
EDS MEETINGS CALENDAR	58
EDS MISSION, VISION AND FIELD OF INTEREST	60

TECHNICAL BRIEFS

MARVELS IN MATERIALS THIN FILMS—BREAKTHROUGHS THANKS TO HETEROSTRUCTURES



*Simon Deleonibus,
Past Chief Scientist
CEA-LETI*

What is the commonality between SiGe, InGaN and inorganic or organic TFTs, besides the fact that they are based on semiconductors? In all cases, when used as thin film, they are superior and have remarkable properties which can qualify them as marvels of the Electronics and Microelectronics. Heterostructures are the micro-electronic fuel to generate electrical amplification and light emission or absorption. SiGe, InGaN and TFTs, have demonstrated their extraordinary power because we can build heterostructures that evidence and value the exceptional properties that thin films can effect on their environment.

Many years or decades of struggles have been necessary worldwide to come out with commercial applications of high societal impact. In this issue, we illustrate, by three examples, how innovation in materials science and technology had an extraordinary impact on microelectronics advancement. Today’s mobile smart phones are a good example of the combination of integrated multifunctions including the RF Front end, backside lighting and display technology in a single device, which occupies our daily life and is made possible thanks to the science and technology advancements using thin film materials, in little over a century. Thin film heterostructures’ beauty resides as well in the powerful capability to pervade and extend the technology in other domains such as sensors, Si

(continued on page 3)

YOUR COMMENTS SOLICITED

Your comments are most welcome. Please write directly to the Editor-in-Chief of the Newsletter at clilley@uic.edu

ELECTRON DEVICES SOCIETY

President

Fernando Guarin
GlobalFoundries
E-mail: fernando.guarin@ieee.org

President-Elect

Meyya Meyyappan
NASA Ames Research Center
E-mail: m.meyyappan@nasa.gov

Treasurer

Subramanian S. Iyer
UCLA
E-mail: iyer@ieee.org

Secretary

Jacobus Swart
FEEC/UNICAMP
E-mail: jacobus@fee.unicamp.br

Jr. Past President

Samar Saha
Prosopient Devices
E-mail: samar@ieee.org

Sr. Past President

Albert Z.H. Wang
University of California, Riverside
E-mail: aw@ee.ucr.edu

Vice President of Membership and Services

Ru Huang
Peking University
E-mail: ruhuang@pku.edu.cn

Vice President of Publications and Products

Tsu-Jae King Liu
University of California at Berkeley
E-mail: king@eecs.berkeley.edu

Vice-President of Regions/ Chapters

M.K. Radhakrishnan
NanoRel
E-mail: radhakrishnan@ieee.org

Vice President of Technical Committees & Meetings

Ravi Todi
GlobalFoundries
E-mail: rtodi@ieee.org

IEEE Newsletters

Theresa Smith
IEEE Operations Center
E-mail: tsmith@ieee.org

Operations Director

James Skowrenski
IEEE Operations Center
E-mail: j.skowrenski@ieee.org

Content Management

Joyce Lombardini
IEEE Operations Center
E-mail: j.lombardini@ieee.org

EDS Board of Governors (BoG)

Elected Members-at-Large

Elected for a three-year term (maximum two terms) with 'full' voting privileges

2018	TERM	2019	TERM	2020	TERM
Navakanta Bhat	(1)	Joachim N. Burghartz	(1)	Roger Booth	(1)
Daniel Mauricio	(2)	Ru Huang	(2)	Mukta Farooq	(2)
Camacho Montejó	(1)	Shuji Ikeda	(1)	Edmundo A. Gutierrez-D.	(1)
Simon Deleonibus	(1)	Meyya Meyyappan	(1)	Benjamin Iniguez	(1)
Meikei leong	(1)	Arokia Nathan	(1)	Carmen M. Lilley	(2)
Murty Polavarapu	(1)	Jacobus VV. Swart	(2)	Durga Misra	(2)
Ravi M. Todi	(1)	Bin Zhao	(1)	Manoj Saxena	(1)
Douglas P. Verret	(2)			Sumant Sood	(1)

NEWSLETTER EDITORIAL STAFF

Editor-In-Chief

Carmen M. Lilley
University of Illinois at Chicago
E-mail: clilley@uic.edu

REGIONS 1-6, 7 & 9

Eastern, Northeastern & South-eastern USA (Regions 1,2 & 3)

Rinus Lee
GlobalFoundries
E-mail: rinuslee@ieee.org

Central USA & Canada (Regions 4 & 7)

Michael Adachi
Simon Fraser University
E-mail: mmadachi@sfu.ca

Southwestern & Western USA (Regions 5 & 6)

Kyle H. Montgomery
Air Force Research Laboratory
E-mail: kyle.h.montgomery@ieee.org

Latin America (Region 9)

Edmundo A. Gutierrez-D.
INAOE
E-mail: edmundo@inaoep.mx

REGION 8

Eastern Europe

Daniel Tomaszewski
Institute of Electron Technology
E-mail: dtomasz@ite.waw.pl

Scandinavia & Central Europe

Marcin Janicki
Lodz University of Technology
E-mail: janicki@dmcs.pl

UK, Middle East & Africa

Jonathan Terry
The University of Edinburgh
E-mail: jonterry@ieee.org

Western Europe

Mike Schwarz
Robert Bosch GmbH
E-mail: mike.schwarz1980@googlemail.com

REGION 10

Australia, New Zealand & South East Asia

P Sushitha Menon
Universiti Kebangsaan Malaysia
E-mail: susi@ukm.edu.my

Northeast Asia

Kuniyuki Kakushima
Tokyo Institute of Technology
E-mail: kakushima@ep.titech.ac.jp

East Asia

Ming Liu
Institute of Microelectronics
E-mail: liuming@ime.ac.cn

South Asia

Manoj Saxena
University of Delhi
E-mail: msaxena@ieee.org

CONTRIBUTIONS WELCOME

Readers are encouraged to submit news items concerning the Society and its members. Please send your ideas/articles directly to either Editor-in-Chief or the Regional Editor for your region. The e-mail addresses of all Regional Editors are listed on this page. E-mail is the preferred form of submission.

NEWSLETTER DEADLINES

ISSUE	DUE DATE
January	October 1st
April	January 1st
July	April 1st
October	July 1st

The EDS Newsletter archive can be found on the Society web site at <http://eds.ieee.org/eds-newsletters.html>. The archive contains issues from July 1994 to the present.

IEEE Electron Devices Society Newsletter (ISSN 1074 1879) is published quarterly by the Electron Devices Society of the Institute of Electrical and Electronics Engineers, Inc. Headquarters: 3 Park Avenue, 17th Floor, New York, NY 10016-5997. Printed in the U.S.A. One dollar (\$1.00) per member per year is included in the Society fee for each member of the Electron Devices Society. Periodicals postage paid at New York, NY and at additional mailing offices. Postmaster: Send address changes to IEEE Electron Devices Society Newsletter, IEEE, 445 Hoes Lane, Piscataway, NJ 08854.

Copyright © 2018 by IEEE: Information contained in this Newsletter may be copied without permission provided that copies are not used or distributed for direct commercial advantage, and the title of the publication and its date appear on each photocopy.



MARVELS IN MATERIALS THIN FILMS—BREAKTHROUGHS THANKS TO HETEROSTRUCTURES

(continued from page 1)

CMOS transistor chip performance enhancement, and public lighting.

The author of this article asked the pioneers in some selected domains to talk about their experience on the way these materials and their process came into play and produced marvels that we find commonly today as being part of our daily life. Joachim Burghartz of IMS CHIPS in Stuttgart in Germany, Shuji Nakamura of UC Santa Barbara in the US, and Arokia Nathan, of University of Cambridge in the UK, accepted to share their experience. Their constructive and knowledgeable cooperation is particularly acknowledged.

SiGe Heterostructures

Heterostructures have often been mentioned in the case of superlattices based on III-V compounds (see hereafter in the InGaN Double Heterostructure section). They can effect in introducing potential barriers, increase electric fields or modify the band structure of the surrounding materials. Pioneering work on SiGe/Si superlattices growth started by Kasper (Applied Physics 1975) at AEG and John Bean's team (Applied Physics Letters, Jan. 1984) at Bell Labs, both with Molecular Beam Epitaxy (MBE). They demonstrated the feasibility of Si_{1-x}Ge_x pseudomorphic epitaxial growth. Following these preliminary studies, exploratory research on SiGe limited reaction processing started in Jim Plummer's group at Stanford. This effort moved to IBM, thanks to the former Stanford PhD graduates Hans Stork, Gary Patton, David Hareme and Emmanuel Crabbé. Initially, they wished to realize an idea proposed by Herbert Kroemer in 1954 on the benefit on the base transit time from establishing a drift region between the emitter and the collector through

the base region by a graded band-gap junction. By that time, Kroemer already had mentioned a SiGe alloy as a possible solution.

The first publications reporting working SiGe bipolar transistors that were superior in performance when compared to their Si counterparts appeared in 1988 from IBM (Patton et al) and 1989 from Stanford (King et al) (Figure 1) both in EDL, reporting on two radically different base materials featuring 12% and 31% Ge, 1000 Å and 1300 Å thick, respectively. In the first case at IBM, the collector, the strained base and emitter were obtained by Molecular Beam Epitaxy, whereas the Stanford team, in the second case, used the limited reaction processing mentioned, a rapid thermal CVD technique. Band offsets between the SiGe alloy base and collector/emitter were clearly observed, reporting increased current gains and Early voltages but still remaining unexplained interface defects and possible SiGe film instability. *In the late 1980's, IBM was looking for a fundamental technology improvement of their implanted-base double-poly self-aligned transistor technology, which was limited in base width and transit frequency. At that time I was a PostDoc at IBM,"* says Joachim Burghartz. *"We were able to demonstrate the first selective epi base transistor, which was published in EDL in 1988, but gave up on any further effort due to several technical difficulties we encountered, particularly loading effects of the selective epitaxy process and resistance by IBM's product division to apply selective epi in manufacturing. Ironically, the selective epi base idea for SiGe bipolar was picked up by NEC and Hitachi in Japan."* First results were based on selective MBE and were published at IEDM 1990 by

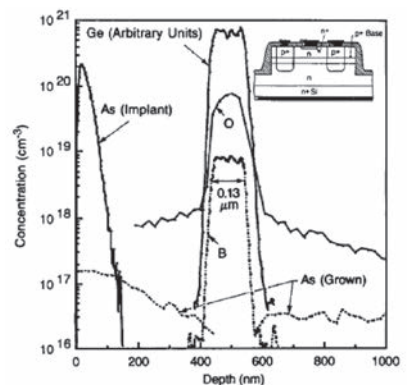


Fig.1. SIMS vertical profile of SiGe HBT. The SiGe film contained 31% Ge (Stanford University IEEE Electron Device Letters, Feb 1989)

Fumihiko Sato et al. from NEC. Hat-suya Oda from Hitachi showed 130 GHz SiGe selective epi base transistors at IEDM 1997.

All together, three SiGe epitaxial growth techniques and three self-aligned SiGe bipolar transistor technologies were investigated at IBM at the same time. Bernie Meyerson used UHV/CVD epitaxy at temperatures as low as 500 °C. Subu Iyer used on MBE and Tom Sedwick worked on APCVD. Achieving high performance SiGe base HBT competing with established bipolar devices met several major technical hurdles to make it manufacturable and cost effective. Struggles had to be faced with SiGe film stability compatible with short base transit time, sufficiently high Gummel number, minimum parasitics and, through modest Ge content, maintaining the intrinsic SiGe base strain during high temperature dopant activation anneals and preventing from dopant outdiffusion from the intrinsic base. A double self-aligned polysilicon architecture responded to the first two requirements.

"Gary Patton and colleagues (Figure 2) demonstrated a superior SiGe



Fig.2. IBM SiGe Team in 1990 showing from left to right side: Joachim Burghartz, Hans Stork, Gary Patton, Jim Comfort, Jack Sun, Edouard de Frésart, David Hareme and Emmanuel Crabbé (courtesy J. Burghartz)

strated record circuit performance for SiGe versus Si bipolar devices for a double-poly structure and for a single-poly device, showing ring oscillator delays below 30 ps”

The last hurdle was overcome by incorporating Carbon in SiGe: very small amounts (less than 1%) were necessary to limit Boron outdiffusion from the intrinsic base, especially during high temperature anneals or by transient enhanced diffusion. High Carbon content induced a band off-sets and compensated SiGe/Si strain from compressive to tensile. The credit for the real breakthrough research on SiGe:C goes to IHP in Frankfurt/Oder (Jörg Osten and co-workers at IEDM 1999) but the first demonstration was achieved by Princeton (Jim Sturm’s team, IEDM 1996).

“Today, the SiGe and SiGe:C epitaxy processes look more like Tom Sedgewicks single-wafer APCVD, the device integration is double-poly self-aligned and the SiGe base profile reflects a trade-off between a heterojunction bipolar device and a drift transistor” concludes Burghartz. Most of the results obtained during the research on SiGe HBT have been transferred to the achievement of BiCMOS architectures, thanks to the growing business of telecommunications requesting low power as well as high frequency capabilities. Basically all BiCMOS technologies on the market today are based on SiGe or SiGe: C. David Hareme and B. Meyerson at IBM mainly contributed to its popularity. Not to forget former IBMer John Cressler, now at Georgia Tech and previously at Auburn University, who educated numerous students who are keeping the SiGe technology advancement and industrial application going.”

SiGe today is also used to locally strain bulk pMOS channels (Intel at IEDM 2004) by epitaxial growth in the source/drain areas. It is also applied to add uniaxial strain to already biaxially strained ultra thin body n(Si) and p(Si_{0.7}Ge_{0.3})-channel SOI transistors, thanks to respectively

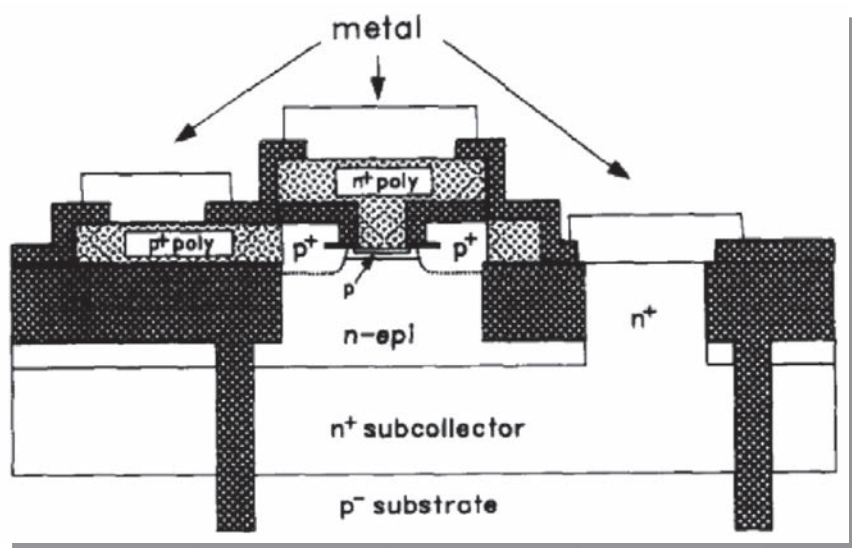


Fig.3. SiGe base double poly HBT by the SEEW (Selective Epitaxial Emitter window) architecture (IBM, IEDM 1990)

bipolar transistor in a paper in the IEEE Electron Device Letters in April 1990, using a built-in drift field in the base region according to Herbert Kroemer’s old idea of the drift transistor and exploiting Bernie Meyerson’s UHV/CVD epitaxy. At about the same time Erich Kasper’s group at AEG in Germany worked on an implementation of Kroemer’s idea

of the wide bandgap emitter, though using MBE which was unlikely transferable to a manufacturing process. For about a couple of years it was a race for record transit frequencies between IBM’s SiGe drift transistor concept and AEG’s SiGe HBT.”, proceeds Burghartz. However, these structures were not self-aligned. “At IEDM in 1990 (Figure 3), we demon-

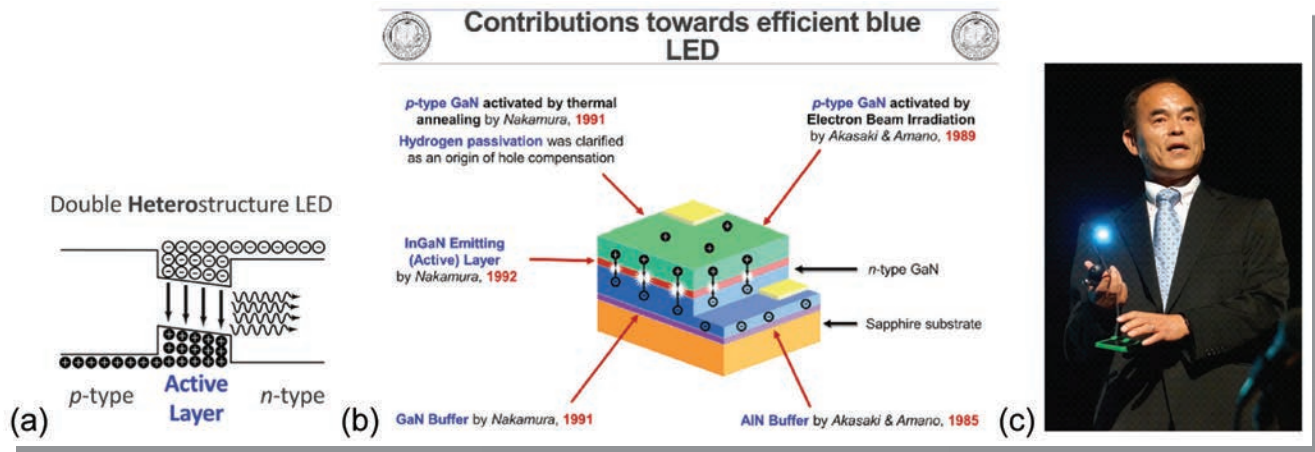


Fig.4. LED principles and history. (a) Double Heterostructure band diagram and light emission process; (b) Blue LED history in Nakamura's 2014 Nobel lecture; (c) Shuji Nakamura showing a blue LED during his Nobel lecture (all figures by courtesy of S. Nakamura)

SiGe:C and SiGe elevated sources and drains (LETI at VLSI Technology Symposium 2005; LETI, STMicro, IBM at IEDM 2013). The multilayered SiGe/Si, featuring SiGe layers thinner than a critical thickness depending on Ge content, allows to build up to 19 multiple defect free stacked Gate all Around Si Nanowires channels (LETI, STMicro at IEDM 2006), delivering MOSFETs record saturation current per footprint. The work achieved on Si/SiGe heterostructures since the 1980s is for sure the foundation of the extension to modern CMOS technology.

InGaN Double Heterostructures for Blue LEDs and White Lighting

As we already mentioned, the phenomenon of seeking Graals is not limited to microelectronics. In the area of photonics, the invention of the blue LED is also emblematic whereas it made white lighting possible and up-scalable. The realization of the first room temperature blue emitting InGaN (Nakamura 1992) was a determinant step to further complete the set of red and green LEDs that would make white lighting possible. In this field, Herbert Kroemer left his marks as he proposed the SiGe base/Si heterostructures drift region to improve HBT performance (1954), already mentioned hereabove in the SiGe section. Later, Kroemer (1963) introduced

the double heterostructure (DH) based on high band gap/low band gap materials to realize high efficiency lasers and LEDs (Figure 3a). There were many hurdles to be overcome to realize cheap and reliable, highly performant GaN/InGaN (DH). First, the GaN epitaxial growth by MOCVD on a sapphire requested high crystalline quality (Akasaki and Amano 1985), and further crystal improvements (Nakamura, Two flow mode MOCVD 1991).

Professor Shuji Nakamura, 2014 Nobel Prize in Physics, kindly accepted to give us some details concerning his research: "In 1989, I started GaN growth after getting a commercially available MOCVD, after coming back to Japan from USA. I tried to grow GaN epitaxial films on sapphire substrates for a couple of months. However, I mostly did not observe GaN deposition, or even if there was growth, the color of the GaN film was black. Then, I started to modify the MOCVD system every morning by cutting and welding the quartz, graphite, and other materials of the reactor. Every afternoon, I ran the epitaxial growth of GaN at least 3–5 times to check the new modifications by changing the growth conditions. I continued in this manner every day for one-and-a-half years. In October 1990, I completed a totally new MOCVD reactor, named the two-flow (TF) MOCVD. Conventional MOCVD

had one horizontal flow to achieve a laminar flow. I added another vertical flow to suppress the thermal convection caused by the high temperature and atmospheric pressure growth. When I grew undoped GaN using the TF-MOCVD, the residual electron mobility was the highest ever reported. In my life, I never experienced a world record. This was my first experience. Since the invention of the TF-MOCVD, and owing to the system's performance, I was able to achieve breakthroughs in the growth of GaN, p-type GaN, InGaN, blue LEDs, and blue laser diodes every 2–3 months."

Yet, several key breakthroughs were still needed to improve the TF-MOCVD technique to make LEDs working efficiently. A final interstitial H⁺ depassivation of holes was necessary to obtain highly conductive Mg doped p-type GaN (Nakamura 1992, Akasaki and Amano 1989).

Nakamura reports: "In 1991, I obtained p-type GaN films by thermal annealing for the first time, and I could finally clarify the mechanism of Hydrogen passivation as a hole compensation. Since the beginning of GaN research in the 1960s, this hydrogen passivation of the Mg acceptors had prevented many researchers from obtaining p-type GaN films.

In 1992, I also grew the first InGaN single crystal layers which showed

the first band to band blue emission in PL and EL at room temperature. These InGaN layers have been used as emitting layers in all of the blue/green/white LEDs and all of the violet/blue/green semiconductor lasers. Without this invention of InGaN layers, there would have been no blue/green/white LEDs and no violet/blue/green semiconductor laser diodes."

There has never been any collaboration with the two other 2014 Nobel prize co-recipients Professors Akasaki and Amano of Nagoya University. "Their contribution was: 1) the development of AlN buffer layer to improve the crystal quality of GaN in 1986. 2) the demonstration of the first p-type GaN using electron beam irradiation. However, they could not understand why they got p-type GaN. See figures 3b and c.

Finally, a demonstration of a bright Blue InGaN/GaN DH emitting 1 candle was obtained in 1994(Nakamura). The Indium content allowed to tune the LED colour emission from yellow to blue. Commercialization by Nichia Corp. of white lighting devices based on InGaN/GaN LED DHs began in 1996.

Nakamura's way to success was atypical and paved with quite a few technical and professional difficulties! From 1979 to 1985, Nakamura worked for Nichia Chemical Ind. to develop GaP and GaAs bulk crystal as a source material for conventional infrared and red LEDs. The sales of those products were poor due to tough competition with big semiconductor and LED companies. His curiosity from the reading of literature was far the strongest to pursue the idea of developing blue LED: he biggest problems in LEDs came from the absence of efficient blue and green devices. If efficient blue and green LEDs were available, there would be a huge market for LEDs. So, I gradually wanted to develop the blue LED myself". He was lucky to get his company president to provide him a funding to continue his research, went abroad to

the University of Florida, one year from 1988, as a visiting researcher to study GaAs on Si using MOCVD, while his boss rejected his funding request to work on blue LED! "One year later, in 1989, I came back to Japan to start the blue LED research. At that time, my dream became getting a Ph.D. degree instead of developing blue LEDs. I never expected that I could invent the blue LEDs myself!"

The inventions brought by Nakamura, Akasaki and Amano thanks to their flexible up and down scalability, make accessible since the beginning of mass production in 1993, new lighting modes for mobile phones and large area home displays, automotive, agriculture, healthcare, etc... with the possibility to invent new lighting devices shapes.

Nakamura asserts on the huge revolution started in the lighting area: "The application with the greatest impact to the world's energy consumption is that of general illumination, recognizing that one quarter of all the world's electricity is used for lighting. LED Light bulbs are more than ten times efficient than incandescent bulbs, and they last for 50 years! At their current adoption rates, by 2020 LEDs can reduce the world's need for electricity by the equivalent of nearly 60 nuclear power plants. LEDs are also efficient enough to be driven by a simple solar cell powered battery. Now this clean and inexpensive technology can help bring light to millions of people around the world who don't have access to electricity. LED Lighting has now truly become a reality. Nowadays we can buy energy efficient LED Light bulbs at the super-market and help reduce energy use. I hope that everyone can use efficient LED Lighting to save energy and do their part to reduce Global Warming."

White lighting based on LEDs is massively used today and has revolutionized lighting thanks to its efficiency and device lifetime: 40% of world electricity consumption would be saved by 2030. Nowadays, LED manufacturers are trying to optimize

the power efficiency and necessary trade off with reliability of the devices. "To maintain high light output, manufactures may use multiple LEDs in parallel, effectively increasing the overall active area and hence reducing current density. The primary origin of efficiency droop is Auger recombination or carrier overflow process."

"An alternative method to produce white light is by using a blue laser, as opposed to an LED, in combination with a phosphor. Above the lasing threshold, the carrier density is clamped at threshold, fixing its density. Increases in carrier density beyond the threshold density immediately contribute to stimulated emission, or lasing. Thus, the carrier density is maintained at the lower, threshold density, prohibiting it from reaching densities where the Auger recombination process becomes the dominant recombination process. Auger recombination, with the resulting efficiency droop, does not appreciably occur in blue laser diodes.

Current commercial blue lasers have already demonstrated comparable external quantum efficiencies to those of blue LEDs at significantly higher current densities, and hence light output. It is therefore of great interest to further pursue lasers as they have the potential of operating at high current densities, resulting in white light sources with staggering light output.

While laser based lighting has the potential of being more efficient with smaller chip sizes with a very high current density region, it also offers intrinsic directionality of the light output as an ultimate point light source—a feature that car manufacturers have already leveraged in their high-end vehicles ...for their headlamps, allowing drivers to see further down the road without blinding oncoming traffic. Future modifications to the laser based lighting technology may well enable the next generation of white lighting with higher efficiencies at lower cost."

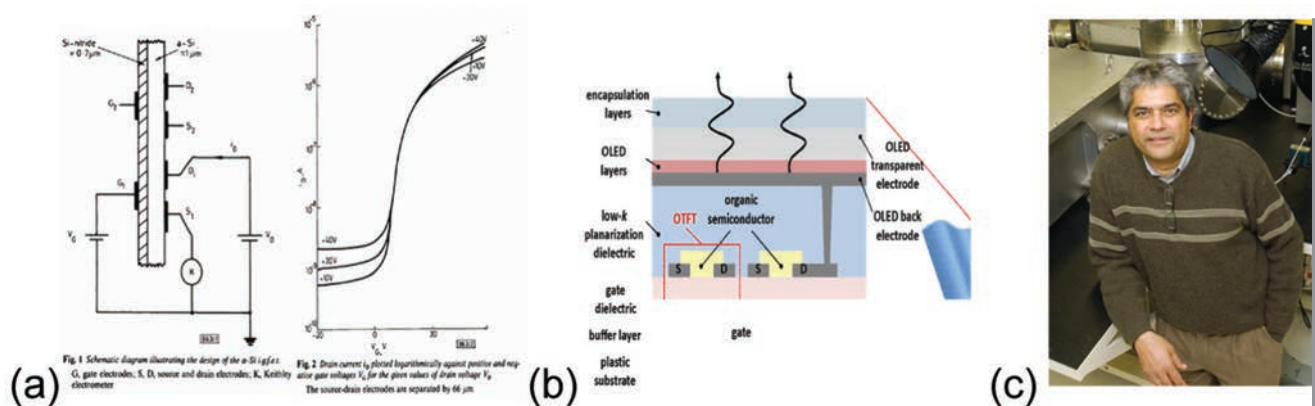


Fig. 5. (a) Detail of first publication on amorphous Silicon IGFET, by P.G. Le Comber, W.E. Spear and A. Ghaith in *Electronic Letters*, February 5, 1979, suggested to address displays active matrix LCDs; (b) AMOLED addressed by OTFTs on flexible substrate; (c) Arokia Nathan (b and c by courtesy of A. Nathan)

The innovations in white lighting by LED represent a major benchmark event of the end of the 20th century history. The adventure is starting and will continue as long as imagination can permit!

Between a SiHTFT and OTFT

Displays certainly have a very long history dotted with so many disruptions.

Coming up with a low cost solution, capable of meeting high vision quality requirements, together with High mechanical durability and robustness, weight and low power consumption, has been a great challenge since the invention of television. The implementation of transistors and light emitting devices both made on thin films, inorganic or organic, have brought new opportunities such as the volume reduction from 3D to 2D and back to 3D, with different perspectives (!), in many new situations and purposes. The display has become ubiquitous in all areas in our daily life as consumers or professionals have been invested by displays. They are multiformed and must adapt to different substrates: from stainless steel to glass or paper, plastic foils and organic substrates, and many kind of fabrics such as clothing! Today all displays are the active-matrix type, whereas the simple cross point interconnect system (or the passive matrix) of the beginning was a se-

rious hurdle for mastering their power consumption and poor resolution. Concomitantly, Thin Film Transistors (TFTs), have followed MOSFET history since the beginning of their developments. Nevertheless and ironically, the challenge of large area electronics with the hybrid integration of the vision grid, produced at low cost, was specific to the world of displays. It was the price to pay to win the struggle of entering into the consumer electronics business.

The ancestor of TFT was described by its function as an Insulated Gate Field Effect Transistor (IGFET). The device imagined by the Dundee University team were considered as laboratory characterization tools for materials development purposes (Figure 4a).

In the late 1960s and 1970s, the research on amorphous semiconductors and more specifically amorphous silicon (a-Si) were very active worldwide under the seminal impulses of N.F. Mott (University of Cambridge, UK), 1977 Nobel Prize. Arokia Nathan comments: *"Prior to the disclosure of the TFT, display panels (based on twisted nematic mode liquid crystal sandwiched between polarisers) were addressed by a matrix of row and column (X-Y) interconnecting lines. These were referred to as passive matrix displays. T.P. Brody; J.A. Asars; G.D. Dixon had reported a display based on ac-*

tive matrix but using CdSe devices in 1973 in IEEE Trans-ED. But the material led to large charge leakage in the off-state of the transistor serving to undermine display quality. Here the TFT is placed at the junction of the X-Y matrix which when addressed or switched on will rotate the plane of polarization of the liquid crystal thereby modulating the light transmitted through the liquid crystal. The a-Si TFT had far better long-term stability than the II-VI counterpart compounds." The hydrogenation of glow discharge deposited, so-called today: Plasma Enhanced Chemical Vapor Deposition (PECVD), a-Si brought in by the Dundee team was for sure a major roadblock to overcome before the association of TFT and Liquid Crystals to make large area and reliable flat displays (LCD) in the early 1980s. The drastic passivation and reduction of defects made n and p (type doping of a-Si) possible and drastically increased the mobility in the material. Prior to this was the discovery of the "liquid crystalline nature of cholesterol" in 1888 by Friedrich Reinitzer and further works of Otto Lehmann (1904) on Liquid Crystals and Charles Mauguin (1911), who experimented the first "liquid crystal confinement" in between two electrodes! Commercial devices became available not before the 1960s Nathan says: *"Between 1964 and 1968, at the*

RCA David Sarnoff Research Center in Princeton, New Jersey, George Heilmeyer with Louis Zanon and Luciano Barton, devised a method for electronic control of light reflected from liquid crystals and demonstrated the first liquid crystal display. This was the passive matrix display."

Looking back to the past makes us appreciate even more the many breakthroughs this field has gone through, in a 50 years time frame. That is especially due to the wide range of applications and also the huge public that is eager to use them in so many different ways.

"New generations of displays have evolved—a good example being the active matrix organic LED display or AMOLED displays (Figure 4b) which come in the form of cell phone displays and TV screens. Other displays include the electrophoretic display which is used in E-books. TFTs have also evolved and they can be made with organic materials making them amenable to printing technologies. This has now led to the emergence of flexible electronics and displays which can be rolled/folded and is expected to

soon hit the market. Pushing more into the future, are wearable devices for health care monitoring where power consumption can become a critical issue making ultra-low power operation a must!," says Nathan.

Light emission from Organic materials has been investigated since the 1950s (Bernanose et al. J. Chim. Phys., 1953). However, the world's first working OLED was demonstrated in 1987 by Ching W. Tang and Steven Van Slyke at Eastman Kodak. Active matrix OLEDs have established their huge success thanks to their lower power consumption (a factor of 10 less), higher reliability and application on large surfaces free of form factor. Main display and TV manufacturers such as Samsung, SONY, LG have been very active in the production of high capacity large area displays since the mid years 2000, still relying on the success of TFTs to address the light emitting devices. Today, 65 inches diagonal rollable TVs based on AMOLED technology have been demonstrated (by LG in the January 2018 CES).

OTFTs have now emerged because their low process tempera-

ture that matches well for the multiple applications of AMOLEDs on various substrates such as paper, plastic, etc... Although high quality a-SiH could be obtained at these low process temperatures it is form-factor constrained. The discovery of conductive polymers by Shirakawa, Heeger and MacDiarmid in 1977 was certainly a sign to boost the organic electronics field. They were awarded the Chemistry Nobel Prize in 2000. Significant conductivity/doping results comparable to inorganic semiconductors were obtained in the 1980s and with the achievements of the first organic channel transistors based on poly-acetylene/polysiloxane (Ebisawa et al, JAP 1983). Given the wide scope of the applications they might serve, AMOLED and OTFTs already have a huge societal impact. Significant work (see for example Nathan's team publications in Science, October 2016 and IEEE J. ESTCS March 2017) has been reported to compensate material shortcomings to extend the lifetime of systems based on disordered materials encompassing TFTs and OLEDs.

YOUR CHAPTER COULD BE MISSING IMPORTANT NOTICES AND FUNDING OPPORTUNITIES!

Please remember, whenever there is a change to Chapter Officers, both IEEE and EDS must be notified. Please follow these two steps:

- 1) Report officer changes to IEEE via the vTools Officer Reporting form:
<https://officers.vtools.ieee.org/> (access to vTools requires use of an IEEE account).
- 2) Report officer changes to EDS by completing the Chapter Chair Update Form:
<https://ieeeforms.wufoo.com/forms/pgu6n1i1ixepnu/>

Thank you in advance for your assistance.

UPCOMING TECHNICAL MEETINGS

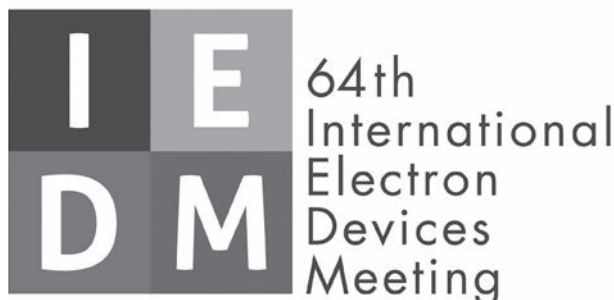
2018 IEEE INTERNATIONAL ELECTRON DEVICES MEETING (IEDM) TO SHOWCASE BREAKTHROUGHS IN SEMICONDUCTOR TECHNOLOGY

- *This year's theme is "Device Breakthroughs from Quantum to 5G and Beyond" – chosen to reflect the expanding reach of electronics technology in society*
- *An extensive offering of tutorials, short courses, focus sessions, panels, poster sessions from affiliated groups and supplier exhibits complements the technical program*
- *New luncheon format to be introduced: Industry leaders will engage the audience on the state of the industry and discuss careers in device and VLSI technology*

SAN FRANCISCO, CA (August 14, 2018)—The 64th annual IEEE International Electron Devices Meeting (IEDM), the world's largest, most influential forum for technologists to unveil breakthroughs and new concepts in transistors and related micro/nanoelectronics devices, will be held December 1–5, 2018 at the Hilton San Francisco Union Square hotel. The late-news submission deadline is September 10.

The IEDM's tradition of spotlighting more leading work in more areas of the field continues, even as the conference evolves to support the interdisciplinary and continuing educational needs of the scientists, engineers and students whose efforts make possible the expansion of the worldwide electronics industry.

"We live in a time when electronics technology touches more aspects of business and industry than ever before," said Kirsten Moselund, IEDM 2018 Publicity Chair and Research Staff Member at IBM Research—



Zurich. "No matter what their specialty is, attendees will come away from the conference with a deeper understanding of the challenges and opportunities before them."

"In terms of industrial applications, the evening panel session on EUV will give attendees the opportunity to explore and debate this emerging technology with the very people who are driving it forward," said Rihito Kuroda, IEDM 2018 Publicity Vice Chair and Associate Professor at Tohoku University. "This is just one way in which the IEDM conference gives people insights into the technologies that will become mainstream in a few years."

Here are details of some of the talks and events that will take place at this year's IEDM. The papers to be presented in the technical sessions will be chosen in late September and highlights from them will be forthcoming soon thereafter:

Focus Sessions

- **Quantum Computing**—Quantum computing will enable new types of algorithms to tackle problems in areas from materials science to medicine to artificial intelligence. We are still in early stages, facing fundamental questions such as: What is the best way to implement a quan-

tum bit of information? How to connect them together? How to scale to larger systems without being overwhelmed by errors? This session brings together experts at the forefront of quantum computing research. Starting from an applications perspective, attendees will hear about different approaches to address fundamental questions at the device level; the progress achieved so far; and next steps.

- **Materials and Device Challenges for Near-Term Superconducting Quantum Processors**, Jerry Chow, IBM
- **Towards Scalable Silicon Quantum Computing**, Maud Vinet, CEA-Leti
- **Silicon Isotope Technology for Quantum Computing**, Kohei Itoh, Keio University
- **Qubit Device Integration Using Advanced Semiconductor Manufacturing Process Technology**, Ravi Pillarisetty, Intel
- **Scalable Quantum Computing with Single Dopant Atoms in Silicon**, Andrea Morello, Univ. New South Wales
- **Majorana Qubits**, Leo Kouwenhoeven, Microsoft
- **Future Technologies Towards Wireless Communications: 5G and Beyond**—5G technology will drastically reduce limitations on accessibility, bandwidth, performance, and latency, but as it triggers fundamentally new applications it also will impose unique hardware requirements. This focus session will set a big picture view

and then narrow down to how innovations in CMOS technologies, devices, filters, transceivers and antennas are coming together to enable the 5G platform.

- *Intel 22 nm FinFET (22FFL) Process Technology for RF and mmWave Applications and Circuit Design Optimization for FinFET Technology*, Hyung-Jin Lee, Intel
- *100–340 GHz Systems: Transistors & Applications*, Mark Rodwell, Univ. California-Santa Barbara
- *GaN HEMTs for 5G Base Station Applications*, Shigeru Nakajima, Sumitomo Electron Devices
- *Highly Integrated mm-Wave Transceivers for Communication Systems*, Vadim Issakov, Infineon
- *BAW Filters for 5G Bands*, Robert Aigner, Qorvo
- *Reconfigurable Micro/Millimeter-wave Filters*, Dimitrios Peroulis, Purdue
- **Challenges for Wide Bandgap Device Adoption in Power Electronics**—Wide bandgap (WBG) power devices offer potential savings in both energy and cost. But converters powered by WBG devices require innovation at all levels, entailing changes to system design, circuit architecture, qualification metrics and even market models. Can SiC or GaN push beyond what silicon can possibly achieve? What are the big challenges researchers should answer over the next decade? A team of experts will interpret the landscape and discuss challenges to the widespread adoption of these technologies.
- *GaN and SiC Devices for Automotive Applications*, Tetsu Kachi, Nagoya University
- *SiC MOSFET for Mainstream Adoption*, Peter Friedrichs, Infineon
- *GaN Power Commercialization with Highest Quality-Highest*

Reliability 650 V HEMTs- Requirements, Successes and Challenges, Primit Parikh, Transphorm

- *The Current Status and Future Prospects of SiC High Voltage Technology*, Andrei Mihaila, ABB
- *Barriers to Wide Bandgap Semiconductor Device Adoption in Power Electronics*, Isik Kizilyalli, ARPA-E
- *High to Ultra-High Voltage SiC Power Device Technology*, Yoshiyuki Yonezawa, AIST
- *Effects of Basal Plane Dislocations on SiC Power Device Reliability*, Robert E. Stahlbush, Naval Research Laboratory
- **Interconnects to Enable Continued Technology Scaling**—BEOL copper (Cu) interconnects are close to end-of-life as a manufacturing technology, while the increasing complexity of MEOL processes requires novel materials. Also, the end of the Cu roadmap will coincide with significant changes in the dominant transistor architecture, and therefore the interaction between transistor architecture and interconnect will drive future interconnect development. This session provides a holistic perspective of interconnect scaling challenges and solutions. It will address the drivers of future interconnect architectures, the process options likely to be implemented in manufacturing, and how they will be tuned to ensure circuit reliability is maintained.
- *Interconnect Design and Technology Optimization for Conventional and Exotic Nanoscale Devices: A Physical Design Perspective*, A. Naeemi, Georgia Tech
- *Mechanisms of Electromigration Damage in Cu Interconnects*, C. K. Hu, IBM
- *Interconnect Metals Beyond Copper: Reliability Challenges and Opportunities*, K. Croes, Imec
- *Microstructure Evolution and Effect on Resistivity for Cu Na-*

no-interconnects and Beyond, Paul Ho, UT Austin

- *Integrating Graphene into Future Generations of BEOL Interconnects*, H.-S. Philip Wong, Stanford
- *Interconnect Trends for Single Digit Nodes*, Mehul Naik, Applied Materials

90-Minute Tutorials—Saturday, Dec. 1

A series of 90-minute tutorial sessions on emerging technologies will be presented by experts in the fields, bridging the gap between textbook-level knowledge and leading-edge current research.

- *Reliability Challenges in Advanced Technologies*, Ryan Lu, TSMC
- *STT-MRAM Design and Device Requirements*, Shinichiro Shiratake, Toshiba Memory
- *Quantum Computing Primer*, Mark B. Ritter, IBM
- *Power Transistors in Integrated BCD Technologies*, Hal Edwards, Texas Instruments
- *Design-Technology Co-optimization at RF and mmWave*, Bertrand Parvais, IMEC
- *Emerging Device Technologies for Neuromorphic Computing*, Damien Querlioz, CNRS

Short Courses—Sunday, Dec. 2

Full-day Short Courses will be held, offering the opportunity to learn about important areas and developments, and to network with experts from around the world.

- **It's All About Memory, Not Logic!**, organized by Nirmal Ramaswamy, Micron
- *DRAM: Its Challenging History and Future*, Dong Soo Woo, Samsung
- *3D Flash Memories: Overview of Cell Structures, Operations and Scaling Challenges*, Makoto Fujiwara, Toshiba Memory Corporation.
- *Emerging Memories Including Cross-Point, Opportunities and Challenges*, Kiran Pangal, Intel

- *Memory Reliability, Qualification and their Relation to System-Level Reliability Strategies*, Todd Marquart, Micron
- *Packaging Technology for High Bandwidth Memory*, Nick (Namseog) Kim, SK Hynix
- *Processing in Memory (PIM): Performance and Thermal Challenges and Opportunities*, Mircea Stan, UVA
- **Scaling Survival Guide in the More-than-Moore Era**, organized by Jin Cai, TSMC
 - *Extreme-UV Lithography—Principles, Present Status and Outlook*, Tony Yen, ASML
 - *MOSFET Scaling Knobs (GAA, NCFET...) and Future Alternatives*, Witek Maszara, Globalfoundries
 - *Overcoming Variation Challenges*, Sivakumar Mudanai, Intel
 - *Embedded Memory: Present Status and Emerging Architecture and Technology for Future Applications*, Eric Wang, TSMC
 - *3D Integration for Density and Functionality*, Julien Ryckaert, Imec
 - *Advanced Packaging: the Next Frontier for Moore's "Law,"* Subramanian Iyer, UCLA

Plenary Presentations—Monday, Dec. 3

- *Future Computing Hardware for AI*, Jeffrey Welser, Vice President, IBM Research-Almaden
- *"4th Industrial Revolution and Foundry: Challenges and Opportunities,"* Eun Seung Jung, President of Foundry Business, Samsung Electronics

- *"Venturing Electronics into Unknown Grounds,"* Prof. Gerhard P. Fettwies, TU Dresden

Evening Panel Session—Tuesday Evening, Dec. 4

- *EUV: Too Little, Too Late, Too Expensive or the Ultimate Cure-All?*, organized by Sanjay Natarajan, Senior VP of Applied Materials. Much progress has been made in EUV patterning technology, and yet manufacturing throughput, masks, pellicles and resists still persist as problems today. The complexity of reliably transferring features at the 7 nm node and below using quadruple patterning and 193 nm immersion is affecting yield, affecting the cost-per-gate reduction and slowing down Moore's Law. The industry eagerly awaits EUV, but is it too little, too late and too expensive, or is it the ultimate panacea? A team of world-renowned experts from the leading logic and memory IDMs, foundries and fabless companies will vigorously debate the issue.

Luncheon—Tuesday, Dec. 4

IEDM will have a new career-focused luncheon event this year that features industry leaders talking about their personal experiences in the context of career growth. The speakers will be:

- Veena Misra, Distinguished Professor and Director of the ASSIST Center at NC State University
- John Chen, Vice President of Technology and Foundry Management at Nvidia

Vendor Exhibition/Poster Sessions

- A vendor exhibition will be held once again, with special exhibit events in the evenings.

- This year two poster sessions will be held, one on MRAM technology organized by the IEEE Magnetics Society, the other a student research showcase hosted by the Semiconductor Research Corporation.

Further Information About IEDM

For registration and other information, visit www.ieee-iedm.org.

Follow IEDM via Social Media

- Twitter: www.ieee-iedm.org/twitter
- LinkedIn: www.ieee-iedm.org/linkedin
- Facebook: www.ieee-iedm.org/facebook

About IEEE & EDS

IEEE is the world's largest technical professional organization dedicated to advancing technology for the benefit of humanity. Through its highly cited publications, conferences, technology standards, and professional and educational activities, IEEE is the trusted voice in a wide variety of areas ranging from aerospace systems, computers, and telecommunications to biomedical engineering, electric power, and consumer electronics. Learn more at <http://www.ieee.org>.

The IEEE Electron Devices Society is dedicated to promoting excellence in the field of electron devices for the benefit of humanity, and sponsors the IEDM. Learn more at <https://eds.ieee.org/>.

Gary Dagastine
Dagastine & Co.

Chris Burke
BtB Marketing Communications

IEEE INTERNATIONAL RELIABILITY PHYSICS SYMPOSIUM (IRPS)

The IEEE International Reliability Physics Symposium (IRPS) is the world's premier forum for leading-edge research addressing developments in the Reliability Physics of devices, materials, circuits, and products used in the electronics industry. IRPS is the conference where **emerging reliability physics challenges and practical solutions** to achieve realistic **end-of-life projections** are first discussed.

This year, the IRPS will be held **March 31st–April 4th at the Hyatt Regency, Monterey, California**. The IRPS begins with two full days of tutorials and a year-in-review on Sunday, March 31st and Monday, April 1st followed by three days (Tuesday–Thursday, April 2nd–4th) of plenary and parallel technical sessions presenting original, state-of-the-art work. **Abstracts are due October 26, 2018**. Late paper submission due January 25, 2019.

The IRPS draws presentations and attendees from industry, academia and governmental agencies worldwide. No other meeting presents as much leading work in so many different areas of reliability of electronic devices, encompassing silicon device, non-silicon device, process technology, nanotechnology, optoelectronics, photovoltaic, MEMS technology, circuits and systems reliability including packaging. This year, the IRPS is **soliciting increased participation** in the following areas: **Modeling of Circuit Reliability and Aging, Beyond CMOS—Reliability Issues in Neuromorphic Computing, Reliability Challenges in Automotive Electronics, and Advanced Packaging (2.5/3D)**.

The IRPS is heading back to Monterey this year which is a scenic and historic coastal California destination. Just two hours by car from San Francisco or a five-hour drive from Los Angeles, Monterey is a place to **EXPLORE** and **ENJOY!** From the Monterey Bay National Marine Sanctuary to Span-



SEE MONTEREY

ish-era adobes and John Steinbeck's Cannery Row, Monterey welcomes visitors from around the world.

Opportunities at the symposium include:

- **Two-Day Tutorial Program** (Sunday—Monday, March 31st–April 1st). The IRPS tutorial program is a comprehensive two-day event designed to help both the new engineer and experienced researcher. The program contains both beginner and expert tracks and is broken down into topic areas that allow the attendee to participate in tutorials relevant to their work with minimal conflicts between subject areas.
- **Year-in-Review Session** (Monday, April 1st). These seminars provide a summary of the most significant developments in the reliability community over the past year. This serves as a convenient, single-source of information for attendees to keep current with the recent reliability literature. Industry experts serve as the “tour guide” and save you time by collecting and summarizing this information to bring you up to date in a particular area as efficiently as possible.
- **Evening Poster Reception**. The poster session provides an additional opportunity for authors to present their original research. The setting is informal and allows for easy discussion between authors and other attendees.

- **Evening Session Workshops.**

These workshops enhance the symposium by providing the attendees an opportunity to meet in informal groups to discuss key reliability physics topics with the guidance of experienced moderators. Some of the workshop topics are directly coupled to the technical program to provide a venue for more discussion on the topic.

- **Vendor Exhibits**. Held in parallel with the technical sessions, the equipment demonstrations provide a forum for manufacturers of state-of-the-art laboratory equipment to present their products. Attendees are encouraged to visit the manufacturers' booths for information and demonstrations.
- **IRPS Paper Awards**. IRPS bestows awards for Best Paper, Outstanding Paper, Best Poster and Best Student Paper. The Best Paper author is typically invited to present the paper at ESREF in October.
- **IEW Co-Location**. This year the IRPS will be co-located with the International ESD Workshop. Now in its 13th year, the IEW provides a relaxed, invigorating atmosphere to present new work and engage in discussions about the latest issues confronting the ESD and EOS communities.

For registration and other information, visit the IRPS-2019 home page at www.irps.org.

The IRPS committee members look forward to seeing you in Monterey!

Mark Porter
2019 IRPS General Chair
Medtronic

Jason Ryan
2019 IRPS Publicity Chair
NIST

SOCIETY NEWS

MESSAGE FROM EDS PRESIDENT-ELECT

Dear EDS members:



Meyya Meyyappan

I am honored to serve EDS as the President-Elect in 2018–2019. We have a talented and passionate leadership in place governing the EDS and guiding the Society through challenges related to declining membership, delivering services to the broad spectrum of our membership and meeting (and even exceeding) their expectations, and maintaining the highest quality of our publications and conferences. My immediate goal is to completely support EDS President Fernando Guarin in executing his vision for the Society and assist him and the BoG in anyway I can.

In the long term, my goal is to focus on the Strategic Directions for EDS for the future. Our profession is changing rapidly. The End of Moore's Law is definitely in sight. The famed ITRS Roadmap is not going to have any more editions. Instead, SEMI, IEEE and ASME have been working to replace it with the so-called *Heterogeneous Integration Roadmap* (HIR). I am proud to say that EDS is one of the three IEEE Societies engaged in this road-mapping activity. IEEE is also engaged in another road-mapping activity called the *International Roadmap for Devices and Systems* (IRDS); again, EDS is a key contributor to this effort. Areas and challenges to be identified in such roadmaps, emerging fields such as *IoT*, flexible electronics, etc. are going to define

who we are as a Society and what our members would be doing for a living in 20 years from now. Are we prepared for these new turn of events and directions? I would like to focus on this with your help and support.

Fortunately, the EDS leadership with the help of an *ad hoc* committee has recently prepared a Strategic Direction Report. This comprehensive report presents several vital ideas in every aspect of EDS governance. I will work with the BoG and the leadership to implement the recommendations so that we will flourish as a Society in the coming decades. This will be my primary goal. For the rest, stay tuned.

Meyya Meyyappan
EDS President-Elect
2018–2019

REPORT ON THE BOARD OF GOVERNORS MEETING IN CARTAGENA, COLOMBIA, ON JUNE 3, 2018



Jacobus W. Swart
EDS Secretary

The BOG meeting was held in Cartagena de Indias, Colombia, following the ExCom meeting on the day before. The meeting proceeded after establishing that the quorum defined by C&B was satisfied. The picture taken at the end of the BOG meeting shows most of the participants. After the welcome words by the president, the full agenda was covered, the scheduled reports were



Attendees of the EDS Board of Governors Meeting in Cartagena, Colombia

presented and motions discussed and approved.

EDS President, Fernando Guarin highlighted the society's accomplishments, such as the high Impact Factor achieved by J-EDS, the gradual shortening of time from submission to publish papers in EDS journals, the success of the new flagship conference in Asia, EDTM, beside the progress on the working document of strategy plan for EDS.

A total of 14 reports were presented and discussed, including reports by the treasurer, technical committees and meetings, regions

and chapters, publications and products, ExCom meeting, region 9 chapters meeting (held the previous day in the same location), education activities, EDS awards, newsletter update and Fellow Evaluation update, beside others.

A total of 18 motions were approved at the meeting. A few new appointments for different committees were approved. Some articles in the C&B and also charters of committees were adjusted to comply with motions approved in previous BoG meetings. A revival plan for the Distinguished Lecturer program

was approved. The membership dues were approved to remain flat at \$18.00. A best paper award of J-EDS was proposed and approved. After the Young Professional report presentation a budget of \$9,000 was approved for initial development of a new social media tool in 2018. The next mid-year BoG meeting was approved to occur in Tarragona, Spain, on May 25–26, 2019.

Jacobus W. Swart
EDS Secretary
FEEC/UNICAMP
Brazil

MESSAGE FROM EDITOR-IN-CHIEF

Dear Readers,



Carmen M. Lilley
Editor-in-Chief

In this issue, I think you will find interesting news and articles of EDS member activities and events in the past few months from around the world as well as announcements

of upcoming EDS sponsored conferences. In addition, we continue the series of "Marvels of Microelectronics Engineering," which was well received from by our readers and has generated enthusiastic feedback. In this message, I would like to include a letter from Dr. Lewis Terman, who submitted the following Letter-to-the-Editor.

Dear Carmen,
I just received the EDS Newsletter, which was extremely well done. Thanks for a great job, as usual.

However, I would like to call your attention to an error in the "Marvels of Microelectronic Engineering" article. On Page 3, at the bottom of the left hand column, the text states "... However, right after Bob Noyce at Fairchild proposed the planar wafer integration process in 1959..." Actually, it was Jean Hoerni, also at Fairchild, who invented the silicon planar process (Crystal Fire, Riordan and Hodgeson, page 262; also see the following links—two of numerous on-line references).

https://en.wikipedia.org/wiki/Planar_process

<http://www.computerhistory.org/siliconengine/invention-of-the-planar-manufacturing-process/>

Sincerely,
Lewis Terman
IEEE SSIT Secretary
2008 IEEE President
2013–2014 IEEE Awards Board
Chair

To this feedback, Simon Deleonibus and Joachim Burghartz state:

In our July 15, 2018 **article**, we reported on Page 3, line 49 of the left hand column, the following text: "... However, right after Bob Noyce at Fairchild proposed the planar wafer integration process in 1959..." We thank Dr. Lewis Terman for pointing out this unprecise assertion.

In our mind, Noyce's invention was the one that bears the highest resemblance with today's integrated circuits by adding to Kilby's and Hoerni's ideas the practical solution of integrated interconnect.

We look forward to hearing from other readers in the future. If you have any feedback or suggestions for the newsletter, please send them to me at clilley@uic.edu

Sincerely,
Carmen

2017 EDS PAUL RAPPAPORT AWARD

A high priority of the Electron Devices Society (EDS) is to recognize and enhance the quality of papers published in EDS archival literature. Every year, the Society confers its prestigious Paul Rappaport Award to the best paper published in the *IEEE Transactions on Electron Devices*. Among other criteria including technical excellence, an important metric for selection for the award is comprehensive and impartial referencing of prior art.

The winning paper was selected from over 760 articles that were published in 2017. The winning paper is entitled *"Strained Germanium Gate-All-Around pMOS Device Demonstration Using Selective Wire Release Etch Prior to Replacement Metal Gate Deposition"*. This paper was published in the November 2017 issue of the *IEEE Transactions on Electron Devices*, and was authored by L. Witters, H. Arimura, F. Sebaai, A. Hikavy, A. P. Milenin, R. Loo, A. De Keersgieter, G. Eneman, T. Schram, K. Wostyn, K. Devriendt, A. Schulze, R. Lieten, S. Bilodeau, E. Cooper, P. Storck, E. Chiu, C. Vrancken, P. Favia, E. Vancoille, J. Mitard, R. Langer, A. Opdebeeck, F. Holsteyns, N. Waldron, K. Barla, V. De Heyn, D. Mocuta, and N. Collaert.

The award will be presented at the plenary session of the International Electron Devices Meeting to be held on December 3, 2018, in San Francisco, CA. In addition to the award certificate, the authors will receive a check for \$2,500 to be shared equally among all authors. On behalf of the Electron Devices Society, I would like to congratulate the authors for this achievement. Brief biographies of some of the authors follow.

Liesbeth Witters is a principal engineer working on the integration of high mobility channel materials. Prior to joining imec in 2001, she worked as a CMOS technology development engineer in



Conexant, California. She holds degrees in chemical engineering from Katholieke Universiteit Leuven, Belgium and ENSPM, France.



Hiroaki Arimura received M.Sc. and Ph.D. degrees from Osaka University in 2009 and 2011, respectively. In 2011, he joined the reliability

group of imec as a postdoc of KU Leuven. Since 2013, he has been a researcher in logic technologies department of imec and working on Ge channel technologies.



Farid Sebaai received the M.Sc. degree in 2004 in materials science from the University of Strasbourg, France and he is a process engineer

specialized in CMP and wet/cleaning for 14 years. At imec, he is responsible for developing the necessary wet and cleaning steps in FEOL for advanced integration schemes for more than 10 years.



Hikavy Andriy received the M.Sc. degree in Physical Electronics from Chernivtsi State University, Ukraine in 1998 and Ph.D. in applied

electronics from Ghent University, Belgium in 2003. Between 2003 and 2006 he worked as a researcher at the Department of Solid State Physics of the same university. In 2006 he joined Epitaxy group of imec where

he currently works on selective epitaxial growth of Si and SiGe.



Alexey Milenin received his Ph.D. on Physics of sub-monolayer microstructures at IACP, Russia, 2000. In 2002, he started PostDoc at MPI of

Microstructure Physics, Germany. In 2007, he joined imec, Belgium. Starting in the BEOL, he is currently working as a researcher on advanced etch processes in the FEOL team.



Roger Loo received his M.Sc. degree in experimental physics in 1993 and his Ph.D. degree in 1997, both from the R.W.T.H. Aachen,

Germany. In January 1997, he joined imec in Leuven, Belgium. At imec, he is the leading principal scientist for Group IV epi activities.



An De Keersgieter received the M.Sc. degree in physics from the University of Gent, Belgium, in 1984. She joined imec in 1985, working

on process modeling. At present she is mainly focusing on process and device simulation and calibration of N14 and smaller CMOS technologies. Among fields of interest are strain-engineering and multi-gate devices. Next to this she is responsible for support of TCAD tools used at imec.

Geert Eneman received the B.Sc., M.Sc. and Ph.D. degrees in electrical engineering from the Catholic University of Leuven, Belgium, in 1999, 2002, and 2006. He is currently



working at imec. His current research interests include modeling of alternative device architectures, strain effects and leakage and layout effects in advanced MOSFETs.



Tom Schram received his Ph.D. in chemical engineering in 1999 from the Free University of Brussels. He has been working at imec since 2001 as an integration engineer. His focus topics have been or are: high-k & metal gate, DRAM PERI, Si and (Si)Ge devices and 2D materials.



Kurt Wostyn received his Ph.D. degree in Chemistry from Katholieke Universiteit Leuven, Belgium in 2003. After a postdoctoral research position at the University of Cambridge (UK), he joined imec in 2004 where he is working on wet etch and clean processes for Group IV semiconductor materials.



Katia Devriendt is a senior R&D engineer in the Electrodeposition, CMP and Thinning group of the UPM division at imec, a position she has held since 1997 after receiving her M.Sc. and Ph.D. degree in Chemistry at the University of Leuven. Currently she is involved in the FEOL CMP process steps development of the 7nm technology node and below.

Andreas Schulze serves as a metrology and materials characterization



consultant supporting imec's process and integration teams. Dr. Schulze holds a Ph.D. degree in Physics from KU Leuven (Belgium, 2013) and a M.Sc. degree in Electrical Engineering from Technical University of Dresden (Germany, 2008).



Ruben Lieten is Senior Technologist at Entegris Inc. He has expertise in semiconductor process technology and devices, including epitaxial growth of group IV and III-V semiconductors, chemical mechanical polishing, optical characterization of semiconductor materials and MOSFET processing. He holds a Ph.D. in Electronic engineering, and MBA degree from Vlerick Belgium.



Steven Bilodeau is a Principal Scientist at Entegris Inc. He has developed process technology for fabrication of optical and electronic devices. Areas of interest include CVD and ALD and surface preparation technologies. He holds a Ph.D. in Materials Science from Rensselaer Polytechnic Institute.



Emanuel Cooper is Principal Scientist at Entegris Inc. He has worked in various chemistry and materials science areas—molten salts and ionic liquids, ceramics, electroplating, etc., focusing since 2005 on selective film etching and cleaning for microelectronics. He holds a D. Sc. in chemistry from the Technion (Haifa, Israel).



Peter Storck holds a Ph.D. in Physical Chemistry from TU Darmstadt, Germany, and has worked for Siltronic AG in Portland, Oregon, and Burghausen, Germany, since 1996. Since 2004, he is the manager of Siltronic's Innovation Projects group developing engineered substrates. His research topics include Si, SiGe, rare-earth oxide and III-N epitaxy.



Eddie Chiu is Head of Process Engineering and Key Account Technology at HPSP, he is responsible for process R&D, applications and key accounts. He holds various publications and patents in semiconductor and optoelectronics technology. Eddie received his education in Electrical Engineering and Computer Sciences at the University of California, Berkeley.



Paola Favia received the Ph.D. degree in solid state physics from the Ecole Polytechnique Federale de Lausanne—Switzerland. From 1997 to 2004 she was R&D researcher at Gatan Inc., California. Since 2006 she is a researcher at imec, Belgium focusing on strain and chemical analysis of semiconductors by TEM.



Eric Vancoille leads the Transmission Electron Microscopy at imec Materials and Components Analysis Department since 2014, having worked previously in Thin Films and Epitaxy process groups. Prior to 2008 he was transceiver designer with

Broadcom Ltd and Optoelectronics Researcher AStar in Singapore since 1997. He holds a Ph.D. in Materials Science from University of Leuven.



Jérôme Mitard

After a Ph.D. in microelectronics performed at LETI/Grenoble together with STMicroelectronics/Grenoble/France, Jérôme

Mitard joined imec/Leuven/Belgium, in 2007 as a device researcher working on high-mobility channel MOSFETs. He is currently team leader of the 300 mm Platform Device Research team.



Robert Langer is heading imec's Epitaxy research group which develops SiGe, III-V and GaN based devices and novel integration ap-

proaches. Prior to that, he was responsible for growth processes and engineered substrates at Picogiga and later Soitec for RF applications. He received a Dipl.-Phys. degree from University Karlsruhe in 1996 and a Ph.D. degree from UJF Grenoble in 2000.

Ann Opdebeeck received a B.Sc. in Chemistry in 1991 in Rega School Leuven. She joined imec the first



time in 1991 as process assistant in the Ultra Clean Processing group. In 2006 she joined imec a 2nd time as development engineer in the logic technologies department supporting different process technologies and ensuring process stability.



Niamh Waldron graduated with the Ph.D. degree from the Massachusetts Institute of Technology in 2007. She has been with imec,

Belgium since 2008 and her research has focused on the integration of varied III-V devices on Si substrates for logic and high speed RF applications.



Kathy Barla joins imec in October 2012 as Unit Process & Modules Department Director. Kathy had 30 years of experience in micro-

electronics working for France Telecom Microelectronics Research Center (CNET) and ST Microelectronics at Crolles including 3 years at the International Semiconductor Development Alliance, IBM East Fish-

kill, to develop & transfer the 28 nm technology.



Vincent De Heyn is an Operations Program Manager at imec Logic Technology department. He received his M.Sc. in electrical engineering

in 1998 from University Libre de Bruxelles. He has 20 years research experience in various semiconductor domains such as Reliability, AnalogRF circuit design and CMOS process technologies. He has authored and co-authored more than 35 publications.



Nadine Collaert has been involved in the research of FinFET, emerging memories and transducers for biomedical applications. From 2012

to 2016, she was program manager of the LOGIC program. Currently she is distinguished member of technical staff, responsible for heterogeneous integration of new materials with Si and material-enabled approaches to increase system functionality.

Hisayo S. Momose
EDS Vice-President of Publications
and Products
h.s.momose@ieee.org

LATIN-AMERICAN EDS CHAPTERS MEETING IN CARTAGENA, COLOMBIA

EDS is consolidating in Region 9 and is one of the main conclusions of the EDS chapters meeting in region 9, which took place on June 1 and 2 in the city of Cartagena, Colombia at the facilities of the Technological University of Bolívar. The meeting was attended by 30 dele-

gates from 22 chapters and 6 countries, including Brazil, Mexico, Nicaragua, Colombia, Peru and Venezuela. At the meeting, aspects of good practices in the management and governance of the chapters were presented, a review was made of the current status of the

different chapters of the region and strategies were discussed to address the various challenges facing the chapters of the region. The meeting was chaired by Arturo Escobosa, Chair of Region 9 and M.K. Radhakrishnan Vice President of Regions & Chapters.



Attendees and Distinguished Lectures at the Latin American EDS Chapters Meeting

Complementary to the meeting, two mini-colloquia of EDS were held. In the city of Bogotá, a mini-colloquium was held at the Javeriana University and the District University where DL Adelmo Ortiz Conde, Cor Clays, Fernando Guarín, Jacobus Stewart, and Edmundo Gutierrez participated. Another mini-colloquium was held in Cartagena de Indias on June 1st, where the following Distinguished Lecturers participated, Mukta Farooq, Meyya Meyyappan, Adelmo Ortiz, M.K. Radhakrishna and Fernando Guarín.

2017 EDS GEORGE E. SMITH AWARD

A high priority of the Electron Devices Society (EDS) is to recognize and enhance the quality of papers published in EDS archival literature. The George E. Smith Award was established in 2002, to recognize the best paper appearing in a fast turnaround archival publication of EDS, targeted to the *IEEE Electron Device Letters*. Among other criteria including technical excellence, an important metric for selection for the award is comprehensive and impartial referencing of prior art.

The paper winning the 2017 George E. Smith Award was selected from over 400 articles that were published in 2017. The paper is entitled, "Negative Capacitance as Performance Booster for Tunnel FETs and MOSFETs: An Experimental Study". This paper appeared in the October 2017 issue of the *IEEE Electron Device Letters* and authored by Ali Saeidi, Farzan Jazaeri, Francesco Bellando, Igor Stolichnov, Gia V. Luong, Qing-Tai Zhao, Siegfried Mantl, Christian C. Enz, and Adrian M. Ionescu.

The award will be presented at the plenary session of the IEEE International Electron Devices Meeting to be held on December 3, 2018 in

San Francisco, California. In addition to the award certificate, the authors will receive a check for \$2,500, to be shared equally among all authors. On behalf of the Electron Devices Society, I would like to congratulate the authors for this achievement. Brief biographies of the authors follow.



Ali Saeidi received the B.S./M.S. degree in electronic engineering from the University of Tehran, Tehran, Iran. In 2014, he joined the Laboratory of Micro/Nanoelectronic Devices, École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland, as a PhD student. His current research focuses on exploration of negative capacitance ferroelectric device concepts and technologies.

Farzan Jazaeri received the PhD degree from EPFL in 2015. Currently, he is a Research Scientist and a Project Leader at ICLAB, EPFL. His research interests include solid-state physics for operation within extreme harsh environments, i.e.



high-energy particle background and cryogenic temperatures for space applications and quantum computations.



Francesco Bellando was born in Torino, Italy, in 1989. He received his Master in Nanotechnologies for the I.C.T.s in 2015 from the Politecnico di Torino and in the same year he started working for his PhD at EPFL, Switzerland, in the field of Nanotechnologies for diagnostic applications.



Igor Stolichnov, PhD, Swiss Federal Institute of Technology (EPFL), 2000. Currently senior scientist at EPFL, member of the Nanoelectronic devices laboratory (NANOLAB). His scientific interests focus on functional

materials and their applications for information processing and storage, including ferroelectrics, dielectrics and multiferroics.



Gia Vinh Luong received the Dipl. Ing. degree from Technical University Dortmund, Germany, in 2012, and the PhD degree in electrical engineering from the Forschungszentrum Jülich, Germany, in 2018. His research focuses on fabrication of Si nanowire energy efficient tunneling field effect transistors and digital circuits.



Qing-Tai Zhao received PhD in 1993 from Peking University, and then started his career at Peking University as lecturer and associ-

ate professor. In 1997, he joined PGI-9, Forschungszentrum Jülich, where he is currently a senior research scientist and the leader of Group IV Electronic Device Group.



Siegfried Mantl is head of the ion beam division of the Peter Gruenberg Institute 9, professor of physics at the RWTH Aachen and holds an honorary Helmholtz professorship. His research concentrates on silicon related nanoelectronic materials and devices.



ChristianENZ, PhD, Swiss Federal Institute of Technology (EPFL), 1989. Currently Professor at EPFL, Director of the Institute of Micro-

engineering and head of the IC Lab. Until April 2013, VP at the Swiss Center for Electronics and Microtechnology (CSEM), Switzerland. Until 1999, Principal Senior Engineer at Conexant, Newport Beach, California.



Adrian M. Ionescu is a Professor at Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland. His group pioneered novel concepts for beyond CMOS devices. He received the IBM Faculty Award 2013 and the André Blondel Medal 2009. He is an IEEE Fellow and member of the Swiss Academy of Engineering Sciences.

Hisayo S. Momose
EDS Vice-President of Publications
and Products
h.s.momose@ieee.org



2019 IEEE EDS WILLIAM R. CHERRY AWARD CALL FOR NOMINATIONS



The IEEE Electron Devices Society invites the submission of nominations for the 2019 William R. Cherry Award.

This award is named in honor of William R. Cherry, a founder of the photovoltaic community. In the 1950's, he was instrumental in establishing solar cells as the ideal power source for space satellites and for recognizing, advocating, and nurturing the use of photovoltaic systems for terrestrial applications. The William R. Cherry award was instituted in 1980, shortly after his death. The purpose of the award is to recognize an individual engineer or scientist who devoted a part of their professional life to the advance-

ment of the science and technology of photovoltaic energy conversion.

The award consists of a plaque, monetary award, recognition and a dedicated Cherry Award Talk during the Opening Session of the IEEE Photovoltaic Specialists Conference (PVSC). In addition, a reception is held in honor of the Cherry Award winner during the PVSC.

Nominate: Information on the PVSC conference website: <https://www.ieee-pvsc.org/PVSC46/awards-cherry.php>

William R. Cherry Award on-line nomination form: <https://ieeeforms.wufoo.com/forms/eds-william-r-cherry-award-nomination-form/>

Submission Deadline: January 14, 2019



ELECTRON DEVICES SOCIETY MEMBERS NAMED RECIPIENTS OF 2018 IEEE MEDALS



Two EDS members were named 2018 IEEE Medal award winners. Please be sure to visit IEEE TV at <http://ieeetv.ieee.org/> to view the award presentations and acceptance speeches.

2018 IEEE Edison Medal

Sponsored by Samsung Electronics Co., Ltd.



Eli Yablonovitch

For leadership, innovations, and entrepreneurial achievements in photonics, semiconductor lasers, antennas, and solar-cells

The technologies developed by Eli Yablonovitch affect anyone who uses a mobile phone or searches the Internet. Yablonovitch proposed that semiconductor lasers should be strained, in order to benefit from reduced valence band (hole) effective mass. Today, with almost every human interaction with the Internet, optical telecommunication occurs by strained semiconductor lasers. Most likely, billions of people are unknowingly using his idea every time they connect to the Internet, make a phone call, or check e-mail. In his photovoltaic research, Yablonovitch's 4n2 light-trapping factor is in worldwide use for almost all commercial solar panels. Known as the Yablonovitch Limit, this factor increased the theoretical limits and practical efficiency of solar cells. To the extent that solar electricity is blended with other power sources, there are billions of people unknowingly taking advantage of the Yablonovitch Limit. In his photonics work, Yablonovitch unified Maxwell's Equations and Schrodinger's Equation through the concept of the photonic crystal. The geometrical structure of the first experimentally



realized photonic bandgap is often called Yablonovite. His invention of photonic crystals unifies optics, solid-state physics, electromagnetics, and quantum optics. Among other applications, photonic crystals are used in telecommunications, particularly in polarization splitting, two-dimensional, grating couplers—which are a critical part of silicon photonic integrated circuits. His original paper on photonic crystals has been cited over 10,000 times and is the second-most-cited paper in the history of Physical Review Letters. Yablonovitch has co-founded four science-based companies, including Ethertronics, which became a major independent cell-phone antenna manufacturer, having shipped over 2 billion antennas.

An IEEE Fellow and member of both the U.S. National Academy of Engineering and National Academy of Sciences, Yablonovitch holds the James and Katherine Lau Chair in Engineering and is a professor with the Electrical Engineering and Computer Sciences Department at the University of California, Berkeley, CA, USA.

2018 IEEE Jun-ichi Nishizawa Medal

Sponsored by the Federation of Electric Power Companies, Japan



Joe C. Campbell

For contributions to the development of high-speed, low-noise, long-wavelength avalanche photodiodes

A leading innovator in the field of photonics, Joe C. Campbell's development and advancement of avalanche photodiodes (APDs) have raised the sensitivity of optical receivers to a new level to increase the amount of information that can be transmitted in high-bandwidth fiber-optic networks. Optoelectronic devices play an integral role in communication systems with lasers and photodetectors acting as information sources and receivers, and the APD has become the standard for long-haul, high-bitrate systems. APDs are also widely used in laser range finders, in biomedical imaging applications such as positron emission tomography, and in particle physics experiments. Beginning with his work at Bell Labs in the 1980s and continuing through his academic career at the University of Texas at Austin and the University of Virginia, Campbell has carried out groundbreaking work that has enabled the realization and

advancement of high-performance APD-based fiber-optic receivers crucial to long-distance telecommunications links. Campbell was responsible for the initial design, fabrication, and experimental characterization of the APD, and he demonstrated the order-of-magnitude improvement in system performance that APDs enabled. He also demonstrated the critical importance of separate avalanche and detection (SAM), as well as the importance of charge (SACM) and grading (SAGM) layers in this design. He

showed the importance of nonlocal effects and how APD receivers can be made superior to existing theories as a result of this effect in superlattice APDs. Campbell was the first to show that the multiplication noise of these high-speed APDs did not degrade for very thin multiplication regions. Campbell also modeled the noise and frequency response of the SAM-APD. His analytic treatment of the frequency response includes all the physical mechanisms that affect the speed. This model is widely ac-

cepted as the most accurate method to simulate the frequency response of the technologically important APD.

An IEEE Life Fellow and member of the U.S. National Academy of Engineering, Campbell is the Lucian Carr Professor of Electrical and Computer Engineering at the University of Virginia, Charlottesville, VA, USA.

*Samar Saha
EDS Awards Chair
Prosperious Devices
Milpitas, CA, USA*

EDS MEMBERS RECENTLY ELECTED TO IEEE SENIOR MEMBER GRADE

Ghulam Abbas
Asrulnizam Abd Manaf
Francois Andrieu
Douglas Barlage
Charles Baudot
Paul Bergstrom
David Brown
Christopher Chang
Stefan Cosemans
Cory Cress
Maria De Souza
Nima Dehdashti Akhavan
Mohammed Fakhruddin
Samuel Graham
Sen Huang

Seth Martin Hubbard
Makoto Ikeda
Ali Javey
Harsupreet Kaur
Pedram Khalili Amiri
Darsen Lu
Xiaorong Luo
Kausik Majumdar
Raja Mir
John Moses
Yasir Naif
Byung-Gook Park
Bejoy Pushpakaran
K. Radhakrishnan
Munaf Rahimo

Nancy Saldanha
Jay Sarkar
Anmol Saxena
Amretashis Sengupta
Uttam Singiseti
Florian Solzbacher
Haiding Sun
Pramod Tiwari
Richard Toftness
Ikechi Ukaegbu
Wilfried Van Sark
Tri-Rung Yew
Huaxiang Yin
Bo Zhang

If you have been in professional practice for 10 years, you may be eligible for Senior Membership, the highest grade of membership for which an individual can apply. New senior members receive a wood and bronze plaque and a credit certificate for up to US \$25 for a new IEEE society membership. Upon request, a letter can be sent to employers, recognizing this new status. For more in-

formation on senior member status, visit: http://www.ieee.org/membership_services/membership/senior/index.html

To apply for senior member status, fill out the online application after signing in with your IEEE account: https://www.ieee.org/membership_services/membership/senior/application/index.html.

YOUNG PROFESSIONALS

INNOVATING THE WAY OF TRAINING FUTURE ENGINEERS

Over the years, IEEE has held an important role that has transformed our way of life in a silent but powerful manner. Many of the inventions that seem daily and normal, have arisen from minds that have bet on the development of new technologies.

This process of vertiginous evolution has led us to see not only the advance of technology as a tool for human evolution, but also as an opportunity to make this a better world. Hence, programs such as E4C (Engineers for Change), SIGHT, EPICS, among others, are now the channels for the promotion of ideas for change. One of the success stories of this new trend is the outreach program based on SNAP CIRCUITS, a program that has been implemented worldwide now for several years, thanks to the initiative, financial support and motivation of EDS worldwide, it has enabled many communities around the world, to learn about basic electronic circuits.

In December 2017, within the framework of the 9th CHRISTMAS FEEELIZ program, and thanks to the participation of EDS Colombia volunteers, the idea of integrating efforts between SIGHT Colombia and EDS worldwide was conceived, with the purpose of maximizing the impact to the communities. During early 2018, work began on a program that will not only allow the expansion and growth of the SNAP CIRCUITS program, but also make these activities the point of contact with the community, thus allowing interest to be incubated; engineering on the one hand, and on the other, the possibility of identifying needs that can be met through technology with the support and involvement of the community.

This is how, after several work sessions, the SNAPWORLD program was

born, as a response to an identified need, allowing not only for the communities to benefit from the teams within the communities, but also for the student branches to be trained with soft skills, these improvements directly led to the realization of better and more productive workshops.

The structure has two introductory modules, lasting 4 hours each, using the SC-100 basic module. These modules will familiarize attendees with the platform, its capabilities that include the different circuits and possibilities that this tool could offer. Additionally, the session was designed so the instructors were taught about how to get the students interested, within minutes



DA EL PRIMER PASO PARA TRANSFORMAR EL MUNDO.
Convértete en todo un experto del Snap World y comienza a construir con tu comunidad un mundo mejor.

INSCRIPCIONES ABIERTAS - CUPOS LIMITADOS

Important Dates:
MARZO 24 - Lanzamiento convocatoria
ABRIL 14 - Snap Circuit Nivel básico
ABRIL 21 - Snapino World

Una alianza por un mejor país entre:



they were developing the activities with the team. We encourage an approach, so the participants find in each other the skills that allow teaching the children about basic electronic concepts. We showed the participants that, through familiar images and everyday examples or stories, they could capture the children's attention, thus leading them to understand the concepts explained.

This second module was based on the SNAPINO tool (integrated Arduino®), which, being a bit more complex, required a greater commitment on the part of the participants. The reception was excellent, and in addition to working with the platform, a talk was offered in which it was explained how programming code should be constructed by means of the block diagram, starting from daily activities, thus allowing participants to have colloquial examples as tools for the transfer of more technical programming concepts.

Both sessions were a total success, for the pilot program, we had the support of the "Universidad Católica de Colombia" and the IEEE student branch of the University, for the development of both sessions. It also included the participation of volunteers from more Universities such as "San Buenaventura" Escuela Colombiana de Ingeniería, "Universidad Distrital", "Manuela Beltrán University", among others. Putting together a total of 13 pioneers for our pilot proposal all ready and willing to enact change.

Some challenges will be faced in the future. The challenge of offering this program in other areas as well as in other regions is latent, our work is now focused on our participants, those pioneers of our program, working within their own communities as a gateway to reach them, thus achieving, new paradigms within communities, and thus achieving the generation

of initiatives that transform and offer welfare in each of their areas.

They are small tasks that are born from the passion of us as volunteers, engineers such as Camilo Téllez or the Engineer Luis Miguel Quevedo, who despite their many professional commitments have found the time to share their passion and the knowledge they possess along with the motivation to give back what they have received in their training. Sharing particularly with the most needy, making their effort not only a call to send aid, but an opportunity to transform lives through science and technology, thus forging the next generation of providing a tangible path to realize their dreams and opening their eyes to the magical world of technology and the boundless opportunities it provides not only for their life for the benefit of society.

The leaders of the initiative:



Quevedo, Luis Miguel was born in Bogotá. He received his B.S. degrees in mechatronic engineering from the University of San

Buenaventura, Bogotá, in 2015 and the specialization degree in business and services of telecommunications from the same University, in 2016. In 2015, he founded JWG S.A.S a company implementing automation solutions in Colombia for companies including: General Motors, Andina, Quala S.A., and PEPSICO. He has led the EDSETC program since 2017. His interests include Internet of Things, STEM, factory automation, nanoparticles, and innovation on sensorless control. He is a member of committee of student activities in the IEEE Colombia Section. Mr. Quevedo was a recipient of the Industry Applications Society Award outstanding student branch chapter in 2013.



Camilo E. Téllez. Camilo studied electronic engineering at Universidad de San Buenaventura (Bogotá), since 2004 to 2009. He

started master studies in Nanoelectronics systems at Technische Universität Dresden in Germany. His work is focused in the institute of materials science, TU Dresden, Germany, in themes related to print techniques, like alternative methods, for develop sensors. Between 2016–2017, he has been advisor and professor of Escuela Tecnológica Instituto Técnico Central la Salle and Universidad Católica de Colombia, where he is recently professor.



Oscar J. Rodríguez Electronic engineer of Universidad de San Buenaventura, in Bogotá Colombia, with Master on Business Admin-

istration MBA of Universidad Sergio Arboleda. Oscar has been IEEE volunteer since 2007, during this time he was student branch chair of Universidad de San Buenaventura, Co-chair of the Student Master Thesis Contest of Industry Applications Society. Vice Chair of the professional Chapter in Colombia. Since 2013, he founded and lead the SIGHT Colombian team, to 2017. He was a part of the Steering Committee for SIGHT like operations chair. In Colombia, he is a Professor at Universidad de San Buenaventura with emphasis in social impact initiatives, is consultant for small and mediums entrepreneurship about business strategy, and is working in SIGHT Colombia as New Initiatives Coordinator.

YOUNG PROFESSIONALS SAY “ALOHA” AT MENTORING EVENT IN HAWAII

By ABIRA SENGUPTA

Young Professional (YP) and student members of the IEEE Solid-State Circuits Society (SSCS) and the IEEE Electron Devices Society (EDS) had the opportunity to mingle with luminaries in the fields of solid-state circuits and electron devices at a mentoring event in Hawaii.

YP's and students enjoyed food, drink, and friendly conversation at the “SSCS/EDS Young Professionals & Students Micro-Mentoring and Career Coaching Session” or-

ganized by SSCS YP Chair Emre Ayranci and EDS YP Chair Camilo Velez Cuervo at the 2018 IEEE VLSI Symposium on 20 June 2018 at the Hilton Hawaiian Village in Honolulu, Hawaii.

Ayranci kicked off the event with a welcome presentation about the numerous benefits of SSCS and EDS membership. SSCS and EDS Leaders and AdCom members—who acted as the mentors—went around the room and described their

journey to their careers and how being an IEEE and Society member has benefited them, helped them make valuable connections, and helped shape their careers and personal lives.

After the introductions, the YP's and mentors had the opportunity to talk one-on-one. Mentors gave mentees advice on entrepreneurship, going into academia vs. industry, work/life balance, journal authorship, and much more.



The mentors and mentees at the Mentoring Event at VLSI 2018

WOMEN IN ENGINEERING MENTORING EVENT AT VLSI 2018

By ABIRA SENGUPTA

The IEEE Solid-State Circuits Society (SSCS) and the IEEE Electron Devices Society (EDS) hosted a Women in Engineering Networking Luncheon in conjunction with the 2018 Symposium on VLSI Technology and Circuits. The networking event attracted over 20 attendees. The conversation flowed, connections were made, and delicious food was consumed at the beautiful Hilton Hawaiian Village in Honolulu, Hawaii.

The event began with opening statements from Prof. Edith Beigne,



Barbara De Salvo gave an inspiring talk at the Women in Engineering Mentoring Event at the 2018 VLSI Symposium

who organized the event. Prof. Beigne talked about the benefits of joining SSCS and EDS and the women in engineering program. She spoke about the various networking opportunities at IEEE conferences and local chapter

events where women can meet and interact with each other.

Afterwards, attendees had the opportunity to listen to an inspiring talk from Barbara De Salvo, Chief Scientist and Deputy Director of

CEA-Leti, Grenoble, France. Barbara talked about the hardships that women have had to face when it comes to navigating in the engineering industry and her own career and experiences.

STUDENT MEMBERS FROM ED TSINGHUA UNIVERSITY STUDENT BRANCH CHAPTER PRESENT AT 2018 CHINESE NATIONAL SCIENCE AND TECHNOLOGY WEEK

By YANCONG QIAO

Science and Technology Week is a large-scale mass science and technology event approved by the Chinese government in 2001. According to the approval of the State Council, the third week of May is "Science and Technology Week" each year. The Ministry of Science and Technology will organize the Organizing Committee for Science

and Technology Week with 19 departments and units such as the Central Propaganda Department, the China Association for Science and Technology, as well as organize the implementation throughout the country.

The 2018 Chinese National Science and Technology Week was held May 19–26, at the Chinese People's

Revolutionary Military Museum. Professor Tian-Ling Ren and students of the ED Tsinghua University Student Branch Chapter, gave an introduction about graphene intelligent throat to leaders and audiences for the duration of the event.

~ Ming Liu, Editor

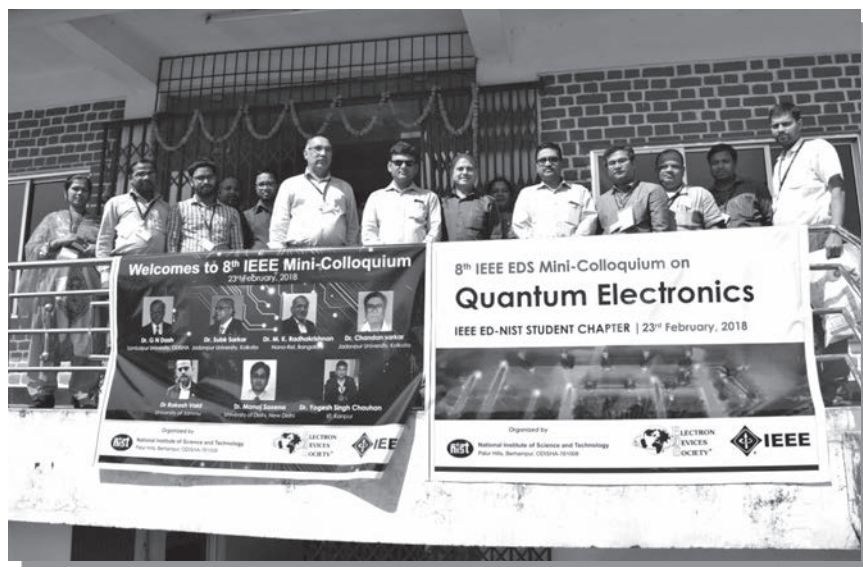


The students giving their presentations on an intelligent artificial throat

ED NIST STUDENT BRANCH CHAPTER ORGANIZES EDS MINI-COLLOQUIUM ON “QUANTUM ELECTRONICS”

By AJIT K PANDA

The ED National Institute of Science & Technology Student Chapter organized the 8th Mini-Colloquium on “*Quantum Electronics*” on February, 23, 2018 at National Institute of Science & Technology, Palur Hill, and Berhampur for the graduate and undergraduate students. More than 120 participants registered and traveled from different institutes and universities from Odisha and outside as well. Four Distinguished Lectures were held throughout the day followed by the inaugural function. Dr. Subir Kumar Sarkar, from Jadavpur University talked about MOSFET Scaling: Basic Concepts and approaches. He gave the new dimensions of research methods focusing on low threshold and parasitics and effect of EM and ESD. Dr. G N Dash pushed the concept of Graphene structure and a true alternative of MOS Device. Dr. Chandan Kumar Sarkar from Jadavpur University and Dr. Yogesh Singh



Organizers and Distinguished Lecturers at the 8th IEEE EDS MQ on Quantum Electronics

Chauhan from IIT-Kanpur talked about the compound Semiconductors and their structures. The ED NIST Student Chapter has conducted this 8th Mini-Colloquium in a series and has given opportunities

to all the students and researchers to interact with different DLs and to create new milestones in the field of electronics and semiconductors.

~ Manoj Saxena, Editor

NEW WEBINARS AVAILABLE IN THE EDS COLLECTION

EDS is many things to its members—scientific publisher, technical conference sponsor, networking resource—but at its core EDS is a community of learning. From undergraduate students and PhD candidates to tenured professors and world-renowned researchers, EDS provides device engineers from across the spectrum engaging and enriching educational opportunities.

As part of our commitment to enhancing the value of membership in EDS, we are pleased to present the EDS Webinar Archive. The online collection provides our members

with on-demand access to streaming video of past events. The following recently held webinars can be accessed here: <http://eds.ieee.org/webinar-archive.html>.

When More Moore and More than Moore Will meet for 3D—On the Way to the Energy and Variability Efficient (E.V.E.) Era
Presented by: Simon Deleonibus, IEEE Fellow

Abstract

Major power consumption reduction will drive future design of tech-

nologies and architectures that will request less greedy devices and interconnect systems. The electronic market will be able to face an exponential growth thanks to the availability and feasibility of autonomous and mobile systems necessary to societal needs. The increasing complexity of high volume fabricated systems will be possible if we aim at zero intrinsic variability, and generalize 3-dimensional integration of hybrid, heterogeneous technologies at the device, functional and system levels. Weighing on the world energy saving balance will be possible

and realistic by maximizing the energy efficiency of co integrated Low Power and High Performance Logic and Memory devices. The future of Nanoelectronics will face the major concerns of being Energy and Variability Efficient (E.V.E.).

Silicon Terahertz & sub-THz Electronics for Imaging, Sensing, Testing & Communications

Presented by: Dr. Michael Shur

Abstract

Silicon and silicon germanium transistors with feature sizes below 100 nm have demonstrated operation in sub-terahertz and terahertz frequency ranges with potential applications in communications, Beyond 5G WIFI, sensing, and imaging. New features of ballistic electron transport in deep submicron devices must be

accounted for design, modeling, and characterization of Si and SiGe transistors operating at sub-THz and THz frequencies. The key issue is the crucial role that the electron inertia and electron viscosity play at ultra-short sizes determining the frequency and decay of the plasma waves, which are the electron density oscillations in the transistor channel. This webinar will review of the state-of-the art of the Si and SiGe THz electronics and the existing and potential applications of this technology and will discuss the new device physics that is the key for developing the next generation of Si and SiGe THz devices and systems.

Hybrid Systems-in-Foil: Enabler or Flexible Electronics

Presented by: Joachim N. Burghartz

Abstract

Flexible electronics add mechanical flexibility, shape adaptivity and stretchability as well as large-area place ability to electronic systems, thus allowing for conquering fundamentally new markets in consumer and commercial applications. Hybrid assembly of large-area devices and ultra-thin silicon chips on flexible substrates is viewed as an enabler to high-performance and reliable industrial solutions as well as to high-end consumer applications of flexible electronics. This talk discusses issues in ultra-thin chip fabrication, device modeling and circuit design, as well as assembly and interconnects for thin chips embedded into foil substrates, in which flexible large-area components are implemented for an overall optimized Hybrid System-in-Foil (HySiF).

HOW TO PLAN AN EDS DISTINGUISHED LECTURE EVENT

When planning your upcoming chapter meetings, workshops, etc., please remember to visit the EDS website for a recent list of EDS Distinguished Lecturers (DLs) and lecture topics.

✓ Checklist

- Chapter contacts EDS DL to check availability, confirms date/location of lecture, discusses DL funding needs and determines chapter funding
- EDS DL completes EDS DL Activity Log and Funding Request Form
- If applicable, obtain EDS funding approval
- Chapter publicizes lecture via web, email, etc. Obtain a chapter member list via SAMIEEE (<http://www.ieee.org/about/volunteers/samieee/index>)
- If applicable, DL submits an IEEE expense report to Laura Riello to receive reimbursement
- Chapter Chair/DL Coordinator submits an EDS DL/MQ Feedback Form

If you have any questions and/or need more information, please do not hesitate to contact Laura Riello, EDS Executive Office.

Thank you for your continued support of the Society.

CHAPTER NEWS

MQs, DLs AND CONFERENCE REPORTS

2018 IEEE SILICON NANOELECTRONICS WORKSHOP (SNW)

The 2018 IEEE Silicon Nanoelectronics Workshop (SNW) is a satellite workshop of the 2018 VLSI Symposia sponsored by the IEEE Electron Devices Society. The workshop, now in its twenty-third year, showcases original work on nanometer scale devices and technologies that utilize silicon or are based on silicon substrates. This year, SNW was held at the Hilton Hawaiian Village in Honolulu, Hawaii, June 17–18. SNW 2018 included two days of technical paper presentation, prior to the 2018 VLSI Technology and Circuits Symposia. The program included 2 plenary talks, 5 invited talks, 23 oral presentations, and 73 poster papers, organized into 9 oral sessions and 2 poster sessions. Contributions of researchers from over 15 countries around the world were featured. The workshop continues to provide an excellent opportunity for engineers, professors, and students to share and discuss their recent work on nanometer-scale devices and technologies.

We were also very delighted to have two keynote speakers for the plenary session. Prof. Mark Lundstrom of Purdue University gave a talk on *“Electron and Phonon Transport from the Nanoscale to the Macroscale,”* in which he provided us insight on what we have learned from the nanoscience, and Prof. Tetsuya Asai of Hokkaido University gave a talk on *“Unconventional AI and Neuromorphic Computing driven by Emerging Devices and Materials.”* Increasingly this year, we received lots of feedback from authors who expressed interest in presenting their work on artificial intelligence (AI). AI is a cornerstone of related technologies that will lead the industry to ex-



2018 SNW: (Top left) Prof. A. Toriumi (Q&A session), (Top right) Patrick Fay and Steve Chung
The poster session (bottom)

plore more applications via innovative, more in-depth, and comprehensive work with emphasis on hardware-development based on advanced semiconductor technologies.

The symposium also featured five invited speakers in current interest topics:

- Analog Memory-based Hardware Accelerators for Deep Learning (Dr. Stefano Ambrogio, IBM Research—Almaden Lab),
- Challenges and Opportunities for Accelerating Computationally Intensive Deep Learning Using Emerging Memory Technologies (Prof. Alex T. H. Hou, NCTU),
- 3D-monolithic Integration for Enhanced-functionality CMOS (Dr. François ANDRIEU, CEA-Leti),
- Technology Breakthrough by Ferroelectric HfO_2 for Low Power Logic and Memory Applications



2018 SNW: (left) the auditorium (right) Prof. Mark Lundstrom (top); Prof. T. Asai (bottom)

(Prof. Masaharu Kobayashi, University of Tokyo), and

- Prospects for High Performance RF Interconnects and Functional Integration Using GaN on Silicon (Prof. Patrick Fay, Univ. Notre Dame)

In the poster session, authors were asked to present their work in a one-minute oral format, along with the display of their work for two hours of discussion time. Overall, the workshop was very successful with extensive discussion among our attendees and a

venue with extensive space for oral sessions as well as poster presentations.

Finally, an announcement was made by the 2019 team, that SNW will be moved back to Kyoto. Prof. Takahiro Shinada of Tohoku University will be the General Chair and Dr. Toshifumi Irisawa of AIST will be the Technical Program Chair.

Steve S Chung
2018 General Chair

Peter Ye
2018 Technical Program Chair

Pei-Wen Li
2018 Technical Program Co-Chair

~ Kyle Montgomery, Editor

NEW AWARD AT THE IEEE INTERNATIONAL VACUUM ELECTRONICS CONFERENCE

The IEEE EDS Vacuum Electronics Technical Committee will celebrate their first Vacuum Electronics Young Scientist Award to celebrate and inspire a new generation of talented scientists in vacuum electronics during the first phase of their careers. This award recognizes technical achievements, leadership in service, education, innovation and entrepreneurship.

Vacuum electronics is a vibrant and exciting discipline that marked the beginning of electronics. Hundreds of young researchers in industry, academia, and government institutions are active worldwide. The first part of a career in vacuum electronics is full of challenges, achievements, and flourishes new ideas. The new award aims to motivate and recognize outstanding contributions from excellent young scientists.

The new award is also intended to fill a career gap between the Best Student Paper Award, reserved for students, and the John R. Pierce award

for Excellence in Vacuum Electronics, which honors senior distinguished scientists.

The recipient of the Vacuum Electronics Young Scientist (VEYS) Award will be celebrated at the International Vacuum Electronics Conference with a plaque, a check, and an award keynote or mini-plenary talk, to inspire all the young scientists that usually attend the conference.

A candidate must be nominated by a Nominator who is an IEEE member. The candidate need not be an IEEE Member at the time of submission, but must be an IEEE Member to receive the award. A candidate must have a minimum of 5 years experience as a professional in the field of Vacuum Electronics since the last degree and must be under 35 years old at the deadline of the nomination. The candidate must be active in the field of Vacuum Electronics in industry, academia, or government institutions. Areas of interest include, but

are not limited to, design, fabrication, manufacturing, and applications of vacuum electronic devices.

The VEYS Award is awarded by a panel chaired by Dr. Monica Blank (CPI) and composed by members of the EDS Vacuum Electronics Technical Committee. The VEYS Award Panel will evaluate the nominations and select the winner. Eligibility and information for the nomination can be found at <http://www.vacuumelectronics.org/VEYSAward.html>.

The deadline for the 2019 VEYS Award is 30 October 2018.

We look forward for your nomination.

Monica Blank
Chair of the Vacuum Electronics
Young Scientist Award Panel

Claudio Paoloni
Chair of the EDS Vacuum
Electronics
Technical Committee

EDS DISTINGUISHED LECTURER MINI-COLLOQUIUM

SiC: TECHNOLOGY, DEVICES, MODELING

By DANIEL TOMASZEWSKI

The Poland MQ “SiC: technology, devices, modeling” was held on June 20, 2018 at Gdynia Maritime University thanks to the support provided by IEEE Electron Device Society. The Mini-Colloquium was organized by ED Poland Chapter, Gdynia Maritime University, and Instytut Technologii Elektronowej—ITE, Warsaw. A technical support was provided by Department of Microelectronics and Computer Science (Lodz University of Technology)—DMCS. The Mini-Colloquium was opened by Prof. Janusz Zarębski, Rector of Gdynia Maritime University, and Prof. Andrzej Napieralski, Chair of DMCS. Next, six talks were delivered.

Dr. Muhammad Nawaz (ABB Corporate Research) gave a lecture “SiC technology offerings; challenges and opportunities”, focused on the requirements and issues using SiC MOSFETs facing high power applications, and addressing the potential benefits for high power converters. Reliability concerns from the end user’s perspective were addressed as well. Prof. Simon Deleonibus (CEA Research Director) delivered a talk “On the way to the Energy and Variability Efficient (E.V.E.) Era”. He addressed aspects of future nanoelectronics, e.g. requirements for less greedy devices and interconnects, availability and feasibility of autonomous and mobile systems, pursuing zero intrinsic variability, and 3D integration at the device, functional and system levels. Dr. Victor Veliadis (PowerAmerica, NCSU) gave a lecture “SiC power device fabrication and path to commercialization”. He discussed major SiC power device application areas and touched on foundry models, cost reduction strategies, and path to commercialization. The advantages of SiC over other power



Participants (not all) of ED Poland Mini-Colloquium “SiC: technology, devices, modeling”

electronic materials were outlined. SiC devices currently developed for power electronic applications were introduced with emphasis on SiC MOSFETs and SiC Edge Termination techniques. Prof. Henryk Przewłocki (Instytut Technologii Elektronowej) gave a lecture “The importance of the diffusion currents in the photoelectric investigations of the MIS system”. He summarized shortcomings of a standard theory of an internal photoemission in the MIS system, due to neglecting the diffusion current, important at low electric field in the insulator. The speaker presented the modified theory providing perspectives for new measurement methods of the MIS system. Prof. Mike Brinson (Centre for Communications Technology, London Metropolitan University) delivered a talk “Verilog-A compact modelling of SiC devices with Quacs-S, QuacsStudio and MAPP/Octave FOSS tools”. He provided an overview of the fundamentals of the Verilog-A language and its use in compact modelling of established and emerging semicon-

ductor devices including the SiC devices. In the presentation a series of modelling case studies were outlined. Dr. Wlodek Grabinski (MOSS-AK) gave a lecture “FOSS TCAD/EDA Tools for Advanced Compact Modeling”. He discussed selected FOSS CAD tools along a complete technology/design tool chain from nano-scaled technology processes; thru the device compact modeling, to advanced IC design support. The speaker provided application examples of the FOSS TCAD tools and their use for the parameter extraction and PDK development.

The lectures triggered questions from the audience, coming from universities and companies. It is worthwhile to mention participation of PhD students from Indian Institute of Technology, Gdynia Maritime University, and DMCS. A gratitude should be expressed for the local organizers for a well-prepared event and a social support.

~ Marcin Janicki, Editor

TOOLS AVAILABLE TO MAKE IT EASIER TO BE ON BRAND



The IEEE brand is a promise—to our members, volunteers, customers, staff, and the global community—of our dedication to our mission of advancing technology for the benefit of humanity. As a large global organization working across different areas of technology, the IEEE brand family includes many sub-brands, including IEEE Electron Devices Society.

Our brand is a collection of symbols, experiences, and associations that shape how people perceive IEEE and the trust they have in our organization. This trust has been built over time through careful positioning of our brands at every touch point—be it an email, website, phone call, brochure or experience at one of our conferences.

As representatives of IEEE, we have a responsibility to nurture the brand and influence how people see our organization. The IEEE Brand Experience website

offers a multitude of tools and resources to help with this, including:

- Logo files
- Editable templates (including certificates, flyers, banners and more!)
- Brand and digital guidelines
- Downloadable brochures and videos
- Contact information for any brand-related help that is needed

We encourage you to visit the site to see all that is available to you to use now. Thank you in advance for all the work you do in helping to support IEEE and our society!

IEEE Brand Team

branding@ieee.org

IEEE Brand Experience Website:

<https://brand-experience.ieee.org/>

SINANO MODELLING SUMMER SCHOOL AND IEEE EDS MQ ON SEMICONDUCTOR DEVICE MODELLING

By BENJAMIN INIGUEZ

The 8th SINANO Modelling Summer School took place in Tarragona (Catalonia, Spain) from September 25 to 28, 2018, co-organized by the Department of Electronic, Electrical and Automatic Control Engineering (DEEEiA) of the Universitat Rovira i Virgili (URV), in Tarragona. It is also partially sponsored by the SINANO Institute and the DOMINO EU H2020 project. The Chair of this edition of the SINANO summer school is Prof. Benjamin Iñiguez (URV).

During the SINANO Modelling Summer School an IEEE EDS MQ on Semiconductor Device Modelling took place. Lectures were given by Sorin Cristoloveanu (MINATEC, France) on the topic of "Characterization Techniques for Ultrathin Materials and Devices," by Jamal Deen (McMaster

University, Canada) on "Compact Modeling of Organic Thin Film Transistors," by Tibor Grassner (TU-Wien, Austria) on "Multiscale Reliability Modeling," and by Wlodek Grabinski (GMC, Switzerland) on "FOSS TCAD/EDA Tools for Compact Modeling."

The SINANO Modelling Summer School contained lectures given by Javier Mateos (University of Salamanca, Spain) on "Monte Carlo simulation of THz nanodevices based on III-V semiconductors," by Francisco Gámiz (University of Granada, Spain) on "Monte Carlo simulation of emerging Si devices," by Elena Gnani (University of Bologna) on "Steep-slope devices: prospects and challenges," by Thierry Ferrus et al. (Hitachi Cambridge Laboratory, UK) on "Physics of novel devices for quantum informa-

tion science," by François Danneville (IEMN, France) on "Spiking Neural Circuits and Systems," by Montserrat Nafria (Autonomous University of Barcelona, Spain) on "Time Dependent Variability in CMOS devices: characterization and compact modeling," by Kurt Stokbro (Synopsis QuantumWise, Denmark) on "Atomic-scale modeling of semiconductor technology," by Lluís F. Marsal (Universitat Rovira i Virgili, Spain) on "Physics and modeling of organic and hybrid photovoltaic devices," by Ahmed Nejim (Silvaco Europe Ltd., UK) on "Complex structure deformation simulation in TCAD for flexible electronics," by Firas Mohamed (Infiniscale, France) on "Mathematical and Semi-physical modeling for emerging device technologies & needs," by

Sourabh Khandelwal (Macquarie University, Australia) on “Advanced modeling of AlGaIn/GaN HEMT transistors: the ASM HEMT model,” by Thomas Gneiting (AdMOS GmbH, Germany) on Electrical characterization of low frequency noise,” by Radu Sporea (University of Surrey, UK) on “TCAD and compact modeling of source-gated transistors,” by Rodrigo Picos (Universitat de les Illes Balears, Spain) on “Compact modeling of memristors,” by Jean-Pierre Raskin (Université catholique de Louvain, Belgium) on “Current status and trends in RF SOI material and devices,” by Yvan Bonnessieux (Ecole Polytechnique, France) on “Characterization and Modeling of Organic Diodes and TFTs,” by Slobodan Mijalkovic (Silvaco Europe Ltd., UK) on “Mechanical Deformation-Aware Compact Modeling for Flexible Electronics,” by Giuseppe Iannaccone

(University of Pisa, Italy) on “Physics and operation of sonic devices,” and by Benjamin Iñiguez (Universitat Rovira i Virgili, Spain) on the topic “Parameter extraction and modeling of Amorphous Oxide TFTs.”

The SINANO summer school was established in 2005, in the form of the SINANO Network of Excellence (funded by the 6th Framework Programme of the EU). The previous editions were held in Glasgow (2005) and in Bertinoro, Italy (2016, 2014, 2012, 2010, 2008, 2006).

The Sinano Modelling Summer School is a bi-annual comprehensive set of classes aimed at doctoral or post-doctoral level researchers from both industry and academia. Via a program consisting of lectures, tutorials, advanced discussion groups, students will expand and refine their knowledge of the design, optimization, simulation and characterization of cutting

edge semiconductor devices, with the world’s leading device simulation and electrical characterization experts.

This year the SINANO Modelling Summer School targeted multi-scale modelling of semiconductor devices. It includes a total of 23 lectures targeting topics related to the modelling, simulation and characterization of different types of semiconductor devices for nanoelectronics, flexible electronics and photonics. Very hot topics, such as devices for quantum computing, neuromorphic computing, THz electronics and printed electronics will also be addressed. The lecturers are internationally well recognized experts in these fields. The SINANO Summer School is a unique opportunity for young researchers to become familiar with all scales of device modelling and for many.

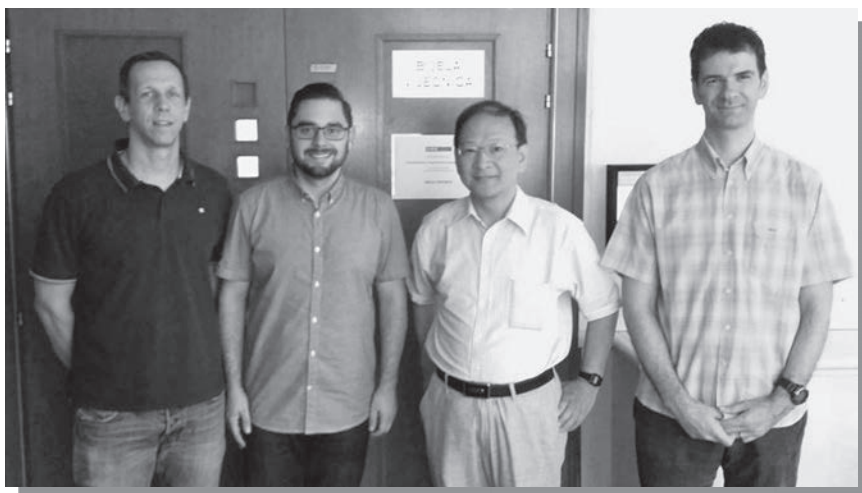
~ Mike Schwarz, Editor

EDS DISTINGUISHED LECTURE—“NANOELECTRONICS: TOWARDS END OF SCALING AND BEYOND”

By MIRKO POLJAK

Prof. Bin Yu from the State University of New York (SUNY), gave an EDS Distinguished Lecture on nanoelectronics and the end of scaling. The seminar was held on June 11, 2018, at the Faculty of Electrical Engineering and Computing, University of Zagreb (UNIZG-FER), Croatia, under the auspices of Prof. Mirko Poljak and Prof. Marko Koričić, Chairs of the Joint ED/SSC Chapter, Croatia section.

Prof. Yu divided the seminar into two parts. In the first part, he gave a review on general trends in nanoscale silicon-based CMOS technology from material, devices, performance, and integration perspective. As one of the examples of the latest industrial efforts, Prof. Yu gave an overview of non-conventional transistor structures with focus on the “three-



Left to right: M. Koričić, M. Poljak, B. Yu (Distinguished Lecturer), T. Suligoj

dimensional” FinFET. In the second part, he discussed the role of emerging nanostructures and the associated

nano-devices in the “post-silicon” era. Prof. Yu explained why graphene has received such significant interest

from academia and industry, by discussing graphene's distinctive layered configuration, band structure, quantum phenomena and manufacturability. Prof. Yu reported about the research achievements of his group at SUNY, which included latest results about logic switches, memories,

and on-chip interconnects based on emerging 2D materials.

There were about twenty attendees including undergraduate and graduate students, university professors and research staff. The audience engaged in interesting and fruitful discussions about the current status of the FinFET

technology, issues in graphene manufacturing and photodetectors based on 2D materials, especially with the members of the Micro and Nano Electronics Laboratory at UNIZG-FER (MINEL, headed by Prof. Tomislav Suligoj).

~ Marcin Janicki, Editor

2018 INTERNATIONAL MEETING FOR FUTURE OF ELECTRON DEVICES (IMFED)

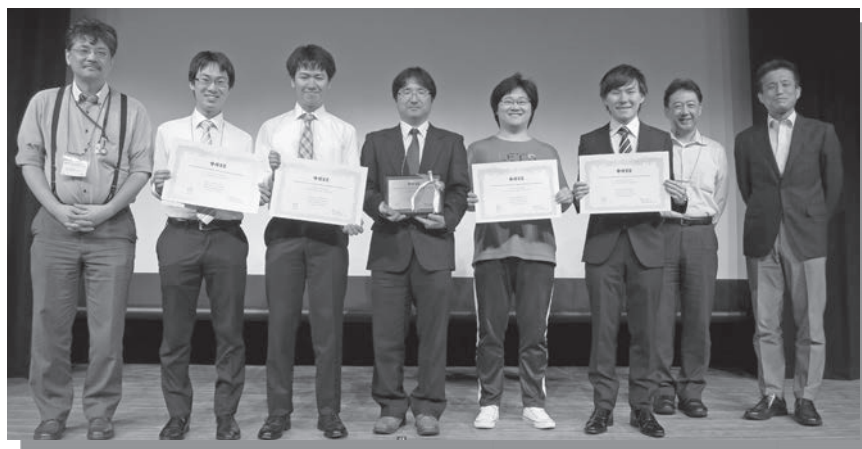
By MICHINORI NISHIHARA

The ED Kansai Chapter held the 16th International Meeting for Future of Electron Devices, Kansai (2018IMFEDK) at Ryukoku University Kyoto Hall, Kyoto, Japan, Jun 21–22, 2018 with the theme of "Emerging Materials and Devices for Next-Generation Electronics." The meeting attracted 93 attendees and was preceded by a tutorial seminar with two Distinguished Lecturers:

- 1) "Present status and issues of retinal prostheses" by Prof. Jun Ohta of Nara Institute of Science and Technology and
- 2) "Recent evolution and future prospects of gallium oxide materials and devices" by Prof. Shizuo Fujita of Kyoto University. The formal program began after the tutorial session with opening remarks by the general chair Prof. Yasuhisa Omura. The two-day program featured a keynote titled "Ferroelectric Thin Films and Electron Devices" by Prof. Masanori Okuyama of the Osaka University.

There also were three invited papers:

- 1) "Future of Tunnel FET for Low-Power High-Frequency Applications" by Prof. Abhijit Mallik of University of Calcutta;
- 2) "Development of corundum-structured gallium oxide power devices by MIST EPITAXY" by Dr. Takashi Shinohe of FLOSFIA;
- 3) "Brain-inspired computing with spintronics devices" by Dr. Sumi-



2018 IMFEDK Awards Winners



2018 IMFEDK Poster Session

to Tsunegi of National Institute of Advanced Industrial Science and Technology.

In addition, there were 13 papers in three regular technical sessions and a

poster session with 19 posters with topics spreading out to Silicon, Compound, and Emerging Technologies, prompting many student discussions in front of their posters during the session.

At the end of the meeting the following awards were presented:

- IEEE EDS Kansai Chapter IMFEDK Best Paper Award to Dr. Hidenobu Mori of University of Hyogo.
- IEEE EDS Kansai Chapter IMFEDK Student Paper Award to the following four persons:

Jiang Yuyang (Kansai University), Hiroki Mito (Osaka Institute of Technology), Takashi Nishitani (University of Fukui) and Ryo Nakajima (Kansai University)

All participants warmly congratulated the award winners. IMFEDK will continue to encourage and contrib-

ute to our student members in the Kansai area by providing opportunities to present their ideas in English, hence extend their technical network to other countries.

~ Kuniyuki Kakushima, Editor

DR. RAJIV JOSHI, EDS DISTINGUISHED LECTURER PRESENTS VARIABILITY AND RELIABILITY OF VLSI CIRCUITS

By FERNANDA IRRERA

Last June 22, at 9 a.m., in the wonderful location of the Centro Congressi of the Federico II University in Via Partenope 34, in Naples (Italy), in front of the Tirrenian Sea, Dr. Rajiv Joshi, Distinguished Lecturer of EDS, gave a Lecture entitled "Winning Over Variability And Reliability Of VLSI Circuits: Is It Possible?"

Dr. Joshi is a Fellow IEEE, Research Leader of the IBM T.J. Watson Research Center, Yorktown Heights NY 10598. He served as a Distinguished Lecturer for IEEE CAS society too, and is a member of IBM Academy of technology. He was recently awarded of the

prestigious IEEE Daniel Noble award for 2018. He is recipient of 2015 BMM award. He is inducted into New Jersey Inventor Hall of Fame in Aug 2014 along with pioneer Nicola Tesla. He is a recipient of 2013 IEEE CAS Industrial Pioneer award and 2013 Mehboob Khan Award from Semiconductor Research Corporation.

The Lecture was focused on the impact on the design yield of process, voltage and temperature variations and model inaccuracies due to technology scaling. Reliability too was introduced as a key concern, which may have significant implications

on functionality and performance. In that Lecture, predictive analytical technique based on statistical analysis methodology targeting both memory and custom logic design applications was highlighted and an efficient statistical methodology to evaluate and minimize the aging of memory chips was proposed.

The Lecture lasted 60 minutes and more than one hundred persons attended, most of which were IEEE members and around twenty of which were PhD students.

~ Mike Schwarz, Editor



Dr. Rajiv Joshi presenting "Winning Over Variability And Reliability Of VLSI Circuits: Is It Possible?"



Fernanda Irrera and Dr. Rajiv Joshi during some discussions

AP/ED BOMBAY CHAPTER'S IEEE EDS MINI-COLLOQUIUM ON "SOLAR PHOTOVOLTAICS"

By ANIL KOTTANTHARAYIL

An EDS Mini-Colloquium on "Solar Photovoltaics" was organized by the AP/ED Bombay Chapter, January 13, 2018, at the Victor Meneses Convention Centre, IIT Bombay. Fifty-four participants attended. The MQ, which was mentored by the EDS technical committee on photovoltaics, included expert lectures on recent advances in PV technology, performance losses in PV systems related to reliability of PV modules and soiling, challenges in integration of PV systems to the grid and business perspectives on PV technology.

After the introductory session, there were technical talks by experts in the field of PV technology. Prof. Vikram Dalal, Fellow IEEE and EDS Distinguished Lecturer, Iowa State University, and spoke on "Recent advances in PV technology." Prof. Juzer Vasi, FIEEE, IIT Bombay gave a talk on "Reliability and Soiling of Photovoltaic Modules in India." Talks were also given by Prof. Anil Kottantharayil, SMIEEE, IIT Bombay and a Dis-



Experts with the participants of the Bombay Mini-Colloquium on Solar Photovoltaics

tinguished Lecturer on "Advanced Silicon Solar Cells;" Mr. Ardeshir Contractor, Founder and Managing Director, Kiran Energy, India, about "Industry perspectives on Photovoltaics"; and Prof. B.G. Fernandes, SMIEEE, IIT Bombay on "Challenges in Grid Integration of Photovoltaics." There was also an evening panel session chaired by Prof. Vasi. The audience participated in the panel dis-

cussion with great enthusiasm and put forth interesting questions to the panel members.

Overall, the mini colloquium was an enriching experience for the participants and served as an excellent platform for dissemination of valuable information regarding advancements in the field of photovoltaics.

~ Manoj Saxena, Editor

25TH INTERNATIONAL CONFERENCE "MIXED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS"—MIXDES 2018

By MARIUSZ ORLIKOWSKI

On June 21–23, 2018, Gdynia, Poland, the International Conference MIXDES 2018 took place. The event was organized by the Lodz University of Technology together with the Warsaw University of Technology. The conference was co-sponsored by Poland Section IEEE ED & CAS Societies, Polish Academy of Sciences (Section of Microelectronics and Electron Technology), and Commission of Electronics and Photon-

ics of Polish National Committee of International Union of Radio Sciences—URSI.

The conference three-day program included 94 talks including invited speeches, as well as oral and poster presentations selected from all submissions from 27 countries.

In addition to the regular programme, there were eight invited speakers:

- *Artificial Intelligence Contribution to eHealth Applications*

Joan Cabestany (Universitat Politècnica de Catalunya, Spain)

- *Commissioning and First User Operation of European XFEL*
Holger Schlarb (DESY, Germany)
- *Footprints of RF CMOS Compact Modeling Technology; From Wireless Communication to IoT Applications*
Sadayuki Yoshitomi (Toshiba, Japan)
- *Learning Robust Feature Representations in Deep Networks for Image Classification*



Group photo of MIXDES participant during banquet on Dar Pomorza—museum sailing ship

- Breton Minnehan and Andreas Savakis (Rochester Institute of Technology, USA)
- *Modern Physical Verification for Advanced Technology Nodes* Wojciech Wójciak (Cadence, USA)
- *Qualification of Electronic Components/Systems for a Radiation Environment of Particle Accelerators: When Standards Do Not Exist* Sławosz Uznański (CERN, Switzerland)
- *Towards a World of More Functions in Integrated Sustainable Systems—* Simon Deleonibus (CEA, France)

- *Virtual Prototyping of μ -Structured Devices and Systems by High-Fidelity Predictive Simulation* Gerhard Wachutka (Technische Universitaet Muenchen, Germany)

The sessions also included presentations in the frame of two special sessions:

- *Compact Modeling for Characterization and Design of Micro- and Nanoelectronic Systems* organised by Daniel Tomaszewski (Institute of Electron Technology, Poland) and Władysław Grabiński (GMC, Switzerland)

- *Large Scale Research Facilities* organised by Stefan Simrock (ITER, France) and Dariusz Makowski (Lodz University of Technology, Poland)

The 2019 MIXDES Conference will take place in Rzeszów, Poland. The Preliminary Call for Papers is available at <http://www.mixdes.org/downloads/call2019.pdf>. More information about past and future MIXDES Conferences can be found at <http://www.mixdes.org>.

~ Marcin Janicki, Editor

16TH MOS-AK WORKSHOP AT ESSDERC/ESSCIRC

By MIKE SCHWARZ

The MOS-AK Compact Modeling Association, a global compact/SPICE modeling and Verilog-A standardization forum, held its 16th MOS-AK Workshop in the timeframe of ESSDERC/ESSCIRC. The event was host-

ed on September 3, 2018, by the TU Dresden in Dresden, Germany. The technical program of the event was coordinated by the MOS-AKTPC Committee. The workshop has received technical program promotion provid-

ed by ASCENT Network, Europractice, EPFL EDIab, IJHSES as well as NEEDS of nanoHUB.org

The MOS-AK workshop was opened by Wladek Grabinski, who has welcomed all the attendees.



Part of the participants of the 16th MOS-AK Workshop at ESSDERC/ESSCIRC, Dresden on September 3, 2018

A group of 30+ international academic researchers and modeling engineers attended 10 technical compact modeling presentations covering full development chain from the nano-scaled technologies thru semiconductor devices modeling to advanced IC design support.

The workshop was chaired by Larry Nagel, OEC (USA), Suba Subramaniam, XFAB (Germany) and Matthias Bucher, TUC (Greece). In the first morning session Wladek Grabinski gave an overview of the MOS-AK Community. Afterwards, Prof. Muhammad Mustafa Hussain from Kaust University (Saudi Arabia) held a talk of "Physically Compliant CMOS Electronics Enabled Interactive Electronic System." It followed a talk by Dr. Sadayuki Yoshitomi from Toshiba Memory Corp. (Japan) gave some insights of "RF CMOS Compact modeling technologies past and future."

Krishna Pradeep from ST Microelectronics (France) started the second morning session with a talk entitled "Analysis and modelling of wafer level process variability in advanced

FD-SOI devices using split C-V and gate current data." Kerim Yilmaz from TH Mittelhessen (Germany) offered a modeling approach for "Scaling correlation between DG & GAA MOSFETs." Dr. Laurie Calvet from Universit Paris-Sud (France) held a talk on "Compact Modeling for Neuromorphic Applications." The morning session ended with "Advanced PDK and Technologies accessible through ASCENT" by Dr. Luca Perniola from CEA (France).

The afternoon session continued with four additional talks, where Dr. Farzan Jazaeri from EPFL (Switzerland) gave a talk on "Reliability Modeling in Harsh Radiation for Space Applications." Prof. Benjamin Iniguez from URV (Spain) explained the latest results on "Low frequency noise modeling of organic and IGZO TFTs." Dr. Mike Schwarz from NanoP (Germany) continued with the topic "Schottky Barrier MOSFET Device Physics for Cryogenic Applications." The session was closed by Dr. Daniel Tomaszewski's talk on various methodologies of "Compact Modeling for Process and Device Characterization."

The MOS-AK speakers have shared their latest perspectives on compact/SPICE modeling and Verilog-A standardization in the dynamically evolving semiconductor industry and academic R&D. The event featured advanced technical presentations covering compact model development, implementation, deployment and all the presentations are available online for download at http://www.mos-ak.org/dresden_2018/.

The MOS-AK Association plans to continue its standardization efforts by organizing future compact modeling meetings, workshops and courses in Europe, USA, China and India throughout coming 2018/2019 years, including:

- 11th International MOS-AK Workshop, Silicon Valley (US) December 5, 2018
- 2nd International MOS-AK/India Workshop, IIT Hyderabad, February 25-27, 2019
- 4th Sino MOS-AK Workshop, Chengdu (CN) June 2019
- 17th MOS-AK at ESSDERC/ESSCIRC, Krakow (PL), September 2019

IEEE WORKSHOP ON MICROELECTRONICS AND ELECTRON DEVICES 2018

By VENKATESH AVULA

The 16th IEEE WMED—Workshop on Microelectronics and Electron Devices was held on April 20, 2018, at the Boise State University, Boise, USA. The event was supported by the IEEE Electron Devices Society, Boise chapter and Micron Foundation. The welcome and opening speech was delivered by Randy Wolff, the General Chair of the workshop. It was followed by two keynote addresses. The first keynote, “Memory: Transforming the Future”, by Russ Meyer from Micron Technology, highlighted the role of vertical integration and multi-level cells in solving the challenges faced by memory industry. In the second keynote, “Nanomaterials for a New Era of Electronics Devices: Extending and Transforming the Trend,” Prof. Aaron Franklin, from Duke University, presented his latest research advances on 2D nanomaterials and its engineering applications like scalable low-voltage negative capacitance transistors, printed electronics and ultrasensitive sensors.

The later part of the workshop had invited tutorials and talks organized in two parallel technical tracks—Process & Devices and Circuits & Systems. In the tutorial titled “Physical Characterization of Advanced Device Materials”, Prof. Robert Wallace from University of Texas, Dallas comprehensively covered physical and chemical characterization of advanced materials

such as III-V, 2DTMDs for defect detection and modeling and the resultant electrical behaviour in devices like Tunnel Field-Effect Transistors, 3D FinFET, Gate-all-around (GAA) FET. In a parallel tutorial session, Dr. Scott Wedge, from Synopsys, has presented “Predicting the Impact of Device Noise on Circuits and Systems” on modeling device noise sources including shot, flicker & fadom telegraph noise (RTN) and performing analyses based on non-linear, time & frequency domain, transient & periodic methods to estimate voltage fluctuation, phase noise and jitter performance of amplifier, oscillator and PLL circuits. Poster session took place during the lunch break. Students also had the opportunity to participate with walk-in posters. Participants showed and demonstrated their projects on the topics of package on package (POP) design, carry lookahead adder (CLA) analysis and improving chemical-mechanical planarization (CMP) planarization efficiency.

The post-lunch session of the workshop had four technical talks and papers. A state-of-the-art talk by Scott Light, from Micron Technology, was on Extreme Ultraviolet (EUV) Lithography, covering its fundamentals, benefits and challenges such as Photon Shot Noise and pellicles. Prof. Ehsan Afshari, from University of Michigan, gave an inspiring talk on

exploring and exploiting ideas behind every day physical phenomenon in designing novel circuits such as Soliton inspired picosecond pulse generator, electrical lens based Fourier transformer and swing pumping principled parametric amplifier. In the emerging devices talk, Dr. Samar K. Saha, from Prospicient Devices, discussed the novel buried-halo MOSFET (BH-MOSFET) device architecture for low power applications. An exciting talk by Dr. Daniel Friedman, IBM T.J. Watson Research Center, highlighted the latest research work on high speed serial link transceivers and architectures at data rates up to 112 Gb/s, including PAM-4 signaling and CMOS optical receivers. After a break, technical paper session followed. Papers on machine learning based predictive maintenance (PdM) techniques, 16 Gb/s GDDR6 memory, memristor and redox-conductive bridge based emerging memory were presented.

The full-day event ended with presenting the best paper and poster awards. The workshop was very well received by the more than 500 attendees from industry and academia, providing forum for discussion and collaboration. The workshop was helped by many sponsors. More information about the IEEE WMED workshop can be found at <http://www.ieeewmedboise.org/>.

~ Kyle Montgomery, Editor

REGIONAL NEWS

USA, CANADA & LATIN AMERICA (REGIONS 1-6, 7 & 9)

IEEE Spokane Section and EDS Chapter Celebrate 105th Anniversary

—by Steve Simmons

The Spokane EDS Chapter joined the Spokane section on Thursday, July 19, 2018, in celebrating the birth of the Spokane section in 1913 and the many engineering events over the next 105 years. Appropriately, the event was held at Barrister Winery, housed in a magnificent 100-year-old warehouse and located in downtown Spokane. The venue, formerly used to warehouse early automobiles, boasts soaring ceilings, exposed brick walls and weathered beams to create an evocative historic ambience. Celebration live music featured local band Cabaret Jive, a celebration buffet with cedar planked wild Sockeye Salmon plus grilled chicken breasts with smoky barbeque sauce, and was attended by about 100 regional engineering members and guests, including the Spokane Section officers and Spokane EDS Chapter Chair, Dr. Steve Simmons.

The section and chapter have much to celebrate. The 105th anniversary year kicked off in Feb, 2018, with the receipt of a major award for the “top small section in IEEE Region 6.” The award was presented at the IEEE San Francisco OpCom meeting, on Feb 3—where the Spokane Section was cited as: “The most active and best organized small section” in the entire region. IEEE Spokane section chair Amber Orr accepted the award, while being applauded by an audience of over 100 IEEE officers and representatives of IEEE USA and around the world.

Other anniversary year highlights included the recent exceptional growth of the Spokane Section—enhanced by the creation of 3 new affiliate organizations in the Spokane region, including the rapidly-growing new Women in Engineering group; a new Spokane Young Professionals group, and a new regional IEEE student group. Both IEEE membership and monthly events were increased by this, since many new activities for these groups were added to the busy IEEE calendar for the area.

Of special interest to the Spokane EDS Chapter was the launch of a new technical presentation series in radio electronics during the 2018 event season. These talks included presentations on topics as diverse as antenna physics, 5G Cellular wireless technical advances, and the use of a composite big-data, computer network and geographically spaced large antenna system to further the SETI project in radio astronomy.

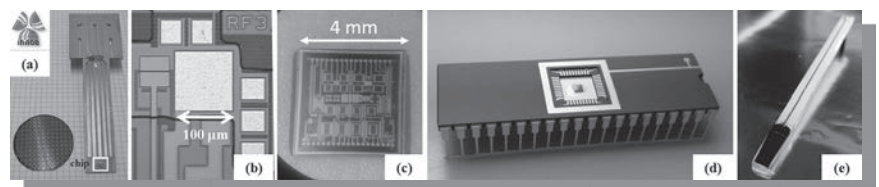
~ Kyle Montgomery, Editor

Nanotechnology for Water Sensing and Treatment

—by Joel Molina-Reyes

A research team at the National Institute of Astrophysics, Optics and Electronics (INAOE) in Puebla-Mexico, has developed a simple semiconductor structure able to measure the concentration of hydrogen ions (pH) in water sources. This parameter (along

with others like turbidity, conductivity, density of bacteria and heavy metals), provide useful information related to the quality of water destined for human consumption. Additionally, this technology for pH detection [1–2] is complemented with treatments based on TiO₂ nanostructures [3–4] that are able to inactivate a large number of common bacteria (*Escherichia coli*) that is present in samples of contaminated water. According to the research team, “The objective of fabricating our own sensors responds to the need of improving their performance, but also, we want to use simpler processing steps in their fabrication so that most universities and research centers are able to develop them with their own infrastructure and with reduced fabrication costs. With this in mind, we have developed a quite practical and portable prototype able to sense pH with good sensitivity. This final device came as a natural evolution of an Ion-Sensitive Field-Effect Transistor (ISFET), which we could fabricate back in the year 2000 after adapting our 5 μm based CMOS process for ISFET development. This working ISFET device was the first of its type in Mexico and was fully designed, fabricated and optimized for pH detection in our labs. Since then, improved and simpler ion-sensitive integrated devices have been continuously developed by adopting more reliable processes and materials as well as simplified device architectures for pH detection here at INAOE.”



Time evolution of integrated ion-sensing devices fabricated at INAOE. (a) First ISFET sensing device, year 2000 (b) floating-gate FG-ISFET devices, fabricated in collaboration with Freescale Semiconductor Corp., year 2010 (c) ion-sensitive capacitors ISCAP, year 2013 (d) ISCAP with higher sensitivity for pH sensing, year 2014 (e) extended-gate EG-ISFET, the simplest architecture for sensing pH, year 2017



Left: electrode covered by an ultra-thin and biocompatible metal oxide film sensitive to pH. Middle: Arduino-based prototype (including the developed electrode) before immersion. Right: measuring the pH of a cup of coffee (pH = 5.50) and which data is constantly transmitted and stored in a smartphone

Dr. Molina's group developed the simple pH sensing structure which, combined with off-the-shelf electronics and the Arduino platform, is able to remotely measure pH in water samples with low power consumption and with high modularity. Additional sensors could also be integrated into a single platform, with the advantage to also realize read-out, processing, storage and wireless transmission of data almost in real-time, which is important for on-field applications. For this sensing solution, an Extended Gate (EG)-ISFET device is quite useful since the materials sensing the pH, are now detached of the electronic transducer (a commercial MOSFET device with low-threshold voltage) and therefore, the highest electrochemical sensitivity for pH detection is now combined with the highest transconductance of a well-known electronic device.

References

- [1] J. Molina "Design and Electrochemical Characterization of Ion-Sensitive Capacitors with ALD Al_2O_3 as the Sensitive Dielectric", *IEEE Sensors Journal*, Vol. 18, pp. 231–236 (2018).
- [2] J. Molina et al., "Integration of MOSFET/MIM structures using a CMOS-based technology for pH detection applications with high-sensitivity", *Procedia Chemistry*, Vol. 6, pp. 110–116 (2012).
- [3] J. Molina et al., "Study on the Photocatalytic Activity of Titanium Dioxide Nanostructures: Nanoparticles, Nanotubes and Ultra-Thin Films", accepted

for publication in *Catalysis Today* (2018). DOI: 10.1016/j.cattod.2018.05.033.

[4] J. Molina et al., "Low-Temperature Processing of Thin Films based on Rutile TiO_2 Nanoparticles for UV Photocatalysis and Bacteria Inactivation", *Journal of Materials Science*, Vol. 49, no. 2, pp. 786–793 (2014).

~ **Edmundo Guiterrez, Editor**

EUROPE, MIDDLE EAST & AFRICA (REGION 8)

ED Scotland

— by **Marc Desmulliez**

On June 12th, the Scottish Chapter of the Electron Devices Society was happy to welcome IEEE Fellow and EDS Distinguished Lecturer, Professor Bin Yu, Chair of Nanoengineering at the State University of New York to speak

to its members and invited guests. The title of Professor Yu's talk was *Nano-electronics: Towards End of Scaling and Beyond*, and was hosted by the Institute for Integrated Micro and Nano Systems at the University of Edinburgh. The lecture started with a review of some general trends in nanoscale silicon-based CMOS integrated chip technology including research on non-conventional transistor structures such as the "three-dimensional" FinFET. This was followed with insights into the role of emerging nanostructures and associated nano-devices in the "post-silicon" era, in particular the growing interest in Graphene and other emerging 2D materials with their distinctive layered configuration, band structure, and quantum phenomena. The audience were introduced to the latest research in logic switches, memories, and on-chip interconnects that have arisen from these material advances. The lecture highlighted both the major challenges and the near-future research opportunities that are available in this exciting field.

Thanks are due to the Universities of Edinburgh and Heriot-Watt, for co-sponsoring the event, which saw an enthusiastic audience of over thirty including academics and researchers from the disciplines of Engineering, Chemistry and Physics. As a result of the diverse audience, a lively and wide-ranging question and answer session following the presentation.

~ **Jonathan Terry, Editor**



ED Scotland Chapter Chair, Marc Desmulliez pictured with IEEE EDS Distinguished Lecturer, Bin Yu

ED Benelux Chapter

IEEE EDS Seminar at IMEC

—by Mike Schwarz

The IEEE EDS seminar was held on September 9, 2018, at IMEC, Belgium. Prof. Hussain gave a talk entitled “Manufacturable Heterogeneous Integration of Compliant CMOS Electronics for Interactive Electronic System.”

Prof. Hussain started with the introduction: “We live in the age of information where electronics play critical role in our daily life. Moore’s Law: performance over cost has inspired innovation in complementary metal oxide semiconductor (CMOS) technology enabled high performance, ultra-scaled CMOS electronics. Moving forward as Internet of Everything (IoE) seamlessly connects people, process, device and data—can CMOS technology be expanded further to achieve new features in CMOS electronics while maintaining and/or strengthening existing attributes? Will the functionalities over cost be advantageous? Can the existing applications be further strengthened and/or diversified? What potential applications may emerge?”

To address these questions, Prof. Hussain discussed rational design of materials, processes and devices to develop robust manufacturing processes through heterogeneous integration of state-of-the-art CMOS technologies to transform conventional high performance but rigid CMOS electronics into fully compliant one; various printing techniques (inkjet for interconnects, 3D printing for encapsulation); electrochemical deposition (ECD) for through polymer via (TPV); automated transfer; Lego like lock and key assembly; non-functionalized household papers and other responsive materials based sensors and actuators, respectively and finally their roll-to-roll processing to achieve nature inspired fully compliant in-plane and out-of-plane CMOS electronics for emerging IoE applications. He also showed a few examples on their extensive work on interactive electronic

system and discuss the design criteria as a new generation of add-on, wearable and implantable electronics.

Biography

Dr. Muhammad Mustafa Hussain (PhD, ECE, UT Austin, Dec 2005) is a Professor of Electrical Engineering, KAUST. He was Program Manager in SEMATECH (2008–2009) and Process Integration Lead for 22 nm node FinFET CMOS in Texas Instruments (2006–2008). His research is focused on futuristic electronics which has received support from DARPA, Boeing, Lockheed Martin, GSK-Novartis and SABIC. He has authored 300+ research papers and patents. His students are serving as faculty in KFUPM, KAU, Jeddah University and as researchers in MIT, Caltech, UC Berkeley, Harvard, UCLA, TSMC, and DOW Chemicals. He is a Fellow of American Physical Society and Institute of Physics, a distinguished lecturer of IEEE Electron

Devices Society, and an Editor of IEEE T-ED. Scientific American has listed his research as one of the Top 10 World Changing Ideas of 2014. Applied Physics Letters selected his paper as one of the Top Feature Articles of 2015. He and his students have received 41 research awards including IEEE Outstanding Individual Achievement Award 2016, Outstanding Young Texas Exes Award 2015 DOW Chemical Sustainability Challenge Award 2012, etc. His research has been highlighted extensively in international media like in Washington Post, Wall Street Journal (WSJ), IEEE Spectrum, etc.

ED Germany Chapter

2nd Symposium on Schottky Barrier MOS Devices

—by Mike Schwarz

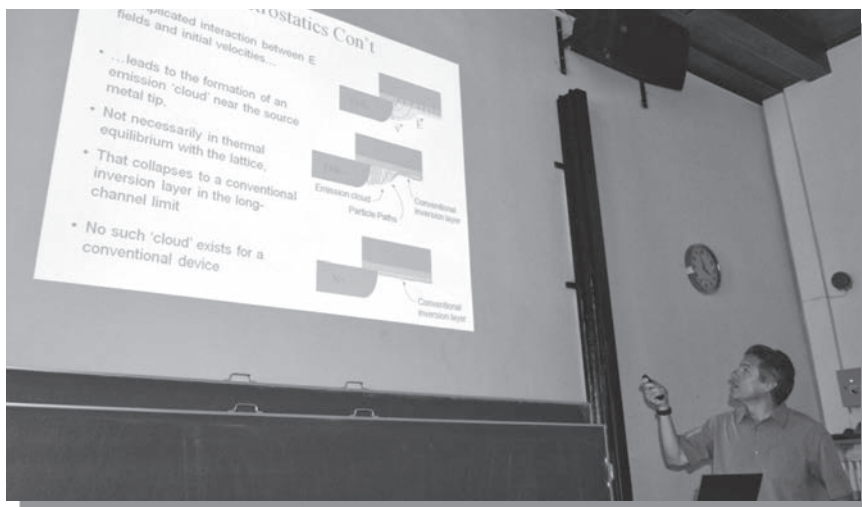
The 2nd Symposium on Schottky barrier MOS devices was held on August



Prof. Schwalke welcomes the symposium participants



Fabian Horst presents DC/AC Compact Modeling of TFETs



Dr. John Snyder discussing the electrostatics of Schottky barriers



Dr. Walter Weber presenting NamLab activities



Participants discussing the different topics of the symposium

7th, 2018, at the IHTN of TU Darmstadt. It was sponsored by the EDS German chapter and hosted and sponsored by the IHTN of Prof. Schwalke from TU Darmstadt. It was a pre celebration conference regarding the 40th anniversary of Institut für Halbleitertechnik und Nanoelektronik (IHTN).

The symposium, chaired by Prof. Alexander Kloe from NanoP of Technische Hochschule Mittelhessen, started with a welcome by Prof. Schwalke from the Institute and an introduction that Schottky barriers in terms of the semiconductor rectifier effect were first observed by Karl Ferdinand Braun (born in Hessen, Germany) almost 144 years ago. Furthermore, Walter Schottky received an honorary Ph.D. from TU Darmstadt.

Afterwards, Dr. Mike Schwarz from Robert Bosch GmbH gave a talk about simulation methodologies for Schottky barrier simulations including hints to account for more precise results.

Fabian Horst, Ph.D. candidate from Technische Hochschule Mittelhessen presented compact modeling approaches for TFETs in comparison with measurement data and how Schottky barriers play an important role in combination with AC capacitance measurements.

The morning session ended with an impressive talk and discussion by Dr. John Snyder from JCap, LLC who discussed the benefits of Schottky Barrier versus conventional doped Source/Drain MOS devices.

The afternoon session started by an impressive overview of the NamLab activities given by Dr. Walter Weber from TU Dresden. One topic besides many others was the epitaxial growth of NiSi₂ on Si nanowires for perfectly aligned Schottky barrier interfaces.

Prof. Schwalke followed with a detailed talk about the activities of IHTN entitled "Nanoelectronics: From Silicon to Carbon" with the latest results.

After a short coffee and refreshment break Dennis Noll, Ph.D. candidate from TU Darmstadt, gave an interesting talk about the fabrication

of transfer-free fabrication of nanocrystalline graphene and its application as a gas sensor. He also showed the measurement setup for in-situ vacuum gas measurements.

Finally, the symposium was closed by an excellent talk in the field of neuromorphic devices and the modeling approaches given by Dr. Laurie Calvet from Université Paris-Sud, France.

ED Italy Chapter

Seminar "Tapping into Solar Energy by Rectenna Technology" at Sapienza University, Rome

—by *Fernanda Irrera*



Professor Ivona Z. Mitrovic

Last May 28, at 2:30 p.m., in the Sala Affrescata del Chiostro of the Engineering Faculty of the Sapienza University, Rome (Italy), Prof. Ivona Mitrovic held a Seminar entitled

"Tapping into Solar Energy by Rectenna Technology."

Ivona Z. Mitrovic (PhD, MSc, BSc EE) is a Professor at the Department of Electrical Engineering and Electronics, University of Liverpool, UK, conducting research on materials and devices for RF communications, advanced CMOS, energy harvesting. She led activity on innovative germanium devices for industrial production target in 2018. Current research includes nanodevices for terahertz energy harvesting and healthcare applications.

The Seminar was focused on strong energy harvesting. Current world energy consumption is ~10 terawatts (TW) per year, with projection of ~30TW by 2050. The terawatt challenge is the effort to supply up to 30 TW of carbon-free power by 2050, to stabilize CO₂ in the atmosphere. Only solar energy can meet this level of demand. This talk will explore the rectenna concept to tap into solar energy, in particular focusing on a diode nanostructure that can work at THz frequencies.

The Lecture lasted 60 minutes and around twenty students of the Master Degree in Electronics Engineering, ten PhD students and a few Professors attended.

ED Spain Chapter

IEEE EDS Seminar at the Universitat Rovira i Virgili (URV)

—by *Benjamin Iniguez and Mike Schwarz*

The Department of Electronic, Electrical and Automatic Control Engineering of the Universitat Rovira i Virgili (URV), in Tarragona (Catalonia, Spain), organized the 16th Graduate Student Meeting on Electronics Engineering, from June 28 to 29, 2018. It is an annual event that consists of two days of plenary talks given by invited prestigious

researchers about selected topics related to electronic engineering (with emphasis on semiconductor devices and sensors), short talks and poster presentations given by Ph. students presenting their last research results.

Prof. Henryk Przelawski, from the Institute of Electron Technology in Warsaw (Poland), gave a talk as EDS Distinguished Lecturer, entitled "The new approach to photoelectric properties of the MIS system at near zero photocurrents. Theory and Applications."

There were three more plenary talks. Prof. Bram Heijs (Leiden University Medical Center, The Netherlands) addressed "Mass Spectrometry Imaging in Clinical Research." Prof. Joan Josep Cerdà (Universitat de les Illes Balears, Spain) targeted "Magnetic filaments: a new promising technological field." Finally, Prof. Maria Pilar



PhD students presenting their last research results during a poster session



Presentation about compact modeling of Tunnel-FETs, given by PhD candidate Fabian Horst

Pina (University of Zaragoza, Spain) conducted a lecture entitled "Smart Surfaces for SERS Detection." In addition, this event included nine Student talks and ten Student posters.

~ **Mike Schwarz, Editor**

ED Romania Chapter

—by *Cristian Ravariu*

ED Romanian Chapter Welcomes Distinguished

Lecturer Prof. Adrian M. Ionescu

The ED Romania Chapter held a special colloquium as a technical meeting with invited Distinguished Lecturer

Prof. Adrian M. Ionescu from EPFL. The colloquium was held on May 17, 2018, in "Universitatea Politehnica Bucuresti", Bucharest, Romania, at the Faculty of Electronics.

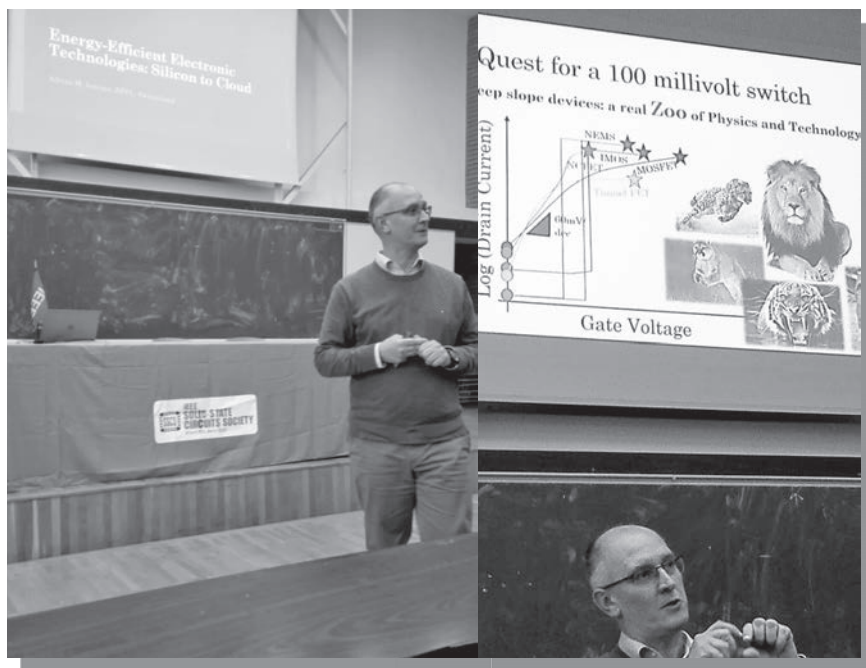
Professor Adrian M. Ionescu is a Director of the Nanoelectronic Devices Laboratory at Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland. He served as Director of the Doctoral Program in Microsystems and Microelectronics of EPFL. His group pioneered new concepts in low power beyond CMOS devices and technologies. He is the recipient of the IBM Faculty Award 2013 and of the André Blondel Medal 2009 of

the Society of Electrical and Electronics Engineering, Paris, France. He is an IEEE Fellow and a member of the Swiss Academy of Sciences (SATW). In 2016, he was awarded an Advanced European Research Council Grant to develop energy efficient millivolt transistors and sensors for Internet-of-Things.

Prof. A. M. Ionescu was invited to give a talk on "Energy-Efficient Electronic Technologies: Silicon to Cloud." More than 120 people attended the colloquium. Prof. Ionescu emphasized some of the great research challenges and opportunities related to energy efficient computing and sensing devices and systems, in the context of the Internet of Things (IoT) revolution in the 21st century. In the future, major innovations will require holistic approaches encompassing silicon and cloud technologies. There is still an important role to be played by innovations in energy efficient technologies, devices, and system design, building on the success of silicon CMOS. The presentation suggested that CMOS, beyond CMOS, neuromorphic and quantum computing platforms could co-exist and co-develop in the new electronic ecosystem centered on big/abundant data.

This event was organized by the ED Romania Chapter. A technical support for the colloquium was provided by SSCS Romanian Chapter and by the Doctoral School of the Faculty of Electronics Telecommunications and Information Technologies in Bucharest.

~ **Daniel Tomaszewski, Editor**



Prof. Ionescu from EPFL, Lausanne, Switzerland, gives a talk to the ED Romanian Chapter and IEEE members



The audience of Prof. Ionescu's lecture consisted of students, professors, and people from industry

ASIA & PACIFIC (REGION 10)

ED Japan Joint Chapter

EDTM-2018 (IEEE Electron Devices Technology and Manufacturing) Report Session

—by Akira Nishiyama
and Yuichiro Mitani

On August 2, 2018, the report session of IEEE EDS 2nd Electron Devices Technology and Manufacturing (EDTM) Conference 2018 (<http://ewh.ieee.org/conf/edtm/2018/>) was held at Tamachi campus of Tokyo Institute of Technology. Prof. Hitoshi Wakabayashi, General Chair of EDTM-2018 and Dr. Kazunari Ishimaru, Technical Program Chair of EDTM-2018, reported EDTM-2018 activities and the next EDTM-2019 plans. At the report session, the subcommittee members reported the trends of the respective technical sessions. After that, the following topics selected from outstanding papers were introduced and discussed.

- “Electrode material dependence of resistive switching behavior in Ta_2O_5 resistive analog neuromorphic device” and “Direct Observation of Chemical States in ReRAM by Laser-based Photoemission Electron Microscopy,” by Dr. Hiroyuki Akinaga (AIST).
- “Origin of High Mobility in InSn-ZnO MOSFETs,” by Dr. Keiji Ikeda (Toshiba Memory).
- “Top gate Sputtered MoS_2 FET” and “P/N-stacked NW on Fin-FET,” by Prof. Hitoshi Wakabayashi (Tokyo Institute of Technology).

The program and announcement of this report session are posted on the Japan Chapter’s webpage; (<https://www.ieee-jp.org/section/tokyo/chapter/ED-15/>)

The next EDTM (IEEE EDTM-2019) will be held at Marina Bay Sands, Singapore, on March 12–15,



The report session of EDTM-2018 (IEEE Electron Devices Technology and Manufacturing) attendees on August. 2, 2018, Tokyo

2019. (<http://ewh.ieee.org/conf/edtm/2019/>)

~ Kuniyuki Kakushima, Editor

ED/SSC Hong Kong Chapter

IEEE Electronic Endeavor Match

—by Yang Chai

Following the success of the 1st IEEE Electronic Endeavor Match in 2017, the 2nd IEEE Electronic Endeavor Match was held in Hong Kong Science Park on April 7, 2018, which was hosted by the ED/SSC Hong Kong

Chapter. There have been efforts to introduce electronic circuit concepts as part of the STEM (Science, Technology, Engineering and Mathematics) to pre-university students. The IEEE Electronic Endeavor Match is aimed as recognizing primary and secondary school students who have developed their interest and skill in constructing electronic circuits.

The participants were from different elementary and middle schools in Hong Kong. The 98 participants were divided into three different groups according to their age. After 3-phase competition, the committee



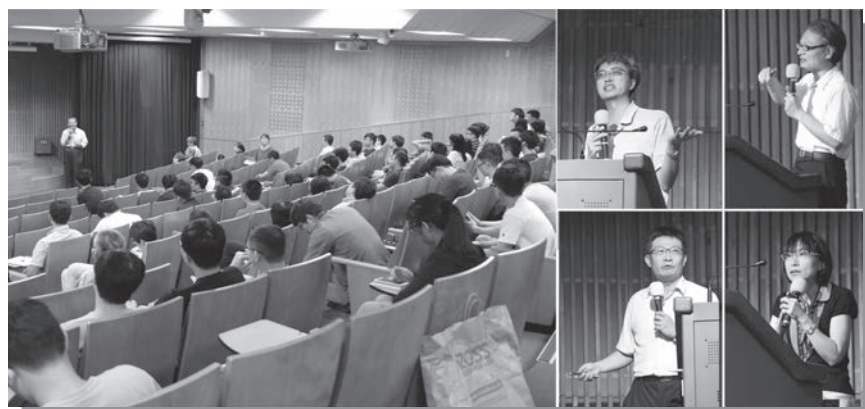
(Upper left) The host explaining rules of the competition; (Upper right) Venue of the Competition; (Lower left) A contestant constructing her circuit; (Lower right) Award ceremony

selected three awardees and the best design award from each group. The students exhibited their interest in electronic circuits and provided positive feedback on this event. More information about the match can be found at <http://www.ieee-elex.org/eem2018>.

ED Taipei Chapter and EDS NCTU Student Chapter

—by Steve Chung

The ED Taipei Chapter together with the EDS NCTU Student Chapter held one invited talk and a workshop in the second quarter of 2018. The invited talk was held April 20th, with Dr. T. Endo, AIST Japan, giving a talk entitled, "Post Silicon Devices Technology and Related TCAD Developments at AIST." Dr. Endo presented the current research activities at AIST where the research focus has been on exploring device integration technologies for going beyond the performance limit of Si CMOS. The research topics include Ge/III-V MOSFET, 3D build-up integration, 2D channel materials, and devices incorporating new materials and mechanisms such as spin FET and negative capacitance FET. He also introduced the methodology and modeling of TCAD simulation and their application for various semiconductor devices. The research activities at AIST is on the cutting-edge technology and they welcome



ED Taipei—Workshop on June 29th (left) the auditorium, Steve Chung (give the briefing); (right) clockwise, speakers: Profs. T.H. Hou, K. S. Chang-Liao, P.W. Li, and H. C. Lin

collaborations worldwide. This talk was attended by around 30 professors and graduate students, most of them EDS members.

One major occurrence in the region and premier event on VLSI, the leading technology conferences worldwide for over 35 years, 2018 VLSI-TSA and VLSI-DAT, held April 24–27, 2018 (<http://expo.itri.org.tw/2017vlsitsa>). Both are mainly sponsored by the IEEE EDS and SSCS, and attract over 850 attendees from around the world for the technical sessions and more than 350 for the short course series. About 60% of attendees are from industries and 40% from universities. Next year, the conference will once again be held in Hsinchu, Taiwan and is scheduled for to be held April 16–19, 2019. The paper submission

deadline is October 31, 2018 (<http://expo.itri.org.tw/2018vlsitsa/Submission>). For further information, please contact Miss Evelyn Chou, vlsitsa@itri.org.tw.

Another important workshop is a one day post-conference review of IEEE SNW and VLSI, which were held June 17–18 and June 18–22, respectively, in Hawaii. The post-conference review was held June 29, 2018. For those who did not have chances to attend the conferences, the chapter asked experts who participated in both conferences to present several major topics from the conferences. The six topics presented were: (1) Advanced Device Technology Reported at SNW (K. S. Chang-Liao), (2) Ge(Sn)/III-V Device Technology (P. W. Li), (3) Memory Technology (T. H. Hou),



ED Taipei—Invited Talk on April 20th (left) The speaker T. Endo (1st row, 5th from left), seminar chair Steve Chung (4th) with EDS members; (right) T. Endo (speaker)

(4) Logic Device Technology (H. C. Lin), (5) Negative-Capacitance Device Technology (Y. T. Tang), (6) AI and IOT-Related Device/Circuit Technology (E. R. Hsieh). Three out of the 6 speakers were presenters at the VLSI Technology Symposium.

At the end, Prof. Steve Chung made a briefing of the status of both SNW and VLSI, which were very successful by comparison to two years ago in Hawaii. The SNW has a historical record with the largest number of paper submissions as well as participants. The VLS Symposium has an increase in the number of participants to short courses by 30% and an increase in the number of technical sessions by more than 10%. Finally, the chapter provided 7 free memberships to students joining as new members. This is to encourage participation of students in the IEEE Electron Devices Society, as well as to help further their careers in the field of semiconductors. This talk was attended by more than 130 professors and graduate students, and engineers from the science park.

~ Ming Liu, Editor

ED Malaysia Kuala Lumpur Chapter

—by Aliza Aini Md Ralib & Afishah Alias

Technical Talk by Prof. Marco Lonca from Harvard University

On April 13, 2018, the chapter and the Institute of Microengineering and Nanoelectronics (IMEN), UKM organized a technical talk at IMEN, UKM. The invited speaker was Prof. Marco Lonca from Harvard University. The talk entitled “Recent Advance in Integrated LiNbO₃ Materials” was very interesting and useful to other researchers and students. Mainly, it was the sharing about aim at the development of integrated lithium niobate platform, featuring sub-wavelength scale light confinement and dense integration of optical and electrical components that has the potential to revolutionize optical communication and microwave



Students and members of the EDS UKM Student Branch



Students with their certificates at the end of the EDS-ETC program

photonics. A total of 50 staff and students attended Prof. Lonca's lecture.

UKM EDS SB AGM at Puri Pujangga Hotel, Universiti Kebangsaan Malaysia

On April 18, 2018, the ED UKM Student Branch held their Annual General Meeting (AGM) at Puri Pujangga Hotel, Universiti Kebangsaan Malaysia, for the official dissolution of the 2017 session committee and the election of the Executive Committee for 2018 Session. A voting exercise was held and Muhammad Izzuddin Abd Samad won the post of Chapter Chair. The newly elected Chapter Chair hopes everyone will work together closely and actively participate in activities in order to achieve the IEEE vision and mission.

Engineers Demonstrating Science: an Engineer Teacher Connection (EDS-ETC) Activities

Continuing from numerous programs conducted in 2017, the chap-

ter is committed in promoting the EDS-ETC program by conducting a fun and exciting event “Electronics Magic” with primary school students (Year 3), of Sekolah Rendah Islam Al Amin Gombak, Selangor. A total of 83 students participated in the event. In showing the wonderful world of electronics at an early age, the program was conducted through exploration games where at each check point, the students were required to construct the Snap Circuits and understand the theory behind it. The event was conducted in collaboration with Persatuan Saintis Muslim Malaysia (PERINTIS).

Membership Drive and Technical Talk at UPSI

On April 25, 2018, the chapter organized a membership drive for students at UPSI headed by the Chapter Vice-Chair, Dr. Norhayati Soin. A total of 40 staff and students attended the talk.



Gathering after ED Malaysia Chapter membership drive and talk at UPSI

2018 IEEE EDS Malaysia Final Year Project Award

The chapter sponsored eleven prizes for the 2018 Final Year Project Award organized by several universities in Malaysia. The award is to encourage FYP projects related to the area of VLSI, MEMS/NEMS, micro and nanoelectronic devices, and to acknowledge students working in these areas. A complete list of winners can be obtained from the chapter. Congratulations to all winners!

ICSE2018 Technical Review Meeting and "Buka Puasa" Social Event at Tenera Hotel

The chapter organized a Buka Puasa event as part of the program planned for the Social and Community Portfolio on May 24, 2018 at Tenera Hotel, Bandar Baru Bangi, Selangor. The 2018 IEEE EDS Buka Puasa event program welcomed EDS members to a lively and meaningful event. The event was immediately after the ICSE 2018 technical meeting, which was held from

4 pm to 7 pm at the same venue. The Buka Puasa event started began 7.20 pm exactly, at the Maghrib prayer time. All EDS members enjoyed the buffet with a variety of local and international food and beverages, as well as special cuisines prepared for the Buka puasa event. Attendees also enjoyed exchanging news and ideas between members during this beautiful event.

~ P. Susthitha Menon, Editor



EDS members after ICSE 2018 technical meeting

ED Delhi Chapter

—by R. S. Gupta and Sneha Kabra

On January 8, 2018, IIT Delhi in collaboration with the chapter organized a Distinguished Lecture (DL) on “**Electronics for all**” by Prof. Muhammad Mustafa Hussain (KAUST, Thuwal, Saudi Arabia). This DL emphasized on attributes of the future generation of physical electronics including: (i) dynamic performance; (ii) ultra-low to self-powered operation (i.e. co-integration of energy harvesters); (iii) robust communication; (iv) interactive (data acquisition through sensors, data processing, storage, communication and decision execution through actuators will be heterogeneously integrated); (v) democratized (easy to understand, simple to implement, use and affordable), and (vii) free form (physically flexible, stretchable and reconfigurable to conform to the soft tissue, irregular contour and asymmetric skin surfaces of living beings: human, plants and animals). The talk was attended by about 45 people, including students and faculty.

On January 9, 2018, IIT Delhi in association with the Chapter organized a seminar on New Era of Electronics: Devices, Packaging, Systems and Global Markets, by Prof. Rao R. Tummala, Georgia Institute of Technology, Atlanta, USA, and another talk on March 21, 2018 on Non-reciprocal photonics with optomechanical resonator systems by Dr. Gaurav Bahl, University of Illinois, Urbana-Champaign, Illinois.

The Two-Day National Workshop on Advances in Interdisciplinary Sciences, organized by the Department of Electronics, University of Jammu in collaboration with the Chapter and IETE Jammu Centre, was held on January 11–12, 2018, at University of Jammu. In this workshop more than a hundred papers were presented as oral and posters by the faculty/scientists/research scholars of the various institutions in and around J&K and outside in different disciplines. Prof.

Haq Nawaz, Prof. Namarta Sharma and Dr. Shah Jahan Wani acted as jury members in the Chemical Sciences, Life Sciences & Electronics sections respectively, whereas Prof. K. K. Bamzai, Prof. Vinod Sharma, Dr. Romesh Kumar and Dr. Ravender Tickoo acted as jury members in the Physical Sciences, Mathematical Sciences & Computer Science sections.

The Chapter and Sri Venkateswara College, University of Delhi jointly organized the Lecture on Incubation and Entrepreneurship in ESDM (Electronic System Design and Manufacturing) on February 6, 2018, at Sri Venkateswara College for the under-graduate students. The CEO (Mr. Sanjeev Chopra) of Electropreneur Park, University of Delhi South Campus, enlightened the students about incubation in ESDM sector, various programs and opportunities offered by them for the students in terms of an internship, mentorship, and an insight about how an idea can

be converted into a product/service, which also has commercial viability.

On February 2, 2018, the chapter in collaboration with the Department of Electronics Science, University of Delhi and CoreEL Technologies, organized a technical demonstration of FPGA Implementation on Xilinx Hardware Boards, which was attended by 40 students and faculty members.

An International Conference on Applicable Mathematics was organized by the Department of Mathematics, Motilal Nehru College, Delhi University, in association with the Chapter on February 19–20 2018. A group of seven plenary speakers from around the world; Asgar Rahimi (Iran), Mati Abel (Estonia), Mart Abel (Estonia), Juan H. Arrendondo (Mexico), Gabriel Kantun Montiel (Mexico), and Reyna Maria Perez Tiscareno (Mexico) became a part of this conference. There were six short talks, one invited talk and around forty-five paper presentations held.



Address by Chief Guest Prof. R. D. Sharma, Hon'ble Vice Chancellor, University of Jammu, Jammu



Organizers and Participants of International Conference on Applicable Mathematics at Motilal Nehru College, University of Delhi



Prof. Mridula Gupta with Resource persons, Mr. Ankur Sangal and Mr. Paramahans from CoreEL Technologies, along with participants of the workshop

IIT Delhi in association with the Chapter organized a seminar on New Era of Electronics: Devices, Packaging, Systems and Global Markets at IIT Delhi on March 9, 2018. The speaker was Prof. Rao R. Tummala, Georgia Institute of Technology, Atlanta, Georgia, USA. Another Invited talk on Non-reciprocal photonics with optomechanical resonator systems by Dr. Gaurav Bahl, University of Illinois, Urbana-Champaign, Illinois was organized at IIT Delhi on March 21st.

Under the aegis of Delhi Chapter, Department of Electronic Science, University of Delhi South Campus and CoreEL Technologies jointly organized Workshop on VLSI Current Trends Using Mentor Graphics & Xilinx on March 21–22, 2018. The participants were given hands on training on describing the general Artix-7 All Programmable FPGA architecture, Understanding the Vivado design flow, Configuring FPGA and verify hardware operation, Creating and integrate IP cores into design flow using IP Catalog and Using Logic Analyzer to perform on-chip verification.

ED Meghnad Saha Institute of Technology Student Branch Chapter

—by Manash Chanda and Swapnadip De

The ED MSIT Student Branch Chapter and MSIT Student Branch, in as-

sociation with the Department of ECE, MSIT organized the One Day IEEE EDS Distinguished Lecture by Prof. Muhammad Mustafa Hussain, Professor, Electrical Engineering Computer Electrical Mathematical Science and Engineering Division King Abdullah University of Science and Technology (KAUST) on January 11, 2018 at the Seminar Room of MSIT. The topic of the talk was “Electronics for all” which was attended by 60 students.

One week summer training on “Advance VLSI Design and IoT” was organized by the Chapter in association with the Department of ECE from January 5–12, 2018, in the Advance VLSI Design Lab. The program covered transistor level modelling

and simulation of the arithmetic and logical building blocks using Non-planar MOSFET, Internet on Things (IoT) based projects etc.

A membership awareness program was organized by the chapter on February, 13th to share the importance of IEEE membership and the activities of the ED SBC with the 2nd year students of the Dept. of ECE.

On March 24, 2018, “Electroclash” was organized by the Chapter in association with the “Megatronix” club in “PARIDHI 2018”. The event was based on “spot simulation” and certain problem statement was provided to individual one. The student who could provide an optimal solution using minimal components for the program was given the prize. A total of thirty-eight members registered for the event, of which twenty were IEEE student members. “Electro-survivor” was organized by the ED MSIT SBC on March 25th in association with the “PARIDHI 2018”. This event was organized to encourage the students towards circuit design in the field of electronics. Almost twenty-two teams participated, with two members on each team. There were thirty IEEE student member attendees in this event. The first round was circuit rectification and the next round was to design a circuit on the basis of problem statement given.



Participants of ED MSIT Student Branch Chapter activity

ED Calcutta Chapter

—by Manash Chanda and
Angsuman Sarkar

The ED Calcutta Chapter and IEEE Techno India-Batanagar Student Branch in association with ED Calcutta University Student Branch Chapter jointly organize a one-day Technical talk on “Low Power VLSI Design” by Dr. Soumya Pandit, Assistant Professor, Institute of Radio Physics and Electronics, University of Calcutta, SRC Vice Chair- EDS Region 10 on February 20, 2018. Almost sixty students attended the event. Dr. Pandit not only discussed the various aspects of VLSI Circuits and Systems but also derived numerical examples over white board to make the session interactive and interesting.

February 23, 2018, a technical project competition was organized by the Chapter and IEEE Techno India – Batanagar Student Branch. More than 80 projects were demonstrated by the engineering and school students. Prof. (Dr.) Angsuman Sarkar, Chair, IEEE EDS Calcutta Chapter and Prof. (Dr.) Manash Chanda, Secretary, IEEE EDS Calcutta Chapter judged the competition under the project category of ECE & EE division. They interacted with student participants and motivated them to carry on the research work. They encouraged the students to join IEEE and publish their work in papers in the seminars/conferences organized by IEEE. More than 150 students participated in the project competition



Dr. Manash Chanda, Secretary, IEEE EDS Calcutta Chapter, judging in Project Exhibition at TIG Batanagar, Kolkata



Group picture of IEEE EDS Technical Talk by Dr. Soumya Pandit, SRC Vice Chair, IEEE EDS, R-10

including around twenty IEEE student members.

The ED Calcutta Chapter and IEEE Techno India-Batanagar Student Branch, in association with Dept. of ECE organized a one-day IEEE EDS Distinguished Lecture on “Future Challenges and Advanced Innovations in VLSI Design” by Prof. (Dr.) Subir Kumar Sarkar, Senior Member IEEE & IEEE Distinguished Lecturer of the IEEE Electron Devices Society, Professor & Former Head, Department of Electronics and Telecommunication Engineering, Jadavpur University on March, 29, 2018.

ED University of Calcutta Student Branch Chapter

—by Soumya Pandit

A technical lecture was organized by the ED University of Calcutta Stu-

dent Branch Chapter December, 12, 2017, in the Institute of Radio Physics and Electronics. The talk on VLSI Design of Cellular Automate (CA) based coding, was delivered by Prof. Jaydeb Bhaumik, Associate Professor of ETCE Department, Jadavpur University and emphasized the fundamental issues related to cellular automata, information theory and coding and VLSI design of the same. A total of twenty participants, including 12 EDS members and 5 faculty members, attended the program.

An outreach technical lecture was organized by the chapter on February 20, 2018 at Techno India Batanagar College, Kolkata, on Low Power VLSI Design. The talk was delivered by Dr. Soumya Pandit, Assistant Professor, Institute of Radio Physics and Electronics, University of Calcutta. The fundamental issues related to the



Speaker and some participants of the VLSI Design of Cellular Automate talk on December 12th



Some of the participants of the Low Power VLSI Design talk on February 20th

dissipation of power in MOS circuits were clearly explained, and the present day strategies to minimize power dissipation of CMOS circuits at various levels of abstraction were discussed in detail. The program was attended by nearly 60 members including a few faculties of the host institute and several EDS student volunteers.

ED NIST (National Institute of Science & Technology) Student Branch Chapter

—by Ajit K Panda

The ED NIST Student Branch Chapter organized a technical lecture on **“Scaling vs ESD: The driving strength of Semiconductor Industry”** on February, 21, 2018 at the National Institute of Science & Technology, Palur Hill, and Berhampur, for the graduate and undergraduate students to enhance their research activity. Mr. Basudev Dash, currently working as a Sr.

Analog Design Engineer at Intel Corporation, US, was invited to speak. During the interaction he pointed the technology scaling and his experience with 45 nm, 22 nm, 16 nm, 7 nm and beyond. Technology scaling solves many issues at a cost of ESD. ESD protection plays a major role for improving yield. Approximately 120 participants attended the talk and responded with a very nice interactive session.

The Chapter also organized the 4TH National Conference on Devices and Circuits (NCDC-2018) on February 24, 2018 at National Institute of Science & Technology, Palur Hill, and Berhampur for the final year graduate and undergraduate students. More than 80 participants registered from different institutes and universities from Odisha and outside as well. Approximately 60 papers were received from different universities and institutes like NIST Berhampur, KIIT Bhubaneswar, VSSUT Burla, University of Calcutta and many other research institutes in devices, circuits, and testing.

The selection committee selected 42 papers for publishing in the proceedings of the 4TH National Conference on Devices and Circuits with ISBN number 978-93-83060-16-0. Professor Rakesh Vaid from University of Jammu and Professor Soumya Pandit from University of Calcutta gave the invited talks in two different sessions. The works “Effect of Cap Layer in an InP/InGaAs Metamorphic

δ -doped Heterojunction Bipolar Transistor” and “RTL Implementation of Programmable Peripheral Interface using UMC180nm Technology” were awarded as best presentation in device and circuit session respectively.

ED/CAS Hyderabad Chapter

—by Arif Soheli

The ED/CAS Chapter organized a third membership development workshop on Internet of Things at IEEE Student Branch, Jayamukhi Institute of Technological Sciences, Warangal on February 17 and 18, 2018. The workshop was funded under the CASS outreach program and supported by JITS, Warangal. A very positive outcome of the workshop was that 32 of the 68 participants enrolled as society members to attend this event. The participants represented eight student branches spread across the states of Telangana and Andhra Pradesh and the arrangement of accommodation for 28 outstation participants was done at the Guest house of NIT Warangal.

As the workshop was hands-on, the practical session with nine experiments ranging from preliminary IoT experiment to advanced once like waste management, home automation and toll gate were conducted. The first day of the workshop had an interesting lecture on introduction to IoT by Dr. Arif Soheli, Chair, IEEE CAS/EDS chapter in the morning session and a talk on Energy harvesting for IoT applications in the afternoon session. Five experiments were completed on day one, in which students were introduced to Node MCU board, Blynk mobile app and Thingspeak IoT cloud.

On the second day of the workshop, Mr. Suresh, V.S., Co-founder of Startoon Labs, who had ten plus years of industry experience gave a talk on Industrial applications of IoT in the morning session and Enabling a technology startup in IoT domain in the afternoon session. He gave a first-hand explanation of the gap



Speaker and chapter advisor at the ED NIST Student Branch Chapter technical lecture

between industry and academia and proposed various feasible strategies to fill the same. He also beautifully mapped the engineering curriculum with the various core electronic domains in which plenty of job opportunities exist. The students were highly impressed with the presence of an industry professional amidst them and it resulted in a very fruitful offline discussion. On the experimental side, the students performed waste management using IoT and were able to send out tweets on the Twitter platform when the waste bins are full using ultrasonic sensors

Prof. Rangaiah, an octogenarian and a dedicated IEEE volunteer who is also the Branch Counselor of IEEE Student Branch of JITS, was present during the Valedictory session and gave away the certificates and IoT kits to the participating teams. Mr. A. Chakradhar, Member, IEEE CAS/EDS ExCom and facilitator of the workshop announced that a formal petition to start a CAS chapter in JITS was launched during this workshop, thus achieving its desired outcome of membership development. The participants from eight different colleges presented their feedback in the closing session and expressed keen interest to start IEEE CAS chapter in respective Student branch and requested the IEEE CAS/EDS Chapter to conduct similar programs at their student branches also. Dr. Arif Sohel, expressed his profound thanks to management of JITS for supporting the workshop by hosting and sponsoring the local hospitality.

The IEEE EDS/CAS joint chapter of Hyderabad section organized a panel discussion on career opportunities in Core electronics sector on March 17, 2018 at ECE Department, Osmania. Eminent industry professional with expertise in the areas VLSI Design, IOT, Communications and Embedded Systems were invited as panelists. The event started with Dr. P. Chandrasekhar, Head, ECED, Osmania University giving the welcome address. Dr.



Dr. Arif Sohel delivering his talk on IoT applications



Mr. Suresh VS delivering talk on IoT in Industry



Dr. Arif Sohel giving practical demo of IoT based home automation system

Mohammed Arifuddin Sohel, presenting the activities of IEEE EDS/CAS Chapter and elucidated about the motive of this panel discussion, which is to attempt to bridge the industry academia gap.

The first speaker, Mr. N. Venkatesh, Vice President, Redpine Signals, discussed the interview process of the core electronics companies and the importance of having clarity

of fundamentals. He mentioned that a quick self-learning ability and a proactive attitude are mandatory requirements of core area. He encouraged the students to learn new things every month. To start with the students can take an online course on Python/PYTHON/TCL which are important scripting languages used in the industry.

Mr. Govind Krishnan, Director, Microsemi talked about the growth



(L-R)—Arif Soheli, Jodinder, Venkatesh, Govind Krishnan, Kashyapa Balemarthy, S.V. Rao



Section of audience during the panel discussion

in semiconductor design market which is expected to be 10% per year for next 5 years as predicted by IESA. He mentioned that VLSI Industry can be broadly classified into ASIC and FPGA design, wherein it is a very challenging job to build a ICs with no scope of mistakes. The job requires skills like verilog, VHDL, knowledge of protocols etc. He listed the following skills that the hardware design industry would look for in a potential Electronic engineer—Logic design fundamentals (from reference book-Morris Mano), Scripting languages(Python, TCL, C Shell—any one), C and C++ for verification, Exposure to Hardware so as to translate verilog to hardware, problem solving skills in which the approach of the candidate is monitored and finally application of learning in the form of projects.

Dr. Kashyapa Balemarthy, Scientist, OFS Optics who is a commu-

nication engineering expert gave a powerpoint presentation on the career options after graduation and addressed the big question of choosing between Core and Non-Core jobs. He suggested that one should self-introspect what one wants, is it money, Power, Status, Passion. He listed a few companies that recruit in core electronics area.

Mr. S.V. Rao, Director, AMD who also has a good teaching experience as an engineering faculty highlighted that companies look for people who can identify problems, and also propose solutions.

Mr. Joginder, CEO of Vajra Infratech pvt. Ltd mentioned that in the last decade 9 out of 10 engineers would do IT and settle in US but the times are now changing and outsourcing is not that lucrative business any more. Due to this scenario one should not just look for getting

employed but also to start their own business.

The panel discussion was very well attended by about 150 students from around 8 colleges of which about 70 were IEEE members. The students gave a very good feedback and have recommended that a full day session be conducted in this regard so that they will be better prepared for the future. A very interesting question and answer session followed the panel discussion.

ED/SSCS Bangladesh Chapter, Dhaka, Bangladesh

—by Mahnaz Islam

The ED/SSC Bangladesh Chapter and Department of EEE, BUET jointly organized a workshop on “RF Circuit Design using Computer Simulation Technology (CST)” on January 24, 2018 at the Department of EEE, BUET. The workshop was conducted by Dr. Emran Md Amin, R&D Design Engineer for Radio Frequency Systems, Melbourne, Australia. Total 15 participants with 06 IEEE members participated in the workshop. He introduced one of the most widely used 3D simulator Computer Simulation Technology (CST) for RF circuit design. The primary agenda of this workshop is to familiarize with CST Microwave Studio (MWS) for the 3D EM simulation of high frequency passive components.

The chapter and Department of EEE, BUET jointly organized a workshop on “RTL Verification with System Verilog” on January 25, 2018 at Department of EEE, BUET. The workshop was conducted by Md. Tanvir Hasnain Shovon, Senior Design Engineer, Neural Semiconductor, DBL Group. Total 17 participants with 06 IEEE members attended in the workshop. In this workshop, Md. Tanvir Hasnain Shovon will introduce the concept of Verification with the help of the basic syntax of System Verilog. Further, participants will also gain knowledge about Layered Test



Dr. Emran Md Amin is conducting a workshop on CTS at BUET

bench writing for ALU and receive an overview of Verification plan. The participants will be provided with the presentation slides used in this workshop, along with the source RTL, Test bench, and Verification Textbook.

Executive Committee Meeting of IEEE Electron Devices Society and the IEEE Solid State Circuits Society (ED/SSCS) Bangladesh Chapter was held on March 24, 2018 at the Multipurpose Room of Department of EEE, BUET for the Planning of future activities and events, which include technical talks, workshops and student membership drive, was discussed in the meeting.

ED/AP Bombay Chapter

—by Anil Kottantharayil

The AP/ED Bombay Chapter organized several talks in IIT Bombay during the last quarter and the highlight of these was the mini-colloquium that was held on January 13, 2018. All the talks were attended by students, research staff and faculty of IIT Bombay, students and faculty members from educational institutions in and around Mumbai, and researchers and engineers from several companies in and around Mumbai.

- Prof Shankar Ekanath Madathil, Professor, Electronic and Electric Engineering, University of Sheffield and Rolls-Royce Royal Acad-

emy of Engineering Research Chair gave a talk on “Recent Status in Polarization Super Junction technologies in Gallium Nitride” on January 3, 2018.

- Dr. Sushanta Mitra, Executive Director of the Waterloo Institute for Nanotechnology and a Professor in Mechanical and Mechatronics Engineering at the University of Waterloo delivered a talk titled, “Convergence of Science, Engineering and Technology for Global Challenges” on January 4, 2018.
- DL talk by Prof. Muhammad Mustafa Hussain, Department of Electrical Engineering, King Abdullah University of Science and Technology gave a distinguished lecture on “Electronics for All” on January 5, 2018.
- Prof. Gokul Gopalakrishnan, University of Wisconsin, Platteville gave a talk on “Stiction aided fabrication of Silicon nanomembranes for MEMS applications” on January 8, 2018.
- Dr. Bhaswar Chakrabarti, University of Chicago, delivered a lecture on “Neuromorphic engineering: from devices to circuits for energy-efficient computing and bio-hybrid interfaces” on January 9, 2018.
- DL talk by Prof. Hiroshi Iwai, Tokyo Institute of Technology, Yokohama, Japan, delivered a

distinguished lecture on “Recent progress in semiconductor power devices” on January 12, 2018.

- DL talk by Victor Veliadis, Deputy Executive Director and CTO of Power America and Professor in Electrical and Computer Engineering, North Carolina State University gave a distinguished lecture on “SiC Power Device Processing—An Exercise in Si Fabrication with a High Temperature Twist” on March 07, 2018.

ED Nepal Chapter

—by Bhadra Prasad Pokharel

The ED Nepal Chapter organized a talk program on “*Macaroni fullerene for high energy storage devices.*” on February 27, 2018 in Pulchowk Campus, IOE, Pulchowk which was attended by nearly 25 IEEE members and students. The talk was delivered by Dr. Lok Kumar Shrestha, Senior Researcher, National Institute for Materials Science (NIMS), Namiki, Tsukuba, Japan. He discussed that the fullerene derived from macaroni has very high surface area and high value of supercapacitance. It can be used for high energy storage devices. The fullerene is also used as a sensor for gases as per QCM result. A prospective of research work on this field is emerging in recent years, and is very suitable for Nepalese context. He also stressed on the collaborative research work between IOE and NIMS on this field.

IEEE Sub-Section in association with the ED Nepal Chapter organized a one-day technical workshop “*IEEE Standards on Smart Grid and Cyber Security*” on March 16, 2018 in Pulchowk Campus Institute of Engineering. Total participation in the program were 30, in which 15 were IEEE members and rest were Faculty, engineers and scientists.

Participants were from Government of Nepal, Pulchowk Campus, IOE, Nepal Electricity Authority, Nepal Telecom, Engineering Colleges and different Hydro-power organizations.



Technical workshop organized by ED Nepal Chapter



Parth Darji (Ethos Inc), presenting at ED/SSC Gujarat Chapter event

The program began with a welcome speech of Dr. Arun Timalisina, Sub-Section Chair and chairing the session. First lecture was delivered by Dr. Netra Gywali, from Government of Nepal, on “Power Sector Scenario: Smart Power Grid System in Nepal.” He presented the energy scenario in the present of Nepal. The chief guest and IEEE Distinguished Lecturer, Senior Director of IEEE Standards Association, Dr. Sam Sciacca, delivered an interesting and very informative talk on “IEEE standards on smart grid and cyber security.” During his talk, he explained and provide lot of information on IEEE standards both on smart grid and cyber security. He mainly stressed on i) Smart grid, ii) smart meter, and iii) cyber security. He provided the ideas of the standards IEEE 1547, IEEE 937, 1901, 1703, 1377, etc.

Our next guest Dr. Harish Mysore, Director IEEE India Operations pro-

vided the information of IEEE to all participants and methods of getting membership as well as its member-benefits. The ED Nepal Chapter Chair, Prof. Bhadra Pokharel, also provided the information on IEEE and the IEEE Electron Devices Society, its activities and contributions/benefits to the members in his lecture.

ED/SSC Gujarat Section Chapter

—by Amit Bhatt

On February 22, 2018, the chapter organized a technical talk by Parth Darji (Ethos Inc) on embedding Augmented Reality in a motorcycle helmet, which was attended by over 45 students.

The chapter also organized a workshop on Tips and techniques in Cadence physical design flow at DAI-ICT, Gandhinagar.

ED Heritage Institute of Technology Student Branch Chapter

—by Atanu Kundu

The ED Heritage Institute of Technology Student Branch Chapter organized a 3-day hands-on Autonomous Robotics Workshop “Lord of the Tracks 1.0,” February 20–22, 2018. Ten teams, comprising of 40 students from second year B.Tech. ECE, participated in the workshop. The teams were mentored and guided by 10 student member volunteers, Student Branch Counselor Dr. Mousiki Kar, and ED HIT SBC Advisor Dr. Atanu Kundu. The event was hosted at the IEEE EDS Center of Excellence, Heritage Institute of Technology, Kolkata, India.



Participants and mentors of ‘Lord of the Tracks 1.0’ held February 20–22, 2018



Participants and mentors of 'Lord of the Tracks 2.0' held during March 13–15, 2018

Motivated by the overwhelming response and requests from students, the chapter organized another 3-day hands-on Autonomous Robotics Workshop, "Lord of the Tracks 2.0," March 13–15, 2018. The workshop was proactively executed by 10 student member volunteers, Student Branch Counselor Dr. Mousiki Kar, and ED HIT SBC Advisor Dr. Atanu Kundu. A total of 45 students from 2nd year B.Tech. ECE participated in the workshop hosted at the IEEE EDS Center of Excellence, Heritage Institute of Technology, Kolkata, India.

ED Netaji Subhash Engineering College Student Branch Chapter
—by Ayush Thakur

On March 20, 2018 the chapter in association with the Department of ECE organized a technical lecture on "Electron Devices and Applications" by Dr. Soumya Pandit, Institute of Radio Physics and Electronics under Calcutta University. The lecture dealt with nano scale MOS transistors, with Dr. Pandit addressing various aspects of MOSFETs including the challenges, solutions and approaches. He briefly introduced the short type MOSFET, long type MOSFET, scaling and the challenges involved, leakage current, tunneling, FinFET, UTB-SOI MOSFET. Almost 70 students attended, along with 12 IEEE members, the counselor and the advisor.

ED St. Joseph College of Engineering Student Branch Chapter

—by G. S. Uthayakumar

On January 5, 2018, the chapter organized the IEEE Sponsored National Workshop on RealTime Imaging, Machine Learning & Internet of Things with MATLAB." Lecture and Hands-on sessions for the course handled by M/s. Design Tech & Math Works. On February 16, 2018, the chapter organized a technical lecture on Recent applications of Nano-Bio Devices by Dr. S. Bhagyaraj, Associate Professor, Department of Biomedical Engineering, S.S.N. College of Engineering, Chennai. On March 2–3, 2018, a robotics workshop was organized with Professor P. V. Manivannan, Dept. of Mechanical Engineering, IIT, Madras, as the resource person. On March 23, 2018, a paper presentation on Recent Trends in EDS was coordinated by Dr. S. Aghalya, HOD-Student Affairs, St. Joseph's College of Engineering, Chennai.



Technical lecture, "Electron Devices and Applications," by Dr. Soumya Pandit

~ Manoj Saxena, Editor

EDS MEETINGS CALENDAR



THE COMPLETE EDS CALENDAR CAN BE FOUND AT OUR WEB SITE:

[HTTP://EDS.IEEE.ORG](http://eds.ieee.org). PLEASE VISIT.

<u>2018 International Semiconductor Conference (CAS)</u>	10 Oct - 12 Oct 2018	Rina Sinaia Hotel 8 Carol I Street Sinaia, Romania
<u>2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)</u>	14 Oct - 17 Oct 2018	San Diego, CA, USA
<u>2018 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)</u>	15 Oct - 18 Oct 2018	Hyatt Regency 1333 Bayshore Highway Burlingame, CA, USA
<u>2018 12th International Conference on Advanced Semiconductor Devices and Microsystems (ASDAM)</u>	21 Oct – 24 Oct 2018	Smolenice, Slovakia
<u>2018 Non-Volatile Memory Technology Symposium (NVMTS)</u>	22 Oct – 24 Oct 2018	Sendai, Japan
<u>2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)</u>	31 Oct - 02 Nov 2018	Georgia Tech Hotel and Conference Center Atlanta, GA, USA
<u>2018 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)</u>	05 Nov - 08 Nov 2018	Hilton San Diego Resort and Spa 1775 East Mission Bay Drive San Diego, CA, USA
<u>2018 IEEE International Electron Devices Meeting (IEDM)</u>	29 Nov - 07 Dec 2018	Hilton San Francisco San Francisco, CA, USA
<u>2018 IEEE 49th Semiconductor Interface Specialists Conference (SISC)</u>	05 Dec - 08 Dec 2018	Catamaran Resort Hotel 3999 Mission Boulevard San Diego, CA, USA
<u>2018 International Symposium on Semiconductor Manufacturing (ISSM)</u>	10 Dec – 11 Dec 2018	Tokyo, Japan

<u>2018 4th IEEE International Conference on Emerging Electronics (ICEE)</u>	17 Dec - 19 Dec 2018	Indian Institute of Science Bengaluru Bengaluru, India
<u>2019 Electron Devices Technology and Manufacturing Conference (EDTM)</u>	12 Mar - 15 Mar 2019	Singapore, Singapore
<u>2019 China Semiconductor Technology International Conference (CSTIC)</u>	17 Mar – 18 Mar 2019	Shanghai, China
<u>2019 IEEE International Reliability Physics Symposium (IRPS)</u>	31 Mar - 4 April 2019	Monterey, California, USA
<u>2019 International Siberian Conference on Control and Communications (SIBCON)</u>	18 April - 20 April 2019	Tomsk, Russia
<u>2019 International Vacuum Electronics Conference (IVEC)</u>	28 April - 1 May 2019	Busan, Korea (South)
<u>2019 IEEE 11th International Memory Workshop (IMW)</u>	12 May - 15 May 2019	Monterey, California, USA
<u>2019 IEEE 46th Photovoltaic Specialists Conference (PVSC)</u>	16 Jun - 21 Jun 2019	Chicago, Illinois
<u>2019 20th International Conference on Solid-State Sensors, Actuators and Microsystems & Eurosensors XXXIII (TRANSDUCERS & EUROSENSORS XXXIII)</u>	23 Jun - 27 Jun 2019	Berlin, Germany
<u>2019 IEEE BiCMOS and Compound semiconductor Integrated Circuits and Technology Symposium (BCICTS)</u>	3 Nov – 6 Nov 2019	Nashville, TN USA
<u>2019 IEEE International Electron Devices Meeting (IEDM)</u>	9 Dec – 11 Dec 2019	San Francisco, CA
<u>2019 IEEE 50th Semiconductor Interface Specialists Conference (SISC)</u>	11 Dec – 14 Dec 2019	San Diego, CA



EDS Vision, Mission and Field of Interest Statements

Vision Statement

Promoting excellence in the field of electron devices for the benefit of humanity.

Mission Statement

To foster professional growth of its members by satisfying their needs for easy access to and exchange of technical information, publishing, education, and technical recognition and enhancing public visibility in the field of Electron Devices.

EDS Field of Interest

The EDS field-of-interest includes all electron and ion based devices, in their classical or quantum states, using environments and materials in their lowest to highest conducting phase, in simple or engineered assembly, interacting with and delivering photo-electronic, electro-magnetic, electromechanical, electro-thermal, and bio-electronic signals. The Society sponsors and reports on education, research, development and manufacturing aspects and is involved in science, theory, engineering, experimentation, simulation, modeling, design, fabrication, interconnection, reliability of such devices and their applications.