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Newsletter

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2014 IEEE Symposium on VLSI Technology

HILTON HAWAIIAN VILLAGE, HONOLULU

Rainbow Tower, Hilton Hawaiian Village, Honolulu, Hawaii, USA

The 34th Annual IEEE Symposium on VLSI Technology will be held from June 9–12, 2014, at Hilton Hawaiian Village, Honolulu, Hawaii. This symposium, jointly sponsored by the IEEE Electron Devices Society and the Japan Society of Applied Physics, is the premier international conference on **VLSI semiconductor technology**.

The unique aspect of this conference is that it is held jointly with the Symposium on VLSI Circuits (June 10th–13th) to promote interactions between technologists and circuit/system designers. A single registration fee covers both events, and **special joint focus sessions** will offer unique learning opportunities for both Technology and Circuits attendees on "Design in Scaled Technologies," "Design Enablement," "Memory Technology & Design" and "3D (TSV) & Heterogeneous Integration."

Moreover, the 2014 Symposium on VLSI Technology features **technology focus sessions** on "Non-Volatile Embedded Memory" and "Interconnect: Local & Global," and research results spanning a broad spectrum of VLSI technology topics:

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Your Comments Solicited

Your comments are most welcome. Please write directly to the Editor-in-Chief of the Newsletter at radhakrishnan@ieee.org

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Contributions Welcome

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Newsletter Deadlines

Issue	Due Date
January	October 1st
April	January 1st
July	April 1st
October	July 1st

The EDS Newsletter archive can be found on the Society web site at http://eds.ieee.org/eds-newsletters.html. The archive contains issues from July 1994 to the present.

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Upcoming Technical Meetings

2014 IEEE Compound Semiconductor IC Symposium (CSICS)

We cordially invite you to the 2014 IEEE Compound Semiconductor IC Symposium (CSICS) being held October 19th–22nd at the Hyatt Regency La Jolla at Aventine located in San Diego, California USA. The Symposium has evolved to be the pre-eminent international forum for developments in compound semiconductor circuit and device technology. The scope of the Symposium encompasses devices and circuits, embracing GaAs, SiGe, InP, GaN, InSb and CMOS technology to provide a truly comprehensive conference. CSICS is the ideal forum for presenting the latest results in microwave/mm-wave, high-speed digital, analog, mixed mode, THz, power conversion, and optoelectronic integrated circuits.

The 2014 CSIC Symposium comprises of a full 3-day technical program, two short courses, a primer course, and a technology exhibition. The technical program consists of approximately 60 high quality technical papers. Invited papers and 2–4 panel sessions on topics of current importance to the Compound Semiconductor IC community are key components of the technical program. In addition, the Symposium will continue the tradition of including important "late breaking news" papers. The short courses on Sunday, October 19th provide the attendees the opportunity to learn from world-renowned instructors in their respective areas of expertise. The Sunday introductory-level primer course will provide attendees insight into the design of the principal RF building blocks, namely PAs, LNAs, Mixers and Oscillators, emphasizing the specific background to understand and appreciate the technical program.

The technology exhibition will be held on Monday and Tuesday, featuring informative and interesting displays with corporate representatives on hand. The list of exhibitors can be found in the CSICS advance program to be published in late June. To complement the Symposium, there are several social events including the Sunday Evening CSICS Opening Reception, the Monday CSICS Exhibition Opening Reception, and the Tuesday CSICS Exhibition Luncheon. Breakfasts and coffee breaks will be served on Monday, Tuesday, and Wednesday.

For registration and up-to-date information please visit the CSICS website at www.csics.org. Further questions may be addressed to the Symposium Chair: Douglas S. McPherson, Ph: +1 613-670-3371, Email: dmcphers@ciena.com

Paper Submission Deadline: May 2, 2014

HYATT REGENCY LA JOLLA AT AVENTINE HOTEL

For 2014 IEEE CSICS
Organizing Committee
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2014 CSICS Publicity Chair
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2014 IEEE International Memory Workshop (IMW)

The Sixth IEEE International Memory Workshop will be Held at the Regent Taipei, Taiwan, May 18–21

In response to the growing global interest in memory technologies, the NVSMW—Non Volatile Semiconductor Memory Workshop—and ICMTD—International Conference on Memory Technology and Design—were merged together in 2008 to incorporate the volatile and non-volatile memory aspects in one forum while maintaining the workshop experience. The workshop is sponsored by the IEEE Electron Devices Society and meets annually in May. In 2014, IMW goes back to Asia and will be held in Taipei, Taiwan.

The convergence of consumer, computer and communication electronic systems is leading to an exponential growth in need, mainly for code, computing and data storage. While in the past we could associate a memory technology to a specific market segment (e.g., RAM to computer, NOR Flash to mobile communication, NAND Flash to consumer SSD), today the new electronic systems stack different memory technologies and use microcontroller to facilitate interfacing and managing the overall memory. Moreover, novel memory technologies are entering in the market, providing opportunities for novel applications and challenges for the technology development. The characteristics of these complex memory systems in terms of density, performance, power consumption, packaging and interfacing become of greater interest. The capabilities provided by the new memory technologies, new concepts and material proposed today will drive the definition of these memory systems in the future. The IMW aims to answer this need, extending the scope from non-volatile memory, which had been successfully discussed in more than 30 years of NVSMW's history, to large memory technologies and design, which were the focus of ICMTD, in the view of systems. Innovation is our tradition: IMW widened its focus while maintaining the positive characteristics of a workshop.

IMW is a unique forum for both specialists in all aspects of microelectronic memory and novices wanting to gain a broader understanding of the field. The workshop is usually attended by a wide international community from North America, Europe, Japan and Asian countries. Attendees include industry leaders, researchers in academia and industry as well as end users of memory products. The number of attendees typically exceeds 250 in recent years, reflecting the growing interest in the workshop. Each year we receive over 80 paper submissions and accept about 35 for oral presentation which corresponds to about 40% acceptance rate. Principal topics for discussion are: device physics, silicon processing, product testing, new technologies including new structures and novel approaches, programmable logic, memory cell design, integrated circuits, solid state disks and memory cards, reliability and new applications. Following the tradition established in previous IMW editions, Sunday the 18th of May will be dedicated to a Short Course session. Moreover a poster session for several qualified papers is usually held after the panel discussion.

An important goal of IMW is to provide an informal environment to encourage discussions among participants and lively interactions. There will be morning and afternoon technical sessions, along with a lively evening panel discussion on a hot topic in memory field. Technical interaction among presenters and attendees is encouraged through question and answer sessions and allotting ample time after formal paper presentations for further in-depth discussions. Organized breaks, including snacks and the conference dinner and lunch are provided as opportunities to meet and exchange ideas with colleagues. The morning and afternoon technical sessions are organized in a manner of providing time for the informal exchange and to enjoy the beauty of the Taipei area. The hotel is conveniently situated in Taipei downtown and it is easily accessible from the international airport. Taipei is the gateway to visit Taiwan with high-speed train connections. For more information about the conference, please go and register at the website www.ewh.ieee.org/soc/eds/imw. I look forward to seeing you next May at IMW 2014 in Taipei.

Agostino Pirovano
2014 IMW General Chair
Micron
Agrate Brianza (MB), Italy

2014 IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD)

The International Symposium on Power Semiconductor Devices and ICs (ISPSD) brings together the world's foremost experts on power devices and power integrated circuit technologies and applications. It has become the premier international conference in this field, drawing an annual attendance of about 400 engineers, scientists, students, and professors.

In 2014, ISPSD will return to Hawaii for the first time in nearly 20 years. The conference will be held on the beautiful Big Island of Hawaii, which includes two active volcanoes, beautiful beaches, abundant hiking, snorkeling, and many other outdoor adventures.

ISPSD 2014 will open with an all-day short-course lecture series on June 15th with six exciting topics. This is followed by four full days of technical sessions (June 16th–19th). A total of 110 oral and poster technical papers will be presented. Sessions will run sequentially, with no parallel sessions, enabling participants to listen to, and to ask questions for, every presenter. Frequent breaks will be provided and several social events are planned (including a genuine Hawaiian Luau) to allow conference attendees to network and exchange ideas in an informal setting. In addition, exhibitors' booths will provide an opportunity for participants to learn about the equipment and services of companies that support the power electronics industry.

We have received a significant increase in paper submission this year. The organizing and technical program committees are working hard to ensure that this conference will be a success. The most important factors in that success will be the high-quality technical presentations and the participation of power device enthusiasts from all over the world. Registration is open at www.ispsd.org. Please register early, and help us to make ISPSD 2014 a valuable and memorable experience for all.

Don Disney
2014 ISPSD General Chair
GlobalFoundries
Santa Clara, CA, USA

2014 IEEE Symposium on VLSI Technology

(continued from page 1)

- Logic, Memory, RF, analog, I/O, high-voltage, imaging, MEMS, integrated sensors, and System-on-Chip
- New materials, concepts and breakthroughs in VLSI processes and devices
- Interconnect scaling and Cu alternatives; chip-to-chip interconnects
- Heterogeneous integration of non-Si materials/substrates on Silicon
- Advanced lithography and high-density VLSI patterning technologies
- Beyond-CMOS functional devices
- Packaging technologies, Through-Silicon-Vias and 3D-system integration
- Advanced device analysis, theoretical understanding and modeling; operational fundamentals and reliability of the above devices
- VLSI manufacturing concepts, technologies, and yield optimization

Additional highlights include:

- **Plenary sessions**: *"Storage Architecture for the Data Center in 2020"*, *"Technology Development for Printed LSIs Based on Organic Semiconductors"* (Circuits), and *"Customer Value Creation in the Information Explosion Era"* (Technology)
- **Rump sessions***: "Who Gives Up On Scaling First?"* (Circuits), and *"450mm, EUV, III-V, 3D - All in 7 nm? Are You Serious?!"* (Technology)
- **Full-day short courses** on *"Advanced Data Converter & Mixed-Signal Design"*, *"Advanced Energy-Efficient Digital Design"* (Circuits), and *"High Performance Mobile SoCs enabled by 10 nm SoC Technology"* (Technology)

Two satellite workshops will be held before the conference: *"Silicon Nanoelectronics"* (June 8th–9th) and *"Spintronics"* (June 9th).

We cordially invite you to attend the 2014 Symposium on VLSI Technology. For further information please visit the VLSI Symposia website: http://www.vlsisymposium.org.

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Technical Briefs

Semiconductors and Power Electronics in the 21st Century

Krishna Shenai

The information economy of the 20th century was largely built around the silicon chip technology that revolutionized the computing and communication age. The same can be said about the emerging energy economy of the 21st century where silicon in particular and semiconductors in general, are expected to play a pivotal role in the generation, transmission, distribution, and consumption of electricity. Today, silicon is the "work-horse" for the $250 billion power electronics industry world-wide, and enjoys more than $25 billion annual market with a 30% CAGR. Since power electronics is the key enabler of the 21st century global energy economy, semiconductors are expected to play a pivotal role in shaping the emerging world.

Today, silicon power switching technology is predominantly used for conditioning of the electrical energy at the consumer end. This is largely due to the fact that single-chip silicon power devices are rated below 6.5 kilo volts and 150 amps because of material and packaging limitations. This scenario is expected to change soon as high-voltage power switching devices made from wide bandgap (WBG) semiconductors are slowly entering the commercial market. The WBG semiconductors, including silicon carbide (SiC) and gallium nitride (GaN), offer unprecedented increase in energy efficiency compared to silicon because of their superior electrical and thermal properties. Furthermore, smaller capacitances and higher temperature operation capability of WBG power switching devices lead to dramatic miniaturization of power electronic systems—a key economic driver. Single-chip WBG power switching devices capable of blocking more than 25 kilo volts will be commercially available in the near future. The high-voltage power switching characteristics of WBG semiconductors has the potential for transformative impact on the electricity transmission and distribution (T&D) infrastructure. For example, compact and efficient solid-state transformers may soon replace the humongous magnetic power transformers in today's electricity infrastructure, and the realization of flexible AC transmission and distribution (FACTS) concept may render the conventional AC electricity grid more robust and resilient to load variations.

Perhaps the greatest challenge of the 21st century energy economy pertains to low-cost and efficient electricity generation and utilization from clean distributed renewable energy generators (DREGs). Much of the United States has a mandate to generate least 25% electricity from green resources by 2025. Solar, wind and clean gas are touted to be the prime sources of clean energy. At the dawn of the 20th century, it is becoming apparent that solar cells made from silicon and compound semiconductors could produce much of the electricity generated from the sun. Many experts believe that solar photovoltaics (PV) may become the dominant source for renewable clean electricity generation in the near term. At the same time, semiconductors are also gaining popularity for harnessing electricity for ultra-low power electronics applications including portable wireless devices. The main challenge then comes down to efficient integration and utilization of electricity produced from renewable means. One approach is to feed back the electricity produced from the DREGs to the main utility AC grid; this would require solid-state power inverters. A more attractive and cost-effective alternative is to directly utilize the DC electricity produced from the DREGs since a majority of house-hold electrical loads are DC-powered. This is particularly interesting for the lighting application since it is slated to migrate from incandescent bulbs to solid-state technology within the next decade. One can envision a complete electrical system—from the source to the load—all built from semiconductors, as it would be the case for solar-powered light emitting diodes (LEDs). Solar-powered data centers are already being built. The opportunities are numerous for integrating renewable energy means in order to improve the standard of living of billions of people around the world, and especially those living in the developing and under-developed parts of the globe.

The potential impact of power electronics is even more dramatic on the environment. The ability to freely access fresh water and clean air may dictate the human endeavors in the 21st century. The growing concerns of global warming and ever increased consciousness for increased air and water pollution are demanding rapid electrification of the transportation industry. Power electronics

is the key enabler of hybrid and all-electric vehicles, from automobiles to ships and airplanes. Soon we may see gasoline charging stations replaced with battery charging stations, and the high-ways embedded with wireless battery chargers. The continuous infusion of power, computing, communication and sensing electronics is accelerating the development and deployment of intelligent systems in all walks of human life including transportation, housing and manufacturing.

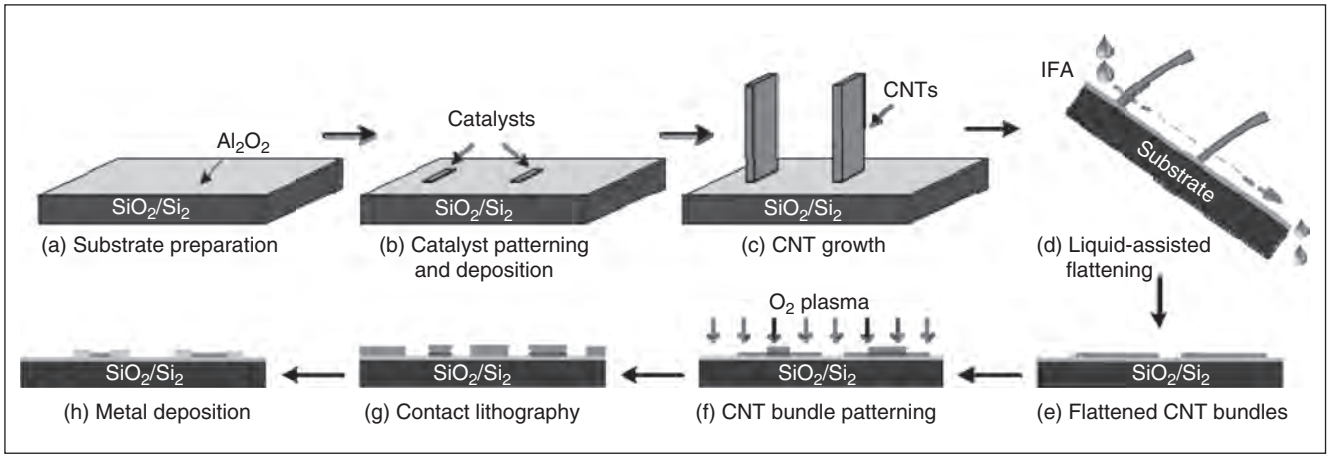
The demands of the 21st century energy- and environment-conscious society open new opportunities and challenges for power semiconductors and power electronics. The focus of electronics system design is already shifting from an all-performance-driven approach to a more energy-driven methodology. The semiconductor manufacturing is likewise drifting from traditional signal- and communication-driven to more power-switching and power-management centric. This is an exciting time for our society as we are destined to be the key benefactors of the emerging energy economy.

Krishna Shenai (F'01) *earned his Ph.D. degree in electrical engineering from Stanford University in 1986. He is employed as a Principal Electrical Engineer within the Energy Systems Division at Argonne National Laboratory in Chicago, Illinois. He is a Senior Fellow at the Northwestern-Argonne Institute of Science and Engineering (NAISE) at Northwestern University, Evanston, Illinois and a Senior Fellow at the Computation Institute at the University of Chicago, Chicago, Illinois. Dr. Shenai is an Editor of IEEE Journal of the Electron Devices Society and is a member of EDS Technical Committees on Power Devices and Semiconductor Manufacturing.*

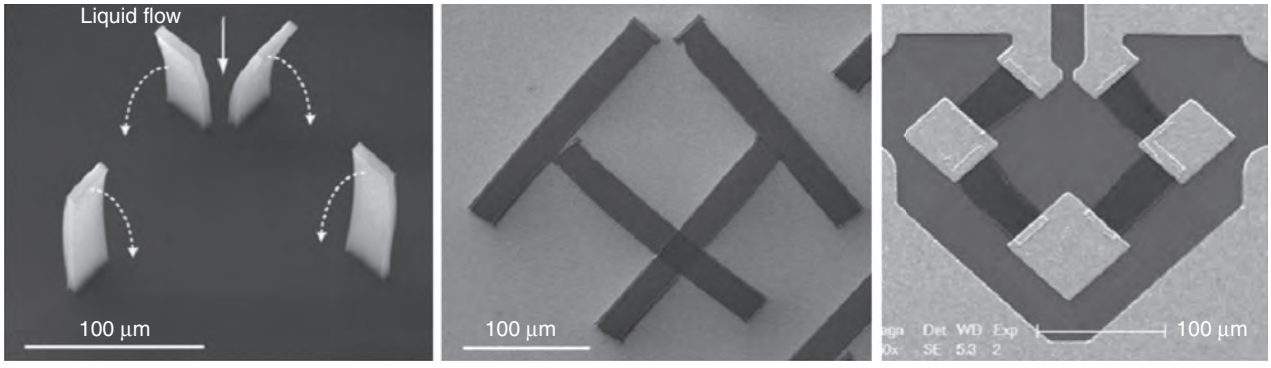
UCSB Researchers Take Carbon Nanotube Interconnects Closer to Reality

The semiconductor industry has been confronting an acute problem in the interconnect area. As IC feature sizes are scaled below 14 nm, copper wires exhibit significant "size effects" resulting in a sharp rise in their resistivity. This has adverse impact on IC performance and reliability in the form of higher communication costs due to increased interconnect delays and chip-level power dissipation, as well as due to reduced current carrying capacity of the copper wires. Carbon nanotubes (CNTs) have very high current carrying capability (at least two orders of magnitude higher than that of copper), long mean free path (on the order of μm), and high thermal conductivities (several times higher than that of copper), indicating that CNTs could be potentially employed as alternative materials for next-generation nanoscale interconnects. Such interconnects can enhance the electrical performance as well as eliminate reliability concerns that plague nanoscale copper interconnects.

However, fabrication and characterization of long and horizontal CNT-bundles necessary for interconnect applications have remained an enigma. In a game-changing development, researchers at UCSB led by Prof. Kaustav Banerjee in collaboration with Dr. Alan Cassell at NASA Ames and Prof. Franz Kreupl



(a–h) Fabrication process flow of horizontal CNT-bundle interconnects.



(a) Placement of vertical CNT-bundles for constructing Manhattan structures with liquid flow along the directions indicated by the solid yellow arrow. Broken yellow arrows indicate the orientation of flattening. (b) 2-D Manhattan structure obtained after flattening of the four vertical CNT-bundles in (a). (c) Spiral inductor formed with metal contacts based on the Manhattan structure in (b).

at TU-Munich have demonstrated a novel process that, for the first time, enables fabrication of high-density, long (over 100 microns) and thick (up to microns) horizontally aligned CNT interconnects. This demonstration has thus overcome one of the biggest challenges facing the CNT interconnect technology and is a vital step for implementation of CNT based interconnects and passive devices in next-generation VLSI. The developed process not only yields horizontal CNT interconnects with the lowest reported resistivity, but also enables the first ever fabrication of a CNT based on-chip spiral inductor. These results have been recently published in Electron Devices Society's flagship journal IEEE Transactions on Electron Devices by Hong Li et al., [1],[2].

Link to Articles

[1] H. Li, W. Liu, A. M. Cassell, F. Kreupl and K. Banerjee, "Low-Resistivity Long-Length Horizontal Carbon Nanotube Bundles for Interconnect Applications—Part I: Process Development," *IEEE Transactions on Electron Devices*, Vol. 60, No. 9, pp. 2862–2869, 2013.

[2] H. Li, W. Liu, A. M. Cassell, F. Kreupl and K. Banerjee, "Low-Resistivity Long-Length Horizontal Carbon Nanotube Bundles for Interconnect Applications—Part II: Characterization," *IEEE Transactions on Electron Devices*, Vol. 60, No. 9, pp. 2870–2876, 2013.

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2013 IEEE International Electron Devices Meeting—Summary

Some 1,400 of the world's leading scientists and engineers in semiconductor and related technologies attended EDS's premier annual technical conference last December in Washington, D.C., the 59th edition of the IEEE International Electron Devices Meeting.

Among the most noteworthy technologies discussed in more than 220 presentations given over five days of tutorial, short course and technical sessions were the following:

- FinFETs and fully depleted silicon-on-insulator (FD-SOI) devices, and which type of device represents the optimum approach for continued scaling
- non-silicon devices such as tunneling FETs (TFETs), which hold promise as a way to control transistor off-state leakage by getting around the sub-60 mV/decade steep substhreshold slope barrier
- various non-volatile memory technologies such as resistive memories (ReRAM or RRAM), which are attracting interest because of their potential to deliver faster write times and greater endurance than flash
- biomedical electronics, which are attracting widespread interest

because of the potential for low-cost DNA-sequencing on a chip

In keeping with the spread of electronics to an increasing variety of applications, the 2013 IEDM offered attendees special focus sessions in the areas of BioMEMS, analog device and circuits, and advanced manufacturing technology.

In addition, the IEDM conference again offered 90-minute Saturday tutorial sessions on emerging topics. These are separate from the day-long short courses which delve more deeply into topics. Interest in the tutorials has grown very strongly, and 416 registrants attended tutorials in 2013 on atomic-scale modeling and simulation for nanoelectronics; interface properties for SiC and GaN MOS devices; low-dimensional systems for device applications in nanoelectronics; TFETs; 3D chip-stacking; and energy-harvesting for self-powered electronic systems.

Technical highlights from IEDM 2013 include:

FinFETs and FD-SOI

To scale down below the 20 nm node, leading-edge semiconductor manufacturers are looking at FinFETs and FD-SOI devices.

Taiwan Semiconductor Manufacturing Co. (TSMC) gave details about its upcoming 16 nm FinFET technology, which includes a 0.07 um^2 SRAM, copper/low-k interconnects, high-k/metal-gate and other features for mobile system-on-a-chip (SoC) applications. The transistors achieved a short channel control with DIBL of <30 mV/V and a Id_{sat} of 520/525 uA/um at 0.75V and I_{off} of 30 pA/um for NMOS and PMOS.

Meanwhile, FD-SOI papers discussed results that included high performance, low leakage, ultra-low power, and excellent variability, reliability and scalability down to the 10 nm node (by means of thin SOI and thin BOX substrates). Performance boosters using high mobility materials such as thin strain Si, Ge, and III-V on-Insulator were also presented.

TFETs

TFETs use the quantum mechanical tunneling of electrons through an ultrathin energy barrier to provide high current at low voltage. They potentially could be used in applications where both high speed and low power are needed, such as smart sensor networks, implantable medical electronics and ultra-mobile computing. Interest in them is growing strongly—the devices were the subject of an IEDM Saturday tutorial session, a Sunday Short Course module, were part of an Evening Panel Session on emerging materials and device concepts, and were the subject of numerous papers.

One noteworthy paper was from Penn State University. It described a TFET geared for medical devices that could be implanted inside the human body. For implanted devices, generating too much power and heat can damage tissue, and draining the battery frequently would require frequent replacement surgery.

ReRAM

Many ReRAM papers were presented at the IEDM. A noteworthy paper from IMEC described a conductive bridging RAM (CBRAM) technology. It relies on the fact some amorphous materials with relatively large amounts of metal can behave as solid electrolytes. Under a voltage bias, metal ions can form a conductive filament, and the process can be reversed as needed, enabling the reading and writing of data. IMEC researchers described a 3D imaging approach that enabled them to "see" filament formation, a necessary step to optimizing it.

Bio-medical Electronics

Noteworthy biomedical electronics papers described novel ways to accomplish low-cost DNA-sequencing on a chip. Hitachi researchers described a way to identify the nucleotides making up the DNA molecule by means of a side-gated ultrathin FET containing a nanopore through which DNA strands pass. Channel current is modulated by the electrical charges each DNA nucleotide produces as it passes through the nanopore. A Kookmin University paper described a hybrid biosensor which, for the first time, integrates silicon nanowires and CMOS devices for DNA detection. It demonstrated extremely impressive and consistent sensitivity, expressed as a change in output voltage of 1.2 V per 0.4 change in pH level, and as a 1.2 V change per 200 fM of DNA. A paper by IBM described a CMOS-compatible, 200-mm wafer-scale sub-20-nm nanochannel fabrication method that enables stretching, translocation and real-time fluorescence microscopy imaging of single DNA molecules.

Plenary Talks

As the conference began, three plenary speakers delivered thought-provoking views of future trends. Andrea C. Ferrari from the University of Cambridge spoke on, *Graphene: Future Emerging Technology.* He presented an unbiased story depicting the challenges and opportunities in graphene to be the disruptive device technology of the 21st century.

Meanwhile, a talk by Mitsumasa Koyanagi from Tohoku University on the topic, *Heterogeneous 3D Integration: Technology Enabler Towards Future Super-Chips,* delved into the details of realizing the Super Chip of the future, which will include heterogenous integration of compound semiconductor devices, photonic devices and spintronic devices using 3D integration.

Finally, Geoffrey Yeap of Qualcomm delivered an address titled, *Smart Mobile SoC Driving the Semiconductor Industry: Technology Trend, Challenges and Opportunities.* He highlighted the explosive growth in demand for smart mobile devices in the last decade, and described a judicious strategy of selecting technology nodes, transistor architectures, embedded memory type and

backend design rules to address the power, performance and cost requirement of future mobile SoCs.

Luncheon Speaker

The IEDM luncheon address was given by Eric Enderton of Nvidia Corp., on the topic *Graphics and GPU Computing: Past, Present and Future*. He described the development and growth of graphic processing unit-based (GPU-based) computing, with regard to both supercomputing and the evolution of fixed-function graphics pipelines. He gave an overview of architectural differences between GPUs and CPUs, discussed the evolution of graphics into a general-purpose computational problem, and argued that GPU-based computing because of its inherent parallelism is a better way to address many of today's computing needs than are more traditional single- or few-threaded CPUs.

Entrepreneur's Lunch

Based on the success of the initial Entrepreneur's Lunch at IEDM 2012 in San Francisco, the IEDM conference and EDS Women in Engineering again co-sponsored the event in 2013. The event was moderated by Thuy Dao from Freescale Semiconductor, Chair of EDS Women in Engineering.

The speaker was Steve Nasiri, angel investor and mentor at Nasiri Ventures LLC. For 35 years Nasiri has been a serial Silicon Valley entrepreneur, most recently with InvenSense, which he founded in 2003 and where he served as President, CEO and Chairman until October, 2012, having taken the company public the prior year. Under Nasiri, the company pioneered and became the global market leader in motion-processing solutions for motion-based consumer electronics user interfaces.

Nasiri gave a brief talk on how he came to be an entrepreneur and described some of the main challenges. The remainder of the event was a Q&A session in which he answered numerous questions, ranging from how to approach a venture capitalist to the optimum make-up of a start-up's executive team.

Short Courses and Evening Panels

All-day Sunday short courses and Tuesday evening panel sessions are among the most, well-attended events during any IEDM conference.

IEDM 2013 featured two short courses which ran in parallel: *Challenges of 10 nm and 7 nm CMOS Technologies*, organized by Aaron Thean from IMEC, and *Beyond CMOS: Emerging Materials and Devices*, organized by Thomas N. Theis of Semiconductor Research Corporation.

The evening panel sessions, designed to foster discussion and debate on important technical and industry issues, were *Will Voltage Scaling in CMOS Technology Continue Beyond the 14 nm Generation?,* moderated by Kevin Zhang of Intel Corporation, and *Is There Life Beyond Conventional CMOS?* moderated by Jeff Welser of IBM.

Ken Rim
2013 IEDM Publicity Chair
Qualcomm Inc.
San Diego, CA, USA

Suman Datta
2013 IEDM Publicity Vice-Chair
Penn State University
University Park, PA, USA

2014 IEEE IRPS—Technical Program Highlights

June 1–5, 2014 • Hilton Waikoloa Village • Waikoloa, HI, USA

The International Reliability Physics Symposium (IRPS) is the world's premier forum for leading-edge research addressing developments in the Reliability Physics of devices, materials, circuits, and products. IRPS is the conference where emerging Reliability Physics challenges and possible solutions to achieve realistic End-of-Life projections are first discussed. This year, the IRPS will be held at Hilton Waikoloa Village, Waikoloa, Hawaii, U.S.A. Scheduled for June 1-5, 2014, the IRPS will commence with two full days of tutorials on June 1 and 2.

HIGHLIGHTS OF THE TECHNICAL PROGRAM

The IRPS 2014 Technical Program will consist of 118 platform presentations and 97 poster presentations. This year's symposium will provide a comprehensive look into the current research activities and thinking in semiconductor reliability and physics of failure. Some highlights of the technical program include:

- **BTI and HCI** – Several presentations will address advances in bias-temperature-instability (BTI) and hot-carrier injection damage (HCI). Models for BTI have grown increasingly sophisticated and are now developed to account for the AC duty cycle dependence, although number of aspects remain the topic of lively controversy. The statistics of BTI in very small area transistors is drawing increased attention. Hot carrier damage has also seen increased

interest. Both BTI and HCI are now the topics of new research on FETs fabricated with alternative materials such as III-Vs and Ge, which are being explored as potential Silicon replacements.

- **BEOL Reliability** – Back end of line (BEOL) reliability includes the metallization and low-k dielectrics. As dimensional scaling continues to outpace voltage reduction, this increases the demands on the BEOL to carry higher current densities and support higher electric fields. Several papers highlight both process and design sensitivities for electromigration, stress migration, and low-k dielectric breakdown mechanisms. More accurate and sophisticated reliability models for these mechanisms to allow products to push the technology to the fullest advantage in performance while reducing chip area are presented in these sessions.
- **Soft Error** – Emerging soft error effects, including muon-induced SRAM soft errors, thermal neutron-induced SRAM soft errors in a high-k/metal gate technology, neutron-induced soft errors in multi-level NOR FLASH and heavy ion-induced soft errors in Phase Change Memory are being presented. Several papers on mitigation methods including new flip-flop designs, a well doping approach, a novel transistor design, and application of body-bias will be presented. Characterization and simulation of soft errors in SRAM, flip-flops and logic gates is also addressed.
- **Compound Devices** –This session attracted record submission for 2014, with the reliability of GaN power devices emerging as the key topic. The strong interest in this particular area is driven by the fact that almost all of the large silicon companies today have active programs in GaN power electronics. Several GaN topics will be extensively covered, including physical origin of traps, buffer or barrier, trapping effects on device reliability, such as those causing voltage instabilities and current collapse in D and E-Mode GaN devices, stress methodologies on these devices like hot-cold switching or short-long switching.

TUTORIALS: IRPS 2014 will have four tutorial tracks:

- FEOL/transistor reliability
- MOL/BEOL reliability, including 3D, chip package interaction, ESD and latch-up
- Circuit and component reliability simulation, modeling and statistical techniques
- Systems reliability, including consumer, automotive, avionics and network applications

YEAR IN REVIEW: An afternoon presentation by industry experts on recent advances in key areas of device reliability physics where three areas will be highlighted: reliability of various memory technologies, circuit aging and FinFET reliability.

WORKSHOPS and PANEL DISCUSSION: There will be six workshops covering transistor reliability, NVM (NAND and ReRAM), soft errors, BEOL, circuit reliability and GaN power device reliability. The topic of the panel discussion is "Design for Variability, New Materials, 3D Structures: What role will these techniques play in addressing the reliability of future scaling?"

For more information, visit **www.irps.org**

Chris Henderson
2014 IRPS Technical Program Chair
Semitracks

Chris Connor
2014 IRSP Technical Program
Vice-Chair
Intel

Prasad Chaparala
2014 IRPS General Chair
Alta Devices

Society News

Message from Editor-in Chief

M.K. Radhakrishnan

Dear Readers,

In line with our Society's mission statement—to foster professional growth of its members and to enhance visibility in the field—we are initiating new sections and columns in our Newsletter. With this April issue of the Newsletter we are introducing one new Section "Technical Briefs". With the help of the Editorial teams of TED and EDL as well as our own Editorial team, it is envisaged to grow as a strong section in the Newsletter to disseminate condensed versions of latest research trends in the device area and a platform to discuss future trends. In the current issue we have three feature articles—*IEDM briefs, recent trends in carbon nanotube interconnects, and semiconductors and power electronics in 21st century*.

We have introduced a new Column from this issue "for Young Professionals". This column aims at our new and young members to provide some guidelines and useful stories and to hear their views. A very interesting article on *working successfully in semiconductor industry* by Doug Verret based on his earlier Webinar is included. Further, we are now starting to publish brief answers to the Quest EDS, which will be of immense use to the readers.

Again, the aim is to make the Newsletter a more useful magazine for our Society members. I request all Chapters to provide reports of their social and humanitarian activities also. We may see such news in future issues, and through which Chapters start to know each other better.

However, the success of all these reposes on the feedback and input from our readers. As such, on behalf of the Editorial team and staff, I request your feedback and suggestions. You may note that an exclusive e-mail id is also provided for feedback and suggestions.

Please use: edsnewsletter@ieee.org

M.K. Radhakrishnan
Editor-in Chief, EDS Newsletter
NanoRel, Bangalore, India
e-mail: radhakrishnan@ieee.org

December 2013 EDS Board of Governors (BoG) Meetings

Fernando Guarin
EDS Secretary

The 2013 December EDS Board of Governors (BoG) meeting series was held in conjunction with the 2013 IEEE International Electron Devices Meeting (IEDM) in Washington, DC.

As reported in the January edition of the Newsletter, the 2014 society elections were held. The following members were elected to key positions:

- Members at Large: Arturo Escobosa, Ru Huang, Leda Lunardi, Mikael Ostling, MK Radhakrishnan, Jacobus Swart, and Xing Zhou.
- Secretary: Fernando Guarin
- Treasurer: Ravi Todi
- President-Elect: Samar Saha

In addition, important Constitution and Bylaws changes were approved at the meeting. These changes will provide better consistency, transparency, and flexibility into EDS's structure and operations. A separate article will follow this report, detailing the recently approved changes. The updated EDS Constitution and Bylaws will also be posted in the News and Announcements section of the EDS website.

Several other important motions were passed, as summarized below:

- Approved the proposed list of 2014 committee appointments.
- Approved Singapore as the 2015 mid-year meeting location.
- Approved the proposed list of 2014 Vice Presidents.
- Approved the list of 2015 repeat conferences.

EDS is blessed with a diverse and engaged volunteer corps representing all the world's regions. The December BoG meeting was especially lively, with over 20 volunteers presenting and more than 70 attendees in total. We offer our sincere thanks to you all. It was an outstanding gathering which served to finalize the society's work for 2013 and provided a framework and inspiration for our 2014 initiatives.

Motions

President's Report

1. To approve the proposed list of 2014 committee appointments. **Motion passed unanimously.**

ExCom Update

2. To approve Singapore as the 2015 mid-year meeting location. **Motion passed unanimously.**
3. To approve the proposed list of 2014 Vice Presidents. **Motion passed unanimously.**

Secretary's Report

4. To approve the June 2013 BoG meeting minutes. **Motion passed unanimously.**

Meetings and Conferences Report

5. To approve the list of 2015 repeat conferences. **Motion passed unanimously**.
6. To approve the Constitution and Bylaws amendments from the working group headed by S. Deleonibus. Motion passed, though additional changes may be brought forward at the June meeting with respect to the clauses on amending the Constitution and Bylaws. The EDS Secretary will oversee this effort.
7. To adjourn the meeting. **Motion passed unanimously**.

Fernando Guarin
EDS Secretary
IBM Microelectronics
Hopewell Junction, NY, USA

Announcement of Newly Elected Officers and BoG Members

The EDS officers and Board of Governors members-at-large elections were held on December 8, 2013 in Washington, DC. All voting members were present at this important event. I am pleased to present the results of this election and short bios of the upcoming team that will lead EDS in years to come.

OFFICERS

The following volunteers were elected as Officers beginning 1/1/2014:

President-Elect

Samar Saha received the Ph.D. in Physics from Gauhati University and MS in Engineering Management from Stanford University. Currently, he is a Technical Advisor at Ultrasolar Technology, Santa Clara and an Adjunct Professor in the Electrical Engineering (EE) Department at Santa Clara University. He has worked in various positions for National Semiconductor, LSI Logic, Texas Instruments, Philips Semiconductors, Silicon Storage Technology, Synopsys, DSM Solutions, Silterra, and SuVolta. He has also worked as a faculty member in the EE departments at Southern Illinois University, Carbondale; Auburn University; University of Nevada; Las Vegas; and the University of Colorado; Colorado Springs.

Samar is an elected member of the EDS BoG; Editor-In-Chief, Quest-EDS; and a member, IEEE TAB Periodicals Committee. His past IEEE services include Vice President, EDS Publications; Regions 5 & 6 Editor, EDS Newsletter; member, IEEE Conference Publications Committee; Chair, EDS Compact Modeling Committee; Chair, EDS SRC-NAW; guest editor, three Special Issues of IEEE T-ED; and Chair of the ED Santa Clara Valley Chapter.

Secretary

Fernando Guarin is a Senior Engineer/Scientist at the IBM Microelectronics Semiconductor Research Development Center SRDC in East Fishkill, New York and an Adjunct Lecturer at SUNY New Paltz. He received his BSEE from the "Pontificia Universidad Javeriana", in Bogotá, Colombia, the M.S.E.E. degree from the University of Arizona, and the Ph.D. in Electrical Engineering from Columbia University, New York. He has been actively working in microelectronic reliability for over 30 years.

From 1980 until 1988 he was a member of the Military and Aerospace Operations division of National Semiconductor Corporation. In 1988 he joined the IBM microelectronics division where he has worked in the reliability physics and modeling of Advanced Bipolar, CMOS and Silicon Germanium BiCMOS technologies. He is currently leading IBM's 14 nm technology qualification. Dr. Guarín is an IEEE Fellow, Distinguished Lecturer for the IEEE Electron Devices Society, a member of the IEEE's EDS Board of Governors and Education Committees.

Treasurer

Ravi Todi received his M.S. degree in Electrical and Mechanical Engineering from University of Central Florida in 2004 and 2005 respectively, and his doctoral degree in Electrical Engineering in 2007. His graduate

research work was focused on gate stack engineering, with emphasis on binary metal alloys as gate electrode and on high mobility Ge channel devices. In 2007 he started working as Advisory Engineer/Scientist at Semiconductor Research and Development Center at IBM Microelectronics Division focusing on high performance eDRAM integration on 45 nm SOI logic platform. Starting in 2010 Ravi was appointed the lead Engineer for 22 nm SOI eDRAM development. For his many contributions to the success of eDRAM program at IBM, Ravi was awarded IBM's Outstanding Technical Achievement Award in 2011. Ravi joined Qualcomm as Staff Engineer responsible for 20 nm and 16/14 nm product developments. Ravi had authored or co-authored over 50 publications, has 5 issues US patents and over 20 pending disclosures.

BOG MEMBERS-AT-LARGE

A total of seven members were elected for a three-year term (2014-2016). Four of the seven electees are serving a second term, while the other three have joined the board for the first time. The backgrounds of the electees span a wide range of professional and technical interests. The following are the results of the election and brief biographies of the individuals elected.

Second Term Electees

Arturo Escobosa received a degree in Communications and Electronics Engineering from the National Polytechnic Institute, Mexico, and a Masters diploma in Electrical Engineering from Cinvestav, Mexico. He was granted a Ph.D. degree from the Aachen Technical University, Germany in 1983, due to his work at the Institute of Semiconductor Electronics, in the field of ohmic contacts on GaAs MOCVD epitaxial layers. Since 1983, he has been working as full professor at the Solid State Electronics Group of the Electrical Engineering Department of Cinvestav, México. His research interests include MOCVD Epitaxial Growth of III–V Compounds, Optical Characterization of Semiconductors and X-Ray diffraction for Crystal Characterization. He is Region 9 EDS SRC Vice-Chair since 2012.

Mikael Östling received his MSc and the Ph.D. degrees from Uppsala University, Sweden. He holds a position as professor in solid state electronics at KTH, Royal Institute of Technology in Stockholm, Sweden. He is currently department head of Integrated Devices and Circuits and was the dean of the School of Information and Communication Technology, KTH, between 2004 and 2012. Östling was a senior visiting Fulbright Scholar at Stanford University, and a visiting professor with the University of Florida, Gainesville. In 2005 he co-founded the company TranSiC, acquired in full by Fairchild Semiconductor 2011. He was awarded the first ERC grant for advanced investigators. His research interests are nanoscaled Si and Ge device technologies and emerging 2D materials, as well as device technology for wide bandgap semiconductors for high power / high temperature applications. He has supervised 32 PhD theses work and co-authored about 500 scientific papers published in international journals and conferences. Mikael Östling is an editor of the IEEE Electron Device Letters and a Fellow of the IEEE.

MK Radhakrishnan received M.Sc in Solid State electronics from Sardar Patel University in 1975 and Ph.D from Cochin University in 1981. Currently he is Director of NanoRel Technical Consultants Singapore. During the past 30 years he worked with ST Microelectronics, Philips, ISRO, Institute of Microelectronics and National University of Singapore. He was Technical Chair IEEE IPFA 1995–97, IPFA General Chair 1999, IEEE IEDST General Chair 2009 and Chairman IEEE Rel/CPMT/ED Singapore Chapter 2000-01. He is an EDS Distinguished Lecturer, *Editor-in Chief of EDS Newsletter,* SRC Vice-Chair from Region10 and Member of EDS Technical Committee on Electronic Materials. Radhakrishnan provides technical training in device analysis area to practicing engineers for more than two decades and doing research in the area of physical failures in devices including gate dielectrics. He is a Senior Member IEEE, Fellow IETE, Member ESD Association and Member EDFAS.

Xing Zhou received the B.E. from Tsinghua University, in 1983; M.S. and Ph.D. degrees in electrical engineering from the University of Rochester, in 1987 and 1990, respectively. He is currently a tenured faculty in the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore. His past research interests include Monte Carlo simulation of photocarrier transport and ultrafast phenomena as well as mixed-mode circuit simulation and CAD tool development. His recent research mainly focuses on nanoscale CMOS compact modeling. He has more than 120 referred journal/conference publications, and given more than 100 distinguished lectures and invited talks at various industrial and academic institutions.

He is the founding chair for the Workshop on Compact Modeling in association with the Nanotech Conference since 2002. Dr. Zhou is an elected Member-at-Large of the EDS Board of Governors and Vice President of Regions/Chapters. He has been an EDS Distinguished Lecturer since 2000 and Editor for the Electron Device Letters since 2007.

FIRST-TIME ELECTEES

Ru Huang is currently the Professor, Director of Institute of Microelectronics and Deputy Dean of School of EECS, Peking University, China. Her research interests include nano-scaled CMOS devices, nonvolatile memory devices and device reliability/variability analysis. Since 2000, she has been a leader of several State Key Research Projects in China. She has authored or coauthored four books and more than 250 papers, including more than 50 IEDM/VLSI and EDL/T-ED papers. She is the holder of more than 100 granted patents. She was the winner of Chang-Jiang Scholar Distinguished Professor, National Science Fund for Distinguished Young Scholars and many other awards in China, including National Award for Technological Invention. She is an Associate Editor-in-Chief of "Science in China" and an editor of IEEE T-ED. She was the General Co-Chair of 2012 ICSICT, 2013 ISLPED, TPC Co-chair of 2004 and 2008 ICSICT and committee members of many other international conferences and symposiums.

Leda Lunardi has been a professor since 2003 in Electrical and Computer Engineering Department at North Carolina State University in Raleigh, North Carolina. She received the Ph.D. degree in electrical engineering from Cornell University, Ithaca, New York. After graduation she worked for AT&T Bell Labs starting in Murray Hill, New Jersey and then AT&T Labs Research after the trivesture. She was with JDS Uniphase as a group leader and senior scientist before joining academia.

From 2005 to 2007 she served as program director for the electrical, communications and cyber systems (ECCS) division in the engineering directorate of the National Science Foundation (NSF) in Arlington, Virgina. Under her direction, she started the hybrid communication systems program sponsoring research in free space optics, terahertz components, RF and microwave devices and subsystems.

Her research is on traditional electronic and photonics devices and their applications on energy scavenging, or high speed integration. She has been devoted to increase the number of women and underrepresented minorities in engineering and science careers. Presently she is the principal investigator of the NSF sponsored undergraduate REU-Site: Engineering the Grid, related to energy research.

For over two decades she has been a technical volunteer serving as member or chair on several IEEE executive and technical committee conferences, as well as national and international governments' ad-hoc committees for grants and projects reviews. Some of her present professional activities include member of the editorial board for IEEE Proceedings, editor for the IEEE Transactions of Electron Devices (Optoelectronics Devices), and treasurer for the IEEE Photonics Society Eastern Carolina Chapter.

At NC State, she was director of graduate programs of the ECE Department in 2007, one of the largest programs in the Southeast. From 2008–2011, she was in the leadership team of the NSF-ERC Future Renewable Electric Energy Delivery and Management (FREEDM) Systems Center, as the education program director. She has served and chaired on several department, college and university committees. As Faculty Senate member, she is committed to represent her fellow faculty members.

Jacobus Swart received B. Engineer and Dr. Engineer Degrees in 1975 and 1981 respectively, from the Polytechnic School of the University of São Paulo, Brazil. Afterwards he worked at the following institutions: K. U. Leuven, Belgium, 1982–83, as a pos-doc.; CTI, Campinas, 1984, as head of Process Engineering; LSI-University of São Paulo, 1985-88, as Assistant Professor; SID Microeletrônica, 1986; RTI, USA, 1991, as a Visiting Scientist; and UNICAMP, since 1988, as Full Professor. He served as director of the Center for Semiconductor Components, 1998–2005 and as Director of CTI, 2007–2011. He is currently IMEC representative in Brazil. He is ranked as fellow researcher, level 1A (highest), at CNPq and is a Fellow of IEEE and of the São Paulo State Academy of Science. He is currently the leader of a large research network in Brazil, called NAMITEC.

I welcome all electees and urge them to truly get engaged in the affairs of the Electron Devices Society. EDS is considered to be a volunteer-led, volunteer-driven organization and we expect nothing less from all to continue this tradition.

Renuka Jindal
EDS Nominations and Elections Chair
University of Louisiana at Lafayette
Lafayette, LA, USA

Summary of Changes to the EDS Constitution and Bylaws

As reported in the January issue of the Newsletter, on December 8, 2013, the EDS Board of Governors (BoG) approved changes to the EDS Constitution and Bylaws. These amendments were then approved in February, 2014 by the Chair of the IEEE Technical Activities Board (TAB). The changes will take effect 30 days following their publication in this copy of the Newsletter (distributed to all EDS members), unless objections are received from at least 5% of the EDS membership. The following is a high-level summary of the changes:

Constitution

Article V. Sections 1–7: The changes here create the EDS Forum, separate from the BoG. Basically, the Forum handles all issues relating to society business except Constitution and Bylaws changes and election of officers and members-at-large. In short, the BoG handles items formerly reserved for what was called "Full-voting members" and the Forum handles everything else: approving the budget, member dues, pages counts for publications, ratifying committee appointments, approving motions, conference and meeting approvals… etc.

Article V. Section 9: Make committee appointments 2 years, not three years.

Article V. Section 10: These are the ExCom changes per then President-elect Albert Wang's Ad Hoc and approved by BoG via email vote in 2013. The changes consolidate the VP positions of Awards, Technical Activities, and Education into other VP roles.

Article VII. Section 4: Fixed the quorum number for both the BoG and the Forum to be a majority of the voting members of each respective body.

Bylaws

Section 3.4 (was 3.8): Added that BoG must vote to remove a member from its ranks. Also, we have added that in order to be removed, two-thirds vote of the BoG with quorum present is required.

Section 3.5 (was 3.9): Added "or other society governing documents" (such as committee charters) as taking precedent over Robert's Rules.

Section 5.3, 5.5, and 5.6, 7.3: Clarified that the Nomination and Elections committee's role is to verify that candidates are qualified. They cannot remove candidates from the slate.

Section 5.6: A new 5.6 was added, granting permission to pilot general elections.

Section 7.1: Changed the requirement for running for an Officer position to require a candidate has served as either a member of ExCom for one year or as an elected member-at-large for one year.

Section 9.1: Defined EIC terms as per the guidance of then Publications VP Samar Saha's ad-hoc committee.

Section 13: What we have done here is clearly define the standing committees that exist and to require that each draft a charter outlining their roles, responsibilities, and operating polices to be approved by the Forum. What was previously in the Bylaws about standing committees was incomplete both in terms the committees themselves and how they function. These changes list the committees and provide a means of defining how each is structured and operates, but does so outside of the Bylaws… which is generally where such things should be defined.

These are a summary of the major changes to our Governing Documents. A detailed listing of all the changes made is available by contacting me at c.jannuzzi@ieee.org.

The complete EDS Constitution and Bylaws are available on the EDS website.

Christopher Jannuzzi
EDS Executive Director

Report on the VLSI Technology and Circuits Committee Meeting

The VLSI Technology and Circuits Committee Meeting was held on December 7th, at the site of the 2013 IEDM in Washington, DC.

Some key discussion points were:

1. Invite more members from Korea, Taiwan, India and Hong Kong
2. Proposal for T-ED special issue scheduled to be published in 2015: "Variation aware technology and circuits design for <14 nm"
3. Create three new sub-committees: Publication, Conferences/Workshops, and Publicity. All committee members should join at least one of the sub-committees.

Role of each subcommittee:

a. Publication: propose topics, special issues for journal, book, and review papers

b. Conferences/Workshops: input topics, invited talks, panel sessions, and candidates of committee members
c. Publicity: promote our activities in EDS Newsletter, website and other media

Seiichiro Kawamura
Publicity Chair
JST/CRDS, Tokyo, Japan

Shu Ikeda
VLSI Technology and Circuits Committee Chair,
Tei Technology
Austin, TX, USA

The VLSI Technology and Circuits Committee Meeting Attendees

23 EDS Members Elected to the IEEE Grade of Fellow

Effective 1 January 2014

Leda Lunardi
EDS Fellows Chair

Seiichi Aritome, SK Hynix Inc., Icheon-si, South Korea
for contributions to flash memory technologies

Phaedon Avouris, IBM Research Corporation, Yorktown Heights, NY, USA
for contributions to carbon electronics and photonics

Richard Brown, University of Utah, Salt Lake City, UT, USA
for contributions to microsystem design

Babu Chalamala, MEMC Electronic Materials, Inc., St. Peters, MO, USA
for contributions to the development of advanced materials and device technologies for vacuum microelectronics and field emission displays

Jing Kevin Chen, Hong Kong University of Science and Technology, Kowloon, Hong Kong
for contributions to compound semiconductor heterojunction transistor technologies

Donald Disney, Avogy, Inc., Cupertino, CA, USA
for contributions to power integrated circuits and energy efficiency applications

Ichiro Fujimori, Broadcom Corporation, Irvine, CA, USA
for contributions to oversampled data converters and gigabit wireline transceivers

Bruce Gurney, HGST, a subsidiary of Western Digital, San Jose, CA, USA
for contributions to spin valve Giant Magnetoresistance sensors for magnetic recording systems

Kazunari Ishimaru, Memory Division, Toshiba Corporation, Yokohama, Japan
for contributions to static random access memory and complementary metal-oxide semiconductor devices

Byoungho Lee, Seoul National University, Seoul, South Korea
for contributions to diffractive optics and three-dimensional display technologies

Kwyro Lee, Korea Advanced Institute of Science and Tech., Daejeon, South Korea
for management and R&D leadership in semiconductor technology

Zachary Lemnios, IBM Corporation, Yorktown Heights, NY, USA
for leadership in advanced technologies of defense security systems

Philip Mok, Hong Kong Univ. of Science & Technology, Hong Kong, China
for contributions to the design of analog power-management integrated circuits

Taiichi Otsuji, Tohoku University, Sendai, Japan
for contributions to plasmonic semiconductor integrated device technology for terahertz sensing

Daniel Radack, Institute of Defense Analyses, Kensington, MD, USA
for leadership in microwave and millimeter-wave integrated circuit technologies and packaging techniques

Jean-Pierre Raskin, Universit Catholique de Louvain (UCL), Louvain-la-Neuve, Belgium
for contributions to the characterization of silicon-on-insulator RF MOSFETs and MEMS devices

William Redman-White, University of Southampton, Hampshire, UK
for contributions to chip design aspects of telecommunications systems and RFIC design

Robert Reed, Vanderbilt University, Nashville, TN, USA
for contributions to understanding the effects of single-event particle radiation on integrated circuits

Mircea Stan, University of Virginia, Charlottesville, VA, USA
for contributions to power- and temperature-aware design of VLSI circuits and systems

Jacobus Swart, State University of Campinas—UNICAMP, Campinas, Brazil
for contributions to microelectronics education in Brazil

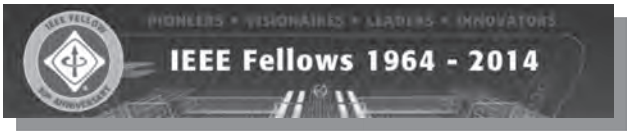
Jan Van Houdt, IMEC, Leuven, Belgium
for contributions to flash memory devices

Ya-Hong Xie, University of California, Los Angeles, CA, USA
for contributions to strained-silicon materials and devices

Rui Yang, University of Oklahoma, Norman, OK, USA
for contributions to the mid-infrared interband cascade laser and related optoelectronic devices

Leda Lunardi
EDS Fellows Chair
North Carolina State University
Raleigh, NC, USA

New Fellows Directory



New to the Fellow Web Site is the redesigned Fellows Directory. It is the most comprehensive online search and networking tool available to members. If you need to complete an IEEE Fellow Nomination, gather information for a region, section, or society, it's now easy to accomplish.

The information in the directory can be accessed by six categories: alphabetical by last name, year elevated, gender, IEEE region, IEEE society, and deceased. Within these categories, members can search, sort, or run a filter. For example, a report can be compiled on all Fellows within a specific region elevated in a particular year. The directory allows members to view the profiles of Fellows plus the ability to network with the Fellows. If you are not an IEEE member, you will have limited access to certain information.

Check it out today. The directory works on handheld devices and computers. To access the directory, go to www.ieee.org/fellows, then click the Fellow Directory icon.

Applauding 50 Years of Fellows

In 2014, IEEE will mark its 50th Fellow Class. It represents decades of honoring IEEE Fellows whose extraordinary accomplishments have changed the world.

The IEEE grade of Fellow was born in 1964 out of the merge of the American Institute of Electrical Engineers (AIEE) and the Institute of Radio Engineers (IRE). The emphasis on the elevation was and still is reserved for select IEEE members who have contributed importantly to the advancement of engineering, science, and technology, bringing the realization of significant value to society.

Only one-tenth of one percent of the total voting membership can be elevated in any one year. Over the last fifty years, IEEE has elevated roughly 10,000 members to this honor. This is a very small percentage compared to the total membership. Unquestionably, Fellows are the crown jewels of the organization. One can only imagine what the next fifty years will bring, and the new technology that will be developed, discovered, or taught, and what new IEEE Fellows will be recognized for their achievements.

Throughout the year, various celebrations will take place to honor those who have achieved this distinction. If you know an IEEE Fellow, congratulate him/her again for receiving this honor. You can recognize them personally, or you can acknowledge them publicly at region meetings, society meetings, section meetings, and/or conferences.

Rosann Marosy
Fellow Activities Manager
IEEE Member and Geographic Activities

Congratulations to the 40 EDS Members Recently Elected to IEEE Senior Member Grade!

Yasushi Akasaka
Travis Anderson
Amr Bayoumi
M S Bhat
Andrea Cester
Baoxing Chen
Hsien-Chin Chiu
Chris Connor
Felice Crupi
Peter Deane
Daniel Edelstein
Dean Gans
Steven Gross
David Grunlach
Hyunsang Hwang
Marek Hytha
Douglas Katzer
Irena Knezevic
Franz Kreupl
Qiliang Li
Chung-Hsun Lin
Ming-Chieh Lin
Cheryl Liss
Yang Liu
Kenneth Mays
Thomas McKay
Kirsten Moselund
Anand Murthy
Horst Rogalla
Frank Ryan
Andrie Scholten
Charles Surya
Pouya Valizadeh
Dapeng Wang
Jian-Ping Wang
Yifeng Wu
Huaqiang Wu
Alister Young
Hsiao Wen Zan
Shengdong Zhang

If you have been in professional practice for 10 years, you may be eligible for Senior Membership, the highest grade of membership for which an individual can apply. New senior members receive a wood and bronze plaque and a credit certificate for up to US $25 for a new IEEE society membership. Upon request a letter will be sent to employers, recognizing this new status.

Please remember to designate the Electron Devices Society as your nominating entity!

For more information on senior member status, visit: http://www.ieee.org/membership_services/membership/senior/index.html

To apply for senior member status, fill out the on-line application: https://www.ieee.org/membership_services/membership/senior/application/index.html. You will need to Sign-in with your IEEE account.

2013 Award Winners

2013 EDS J.J. Ebers Award Winner

The 2013 J.J. Ebers Award, the prestigious Electron Devices Society award for outstanding technical contributions to electron devices, was presented to Dr. Nobukazu Teranishi of the University of Hyogo and Shizuoka University, at the IEEE International Electron Devices Meeting in Washington, DC, on December 9, 2013. This award recognizes Nobukazu Teranishi *"For development of the Pinned Photodiode concept widely used in Image Sensors."*

Nobukazu Teranishi was born in Kobe, Japan in 1953. He received the B.S. and M.S. degrees in physics from University of Tokyo, 1976 and 1978, respectively.

Dr. Nobukazu Teranishi receiving the J.J. Ebers Award from EDS President, Paul Yu at the 2013 IEDM

He developed image sensors and cameras at NEC Corporation from 1978 to 2000 and at Panasonic Corporation from 2000 to 2013. He is now professor of University of Hyogo and Shizuoka University, where he develops photon counting image sensor, imagers for various wavelengths; (visible, infrared, X-ray), and new functions for image sensors.

He invented pinned photodiode (PPD) for image sensors with no image lag, low noise and low dark current in 1980. The PPD CCD has been in mass production since the mid 1980's because of its superior performance. In the late 1990's, PPD was introduced into CMOS image sensors. Then, their performance became competitive to CCD's. The high performance of PPD drove the pixel size

shrinkage, and realized higher resolution. Now, almost all CCD's and CMOS image sensors utilize the PPD. The PPD is most innovative technology for both CCD's and CMOS image sensors. The market has spread into every corner of the globe. As a result, 1.3 billion image sensors were produced in 2010.

He has authored and co-authored 80 papers and holds 46 Japanese patents and 21 US patents. His leadership at academic societies and industry and his PPD invention have been honored by government organizations as well as societies around the globe. He won the Prize of the President of KEIDANREN of National Invention Awards in 1994, Commendation by Minister of State for Science and Technology in 1997, Niwa-Takayanagi Award from the Institute of Image Information and Television Engineers in 2000 and 2013, Progress Medal and Hon. Fellowship from Royal Photographic Society in 2010, Progress Medal from Photographic Society of America in 2011. His group won the Emmy Award in 1991 by the broadcast-use CCD camera development.

He is a fellow member of the Institute of Image Information and Television Engineers of Japan, where he served as a chair of the paper editor committee and a chair of the Information Sensing Committee. He is also a Fellow of IEEE, where he served as a general chair for 1999 and 2005 IEEE Workshop on Charge-Coupled Devices & Advanced Image Sensors. He serves as President of International Image Sensors Society.

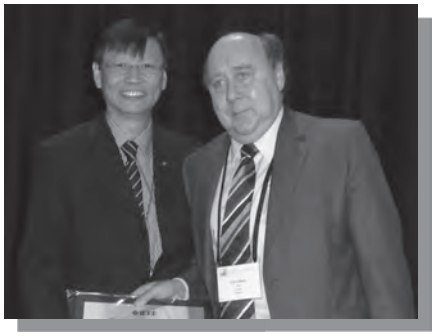
He and his wife, Makiko, have two sons and two lovely granddaughters. They like traveling and hot springs.

Jayant Baliga
EDS J.J. Ebers Award Chair
North Carolina State University
Raleigh, NC, USA

2013 EDS Distinguished Service Award

The IEEE Electron Devices Society (EDS) is extremely proud of the services that it provides to its members. Its members generate the premier new developments in the field of electron devices and share these results with their peers and the world at large by publishing their papers in EDS journals and presenting results in its meetings. This is a global activity that is effective because of the efforts of numerous volunteers. Many of these volunteers labor in relative obscurity, with their only reward being the satisfaction that they receive in being an important part of a successful organization, namely the IEEE Electron Devices Society. One means of thanking these volunteers is to recognize their contributions through the EDS Distinguished Service Award. This award for 2013 was presented to Professor Cor Claeys at the IEEE International Electron Devices Meeting in Washington, DC, on December 9, 2013.

Cor Claeys, born in Antwerp, received the B.S., M.S. and Ph.D. degrees in electrical engineering from KU Leuven in Belgium. His doctoral thesis work was on defect engineering for Charge Coupled Devices. After graduation he remained at the KU Leuven as research assistant and



Professor Cor Claeys (right) receiving the EDS Distinguished Service Award from EDS President, Paul Yu at the 2013 IEDM

staff member of the ESAT Laboratory. In 1984 he joined IMEC, the newly founded microelectronics research centre in Leuven, Belgium, as head of silicon processing, responsible for process development and applications in CCDs, silicon sensors, CMOS, non-volatile memories, SOI-CMOS and BiCMOS. In 1990 he became head of the research group on Radiation Effects, Cryogenic Electronics and Noise Studies. Presently, as Director Advanced Semiconductor Technologies he is responsible for Strategic Relations. Since 1990 he is also a Professor in material sciences at the KU Leuven.

His main interests are semiconductor technology, device physics, low frequency noise phenomena, radiation effects and defect engineering and material characterization. He co-edited a book on "Low Temperature Electronics" and "Germanium-Based Technologies: From Materials to Devices" and wrote monographs on "Radiation Effects in Advanced Semiconductor Materials and Devices" and "Fundamental and Technological Aspects of Extended Defects in Germanium". He authored and co-authored 14 book chapters, over 1100 technical papers and is author or co-author of more than 900 presentations at international Conferences and Symposia. He is editor or co-editor of more than 50 Conference Proceedings.

He has been project manager for a large number of European (SPECTRE, ACCES, STAR, NANOCMOS, PULLNANO, EUROSOI, SINANO, NANOSIL, SEANET, PRINS, NANOFUNCTION, etc.) research projects related to silicon technology and device physics. He also managed projects for the European Space Agency (ESA) related to the development of radiation detectors and radiation hardness of semiconductor devices.

He is active in different professional organizations. He served at

several committees within the Electrochemical Society and was in 2001-2003 Chair of the Electronics Division. For a decade he was editor of the Journal of the Electrochemical Society. Within SEMI he was Chair of the European Technical Programs Committee and is presently Chairman of the European SEMI Industry Strategy Symposium Committee. Since 1995 he became actively involved in IEEE and founded the EDS Benelux Chapter. Subsequently he served at a number of committees and held positions as Chapter Chair, Benelux Section Chair, elected Board of Governors member of EDS, EDS Vice President for Chapters/Regions, EDS President and IEEE Division Director. He was actively involved in the formation of new chapters all over the world and strongly supported the globalization of the society. Since 2000 he is a Distinguished Lecturer and gave presentations at many EDS mini-colloquia.

He is a Fellow of IEEE and also a Fellow of the Electrochemical Society. He was the recipient of the IEEE Third Millennium Medal and received in 2004 the Electronics Division Award.

Cor and his wife Rita, senior R&D integration engineer, live in Leuven, Belgium. They are the proud parents of Carmen, a general practitioner and Claus, a mechanical engineer working towards his Ph.D.

Paul K.L. Yu
EDS Jr. Past President
University of California at San Diego
La Jolla, CA, USA

2013 EDS Education Award Winner

Charvaka Duvvury

The EDS Education Award recognizes an IEEE/EDS Member from an academic, industrial, or government organization with distinguished contributions to education within the fields of interest of the IEEE Electron Devices Society. Charvaka Duvvury was recognized at the IEEE International Electron Devices Meeting in Washington, DC on December 9, 2013 as the 2013 EDS Education Award winner. The award cites Dr. Charvaka Duvvury *"For long-standing services in educating and developing engineers and students in the field of Electro-static Discharge (ESD) and its applications for electronic devices."*

Charvaka Duvvury worked as a semiconductor technologist at Texas Instruments for more than 35 years. He is currently working as an independent consultant in ESD technology, resolving ESD reliability concerns and educating new generations of electronics engineers. He is also co-chair of the Industry Council on ESD, bringing the electronics industry together towards realistic goals on ESD.

After receiving his Ph.D. in Engineering Science from the University of Toledo, he worked as a Post-Doctoral Fellow and an adjunct faculty member in the Physics Department of the University of Alberta at Edmonton, Canada. His research work at the University of Alberta was in Luminescence in Cu_2O.

He joined TI in 1977 where he was part of the original 256K/1Mb DRAM Design Group. During this phase of his career his contributions were in DRAM design, transistor parameter modeling, CHC, and eventually in the development of ESD technology. During the late 80s ESD was becoming much more critical as silicon technologies rapidly advanced with the introduction of LDD and the salicidies. He joined the VLSI Labs of TI-Dallas in 1988 working extensively on the impact of sub-micron technology on IC ESD protection concepts. He was elected Senior Member in 1990, Distinguished Member in 1997, and TI Fellow also in 1997. He was fortunate to have worked with many of the VLSI Lab's distinguished technical members which led to a deeper understanding of ESD for the ever increasing sensitivity of electronic components. This also led to his co-authoring the first book on ESD in silicon ICs.

He has significantly contributed to the industry by offering education in ESD for more than 25 years through tutorials at several IEEE sponsored conferences, as an EDS-DL participant, and as an organizer/instructor of the Berkeley Extension ESD Short Course for over a decade. He was elected as Board of Director for the ESD Association in 1997 and has been serving as the Academic Outreach Chair and Education Liaison promoting education about ESD in the universities by presenting seminars at 20 universities across the world. ESD is becoming critical with the emerging technologies for consumer and automotive electronics. For his consistent promotion of ESD education and research he has been twice awarded the SRC's Mehboob Kahn Outstanding Industry Liaison Award in 1994 and 2012. He also received the Outstanding Contributions Award from the ESD Association in 1990. He is deeply thankful to numerous industry colleagues, distinguished professors, student researchers and the ESDA for their collaborations and for providing opportunities for education in ESD.

He was elected as IEEE Fellow in 2008. From 2004-2006 he served on the IEDM CMOS Reliability Subcommittee, and during 2001-2011 served as editor of the IEEE-TDMR. He has published over 150 papers and holds more than 70 patents. He

enjoys cultural activities and world travels which often lead to visits to exotic places along with his wife, a professor of cultural anthropology and an avid photographer, and his son an architectural/structural engineer and an award-winning composer of classical music.

Meikei Ieong
2013 EDS Education Award Chair
TSMC Europe BV
Amsterdam

2013 EDS Early Career Award Winner

Runsheng Wang

The EDS Early Career Award recognizes an IEEE/EDS GOLD (Graduate of the Last Decade) member who has made outstanding contributions in an EDS field of interest.

The 2013 EDS Early Career Award was presented to Runsheng Wang of Peking University, Beijing, China at the EDS GOLD Event held in conjunction with the IEEE International Electron Devices Meeting in Washington, DC, on December 8, 2013.

Runsheng Wang received the B.S. and Ph.D. degrees from Peking University, Beijing, China in 2005 and 2010, respectively. From November 2008 to August 2009, he was a Visiting Scholar at Purdue University, West Lafayette, IN. He is currently an Associate Professor of Microelectronics at Peking University, Beijing, China. His research activities are presently in nanoscale MOS device reliability, variability and characterization, and also in new structural device modeling and simulation.

Dr. Wang has authored or co-authored over 70 journal and conference papers (including 17 IEDM/VLSI papers and 17 TED/EDL papers), 2 book chapters and 1 Chinese book. He holds 2 US patents and 12 Chinese patents. He co-established the IEEE EDS Peking University Chapter and served as the Chairman from 2008 to 2013. He also has served on the Technical Program Committee of IEEE IIRW and other conferences.

Albert Wang
EDS Early Career Award Chair
University of California
Riverside, CA, USA

EDS Member wins the 2013 Infosys Prize

Dr. Ramgopal Rao

The Infosys Prize 2013 for Engineering and Computer Science is awarded to Dr. V. Ramgopal Rao *"for his wide-ranging contributions to nanoscale electronics, for insightfully integrating chemistry with mechanics and electronics to invent new functional devices, and for innovation and entrepreneurship in creating technologies and products of societal value."* Ramgopal Rao is the Institute Chair Professor in the Department of Electrical Engineering; and Chief Investigator, Centre of Excellence in Nanoelectronics, Indian Institute of Technology, Bombay, India. In the message the Jury Chair, Pradeep K. Khosla, Chancellor, University of California, San Diego congratulated Prof. Ramgopal Rao for his extensive contributions to nanoscale electronics, which is the way of the future and will make tremendous impact.

Dr. V. Ramgopal Rao, M.Tech. from IIT-Bombay (1991) and Dr. Ingenieur from Universitaet der Bundeswehr Munich, Germany (1997) has received several awards including the Swarnajayanti Fellowship (2004), Shanti Swarup Bhatnagar Prize (2005). He received the IBM Faculty Award (2007), the Techno-Mentor award from the Indian Semiconductor Association (2009) and DAE-SRC Outstanding Research Investigator Award (2010). He has served as a visiting faculty at multiple universities around the world. His research led to several international patents that are used in the semiconductor industry, and to the formation of a start-up company. He is a Fellow of the Indian National Academy of Engineering, of the Indian Academy of Sciences, and of the National Academy of Sciences. He is a Senior Member of IEEE and IEEE EDS Region 10 SRC Vice-Chair.

The primary focus of Dr. Ramgopal Rao's research has been the deep understanding of the impact of materials and device design on nanoscale electron transport, and utilizing this understanding in the engineering of semiconductor devices and systems to significantly improve their performance. He was the first to provide clear insights into device-circuit interactions involving lateral asymmetric channel devices and FinFETs, which laid the foundation for power reduction in integrated circuits used in mobile phones. His research on drain-extended MOS (DeMOS) has enabled integration of high voltage and high frequency applications in standard CMOS.

The Infosys Foundation instituted the Infosys Prize, an annual award, to honor outstanding achievements of researchers and scientists and

carries USD100,000 cash prize and citation. The award intends to celebrate success and stand as a marker of excellence in scientific research. The award is presented this year by Dr. Kofi Annan, former UN Secretary General.

The long citation states: Dr. V. Ramgopal Rao has made substantial contributions in the science and engineering of nanoscale electron devices and their use in semiconductor integrated circuits, which has led to significant performance improvements and industrial impact. His leadership in nanoelectronics at the national level has enabled industry-academia partnerships that have led to growth of this industry in India. His creative insights on the chemistry of selective binding between organic and organometallic molecules and their integration with highly sensitive mechanical and electronic transduction in micro / nanodevices have led to a new platform for chemical sensing with unprecedented performance. He has gone further to translate science and engineering into innovative technologies and products by creating a commercial enterprise, which could lead affordable uses in health and security applications.

MK Radhakrishnan
Editor-in Chief, EDS Newsletter
NanoRel
Bangalore, India

Status Report from the 2013 EDS PhD Student Fellowship Recipients

Agis A. Iliadis
EDS Student Fellowship Committee Chair

The EDS PhD Student Fellowship Program is designed to promote, recognize, and support graduate level study and research within the Electron Devices Society's Fields of Interest.

The 2013 EDS PhD Student Fellowship recipients were: **Hong-Yu (Henry) Chen** from Stanford University, **He Tian** from Tsinghua University, and **Tarek Zaki** from the University of Stuttgart. The following are brief progress reports provided by the award winners.

Hong-Yu (Henry) Chen has been making further progress in his research on resistive switching random access memory (RRAM). As a part of his graduate study, he participated in the Stanford School of Engineering China Ph.D. Research Exchange Program in fall, 2014. During the oversea program, he collaborated with Prof. Jinfeng Kang's group at Peking University and Prof. Tian-Ling Ren's group at Tsinghua University simultaneously. His most recent output includes the investigation of pulse rising edge effects on programming and write disturb issues on half-selected cells of cross-point RRAM arrays, and the result will be presented at International Symposium on VLSI Technology, Systems and Applications (2014 VLSI-TSA) in April in Taiwan, R.O.C. In addition, he has worked with another 2013 EDS Ph.D. Fellowship winner, He Tian, on the development of Graphene-based RRAM using Laser-scribing technology, aiming to build low-cost and time-efficient systems on various flexible substrates. His paper citation has increased to more than 200 times with H-index 9. He is expecting to defend his thesis in spring, 2014.

He Tian has been moving forward his research work on wafer-scale flexible graphene strain sensors, multi-functional graphene devices and graphene-based resistive switching memory. He recently gave a presentation at IEDM 2013 in Washington, DC, about making a graphene strain sensor with a gauge factor up to 9.49, demonstrating a significant improvement over conventional metal gauge sensors. His most recent achievement has been the wafer-scale integration of graphene-based electronic, optoelectronic and electroacoustic devices. This work was published in *Scientific Reports* on 8th January 2014. He is also making a cost-effective flexible graphene resistive switching random access memory using laser-scribed graphene technology in collaboration with Henry Hong-Yu Chen (Supervisor Philip Wong) from Stanford University. He is currently the student team leader for a major research project of "DEVELOPING NOVEL FLEXIBLE NANO DEVICES" and the vice president of the IEEE EDS Tsinghua University Student Chapter. His dream is to incorporate graphene devices into real applications and let more students join the IEEE EDS community in the near future.

Tarek Zaki (S'07) is pursuing a Ph.D. degree on low-voltage thin-film transistors and mixed-signal circuits based on organic semiconductors at the University of Stuttgart and the Institute for Microelectronics Stuttgart (IMS CHIPS), Germany. Over the course of his research work, he has set the following milestones and accomplishments in the domain

of organic electronics: (i) realizing the world's shortest channel organic thin-film transistor (OTFT) fabricated through stencil-mask lithography (0.6 μm) and achieving the highest cutoff frequency for low-voltage, air-stable OTFTs (3.7 MHz); (ii) performing the first comprehensive experimental study on the frequency response of OTFTs using S-parameter measurements, thus, allowing for individual ac device characterization; (iii) demonstrating a record in performance (thousand-fold faster) and compactness (thirty-times smaller) for organic-based digital-to-analog converters with respect to prior state of the art; and (iv) developing a physics-based, scalable capacitance compact model for OTFTs. This work benefits from a close cooperation with the Max Planck Institute for Solid-State Research, Stuttgart, Germany, and the results are presented at top publication venues, including EDL, T-ED, JSSC, ISSCC Tech. Dig. and Organic Electronics. Recently, Tarek joined a new project called *Komplexe Systeme in Folie* (Complex Systems-in-Foil), which includes 10 research facilities and industrial partners, such as Festo and Würth Elektronik. The aim of the project is to expand the favorable advancement of flexible electronics and explore the feasibility of producing an industrial design. Tarek's main role in this project is to develop an organic-based smart-skin solution to monitor the bending activity of bionic grippers.

Agis A. Iliadis
EDS Student Fellowship
Committee Chair
University of Maryland
College Park, MD, USA

Status Report from the 2013 EDS Masters Student Fellowship Winners

The EDS Masters Student Fellowship program is designed to promote, recognize, and support Masters level study and research within the Electron Devices Society's Fields of Interest.

The 2013 EDS Masters Student Fellowship winners were: **Enes Battal** from Bilkent University, **Zhongyu Li** from the University of Electronic Science and Technology of China, and **Yang Lu** from the University of Pennsylvania. The following are brief progress reports provided by the award winners.

Enes Battal is expected to obtain his M.S. degree in Electrical and Electronics Engineering at Bilkent University, Ankara, Turkey, in June 2014, and he is planning to continue to pursue the Ph.D. at one of the top ranking universities in the USA. He is currently working on development and characterization of actively tunable optical structures and their use in the realization of novel reconfigurable optical nanodevices. He is interested in thermal, field effect and non-volatile optical modulation methods. He is also exploring novel materials for plasmonics. He published his recent results in Surface Plasmon Photonics 2013 Conference (Ottawa, Canada) and IEEE Photonics 2013 Conference (Seattle, USA). He has authored or co-authored more than 15 journal and conference papers.

Zhongyu Li is expected to obtain his M.S. degree in Electronic Engineering at University of Electronic Science and Technology of China, China, in June 2015, and will continue to pursue the Ph.D degree there. His research interests mainly concern radar imaging system design. In November 2012, his research team conducted a flight experiment of a certain novel radar system for the first time in the world in Xi'an, China. He was responsible for real time imaging using the high speed device of his research, and he achieved the first real time image of this kind in the world. Till now, he has published five papers on several international journals and conferences, and also published six papers as the second author on IEEE GRS Transations, IEEE AES Transactions, etc. He has successfully applied eight Chinese patents for invention.

Yang Lu received the B.S degree in microelectronics from Peking University, Beijing, China, in 2012. He is currently working toward the M.S. degree at University of Pennsylvania, Philadelphia, Pennsylvania and will continue to pursue the

Ph.D. degree there. Since 2011, Yang Lu has been working on Resistive Random Access Memory (RRAM) in various material systems, including metal oxide based, filamentary RRAM and silicon based, nanometallic RRAM. He and his colleagues investigated about switching mechanisms and degradation behaviors in RRAM and successfully developed a simplified model for the RESET process and a circuit model for load effect. Right now, he focuses on purely electronic resistive switching in random materials for economic and CMOS-compatible memory applications. He has published his work in IEEE Electron Device Letters, IEDM 2011 & 2012, and given conference presentations in IRPS 2012, NVMTS 2013, etc.

Agis A. Iliadis
EDS Student Fellowship
Committee Chair
University of Maryland
College Park, MD, USA

2014 Award Call for Nominations

2014 EDS J.J. Ebers Award
Call for Nominations

The IEEE Electron Devices Society invites the submission of nominations for the 2014 J.J. Ebers Award. This award is presented annually for outstanding technical contributions to electron device IEEE International Electron Devices Meeting (IEDM).

The J.J. Ebers Award on-line nomination form is available on the EDS website, at http://eds.ieee.org/jj-ebers-award.html.

The deadline for submission of nominations for the 2014 award is July 1, 2014.

If you have any questions or need further information on this award, please do not hesitate to contact Laura Riello of the EDS Executive Office at l.riello@ieee.org.

2014 EDS Education Award
Call for Nominations

The IEEE Electron Devices Society invites the submission of nominations for the EDS Education Award. This award is presented annually by EDS to honor an individual(s) who has made distinguished contributions to education within the field of interest of the Electron Devices Society. The recipient(s) is awarded a plaque and a check for $2,500, presented at the IEEE International Electron Devices Meeting (IEDM).

The nominee must be an EDS member engaged in education in the field of electron devices, holding a present or past affiliation with an academic, industrial, or government organization. Factors for consideration include achievements and recognition in educating and mentoring students in academia or professionals in the industrial or governmental sectors. Specific accomplishments include effectiveness in the development of innovative education, continuing education programs, authorship of text books, presentation of short-courses at EDS sponsored conferences, participation in the EDS Distinguished Lecturer program, and teaching or mentoring awards.

Since this award is solely given for contributions to education, the nomination should exclude emphasis on technical contributions to engineering and physics of electron devices.

Nomination forms can be found on the EDS web site at http://eds.ieee.org/education-award.html.

The deadline for the submission of nominations for the 2014 award is September 1, 2014.

Call for Nominations
2014 IEEE EDS Early Career Award

Description: Awarded annually to an individual to promote, recognize and support Early Career Technical Development within the Electron Devices Society's field of interest

Prize: An award of US$1,000, a plaque; and if needed, travel expenses not to exceed US$1,500 for a recipient residing in the US and not to exceed US$3,000 for a recipient residing outside the US to attend the award presentation.

Eligibility: Candidate must be an IEEE EDS member and must have received his/her first professional degree within the 10th year defined by the August 15th nomination deadline and has made contributions in an EDS field of interest area. Nominator must be an IEEE EDS member. Previous award winners are ineligible.

Selection/Basis for Judging: The nominator will be required to submit a nomination package comprised of the following:

- The nomination form that is found on the EDS web site, containing such technical information as the nominee's contributions, accomplishments and impact on the profession or economy and a biographical description.
- A minimum of two and a maximum of three letters of recommendation from individuals familiar with the candidate's technical contributions and other credentials, with emphasis on the specific contributions and their impacts.

The basis for judging includes such factors as: the demonstration of field leadership in a specific area; specific technical contribution(s); impact on the profession or economy; originality; breadth; inventive value; publications; honors; and other appropriate achievements.

Schedule: Nominations are due to the EDS Executive Office August 15th each year. The candidate will be selected by the end of September, with presentation to be made in December.

Presentation: At the EDS Awards Dinner that is held in conjunction with the International Electron Devices Meeting (IEDM) in December. The recipient will also be recognized at the December EDS BoG Meeting.

Nomination Form: Complete the online nomination form by August 15, 2014. All endorsement letters should be sent to l.riello@ieee.org by the deadline.

For more information contact: l.riello@ieee.org or visit: http://eds.ieee.org/early-career-award.html

2014 PhD Student Fellowship

Description: One year fellowships awarded to promote, recognize, and support PhD level study and research within the Electron Devices Society's field of interest. The field of interest for EDS is all aspects of engineering, physics, theory, experiment and simulation of electron and ion devices involving insulators, metals, organic materials, plasmas, semiconductors, quantum-effect materials, vacuum, and emerging materials. Specific applications of these devices include bioelectronics, biomedical, computation, communications, displays, electro and micro mechanics, imaging, micro actuators, optical, photovoltaics, power, sensors and signal processing.

It is expected that three fellowships will be awarded, with the intention of at least one fellowship being given to eligible students in each of the following geographical regions every year: Americas, Europe/Middle East/Africa, and Asia & Pacific. Only one candidate can win per educational institution.

Prize: US$5,000 to the student and if necessary funds are also available to assist in covering travel and accommodation costs for each recipient to attend the EDS Administrative Committee meeting for presentation of the award plaque. The EDS Newsletter will feature articles about the EDS PhD Fellows and their work over the course of the next year.

Eligibility: Candidate must be an IEEE EDS student member at the time of nomination; be pursuing a doctorate degree within the EDS field of interest on a full-time basis; and continue his/her studies at the current institution with the same faculty advisor for twelve months after receipt of award. Nominator must be an IEEE EDS member. Previous award winners are ineligible.

Basis for Judging: Demonstration of his/her significant ability to perform independent research in the fields of electron devices and a proven history of academic excellence.

May 15, 2014 Submission Deadline

Nomination Package

- Nomination letter from an EDS member
- Two-page (maximum) statement by the student describing his or her education and research interests, accomplishments and graduation date
- One-page biographical sketch of the student (including student's mailing address and email address)
- One copy of the student's under-graduate and graduate transcripts/grades. Please provide an explanation of the grading system if different from the A-F format.
- Two letters of recommendation from individuals familiar with the student's research and educational credentials. Letters of recommendation cannot be from the nominator.

Timetable

- Completed nomination packages are due at the EDS Executive Office no later than **May 15, 2014**
- Recipients will be notified by July 15
- Monetary awards will be given by August 15
- Formal award presentation will take place at the EDS Board of Governors Meeting in December

EDS is now accepting nomination package submissions via e-mail, fax and mail!

Email: edsfellowship@ieee.org
Fax: +1-732-235-1626

Mail:
IEEE EDS Executive Office
PhD Student Fellowship Program
445 Hoes Lane, Piscataway, NJ 08854 USA

For more information contact:
edsfellowship@ieee.org

Visit the EDS website:
http://eds.ieee.org/eds-phd-student-fellowship-program.html

2014 Masters Student Fellowship

Description: One-year fellowships awarded to promote, recognize, and support graduate Masters level study and research within the Electron Devices Society's field of interest: all aspects of engineering, physics, theory, experiment and simulation of electron and ion devices involving insulators, metals, organic materials, plasmas, semiconductors, quantum-effect materials, vacuum, and emerging materials. Specific applications of these devices include bioelectronics, biomedical, computation, communications, displays, electro and micro mechanics, imaging, micro actuators, optical, photovoltaics, power, sensors and signal processing.

Three fellowships will be awarded, with the intention of at least one fellowship being given to eligible students in each of the following geographical regions every year: Americas, Europe/Mid-East/Africa, Asia & Pacific. Only one candidate can win per educational institution.

Prize: US$2,000 and a plaque to the student, to be presented by the Dean or Department head of the student's enrolled graduate program.

Eligibility: Candidate must be an IEEE EDS student member at the time of nomination; be accepted into a graduate program or within the first year of study in a graduate program in an EDS field of interest on a full-time basis; and continue his/her studies at a graduate education institution. Nominator must be an IEEE EDS member and preferably be serving as the candidate's mentor or faculty advisor. Previous award winners are ineligible.

Basis for Judging: Demonstration of his/her significant ability to perform research in the fields of electron devices and proven history of academic excellence in engineering and/or physics as well as involved in undergraduate research and/or supervised project.

May 15, 2014 Submission Deadline

Nomination Package

- Nomination letter from an EDS member who served as candidate's mentor or faculty advisor.
- Two-page (maximum) statement by the student describing his or her education and research interests, accomplishments and graduation date. This can include undergraduate, graduate and summer internship research work.
- One-page biographical sketch of the student (including mailing address and e-mail address)
- One copy of the student's transcripts/grades
- One letter of recommendation from an individual familiar with the student's research and educational credentials. Letters of recommendation cannot be from the nominator.

Timetable

- Completed nomination packages are due at the EDS Executive Office no later than **May 15, 2014**
- Recipients will be notified by July 15
- Monetary awards will be presented by the Dean or Department Chair of the recipient's graduate program at the beginning of the next academic term.

EDS is now accepting nomination package submissions via e-mail, fax and mail!

Email: edsfellowship@ieee.org
Fax: +1 732-235-1626

Mail:
IEEE EDS Executive Office
PhD Student Fellowship Program
445 Hoes Lane, Piscataway, NJ 08854 USA

For more information contact:
edsfellowship@ieee.org

Visit the EDS website:
http://eds.ieee.org/eds-masters-student-fellowship-program.html

Young Professionals

Working Successfully in the Semiconductor Industry

Doug Verret Ph.D.
IEEE Fellow,
TI Fellow Emeritus

There is a huge difference between surviving in our industry versus thriving. Based upon over three decades of experience in this industry working for an international company, I have observed patterns of behavior that are conducive and others that are detrimental to a successful career.

Let me start with a set of common misconceptions that recent college graduates and junior engineers entertain. They are

- Thinking that:
  - you know most or all of the technical information you need to do the job,
  - all gaps in your knowledge will be filled via formal training,
  - the best technical solution to a problem is the best business solution,
  - solutions to business problems are unique,
  - you have finished your education, and/or
  - data speak for itself
- Vastly underestimating the importance of soft skills *esp. communication skills*
- Dismissing the necessity of possessing business acumen
- Not understanding the importance of relationships and networking

So what are the right ingredients for cooking into your skill set? Actually there are many which I have distilled into the three that are at the top of the list, but which in turn are built upon others.

*The first is **credibility**.* That by itself is the principal value you offer to your customer and your employer. Everything else is secondary. If you lack credibility all else is for naught. Credibility is made up of *technical competence, ethics, integrity and honesty.*

*The second is **ability to influence**.* Modern technology is complex and successful organizations must deal with this complexity by becoming flexible, diverse, nimble and innovative. Modern engineers do not have "authority" over all required technology or technologists. Therefore the ability to influence is essential. Its constituents are *communication skills, networking, cultural sensitivity and teaming skills.*

*The third is **creating customer value**.* Invention is not useful unless it becomes innovation. Innovation really consists of useful ideas which are what create value for customers, which automatically creates value for employers and in turn enhances the value of the employee. Its constituents are *networking, communication skills, business acumen, understanding internal processes and creativity.*

Cultivate these, and that is how you thrive in this industry. An expanded version of this article is available in webinar format which can be viewed at http://eds.ieee.org/webinars.html for EDS members. Non-members can contact me for a copy of the full presentation at Verret@IEEE.org.

Doug Verret Ph.D.
IEEE Fellow, TI Fellow Emeritus
Texas Instruments Inc., retired
Verret@IEEE.org

Latest EDS Webinar

Sarah Kurtz
NREL

The California Energy Commission is planning to propose updates to the requirements for their eligible solar electric equipment guidelines. For PV modules, it will be proposed to add a requirement for a design qualification test to be more consistent with common requirements used around the world. The CEC will also propose the voluntary use of a set of tests that go beyond the standard qualification. Featuring presentations from experts from across the PV spectrum, this webinar provides attendees with a special preview of these proposed changes and their potential impact on PV development and deployment.

To help the EDS and PV communities understand these potential new guidelines, we are pleased to have sponsored a special event entitled *New Requirements to be Proposed for the CEC's Eligible Solar Electric Equipment.* The webinar was held Tuesday, February 4, 2014. EDS volunteer Sarah Kurtz of the National Renewable Energy Laboratory envisioned the event and also served as moderator. Sarah was joined by:

- Patrick Saxton of the California Energy Commission described the process planned for updating the CEC's requirements for their eligible hardware guidelines and he also provided an overview of the proposed changes.

- John Wohlgemuth of the National Renewable Energy Laboratory described Qualification Plus—a set of tests that go beyond the standard qualification test and which the CEC will propose as an optional set of tests.
- Ralph Romero of Black & Veatch explained how Black & Veatch finds these developments useful toward higher quality PV deployments in the U.S.

Several hundred members and non-members alike registered to attend this special event. It was an outstanding talk for which we extend our heartfelt thanks to Sarah, Patrick, John, and Ralph.

For those who missed the live event, you can always view a replay of it on the EDS webinar archive page at, http://eds.ieee.org/webinar-archive.html.

QuestEDS

Samar Saha
EDS President-Elect

Interested in knowing why it's not possible to measure the built-in voltage of a PN junction using a voltmeter? Do you need to understand the best way to derive an expression for the average thermal velocity of an electron? Or are you curious about what quantum dots and wires are? The answers to these questions and more are available through the QuestEDS Question and Answer page.

To ask a question not already addressed on the Q&A page, visit www.ieee.org/go/questeds Technical experts answering the questions posed represent academic, government, and industry sectors.

Questions are grouped into nine technical categories and two general ones. Technical categories cover subject areas like semiconductor and device physics, process technology, device characterization, technology CAD, compact modeling, VLSI interconnects, photovoltaics, and quantum electronics. Subject areas addressed are anticipated to expand in the future. Two other categories address questions pertaining to educational activities and general inquiries about society membership. Within a two week time frame from when the question is asked, an answer is posted online. Incoming questions are handled by an editor-in-chief who ensures that they fall within the technical scope of EDS and that they are adequately answered.

DIODE

Question 001-07

Why is it not possible to measure the built-in voltage of a pn juction using a voltmeter?

Answer: The built-in voltage of a PN junction can be considered as the contact potential between two dissimilar metals. When the leads of a voltmeter are contacted to either side of a PN junction, the contact potential between the voltmeter lead and P-type material, contact potential of the PN junction, and the contact potential between the N-type material and the voltmeter lead form a closed loop. Since the sum of all contact potentials in a closed loop is zero, the built-in voltage cannot be measured by a voltmeter. (Reference: Operation and Modeling of the MOS Transistor, chapter 1, 2nd edition, by Y. Tsividis).

For the answer to this recent submission, visit http://eds.ieee.org/member-sign-in-form.html?notauth=1. Your IEEE login is required to view the answer page. After authentication you will be redirected to the answer page, where you can select the appropriate topic link.

Samar Saha
EDS President-Elect
Ultrasolar Technology
Santa Clara, CA, USA

Chapter News

We are introducing a new section on Chapter News where Chapters are invited to write in and to introduce themselves to others. Mainly the theme is how the Chapter performs and grows. In this issue we are presenting three EDS Chapters which won the 2013 Chapter of the Year Awards.

IEEE ED Delhi Chapter

–by Mridula Gupta and Manoj Saxena

The IEEE ED Delhi Chapter was started in 2007 with initially twenty-two members. Currently we have seventy-three active members. Our motto is to generate wide spread interest in the field of science and engineering particularly in the field of electronics devices amongst the professionals in general and students in particular. The ED Delhi Chapter also helps in shaping career of the students and enlightens them about the various opportunities, in research and industries. We organises various events like Symposia, Workshops, Conferences, DL talks, Mini-Colloquia, Technical talks, etc. at different locations within New Delhi and other neighbouring states like Utter Pradesh and Rajasthan. The Chapter EXECOM has members from diverse disciplines, starting from faculty members of educational institutes to scientists from research laboratories and industry.

In 2013, chapter organized first student conference, National Conference on Recent Developments in Electronics (NCRDE 2013) in conjunction with Third National Workshop on Recent Trends in Semiconductor Devices and Technology where senior scientists from DRDO (Defence Lab), Government of India delivered invited lectures to apprise students and young professionals about the developments in the area of semiconductor device and technology. The chapter also organized several workshops jointly with Three Science Academies of India—Indian National Science Academy (INSA), New Delhi, Indian Academy of Sciences (IASc), Bangalore and National Academy Sciences of India (NASI), Allahabad. The main focus of these workshops was to make undergraduate science and engineering graduate students the frontiers in science and engineering and history of electronics. Lecture Workshop On Trans-disciplinary Areas of Research and Teaching by Shanti Swaroop Bhatnagar Awardee from the area of Physical/ Life Science/ Engineering discussed the role and importance of trans-disciplinary studies and research with under graduate students. The organisation of the workshop helped faculty members in developing innovative undergraduate courses. IEEE student members who act as IEEE volunteers, and mainly are research students, works as a group, ensures the successful organisation of these lectures/workshop/conference. We have experienced that these young bloods motivate many more to join this EDS.

IEEE ED IRE NASU-Kharkiv Student Branch Chapter

–by Illia Fedorin

The IEEE ED IRE NASU-Kharkiv Student Branch Chapter is part of the IEEE Ukraine Section and the IEEE Region 8 (Europe, Middle-East and Africa). The Chapter was initially established in Kharkiv on February 17, 2010 by 12 Founding Student Members.

The Chapter is based in Kharkiv and hosted by the O. Ya. Usikov Institute for Radiophysics and Electronics of NAS of Ukraine (IRE NASU), the leading scientific institution on radio physics, vacuum electronics, quasi-optics, microwave studies in solid-state physics and biophysics, radio wave propagation, remote sensing of Earth from airborne and space-borne platforms, etc.

The main objective of the Chapter is to promote a harmonious interaction between the Students and Science. We try to become a venue for identifying new potential volunteers and leaders. The Chapter is actively involved in the organization of industrial visits, career talks, conferences, lectures, technical meetings, field trips, and other activities of benefit to her members.

The important goal of the Chapter is to create awareness among the students in the field of electron devices, microwaves and telecommunications. With this aim, the Chapter holds the Young scientist conference travel grant program. Ex-USSR applicants are welcome to apply for the annual Conference Travel Grant for attending international conferences outside of the ex-USSR.

The Chapter Committee annually awards several prizes at Kharkiv Young Scientists Conference "Radiophysics, Electronics, Photonics, and Biophysics", which consist in ED-S Student Membership.

The Chapter actively endorsed the practice of having contest-like Young Scientists Seminars, which precede Members of Scientific Council of IRE NASU vote on assignment of annual and biannual competitive bursaries/ scholarships to young scientists of IRE NASU.

With rapidly growing interest in electrical/electronic engineering the Chapter activities become more relevant. We believe, that, in line with the tradition of IEEE of advancing technological innovation and global international community, our Chapter does our best to achieve these goals.

IEEE ED/MTT/EMB Brasilia Chapter

–by Fabiano Araujo Soares

The ED/MTT/EMB Brasilia Chapter is a chapter that focuses mainly in recruiting new potential members by

increasing the number of engineering students. Our main goal until 2013 was the Electron Project. This project, conducted together with the Brasília Student Branch, developed many activities with high school students. With an electron kit, high school students were able to execute several electronic experiments. The aim of this project was to develop an interest in the electronic field, increasing the number of candidates for the electronic engineering courses in Brazil. Also, in 2013 we received some distinguished guests and international speakers such as Dr. Fernando Guarin. For 2014, we are planning a summer camp during which we will invite high school students to the University so they can attend different lectures and workshops about the engineering courses and about the engineering job market in Brazil and in the world, and also have the opportunity to meet international distinguished lecturers in the electronic field. We are also planning to increase the number of speaks for grad and undergrad students. There is still a long way to go, as the demand for engineers in Brazil is now constantly increasing and our Universities have to respond by attracting more talents to supply the developing job market. We hope that with projects like Electron and Summer Camp, we can increase the number of people interested in engineering.

Singapore Chapter Family Day

The REL/CPMT/ED Singapore Chapter organized a social event, Family Day, as a family get together of Chapter members on December 28, 2013, at KT's Grill restaurant with a sumptuous lunch.

Social event, a Family Day lunch in KT's Grill restaurant

Regional News

USA, Canada & Latin America (Regions 1–6, 7 & 9)

2013 SBMicro Conference and EDS Region 9 Best Student Paper Award

–by Jacobus W. Swart,

The 28th Symposium on Microelectronics Technology and Devices, SBMicro 2013, took place in Curitiba, Brazil, from September 3–6, 2013. This symposium was organized by two Brazilian scientific societies: SBMicro (Sociedade Brasileira de Microeletrônica) and SBC (Sociedade Brasileira de Computação) and was technically co-sponsored by the IEEE Electron Devices Society and the Electrochemical Society. The SBMicro symposium is a forum held annually in Brazil and dedicated to fabrication and modeling of microsystems, integrated circuits and devices. The goal of the symposium is to bring together researchers in the fields of processing, materials, characterization, modeling and TCAD of integrated circuits, optoelectronics and MEMS. In conjunction with SBMicro 2013, a co-located symposium was held at the same place and time, namely the 26th Symposium on Integrated Circuits and Systems Design. This symposium was also organized by the same two local societies. The two symposia have been held together since the year 2000. This edition had a total attendance of more than 300 participants.

During the first day of the conference an open tutorial day was organized and partially supported by the local EDS chapters. It is worth to mention that no registration was required for attending this first day, which included three tutorial talks given by EDS Distinguished Lecturers:

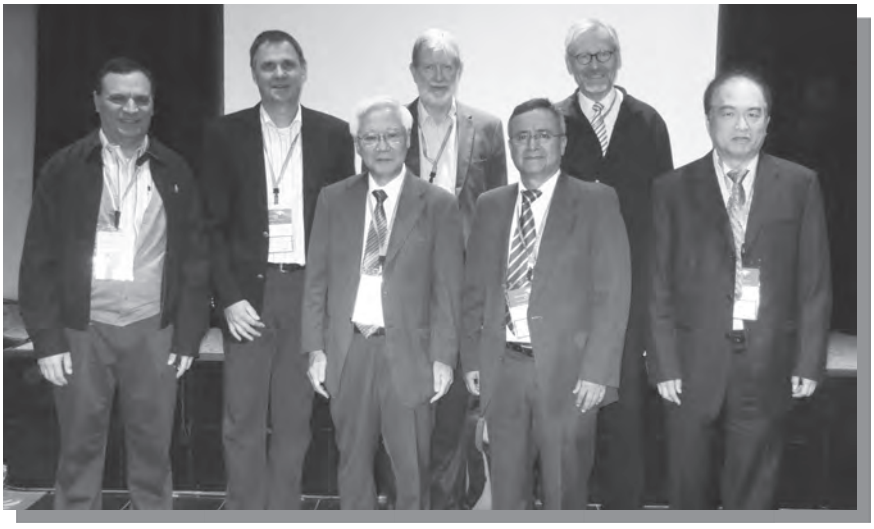
- *"High-Dinamic Range Imagers,"* by Joachim Burghartz from IMS Chips, Germany,
- *"MEMS and 3D Integration,"* by Werner Weber, from Infineon Technologies AG, Germany, and
- *"Methodology and Challenges for the Qualification of Leading Edge Semiconductor Technologies,"* by Fernando Guarin, from IBM Microelectronics, USA.

In addition to the tutorial day lectures, invited papers were delivered by EDS Distinguished Lecturers (DLs) as part of the conference program, which included the following talks:

- *"Future of Nano CMOS,"* by Hiroshi Iwai, TIT, Japan (as key note talk),
- *"3D Stacking of Silicon Chips,"* by Werner Weber, Infineon Technologies AG, Germany,
- *"Atomistic Magnetoconductance Effects in Strained FETs,"* by Edmundo A. Gutierres-D, INAOE, Mexico,
- *"Ultra-Thin Si Chips for Flexible Electronics—Process Technology Characterization, Assembly and Applications,"* by Joachim Burghartz, IMS Chips, Germany,
- *"Study of III–V MOS Capacitors for post CMOS Applications,"* by Eduard Yi Chang, NCTU, Taiwan/ROC, and
- *"Potential and Limitation of UTBB SOI for Advanced CMOS,"* by Cor Claeys, IMEC, Belgium.

During the welcome reception of the conference, awards were delivered to recipients, including the 2013 EDS Region 9 Best Student Paper Award. The award recipient was Renan Trevisoli Doria, from the University of São Paulo for his paper *"Surface-Potential-Based Drain Current Analytical Model for Triple-Gate Junctionless Nanowire Transistor,"* published at *IEEE-TED*, vol.59, no.12, p.3510 (2012). The proceeding of SBMicro 2013 was published for the first time by *IEEE Xplore*. The proceedings of previous years were published as a Transaction book of ECS.

Before and after the SBMicro conference many of the DL's visited the chapters at the University of Campinas and at the University of São Paulo, where they gave additional talks on the same topics, visited the microelectronics labs and discussed



EDS Distinguished Lecturers at the Tutorial Day and some of the SBMicro conference organizers

technical topics with students and academic staff.

The next SBMicro will take place in Aracaju, Sergipe, in the northeast of Brazil, from September 1–5, 2014. Topics of interest include, but are not limited to: semiconductor processing, IC, optoelectronics and MEMS fabrication; novel materials and devices; reliability; technology CAD; displays; thermal effects and models; nanoelectronics; device characterization and modeling; microsystem networks, sensors and actuators; package and technology roadmaps; packaging; photovoltaic technology, plasma technology and engineering education.

Important deadlines are as follows: Submission: March 31, 2014; Notification of Acceptance: May 18, 2014; Camera-ready: June 1, 2014.

For more information please see http://www.sbmicro.org.br/sbmicro and/or contact the publicity chair: Jacobus Swart (jacobus@ieee.org).

1st Brazilian Workshop on Snap Kits and Mini-Colloquium at UNICAMP

–by Salomão M. da Silva, Jacobus W. Swart and Fernando Guarin

The 1st Brazilian Workshop on Snap Kits and Mini-Colloquium were organized by the EDS Region 9 Subcommittee Regions/Chapters together with the EDS Student Chapter at UNICAMP, September 9–10, 2013, at CCS/UNICAMP, Campinas, Brazil. A few years ago some of the EDS chapters in Brazil began volunteering to motivate young talent to try careers in electrical engineering and related fields. The chapters developed programs using Snap Circuit Kits from Elenco Electronics, donated by the IEEE Electron Devices Society. The following chapters and university groups in Brazil were involved in this task: University of Brasilia, Federal University of Para, Federal University of ABC, Federal University of Campina Grande and State University of Campinas. The EDS chapter at INAOE, Mexico, was also invited and participated in the workshop.

Speakers and organizers of the Workshop on Snap Kits and EDS Mini-Colloquium

The purpose of the workshop was to share experiences and materials between the different groups. The workshop began with a general overview of the program: *"Program Overview EDS-ETC – Engineers Demonstrating Science: an Engineer Teacher Connection,"* delivered by Fernando Guarin. Copies of the presentations given by the participants are available on the Region 9 SRC website: www.edsr9.org. The most experimental group is the chapter from the University of Brasilia, reaching many school-age students in their area's public schools. The Brasilia chapter was recognized by IEEE for their results and also distinguished with the EDS Region 9 Chapter of the Year Award for 2013.

After the Workshop on Snap Kits, a Mini-Colloquium was held in sequence including the following talks by EDS Distinguished Lecturers: *"Future of Nano CMOS,"* by Hiroshi Iwai; *"Thin Channel InAs HEMT for Sub Terahertz and Post CMOS Applications,"* by Edward Chang; *"Atomistic Magnetoconductance Effects in Strained FETs,"* by Edmundo Gutiérrez; *"Ultra-thin Chips—a New Paradigm in Silicon Technology,"* by Joachim Burghartz and *"Leading Edge Technologies for a Smarter Planet,"* by Fernando Guarin.

Besides the participants of the Workshop on Snap Kits and the students and academic staff members of UNICAMP, there were also many attendees from nearby universities who attended the Mini-Colloquium, resulting in a fruitful event for all.

~ Francisco J. Garcia, Editor

Europe, Middle East & Africa (Region 8)

ED Finland

–by Ville Viikari

EDS Distinguished Lecturer and Region 8 Vice-Chair of the Electron Devices Society, Simon Deleonibus, visited the IEEE AP/ED/MTT Finland Chapter on December 5, 2013. Simon Deleonibus gave a lecture entitled *"Future Micro/Nano-Electronics: Towards Full 3D and Zero Variability,"* which drew an audience of approximately 50 people. In his lecture, Simon Deleonibus reviewed the major challenges that Nanoelectronics will have to face in the next decades in order to proceed scaling to the sub 10 nm nodes level and to approach zero variability. The main requirements will be to reduce leakage currents and reduce access resistances at the same time in order to fully exploit 3D integration at the device, elementary function, chip and system. New progress laws combined to the scaling down of CMOS based technology will emerge to enable new paths to Functional Diversification.

The distinguished lecture and chapter meeting was followed by

visits to the Aalto University and VTT Technical Research Centre of Finland, where local researchers presented their recent results in the field of the Electron Devices Society. The presentations were followed by further exchanges on materials science, technology, components and design.

ED Poland

–by Mariusz Orlikowski

On June 19–21, 2014, Lviv, Ukraine, the MIXDES 2014: 21st International Conference "Mixed Design of Integrated Circuits and Systems" will take place. The conference is organized by Lodz University of Technology with Lviv Polytechnic National University. The conference is co-sponsored by the IEEE ED Poland Chapter. So far, four invited papers have been confirmed:

1. Cooperation and Adaptation to Improve the Dependability of Networks on Chips—Jacques Collet (LAAS—CNRS, FRANCE)
2. Magnetic Tunnel Junctions for Future Memory and Logic-in-Memory Applications—Viktor Sverdlov (Technische Universitaet Wien, AUSTRIA)
3. Optofluidic Photonic Liquid Crystal Fibers—Tomasz R. Wolinski (Warsaw University of Technology, POLAND)
4. Ultra Fast X-ray Detection Systems in Nanometer and 3D Technologies—Paweł Gryboś (AGH University of Science and Technology, POLAND)

During the conference there are three special sessions planned:

- Compact Modeling Support for Heterogeneous Systems organized by Dr. Daniel Tomaszewski (Inst. of Electron Technolgy, Poland) and Dr. Władysław Grabiński (GMC Suisse, Switzerland)
- Modeling and Simulation of MEMS for Educational Purposes organized by Dr. Michał Szermer (Lodz University of Technology, Poland)
- xTCA for Instrumentation organized by Dr. Dariusz Makowski (Lodz University of Technology, Poland), Dr. Holger Schlarb (DESY, Germany) and Dr. Stefan Simrock (ITER, France)
- The best papers will be recommended for publication in extended versions in domestic and international journals, e.g. International Journal of Microelectronics and Computer Science supported mostly by IEEE ED Poland Section members.

During the conference a joint meeting of the IEEE ED Poland Chapter, Microelectronics Section of Committee of Electronics and Telecommunication of Polish Academy of Sciences and Electronics and Photonics Commission of URSI Poland is also planned. All people interested in this meeting, in particular all the members of the Polish Section of IEEE, are invited to take part in the event. For more information please refer to http://www.mixdes.org.

~Zygmunt Ciota, Editor

ED/AP/MTT/COM/EMC Tomsk

–by Oleg Stukach

The Siberian Conference on Control and Communications SIBCON-2013, flagship event of the Tomsk Joint Chapter and YP Affinity Group of Russia Siberia Section was successfully held at Siberian Federal University in Krasnoyarsk, Russia. The conference was organized with technical co-sponsorship from MTT-S and ED-S. This is the 10th in the series of conferences since 1995.

The event attracted more than 150 people. The three-day technical program is highlighted by three keynote speeches given by our honorable guests. The technical program consisted of two invited talks and 160 oral papers addressing the current in state of the art for topics relevant to nanotechnology, semiconductor materials, sensors, electron devices, the fundamental problems of communication and control theory. To encourage the participation of young professionals, the conference held a best paper competition. We were honored to have 10 distinguished speakers who gave talks on timely and important topics in the areas covered by SIBCON.

We also included a luxury culture program with sightseeing to Krasnoyarsk landmarks and a visit to the Krasnoyarsk Hydroelectric Power Station dam, which is one of the biggest in the world.

The next SIBCON will be held in May 2015. Please visit the conference

SIBCON-2013 participants

website at http://chapters.comsoc.org/tomsk/sibcon for future information and mark this event on your calendar.

~Tomislav Suligoj, Editor

ED Scotland

–by David Cumming

In association with the National Microelectronics Institute (NMI) and the Electronics, Sensors and Photonics Knowledge Transfer Network (ESP KTN), the Scottish Chapter will be holding a networking event entitled "Electrochemical Deposition." This free to attend, day-long meeting will be held at the University of Edinburgh's King's Buildings Campus on Wednesday April 30th and will combine presentations, a poster session, table top exhibition and the opportunity to network with a wide range of experts from the Electronics Manufacturing community.

Within the Electronics Manufacturing community there has been growing interest in electrochemical deposition, predominantly due to its adoption in a number of advanced technologies including electro-less deposition and electroplating of thick metal layers, the electrodeposition of magnetic alloys used in magnetic information storage technologies, as well as the electrodeposition of multilayer films, which have found many applications in the areas of sensors.

Speakers from industry, academia and trade associations will present the state-of-the-art in electrochemical deposition, and to discuss the challenges and opportunities the field represents. The day will be of interest to those working in CMOS fabrication, electrochemistry, and MEMS/microsystem development, as well as anyone wishing to learn more about next generation processing technologies.

Further details can be obtained by contacting Dr. Jonathan Terry (jonterry@ieee.org)

~ Jonathan Terry, Editor

Asia & Pacific (Region 10)

ED Beijing

–by Jinyan Wang

On October 8, 2013, Prof. Hiroshi Iwai from the Tokyo Institute of Technology visited the ED Beijing Chapter. With the Chapter's arrangement, he delivered an EDS Distinguished Lecture entitled *"Future of Nano CMOS Technology"* in the Institute of Microelectronics of Chinese Academy of Sciences (IMECAS). The lecture, hosted by Prof. Ming Liu from IMECAS, the Vice Chapter Chair, attracted more than 40 local professionals and graduate students from the Beijing Chapter.

Prof. Iwai first introduced the development of CMOS would reach its limits after the next decade because of the difficulties in downsizing and some fundamental limits of MOSFETs and the development of new technologies to pursue the downsizing of CMOS for another decade. He talked about the current status of the frontend of the technology, continuous innovation of High-k/metal gate technologies and recent advances in new channel material such as III-V/Ge. Prof. Iwai also explained that device demonstration on emerging technologies (such as Tunnel FET, Junctionless FET, Carbon-based FET.) was increasing, but we could not draw a successful story to replace the Si-CMOS and more time was needed for implementation of these technologies in future generation devices. The new points of his research on SONOS flash memory devices made a big splash and reached an academic discussion.

After the lecture, a symposium was held with the participating researchers from the Laboratory of Nanofabrication and Novel Device Integration Technology of IMECAS. Both sides introduced their recent works, sparking a heated discussion.

ED Shanghai

–by Yu-Long Jiang

The ED Shanghai Chapter held an event at Fudan University on December 23, 2013, inviting Prof. Steve Chung of National Chiao Tung University (Taiwan) to give an EDS Distinguished Lecture. His presentation was titled, *"The Fundamentals of RTN in Exploring the Dielectric and Reliabilities of Advanced CMOS Devices and Nonvolatile Memories."* He began his talk with an introduction to the basics of Id Random Telegraph Noise (RTN) measurement technique and its applications to the understanding of gate dielectric and device reliability for various types of CMOS devices after the 90 nm generation, including the most recent

Prof. Hiroshi Iwai (lecturer, first row, middle), and Prof. Ming Liu (first row, first from left) with professors and student members

December 23, ED Shanghai talk, (from right) B. Z. Li (former Shanghai Chair), Y. L. Jiang (Chapter Chair), M. F. Li, Steve Chung (EDS DL)

interests in trigate CMOS from a 28 nm generation node, as well as the applications of another Ig-RTN to the SONOS and Resistance RAM. The role of a newly observed RTN behavior, which might lead to the failure of ReRAM was also addressed. There were about 20 attendees and after the presentation, more details on further enhancing the activities in the Shanghai area were discussed.

ED Taipei

–by Steve Chung

The ED Taipei Chapter held two invited talks in the fourth quarter of 2013. The first was held on October 28th at National Chiao Tung University, Hsinchu, with Prof. S. Maikap, from Chang Gung University. Prof. Maikap's talk *"TaOx-based resistive switching memory,"* presented the most recent progress in the use of TaOx as a potential resistance RAM (ReRAM). The bilayer structure and the embedded Nano-crystal were also discussed on the further development of ReRAM. His talk was well attended by more than 90 participants, including students and professors from local universities.

The second talk was arranged on December 6, to invite Prof. Gengchiau Liang from the National University of Singapore. He gave a talk on *"Future Electronics Based On 2D Materials and Their Electronic Applications: A Theoretical Perspective."* Recently, as we reached the end of Moore's law, two-dimensional materials, such as grapheme, MoS2, etc., have been extensively studied and generated considerable interests. In his talk, he first gave the introduction to the current development on the FET-related devices and novel functional devices, followed by introducing the fundamentals of material properties of these advanced 2D materials including graphene and beyond graphene, such as transition metal dichalcogenides (TMDs), silicene, Bi2Se3, etc. Finally, a general modeling procedure, self-consistently solving the Non-Equilibrium-Green's-Function transport formalism and the device electronic structure was discussed. This talk was attended by more than 40 students and 10 professors/researchers.

ED UCAS Shanghai

–by Qiaochu Tang

The ED University of Chinese Academy of Sciences (UCAS) Shanghai Student Branch Chapter held an EDS Distinguished Lecture on December 24, 2013. Prof. Steve S. Chung of National Chiao-Tung University was invited to deliver a talk entitled *"Design Guidelines for High-performance and High-reliability strained CMOS Devices."* Prof. Chung presented strain-induced reliability and the design guidelines for a trade-off between performance and reliability. Various design strategies were compared and sophisticated reliability evaluation techniques were introduced. There were about 15 attendees and the talk aroused heated

ED Taipei, October 28th, S. Maikap (speaker) December 6th, 1st row, left) C. H. Chien (5th), Sam Pan (6th), GC Liang (7th, speaker), Steve Chung (8th, seminar host), H. C Lin (9th)

EDS Distinguished Lecturer, Prof. Steve S. Chung (center, right) at ED University of Chinese Academy of Sciences (UCAS), Shanghai

discussion. As a veteran officer of EDS, Prof. Chung also gave a lot of precious advice to the organization of the student chapter. The UCAS Shanghai Student Chapter (along with IEEE UCAS Shanghai Student Branch) have also held many other events and detailed information can be found at http://zhan.renren.com/edsshanghai.

~ Mansun Chan, Editor

ED Kansai

–by Michinori Nishihara

The ED Kansai Chapter hosted the 13th annual Kansai Colloquium Electron Devices Workshop on October 25, 2013, at Osaka Center of Josho Gakuen, Osaka, Japan. The event attracted 36 participants and 13 excellent papers, with authors from the Kansai area, who also presented at the workshop. The papers were specially selected from (1) major conferences such as IEDM or SSDM and (2) technical papers on electron devices published during the past 12 months. The program was divided into three sections as follows: (1) Nanoelectronics, (2) Power and Compund Semiconductor Devices, (3) Sensor, Solar Cell, and Emerging Devices.

The Award Committee selected two papers from student presenters for the 13th IEEE EDS Kansai Chapter MSFK Award. The winners were Dr. Takashi Matsumoto of Kyoto University for his paper titled, *"Impact of Random Telegraph Noise on CMOS Logic Delay Uncertainty under Low Voltage Operation."*

The Committee also selected one paper for the IEEE EDS Kansai Chapter of the Year Award. The winning paper was *"GaN Gate Injection Transistor with Integrated Si Schottky Barrier Diode for Highly Efficient DC-DC Converters"* by Dr. Tatsuo Morita of Panasonic Corporation.

The presented papers were all excellent and stimulated many questions and discussions with the audience, as they were selected from already qualified papers of major conferences and technical journals. This workshop is playing an important role in encouraging students and young engineers in the industry to extend their technical knowledge and career. The ED Kansai Chapter will continue to serve our members' interest.

We will have an annual international meeting called IMFEDK on June 19–20, 2014, in Kyoto, Japan. Please visit www.imfedk.org for more details.

ED Japan

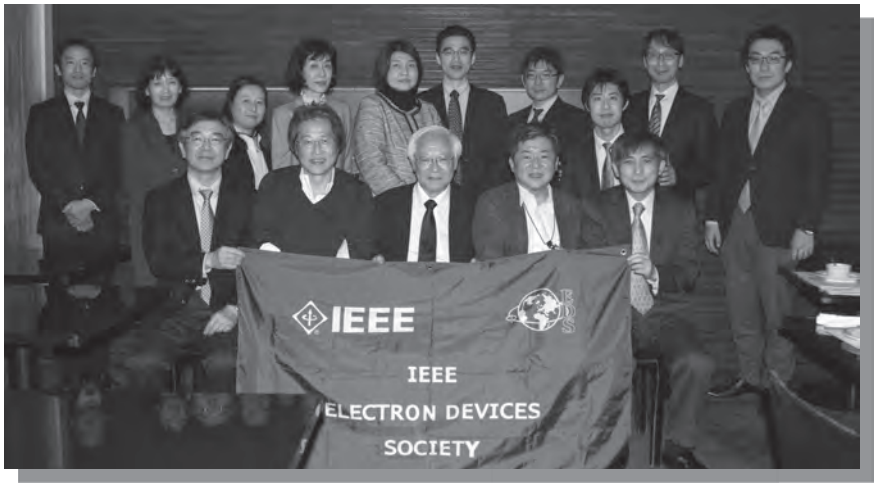
–by Akira Toriumi

On February 3, 2014, the annual meeting of the ED Japan Chapter was held at the University of Tokyo. Prof. Akira Toriumi, Japan Chapter Chair and Dr. Tohru Mogami, the incoming Chapter Chair, reported on 2013 chapter activities and plans for 2014. The 2013 EDS Japan Chapter Student Award (VLSI & IEDM) was presented to 7 students, who made excellent presentations at the Symposium on VLSI Technology 2013 and IEDM 2013. The award winners are posted on the Chapter's webpage; (http://www.ieee-jp.org/japancouncil/chapter/ED-15/ed15_award.htm). The new Executive Committee for 2014 was elected. The following are the new officers for the chapter: Dr. Tohru Mogami, Chair; Prof. Masaaki Niwa, Vice Chair; Dr. Meishoku Masahara, Secretary; and Dr. Takahiro Shinada, Treasurer.

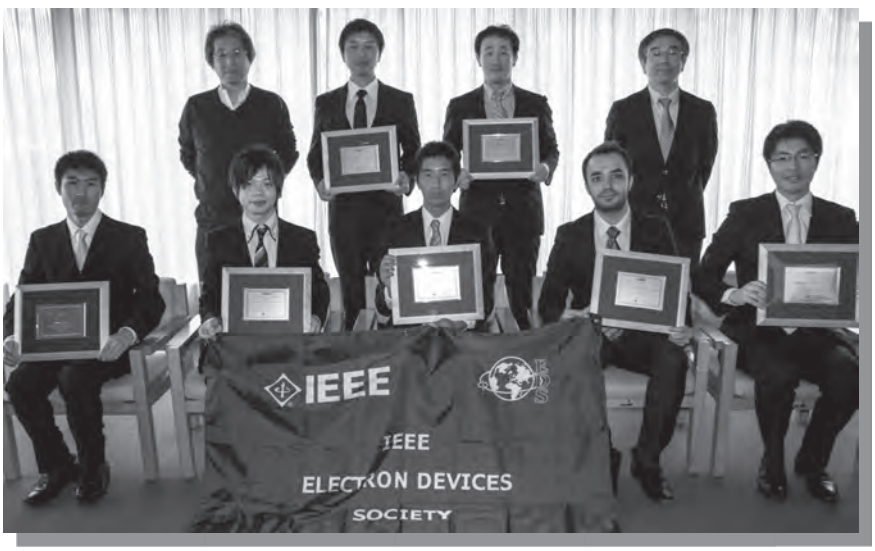
After the annual meeting, the IEDM 2013 Report Session was held, with invited guests: the 6 speakers of the IEDM Report Session, as well as Prof. Hiroshi Iwai, EDS Jr. Past President, Prof. Kuniyuki Kakushima, EDS Newsletter Regional Editor, and Prof. Shinichi Takagi, the 2013

The winners of the 13th MSFK Award and "The Chapter of the Year" at the 13th Kansai Colloquium Electron Devices Workshop: Prof. Yukiharu Uraoka (ED Kansai Chair), Dr. Tatsuo Morita, Dr. Takashi Matsumoto (left to right)

The 13th Annual Kansai Colloquium Electron Devices Workshop Participants



12th EDS Japan Chapter Student Award winners, together with Prof. Akira Toriumi; Chair, and Dr. Tohru Mogami; Vice Chair



ED Japan Chapter's 2014 executive committee meeting

IEEE Andrew S. Grove Award recipient. Nine Japanese members of the IEDM program committee reported on summary, topics and research trends of their sub-committees for more than sixty attendees. This session provided a good opportunity for the attendees to understand the research trends of various areas, especially for those who were not able to attend the IEDM.

~ Kuniyuki Kakushima, Editor

ED/CAS Hyderabad

–by M B Srinivas

The IEEE ED/CAS Hyderabad Chapter organized technical talks and an International Conference PrimeAsia 2013 during the 4th quarter of 2013.

PRIMEASIA 2013 was held December 19-21, 2013, and organized by the Hyderabad Chapter, IEEE Vizag Bay Sub-Section and GITAM University, Vizag. The conference was located in the Beach City of Visakhapatnam, India. As a sister conference of PRIME Europe, PrimeAsia 2013 focused on Digital Design, Analog and Mixed Signal Design, VLSI Process Technology, Nano-Technology, VLSI Routing, DSP, Video Coding and Power Electronics. The 129 paper submissions had a 44 percent acceptance rate and included 42 oral papers presented by authors from India, Canada, UK, UAE, China, Armenia, Norway and Belgium.

The pre-conference tutorials held on December 19, 2013, had a total of over 500 registered attendees. The four half-day sessions were conducted by Prof. Bhim Singh, IIT Delhi; Prof. Shanthi Pavan, IIT Madras; Prof. Rohit Sharma, IIT Ropar, Dr. M.K. Radhakrishnan, NanoRel Singapore; and a parallel full-day tutorial by Diwakar Maurya Xilinx, Hyderabad Design Center. The topics covered included Analog Design, 2D/3D Interconnects, Physical Design and Signoff, Electro Static Discharge Protection and Power Electronics.

The conference on December 20, 2013, was inaugurated by Prof. G. Subrahmanyam, Vice Chancellor, GITAM University followed with a plenary talk by Prof. Franco Maloberti, University of Pavia, Italy on *"Analog Micro Power"* and an invited talk by Dr. MK Radhakrishnan on *"Interfacial Physics in Nano-Electronic Devices."* The third day's plenary talk by Prof. Vijayakrishnan Narayanan of Pennsylvania University, USA, followed by special sessions on

Official release of PrimeAsia proceedings by Dr. M.B. Srinivas, Dr. M. Potharaju, Dr. G. Subramanyam, Dr. Atul Negi and Dr. K. Lakshmi Prasad

'Microelectronics Education' and 'Women in Engineering' that were addressed by Dr. Vazgen Melikyan of Synopsys, Armenia and Dr. Suman Kapur, BITS Pilani.

ED/SP/E/PE Indonesia

Two IEEE EDS Distinguished Lectures were delivered by Prof. Paul R. Berger from Ohio State University, which was held in the School of Electrical Engineering and Informatics, Institute of Technology Bandung, Bandung, Indonesia on August 16, 2013. The morning lecture was entitled *"Plastic Smart Cards Using Quantum Tunneling Electronics"* and the afternoon talk covered *"Manufacturable Passive Millimeter-Wave Imaging Detectors and Nitride Tunneling for Terahertz."* The lectures were hosted by the local IEEE ED Indonesian Chapter and the Microelectronics Center of the Institute. Dr. Basuki Rachmatul Alam and Prof. Ihsan Hariadi were the principle hosts, and the day-long event was keenly attended by the Dean/Prof. Suwarno, Vice Dean and Professors of the School and other local institutions as well as a large number of engineering and science students.

Before presenting lectures on his research work on novel devices and new IC cell topology based on tunneling, Prof. Berger enlightened students upon the benefits of joining IEEE. As a local EDS Chapter Chair and Faculty advisor to two IEEE Student Chapters at OSU, he offered some "best practices" insights to maintaining a vibrant IEEE community. Additionally, Prof. Berger had a chance to deliver an additional DL talk at the school's satellite campus in State Polytechnic of Batam, Batam FTZ Island, Indonesia on August 19, 2013, before crossing the strait and returning to the USA through Singapore. The additional lecture was well attended by the Director, faculty and students of Batam Polytechnic, which has a newly created Microelectronics Manufacturing Teaching factory, with an emphasis on back-end processing.

Prof. Berger talked about membership in the IEEE EDS before faculty and students of Batam Polytechnic as well as FTZ industry

REL/CPMT/ED Singapore

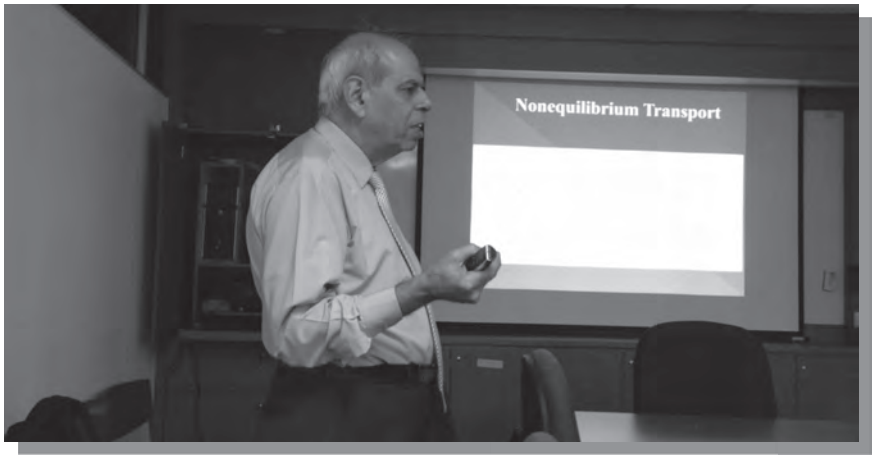
–by Xing Zhou and Yeow Kheng Lim

The REL/CPMT/ED Singapore Chapter organized 3 technical events and 1 social event in the 4th quarter of 2013. The first one was organized on October 31, 2013, by Prof. Vijay Arora of Wilkes University, who is also a distinguished visiting professor at the Universiti Teknologi Malaysia. The DL talk entitled "Carbon: The Soul of Future Nanoelectrnics," was co-hosted by NOVITAS Nanoelectronics Center of Excellence at Nanyang Technological University (NTU).

The second event was jointly organized with the department of Electrical & Computer Engineering (ECE)

Prof. Paul Berger with Dean, faculty and students of SEEI-ITB, Bandung after the Distinguished Lecture

DL talk at NUS, Yee-Chia Yeo, Steve Chung and C-H. Chien (1st row left 3rd, 4th and 5th)



Dr. Vijay Arora giving the DL talk

of National University of Singapore (NUS) on November 22, 2013, hosted by Prof. Yee-Chia Yeo with 2 invited speakers from National Chiao Tung University, Taiwan. The first DL was given by Prof. C. H. Chien on *"High Mobility Ge Channel MOSFETs Directly on Si,"* and the second DL by Prof. Steve Chung entitled *"The Random Dopant Fluctuations of Small Scale CMOS Devices."* The third event on December 13, 2013, was a DL by Dr. John Lau of ITRI, Taiwan, entitled *"Status of TSV Manufacturing,"* which was jointly organized by the NUS department of Mechanical Engineering and hosted by Prof. Andrew Tay of NUS.

ED SJCE - Mysore

–by D. Sushamshushekar and C. R. Venugopal

The IEEE ED SJCE Student Branch Chapter organized various activities to empower students in technical areas with practical training in the second half of 2013. These included Vacation Project Mania, Snap Circuits and Practical Electronics sessions.

Vacation Project Mania VPM 4.0 had three phases. In the first and second phases, students were taught to build basic analog circuits, work on microcontrollers, display devices, Eclipse IDE, etc. The third phase of VPM was a project competition where students came up with ideas and succeeded in providing a working model for the same. This event was a huge success.

Snap Circuits was conducted for students in their second and third year of Engineering. Basic circuits were built using kits, videos were shown and students were taught and allowed to explore these circuits in detail hence, enabling a better understanding of the same. Practical Electronics Sessions are an educative weekly event aimed at improvising the knowledge of student members of the ED SJCE Student Branch. These sessions provided a fundamental approach to students and helped them in developing complex circuits in a step-by-step manner.

~ M.K. Radhakrishnan, Editor

EDS MEETINGS CALENDAR
(As of 28 February 2014)

The complete EDS Calendar can be found at our web site:
http://eds.ieee.org. please visit.

2014 International Caribbean Conference on Devices, Circuits and Systems (ICCDCS) Abstract submission deadline: 10 Jan 2014 Final submission deadline: 21 Feb 2014 Notification of acceptance date: 07 Feb 2014	02 Apr – 04 Apr 2014	Iberostar Quetzal & Tucan Hotel Av. Xaman-Há Fraccionamiento Playacar Playa del Carmen, Mexico
2014 15th International Conference on Ultimate Integration on Silicon (ULIS) Abstract submission deadline: 01 Feb 2014 Final submission deadline: 16 Mar 2014 Notification of acceptance date: 16 Feb 2014	07 Apr – 09 Apr 2014	Stockholm Waterfront Congress Centre, Stockholm, Sweden
2014 IEEE Workshop On Microelectronics And Electron Devices (WMED) Abstract submission deadline: 24 Jan 2014 Final submission deadline: 17 Feb 2014 Notification of acceptance date: 10 Feb 2014	18 Apr – 18 Apr 2014	Student Union Building Boise State University Boise, ID, USA
2014 IEEE International Vacuum Electronics Conference (IVEC)	22 Apr – 24 Apr 2014	Portola Hotel Monterey, CA, USA
2014 International Symposium on VLSI Design, Automation and Test (VLSI-DAT) Abstract submission deadline: 20 Oct 2013 Final submission deadline: 31 Jan 2014 Notification of acceptance date: 31 Dec 2013	28 Apr – 30 Apr 2014	The Ambassador Hotel 188 Chung Hwa Road, Section 2 Hsinchu, Taiwan
2014 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA) Abstract submission deadline: 31 Oct 2013 Final submission deadline: 31 Oct 2013 Notification of acceptance date: 31 Dec 2013	28 Apr – 30 Apr 2014	The Ambassador Hotel 188 Chung Hwa Road, Section 2 Hsinchu , Taiwan
2014 IEEE 6th International Memory Workshop (IMW)	18 May – 21 May 2014	Regent Taipei No. 3, Ln. 39, Sec. 2 ZhongShan N. Rd. Taipei, Taiwan
2014 14th International Workshop on Junction Technology (IWJT) Abstract submission deadline: 31 Jan 2014 Final submission deadline: 01 Apr 2014 Notification of acceptance date: 01 Mar 2014	18 May – 20 May 2014	FuXuan Hotel 400 Guoding Road Shanghai, China
2014 25th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC) Abstract submission deadline: 28 Nov 2013 Final submission deadline: 28 Apr 2014 Notification of acceptance date: 19 Dec 2013	19 May – 21 May 2014	The Saratoga Hilton 534 Broadway Saratoga Springs, NY, USA

2014 IEEE Internatioal Interrconnect Technology Conferencei/Advanced Metallization Conference (IITC/AMC) Abstract submission deadline: 01 Feb 2013 Final submission deadline: 01 Feb 2013 Notification of acceptance date: 08 Mar 2013	20 May – 23 May 2014	DoubleTree by HiltonSan Jose 2050 Gateway Place San Hose, CA, USA
2014 International Conference on electron, Ion, and Photon Beam Technology and Nanofabrication (EIPBN) Abstract submission deadline: 11 Jan 2014 Final submission deadline: 31 Jul 2014 Notification of acceptance date: 14 Apr 2014	27 May – 30 May 2014	Omni Shoreham Hotel 2500 Calvert Street NW Washington, DC, USA
2014 IEEE Radio Frequency Integrated Circuits Symposium (RFIC) Abstract submission deadline: 13 Jan 2014 Final submission deadline: 10 Mar 2014 Notification of acceptance date: 20 Feb 2014	01 Jun – 03 Jun 2014	Tampa Convention Center 333 South Franklin Street Tampa, FL, USA
2014 IEEE International Reliability Physics Symposium (IRPS)	01 Jun – 05 Jun 2014	Hilton Waikoloa Village Waikoloa, HI, USA
2014 IEEE 40th Photovoltaic Specialists Conference (PVSC) Abstract submission deadline: 10 Feb 2014 Final submission deadline: 26 May 2014 Notification of acceptance date: 31 Mar 2014	08 Jun – 13 Jun 2014	Colorado Convention Center Denver, CO, USA
2014 Silicon Nanoelectronics Workshop (SNW) Abstract submission deadline: 01 Apr 2014 Notification of acceptance date: 15 Apr 2014	08 Jun – 09 Jun 2014	Hilton Hawaiian Village Waikiki Honolulu, HI, USA
2014 IEEE Symposium on VLSI Technology	10 Jun – 12 Jun 2014	Hilton Hawaiian Village Honolulu, HI, USA
2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD) Abstract submission deadline: 18 Oct 2013 Final submission deadline: 08 Mar 2014 Notification of acceptance date: 11 Jan 2014	15 Jun – 19 Jun 2014	Hilton Waikoloa Village Waikoloa, HI, USA
2014 20th Biennial University/Government/Industry Micro/Nano Symposium (UGIM) Abstract submission deadline: 14 Feb 2014 Final submission deadline: 30 May 2014 Notification of acceptance date: 31 Mar 2014	15 Jun – 17 Jun 2014	Harvard University Northwest Labs 52 Oxford Street Cambridge, MA, USA
2014 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC) Abstract submission deadline: 21 Feb 2014 Final submission deadline: 15 May 2014 Notification of acceptance date: 15 Apr 2014	18 Jun – 20 Jun 2014	Chengdu, China
2014 IEEE 21st International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA) Abstract submission deadline: 17 Jan 2014 Final submission deadline: 09 May 2014 Notification of acceptance date: 14 Mar 2014	30 Jun – 04 Jul 2014	Marina Bay Sands 10 Bayfront Avenue Singapore

EDS Mission Fund – A Call to Members

The Electron Devices Society (EDS), in partnership with the IEEE Foundation, is proud to announce the establishment of the **IEEE Electron Devices Mission Fund of the IEEE Foundation**. As a new endeavor for the society, this fund will be used to greatly enhance the humanitarian, educational, and research initiatives of EDS by providing members and other constituents of the EDS community with the ability to contribute directly to our mission-driven imperatives, such as EDS-ETC Program and EDS Student Fellowship Program.

EDS's mission is to *promote excellence in the field of electron devices for the benefit of humanity*. As a volunteer-led, volunteer-driven society we pride ourselves on doing the utmost to realize this mission. With the establishment of this fund, all EDS members can play a direct role in this vital work.

Membership in EDS is $18 per year for higher level members. Our affordable membership rates are designed to ensure that money is never a barrier to joining EDS. And we're honored to provide all the benefits of membership at this subsidized rate. However, despite a robust operating budget, the revenue collected from dues is not enough to fully support all our wonderful humanitarian efforts.

About the IEEE Foundation
As the philanthropic arm of the IEEE, the IEEE Foundation is a leader in transforming lives through the power of technology and education. The IEEE Foundation enables IEEE programs that enhance technology access, literacy, and education; supports the IEEE professional community; and inspires the generosity of donors. The IEEE Foundation is qualified under U.S. Internal Revenue Code 501(c)(3). Charitable contributions to the IEEE Foundation are tax deductible to the fullest extent allowed by law in the United States. For other countries, please check with your local tax advisors. To learn more, visit www.ieeefoundation.org.

Therefore, to our members who are able to give more than just the cost of membership, especially those who no longer pay dues to be a part of EDS, please consider contributing to the **EDS Mission Fund**.

Donating is simple. Just go to the IEEE Foundation Online-giving page at www.ieee.org/donate, choose your donation amount, and select "**The IEEE Electron Devices Mission Fund**" in the "Designations" pull down menu. If you prefer to write a check, please make it payable to the **IEEE EDS Mission Fund of the IEEE Foundation** and mail it to the IEEE Foundation, 445 Hoes Lane, Piscataway, NJ, 08854, USA. 100% of your donation will be used exclusively for the humanitarian, educational, and research initiatives of EDS.

Contact EDS executive director Christopher Jannuzzi at c.jannuzzi@ieee.org for more information. To explore other ways to support the **EDS Mission Fund of the IEEE Foundation**, contact the IEEE Foundation at donate@ieee.org.