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TECHNICAL BRIEFS

SSI-LED MADE BY IC COMPATIBLE FAB PROCESS AND MATERIALS

YUE KUO

The lighting function affects everyone's daily life. Table 1 summarizes properties of the 3 most popular commercial lighting devices. The incandescent bulb was invented about 140 years ago, has the lowest cost and emits the warm white light most comfortable for human vision. It suffers from the low efficiency and short lifetime. The fluorescent bulb has a higher efficiency and longer lifetime. However, it contains toxic chemicals, often flicks during operation, and emits the multiple wavelength light with low color rendering index (CRI). The semiconductor based light emitting device (LED), which has a diode structure, has the highest efficiency and longest lifetime. However, the price is high because it is made of single crystal semiconductor films epitaxially grown by the complicated metal organic chemical vapor deposition (MOCVD) process on the expensive single crystal substrate. Due to the limit of the band gap energy, only the narrow band light is emitted from this type of device. For the white light emission, three different types of devices or one short wavelength emitting device with a phosphor layer has to be used.

It is desirable to have a light emitting device made of the IC compatible material. However, since silicon (Si) is an indirect band gap material, it cannot emit the light under the electric stress condition. The nanocrystalline silicon can emit light but the wavelength is critically dependent on the crystal size and the lifetime can be short. Recently, a new type of white light emitting device that is made of the completely IC compatible material and fabrication process has been reported. It has attracted great interests in the scientific community, for example, the first paper published on the *Applied Physics Letters* (March 2013) was selected as a Research Highlight and downloaded for 1,000 times within 2 weeks. Publications on this kind of device have been selected to the cover page of

(continued on page 3)

YOUR COMMENTS SOLICITED

Your comments are most welcome. Please write directly to the Editor-in-Chief of the Newsletter at radhakrishnan@ieee.org

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NEWSLETTER DEADLINES

| ISSUE | DUE DATE |
|---------|-------------|
| January | October 1st |
| April | January 1st |
| July | April 1st |
| October | July 1st |

The EDS Newsletter archive can be found on the Society web site at <http://eds.ieee.org/eds-newsletters.html>. The archive contains issues from July 1994 to the present.

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SSI-LED MADE BY IC COMPATIBLE FAB PROCESS AND MATERIALS

(continued from page 1)

the *J. Vacuum Science and Technology B* (January/February 2014) and the Tech Talk of the *IEEE Spectrum* (12/24/2014). Since the light emission principle of this new device is similar to that of the incandescent light bulb, it is named the solid state incandescent LED (SSI-LED).

The SSI-LED has a simple MOS structure containing a thin metal oxide film sputter deposited on a p-type Si wafer. The top electrode is made of a film of transparent conductive oxide, such as ITO. The oxide film can be embedded with a nanocrystal layer. The complete thin film stack is deposited by the one pump down sputter process followed by the rapid thermal annealing.

Figure 1 shows the typical J - V curve of a SSI-LED. In the low voltage range, it behaves like that of a typical high- k gate dielectric, i.e., the Schottky emission mechanism first and then the Poole-Frenkel mechanism with the increase of the voltage. After the dielectric breakdown, the device behaves like a resistor following the Ohm's law and light is emitted. The sharp dielectric breakdown was only observed under the hole-injection condition, i.e., in the negative gate voltage range for the p-type Si wafer, not under the electron injection condition. Figure 2 shows the emission spectra of SSI-LEDs made of various types of oxide films. They all cover

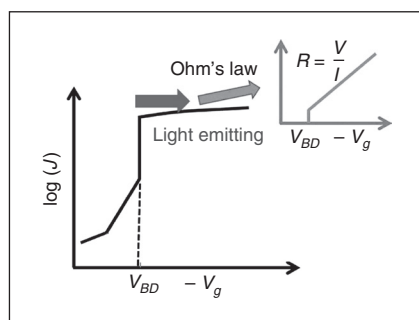


Fig. 1. J - V curves of a SSI-LED.

Table 1. A list of 3 popular commercial lighting devices

| | Incandescent bulb | Fluorescent bulb | Semiconductor based LED |
|---------------------|-----------------------|--|--|
| Size | Bulky | Bulky | Compact |
| Response time | Fast | Slow | Fast |
| Power consumption | High | Low | Low |
| Efficiency | Low | Medium | High |
| Lifetime | 2,000 hr | 10,000 hr | 50,000 hr |
| Emission spectrum | Broad band | Multiple narrow bands | Single narrow band |
| Materials in device | W, Ar, N ₂ | Hg, Tb, Eu ³⁺ :Y ₂ O ₃ , etc. | GaAs, InGaN, Ce ³⁺ :YAG, etc. |
| Fabrication process | Simple | Medium | Complicated |
| Product price | Low | Medium | High |

the whole visible and part of the infrared wavelength range with the peak located in the red region. The intensity of the light is influenced by the original dielectric material, thickness, and thermal history. The emitted lights have large color rendering indices (CRI's) of 95–98, high color correlated temperatures (CCTs) of 2,500–3,000K, and small chromaticity distances to the Planckian loci. They are located in the warm white

light region of the CIE diagram near the conventional incandescent light, as shown in Figure 3. Therefore, the light emission phenomenon is close to that of the black body emission. Light emission was observed under the DC, AC, or rf driving condition.

The dielectric layer is broken down at many different locations in the dielectric stack each of which becomes a conductive path. During the passage of a large current, the

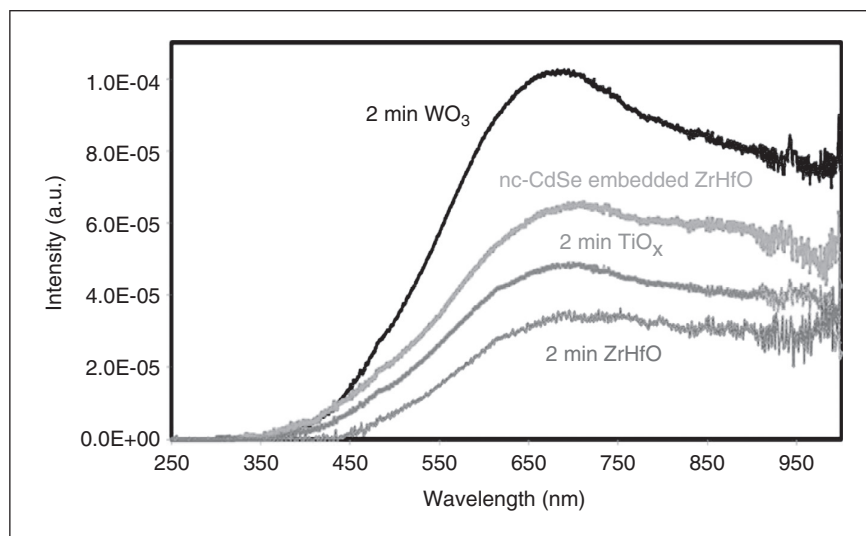


Fig. 2. Emission spectra of various SSI-LEDs.

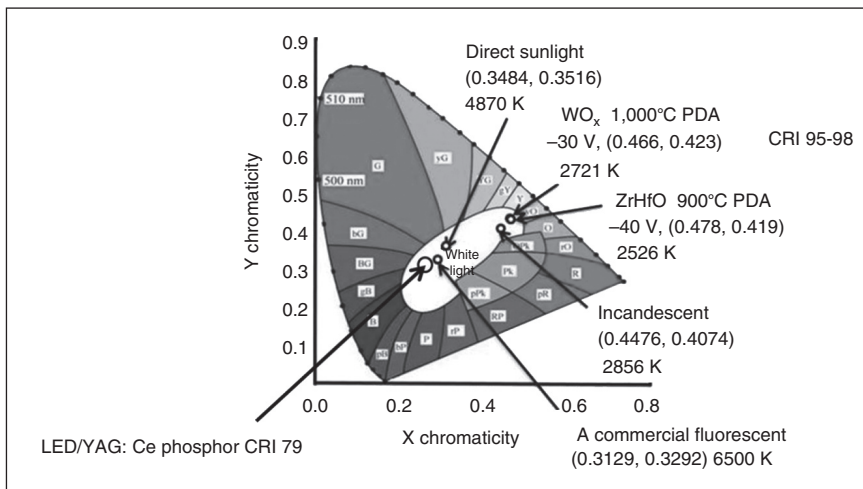


Fig. 3. CIE diagram of lights from SSI-LEDs, an incandescent bulb, a fluorescent bulb, a conventional LED, and sunlight.

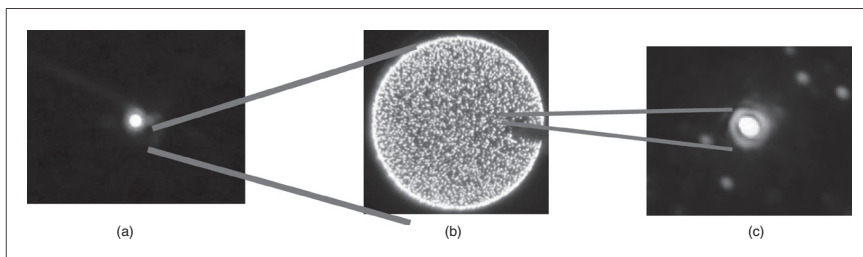


Fig. 4. (a) a low magnification and (b) a high magnification photo of a 300 μm diameter SSI-LED, and (c) an enlarged view of a bright dot.

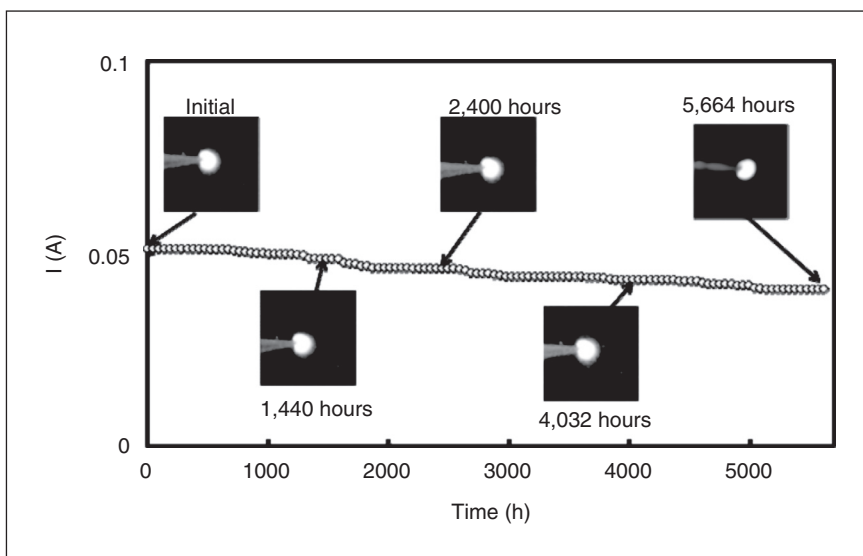


Fig. 5. Leakage current vs. time of an nc-CdSe embedded ZrHfO SSI-LED.

i.e., varying from less than 20 nm diameter to larger than 150 nm and the number increases with the increase of the size.

The lifetime of this kind of device is very long because the conductive paths are surrounded by the high quality dielectric film, which prevents the contact with air. For example, an nc-CdSe embedded ZrHfO SSI-LED has been continuously operated for more than 9,000 hours without failure. Figure 5 shows the change of the leakage current with time in the first 5,664 hours of operation, which includes selected photos of the device at different times. The density of the emitted light, especially in the short wavelength range, reduced slightly with time. It does not show the “droop” failure phenomenon that often occurs in the conventional single crystal based LED because the conductive paths are formed in the amorphous metal oxide film.

The efficiency of a conventional incandescent lamp is inversely proportional to the width and length of the filament. If the same principle is applicable to the SSI-LED that contains the nano size conductive paths, the efficiency should be very high. Based on a rough estimation method, i.e., by dividing the energy of the emission spectrum in 200 nm – 1,000 nm range measured at a distance of 2 mm from the ITO electrode with the input energy, the conversion efficiency is less than 1%. Many methods can be used to improve the efficiency, for example, applying new materials, structures, fabrication processes, and driving schemes.

The cost of the SSI-LED is very low because it is fabricated using the IC compatible materials and processes. This kind of device is applicable to many products, such as lighting, the light source of the on-chip optical interconnect, micro displays, biomedical instruments, and components for novel commercial and defense systems.

conductive paths are thermally excited to a high temperature and then emit light, as shown in Figure 4(a), (b), and (c). The nano dot light emit-

ting pattern is different from the uniform light emitting pattern of the conventional semiconductor based LED. The nano dots are of different sizes,



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erties, and fabrication processes in TFTs, ICs, and novel applications. His work has resulted in many world records and technology breakthroughs that solved the decades-long problems in the solid state field with significant impacts to the production. Dr. Kuo has authored a large number of high impact papers, held patents, and edited journals, conference proceedings, and books. Dr. Kuo is a well-recognized technology leader who has served in committees and conference organizations/chairing for IEEE and other professional societies. He is the founder and key organizer of the world longest, continuously

held TFT conference as well as the ULSIC vs. TFT meeting series. He has served on boards, panels, advisor committees for US National Academies, universities, industry, and governments, globally. Dr. Kuo's honors include Fellow of IEEE, Fellow of ECS, 2015 Gordon E. Moore Medal, ECS Electronics and Photonics award, IBM awards, IEEE EDS Distinguished Lecturer, Distinguished Research and Innovation Awards of Texas A&M University, honorary visiting professors, plenary/keynote/invited speaker, and a large number of most downloaded/cited/highlighted/best paper awards. (contact e-mail: yuekuo@tamu.edu)

INTERNATIONAL YEAR OF LIGHT

Light-based technologies have the potential to transform the 21st Century as electronics did in the 20th Century. Inspired by the crucial role light plays in modern life, the United Nations proclaimed 2015 the International Year of Light and Light-based Technologies (IYL 2015). The global initiative is showing how light provides solutions to worldwide challenges in energy, education, agriculture, communications, and health.

The IEEE Photonics Society, founding partner of the IYL 2015, will support coordinated activities on national, regional, and international levels. Under the initiative, the IEEE Photonics Society will:

- introduce undergrad and pre-university students to the light sciences by organizing summer schools, Student Outreach Ambassador programs and young scientist workshops throughout the year.
- hold various events, such as career workshops, networking



INTERNATIONAL YEAR OF LIGHT 2015

- receptions and an "Introduce a Girl to Photonics Day," through the Women in Photonics program.
- participate in an IYL 2015 Chapter Challenge grant competition to raise awareness and participation at the local level.

- team with Solar Aid, a nonprofit dedicated to ensuring access to safe, clean solar lights in Africa. The IEEE Photonics Society is supporting the effort to eradicate the kerosene lamp by 2020. As such, they have started a "Speed of Light" social giving campaign that allows participants to donate a solar lamp and then connect with friends through an online social community.
- sponsor the Stevens Institute of Technology's "Sure House" design, based on the need for sustainable and resilient coastal houses in the Mid-Atlantic United States affected by Hurricane Sandy, in the U.S. Department of Energy's Solar Decathlon. The goal is to increase demand for intelligent, sustainable environments, like Smart Living Spaces.

For information on IYL 2015, visit the initiative's web site and blog, at <http://www.light2015.org/Home.html> and <http://light2015blog.org/>.

UPCOMING TECHNICAL MEETINGS

THE 2015 IEEE COMPOUND SEMICONDUCTOR IC SYMPOSIUM (CSICS)

OCTOBER 11-14 IN NEW ORLEANS, LOUISIANA

PAPER SUBMISSION DEADLINE: 17 APRIL 2015



We cordially invite you to the 2015 IEEE Compound Semiconductor IC Symposium (CSICS) being held October 11-14 at the Sheraton Hotel located in New Orleans, Louisiana, USA. Since its inception in 1978, the Symposium has become a pre-eminent international forum for developments in compound semiconductor circuit and device technology. The scope of the Symposium encompasses devices and circuits, embracing GaAs, SiGe, InP, GaN, InSb, and CMOS technology to provide a truly comprehensive conference. CSICS is the ideal forum for presenting the latest results in microwave/mm-wave, high-speed digital, analog, mixed mode, THz, power conversion, and optoelectronic integrated circuits.

The 2015 CSIC Symposium is comprised of a full 3-day technical program, two short courses, a primer course, and a technology exhibition. The technical program includes approximately 60 high quality technical papers. Invited papers and panel sessions on topics of current importance to the Compound Semiconductor IC community greatly enrich the technical program. In addition, the Symposium will continue the tradition of including important "late breaking news" papers. The short courses on Sunday, October 11th provide the



PHOTO COURTESY OF THE NEW ORLEANS SHERATON HOTEL

attendees the opportunity to learn from world-renowned instructors in their respective areas of expertise. The Sunday introductory-level primer course will provide attendees insight into the design of principal RF and high speed IC building blocks, emphasizing the specific background needed to understand and appreciate the technical program.

The technology exhibition will be held on Monday and Tuesday, featuring informative and interesting displays with corporate representatives on hand. The list of exhibitors can be found in the CSICS advance program to be published in late June. To complement the Symposium, there are several social events including the

Sunday Evening CSICS Opening Reception, the Monday CSICS Exhibition Opening Reception, and the Tuesday CSICS Exhibition Luncheon. Breakfasts and coffee breaks will be served on Monday, Tuesday, and Wednesday.

For registration and up-to-date information please visit the CSICS website at www.csics.org. Further questions may be addressed to the Symposium Chair: Charles Campbell, telephone: +1 972-994-3644, Email: Charles.Campbell@Qorvo.com.

We hope you can attend,
2015 IEEE CSICS Organizing Committee

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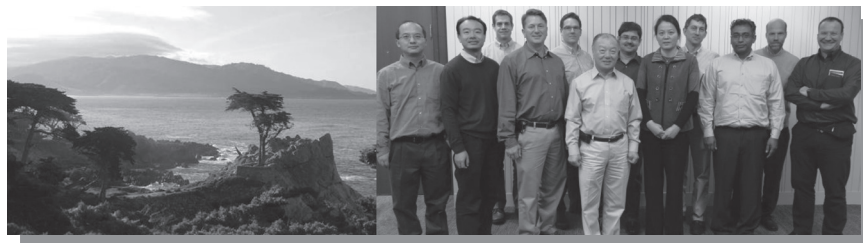
2015 IEEE INTERNATIONAL RELIABILITY PHYSICS SYMPOSIUM (IRPS)

APRIL 19-23 *HYATT REGENCY MONTEREY RESORT AND SPA *MONTEREY, CALIFORNIA, USA

The 2015 IRPS conference has been finalized with 94 platform presentations, 14 invited talks, and 73 posters by a globally well-represented 156 technical program committee members and chairs. The opening keynotes will be given by Kaizad Mistry (Intel) and Brent Keeth (Micron), with details posted already on Facebook. The technical program will then commence with three parallel tracks; a listing of the accepted abstracts is posted with the program in review <http://irps.org/program>. The conference has 15 technical areas which encompass the entire reliability area of semiconductors. Unique to this year's conference is a focus on dielectric breakdown where we have created a new session with transistor breakdown and the backend dielectric presentations to encourage new thought.

Why IRPS?

We've mentioned previously that IRPS is also the only comprehensive reliability conference covering the breadth of device reliability from time dependent dielectric breakdown testing and models to compound device reliability to interconnect electromigration to soft error to electronic system reliability to process integration to chip-package interaction. The conference begins with two days of tutorials plus reliability year in review. Tutorials are divided into three tracks (technology, component and system), with seven sessions in each track category. The traditional front end and back end will be complemented by middle-of-line reliability. A few examples of new topics are self-heating effects, stats in reliability & returns analysis, system level design for reliability, and static random access memory wafer level reliability. The topic list, along with instruc-



Beautiful Monterey- a great place for a conference | Technical Program Committee Meeting
December 2014

tor biography and abstract can be found on <http://irps.org>. This conference is ideal for industry professionals to both broaden and deepen their knowledge while networking with others, whether just starting their career or a seasoned reliability veteran. It is also ideal for students to discover the exciting area of reliability engineering!

Pre-Conference Highlights

We want EDS members to know the selected presentations for highlight prior to the conference which were chosen by the technical program committee. The first is from the transistor reliability session by Kerber et al, titled "*Impact of RTN on stochastic BTI degradation in scaled Metal Gate / High-k CMOS technologies.*" In this work, the authors propose that random telegraph noise (RTN) and negative bias temperature instability (NBTI) have different origins as RTN exhibits no change after NBTI stress. The second highlight is from the circuit aging and reliability session from Lu et al, "*Long-term data for BTI degradation in 32nm IBM microprocessor using HKMG technology.*" This paper details a circuit sensor design to measure and separate NBTI and positive bias temperature instability (PBTI) effects. The sensor can measure BTI degradation at the circuit infant stage rather than after manufacturing test to give high accuracy.

And lastly, the soft error highlighted presentation is by Lee et al, titled "*Radiation-Induced Soft Error Rate Analyses for 14 nm FinFET SRAM Devices.*" This paper has a detailed study of soft errors due to high energy cosmic ray neutrons, alpha particles, and thermal neutrons at multiple planar CMOS process nodes, and the 14 nm FinFET node. Transitioning to FinFETs greatly improves the soft error rate. However, the thermal neutron soft error component decreases less than the high energy cosmic ray neutron and alpha particle components, so thermal neutrons become a larger contributor at 14 nm.

Please take advantage of registration now for lower conference fees and follow us on Facebook, LinkedIn, Twitter @IEEEIRPS, or visit <http://irps.org> for the latest information. We look forward to seeing you in Monterey!

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2015 SYMPOSIUM ON VLSI TECHNOLOGY

The 35th Annual Symposium on VLSI Technology will be held from **June 15–18, 2015**, at the Rihga Royal Hotel Kyoto, Kyoto, Japan. This symposium is jointly sponsored by the Japan Society of Applied Physics (JSAP) and the IEEE Electron Devices Society (EDS) in cooperation with the IEEE Solid-State Circuits Society. This conference is highly regarded as one of few premiere international conferences on semiconductor technology. One of the unique aspects of this conference is that it is held jointly with the Symposium on VLSI Circuits (June 16–19) at the same location. A single registration fee covers both the events. The overlap in the symposia schedules and location offers an open forum for interactions between technologists and circuit & system designers.

Symposium scope includes new concepts and breakthroughs in VLSI technology including:

- Memory, Logic, RF, Analog, Mixed-Signal, I/O, High-Voltage, Imaging, MEMS, integrated sensors, and SOC (system-on-chip)
- Advanced gate stacks, channels, source/drain junctions and contacts
- Heterogeneous integration of non-Si materials/substrates on Si substrates
- Advanced lithography and high-density VLSI patterning technologies
- Beyond-CMOS functional devices with a path for VLSI implementation
- Interconnect scaling and Cu alternatives; chip-to-chip including optical interconnects
- Packaging technologies, through-silicon-vias (TSVs) and 3D-system integration
- Advanced materials, device analysis, and modeling
- Theoretical understanding, operation fundamentals and reliability issues related to the above devices



Kyoto, Japan

- VLSI manufacturing concepts, technologies and yield optimization

In recent years, the Symposium on VLSI Technology has placed a strong emphasis on **Design Enablement** (how new devices, process and materials technologies impact VLSI circuit design and their implications for product performance and cost).

In 2015, the conference will offer joint Technology and Circuits focus sessions comprising invited and contributed papers in the following special areas:

- **Ultra Low Power for IoT:** Technology & design co-optimization for improved performance, yield, reliability, ultra-low voltage/power operation, density, and cost
 - **Emerging NVM (ReRAM, PCRAM, STT-MRAM):** Discrete and embedded NVRAM (Flash, ReRAM, PCRAM, STT-MRAM, etc.) technology/design co-optimization
- In addition, two technology focus sessions will cover the following special areas of interest
- **7 nm Logic Technology and beyond:** Impact of advanced

devices, structures, materials and interconnects on digital circuit performance, power, density; device design & process / technology optimization for analog / mixed-signal circuits

- **3D Systems and Packaging:** 3D-technologies and system co-optimization; power delivery and management; thermal management; inter-chip communications including TSVs.

The joint evening panel discussion of June 16th will be on the “Semiconductor Industry 2020.” This is a very timely topic that should capture the interest of technologists, designers, business managers and analysts alike. This joint panel discussion will complement the other technology panel discussing the post scaling issues, another timely topic among the technical VLSI community.

The Symposium will be preceded by a one-day short course on “More than Moore” and “More Moore” for the Internet of Things given by experts from academia and industry on June 15th.

In addition, two satellite workshops will be held before the conference.

The "Silicon Nanoelectronics" workshop will be held on June 14–15, 2015. This workshop is sponsored by the IEEE Electron Devices Society. The second workshop, the 2015 Spintronics Workshop will focus on "VLSI-implementable Spintronics Technology" will be held on June 15, 2015, also at the same location.

Symposium on VLSI Technology is recognized by its spirit of international collaboration and its informal atmosphere, promoting discussion and debate on new ideas and technology directions. The Symposia location alternates between the United States and Japan, giving it a true international setting.

The 2015 venue in Kyoto, Japan, offers many attractive aspects of Japanese culture, such as natural scenery, temples, shrines, towns and homes intermingling with a poignant historical beauty. A banquet hosted by the symposia offers attendees an opportunity to enjoy various Japanese foods and tradition. The Rihga Royal Hotel Kyoto, located

near Kyoto station, offers both traditional and modern style hotel stay and is convenient to go anywhere in Kyoto. The hotel is easily accessible by 10-minute walk or by shuttle bus from Kyoto station.

For further information, please visit the Symposium website at <http://www.vlsisymposium.org> or contact the following conference secretariats:

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We cordially invite you to attend the 2015 Symposium on VLSI Technology to learn about recent state-of-the-art advancements in IC technology and to take advantage of enriching technical interactions.

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Authors: Rais-Zadeh, M.; Gokhale, V.J.; Ansari, A.; Faucher, M.; Théron, D.; Cordier, Y.; Buchailot, L.
- **Multicamera Laparoscopic Imaging With Tunable Focusing Capability**
Authors: Kanhere, A.; Van Grinsven, K.L.; Chi-Chieh Huang; Yen-Sheng Lu; Greenberg, J.A.; Heise, C.P.; Yu Hen Hu; Hongrui Jiang

SOCIETY NEWS

CALL FOR NOMINATIONS FOR EDITOR-IN-CHIEF IEEE TRANSACTIONS ON ELECTRON DEVICES

For more than 60 years, the IEEE Transactions on Electron Devices (T-ED) has been a flagship publication of the IEEE Electron Devices Society (EDS). T-ED publishes original and significant contributions relating to the theory, modeling, design, performance and reliability of electron and ion integrated circuit devices and interconnects, involving insulators, metals, organic materials, micro-plasmas, semiconductors, quantum-effect structures, vacuum devices, and emerging materials with applications in bioelectronics, biomedical electronics, computation, communications, displays, microelectromechanics, imaging, micro-actuators, nanoelectronics, optoelectronics, photovoltaics, power ICs and micro-sensors. TED publishes regular full-length papers, review papers, invited papers, and special issues. The average publishing cycle time is 16 weeks.

We invite nominations for the position of Editor-in-Chief (EiC) for T-ED for a 3-year term beginning in the second half of 2015. The EiC's duties include appointing Editors to serve across the scope of the journal; supervising the operations of the journal through ScholarOne Manuscripts with the assistance of the EDS publications staff; monitoring the quality and timeliness of publications; and leading development to strengthen the journal.

Criteria for the Nominees:

- Ability and motivation to spend sufficient time on the job;
- Demonstrated competence in at least one of the disciplines included in the EDS field of interest;
- Formal support from the institution for which the nominee works (waived if self-employed);
- Has served or currently is serving on one of the editorial boards of T-ED, EDL (the IEEE Electron Device Letters), or J-EDS (the IEEE Journal of the Electron Devices Society);
- Suitable temperament (ability to work at all levels: editorial boards, IEEE/EDS staff, volunteers, authors, reviewers, officers, etc.) and judgment;
- Be a member of EDS;
- Other desirable qualifications include leadership experience, integrity and ethical standards, organizational and management skills, and a vision for moving the journal to a new level of excellence.

Requirement for Nominations:

- A brief IEEE-style biography (up to 250 words) of the nominee;
- A complete CV and list-of-publications of the nominee;
- A brief statement from the nominator on nominee's qualification and how the nominee meets the criteria listed above;
- A letter from nominee's employer indicating support for the EiC activity;
- No specific requirement on the nominators and self-nominations are permissible;
- Endorsement from two EDS members on the nomination;
- Optionally, a statement (up to 500 words) from the nominee on his/her vision for the journal.

Please email the nomination materials to: Marlene James (m.james@ieee.org) by **April 30, 2015**.

*Bin Zhao
VP of Publications and Products
IEEE Electron Devices Society*

CALL FOR NOMINATIONS FOR EDITOR-IN-CHIEF IEEE ELECTRON DEVICE LETTERS

Since 1980, the IEEE Electron Device Letters (EDL) has been a flagship publication of the IEEE Electron Devices Society (EDS). EDL publishes original and significant contributions relating to the theory, modeling, design, performance and reliability of electron and ion integrated circuit devices and interconnects, involving insulators, metals, organic materials, micro-plasmas, semiconductors, quantum-effect structures, vacuum devices, and emerging materials with applications in bioelectronics, biomedical electronics, computation, communications, displays, microelectromechanics, imaging, micro-actuators, nanoelectronics, optoelectronics, photovoltaics, power ICs and micro-sensors. EDL offers a forum for rapid dissemination of significant original research with an average publishing cycle time 7 weeks.

We invite nominations for the position of Editor-in-Chief (EiC) for EDL for a 3-year term beginning in the second half of 2015. The EiC's duties include appointing Editors to serve across the scope of the journal; supervising the operations of the journal through ScholarOne Manuscripts with the assistance of the EDS publications staff; monitoring the quality and timeliness of publications; and leading development to strengthen the journal.

Criteria for the Nominees:

- Ability and motivation to spend sufficient time on the job;
- Demonstrated competence in at least one of the disciplines included in the EDS field of interest;
- Formal support from the institution for which the nominee works (waived if self-employed);
- Has served or currently is serving on one of the editorial boards of EDL, T-ED (the IEEE Transactions on Electron Devices), or J-EDS (the IEEE Journal of the Electron Devices Society);
- Suitable temperament (ability to work at all levels: editorial boards, IEEE/EDS staff, volunteers, authors, reviewers, officers, etc.) and judgment;
- Be a member of EDS;
- Other desirable qualifications include leadership experience, integrity and ethical standards, organizational and management skills, and a vision for moving the journal to a new level of excellence.

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Please email the nomination materials to: Marlene James (m.james@ieee.org) by **April 30, 2015**.

Bin Zhao
VP of Publications and Products
IEEE Electron Devices Society

MESSAGE FROM THE EDS PRESIDENT-ELECT



Samar Saha
EDS President-Elect

The IEEE and Electron Devices Society (EDS) is a volunteer-driven volunteer-led technology-centric organization. The strength of EDS is its members who are the top professionals in their fields. For a society focused on members, responsiveness to our members' inquiries and facilitate their professional growth are vital to the success of EDS. It is true! the social networking is vital in the operation of any modern dynamic technical community. We should harness its power, using the collaboration tools to support technical communities, to be more responsive to members' queries. And, to facilitate members' professional growth, EDS will continue to provide sponsored and co-sponsored publications and Newsletter for interactive communications. At EDS, we value each one of our members, our profession, and the public. We are committed to create opportunities for each one of EDS members to have access to individualized tools, products, and services that support professional growth and career security so that EDS brand provides increased recognition and prestige for our profession worldwide.

IEEE is a truly global organization and EDS is a part of it. We continue to successfully provide new ways of knowledge distribution that create

and deliver knowledge by combining traditional papers with open access publications, conferences, distinguished lectures, mini-colloquia, webinars, and so on – all to enrich knowledge content. In EDS, we have created a structure and culture of innovation, one that proactively identifies new markets and potentially disruptive innovations and encourages diversity, experimentation, risk taking, and collaboration.

The technology is evolving continuously and so does our field-of-interest (FOI). EDS must become a dynamic organization of technical community within its FOI. We must quickly organize new community around emerging technologies and interests. It will share insights more quickly and broadly within the EDS community. Its publications will be enhanced with interactive discourse for which social networking will be the media. The future EDS will provide better mission fulfillment and better member satisfaction. In EDS, we will persistently focus on strengthening our technical communities and will strongly support the development of the information-technology ecosystem needed to support them. The key to the continued success of the new dynamic EDS community is our members.

In EDS, each and every member is the same and has the same privilege to serve in the technical as well as in governing body depending on their interests irrespective of the geographical distance and cultural diversity. It is encouraging that the

EDS members have taken active participation in the 2014 December general election. Elected or not, each member is encouraged to actively participate in EDS activities, propose new emerging technical area and committee in the EDS FOI.

The dynamic EDS community's aim must be high – pledge to *change the world*. The world is facing tough challenges: vagaries of nature – record high magnitude earthquake and quake-battered Haiti, drought in the western USA and severe snow fall in the east; medical crisis in West Africa – Ebola outbreak; energy shortage around the globe; water shortage in the horizon; and so on. It is our responsibility to engage in research and development to mitigate these challenges. And, I strongly believe that the highly talented, creative, and innovative EDS community will stand up to these challenges and truly *change the world*!

Samar Saha
EDS President-Elect
Ultrasolar Technology
Milpitas, CA, USA

(Samar Saha, the President-Elect of IEEE EDS is the Technical Advisor of Ultrasolar Technology, Santa Clara, CA, USA. He is an internationally recognized expert on IC device architecture within the industry and academia and his recent publication 'Compact Models for Integrated Circuit Design: Conventional Transistors and Beyond' a book on compact modeling.)

MESSAGE FROM EDS VICE PRESIDENT OF PUBLICATIONS AND PRODUCTS



Bin Zhao
EDS Vice President
of Publications and
Products

The journals and periodicals sponsored by the Electron Devices Society (EDS) provide comprehensive coverage and breaking news in Electron Devices and the related technologies as described in the field-of-interest (FOI) for

EDS. I am very pleased to have this opportunity to update you on the latest progress, accomplishments, and key initiatives in EDS publications.

Our flagship journals, the *IEEE Transactions on Electron Devices* (T-ED) and the *IEEE Electron Device Letters* (EDL), continue to do well under the leadership of corresponding Editor-in-Chiefs (EiCs), John Cressler (T-ED EiC), Paul Yu (T-ED Interim EiC), and Amitava Chatterjee (EDL EiC), and with the outstanding work and critical contributions from the T-ED and EDL Editorial Boards, the reviewers, and the EDS editorial staff. The average publishing cycle time has been reduced to 16 weeks for T-ED and to less than 7 weeks for EDL, which are among the fastest of all the IEEE Transactions and the IEEE Letters, respectively. The value and importance of T-ED and EDL in helping researchers and engineers around the globe access the needed information are manifested by the usage of published papers. Based on the paper download statistics from IEEE Xplore, T-ED is ranked among the top 10 in paper downloads of all IEEE publications, while EDL has the most downloaded papers in the Letters publications. In September 2014, we successfully completed the 5-year review by the IEEE Technical Activities Board (TAB) in T-ED, EDL and the *IEEE Transactions on Device and Materials Reliability* (T-DMR, EiC: Tony Oates). While we thank the

TAB Periodicals Committee for their very positive feedbacks and constructive suggestions, I would like to specially thank the EiCs, Christopher Jannuzzi (EDS Executive Director), and the EDS editorial staff for their great work in such a thorough review which helps to ensure our continued leadership and success in these publications.

In response to the recent increased demand for open access (OA) publishing, EDS launched the *IEEE Journal of Electron Devices Society* (J-EDS) in 2013 under the leadership of its first EiC, Renuka Jindal. J-EDS is aimed to publishing high quality papers in the FOI for EDS and in a fully open access format. From J-EDS first-year's operation, we noticed that the papers submitted and published were substantially less than what we originally planned. This phenomenon was reviewed by the EDS Publication and Products Committee and at the EDS Presidents Strategy Meeting in early 2014. From April 2014, we started a few initiatives for J-EDS, including identifying hot topics suitable for JEDS and planning special issues accordingly, enhancing J-EDS Editorial Board in both technical areas and geographical representation, promoting OA as an alternative publication to meet various needs from authors and readers. As a result, the number of papers accepted for publication in 2014 was doubled in comparison to that in 2013 for J-EDS. We look forward to harvesting more positive results from these initiatives.

In addition to T-DMR, EDS also co-sponsors over a dozen leading journals, including the *IEEE Journal of Photovoltaics* (J-PV), the *Journal of Microelectromechanical Systems* (J-MEMS), the *IEEE Transactions on Semiconductor Manufacturing* (T-SM), and the *Journal of Display Technology* (J-DT), just to name a

few. In 2014, J-PV's paper submissions were almost doubled at more than 700 while its impact factor has hit the mark 3. Considering that J-PV was launched in 2011, these are substantial accomplishments for J-PV, the Editorial Board, and the EiC, Tim Anderson. Along with the improvement in publishing cycle time, J-MEMS turned around its financial performance into profit in 2014 under the leadership of J-MEMS EiC, Christofer Hierold, and with the support from the J-MEMS Steering Committee. While we thank the outgoing EiC, Sean Cunningham and welcome Anthony Muscat as the new EiC for T-SM, we are transferring T-SM production in-house for lower cost. As the EiC for J-DT, Arokia Nathan has been leading a few initiatives for J-DT, which involved other IEEE societies and the OSA.

In May 2014, the EDS Publications and Products Committee completed its first charter document on Committee's functions and responsibilities. In December 2014, the Committee discussed and generated a document on EiC Selection Procedure for T-ED, EDL, and J-EDS. These documents are under continued enhancements based on feedbacks from related activities, various reviews and inputs. The technical content directly impacts the influence and the quality of our publications. While we provide the needed coverage in all topical areas of the Society's FOI through efforts from the Editorial Boards of the EDS publications, we take measures to enhance the coverage and to best meet the needs from the technical evolution and revolution in our field. Special issues of T-ED on "*Variation Aware Technology and Circuit Co-Design*" and "*Solid-State Image Sensors*" will be published in June 2015 and January 2016, respectively. To honor the 60th annual IEEE International

Electron Devices Meeting (IEDM) in 2014, we are working with IEDM for a special issue in T-ED while a long term strategy is under development for journal special issues covering the EDS conferences.

EDS publication activities are at the core of the value being delivered to our technical community around the globe and are critical to continue to fulfill the Society's mission, promoting excellence in the field of electron

devices for the benefit of humanity. We look forward to your input and would like to invite you to get more involved by volunteering your time and energy to these activities. Please do not hesitate to contact me at bin.zhao@ieee.org with any suggestions or comments.

Bin Zhao
EDS Vice President of Publications
and Products

Fairchild Semiconductor
Irvine, CA, USA

(Bin Zhao, Vice President of Publications and Products at IEEE EDS, is the Director of Southern California Development Center at Fairchild Semiconductor, USA. He has involved in VLSI technology development, circuit design and implementation of analog/mixed-signal, power management, and RF IC products. He is an IEEE Fellow.)

MESSAGE FROM NEWSLETTER EDITOR-IN-CHIEF



M K Radhakrishnan
Editor-in-Chief
EDS Newsletter

Dear Readers,

The new sections in our Newsletter, especially Technical Briefs and Young Professionals, are getting more attraction from the feedbacks received from our members.

Also, the messages indicate that the Newsletter contents are useful and informative to the readers. However, most of the feedback messages are one or two words only and we would encourage our readers to write in at least one paragraph about their opinion, which will enable us to publish it as Letters to Editor.

This issue has the article on Solid State Incandescent LED in the Technical Briefs section. Also, we are capturing the major conferences in the devices area by providing the latest updates. Chapter News section has coverage of interesting activities by some of the chapter community in the society. Again, I request all our readers to write to us. We would like to hear your opinion. Your e-mails are welcome and you may write to me or to edsnewsletter@ieee.org.

Three of our Regional Editors are completing their service in the editorial team after serving their term. Peyman Servati has been the

Regional Editor for Regions 4 & 7. Tomislav Suligoj served as the Regional Editor for Eastern Europe and Zygmunt Ciota was very active as the Regional Editor in the Scandinavia and Central Europe area of Region 8. They were very efficient communicators and instrumental in corresponding and providing the news from the Chapters in their respective Regions. Their hard work throughout the years is reflected in the articles published in the Newsletter covering various Chapter activities in those regions. On behalf of the entire Newsletter team, I would like to express our sincere gratitude to all of them.

Three new members are joining the Editorial team. Karim S. Karim from University of Waterloo, Canada, will be the Editor for Regions 4 & 7, Central USA and Canada. Mariusz Orlikowski of Lodz University of Technology, Poland, is the Editor for Central Europe and Scandinavia of Region 8. Daniel Tomaszewski from Institute Technologii Electronics (ITE), Warsaw, Poland, is the Editor for Eastern Europe of Region 8. It is my pleasure to welcome all of them to our team as new Editors of the EDS Newsletter.

Karim S. Karim (M'00, SM'08) received the PhD degree in Electrical Engineering from the University of



Waterloo in 2002 where he is currently a Full Professor and the Associate Director for Bioengineering and Biotechnology. Dr. Karim's research interests (<http://star.uwaterloo.ca>) encompass system, circuit, device, and process development using amorphous semiconductors for digital imaging applications. To date, he and his graduate students have co-authored over 200 publications and have been awarded 10 patents. Dr. Karim is an IEEE Electron Devices Society Distinguished Lecturer, a Full Member of the American Association of Physicists in Medicine, and is a registered Professional Engineer in Canada.



Mariusz Orlikowski received MSc and PhD degrees in electrical engineering from Lodz University of Technology in 1995 and 2000, respectively.

He is currently an Associate Professor in the Department of Microelectronics and Computer Science of Lodz University of Technology. His research interests include behavioral modelling,

object oriented programming, distributed programming of data acquisition and processing systems and multi-threaded systems development. He has been secretary of IEEE sponsored international MIXDES Conference series since 2004. He is also Deputy Editor in Chief of International Journal of Microelectronics and Computer Science.

Daniel Tomaszewski graduated from Warsaw University of Technology, Institute of Microelectronics and Opto-



electronics in 1980. Since 1980, he has been with Instytut Technologii Elektronowej (ITE), Warsaw, Poland, where in 1998, he received a Ph.D. degree. He is involved in the numerical and compact modeling, testing and characterization of MOSFETs and other semiconductor devices developed at ITE. The activities in-

clude support for bulk and SOI CMOS technologies, ISFET sensors, radiation detectors and statistical modeling. Since 2007, he is a co-organizer of the special compact modeling sessions at International Conference Mixed Design of Integrated Circuits and Systems (MIXDES).

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M K Radhakrishnan

Editor-in-Chief

EDS Newsletter

e-mail: radhakrishnan@ieee.org

EDS BOARD OF GOVERNORS MEETING AND ANNOUNCEMENT OF NEWLY ELECTED OFFICERS AND BoG MEMBERS



Paul Yu

*EDS Nominations
and Elections Chair*

The December Governance Meeting Series held in conjunction with the IEEE International Electron Devices Meeting (IEDM), held in San Francisco, California, once again convened

the volunteer leadership of EDS to report on the state of the society and to discuss the critical issues facing us today. One important feature added this year were the expanded standing committee meetings held throughout the day on Saturday. The standing committees, 10 of them in all, form the backbone of the society's crucial operations and accordingly, we devoted significantly more time and resources to support these crucial bodies and facilitate their engagement.

The Board of Governors (BoG) and Forum meeting held Sunday, December 14th, showcased lively and spirited debate on a number of topics. Most critical was the discussion on revising the process for selecting and approving new EiCs for our flagship publications. This is an ongoing effort

advanced at the December meeting and one that will continue in 2015. Other important actions taken were to approve the EDS Repeat Conferences for 2016 and the EDS 2015 budget, which includes additional funds for volunteer travel and support and some significant reductions in staffing costs, owing to a restructuring of the executive director's role.

Newly Elected Officers and BoG Members

In 2014, EDS held a pilot program to have one of the eight BoG Member-at-Large seats elected via the entire EDS membership. The remaining seven seats were voted on by our BoG during the election, which took place on December 14, 2014, at the Hilton San Francisco Union Square Hotel in San Francisco, California.

A total of eight members were elected for a three-year term (2015–2017). Three of the eight electees are serving a second term, while the other five join the board for the first time. The backgrounds of the electees span a wide range of professional and technical interests. The following are the results of the election and brief biographies of the individuals elected.

Bog Members-At-Large

Second Term Electees:



Zeynep Çelik-Butler received dual B.S. degrees in electrical engineering and physics from Bogaziçi University, Istanbul, Turkey, the M.S. and Ph.D.

degrees in electrical engineering from the University of Rochester. She was an IBM Pre-doctoral Fellow from 1983 to 1984, and an Eastman Kodak Pre-doctoral Fellow from 1985 to 1987. Her research interests include microelectromechanical systems, multi-functional reconfigurable sensors, noise and reliability in nanoelectronic devices. She has seven patents awarded and three pending, seven book chapters, and over 200 journal and conference publications in these fields. She currently serves in the editorial board of *IEEE Transactions on Electron Devices*, *IEEE Sensors Journal* and *Journal of Nanoelectronics and Optoelectronics*.

Dr. Çelik-Butler is a Fellow of IEEE, member of Eta Kappa Nu, and the American Physical Society. She is a Distinguished

Lecturer of the IEEE Electron Devices Society.



Steve S. Chung received his Ph.D. degree from the University of Illinois at Urbana-Champaign, in Electrical Engineering in 1985.

He is Chair Professor and UMC Research Chair Professor at the National Chiao Tung University (NCTU). After joining NCTU in 1987, he has been the Department Head, 2004–2005, Dean of International Affairs Office, 2007–2008. He was a Visiting Scholar with Stanford University in 2001, visiting professor to University of California-Merced in 2009–2010, and a guest lecturer at Stanford in 2009. He was also the consultant to the two world largest IC foundries, TSMC and UMC. His research areas include: nanoscale CMOS devices and technology; nonvolatile memory technology and reliability; and reliability physics/interface characterization.

He is an IEEE Fellow. Currently he is a BoG member, Distinguished Lecturer, Editor of J-EDS, member of Education committee, VLSI committee etc. in the EDS. His past involvements include: EDL editor, EDS SRC vice-chair and chair, BoG member, Fellowship committee member, Guest editor of TDMR, etc.



Tian-Ling Ren received his Ph.D. degree from Department of Modern Applied Physics, Tsinghua University, China in 1997.

He has been a full professor of Institute of Microelectronics, Tsinghua University, China since 2003. He has been a visiting professor at Electrical Engineering Department, Stanford University from 2011 to 2012. His research is focused on novel micro/nano elec-

tronic devices and key technologies, including MEMS/NEMS, memories, 2D material based nano devices, RF devices, and flexible electronics. He has published more than 300 journal and conference papers and 50 patents. He is a Board of Governors (BoG) member and a Distinguished Lecturer of the IEEE Electron Devices Society. He is also a council member of Chinese Society of Micro/Nano Technology.

First-Time Electees:



Mukta Farooq is a metallurgist/materials scientist, with expertise in 3-Dimensional silicon integration/packaging, die/wafer stacking

for hybrid memory cube, CMOS FET back end structures, C4 technology, lead-free alloys and chip package interaction.

Mukta is an IBM Lifetime Master Inventor with over 175 issued US and international patents. She has 27 external publications and has given invited talks at conferences and universities. She is a founding member of the annual IBM Semiconductor Technology Symposium, having served as Technical and General Chair. Mukta is a Senior Member of IEEE, an IEEE EDS Distinguished Lecturer, Chair of the EDS Mid Hudson Valley Chapter, and Regional Editor, EDS Newsletter.

Mukta is a Senior Technical Staff Member at IBM, and a member of the IBM Academy of Technology. She has a B.Tech. in Metallurgical Engineering from IIT-Bombay, an M.S. in Materials Science from Northwestern University and a Ph.D. in Materials Science & Engineering from Rensselaer Polytechnic Institute.

Patrick Fay is a professor in the Department of Electrical Engineering at the University of Notre Dame. He received a Ph.D. in electrical engineering from the University



of Illinois at Urbana-Champaign in 1996 after receiving a B.S. in electrical engineering from Notre Dame in 1991.

His research interests include the design, fabrication, and characterization of microwave and millimeter-wave electronic devices and circuits, as well as high-speed optoelectronic devices and optoelectronic integrated circuits for fiber optic telecommunications. His research also includes the development and use of micromachining techniques for the fabrication of microwave components and packaging. His educational initiatives include the development of an advanced undergraduate laboratory course in microwave circuit design and characterization. Prof. Fay is a senior member of the IEEE.



Carmen M. Lilley received her Bachelors of Engineering in General Engineering from the University of Illinois at Urbana-Champaign in

1998 and her Ph.D. in Theoretical and Applied Mechanics from Northwestern University in 2003. She joined the Department of Mechanical and Industrial Engineering (MIE) at the University of Illinois at Chicago in 2003 as an Assistant Professor and is currently an Associate Professor in MIE and Adjunct Associate Professor in Electrical and Computer Engineering. Her research is focused on the characterization and modeling of materials at the nano- and microscale. Dr. Lilley has published in highly respected journals and conferences, including *Applied Physics Letters*, *Journal of Applied Physics*, *Nano Letters*, *ASME Journal of Applied Mechanics*, and *IEEE Transactions in Nanotechnology*. Dr. Lilley has also received various awards

and honors recognizing academic and research achievements including the NSF CAREER award in 2009.



Durga Misra is a Professor in the Electrical and Computer Engineering Department of New Jersey Institute of Technology (NJIT).

He received his M.S. and Ph.D. degrees both in Electrical Engineering from University of Waterloo, Waterloo, Canada in 1985 and 1988 respectively. His current research focus is study of nanoscale CMOS gate stacks with high-k gate dielectrics and its reliability. He served as the IEEE EDS SRC Chair for North America (2006–2012) and received IEEE MGA's International Leadership Award. He is currently a Distinguished Lecturer of EDS. He is a Fellow of the Electrochemical Society (ECS) and has received the Electronic and Photonic Division Award and the

Thomas D. Callinan Award from the ECS. He has edited and co-edited more than 30 conference proceedings including several of them on High-k gate stacks. He has published more than 200 articles in journals and international conferences.



Hisayo Momose has been studying Si transistors ranging from 1.2 μm to sub-50 nm during the last 30 years. She engaged in the development of static RAMs,

CMOS/BiCMOS logic LSIs and CMOS analog devices. She did a great deal of work on hot-carrier reliability, oxynitride/stacked nitride-oxide gate MISFETs, Ni salicide MOSFETs and ultra-thin gate oxide MOSFETs in the direct-tunneling regime.

She is currently with Center for Semiconductor Research and Development, Toshiba Corporation, Kawasaki,

Japan. Her current interests include oxide thin film transistors, noise characteristics and the related issues of CMOS imaging devices. She has more than 50 patents and she authored/co-authored more than 200 papers in the technical journal and the conferences.

She served as an editor of *IEEE Transactions on Electron Devices* for the last 10 years. She handled more than 400 manuscripts in the area of MOS devices and technology. She also served as a member of EDS Fellow Evaluations Committee.

I welcome all electees and urge them to truly get engaged in the affairs of the Electron Devices Society. EDS is considered to be a volunteer-led, volunteer-driven organization and we expect nothing less from all to continue this tradition.

Paul Yu

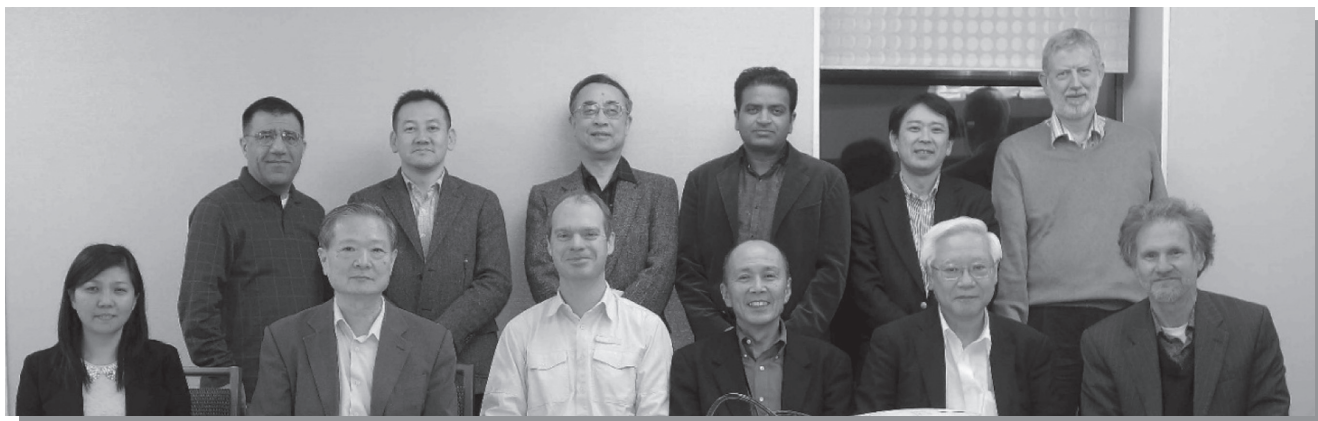
*EDS Nominations and Elections Chair
University of California
San Diego
La Jolla, CA, USA*

REPORT FROM THE VLSI TECHNOLOGY AND CIRCUITS COMMITTEE

On December 13, 2014, the *VLSI Technology and Circuits Committee* met in San Francisco, California, during the 2014 IEEE International Electron De-

vices Meeting (IEDM), held December 15th–17th. This committee has face-to-face meetings twice a year during the IEDM and VLSI Symposiums.

The objective of the *VLSI Technology and Circuits Committee* is to identify new and relevant areas of interest to the Electron Devices and Solid-State



Attendees of the VLSI Committee (sitting left to right), Ru Huang, Steve Chung, Jurriaan Schmitz, Shuji Ikeda, Hiroshi Iwai, John Suehle, (standing left to right), Reza Arghavani, Hitoshi Wakabayashi, Seiichiro Kawamura, Kaustav Banerjee, Kazunari Ishimaru, Jacobus Swart and Mansun Chan (not in picture)

Circuits communities. Based on the nature of the areas, the committee recommends any or all of the following:

- 1) Initiate topical workshops of current interest (attach to existing conferences or incorporate in new ones)
- 2) Special issues for major publications (e.g., T-ED)
- 3) Panel session topics for major conferences
- 4) Special sessions for major conferences

The following topics were discussed during the December 2014 meeting:

- 1) A proposal to create a new conference in Asia (Asian Electron Devices Meeting) with focus on:
 - a) Device Technology
 - b) Industry (manufacturing) and academic related papers

- c) Exhibition from equipment companies
- d) Emerging devices, Bio/Medical and related topics
- e) Tutorials
- f) Location: Taiwan, China, Korea and Japan (first round)

With valuable discussions with various EDS members including IEDM executives, EDS executives, and AdHoc Committee members, the team decided to fine-tune the proposal's mission and logistics in more detail and discuss further at the next committee meeting.

- 2) A special issue of *IEEE Transactions on Electron Devices* on "Variation Aware Technology and Circuit Co Design" was discussed. Dr. Seung-Chul Song from Qualcomm, Dr. Huiling Shang from IBM and Professor

Kaustav Banerjee are leading the efforts on this.

- a) Final invited papers and topics were discussed
 - b) Deadline for reviewers and submitted papers were discussed and finalized
- 3) Membership policy change from three years to two years with potential of one renew was discussed.

Please contact Dr. Kaz Ishimaru (kazu.ishimaru@toshiba.co.jp), conferences/workshops subcommittee chair, or Dr. Shu Ikeda (shu.ikeda@tei-solutions.com), committee chair, for further information.

Reza Arghavani
EDS VLSI TC Committee Member
Lam Research Corporation
Fremont, CA, USA

EDS ELECTRONIC MATERIALS TECHNICAL COMMITTEE REPORT

The Electronics Materials Technical Committee is a newly formed one within the IEEE Electron Devices Society. Although the high- κ dielectrics, metal gate, and high mobility materials have made great contributions to CMOS and memory devices, daunting challenges lay ahead. Along with the EDS BoG Meeting in December 2014, we held the first committee meeting in San Francisco during which the committee decided to propose a special issue on electronic materials related to ultra-low power devices. Portable electronic devices are indispensable in our daily life, and the coming era of Internet of Things will further increase the usage of electronic devices. Ultra-low power is the major technological challenge for more-than-Moore de-

vices, which depends strongly on new electronic materials. For example, adding piezoelectric or ferroelectric materials into MOSFETs is expected to improve the turn-on slope and lower the DC leakage and AC switching power. These new electronic materials can also be used for ultra-low power memory application beyond existing DRAM thereby enabling technology for process-in-memory to mimic the human brains. New electronic materials for other devices will also be included. Based on these considerations, the committee has decided on a special issue covering these topics with planned publication in *IEEE Journal of the Electron Devices Society* (J-EDS). The other topic discussed in the committee meeting is to promote activities

in our field, which may require us to organize or operate sessions at meetings of IEEE. Although electronic materials have made a huge impact on devices and related subjects actively published at the IEDM, VLSI Symposium etc., there is still a lacking of its own IEEE conference. This will be the future goal of the Electronic Materials Technical Committee. For more information on our members, visit the committee page of the EDS website: www.ieee.org/eds/technical-committees/eds-electronic-materials-technical-committee.html.

Albert Chin
EDS Electronic Materials
Technical Committee Chair
National Chiao Tung University
Taiwan

CONGRATULATIONS TO THE 46 EDS MEMBERS RECENTLY ELECTED TO IEEE SENIOR MEMBER GRADE!

Mohamed Ahmed
Abdel Moneum
Yasushi Akasaka
Meng-Fan Chang
Baoxing Chen
Hsien-Chin Chiu
Chris Connor
Victor Corasaniti
E. Cowell III
Felice Crupi
Peter Deane
Daniel Edelstein

Akira Fujiwara
Steven Gross
David Gundlach
Hyunsang Hwang
Marek Hytha
John Jackson
Curt Karnstedt
Douglas Katzer
Seongsin Kim
Irena Knezevic
Franz Kreupl
Qiliang Li

Chung-Hsun Lin
Ming-Chieh Lin
Yang Liu
Kenneth Mays
Thomas McKay
Mohdkhairuddin
Mdardshad
David Meyer
Joel Molina
Anand Murthy
Patrick Roblin
Horst Rogalla

Frank Ryan
Charles Surya
Ravi Todi
Akira Toriumi
Reydezel Torres-Torres
Eric Tournie
Pouya Valizadeh
Dapeng Wang
Jian-Ping Wang
Yifeng Wu
Woojun Yoon
Hsiao Wen Zan

If you have been in professional practice for 10 years, you may be eligible for Senior Membership, the highest grade of membership for which an individual can apply. New senior members receive a wood and bronze plaque and a credit certificate for up to US\$25 for a new IEEE society membership. Upon request a letter will be sent to employers, recognizing this new status.

For more information on senior member status, visit:
http://www.ieee.org/membership_services/membership/senior/index.html

To apply for senior member status, fill out the on-line application: https://www.ieee.org/membership_services/membership/senior/application/index.html.

You will need to Sign-in with your IEEE account.

Please remember to designate the Electron Devices Society as your nominating entity!

28 EDS MEMBERS ELECTED TO THE IEEE GRADE OF FELLOW

EFFECTIVE 1 JANUARY 2015



Leda Lunardi
2014 EDS
Fellows Chair

David Abe, U.S. Naval Research Laboratory, Washington, DC, USA
for leadership and contributions to the development of high power microwave and millimeter wave vacuum electronic devices

Christopher Auth, Intel Corporation, Hillsboro, OR, USA
for contributions to strained silicon transistor technology

Victor Bright, University of Colorado, Boulder, CO, USA
for contributions to micro- and nano-electromechanical systems

Martin Buehler, Decagon Devices, Pullman, WA, USA
for contributions to metrology through development of semiconductor process control test structures, gas sensors and radiation detectors

John Conley, Oregon State University, Corvallis, OR, USA
for contributions to semiconductor process technology to improve radiation hardening of MOS devices

John Dallesasse, University of Illinois at Urbana-Champaign, Urbana, IL, USA
for contributions to oxidation of III-V semiconductors for photonic device manufacturing

Weileun Fang, National Tsing Hua University, Hsinchu, Taiwan
for contributions to measurement methods and process technologies for micro-electro-mechanical systems

Lorenzo Faraone, University of Western Australia, Crawley, WA, Australia
for development of semiconductor optoelectronic materials and devices

Reza Ghodssi, University of Maryland, College Park, College Park, MD, USA

for contributions to materials and processes for microsystems technology

Deepnarayan Gupta, Hypres Inc., Elmsford, NY, USA

for contributions to superconductor digital radio-frequency receivers

Ray-Hua Horng, National Chung Hsing University, Taichung, Taiwan

for contributions to high brightness light emitting diodes

Giuseppe Iannaccone, University of Pisa, Italy, Pisa, Italy

for contributions to modeling transport and noise processes in nanoelectronic devices

Meikei leong, TSMC Europe B.V., Amsterdam, Netherlands

for leadership in development of advanced complementary metal-oxide-semiconductor device technologies

Safa Kasap, University of Saskatchewan, Saskatoon, SK, Canada

for contributions to photoconductive sensors for x-ray imaging

Tsunenobu Kimoto, Kyoto University, Kyoto, Japan

for contributions to silicon carbide materials and devices

Hiroshi Kondoh, Centellax, Inc., Santa Rosa, CA, USA

for contributions to microwave and millimeter wave MMIC technologies

Paul Lee, Exelis Geospatial Systems, Amityville, NY, USA

for contributions to the development of CMOS image sensor technology and the pinned photo-diode active pixel sensor

Yong Liu, Fairchild Semiconductor Corp., South Portland, ME, USA

for contributions in power electronics packaging

Susan Lord, University of San Diego, San Diego, CA, USA

for professional leadership and contributions to engineering education

Roger Malik, First Solar, Santa Clara, CA, USA

for contributions to heterojunction compound semiconductor materials and devices

Wiltold (Witek) Maszara, Global Foundries, Santa Clara, CA, USA

for contributions to high performance CMOS process modules

Sokrates Pantelides, Vanderbilt University, Nashville, TN, USA

for contributions to point-defect dynamics in semiconductor devices

Luca Selmi, University of Udine, Udine, Italy

for research on carrier transport and reliability of semiconductor devices

Paul Tasker, Cardiff University, UK, Cardiff, Wales, UK

for contributions to microwave measurements and their application to microwave models

Jian-Ping Wang, University of Minnesota, Minneapolis, MN, USA

for contributions to magnetic material and spintronic devices for magnetic recording, information processing and biomedical applications

Mark Weichold, Texas A&M University at Qatar, Doha, Qatar

for contributions to international development of engineering education

Chik Patrick Yue, Hong Kong University of Science & Tech., Clear Water Bay, Hong Kong

for contributions to the advancement of CMOS radio-frequency integrated circuits and devices modeling

Yong-Hang Zhang, Arizona State University, Tempe, AZ, USA

for contributions to molecular beam epitaxy growth technology, infrared lasers and photodetectors

Leda Lunardi

2014 EDS Fellows Chair

North Carolina State University
Raleigh, NC, USA

2014 AWARD WINNERS

2014 EDS J.J. EBERS AWARD WINNER

The 2014 J.J. Ebers Award, the prestigious Electron Devices Society award for outstanding technical contributions to electron devices, was presented to Dr. Joachim Burghartz of the Institute for Microelectronics Stuttgart (IMS CHIPS) Stuttgart, Germany, at the IEEE International Electron Devices Meeting in San Francisco, California, on December 14, 2014. This award recognizes Joachim Burghartz *"For contributions to integrated spiral inductors for wireless communication ICs and ultra-thin silicon devices for emerging flexible electronics."*

Joachim Burghartz was born in Aachen, Germany, in 1956. Even though his favorite was architecture he decided on a professional career in engineering, thanks to his late stepfather. He received the Dipl.-Ing. and Ph.D. degrees in electrical engineering from the RWTH Aachen and the University of Stuttgart in 1982 and 1987, respectively. In 1987 he joined the IBM T. J. Watson Research Center in New York, where he worked until 1998. From 1998 through 2005, he was a full professor at the Technical University of Delft in the Netherlands, where in 2001 he became the Scientific Director of the research institute DIMES. Since 2005 he is the director of the Institute for Microelectronics Stuttgart (IMS CHIPS) and also full professor at the University of Stuttgart.

At IBM, in 1993, he started to explore possibilities to integrate high-quality spiral inductors on silicon for communication ICs. His 1995 IEDM Late News paper proved for the first time that useful quality factors ($Q > 20$) were feasible for inductors on silicon substrates. In the following years, at IBM and at TU Delft, he made sustained contributions to the integration of inductors and other passive components which are key



Joachim N. Burghartz receiving the J.J. Ebers Award from EDS President, Albert Wang at the 2014 IEDM

elements of today's wireless communication ICs and have allowed boosting band width and lowering system power and cost.

During his early term at IBM he was a member of the team that pioneered SiGe bipolar technology. He was able to demonstrate, for the first time, selective epitaxial base and self-aligned SiGe bipolar transistor structures as well as APCVD-grown SiGe HBTs.

From 2006, at IMS CHIPS, he has been exploring ultra-thin silicon chips and its application to flexible electronics. This work has led to innovations in stress management for CMOS devices and ultra-thin chips, in thin chip mechanical stability optimization, in stress-impacted device modeling and circuit design, in electrical and mechanical characterization, and in assembly of thin chips. For this work he received the prestigious Research Award of the State of Baden-Wuerttemberg in Germany in 2009.

He has authored and co-authored more than 350 peer-reviewed

publications. In 2013, Joachim Burghartz edited the book *'Guide to State-of-the-Art Electron Devices'* on behalf of the IEEE Electron Devices Society (EDS) to celebrate 60 years of EDS's work from its inception in IRE in 1952 to its official foundation as an IEEE society in 1976. This book received the PROSE Award as the best book of the year 2013 in the category engineering and technology.

Joachim Burghartz is an IEEE Fellow and has served as EDS Vice-President of Technical Activities, as an associate editor of the *IEEE Transactions on Electron Devices* and as a special advisor at numerous IEEE-sponsored conferences. He and his wife, Susanne, have three daughters. They love nature, sports, music and arts, as well as staying in touch with many good friends.

Jayant Baliga
EDS J.J. Ebers Award Chair
North Carolina State University
Raleigh, NC, USA

2014 EDS DISTINGUISHED SERVICE AWARD

The IEEE Electron Devices Society (EDS) is extremely proud of the services that it provides to its members. Its members generate the premier new developments in the field of electron devices and share these results with their peers and the world at large by publishing their papers in EDS journals and presenting results in its meetings. This is a global activity that is effective because of the efforts of numerous volunteers. Many of these volunteers labor in relative obscurity, with their only reward being the satisfaction that they receive in being an important part of a successful organization, namely of the IEEE Electron Devices Society. One means of thanking these volunteers is to recognize their contributions through the EDS Distinguished Service Award. This award for 2014 was presented to Professor Yuan Taur at the IEEE International Electron Devices Meeting in San Francisco, California on December 14, 2014.

Yuan Taur was born in Nanchang, Jiangxi, China. He earned the highest score in the unified university entrance exam in Taiwan in 1963. Yuan received the B.S. degree in physics from National Taiwan University in 1967, and the Ph.D. degree in physics from University of California, Berkeley, in 1974, with thesis "Josephson junctions as microwave heterodyne detectors".

In 1981, Yuan joined the Silicon Technology Department of IBM Thomas J. Watson Research Center, Yorktown Heights, New York. Later, he led a group and developed self-aligned silicide on shallow junctions, dual n+/p+ polysilicon gates, and shallow trench isolation to enable low voltage, high density 0.5 μm and 0.25 μm CMOS technologies. In 1993, he published a seminal paper on 0.1 μm CMOS with 1.5 V supply voltage. In 1997, Yuan wrote a landmark paper in IEEE Proceedings on scaling CMOS devices to their lim-



Professor Yuan Taur (right), receiving the EDS Distinguished Service Award from EDS President, Albert Wang at the 2014 IEDM

its. His other notable works include "shift and ratio" method for channel length extraction, "super-halo" design for suppression of short-channel effects, and "generalized scale length theory" for MOSFET scaling.

In 2001, Yuan took a professor position in the Department of Electrical and Computer Engineering, University of California, San Diego. In 2004, he published an analytic potential model for double-gate MOSFETs, which became the de facto standard for compact modeling of multi-gate devices, including FinFETs. Over the past few years, he and his students developed a distributed bulk-oxide trap model, and a new methodology for applying the full interface-state model to III-V MOS devices. In 2014, he was appointed Distinguished Professor at UCSD.

Dr. Yuan Taur was elected a Fellow of the IEEE in 1998, "for outstanding contributions to advanced CMOS technology." He received the IEEE Electron Devices Society's J. J. Ebers Award in 2012, "for contributions to the advancement of several generations of CMOS process technologies." He has served as the Editor-in-Chief of *IEEE Electron Device Letters* from 1999 to 2011, during which period the number of annually published

papers had grown from below two hundred to over five hundred, while the time from submission to publication was reduced from eight months to two and a half months. He has also served as General Chairman for the Symposium on VLSI Technology.

Dr. Yuan Taur has authored or co-authored over two hundred journal and conference papers and holds fifteen U.S. patents. He co-authored a book with Dr. Tak Ning of IBM, "*Fundamentals of Modern VLSI Devices*," published by Cambridge University Press in 1998. It has been widely circulated among the engineers in the industry and adopted in many major universities in the US and worldwide as a textbook in solid-state electronics. The 2nd edition was published in 2009. Both editions have been translated into Japanese.

Yuan and his wife Katie live in San Diego. They are members of the Morgan Run Golf Club, Rancho Santa Fe. They are entertained in their leisure time by their 4-year old black dachshund, Gala.

*Paul Yu
EDS Awards Chair
University of California at San Diego
La Jolla, CA, USA*

2014 EDS Education Award Winner

The EDS Education Award recognizes an IEEE/EDS Member from an academic, industrial, or government organization with distinguished contributions to education within the fields of interest of the IEEE Electron Devices Society. Juin Liou was recognized at the IEEE International Electron Devices Meeting in San Francisco, California, on December 14, 2014 as the 2014 EDS Education Award winner. The award cites Professor Liou "For promoting and inspiring global education and learning in the field of electron devices".

Juin J. Liou received the B.S. (honors), M.S., and Ph.D. degrees in electrical engineering from the University of Florida, Gainesville, in 1982, 1983, and 1987, respectively. In 1987, he joined the Department of Electrical and Computer Engineering at the University of Central Florida (UCF), Orlando, Florida, where he is now a Professor. His current research interests are electrostatic discharge (ESD) and electromagnetic compatibility (EMC) protection design, characterization, modeling and simulation.

Dr. Liou holds 8 U.S. patents, and has published 11 books, more than 270 journal papers, and more than 220 papers in international conference proceedings. His UCF awards include the Pegasus Distinguished Professor – the highest honor bestowed to a faculty member at UCF, Lockheed Martin St. Laurent Professor of Engineering for his significant research contributions, and UCF-ADI Fellow for his long-term and productive partnership with the industry sponsor Analog Devices, Inc. His



Juin J. Liou receiving the EDS Education Award from EDS President, Albert Wang, at the IEDM

other honors are the IEEE Joseph M. Biedenbach Outstanding Engineering Educator Award for his exemplary teaching, research, and international collaboration, Fellow of IEEE, and Fellow of IET. He holds several honorary professorships, including the Chang Jiang Scholar Endowed Professor of Ministry of Education, China – the highest honorary professorship in China, International Honorary Chair Professor of National Taipei University of Technology, Taiwan, Chang Gung Endowed Professor of Chang Gung University, Taiwan, Feng Chia Chair Professor of Feng Chia University, Taiwan, and Chunhui Eminent Scholar of Peking University, China.

Liou has served as a general chair or technical program chair for a large number of international conferences, and as an editor or guest

editor for several top-tier journals in the field of electron devices and microelectronic reliability. Dr. Liou has been active in volunteering professional services. He has served as the IEEE EDS Vice-President of Regions/Chapters, IEEE EDS Treasurer, IEEE EDS Finance Committee Chair, Member of IEEE EDS Board of Governors, and Member of IEEE EDS Educational Activities Committee. He enjoys world travels which often lead to new academic exchanges and friendships.

Juin and his wife, Peili, are the proud parents of Will, a pediatric dentist, and Monica, an optometrist.

*Meikei leong
2014 EDS Education Award Chair
TSMC Europe BV
Amsterdam*

STATUS REPORT FROM THE 2014 EDS PhD STUDENT FELLOWSHIP RECIPIENTS



Carmen Lilley
EDS Student
Fellowship
Committee Chair

The EDS PhD Student Fellowship Program is designed to promote, recognize, and support graduate level study and research within the Electron Devices Society's Fields of Interest.

The 2014 EDS PhD Student Fellowship recipients were: **Amit Ranjan Trivedi** from Georgia Institute of Technology, **Peng Huang** from Peking University, and **Sam Vaziri** from KTH Royal Institute of Technology, Kista. The following are brief progress reports provided by the award winners.



Peng Huang has been making further progress in his research work on modeling and simulation of resistive switching memory (RRAM).

His most recent output is the investigation of resistive switching mechanism of TaOx/Ta2O5 based RRAM accounting for the self-compliance

and robust endurance characteristic. This work will be presented at the VLSI-TSA 2015 in April at Hsinchu, Taiwan. He also proposed a parameter extraction method to extract the dominated switching parameters of HfOX based RRAM. As a part of his graduate study, he was on a three-month internship at Stanford University focusing on the match of selector and RRAM device in the crossbar architecture. He is expecting to defend his thesis around mid-May 2015.



Amit Ranjan Trivedi has been looking into non-conventional transistor designs to suit non von Neumann and neuromorphic computing. He recently published his article in *IEEE Electron Device Letters* demonstrating negative gate transconductance in source/gate overlapped heterojunction Tunnel FET. He is further expanding this work by utilizing a network of source/gate overlapped heterojunction Tunnel FETs in area/energy-efficient pattern matching system. Amit is expecting to defend his thesis around mid-August 2015.



Sam Vaziri's research activities have been focused on process development for the fabrication and integration of graphene-based

devices. He has developed a wafer-scale graphene transfer method optimized for integration of graphene with semiconductors and dielectrics. This work was presented at ESSDERC 2014 and contributed to another publication in *Solid-State Electronics*. Furthermore, he is working on bilayer dielectric tunneling barriers for high frequency vertical graphene base transistors (GBTs). He has succeeded to dramatically improve the injection current in comparison to his previous report in *Nano Letters* 2013, and is working on a manuscript based on this work. Sam has planned to finish his PhD studies by the end of this year.

Carmen Lilley
EDS Student Fellowship
Committee Chair
University of Illinois at Chicago
Chicago, IL, USA

2014 EDS EARLY CAREER AWARD WINNER

The EDS Early Career Award recognizes an IEEE/EDS member who has made outstanding contributions in an EDS field of interest.

The 2014 EDS Early Career Award was presented to Can Bayram of the University of Illinois at Urbana-Champaign, Urbana, Illinois, at the EDS Awards Dinner held in conjunction with the IEEE International Elec-

tron Devices Meeting in San Francisco, California, on December 14, 2014.

Can Bayram is an Assistant Professor in the Department of Electrical and Computer Engineering of University of Illinois at Urbana-Champaign, IL, USA. His research is in development and application of novel photonic and electronic devices. His group, Innovative Compound

semiconductor (ICOR) Laboratory, currently explores novel designs of light emitting diodes for disinfection and lighting; and of GaN-based transistors for next generation power devices. He invented GaN-on-Graphene technology which was published in *Nature Communications* (downloaded more than 1400 times in its first month). His work has been

recognized widely. He is the recipient of the Best Paper Award at the 11th International Conference on Infrared Optoelectronics.

His postdoctoral work at IBM on a novel means of thin film technology achieved record-breaking specific power solar cells and was featured on the cover of *Advanced Energy Materials*. He has – for the first time—integrated GaN-based devices on CMOS-compatible silicon substrates. This work was highlighted as the frontispiece in the *Advanced Functional Materials* issue. His thesis work has demonstrated the first ultraviolet regime single photon detection, the first hybrid LED, and the first GaN intersubband devices. He received IEEE Electron Devices and IEEE Photonics Societies' fellowship awards and the Laser Technology, Engineering



Can Bayram (left) accepting the 2014 EDS Early Career Award from Albert Wang, EDS President

and Applications Award from SPIE. He was an IBM and Link Foundation PhD fellow and the recipient of Boeing Engineering and Dow Sustainability Innovation awards.

Prof. Bayram is an affiliate faculty of Micro and Nanotechnology Laboratory. He has (co-) authored 32 journal papers (h-index ≥ 17), 23 conference proceeding papers, and has 15 patents pending. For his achievements in ultraviolet-to-terahertz engineering of III-V semiconductor materials and devices, SPIE recognized him with senior member status. He was a Postdoctoral Research Scientist at IBM Thomas J. Watson Research Center, Yorktown Heights, NY, USA from 2011 till 2014. He received the Ph.D. degree from EECS of Northwestern University, IL, USA with a focus on Solid State and Photonics in 2011.

*Samar Saha
EDS Early Career Award Chair
Ultrasolar Technology
Santa Clara, CA, USA*

STATUS REPORT FROM THE 2014 EDS MASTERS STUDENT FELLOWSHIP WINNERS



*Carmen Lilley
EDS Student
Fellowship
Committee Chair*

The EDS Masters Student Fellowship program is designed to promote, recognize, and support Masters level study and research within the Electron Devices Society's Fields of Interest.

The 2014 EDS Masters Student Fellowship recipients were: **Yexin Deng** from Purdue University, and **Siu-Sik Lam** from The University of Hong Kong. The following are brief progress reports provided by the award winners.

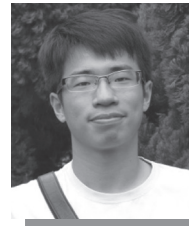
Yexin Deng has been making more progress in his research work



p-n diode based on phosphorene (a novel 2D material from an allotrope of phosphorus) and MoS₂, as well as high performance photodetector based on phosphorene. There works have been published on *ACS Nano*, and presented on the 2014 IEEE IEDM, respectively. He is currently working towards his Ph.D. degree.

Sik-Lam Siu received his BEng degree in electronic engineering from City University of Hong Kong in

on 2D electronics and optoelectronics. His most recent output has been demonstration of van der Waals heterojunction



working with microelectronic circuit design since 2008. His research interests included nano-device characterization, radio-frequency circuit design, power-management circuit design, and development of integrated sensing system.

*Carmen Lilley
EDS Student Fellowship
Committee Chair
University of Illinois at Chicago
Chicago, IL, USA*

2015 AWARDS - CALL FOR NOMINATIONS

CALL FOR NOMINATIONS 2015 EDS J.J. EBERS AWARD



The IEEE Electron Devices Society invites the submission of nominations for the 2015 J.J. Ebers Award. This award is presented annually for outstanding technical contributions to electron devices. The recipient(s) is awarded a plaque and a check for \$5,000, presented in December at the IEEE International Electron Devices Meeting (IEDM).

The J.J. Ebers Award on-line nomination form is available on the EDS web-site at <http://eds.ieee.org/jj-ebers-award.html>. The deadline for submission of nominations for the 2015 award is July 1, 2015.

If you have any questions or need further information on this award, please do not hesitate to contact Laura Riello of the EDS Executive Office at l.riello@ieee.org.



CALL FOR NOMINATIONS 2015 EDS EDUCATION AWARD



The IEEE Electron Devices Society invites the submission of nominations for the EDS Education Award. This award is presented annually by EDS to honor an individual(s) who has made distinguished contributions to education within the field of interest of the Electron Devices Society. The recipient(s) is awarded a plaque and a check for \$2,500, presented at the IEEE International Electron Devices Meeting (IEDM).

The nominee must be an EDS member engaged in education in the field of electron devices, holding a present or past affiliation with an academic, industrial, or government organization. Factors for consideration include achievements and recognition in educating and mentoring students in academia or professionals in the industrial or governmental sectors. Specific accomplishments include effectiveness in the development of innovative education, continuing education programs, authorship of textbooks, presentation of short-courses at EDS sponsored conferences, participation in the EDS Distinguished Lecturer program, and teaching or mentoring awards.

Since this award is solely given for contributions to education, the nomination should exclude emphasis on technical contributions to engineering and physics of electron devices.

Nomination forms can be found on the EDS web site

The deadline for the submission of nominations for the 2015 award is September 1, 2015.



CALL FOR NOMINATIONS 2015 IEEE EDS EARLY CAREER AWARD



Description: Awarded annually to an individual to promote, recognize and support Early Career Technical Development within the Electron Devices Society's field of interest

Prize: An award of US\$1,000, a plaque; and if needed, travel expenses not to exceed US\$1,500 for a recipient residing in the US and not to exceed US\$3,000 for a recipient residing outside the US to attend the award presentation.

Eligibility: Candidate must be an IEEE EDS member and must have received his/her first professional degree within the 10th year defined by the August 15th nomination deadline and has made contributions in an EDS field of interest area. Nominator must be an IEEE EDS member. Previous award winners are ineligible.

Selection/Basis for Judging: The nominator will be required to submit a nomination package comprised of the following:

- The nomination form that is found on the EDS web site, containing such technical information as the nominee's contributions, accomplishments and impact on the profession or economy and a biographical description.
- A minimum of two and a maximum of three letters of recommendation from individuals familiar with the candidate's technical contributions and other credentials, with emphasis on the specific contributions and their impacts.

The basis for judging includes such factors as: the demonstration of field leadership in a specific area; specific technical contribution(s); impact on the profession or economy; originality; breadth; inventive value; publications; honors; and other appropriate achievements.

Schedule: Nominations are due to the EDS Executive Office on August 15th each year. The candidate will be selected by the end of September, with presentation to be made in December.

Presentation: At the EDS Awards Dinner that is held in conjunction with the International Electron Devices Meeting (IEDM) in December. The recipient will also be recognized at the December EDS BoG Meeting.

Nomination Form: Complete the nomination form by August 15, 2015. All endorsement letters should be sent to l.riello@ieee.org by the deadline.

For more information contact: l.riello@ieee.org or visit: <http://eds.ieee.org/early-career-award.html>

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2015 PhD Student Fellowship

Description: One year fellowships awarded to promote, recognize, and support PhD level study and research within the Electron Devices Society's field of interest. The field of interest for EDS is all aspects of engineering, physics, theory, experiment and simulation of electron and ion devices involving insulators, metals, organic materials, plasmas, semiconductors, quantum-effect materials, vacuum, and emerging materials. Specific applications of these devices include bioelectronics, biomedical, computation, communications, displays, electro and micro mechanics, imaging, micro actuators, optical, photovoltaics, power, sensors and signal processing.

It is expected that three fellowships will be awarded, with the intention of at least one fellowship being given to eligible students in each of the following geographical regions every year: Americas, Europe/Middle East/Africa, and Asia & Pacific. Only one candidate can win per educational institution.

Prize: US\$5,000 to the student and if necessary funds are also available to assist in covering travel and accommodation costs for each recipient to attend the EDS Administrative Committee meeting for presentation of the award plaque. The EDS Newsletter will feature articles about the EDS PhD Fellows and their work over the course of the next year.

Eligibility: Candidate must be an IEEE EDS student member at the time of nomination; be pursuing a doctorate degree within the EDS field of interest on a full-time basis; and continue his/her studies at the current institution with the same faculty advisor for twelve months after receipt of award. Nominator must be an IEEE EDS member. Previous award winners are ineligible.

Basis for Judging: Demonstration of his/her significant ability to perform independent research in the fields of electron devices and a proven history of academic excellence.

Nomination Package

- Nomination letter from an EDS member
- Two-page (maximum) statement by the student describing his or her education and research interests, accomplishments and graduation date
- One-page biographical sketch of the student (including student's mailing address and email address)
- One copy of the student's under-graduate and graduate transcripts/grades. Please provide an explanation of the grading system if different from the A-F format.
- Two letters of recommendation from individuals familiar with the student's research and educational credentials. Letters of recommendation cannot be from the nominator.

Timetable

- Completed nomination packages are due at the EDS Executive Office no later than **May 15, 2015**
- Recipients will be notified by July 15
- Monetary awards will be given by August 15
- Formal award presentation will take place at the EDS Board of Governors Meeting in December

EDS is now accepting nomination package submissions via e-mail, fax and mail!

Email: edsfellowship@ieee.org

Fax: +1-732-235-1626

Mail:

IEEE EDS Executive Office
PhD Student Fellowship Program
445 Hoes Lane, Piscataway, NJ 08854 USA

For more information contact:
edsfellowship@ieee.org

Visit the EDS website:
<http://eds.ieee.org/eds-phd-student-fellowship.html>

**May 15, 2015
Submission Deadline**



2015 Masters Student Fellowship

Description: One-year fellowships awarded to promote, recognize, and support graduate Masters level study and research within the Electron Devices Society's field of interest: all aspects of engineering, physics, theory, experiment and simulation of electron and ion devices involving insulators, metals, organic materials, plasmas, semiconductors, quantum-effect materials, vacuum, and emerging materials. Specific applications of these devices include bioelectronics, biomedical, computation, communications, displays, electro and micro mechanics, imaging, micro actuators, optical, photovoltaics, power, sensors and signal processing.

Three fellowships will be awarded, with the intention of at least one fellowship being given to eligible students in each of the following geographical regions every year: Americas, Europe/Mid-East/Africa, Asia & Pacific. Only one candidate can win per educational institution.

Prize: US\$2,000 and a plaque to the student, to be presented by the Dean or Department head of the student's enrolled graduate program.

Eligibility: Candidate must be an IEEE EDS student member at the time of nomination; be accepted into a graduate program or within the first year of study in a graduate program in an EDS field of interest on a full-time basis; and continue his/her studies at a graduate education institution. Nominator must be an IEEE EDS member and preferably be serving as the candidate's mentor or faculty advisor. Previous award winners are ineligible.

Basis for Judging: Demonstration of his/her significant ability to perform research in the fields of electron devices and proven history of academic excellence in engineering and/or physics as well as involved in undergraduate research and/or supervised project.

Nomination Package

- Nomination letter from an EDS member who served as candidate's mentor or faculty advisor.
- Two-page (maximum) statement by the student describing his or her education and research interests, accomplishments and graduation date. This can include undergraduate, graduate and summer internship research work.
- One-page biographical sketch of the student (including mailing address and e-mail address)
- One copy of the student's transcripts/grades
- One letter of recommendation from an individual familiar with the student's research and educational credentials. Letters of recommendation cannot be from the nominator.

Timetable

- Completed nomination packages are due at the EDS Executive Office no later than **May 15, 2015**
- Recipients will be notified by July 15
- Monetary awards will be presented by the Dean or Department Chair of the recipient's graduate program at the beginning of the next academic term.

EDS is now accepting nomination package submissions via e-mail, fax and mail!

Email: edsfellowship@ieee.org

Fax: +1 732-235-1626

Mail:

IEEE EDS Executive Office
PhD Student Fellowship Program
445 Hoes Lane, Piscataway, NJ 08854 USA

For more information contact:
edsfellowship@ieee.org

Visit the EDS website:

<http://eds.ieee.org/eds-masters-student-fellowship.html>

**May 15, 2015
Submission Deadline**

YOUNG PROFESSIONALS

ICORLAB GEARING UP FOR THE 21ST CENTURY

CAN BAYRAM



Can Bayram
Department of
Electrical and
Computer Engineering
University of Illinois at
Urbana - Champaign

Growing world population and increasing energy demand call for energy savings in every aspect of our lives. In this respect, electrical engineering discipline develops continuously and propel novel technologies (such as electric cars, solar

energy, solid state lighting, and ultra-high-speed data communications) into our society. Yet I find educational and career challenges of electrical engineers, who bring these novelties into life, be similar to those once I faced.

More than a decade ago when I started my undergraduate education in the Electrical Engineering Department of Bilkent University (Ankara, Turkey), I had my first academic challenge: *Picking an area of concentration*. For the degree completion, (under)graduates today make their very first career decision via choosing classes from the diverse set of electrical engineering disciplines: Microelectronics/Photonics, Circuits, Electromagnetics, Bio-Imaging, Control, Power, Acoustics, Computing Systems, Networks... the list goes on.

I observe that students, who are exposed to individual research carried out at home institution, summer internships, and academic societies, are not only knowledgeable about the areas of concentration but also happy about their choices. Particularly nonprofit academic societies such as IEEE offer unique opportunities through (local) chapter meetings, newsletters, and webinars. Moreover, the membership cost for

subdivisions of IEEE, such as Electron Devices Society (EDS), are very affordable yet rewarding as EDS offers variety of educational and career benefits.

After I had decided to concentrate on Microelectronics/Photonics, I joined Center for Quantum Devices of Northwestern University (IL, USA) as a doctoral student. Thanks to my work on solid state lighting and quantum devices, IEEE EDS recognized me as a PhD Fellow in 2010. Such an exceptional recognition as a doctoral student motivated me go further in my research as well as opened up channels of networking with leading researchers.

Upon graduation, I joined IBM's Thomas Watson Research Center (NY, USA). My IBM journey had indeed begun during my doctoral studies, with being an IBM PhD Fellow. I joined a team developing high efficiency, light-weight, and flexible photonic devices. One of our breakthroughs is record-breaking specific power solar cells, which has received attention as the cover article in *Advanced Energy Materials*. We have also demonstrated thinnest inorganic light emitting diodes through a novel release mechanism that is published in *Nature Communications*. This work has been highlighted by popular press including *EE times*.

Later in my IBM career, I moved towards next generation electronics and combined my gallium nitride expertise with IBM's silicon technology know-how. This co-integration approach is quite interesting for power devices as gallium nitride devices outperform any silicon-only-based technology. Our work is selected as the frontispiece cover article in *Advanced Functional Materials* and

picked up by the popular magazines such as *Compound Semiconductor*, *Power Electronics World*, and *Semiconductor Today*.

IEEE EDS conferences are crucial for staying up-to-date, networking, and developing presentation skills. One instance is IEDM. During my IBM career, I recall many IBMers highlighting IEDM as one of the premier meetings to report on breakthroughs. This meeting is a good example with large attendance from both academia and industry. Today, with ever changing technology, multidisciplinary work and academia-industry interaction are essential. A major challenge for all of us is staying aware of the critical developments in our fields given so many diversification and publications. I found being a member of IEEE EDS rewarding as I am exposed to timely of-interest information on my own area.

At UIUC, I am establishing the Innovative COMpound semiconductor Laboratory (ICORLAB) so as to develop novel photonic and electronic devices for consumer, medical, and defense applications.

In photonics, our focus is engineering ultraviolet-to-visible light emitting diodes for various lighting applications. We engineer aluminum gallium indium nitride based emitters to cover two key spectra: ultraviolet and visible. Ultraviolet region is very important as many biological agents (such as anthrax, plague, and Ebola) can be detected and eliminated via such detectors/emitters. Thus high efficiency and compact ultraviolet LEDs find applications in sterilization such as enabling clean drinking water in remote locations of the world. Visible LEDs are critical for general lighting applications, and

we are looking into enabling visible LEDs for other (such as biomedical) lighting applications.

On the electronics side, we are developing next generation gallium nitride based power transistors. Notably, GaN devices employed in the power amplifier and in the power train of the buck converter allow power densities and performance unachievable with any silicon-only-based technology. This switch from silicon to gallium nitride devices is quite important as the latter

promises energy savings for power converters—used in ever-increasing data centers, electric vehicles, and solar farms.

I have been a member of IEEE EDS almost a decade and am glad to be able to contribute to and benefit from the EDS early in my career. Particularly I find EDS webinars very useful for following the most important developments in the field. There are recognition opportunities for various career levels (from students to engineers; from

scientists to professors) within the society, and I am proud to be recognized as the 2014 IEEE EDS Early Career Awardee. Such a prestigious recognition propels me to explore the fundamental limitations in energy conversion, and invent novel photonic and electronic devices. With increasing level of (scientific) information in the 21st century, it has never been more important to expose ourselves only to the critical information as we identify *time* and *energy* our most critical.

NEW CAREER RESOURCE ON EDS WEBSITE

To assist EDS members with finding employment and to support their career growth, the society website now provides an RSS feed that features a scrolling list of jobs related to electron devices, posted by technology employers looking to hire IEEE members. Upon clicking on a job in the feed, members will be taken to the main IEEE Job Site, where they can sign in and save their resume, favorite jobs, etc.

Use this link to access the RSS feed on the EDS website:
<http://eds.ieee.org/component/content/article/578.html>



IEEE Journal of Photovoltaics

Electronic Version FREE to EDS Members



<http://eds.ieee.org/jpv.html>



NEW EDITIONS TO THE EDS WEBINAR ARCHIVE

EDS is many things to its members—scientific publisher, technical conference sponsor, networking resource —but at its core EDS is a community of learning. From undergraduate students and PhD candidates to tenured professors and world-renowned researchers, EDS provides device engineers from across the spectrum engaging and enriching educational opportunities.

Launched in 2011, the EDS webinar series delivers live, interactive lectures right to your desktop with luminaries from the device engineering field. And, if you can't attend in person, you can always watch replays on the EDS site 24/7.

Recent Events:

Show Me the Money! Strategies and Tips for Taking Ideas from Concept to Funded Research Program

Presented by Kyle Montgomery, Steven Ringel and David Wilt

Abstract

This EDS Webinar, sponsored by the Young Professionals Committee, will examine a core aspect of many professions, from academia to industry—raising funds to support your research initiatives. Led by Kyle Montgomery of the Young Professionals Committee, this webinar will be a discussion with two distinguished EDS volunteers. Professor Steven Ringel from The Ohio State University will share insights from his long career in raising funds to support multiple research programs, including the Institute for Materials Research (IMR). David Wilt from the Air Force Research Laboratory will discuss his perspective as a Program Manager and share valuable insight to the review process that will aid you in preparing a strong proposal for your next research endeavor. Following a prepared discussion about valuable techniques and tips, we will open up the webinar for questions from audience members. Mark your calendar now for what will certainly be a valuable and useful discussion for all!

IEEE Women in Engineering Live Chat

Alice's Adventure in the Micro/Nano Field and Her Self-powering Life

Presented by Haixia (Alice) Zhang

Director of the Alice @ Micro-Nano Wonderlab, Peking University. Her major focus is the micro energy harvester for low power consumption devices and smart systems. She is the initiator of the International Contest of Applications in Nano-Micro Technologies (iCAN, since 2007), which has more than 10,000 students from all over the world involved each year. Trying her best to make sure every youth in the world can be motivated by "Yes, I CAN!"

The IEEE Women in Engineering Live Chat is brought to you by a partnership between the IEEE Electron Devices Society, the IEEE Nanotechnology Council, and IEEE Women in Engineering.



UNIVERSIDADE DE BRASILIA STUDENT BRANCH (CENTRO-NORTE BRASIL SECTION)

LUIZ FERNANDO DE ANDRADE GADELHA



Engineers Demonstrating Science:
an Engineer Teacher Connection

We are glad to share that Universidade de Brasilia Student Branch (Region 9, Centro-Norte Brasil Section) won "The Darrel Chong Student Activity Award 2014 – GOLD Level." The EDS-ETC Project (Projeto Electron) in conjunction with IEEE Women In Engineering (WIE) activities, are the main activity of this very active Student Branch.

The Darrel Chong Student Activity Award

The purpose of this recognition system serves to change the mindset of our student groups from being number-driven to becoming value-driven and to acknowledge exemplary student activities around the world. The goal is to improve the quality of activities and to foster knowledge sharing among students. Ultimately, the initiative is targeted at improving student-membership growth. This will encourage and motivate students to continue to innovate and implement meaningful ideas.

For a full list of the 2014 Darrel Chong Student Activity Award winners, visit http://www.ieee.org/membership_services/membership/students/awards/chong.html.



Members of the Universidade de Brasilia Student Branch wearing their Project Electron t-shirts proudly



A Project Electron workshop given by the Universidade de Brasilia Student Branch



Samar Saha
EDS President-Elect

Interested in knowing why it's not possible to measure the built-in voltage of a PN junction using a voltmeter? Do you need to understand the best way to derive an expression for the average thermal velocity of an electron? Or are you curious about what quantum dots and wires are? The answers to these questions and more are available through the QuestEDS Question and Answer page.

To ask a question not already addressed on the Q&A page, visit www.ieee.org/go/questeds. Technical experts answering the questions posed represent academic, government and industry sectors.

Questions are grouped into five technical categories and two general ones. Technical categories cover subject areas like semiconductor and device physics, process technology, device characterization and quantum electronics. Subject areas addressed are anticipated to expand in the future. Two other categories address questions pertaining to educational activities and general inquiries about society membership. Within a two week time frame from when the question is asked, an answer is posted online. Incoming questions are handled by an editor-in-chief who ensures that they fall within the technical scope of EDS and that they are adequately answered.

For an archive of past questions and answers, visit <http://eds.ieee.org/questeds/question-and-answer-page.html>.

Question 060-13:

Considering that an organic semiconductor, such as "Tips-pentacene", was spin-coated on top of an aluminium sheet, sintered and subjected to a final 3rd layer of gold (applied using a square shadow mask), what would be an appropriate set of formulas that would predict the current dynamics as a function of the voltage and geometry of the layers in this schottky device?

If the same experiment were performed, but this time applying the tips-pentacene by drop-cast, how should expectedly vary the results?

Does the rugosity of the layers affects the performance of the device? Why should one consider the rugosity relevant?

Answer 060-13:

Generally, to fabricate the vertical organic diodes, it is preferred to coat TIPS-pentacene on the top of Au, and then evaporate Al on the top of the TIPS-pentacene, since Al surface is very easy to oxidize. Typically, the Al/TIPS interface forms a large barrier for injection of holes from Al into the HOMO level of TIPS-pentacene. In contrast, Au electrode has a very low barrier for injection of holes into the HOMO level of TIPS-pentacene. Therefore, assuming perfectly injecting ohmic contacts of Au electrode with TIPS-pentacene, the forward-biased current (flowing from the Au electrode to the Al electrode) can be described by the space-charge-limited current density [1]. The reverse-biased current can be described by Schottky diode reverse current model [2]. The main difference to the classical Schottky diode theory is that the organic semiconductor layer is always fully depleted due to the very low carrier density, and thus the devices could show a voltage-independent, constant reverse-bias capacitance [3].

For solution processed TIPS-pentacene devices, the different coating processes could form thin films with different crystalline structures, which then affect the contact properties and bulky trap states. Therefore, the electrical characteristics could be influenced. Currently, there have been very few experimental studies on solution processed organic small molecule diodes, and this area is worth further investigation.

References

- [1] M. Raja, et al., "Modelling of polymer Schottky diodes for real device applications," Proc. of ESSDERC, 2005, pp. 253–256.
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- [3] C.H. Kim, et al., "Capacitive behavior of pentacene-based diodes: quasistatic dielectric constant and dielectric strength," J. Appl. Phys., vol. 109, no. 8, pp. 083710-1–083710-9, Apr. 2011.

CHAPTER NEWS

REPORT ON THE DECEMBER 2014 EDS REGIONS/ CHAPTERS MEETING



"Joe" Xing Zhou
EDS Vice President-
Regions/Chapters

The EDS Regions/Chapters (R/C) meeting was held in December 2014 in San Francisco, California and was attended by 15 committee members and volunteers. Many items were discussed at

the meeting, including newly formed and potential chapters, Chapter of the Year (CoY) awards, the sub-committees for regions/chapters (SRC) budget utilization/allocation, and mini-colloquia/distinguished lecturer (MQ/DL) programs.

Since we adopted regional-based CoY awards two years ago, we have encountered issues of having low submission rates. The R/C committee discussed various ways to improve the situation, including more prestigious society-level CoY award while keeping current regional awards as well as CoY awards for student branch

chapters to increase participation. As the regional CoY awards have only been in practice for two years, the EDS Forum decided to let it run for another year. In the meantime, I would like to call for all chapters' pro-active participation in the CoY awards program. Information on CoY award nominations can be found on the EDS website (<http://eds.ieee.org/chapter-of-the-year-award.html>).

The Sub Committee for Regions/Chapters (SRC) scheme was created many years ago for effective bridging of EDS with chapters in various regions. We have given SRC chairs/vice-chairs more authorities and responsibilities in coordinating regional activities, such as arranging for chapter visits, initiating MQs and linking DLs with chapters. The meeting discussed ways to give more incentives for better and efficient utilization of the SRC budgets, which will be implemented in 2016.

The MQ/DL programs, now under the purview of the Vice President of

Regions and Chapters, have been very successful in serving our members and chapters. This year EDS has increased the MQ budget by \$10K, with a total \$100K budget for the MQ/DL programs. We wish that this investment be fully and effectively used toward our chapters and members, and as a way of assisting our DLs and volunteers. We would like to call for more coordinated efforts in MQ/DL organizations, for which individual chapters, R/C committee members, as well as SRC chairs/vice-chairs can all play a pro-active role. We encourage more resource sharing, such as joint MQs and DL travels on side trips. With everyone's contribution, let's make these programs even better in serving our members and rewarding our volunteers.

"Joe" Xing Zhou
EDS Vice President-Regions/
Chapters

*Nanyang Technological University
Singapore*

IEEE EDS SOUTH ASIA CHAPTERS MEETING

The IEEE EDS South Asia Chapters meeting was held at Centre for Nano Science and Engineering (CeNSE), IISc, Bangalore, India on December 5, 2014. This is the 11th meeting of Chapter Chairs from this region, which is normally held every year. Currently, there are 21 EDS Chapters in the South Asia region out of which 10 are Student Chapters. Main objective of these meetings are the coordination of activities between Chapters and effective communication. This 2014 meeting was attended by Samar Saha (EDS President-Elect)

and Ravi Todi (EDS Treasurer) and MK Radhakrishnan (EDS BoG Member and Region 10 SRC Vice Chair), apart from Chapter Chairs and representatives. The meeting was held in conjunction with ICEE 2014, and was hosted by the IEEE ED/SSC Bangalore Chapter.

In his deliberations Ravi Todi explained the overall EDS activities, chapters' functioning, importance of SRC and how EDS supports various chapter activities in different regions. The summary of various Chapter activity reports were presented and

reviewed. Three new Chapters were formed in 2014 – ED Kalyani Student Chapter at Calcutta, ED VIT Chennai Student Chapter and ED Coimbatore Chapter. It was decided to start a common web link for the EDS South Asia Chapters group, through which more efficient communication can be made. For more effective utilization of EDS DL resources and funds, it is planned to have joint MQ activities by Chapters. MKR suggested various modes of obtaining self-sustainability for Chapters. All Chapters may work towards self-sustainability



Attendees of EDS South Asia Chapter meeting in Bangalore on December 5, 2014

than relying on the subsidies for activities. By organizing value added events like workshops and seminars and charging a nominal sum for attendance, with proper discount to IEEE members, funds can be raised and can be used as reserve fund for Chapters.

Samar Saha suggested that Chapters' feedback is required for effective working of the Society

and he encouraged all Chapters and members to communicate. All Chapter Chairs are requested to submit their activity reports regularly, as when a program is completed, through L31 forms to EDS HQ and SRC. Further, it was decided that all requests for MQs as well as Chapter subsidy must be copied to Region 10 SRC Chair and Vice-Chairs, so that effective utilization of funds can

be monitored and guided. All the attendees expressed satisfaction over the successful organization of an important conference ICEE and thanked the ED/SSC Bangalore Chapter and CeNSE for organizing the event.

*MK Radhakrishnan
EDS BoG Member and
Region 10 SRC Vice-Chair*

REPORT ON THE IEEE EDS WIMNACT SERIES - CHINA

IEEE EDS WIMNACT (Workshop and Mini-Colloquium on Nanometer CMOS Technology) series held 3 distinctive programs in China during November 27–28, 2014. Three MQs were held in three different academic institutions which enabled to cater to a wide group of professionals including academicians and students, initiating many interactions and discussions between the speakers and the attendees.

WIMNACT – 42 at Shanghai *–by Yu-Long Jiang, ED/CPMT Shanghai Chapter Chair*

The first MQ, WIMNACT-42 was jointly organized by the IEEE ED/CPMT Shanghai Chapter and Fudan University, on November 27, 2014 at Fudan University, which was co-sponsored by the Centre of Excellence in Nanoelectronics, Fudan University.

This MQ had four talks by EDS Distinguished Lecturers: Dr. MK Radhakrishnan of NanoRel Technical Consultants, Prof. Steve S. Chung of National Chiao Tung University, Prof. Xing Zhou of Nanyang Technological University, Prof. Ramgopal Rao of IIT Bombay.

The event was attended by about 70 members and non-members, from local academic and industry, including Fudan University, East China



Audience at WIMNACT 42

and discussed the strategies of the Society, regional activities, chapter incentives, and promotion opportunities offered by the EDS. After the talks, EDS officers, Prof. Zhou VP, Regions/Chapters and Prof. Chung, EDS Region 10 SRC Chair, had active discussions with student representatives on the ways to establish student chapters in the Shanghai region and how to attract students to join IEEE EDS as new members.

WIMNACT – 43 at Nanjing

*–by Weifeng Sun, Vice-Chair,
ED/SSC Nanjing Chapter*

The 43rd WIMNACT was held at the Sipailou campus of Southeast University in Nanjing, China, on November 28, 2014. It was jointly organized by IEEE Nanjing ED/SSC Chapter and School of Electronic Science & Engineering, Southeast University. Prof. Litao Sun from Southeast University gave the opening address for the program which had three EDS Distinguished Lectures. Prof. Ru Huang of Peking University gave the first talk on “*Emerging Devices with Structure Engineering and Mechanism Engineering for Low Power Applications*.” The DL by Prof Steve S. Chung of National Chiao Tung University was on “*The Random Dopant Fluctuation and Random Trap Fluctuation of the Trigate FinFETs*” and Dr. MK Radhakrishnan of NanoRel



ED/CPMT Shanghai Chapter officials and EDS Distinguished Lecturers

Normal University, Shanghai University, Chinese Academy of Sciences, Shanghai Huali Microelectronics Co., and CISCO China. The chapter chair, Prof. Yu-Long Jiang, welcomed the gathering. MK Radhakrishnan, gave the first talk on “*Interface Physics in Silicon Nanodevices*,” followed by Steve S. Chung on “*The Random Dopant Fluctuation and*

Random Trap Fluctuation of the Trigate FinFETs, Xing Zhou on “*A Unified Compact Model for GaN-Based HEMTs*” and Ramgopal Rao, on “*Polymer Nano-Electro-Mechanical-Sensor Systems for Healthcare and Environmental Applications*.”

Besides the technical talks, Xing Zhou, EDS Vice President of Regions/ Chapters, gave a brief introduction



Speakers and attendees of WIMNACT 43 at Nanjing



WIMNACT-44 – Speakers with the attendees at Hangzhou

Technical Consultants, Singapore, gave the DL on “*Interface Physics in Silicon Nanodevices*.” About 100 students and professors from Southeast University and Nanjing University attended this event which covered three different topics of research interests.

Prof. Steve Chung gave an introduction of EDS activities and discussed the strategies of the Society, regional activities, chapter incentives, and especially opportunities for student members in the Society. Students asked many questions and discussed with EDS officers, Steve Chung (EDS Region 10 SRC Chair) and MK Radhakrishnan (EDS SRC Region 10 Vice-Chair) on the incentives for the students to join as EDS member, how to invite DL lecturers and the motivations on establishing possible student branch chapters.

WIMNACT – 44, Hangzhou

–by Wenjun Li, ED Hangzhou Chapter

The 44th Workshop and IEEE EDS Mini-Colloquium on Nanometer CMOS Technology (WIMNACT-44) was organized by the ED Hangzhou Chapter at the Hangzhou Dianzi University, on November 28, 2014. Over 150 researchers, engineers, students and professors from Hangzhou and Zhejiang University as well as from industries attended the event. The objective of the MQ was to present the topics of interests in nano-devices and modeling, and a special topic on the applications of bioelectronics.

The event started with a welcome and opening address by Prof. Wenjun Li, secretary of the ED Hangzhou Chapter. Prof. Zhou, EDS VP of Regions/Chapters, briefly introduced the strategies, regional activities, chapter incentives and promotion

opportunities of the Society. Distinguished Lecturers were: “*A Unified Compact Model for GaN HEMTs*” by Prof. Xing Zhou, Nanyang Technological University, Singapore; “*Top down meets Bottom-up: An integrated approach for Nanoscale Devices*” by Prof. Ramgopal Rao, IIT Bombay, India; and “*Micro-electrode Array for Communication Between Silicon Chip and Living Cells*” by Prof. Mansun Chan, Hong Kong University of Science & Technology, Hong Kong.

After the lectures, the EDS officers, Prof. Zhou (EDS VP Regions/Chapters), Prof. Mansun Chan (Vice-Chair, ED SRC Region 10), Prof. Ramgopal Rao (Vice-Chair, ED SRC Region 10), discussed with chapter officers and professors on how to promote chapter activities, and especially on how to attract students to join IEEE and EDS.

REPORT OF ICEE-2014 CONFERENCE

The 2nd International Conference on Emerging Electronics (ICEE 2014) was held in Bangalore, India, December 3–6, 2014. ICEE, a biennial conference is the brain child of the IEEE EDS South Asia Chapters Meetings, to fulfill the need of a Devices meeting in the region to discuss the latest trends in the emerging areas.

All the EDS Chapters in South Asia are the stake-holders of this conference which is technically co-sponsored by the IEEE Electron Devices Society. ICEE 2014 was organized jointly by the IEEE ED/SSC Bangalore Chapter and the Centre for Nano Science and Engineering (CeNSE), Indian Institute of Sci-

ence, Bangalore. The wide range of topics and scope of the conference was reflected in the more than 15 different sessions containing 11 technical symposia running simultaneously over a period of 3 days, and also in the pre-conference tutorials spreading over 6 topics of emerging electronics, such as,



ICEE-2014 Session audience

Photovoltaics, Graphene, Modeling and Simulations, Sensors, GaN electronics, and Photonics. The Conference had an exciting dynamic brought about by countless fields

of individual research that are still united by a common core.

The three-day conference program had 15 technical sessions, 8 plenary lectures, 2 public lectures

and 30 invited talks as well as 100 oral and poster presentations. The pre-conference tutorial day had 8 tutorial workshops. The plenary speakers included Krishna Saraswat of Stanford University, Jerney Levy of University of Pittsburgh, J. Parpia of Cornell and A.C. Huber of CUT, Germany. The two public lectures were delivered by Rao Tummala of Georgia Tech and Stuart Parkin of Max Plank Institute.

More than 500 active researchers attended the conference as participants from eight countries. The next ICEE conference will be held in 2016 at IIT Bombay and organized by the IEEE ED/AP Bombay Chapter.

Sanjeev Srivastava
2014 ICEE Organizing Chair

V JanakiRaman
IEEE ED/SSC Bangalore Chapter Chair

ELECTRONIC WINTER CAMP TO FOSTER FUTURE ENGINEERS

The IEEE Hong Kong ED/SSC Chapter and the Hong Kong University of Science and Technology co-organized a 3-day Electronic Winter Camp on December 29–31, 2014, to let primary and secondary students with ages ranging from 10 to 15 to experience the fun of electronic designs. This is the third time the camp is offered and it has become a major annual event for the chapter. It also represents the chapters mission to reach out to the community and young people in addition to serving its members. The instructors and student helpers are all Undergraduate Electronic Engineering students. In the camp, the young children have constructed various electronic gadgets such as running light, electronic piano, infrared transmitter/receiver and digital counter on breadboards with generic components. In addition to stimulate the interest of young children to electronic design, the camp



Winter Camp participants at the Hong Kong University of Science and Technology



also provided an opportunity for the university students to practice their presentation and organization skills.

The camp was a big success with more than 70 participants and the youngest only 10 years old. The participants were excited about the projects and asked many questions, resulting in a lot of discussions. The camp has successfully aroused the interest of the students to electronic engineering and everyone enjoyed the camp with lots of laughter.

Mansun Chan
Region 10 SRC Chair

AN EVENING WITH CHILDREN

The IEEE Singapore REL/CPMT/ED Chapter engaged the evening of November 8, 2014, through a social and humanitarian event in which a dinner and movie screening for children from “Chen Su Lan Methodist Children’s Home” was held. We had a wonderful evening with the families and children—a total of 120 participants. Dinner was at “The Chop

House” followed by a movie screening at the Vivo City Golden Village cinema. “The Book of Life,” chronicles the journey of Manolo, a young man torn between fulfilling the expectations of his family and following his heart. Rich with a fresh take on pop music favorites, The Book of Life encourages us to celebrate the past while looking forward to the

future. We would like to thank the committee members and families who had helped to make this social event successful and meaningful. A special thank you to Jasmine Leong for her help in organizing the event.

Gan Chee Lip
IEEE REL/CPMT/ED Singapore
Chapter Chair

*Leveraging Technology
for a Better Tomorrow*

IEEE Day

6 OCTOBER 2015

SAVE THE DATE — CELEBRATE IEEE DAY

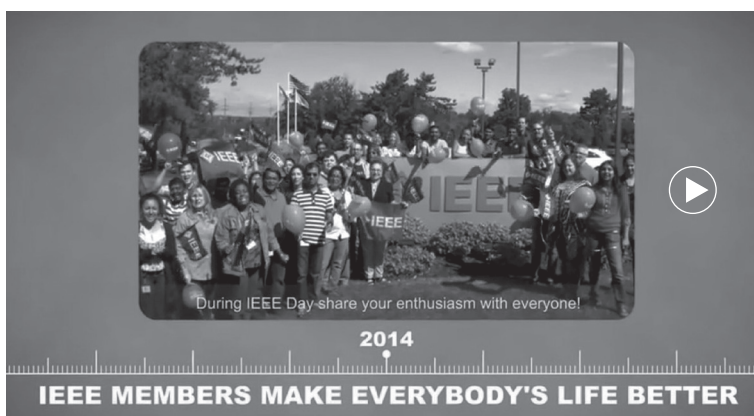
[HTTP://WWW.IEEEDAY.ORG](http://www.ieeeday.org)

Get Involved

Preparations for IEEE Day 2015 are underway for the 6th time in history when engineers worldwide will celebrate the anniversary of the first time members gathered to share their technical ideas in 1884.

Organize and collaborate to bring IEEE Day joy to your local group. There are many fun ways to participate. Use the IEEE Day event map to look up the various ways IEEE chapters celebrate around the world: <http://www.ieeeday.org/local-events/>.

Start planning your event soon and don’t forget to network online and promote it on social media sites.



<http://www.youtube.com/watch?v=C3-vBcsOdkU&feature=youtu.be>

IMPORTANT REMINDER TO CHAPTER MEMBERS

- Changes to chapter officers need to be submitted to both IEEE and EDS
- Please report changes to IEEE via the vTools.OfficerReporting tool
 - (Access to the tool requires use of an IEEE Account)
- To report officer changes to EDS, please submit a chapter chair update form
 - <https://ieeeforms.wufoo.com/forms/pgu6n1i1ixepnu/>

REGIONAL NEWS

USA, CANADA & LATIN AMERICA (REGIONS 1-6, 7 & 9)

ED Mid-Hudson Valley Chapter

—by Mukta Farooq

On April 23, 2014, the ED Mid-Hudson Valley Chapter hosted a first-of-its-kind event by an EDS chapter – a live webinar broadcast from the chapter located in Fishkill, New York to EDS Chapters around the world. The talk was given by Dr. Stewart E. Rauch III, an EDS DL (Distinguished Lecturer) and faculty member at SUNY New Paltz, on **Terrestrial Radiation Induced Soft Errors in Integrated Circuits**. The talk was attended locally by about 25 people as well. A brief abstract of that talk follows. The impact of background radiation on microelectronics is generally unappreciated. Soft errors, or single event upsets, are random, transient, recoverable failures unrelated to any defects or device shifts. There are three main terrestrial sources of radiation that cause soft errors in integrated circuits. The discoveries of these various mechanisms are discussed from a historical perspective, and the current physical understanding of each is presented. Next, methods used to test and model the soft error rate of circuits are explained. Finally, process, technology, and circuit mitigation techniques, and the effects of scaling, are covered.

Dr. Souvik Mahapatra, EDS DL and faculty member at IIT Bombay gave a talk on May 5, 2014. Topic was **"Bias Temperature Instability in HKMG MOSFETs - Characterization, Process Dependence, DC / AC Modeling and Stochastic Effects"**. The talk was attended locally by about 25 people. A brief abstract follows. A

common framework involving mutually uncorrelated trap generation and trapping sub-components is introduced to explain NBTI and PBTI degradation in HKMG MOSFETs. The framework can explain experimentally observed impact of different HKMG processes on BTI, including that of IL scaling and Nitridation. The underlying trap generation and trapping sub-components are independently verified by direct characterization techniques, and their relative impact on overall BTI is established for different HKMG processes. The similarities and differences between NBTI and PBTI mechanisms are highlighted using carefully designed HKMG process splits. A comprehensive physics-based model is established for prediction of time evolution of degradation and recovery during and after DC and AC stress at different bias and temperature, and AC stress at different frequency and duty cycle. The model can predict end-of-life degradation for DC and AC stress. The framework is extended to explain stochastic BTI observed in small area devices. The relative impact of process variability and BTI variability is discussed. Finally, a SPICE compatible compact model is introduced for macroscopic and stochastic BTI.

The Chapter organized a mini-colloquium on November 19, 2014, called the **"IBM Semiconductor Technology Symposium"**. This is the 6th consecutive year of this program. The topic this year was the IoT (Internet of Things), for which an invited panel of distinguished speakers from academia and industry gave talks. These included Rob Aitken from ARM: "Device and Technology Implications of the IoT"; Bill Gerhardt from Cisco: "Accelerating Innovation through IoT"; John Thomson from IBM: "Bringing Clarity to the IoT"; and Steven Feiner from Columbia University: "Seeing

through Augmented Reality". After the morning session of invited speakers, the afternoon sessions consisted of technical papers on multiple topics including Device Characterization, Reliability, Semiconductor Manufacturing, and Process Technology. The event was attended by 300+ people on site. Additionally there was a live webcast to Burlington, Vermont and Bangalore, India.

—Mukta Farooq, Editor

IEEE Hawaii Section

—Cor Claeys

The University of Hawaii IEEE Student Branch and IEEE Hawaii Section organized an IEEE EDS Distinguished Lecture (DL) on October 16, 2014, at the University of Hawaii, Manoa Campus.

Prof. Cor Claeys of imec and KU Leuven, and EDS Distinguished Lecturer, presented a talk titled, **"Trends and Challenges in Micro- and Nanoelectronics for the Next Decade"**. The audience of this event, of approximately 30 people, was composed of University staff, students and invited guests.

Since imec is a world leading R&D center in micro- and nanoelectronics, the lecture gave an overview of the present CMOS scaling activities and the strong innovation



Prof. Cor Claeys (middle), accompanied by the Dr. John Borland (left, Hawaii Section Chair) and Mr. Kenny Luong (right, IEEE Hawaii Student Branch Chair)



Prof. Cor Claeys

drive of these technologies in More than Moore applications related to ambient intelligence, automotives, molecular electronics, nano-biotechnology, polymer electronics, human and Internet of Things.

Earlier this year, on June 12th another EDS Distinguished Lecture was given by Dr. Subramanian S. Iyer from IBM, on *"Orthogonal Scaling to extend Computing into the Cognitive Era"*.

ED South-Brazil

University of Sao Paulo, Brazil
—by Joao Antonio Martino

The Polytechnic School of the University of Sao Paulo and the ED South-Brazil Chapter organized the First Hands-on on Microelectronic Fabrication of SOI nMOSFET of Latin America at University of Sao Paulo for educational application.

The graduate and undergraduate student had an opportunity to design the main step process parameters, to perform the fabrication (clean room)



The organizers: Joao Antonio Martino, Marcelo Carreno and Ricardo Rangel from University of Sao Paulo (fourth, fifth and eighth from right to left) and some of the students

and the electrical characterization of the SOI nMOSFET fabricated.

This hands-on fabrication was held at University of Sao Paulo on August 2014 (40 hours – one week) using only three photolithograph steps and self-aligned polysilicon-gate Fully Depleted SOI nMOSFET.

On a p-type SOI wafer with doping concentration around 10^{15}cm^{-3} , $\langle 100 \rangle$ crystallography orientation, silicon film of 100 nm and a buried oxide layer of 200 nm we start the fabrication of device. The simplified steps are the following: 1) Thermal Oxidation; 2) Boron Ion Implantation for threshold voltage (V_{TH}) definition and annealing; 3) First Lithography (Active Region Definition); 4) Etch of SiO_2 over silicon film; 5) Gate Oxidation; 6) LPCVD Poly-Si Deposition; 7) Poly-Si Doping (Phosphorous); 8) Second Lithography (Poly defini-

tion); 9) Phosphorous Ion implantation (source/drain doping) and annealing; 10) Etch of SiO_2 over source and drain. 11) Metal Deposition; 12) Third Lithography (definition of Aluminum).

This course was opened for everyone of EDS Region 9, who were interested in this subject. The limitation is due to the clean room facilities and it is 12 people per course.

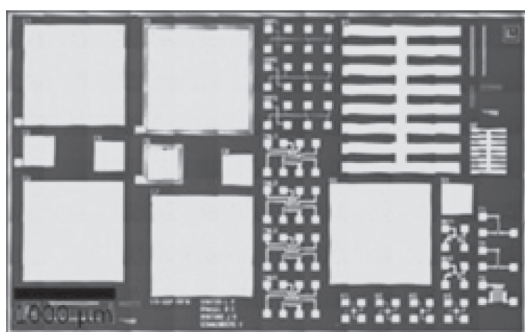
For additional information, contact Professor Joao Antonio Martino at martino@usp.br.

ED Venezuela

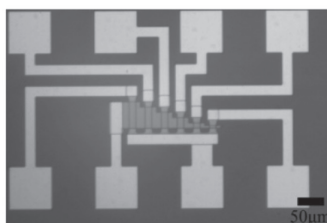
Simón Bolívar University, Venezuela
—by A. Ortiz-Conde

Continuing Venezuela's Chapter series of technical seminars and workshops, a technical lecture was held on Tuesday December 16, 2014, at Simón Bolívar University, Caracas. The special invited lecturer on this occasion was Ramón Salazar, who talked on the topic of *"Toward Low-Power Electronics: Tunnel Field Effect Transistor."* Ramón is presently a Ph.D candidate at Purdue University, USA, under the guidance of Prof. Joerg Appenzeller.

More than 30 faculty members as well as graduate and undergraduate students actively participated in the seminar. There was a very lively involvement of the audience in discussions, and the many interesting



(a)



(b)

(a) Test Chip fabricated at University of Sao Paulo (USP) during the Hands-on on microfabrication of SOI nMOSFET; (b) Transistor Array down to $0.4\ \mu\text{m}$



Ramón Salazar (left) during his presentation and with a part of the audience

questions and answers motivated additional informal meetings which took place after the conclusion of the official seminar.

For additional information, contact Professor Adelmo Ortiz-Conde at ortizc@ieee.org.

~Joao Antonio Martino, Editor

EUROPE, MIDDLE EAST & AFRICA (REGION 8)

ED Poland

~by Zygmunt Ciota and Mariusz Orlikowski

On December 2, 2014, Łódź, Poland, a joint meeting was held with the IEEE ED Poland Chapter, and the Section of Microelectronics of Committee of Electronics and Telecommunication of Polish Academy of Science and Commission of Electronics and Photonics - URSI Poland. The meeting began with a presentation by Prof. Jan Dziuban from Poznań University of Technology, "New Microelectronic Revolution: Microsystems, Miniaturized Instrumental Systems and Internet." Afterwards, Dr. Rafał Długosz presented a lecture entitled, "Low-Power Embedded Integrated Circuits Working in Parallel and Asynchronous Mode." The audience of this event, more than 40 people, was composed of DMCS staff (Łódź

University of Technology) and guests from all the main Polish institutes involved in electron devices researches. The current state and prospective development of MEMS and Microsystems design and production in Poland were discussed at the end of the meeting. As a conclusion the most important steps for the nearest future were identified.

~Zygmunt Ciota, Editor

ED Scotland

~by Anthony Walton

At the end of 2014, members of the Scottish Chapter of EDS and their guests were invited to visit the premises of Forth Dimension Displays in Dalgety Bay, Fife. Originally founded in 1998 as Micropix, Forth Dimension Displays has since become a world leader in the design

and manufacture of near-to-eye microdisplays based on high-speed, ferroelectric liquid crystal on silicon technology. These microdisplays are widely used in demanding, high performance applications such as virtual reality, medicine, defence and high-end camera viewfinders.

A group of nine were treated to a tour of the company's facilities where they were shown the production of the microdisplay devices. This was followed by an informative presentation from Greg Truman, the CEO of the company. The tour group were unanimous in their enjoyment of the event and keen interest was shown in future industrial visits. The Chapter's thanks go to all the staff at Forth Dimension Displays for their kind efforts during the visit.

~Jonathan Terry, Editor



ED Scotland chapter members and guests following their tour of the facilities at Forth Dimension Displays and a presentation by CEO, Greg Truman (far right)



From the all-day workshop "Memristive Devices and Neuromorphic Applications"

IEEE Swiss Memristive Devices and Neuromorphic Applications Workshop

—by Shih-Chii Liu

The first IEEE Swiss Memristive Devices and Neuromorphic Applications workshop took place at the Irchel Campus, University of Zurich on November 28, 2014. This workshop was co-organized by the IEEE CAS/ED Swiss Chapter and IBM Research Zurich. Eight experts from different institutions in Europe and in Switzerland presented their recent work on advances in memristive devices such as phase change memory, memristor device physics, neuromorphic chips, memristor device models, and the potential applications of memristors in deep neural networks. The workshop concluded with a lively apero combined with a dozen posters and demos. The workshop had over 75 registered participants from various institutes and companies in Switzerland and Europe.

~Jan Vobecky, Editor

ASIA & PACIFIC (REGION 10)

IEEE Distinguished Lecture on 3D IC Integration and Packaging

—Yu-Long Jiang

On December 1, 2014, IEEE Distinguished Lecturer John H Lau,

presented a talk on 3D IC Integration and Packaging at Fudan University, Shanghai, China. The event was hosted by Prof. Yu-Long Jiang, the chair of the IEEE ED/CPMT Shanghai Chapter. More than 40 attendees from the local region shared Lau's excellent talk.

In his talk, Lau mentioned that 3D IC integration is taking the semi-

conductor industry by storm. It has been: (a) impacting the chip suppliers, fab-less design houses, foundries, integrated device manufacturers, outsourced semiconductor assembly & test, substrates, electronic manufacturing service, original design manufacturers, original equipment manufacturers, material and equipment suppliers, universities, and research institutes; (b) attracting the researchers and engineers from all over the world to go to conferences, lectures, workshops, panels, and forums to present their findings, exchange information, look for solutions, learn the latest technologies, and plan for their future; and (c) pushing the industry to build standards, infrastructures, and ecosystems for 3D IC integration.

He also pointed out that people think that Moore's law is going to roll off soon and 3D IC integration can be the solution. The potential applications



IEEE Distinguished Lecturer John H. Lau



Yu-Long Jiang, chair of IEEE ED/CPMT Shanghai Chapter (front row 1st from left), and IEEE Distinguished Lecturer, John H Lau (3rd from left), with some of the attendees

and high volume manufacturing of 3D IC integrations can be classified into 4 groups, namely; memory-chip stacking, wide I/O DRAM 2 or hybrid memory cube (HMC), high bandwidth memory (HBM), and wide I/O interface (or 2.5D IC integration).

John is the Senior Technical Advisor of ASM. With more than 35 years of R&D and manufacturing experiences, he has authored more than 430 papers and 17 books in electronics packaging. He is an ASME fellow and an IEEE fellow.

Report on 2014 IEEE Student Symposium on Electron Devices and Solid-State Circuits

—by Mansun Chan

The IEEE ED/SSC Hong Kong Chapter hosted the IEEE Student Symposium on Electron Devices and Solid-State Circuits on December 5, 2014, at Lim Por Yen Lecture Theatre Two of the Hong Kong Polytechnic University. The aim of this symposium is to provide an opportunity for the students to present their research results and exchange ideas with peers in the community. There were 19 student papers accepted for presentation among different institutions in Hong Kong. In addition to demonstrating their work in a poster session, each student gave a 10 minute presentation about his/her research work, followed by a question and answer session. The presentations were

excellent and provided the audience with a lot of useful information. Eight professors from various universities in Hong Kong attended this symposium to facilitate the discussion among the students and be the judges for the Best Student Paper Awards. Professor Mansun Chan, Chairman of the IEEE ED/SSC Hong Kong Chapter, presented the awards to the students who received the Best Paper Awards and also gave a closing remark.

ED Peking University

—by Xiaobo Jiang

The ED Peking University (PKU) Student Chapter held one distinguished lecture on October 24, 2014. Prof. Hiroshi Iwai from Tokyo Institute of Technology was invited to deliver an IEEE Distinguished Lecture entitled “*Future of Logic Nano CMOS Technology*,” in which he thoroughly

explained the past, now and future of logic MOS technologies. First, he gave a brief review on the history of logic MOS technology scaling. Then, he presented the challenges we’re facing today and the solutions we’ve come up with, like multi-gate devices and FDSOI MOSFETs. At last, he gave an anticipation on the major difficulties of MOSFETs downscaling to deep sub-10nm. There were about 60 attendees at this event, with several of our members and students fortunate to have a discussion with Prof. Iwai afterwards.

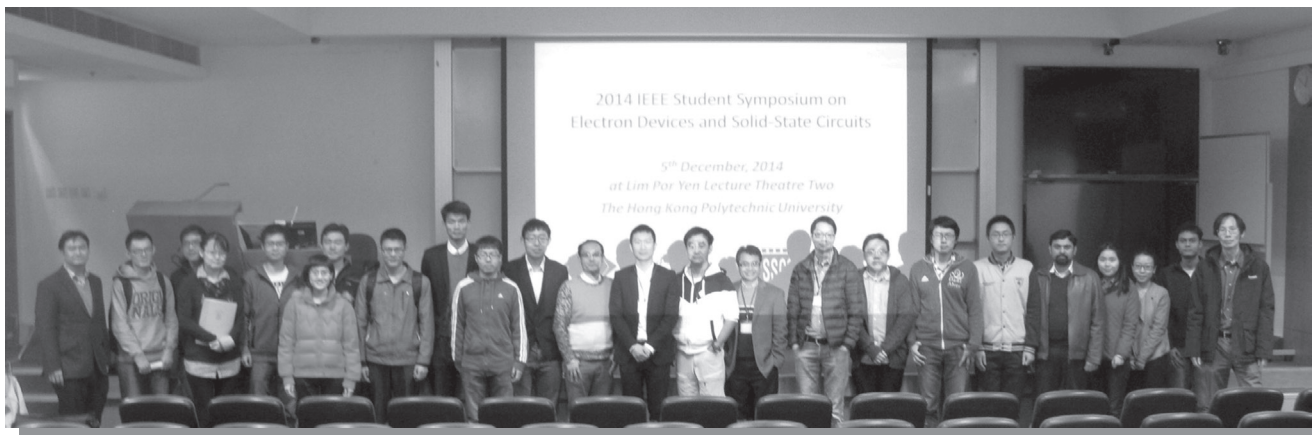
ED Taipei

—by Steve Chung

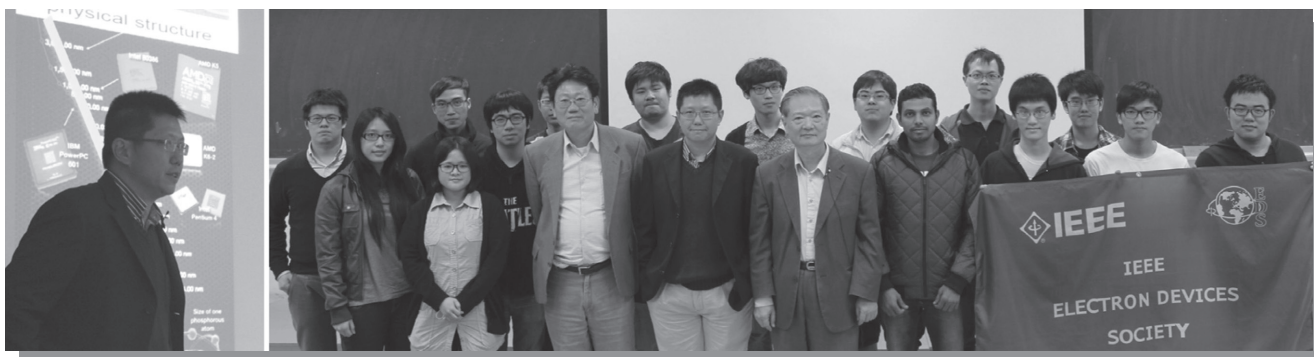
The ED Taipei Chapter held two invited talks in the fourth quarter of 2014. The first invited speaker was Prof. G. C. Liang, from National University of Singapore. On November 17th, he gave a talk on “*Nanoscale*



Prof. Hiroshi Iwai (front row, 5th from the left) pictured with Prof. Ru Huang (4th from left), the chapter advisor and other members of the Chapter



Judges and student presenters of the 2014 IEEE ED/SSC Student Symposium



ED Taipei, November 17 – (left) G.C. Liang (speaker), and (right, 1st row from left) G. C. Liang (4th), Steve Chung, seminar host (5th)



ED Taipei, December 30 – (left) Ming Liu (DL speaker), (right, 1st row from left) Steve Chung, seminar host (4th), Ming Liu (5th), T. Y. Tseng (6th), and T. H. Hou (7th)

FETs and Other Novel Functional Devices based on the low dimensional structures. As we will soon reach the end of Moore's law, two-dimensional materials, such as graphene, MoS₂, etc., have been extensively studied and received considerable interests. In his talk, he first gave the introduction to the current development of the FET-related devices and novel functional devices, followed by introducing the fundamentals of material properties of these advanced 2D materials including graphene and beyond graphene, such as transition metal dichalcogenide (TMD), silicene, Bi₂Se₃, etc. Finally, a general modeling procedure, was applied to investigate the device physics/performance of conventional FETs, tunneling FETs, NEMs, spin filters and other potential devices for low power, high performance applications. This talk was attended by more than 90 students and professors/researchers.

The second DL arranged on December 30th, invited Prof. Ming Liu

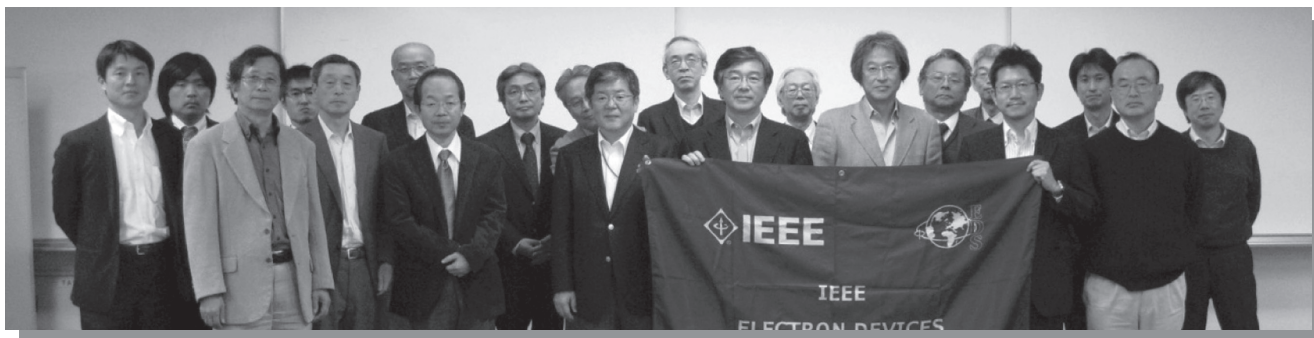
from the Institute of Microelectronics, (IME), Chinese Academy of Sciences (CAS). Her talk entitled, *"The Development and Challenges of Nonvolatile Memory with Focus on CBRAM switching Mechanism,"* in which the organization, the research areas of her team and the status of the CAS with more than 100 institutes nation-wide was introduced. Then, on the subject of the technical talk, she presented first the most recent progress on the development of nonvolatile memory, followed by the focus on the recent study of CBRAM. While, presenting the switching mechanism with conductive ions as the dominant mechanism in a CBRAM, a nano-crystal structure in the insulator can be used to improve the current uniformity of the memory. This non-uniformity has been a critical issue for the CBRAM. This talk was attended by more than 80 students and professors/researchers.

Two forthcoming events, IEEE and EDS technical co-sponsored confer-

ences, will be in the first-half year in 2015 in the Hsinchu Science Park. The first event, the International Symposium on VLSI Technology, Systems, and Applications (VLSI-TSA), will be held, April 27-29, 2015, at the Ambassador Hotel, Hsinchu, with a two-and-half days paper presentations and half-day short courses. The submission deadline is past, however, for registration details please visit the conference website at: <http://vlsi-tsa.itsa.itri.org.tw/2015/General/>.

The second event, IPFA 2015, will be held June 29 to July 2, 2015, at Lakeshore Hotel, Hsinchu, Taiwan. This is the second time this event will be held in Taiwan, with its first move out of Singapore in 2004. The event consists of a one day tutorial and 3 days of technical paper presentations, in which measurement/testing equipments exhibition will be demonstrated concurrently. For more details, please visit the conference website: <http://ieee-ipfa.org>.

~Mansun Chan, Editor



Speakers and some of the attendees at Arakan 2014

ED Japan

–by Kuniyuki Kakushima

The Arakan 2014 Meeting was held at Shimane University in Matsue on November 7th, on the purpose of re-study of highly sophisticated Si material, process and devices. More than 30 attendees enjoyed discussions on the following topics given by the lecturers:

- Prof. T. Mizuno – strain technology of CMOS devices
- Prof. K. Yamabe – thin and strong gate insulators
- Prof. T. Tsuchiya – MOS interface study by charge-pumping method
- Prof. M. Niwa – Si (100) surface and SiO_2/Si interface
- Prof. A. Toriumi – difference between SiO_2 and GeO_2
- Prof. M. Tabe – single dopant study for Si devices
- Dr. T. Mogami – p+-gate PMOS and salicide technique in CMOS devices
- Prof. A. Yokoyama – bio-sensors with silicon photonics
- Prof. Y. Suda – sputter epitaxy study and its device application
- Prof. K. Kikkawa – multilayer interconnect and wireless connection
- Prof. N. Matsuo – amorphous SiGe films
- Prof. Zaima – GeSn semiconductor physics

ED Kansai

–by Michinori Nishihara

The ED Kansai Chapter hosted the 14th annual Kansai Colloquium



The winners of the 14th MSFK Award and “The Chapter of the Year” at the 14th Kansai Colloquium Electron Devices Workshop: Dr. Yukihiro Kaneko, Prof. Yukiharu Uraoka (ED Kansai Chair), Dr. Takayuki Uchida (left to right)



The 14th Annual Kansai Colloquium Electron Devices Workshop Participants

Electron Devices Workshop on December 17, 2014, at OIT UMEKITA Knowledge Center, Osaka, Japan. The event attracted 35 participants and 11 excellent papers, with authors from the Kansai area, who also presented at the workshop. The papers were specially selected from (1)

major conferences such as IEDM or SSDM and (2) technical papers on electron devices published during the past 12 months.

The program was divided into three sections as follows: (1) Power and Compound Semiconductor Devices, (2) Sensor, Solar Cell, and

Emerging Devices, (3) CMOS Processing, Device, and Circuit.

The Award Committee selected two papers from student presenters for the 14th IEEE EDS Kansai Chapter MSFK Award. The winner was Dr. Takayuki Uchida of Kyoto University for his paper titled, *"Fabrication of Aluminum Oxide Thin Films by Solution-Source Non-Vacuum Process of Mist Chemical Vapor Deposition with Ozone Assistance."*

The Committee also selected one paper for the IEEE EDS Kansai Chapter of the Year Award. The winning paper was *"Neural Network based on a Three-Terminal Ferroelectric Memristor,"* by Dr. Yukihiro Kaneko of Panasonic Corporation.

The presented papers were all excellent and stimulated many questions and discussions with the audience, as they were selected from already qualified papers of major conferences and technical journals. This workshop is playing an important role in encouraging students and young engineers in the industry to extend their technical knowledge and career. The ED Kansai Chapter will continue to serve our members' interest.

We will have an annual international meeting called IMFEDK on June 3–5, 2015, in Kyoto, Japan. Please visit www.imfedk.org for more details.

~Kuniyuki Kakushima, Editor

IPFA 2015 – Reliability/CPMT/ED Singapore

~by Gan Chee Lip

The 22nd International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA 2015) is organized by the IEEE EDS Taipei Chapter and the IEEE Reliability/CPMT/ED Singapore Chapter. The Symposium is technically co-sponsored by the IEEE Electron Devices Society and IEEE Reliability Society.

IPFA 2015 is devoted to the fundamental understanding of the physical mechanisms of semiconductor

device failures and issues related to semiconductor device reliability, yield and performance, especially those related to advanced process technologies. The symposium will be held in Hsinchu Science Park, Hsinchu, Taiwan, for the second time in the IPFA series. The venue is next to the Science Park with only 10 minutes driving distance, and the park is well-known as "Taiwan's Silicon Valley".

Attendees may enjoy a visit to the cultural downtown of Hsinchu that was developed more than 200 years ago. Be sure to plan a visit to the well-developed science park where major IC manufacturing/design companies are located. IPFA 2015 will consist of a one day tutorial, 3 days of technical presentations with two Keynote Addresses and many Invited Talks given by renowned speakers. The one day tutorial will be part of the technical program of IPFA 2015. Vendor exhibits presenting state-of-art laboratory equipment and technologies are held in parallel with the technical sessions. On behalf of the IPFA 2015 committee, we are sincerely looking forward to your attendance.

COMMAD2014 – ED Western Australia

~by Adam Osseiran

The 12th Conference on Optoelectronic and Microelectronic Materials and Devices (COMMAD 2014) was held at The University of Western Australia, Perth, from December 14–17, 2014. The conference was chaired by Professor Lorenzo Faraone (FIEEE) and Professor Mariusz Martyniuk (SMIEEE) from the Microelectronic Research Group (MRG) of UWA with the support of the IEEE Western Australia Section—EDS-SSCS-IPS Chapter, the Australian National Fabrication Facility (ANFF), the Australian Nanotechnology Network and Perth Convention Bureau.

COMMAD2014 provided a forum to present and discuss recent progress in advanced materials growth

and synthesis, processing and characterisation, as well as device physics, design, nanofabrication, testing and applications. It also covered optoelectronic and microelectronic materials including inorganic and organic semiconductors and technologies such as Si, SiGe, SiC, ZnO, GaAs, InP, GaN, ZnSe, HgCdTe, LiNbO₃, dendrimers, polymers and porphyrins, etc, as well as nanophotonic and nanoelectronic structures and devices, such as lasers, modulators, photonic crystals, photodetectors, nanowires, optical switches, photovoltaics, waveguides, quantum dots, HBTs, HEMTs, MISFETs, flat panel displays, plastic electronics, electronic sensors, solar cells and fuel cells.

The attendees were mainly from Australia but also from Canada, China, Croatia, France, Germany, India, Japan, New Zealand, Poland and the USA. There were 10 keynote invited papers and 91 regular contributions (51 in oral sessions and 40 posters) presented.

ED Malaysia Kuala Lumpur

~by Mohd Nizar Hamidon and PS Menon

The IEEE ED Malaysia Chapter organized two Distinguished Lectures (DLs) by Dr. Vijay K. Arora from Wilkes University, USA, on December 23–24, 2014, at two different locations in Malaysia. On December 23rd, Prof. Arora delivered his DL on *"Carbon: The Soul of Nanoelectronics"* at the Institute of Microengineering and Nanoelectronics (IMEN), UKM. On December 24th, Prof. Arora gave another DL entitled *"Nanoelectronics: Quantum Engineering of Low-Dimensional Nanoensembles"* at ITMA, UPM. Membership booths were setup during both of these events.

A professional short course on Integration of TRIZ and Taguchi Optimization for R&D was co-organized by the IEEE ED Malaysia Chapter and the Institute of Microengineering and Nanoelectronics (IMEN),



Attendees of Prof Vijay Arora's DL at IMEN, UKM



Participants of Short Course on TRIZ and Taguchi method at IMEN, UKM

Universiti Kebangsaan Malaysia (UKM) from September, 9–10, 2014, at UKM. A total of 20 participants from academia attended the short course which was delivered by Dr. Prakash R. Apte from the College of Engineering Pune (COEP), India. The

course objective is to use TRIZ Innovation methodology to first identify the "RIGHT" problem and then to find several "innovative" solutions. Taguchi Method is then applied to one of the solutions by planning, conducting and analyzing a set of

experiments so as to obtain the best parameter settings and results.

~Susthitha Menon, Editor

ED Calcutta

–by Swapnadip De and Soumya Pandit

The IEEE Electron Devices Society Calcutta Chapter jointly with IEEE Electron Devices Society Calcutta University Student Branch Chapter and EDS Heritage Institute of Technology SBC organized a Mini Colloquium (MQ) on December 3–4, 2014, at KIIT Bhubaneswar.

The Distinguished Lecturers who delivered talks at the MQ were Dr. Samar Saha, IEEE EDS President-Elect, Dr. Ravi Todi, IEEE EDS Treasurer and IEEE Fellow, Prof. Chandan Kumar Sarkar, Jadavpur University and Prof. Gananath Dash, Sambalpur University. Dr. Ravi Todi in his talk highlighted on the challenges faced by Semiconductor Industries and their solutions. Prof. Dash spoke on the recent development of Graphene and its applications on Transistor design for digital and analog applications. Prof. C. K. Sarkar delivered his lecture on Advanced MOS transistors; Dr. Samar K. Saha spoke on MOSTransistor for Low Power Applications. The Mini Colloquium also consisted of a series of Invited Talks



Organizing Committee MQ with IEEE EDS DLs

other than poster presentations from students and research scholars. Professor Mohankumar, SKP Engineering College and Dr. Soumya Pandit, Chair of the IEEE ED Kolkata Chapter delivered their talks on HEMT devices and modeling and Mobile SoC Design respectively. Professor S. K. Mondal, KIIT University spoke on Inductor Design for RFIC applications. The MQ was also attended by over 100 research students from KIIT and other parts of India.

ED University of Calcutta Student Branch Chapter

—by Sarmista Sengupta and Soumya Pandit

The ED University of Calcutta Student Branch Chapter jointly with the ED Calcutta Chapter organized



Soumya Pandit delivering his talk

a one day seminar on Advanced Semiconductor Device Modeling and Fabrication on November 15, 2014. The program was hosted by Abacus Institute of Engineering and Management, JV Techno India and JIS group. The program consists of two invited talks delivered by Dr. Soumya Pandit, Institute of Radio Physics and Electronics and Dr. J.P. Bandyopadhyay, Emeritus Professor, University of Calcutta. Dr. Pandit delivered his talk on Device Characterization of MOS Transistor for VLSI Circuit simulation. He emphasized on the short channel effects and the use of TCAD modeling and simulation. Dr. Bandyopadhyay spoke on the various fabrication and growth techniques of semiconductor devices and integrated circuits. The seminar program was attended by over 65 students from AIEM and several faculties from the same institute.

ED NIST

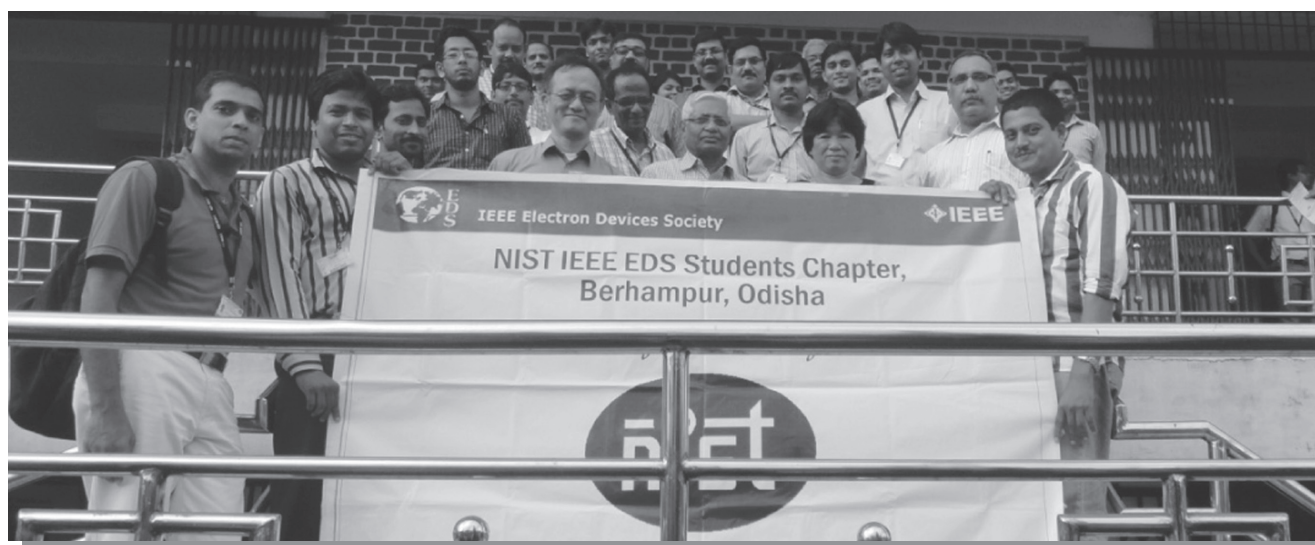
—by Ajit Kumar Panda

On October 17, 2014, the IEEE EDS NIST Chapter organized technical talks by Prof. Kuei H. Chen, Deputy Director of IAMS (Institute of Atomic and Molecular Sciences) Academia Sinica, Taiwan and Prof. Li. C. Chen, Director, CCMS (Centre for Con-



Prof. Kuei H. Chen (left) receiving a memento

densed Matter Sciences), National Taiwan University in the TIFAC seminar Hall on the theme, "Nano Materials for future Energy and Sensing applications." A group meeting was also held where faculty members of the Nano group discussed research of mutual interest. The chapter organized a one day seminar on "Body Area Networks: A Prospective" on November 5, 2014, at NIST, Berhampur. Professor Rutuparna Panda discussed basic concepts and principles of signal processing and communication networks which was attended by nearly 30 participants.



Participants of the ED NIST Chapter event



Prof. Krishna Saraswat (Stanford, California, USA) at ICEE



Dr. Chandrima Shaha delivering her talk

ED/SSC Bangalore

—by Janakiraman

The chapter organized two technical talks, the first on smart solar micro grids which was delivered by Ganesh Shankar, the CEO of a start up in Bangalore and the other by Professor Sanjay Raman on RFICs. The chapter technically sponsored the International Conference on Emerging Electronics (ICEE) held at IISc, Bangalore, December 3–6, 2014. The chapter also arranged for the XI South Asia Chapter Chairs Meeting during the conference.

ED Delhi

—by Mridula Gupta and Manoj Saxena

A one day seminar on “Women in Science: A career in Science”, was organized jointly by Silizium-Electronics Society, Department of Electronics, Deen Dayal Upadhyaya

College, University of Delhi, the IEEE EDS Delhi Chapter and Science Education Panel, Indian Academy of Sciences, Bangalore on October 17, 2014. The seminar was attended by 140 students who enjoyed the following invited speakers:

- Dr. Chandrima Shaha, Director, National Institute of Immunology, New Delhi, delivered an invited talk on “*Scientific career: the pleasure of solving mysteries.*”
- Professor Kasturi Datta, JNU, enlightened the audience through her talk on “*Evidence for Hyaluronan Bonding Protein 1 (HABP1) as a Tumor Biomarker.*”
- Professor Paramjit Khurana, University of Delhi South Campus, gave her talk on “*Engineering Plants for the Changing Climatic Scenario.*”
- Dr. (Mrs.) Niloufer Shroff, Scientist G, Electronics Niketan, DEITY, MCIT, Govt. of India, spoke on “*Photonics Research in India - A Personal View.*”

A Panel Discussion on Encouraging women in science was also organized with Professor Mridula Gupta, Chairperson for the IEEE EDS Delhi Chapter, Professor Riddhi Shah, School of Physical Sciences, JNU, Professor Geetha Venkataraman, School of Liberal Studies, Ambedkar University Delhi and Professor Mini Shaji Thomas, Faculty of Engg. & Tech. Jamia Millia Islamia, New Delhi, as the panelists.

On November 14, 2014, a technical Lecture on “*Atomic Clocks – How do they Work and Why do we need them?*” was delivered by Dr. Amitava Sen Gupta, Scientist H, National Physical Laboratory, New Delhi at University of Delhi South Campus. He discussed the basics of the working of present day atomic clocks - the Cesium fountain. He also described the further accuracy enhancements in the form of optical clocks based on single trapped ions.

~Manoj Saxena, Editor

EDS MEETINGS CALENDAR



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[HTTP://EDS.IEEE.ORG](http://eds.ieee.org). PLEASE VISIT.

2015 IEEE International Reliability Physics Symposium (IRPS)

19 Apr - 23 Apr 2015

Hyatt Regency Monterey Hotel & Spa
1 Old Golf Course Road
Monterey, CA, USA

2015 International Symposium on VLSI Design, Automation and Test (VLSI-DAT)

27 Apr - 29 Apr 2015

The Ambassador Hotel
188 Chung Hwa Road, Section 2
Hsinchu, Taiwan

2015 IEEE International Vacuum Electronics Conference (IVEC)

27 Apr - 29 Apr 2015

Beijing International Convention Center
No.8 Beichendong Rd., Chaoyang Dist.
100101, Beijing, China
Beijing, China

2015 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA)

27 Apr - 29 Apr 2015

The Ambassador Hotel
188 Chung Hwa Road, Section 2
Hsinchu, Taiwan

2015 26th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC)

03 May - 06 May 2015

Hilton
534 Broadway
Saratoga Springs, NY, USA

2015 IEEE 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD)

10 May - 14 May 2015

Kowloon Shangri-La, Hong Kong
64 Mody Road
Tsim Sha Tsui East
Kowloon
Hong Kong

2015 IEEE International Memory Workshop (IMW)

17 May - 20 May 2015

Hyatt Regency Hotel
1 Old Golf Course Road
Monterey, CA, USA

2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)

17 May - 19 May 2015

Phoenix Convention Center
100 N 3rd St.
AZ, USA

2015 IEEE International Interconnect Technology Conference and 2015 IEEE Materials for Advanced Metallization Conference (IITC/MAM)

18 May - 21 May 2015

Minattec Campus
3 Parvis Louis Neel
Grenoble, France

2015 International Siberian Conference on Control and Communications (SIBCON)

21 May - 23 May 2015

Omsk State Technical University
Mira Ave., 11
Omsk, Russia

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| 2015 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC) | 01 Jun - 04 Jun 2015 | Nanyang Executive Center (NEC) 50 Nanyang Avenue Singapore, Singapore |
| 2015 IEEE 42nd Photovoltaic Specialists Conference (PVSC) | 14 Jun - 19 Jun 2015 | Hyatt Regency New Orleans 601 Loyola Avenue New Orleans, LA, USA |
| 2015 Silicon Nanoelectronics Workshop (SNW) | 14 Jun - 15 Jun 2015 | Rega Royal Hotel Kyoto Kyoto, Japan |
| 2015 Symposium on VLSI Technology | 15 Jun - 18 Jun 2015 | Rhiga Royal Hotel Kyoto, Japan |
| TRANSDUCERS 2015 - 2015 18th International Solid-State Sensors, Actuators and Microsystems Conference | 21 Jun - 25 Jun 2015 | Dena'ina Convention Center 600 West 7th Avenue Anchorage, AK, USA |
| 2015 22nd International Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD) | 01 Jul - 03 Jul 2015 | Ryukoku University Avanti Kyoto Hall 31 Nishi Sanno-cho Higashi Kujo Minami-Ku Kyoto, Japan |
| 2015 28th International Vacuum Nanoelectronics Conference (IVNC) | 13 Jul - 17 Jul 2015 | Kaifeng Hotel Sun Yat-sen University north gate, No.135, Xingang Xi Road, Haizhu District, Guangzhou, China |
| 2015 International Workshop on Computational Electronics (IWCE) Abstract submission deadline: 08 Apr 2015 Final submission deadline: 30 Sep 2015 Notification of acceptance date: 27 May 2015 | 02 Sep - 04 Sep 2015 | Purdue University 610 Purdue Mall West Lafayette, IN, USA |
| 2015 International Conference on Solid State Devices and Materials (SSDM) | 27 Sep - 30 Sep 2015 | Sapporo, Japan |
| 2015 37th Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD) | 27 Sep - 02 Oct 2015 | Peppermill Resort Hotel 2707 South Virginia Street Reno, NV, USA |
| 2015 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S) | 05 Oct - 08 Oct 2015 | DoubleTree by Hilton Sonoma One DoubleTree Drive Rohnert Park, CA, USA |
| 2015 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS) Abstract submission deadline: 01 May 2015 Final submission deadline: 17 Jul 2015 Notification of acceptance date: 29 May 2015 | 11 Oct - 14 Oct 2015 | Sheraton New Orleans Hotel 500 Canal Street New Orleans, LA, USA |

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| 2015 IEEE International Integrated Reliability Workshop (IIRW) Abstract submission deadline: 12 Jul 2015 Final submission deadline: 11 Oct 2015 Notification of acceptance date: 14 Aug 2015 | 11 Oct – 15 Oct 2015 | Stanford Sierra Conference Center 130 Fallen Leaf Road South Lake Tahoe, CA, USA |
| 2015 International Semiconductor Conference (CAS) Full Paper Submission deadline: 01 Jun 2015 Final submission deadline: 01 Jun 2015 Notification of acceptance date: 16 Jul 2015 | 12 Oct - 14 Oct 2015 | Hotel Rina Sinaia Bd. Carol I, Nr 8, Sinaia, Romania |
| 2015 15th Non-Volatile Memory Technology Symposium (NVMTS) Abstract submission deadline: 07 Jun 2015 Final submission deadline: 13 Sep 2015 Notification of acceptance date: 12 Jul 2015 | 12 Oct - 14 Oct 2015 | Tsinghua University Haidian District Beijing, China |
| 2015 IEEE Bipolar/BiCMOS Circuits and Technology Meeting - BCTM Abstract submission deadline: 01 May 2015 Final submission deadline: 24 Jul 2015 Notification of acceptance date: 22 Jun 2015 | 26 Oct - 28 Oct 2015 | Hyatt Boston Harbor 101 Harborside Drive Boston, MA, USA |
| 2015 IEEE/ACM International Conference on Computer-Aided Design (ICCAD) | 02 Nov - 06 Nov 2015 | DoubleTree by Hilton Hotel Austin 6505 N. Interstate 35 Austin, TX, USA |
| 2015 IEEE 46th Semiconductor Interface Specialists Conference (SISC) | 02 Dec - 05 Dec 2015 | The Key Bridge Marriott 1401 Lee Highway Arlington, VA, USA |
| 2015 IEEE International Electron Devices Meeting (IEDM) Abstract submission deadline: 26 Jun 2015 Final submission deadline: 22 Sep 2015 Notification of acceptance date: 14 Aug 2015 | 07 Dec - 09 Dec 2015 | Hilton Washington Washington, DC, USA |
| 2016 IEEE International Reliability Physics Symposium (IRPS) | 17 Apr - 21 Apr 2016 | To be determined |
| 2016 IEEE International Vacuum Electronics Conference (IVEC) | 26 Apr - 28 Apr 2016 | Monterey Marriott 350 Calle Principal Monterey, CA, USA |
| 2016 IEEE 43rd Photovoltaic Specialists Conference (PVSC) | 05 Jun - 10 Jun 2016 | Oregon Convention Center 77 NE Martin Luther King Jr. Blvd. Portland, OR, USA |

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| 2016 28th International Symposium on Power Semiconductor Devices and IC's (ISPSD) | 12 Jun - 16 Jun 2016 | Zofin Palace Slovanský ostrov 226 Prague, Czech Republic |
| 2016 IEEE Symposium on VLSI Technology | 14 Jun - 16 Jun 2016 | Hilton Hawaiian Village 2005 Kalia Road Honolulu, HI, USA |
| 2016 IEEE International Electron Devices Meeting (IEDM) | 01 Dec - 09 Dec 2016 | Hilton San Francisco San Francisco, CA, USA |
| 2016 IEEE 47th Semiconductor Interface Specialists Conference (SISC) Abstract submission deadline: 14 Aug 2016 Notification of acceptance date: 18 Sep 2016 | 07 Dec - 10 Dec 2016 | Catamaran Resort Hotel 3999 Mission Blvd. San Diego, CA, USA |
| 2017 IEEE International Reliability Physics Symposium (IRPS) Abstract submission deadline: 30 Sep 2016 Final submission deadline: 01 Feb 2017 Notification of acceptance date: 21 Dec 2016 | 02 Apr - 06 Apr 2017 | Hyatt Regency Monterey One Old Golf Course Road Monterey, CA, USA |
| 2017 IEEE International Electron Devices Meeting (IEDM) Abstract submission deadline: 01 Jun 2017 Final submission deadline: 01 Sep 2017 Notification of acceptance date: 01 Aug 2017 | 04 Dec - 06 Dec 2017 | Hilton San Francisco Union Square San Francisco, CA, USA |
| 2018 IEEE Symposium on VLSI Technology | 12 Jun - 14 Jun 2018 | To be determined |
| 2018 IEEE International Electron Devices Meeting (IEDM) | 29 Nov - 07 Dec 2018 | Hilton San Francisco San Francisco, CA, USA |
| | 09 Dec - 11 Dec 2019 | Hilton San Francisco Union Square |
| 2019 IEEE International Electron Devices Meeting (IEDM) Abstract submission deadline: 01 Jun 2019 Final submission deadline: 01 Sep 2019 Notification of acceptance date: 01 Aug 2019 | | San Francisco, CA, USA |
| 2020 IEEE Symposium on VLSI Technology | 16 Jun - 18 Jun 2020 | To be determined |
| 2020 IEEE International Electron Devices Meeting (IEDM) | 10 Dec - 18 Dec 2020 | Hilton San Francisco San Francisco, CA, USA |
| 2021 IEEE International Electron Devices Meeting (IEDM) Abstract submission deadline: 01 Jun 2021 Final submission deadline: 01 Sep 2021 Notification of acceptance date: 01 Aug 2021 | 13 Dec - 15 Dec 2021 | Hilton San Francisco Union Square San Francisco, CA, USA |

THE 61ST ANNUAL IEEE INTERNATIONAL ELECTRON DEVICES MEETING (IEDM)

DECEMBER 7-9, 2015
HILTON WASHINGTON HOTEL



The world's best scientists and engineers in the field of microelectronics from industry, academia and government will gather at the IEDM to enjoy a technical program of more than 220 presentations, along with panels, special sessions, Short Courses, IEEE/EDS award presentations and other events spotlighting more leading work in more areas of the field than any other conference.

Papers in the following areas are encouraged:

- Circuit and Device Interaction
- Characterization, Reliability and Yield
- Display and Imaging Systems
- Memory Technology
- Modeling and Simulation
- Nano Device Technology
- Power and Compound Semiconductor Devices
- Process and Manufacturing Technology
- Sensors, MEMS and BioMEMS

Paper submission deadline: Monday, June 22nd

For more information, visit the IEDM website: www.ieee-iedm.org.