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IEEE

Technical Briefs

Too Hot to Handle:

Self-heating as an Emerging Performance and Reliability Concern in Modern Surround Gate Transistors

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Abstract
By early 2000s, many researchers would begin their talks with an iconic cartoon that superimposed the increasing power dissipation of an IC and that of a rocket nozzle and the Sun. The message was difficult to ignore: the voltage must be scaled to keep power-dissipation at bay. Fast forward to 2015 – the tyranny of short channel effects at the sub 32 nm nodes has led to the development of FINFET and ETSOI technologies, with gate-all-around III-V transistors on the horizon. The short channel effects are controlled, but at the expense of additional self-heating of the system. Stacks of materials (many poor thermal conductors) now surround the very hot channel to make the bad situation worse. In this article, I explain how self-heating redefines and conflates the traditional notions of performance and reliability of ultrathin transistors and frontend and backend issues of modern ICs.

1. A Short History of Self-heating: Three Revolutions, Catalyzed by Self-heating

It would be unwise to put on parka in a hot summer day: since $T - T_{air} = P \times R_{th}$, even for the same body heat (P), the thermal resistance (R_{th}) of the parka would make self-heating (R_{th}) unbearable. Lately, in desperate pursuit of transistor scaling, we may be surrounding the transistors with similarly poor R_{th} (see Fig. 1): left unchecked, the self-heating will hurt performance and reliability of the transistors.

Self-heating (SH) spelled the end of first two waves of the electronics revolution (vacuum tubes and bipolar transistors), and one day would do the same for MOSFET, forewarned the experts in 1990s. Unless the exponential rise in P is stemmed, the power of

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Issue	Due Date
January	October 1st
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October	July 1st

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Too Hot to Handle

(continued from page 1)

rocket nozzles (1 kW/cm^2) will pale in comparison to hotspots in a CPU (per unit area). The community listened; engineers learned to work with lower voltages, tailor voltages and throttle clockspeed on the fly, redesigned critical paths, turned off inactive regions (dark silicon), and learned to spread the work around in multi cores. The result would impress even a casual observer: following a 100-fold increase since 1985, *P/Area* has plateaued to ~100 W/cm^2 since 2005!

We could celebrate, except that the celebration would be premature!

As transistors scaled, the principles of Dennard scaling was supposed to keep the short channel effect (SCE) at bay. Unfortunately, by the early 2000s, it became clear that planar transistors would not do, the industry would have to adopt variants of surround gate technologies to scale to the ultimate limit. Thanks to ingenious processing (e.g., multiple patterning [1], ALD deposited oxides and gate-metal (WN) [2]), surround gate transistors emerged in quick succession (e.g., FinFET, omega-FET, DG-SOI, ET-SOI, Nanowire-FET, and so on, see Fig. 1). Little did we know that the poor thermal conductivity of the oxides and the ubiquity of interfaces, would increase R_{th}, and eventually lead to a Faustian bargain – increased SCE vs. increased SH, your choice!

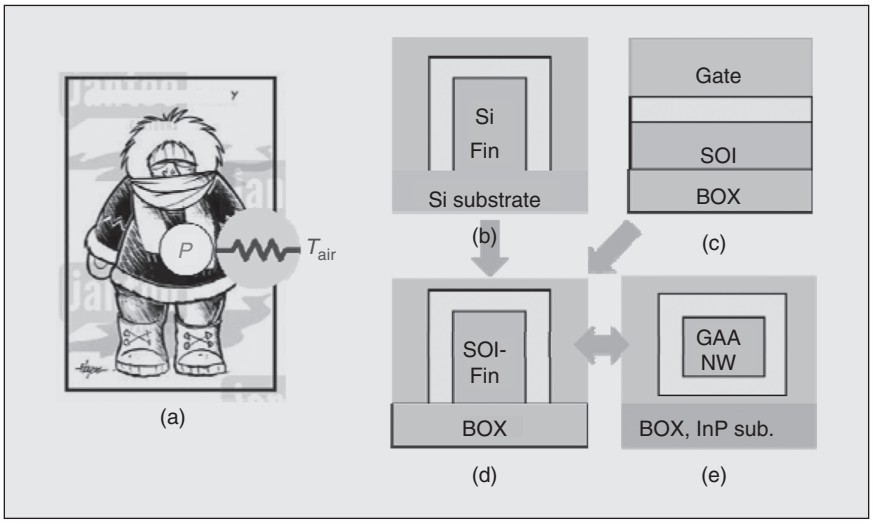

Fig. 1: (a) Putting a parka on the transistor is not a good idea. The transistor geometries, (b) FINFET, (c) SOI-FET, (d) SOI-FinFET, and (e) GAA NW-FET, have increasingly larger R_{th}. Even if P is reduced, the performance and reliability could be a concern.

2. Electrical and Optical Measurements Quantify Self-heating

The simulation results in Fig. 2a show three aspects of SH in a SOI-FinFET [3, 4]: 1) significant temperature rise, 2) nonuniform temperature distribution among the NWs, and 3) R_{th} defined the complex material stack surrounding the transistor. In practice, the channel is hidden from direct view, therefore a set of indirect measurements must be stitched together to quantify these three aspects of SH.

The electrical characterization of SH may involve (i) monitoring the gate [4] or substrate currents [5], or (ii) inserting local probes (a poly-resistor in the gate, or a test transistor nearby) [6,7], or (iii) measuring the frequency-dependent AC conductance of the self-heated channel [3]. These techniques provide only the Fin-averaged temperature; the calibrations are also tricky, and the measures are often qualitative. The optical/IR measurements offer direct (but somewhat diffused) observation of self-heating; in particular, the newly introduced thermo-reflectance measurement resolves the Fin-specific *surface* heating (see Fig. 2b), albeit convolved over the emission from neighboring images [3] The electrical and optical measurement interpreted by self-consistent numerical modeling provides a wealth of information for surround gate technologies [8,9], as follows.

3. Self-heating vs. transistor geometry

By 2010, when researchers began to quantify SH using a combination of electrical and optical methods, everyone was surprised by its magnitude, the peak location, the time constants, and correlations. Intel [7], TSMC [6], and Samsung [5] focused on FINFETs with a combination of computational modeling, embedded thermal monitors, and statistical analysis of on-current and threshold voltage. The signature of self-heating on drain-current was obvious (4–5 times higher than comparable bulk MOSFETs [5], but the reduced *P* due to AC cycling, and the reduced R_{th} due to direct connection to the substrate keep self-heating below 30C. The Backend EM reliability of the local interconnects is affected [6], but rerouting helps.

Unfortunately, these optimistic results do not extend to more advanced designs, namely, III-V Gate-All-Around devices or SOI-FinFET, as shown in Fig. 1 [3, 4]. Here, AC conductance and TR imaging offer nontrivial insights: SH increases I_{on} in a contact-resistance limited device [3, Shin], but deceases I_{on} in devices limited by channel transport. Without an easy escape to the substrate, T_{max} increase to ~ 50 – 80 *C* due to

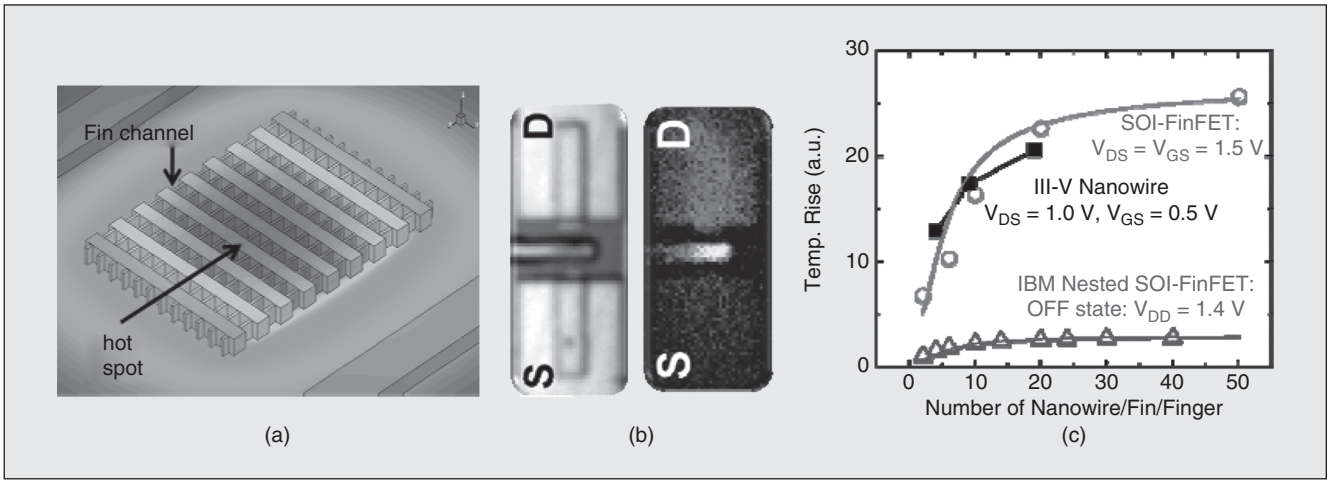

Fig. 2 Self-heating depends on transistor configuration and FIN-number: (a) Numerical simulation of SOI-FinFET demonstrates significant self-heating in transistors (Courtesy: S. Koswatta, IBM) (b) TR-imaging of a 19-NW III-V GAA transistor directly measures SH and locates it within the channel, (c) For various surround gate topologies, temperature rises almost linearly until N ~ 10.

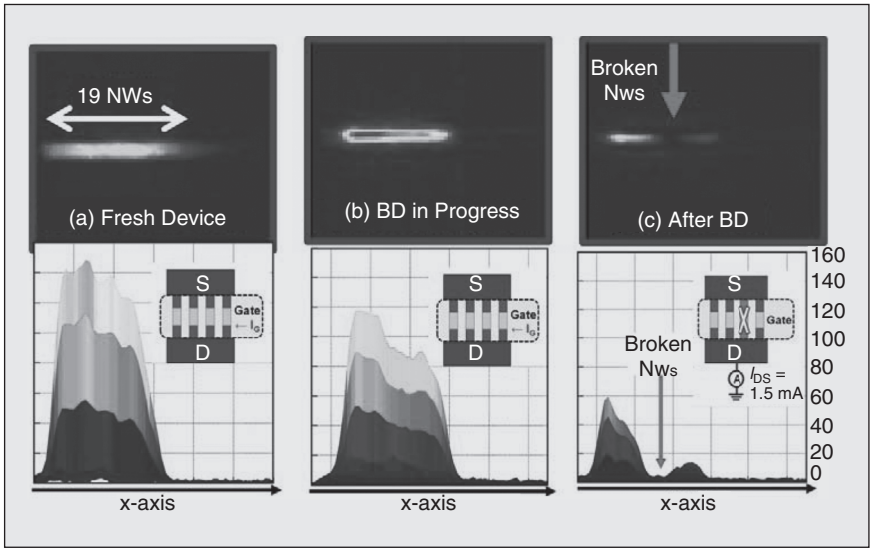

Fig. 3 Dielectric breakdown in GAA-FET requires generalization of classical TDDB concepts. (a) Initially, the middle channel is the most heated, as expected, see Fig. 2. (b) The dramatic increase in heating signals incipient failure. (c) A broken FIN does not break the transistor, but partitions the total current in fewer FINs: the increased current accelerates subsequent failure.

thermal cross talk (see Fig. 2c, and Ref. 4,7,9), and the time-constants span multiple time-scales (ns to μs to ms), as the heat first equilibrates within the channel, then diffuse to the contacts, and eventually escape through the substrate. The memory of SH from the cycles past may shift the threshold voltage and introduce an additional run-time spatio-temporal variability, analogous to the floating body effect for SOI transistors. In this context, a SH friendly via-design, pre-silicon optimization, and post-Silicon validation [5] can help.

Interestingly (and counterintuitively), the thermal images reported by Shin et al. from Purdue [3] locates the peak of temperature within the channel, see Fig. 2b. Based on classical modeling, many believed that the shorter channel transistors would also be cooler (and more reliable), because the quasi-ballistic electrons would dissipate their energy in the drain, kept at T_D = 300 C. In practice, oxides surround source-drain extensions and the significant thermal resistance to the ground increases T_D >> 300 C: this pair of effects pushes the hot spot back into the channel. The increasing SH within the channel, even within a short channel transistors, must be addressed in transistor redesign.

4. Self-heating degrades reliability, the degradation is predictable

Self-heating reduces device lifetime, but more importantly, complicates lifetime projection. Consider, for example, the physics of gate dielectric breakdown (TDDB). Since 1992, three parameters – voltage acceleration, activation energy, and Weibull area/percentile scaling have been sufficient to predict dielectric lifetime [10]. The voltage and temperature differed among various parts of an IC, but was generally uniform over a single transistor.

No longer.

In a 19-Fin device (see Fig. 3a), the central Fin is hotter and therefore degrades faster than its neighbors (Fig. 3b). Once the central FIN fails, the isolation of the neighbors reduces R_{th}, but the redistribution

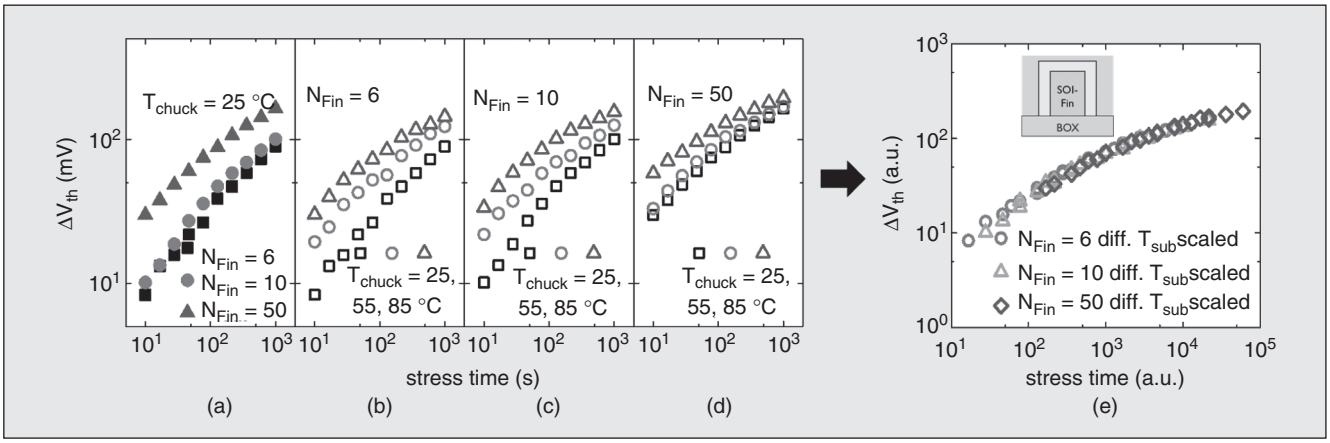

Fig. 4: HCI degradation of SOI-FinFET technologies. (a-d) SH increases with Fin number, and so does the HCI degradation. (e) And yet, the degradation can be scaled to an universal curve, suggesting an opportunity to determine the voltage and temperature acceleration factors for arbitrary number of Fins.

of I_{on} of the failed FIN among the existing NWs would increase P, with unpredictable effect on Fin-specific temperature, and subsequent breakdown. The fundamental physics of TDDB (defect generation terminated by percolation) does not change, but self-heated transistors would need a new formulation and qualification methodology for lifetime prediction.

Often, the reformulation need not be complicated. For example, HCI for FinFET is still correlated to I_{sub}, as a theormometer of the channel electrons T_c, [5], and can be used to predict/optimize HCI performance. For gate-all-around devices, T_c is unavailable, but an equally compelling alternative exists, as follows. We know that HCI of planar transistors depend on V_D, and the time evolution threshold voltage, can be scaled to a universal curve, which in turn allows lifetime prediction based on the a few short-duration stresses [12,13,14]. The scaling concept relies on the idea that V_D determines SH, which in turn dictates the rate of bond dissociation. Although the origin of SH in surround gate transistors is more complex, the basic physics is the same; it is hardly surprising that the scaling principle holds, see Fig. 4.

5. Self-heating correlates performance and reliability

Consider an ET-SOI technology with three different body thicknesses. The thinnest channel offers the best SCE, but its extreme SH reduces I_{on} and degrades HCI lifetime. The opposite is true for the thickest transistor. Therefore, SCE and HCI reliability would be optimized at an intermediate thickness [13]. Similar consideration apply to FinFETs; tightly spaced FINs may reduce I_{on} (and P) per Fin, yet the SH may degrade the overall I_{on} and reliability. A somewhat relaxed spacing (fewer fins/per width) may end up improving both performance and reliability of the technology.

Second, SH couples variability and reliability in interesting ways. Among the NWs of a transistor, the one with lowest V_{th} has higher overdrive ($V_D - V_{th}$), more self-heating, and faster degradation. This in turn reduces process variability by bringing the threshold voltages together [3].

Finally, all transistor topologies show that the AC-SH is always lower than the DC-SH such that the AC-lifetime increases with frequency. This is because, although the average temperature is frequency independent, the maximum temperature (which dictates reliability) is not. The reduction in T_{max} improves reliability [14].

6. Looking ahead: Newer switches, architectures, and brain to the rescue

In the long run, SH should encourage a fundamental rethinking of P and R_{th}. Device physicists hope to reduce P either by changing the channel material (Si vs. Ge vs. III-V) *or* by introducing transistors with steeper subthreshold slope (e.g., NC-FET, tunnel-FET), which operate at lower V_D. The much maligned MOSFET rescued bipolar IC; can the NC-FET or tunnel-FET, similarly rescue MOSFETs, to launch the fourth wave of microelectronics? Similarly, circuit and system designers hope that non-boolean computing paradigms (neuromorphic computing, approximate computing, etc.) will save the day, at least for specialized applications.

In addition to device/system redesign, others propose to focus on reducing R_{th}: instead of cooling by macroscopic fins and fans, it is better to cool at the source by microscopic techniques involving liquid- or two-phase evaporative cooling [15]. In this regard, the brain provides a paradigm and inspiration. The blood vessels (the interconnect of the brain) deliver power and remove waste heat so effectively that brain maintains its temperature within a fraction of a degree [15,17]. The essence of this exquisite control is the 3D intermeshing

of computing and heat removal, so as to obviate the one-dimensional heat diffusion limit [18]. An electro-thermal co-design inspired by the topology and computing paradigm of the brain may eventually be the most effective approach to control of SH in future generation IC's appropriate for the mobile world.

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About the author: *Professor Alam teaches at Purdue University, where his research focuses on classical and novel semiconductor devices. After a decade at Bell Laboratories (Murray Hill, NJ) where he made fundamental contributions to IC reliability and optoelectronic ICs, he returned to Purdue University in 2004, where he is now the Jai N. Gupta professor of Electrical Engineering. Today, he works a broad range of topics of emerging electronics, including biosensors, solar cells, and flexible electronics. He has published over 200 papers and discussed his results at many International conferences. He is a fellow of IEEE, APS, and AAAS. His awards include 2006 IEEE Kiyo Tomiyasu Medal for contributions to device technology for communication systems and the 2015 SRC Technical Award for fundamental contributions to reliability physics. Prof. Alam enjoys teaching – more than 100,000 students have learned some aspect of semiconductor physics from his web-enabled courses.*

Upcoming Technical Meetings

Things are Heating up at the 2016 IEEE International Reliability Physics Symposium (IRPS)

April 17–21, 2016

Pasadena Convention Center

Pasadena, CA, USA

The International Reliability Physics Symposium (IRPS) is the world's premier forum for leading-edge research addressing developments in the Reliability Physics of devices, materials, circuits, and products. IRPS is the conference where **emerging Reliability Physics challenges** and possible solutions to achieve realistic End-of-Life projections are first discussed.

For 54 years, IRPS has been the premiere conference for engineers and scientists to present new and original work in the area of microelectronics reliability. Drawing participants from the United States, Europe, Asia, and other parts of the world, IRPS seeks to promote the reliability of semiconductor devices, integrated circuits, and microelectronic assemblies through an improved understanding of both the physics of failure as well as the application environment. No other meeting presents as much leading work in so many different areas of reliability of electronic devices, encompassing both silicon and non-silicon devices, process technology, packaging, circuits and systems reliability, optoelectronics, photovoltaics, and MEMS. IRPS 2016 will offer evening panel debates and workshops, invited plenary talks, and an **outstanding technical program.**

Interconnect and transistor wearout are accelerated by an elevated temperature, and **self-heating** is exacerbated in the most advanced CMOS technologies. IRPS 2016 will feature two invited talks on this critically important topic. Prof. Jonathan Malen of Carnegie Mellon University will give an invited talk on Nanoscale Heat Transport in Advanced Semiconductor Devices, and Dr. Baozhen Li of IBM will give an invited talk on Thermal Engineering Challenges for Interconnects in Advanced Processes.

Pasadena's city hall and downtown overview

Unsurprisingly, among the regular submissions to the conference, there included several works that focus on self-heating effects. Two groups of researchers — one from Samsung and the other from Purdue University — will present papers that describe the temperature-accelerated HCI effects in FinFET devices. A group of researchers from Xilinx will present a paper that details a comprehensive circuit reliability simulation tool that includes thermal coupling effects and minimizes overall product risk due to transistor aging and electromigration.

ESD-induced failures often are thermally-precipitated. A researcher from Intel will present a paper describing a model for ESD-induced heating in interconnect structures.

Wide bandgap (WBG) semiconductors are preferred for high-power applications due to their ability to safely operate at elevated temperatures. At the 2016 IRPS, there will be an entire session devoted to the reliability of WBG semiconductor devices.

The technical program for the 2016 IRPS also includes invited talks on **Soft Error in Supercomputers, Product-level Reliability of GaN devices, and Reliability Trojans.**

The Convention Center is located in Pasadena's downtown which is best known as the host of the annual Tournament of Roses Parade and Rose Bowl football game. The City also boasts numerous cultural amenities, fine restaurants and top retailers. All this helps Pasadena live up to the true meaning of its name — the Crown of the Valley.

IRPS consists of three days (Tues-Thurs, April 19–21) of plenary and parallel technical sessions presenting original, state-of-the-art work.

Other opportunities at the symposium include:

- Two-Day **Tutorial Program** (Sunday-Monday April 17–18). The IRPS tutorial program is a comprehensive two-day event designed to help both the new engineer and experienced researcher. The tutorial program contains both beginner and expert tracks, and is broken down into parallel tracks dealing with Technology, Component and System reliability challenges, allowing the attendees to participate in tutorials relevant to their work with a minimum of conflicts between subject areas. Among the topics, we are emphasizing this year: **Self-heating effects** on FINFET transistors, interaction of component faults and system security, circuit aging effects, **Systems reliability** comprehending complex applications and self-healing designs, and Chip-Package interactions in 2.5D and 3D packaging.
- **Year in Review** Session (Monday April 18). These seminars provide a summary of the most significant developments in the reliability community over the past year. This serves as a convenient, single source of information for attendees to keep current with the recent reliability literature. Industry experts serve as the "tour guide" and save you time by collecting and summarizing this information to bring you up to date in a particular area as efficiently as possible.
- Evening **Poster Session**. The poster session will provide an additional opportunity for authors to present their original research. The setting is informal and allows for easy discussion between authors and other attendees.
- Evening Session **Workshops**. These workshops enhance the symposium by providing the attendees an opportunity to meet in informal groups to discuss key reliability physics topics with the guidance of experienced moderators. Some of the workshop topics are directly coupled to the technical program to provide a venue for more discussion on the topic.
- **Vendor Exhibits**. Held in parallel with the technical sessions, the equipment demonstrations provide a forum for manufacturers of state-of-the-art laboratory equipment to present their products. Attendees are encouraged to visit the manufacturers' booths for information and demonstrations.
- **IRPS Paper Awards**. IRPS bestows awards for Best Paper, Outstanding Paper, Best Poster and Best Student Talk. The Best Paper author is typically invited to present the paper at ESREF in October.

For registration and other information, visit the IRPS 2016 home page at http://www.irps.org/ .

The IRPS committee members look forward to seeing you in April.

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2016 IEEE Symposium on VLSI Technology

The 36th Annual Symposium on VLSI Technology will be held from **June 13–16, 2015**, at the Hilton Hawaiian Village, Honolulu, Hawaii. This symposium is jointly sponsored by the Japan Society of Applied Physics (JSAP) and the IEEE Electron Devices Society (EDS) in cooperation with the IEEE Solid-State Circuits Society.

VLSI Symposium is a premiere international conference on semiconductor technology defining the pace, the progress and evolution of the microelectronics industry. A unique advantage of this conference is that it is held jointly with the Symposium on VLSI Circuits (June 14–17) at the same location. A single registration covers both symposia. The overlap in the symposia schedules and location offers a platform for interactions between technologists, circuit designers & system architects.

The conference theme this year is **"Inflections for a Smart Society."** Symposium scope includes advances, new concepts and breakthroughs in VLSI technology including:

- **IoT Systems and Technologies** including heterogeneous integration; ultra low power technologies; sensors, display, connectivity; power management; digital/analog, micro-controllers & application processors.
- **Stand-Alone and Embedded Memories** technology and

reliability for DRAM, SRAM, Non-Volatile, Emerging Memories.

- **CMOS Technology, Micro-processors and SoCs** including scaling, VLSI manufacturing concepts, and yield optimization.
- **RF / Analog / Digital Technologies** for mixed-signal SoC; RF front end; analog, mixed-signal, I/O, high-voltage, imaging, MEMS, integrated sensors.
- **Process and Material Technologies** including advanced transistor process and architecture, modeling and reliability; alternate channel; advanced lithography, high-density patterning; SOI and III—V technologies; photonics; local interconnects and Cu/optical interconnects scaling.
- **Packaging Technologies and System-in-Package (SiP)** including through-silicon-vias (TSVs) and 3D-system integration.
- **Photonics Technology and Beyond CMOS Devices** The Symposium on VLSI Technology continues to focus strongly on design/technology co-optimization. In 2016, the conference will offer joint Technology and Circuits focus sessions comprising invited and contributed papers in the following areas:
- **Design in scaled technologies:** scaling of digital, memory, analog & mixed-signal circuits in advanced CMOS processes
- **Design enablement:** design for manufacturing, process-design co-optimization, on-die monitoring of variability and reliability
- **Embedded memory technology and design:** SRAM, DRAM, Flash, PCRAM, RRAM, MRAM, etc.
- **3D & heterogeneous integration:** power and thermal management, inter-chip communication, system in package (SiP) architectures and applications
- **Smart power**
- **Analog/RF integration & design / technology co-optimization in CMOS.**

In addition, two technology focus sessions will address:

- **System and Embedded memory**
- Local, Global and Chip-Chip Interconnects.

The joint evening panel discussion of June 14 will be on the **"More Moore, More than Moore or Mo(o)re Slowly".** A topic that underlines the soul searching taking place in our industry. While scaling continues, the IC industry faces an inflection that is building on heterogeneous integration of leading-edge and mature technologies driving "smart" system level applications. The technology panel on the same day asks the question on **"How Moore's Law, Industry Consolidation and System Trends will shape the Memory Roadmap.**" Both panels should capture the interest of technologists, designers, business managers and analysts alike.

Every year the Symposium offers professional development opportunities, with a one-day short course on June 13 on **"Inflections in VLSI Technology – Cloud and Beyond"** including:

- High performance computing
- Future interconnects – photonics
- Memory for cloud computing communication
- 3D SOC and 2D hetero-integration
- Power management and devices
- Ultra low power computing
- Non-volatile spin logic and memory
- Neurocomputing
- Sensors: MEMS and bio
- Energy consideration and storage

All topics are discussed by leading experts from academia and industry.

In addition, two satellite workshops will be held before the conference: the **"IEEE Silicon Nanoelectronics Workshop"** and the **"Spintronics Workshop"** on June 12–13, 2016.

After a successful experience in 2015, the Symposium on VLSI Technology will organize an executive panel on June 15 on "Semi Business beyond Scaling" with leading industry executives to discuss inflections in microelectronics business and future industry drivers that go beyond traditional scaling. The Symposia are recognized for their spirit of international collaboration and informal atmosphere, promoting discussion and debate on new ideas and technology directions.

For further information, complete conference, author, and registration information, please visit the Symposium website at http://www.vlsisymposium.org or contact the following conference secretariats:

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We cordially invite you to attend the 2016 Symposium on VLSI Technology to learn about recent state-of-the-art advancements in IC technology and to take advantage of enriching technical interactions.

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2016 IEEE Compound Semiconductor IC Symposium

October 23rd–26th, in Austin, Texas

Paper Submission Deadline: April 22 , 016

We cordially invite you to the 2016 IEEE Compound Semiconductor IC Symposium (CSICS) being held October 23rd–26th at the Doubletree by Hilton Hotel located in Austin, Texas, USA. Since its inception in 1978, the Symposium has become a pre-eminent international forum for developments in compound semiconductor circuit and device technology. The scope of the Symposium encompasses devices and circuits, embracing GaAs, SiGe, InP, GaN, InSb, and CMOS technology to provide a truly comprehensive conference. CSICS is the ideal forum for presenting the latest results in microwave/mm-wave, high-speed digital, analog, mixed mode, THz, power conversion, and optoelectronic and Silicon Photonics integrated circuits.

The 2016 CSIC Symposium is comprised of a full 3-day technical program, two short courses, a primer course, and a technology exhibition. The technical program includes approximately 60 high quality technical papers. Invited papers and panel sessions on topics of current importance to the Compound Semiconductor IC community greatly enrich the technical program. In addition, the Symposium will continue the tradition of including important "late breaking news" papers. The short courses on Sunday, October 23rd provide the attendees the opportunity to learn from world-renowned instructors in their respective areas of expertise. The Sunday introductory-level primer course will provide attendees insight into the design of principal RF and high speed IC building blocks, emphasizing the specific background needed to understand and appreciate the technical program.

The technology exhibition will be held on Monday and Tuesday, featuring informative and interesting displays with corporate representatives on hand. The list of exhibitors can be found in the CSICS advance program to be published in late June. To complement the Symposium, there are several social events including the Sunday Evening CSICS Opening Reception, the Monday CSICS Exhibition Opening Reception, and the Tuesday CSICS Exhibition Luncheon. Breakfasts and coffee breaks will be served on Monday, Tuesday, and Wednesday.

For registration and up-to-date information, please visit the CSICS website at www.csics.org. Further questions may be addressed to the Symposium Chair: Chip Moyer, HRL Laboratories, Phone: 1-310-487-3290, E-mail: hpmoyer@hrl.com.

We hope you can attend,

2016 IEEE CSICS Organizing Committee

Thé Linh Nguyen
2016 CSICS Publicity Chair
Finisar Corporation

2016 IEEE International Semiconductor Conference (CAS)

The 39th International Semiconductor Conference (CAS 2016) will be held in Sinaia (Romania), October 10–12, 2016. The conference is focused on developments in micro-and nanotechnologies. For the 2016 edition, papers are expected in the following domains:

- Nanoscience and Nanoengineering
- Micro- and Nanophotonics, and Optoelectronics
- Microwave and Millimeter Wave Circuits and Systems
- Microsensors and Microsystems
- Modelling
- Semiconductor Devices
- Integrated Circuits
- Physics of Materials

The CAS conference was originally launched in 1978. Until 1996 it was organized as the *Annual Semiconductor Conference* (in Romanian – Conferinta Anuala de Semiconductoare – CAS). Since 1991 it has become available to the international scientific community and has changed its name accordingly to *International Semiconductor Conference*, still keeping the acronym (CAS). In 1995, the conference became an IEEE event, sponsored by the IEEE Electron Devices Society. Since 1997, it has been organized by the National Institute for Research and Development in Microtechnologies (IMT Bucharest).

IMT Bucharest is supervised by the Romanian Ministry of Education and

Scientific Research. It is the first institute with this profile in Eastern Europe and the main actor in microtechnologies in Romania. IMT mission consists of research and development in micro-, nano-, biotechnologies, education and training, knowledge dissemination and technology transfer. Between 2003 and 2015, IMT was involved in approximately 45 European projects (FP6, FP7 and related).

The CAS Conference agenda includes plenary sessions with invited papers and regular sessions. The regular papers are selected for both oral and poster sessions. A Student Paper Session is also organized and the Best Student Paper Award is given every year by the IEEE ED Romania Section Chapter. The invited papers and accepted papers will be published in CAS 2016 Proceedings (an IEEE publication). All accepted and presented papers will appear in the *IEEE Xplore* data base.

The CAS2016 event is a milestone for the members of the IEEE ED Romania Chapter. Thanks to the efforts of the EDS team, our chapter attracted ten new members in 2016. The chapter growth is stimulated by the annual CAS forum, where our EDS members find a prolific scientific environment. For a call for papers and further information regarding the CAS2016 conference, please visit the CAS website http://www.imt.ro/cas/. For additional information contact us at e-mail address cas@imt.ro.

Prof. Dan Dascalu
(dan.dascalu@imt.ro)
CAS General Chairman
Member of the Romanian Academy
IEEE EDS Senior Member
IMT Bucharest, Romania

Cristian Ravariu
(cristian.ravariu@gmail.com)
IEEE ED Romania Section
Chapter Chair
Polytechnic University of
Bucharest, Romania

~Editor, Daniel Tomaszewski

The 62nd annual IEEE International Electron Devices Meeting (IEDM)

December 5-7, 2016

Hilton San Francisco Union Square Hotel

IEDM is the world's pre-eminent forum for technological breakthroughs in the areas of semiconductor and electronic device technology, manufacturing, design, physics, and modeling. The world's leading scientists and engineers will gather for a technical program of more than 220 presentations, along with panel sessions, tutorials, short courses, and other events spotlighting more leading work in more areas of the field than any other conference.

New in 2016: To provide faster dissemination of the conference's cutting-edge results, the abstract submission deadline has been moved to August 10th for submission of four-page, camera-ready abstracts. Accepted papers will be published as-is in the proceedings.

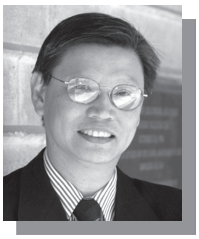
Papers in the following areas are encouraged:

- Circuit and Device Interaction
- Characterization, Reliability and Yield
- Compound Semiconductor and High Speed Devices
- Memory Technology
- Modeling and Simulation
- Nano Device Technology
- Optoelectronics, Displays, and Imagers
- Power Devices
- Process and Manufacturing Technology
- Sensors, MEMS and BioMEMS

For more information, visit the IEDM website: www.ieee-iedm.org

Newly Elected EDS Officers and BoG

ANNOUNCEMENT OF NEWLY ELECTED OFFICERS & BoG MEMBERS



Paul Yu
EDS Nominations and Elections Chair

In 2015, EDS continued the pilot program and had one of the seven BoG Member-at-Large seats elected via the entire EDS membership. The remaining six seats and officer positions were voted on by our BoG during the election, which took place on December 6, 2015, at the Washington Hilton in Washington, DC. The following are the results of the election and brief biographies of the individuals elected.

OFFICERS

The following individuals were elected as officers for a two-year term beginning January 1, 2016:

President-Elect

Fernando Guarín is a Distinguished Member of Technical Staff at Global Foundries in East Fishkill, New York, and Adjunct Lecturer at SUNY New Paltz. He retired from IBM's SRDC after 27 years as Senior Member of Technical Staff. He earned his BSEE from the "Pontificia Universidad Javeriana", in Bogotá, Colombia, the M.S.E.E. degree from the University of Arizona, and the Ph.D. in Electrical Engineering from Columbia University, New York. He has been actively working in microelectronic reliability for over 35 years.

From 1980 until 1988 he worked in the Military and Aerospace Operations division of National Semiconductor Corporation. In 1988 he joined IBM's microelectronics division where he worked in the reliability physics and modeling of Advanced Bipolar, CMOS and Silicon Germanium BiCMOS technologies.

Dr. Guarín is an IEEE Fellow and Distinguished Lecturer for the IEEE Electron Devices Society, where he has served in many capacities including; member of the IEEE's EDS Board of Governors, Chair of the EDS Education Committee, and Secretary for EDS. He is the President-Elect 2016–2017.

Secretary

Simon Deleonibus, retired from CEA-LETI on January 1, 2016, as Chief Scientist after 30 years of Research on Micro Nanoelectronics Devices Architectures. He was with Thomson Semiconductors (1981-1986) where he developed and transferred to production advanced microelectronics devices. He gained his PhD in Applied Physics from Paris University (1982).

He is Visiting Professor at Tokyo Institute of Technology (Tokyo, Japan) since 2014, Visiting Professor at National Chiao Tung University(Hsinchu, Taiwan) since 2015. He was distinguished CEA Research Director (2002), IEEE Distinguished Lecturer (2004), Fellow of the IEEE (2006), Fellow of the Electrochemical Society (2015).

Simon was awarded the titles of Chevalier de l'Ordre National du Merite (2004) and Chevalier de l'Ordre des Palmes Academiques (2011), the 2005 Grand Prix de l'Academie des Technologies.

He is member of the ITRS (1998), the European Research Council Panel (2007), the Nanosciences Foundation Board of Trustees (2007).

He was Associate Editor of *IEEE Transactions on Electron Devices* (2008–2014) and a member of the IEEE Electron Devices Society Board of Governors (January 2009 – December 2014) and re-elected (2016–2018). He is currently Secretary (2016–2017) and Region 8 SRC Chair (2015–2016) of the IEEE Electron Devices Society.

Treasurer

Subramanian S. Iyer (Subu) is Distinguished Chancellor's Professor in the Electrical Engineering Department at the University of California – Los Angeles, where he is director of the Center for Heterogeneous Integration and Performance Scaling (CHIPS). He obtained his B.Tech. from IIT-Bombay, and Ph.D. from UCLA and joined IBM, where he was appointed IBM Fellow and was till recently Director of the Systems Scaling Technology Department. His key technical contributions have been the development of the world's first SiGe base HBT, Salicide, eFuses, eDRAM, 45 nm technology used at IBM and IBM's development partners and 3-Dimensional Integration. He cofounded SiBond LLC to develop SOI substrates. He has published over 250 papers and holds over 70 patents. He has received several outstanding technical achievements and corporate awards at IBM. He is

an IEEE Fellow and a Distinguished Lecturer of the IEEE EDS. He is a Distinguished Alumnus of IIT Bombay and received the IEEE Daniel Noble Medal in 2012.

BoG MEMBERS-AT-LARGE

Second Term Electees:

Daniel Mauricio Camacho received his BSEE for Pontificia Universidad Javeriana, in Bogota, Colombia, in 2007, and his Masters degree from Southern Methodist University in Dallas, Texas in 2009. In 2008, he was awarded the IEEE EDS Masters Student Fellowship for his research work. He joined Intel in 2010, where he has been since then. His area of expertise is design of high-performance analog and mixed signal circuits. He has been a member of the EDS Board of Governors since 2013, he is also the current chairman of the EDS Young Professionals Committee.

Doug Verret was a high school teacher of math and physics from 1969–1974 and an instructor, then Assistant Professor of Physics and Pre-engineering from 1974–1979 at Xavier University, New Orleans, Louisiana. He joined Texas Instruments Inc. in 1979.

He has held several positions at Texas Instruments, the most recent of which was Program Manager for Flash EEPROM Development in which role his team developed micro-controller products with embedded flash for the automotive, safety and IOT markets. Prior to that, he was Program Manager in charge of developing technology for FPGA products. He has sixteen US patents covering such diverse technologies as Cu interconnects, deep trench isolation, polysilicon emitters, advanced bipolar devices and BiCMOS technology.

He was MOS Devices and Technology editor for the *IEEE Transactions on Electron Devices* 1994–2000 and Editor-in-Chief 2000–2011. He received the Electron Devices Society 2012 Distinguished Service Award.

First-Time Electees:

Navakanta Bhat received his Ph.D. in Electrical Engineering from Stanford University, in 1996. Then he worked at Motorola's Advanced Products R&D Lab in Austin, Texas until 1999. He is currently a Professor at the Indian Institute of Science (IISc), Bangalore. His current research is on Nanoelectronics and Sensors. He has more than 200 publications and 20 patents. He was instrumental in creating the National Nanofabrication Centre (NNfC) at IISc, benchmarked against the best university facilities in the world. He is the recipient of IBM Faculty award and Outstanding Research Investigator award (Govt. of India). He is a Fellow of INAE. He was the Editor of *IEEE Transactions on Electron Devices*, during 2013-2016. He is a member of the National Innovation Council in Nanoelectronics. He is the founder and promoter of a startup called "PathShodh Healthcare," which builds point-of-care diagnostics for diabetes and its complications.

Simon Deleonibus retired from CEA-LETI on January 1, 2016, as Chief Scientist after 30 years of Research on Micro Nanoelectronics Devices Architectures. He was with Thomson Semiconductors (1981-1986) where he developed and transferred to production advanced microelectronics devices. He gained his PhD in Applied Physics from Paris University (1982).

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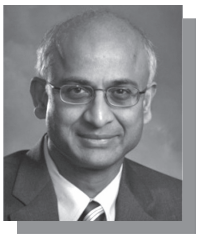
Meikei Ieong is currently Chief Technology Officer at Hong Kong Applied Science and Technology Research Institute (ASTRI). Prior to this, he has held various engineer and leadership positions in Taiwan Semiconductor Manufacturing Company (TSMC) and IBM Research. He holds a PhD degree in Electrical and Computer Engineering from University of Massachusetts, Amherst and an MBA degree from the MIT Sloan Fellows Program at MIT School of Management.

Dr. Ieong was General Chairman of the IEEE International Electron Devices Meeting (IEDM). He has served as an editor for the *IEEE Transaction on Electron Devices* since 2010 and as chair of the IEEE EDS Education Award Committee since 2013. He has published more than one hundred

papers in referred journals and conference proceedings and more than eighty patents. He is an IEEE Fellow in recognition of his leadership and contributions to Complementary Metal-Oxide-Semiconductor (CMOS) Device Technology.



Murty Polavarapu is a semiconductor industry consultant in Oakton, Virginia, USA. He has recently retired from BAE Systems following a long career in developing advanced memory and logic products for defense and aerospace markets. His experience also includes introduction of advanced DRAM and Flash memory products into commercial manufacturing at Toshiba and Micron. He holds Masters degrees in Physics from India, Electrical Engineering from Howard University and Technology Management from the University of Pennsylvania. He has been an active IEEE volunteer at EDS, Nanotechnology Council, IEEE-USA and Member and Geographic Activities. Polavarapu also served as a United States Peace Corps volunteer teacher in rural Fiji on a leave of absence. He has been recognized with IEEE Regional Activities Achievement Award, Dominion Semiconductor President's Award and IBM Outstanding Technical Achievement Award. He has been awarded eleven US patents.

Ravi Todi received his M.S. degree in Electrical and Mechanical Engineering from University of Central Florida in 2004 and 2005 respectively, and his doctoral degree in Electrical Engineering in 2007. His graduate research work was focused on gate stack engineering, with emphasis on binary metal alloys as gate electrode and on high mobility Ge channel devices. In 2007, he started working as Advisory Engineer/Scientist at Semiconductor Research and Development Center at IBM Microelectronics Division focusing on high performance eDRAM integration on 45 nm SOI logic platform. Starting in 2010, Ravi was appointed the lead Engineer for 22 nm SOI eDRAM development. For his many contributions to the success of eDRAM program at IBM, Ravi was awarded IBM's Outstanding Technical Achievement Award in 2011. Ravi Joined Qualcomm in 2012, responsible for 20 nm and 16/14 nm product developments. Currently Ravi is Director of Product Management at GLOBALFOUNDRIES. He is a Distinguished Lecturer for the IEEE Electron Devices Society and serves as Editor for *IEEE Transactions on Electron Devices*. Ravi had authored or co-authored over 50 publications, has over 10 issued US patents and over 25 pending disclosures. He has also served as an Officer/Treasurer for four years (2012–15) for EDS.

I welcome all electees and urge them to get fully engaged in the affairs of the Electron Devices Society. EDS is considered to be a volunteer-led, volunteer-driven organization and we expect nothing less from all to continue this tradition.

Paul Yu
EDS Nominations and
Elections Chair
University of California, San Diego
La Jolla, CA, USA

Message from EDS President Elect

Fernando Guarin
President Elect
(2016-2017)

Dear Readers and EDS Members,

It is a true honor and privilege to write to you as the EDS President Elect 2016–2017. I am grateful for the trust the voting members have placed in me and vow to make every effort to continue the fine example set by those who have preceded me in the EDS Presidency. The Electron Devices Society embodies a proud history of tangible contributions that have transformed society, changing the world in which we live. It is difficult to think of any other technical society that has had such a deep impact on the world. EDS has profoundly changed our ability to communicate, transport, heal, trade, power, compute, sense, control, display information and miniaturize, to name but a few of the applications enabled by advances in electron based devices. This transformation was made possible by the hard work, talent, ingenuity, publications, inventions, educational activities and solid technical foundation of our members. It is the job of the president to enable the continuation of the following outstanding contributions; fostering the dissemination of high quality technical information, bringing a cohesive force that represents the interest of our members throughout the world, providing added value to our members and thus continuing to promote excellence in the field of electron devices for the benefit of humanity.

My vision for the IEEE Electron Devices Society

Continue to work hard to increase EDS's leadership and relevance of our core areas:

- Publications
- Conferences
- Education
- Membership
- Awards and Chapters

I believe in increasing EDS's leadership and relevance, with measures that include:

- Strengthening our ties to academia – with better service to student's needs.
- Strengthening EDS ties to industry – to keep EDS technical areas relevant and enable our society to better serve our members in industry.
- Undertaking and supporting more high visibility projects, especially humanitarian and Smart Planet projects that visibly demonstrate EDS's commitment to its mission.
- The technology world is changing quickly. Internet magazines, social media, and Open Access publishing are allowing other players to provide significant value to technical professionals – which lessen the IEEE's EDS perceived value. We need to strengthen our publications and conferences while striving to create and provide more value for our EDS members.
- I support enhancing the networking and collaboration opportunities for members through use of social media and web based tools, thus demonstrating that EDS can successfully provide value in this space.

I am passionate about the success of EDS and will do may best as EDS President-Elect to increase EDS membership, enable the professional growth of our members, provide increased value to all our members in education, recognizing achievements while living up to IEEE's motto of Advancing Technology for Humanity.

Fernando Guarin
President Elect (2016-2017)
Global Foundries
East Fishkill, New York, USA

Message from Editor-in-Chief

M.K. Radhakrishnan
Editor-in-Chief

Dear EDS Members and Readers,

One of the challenging issues with electron devices is the heating. The technical article in this issue of the Newsletter discusses the self-heating aspects of surround gate transistors, especially in view of reliability and performance. This is the third invited article in the area of device reliability in our Technical article series. The first was "Reliability trends in Nano-scale CMOS" followed by "ESD during times of change" and now "Too hot to Handle". We would like to hear the views of readers about these and we request your suggestions for future topics. The idea behind publishing such technical articles by experts which are so digestible to any reader is to make everyone aware of the developments as well as challenges in the field.

Election to the newly arising positions in the Board of Governors was held during the December 2015 BoG meeting. An introduction of newly elected members is given in this issue. Also, we are announcing the details of various awards won by our members both within IEEE as well as elsewhere. A notable one is Australia's highest National Honor received by our active volunteer Prof. C. Jagadish of Australian National University and is featured in this issue. In the Young Professionals section we feature an interview with the EDS 2015 Early Career Award winner.

As I have repeatedly mentioned in this column, the feedback from readers is very much missing. The entire Newsletter team including editors and all support team members would like to hear from the readers. It is not difficult to make a comment, as the Newsletter is now available in electronic version and accessible to everyone.

Again, we all are looking for readers' views, comments, criticisms as well as suggestions, which only can make this Newsletter robust. And I request all the readers to write the feedback to edsnewsletter@ieee.org OR to me radhakrishnan@ieee.org.

MK Radhakrishnan
Editor-in-Chief, EDS Newsletter
e-mail: radhakrishnan@ieee.org

EDS VLSI Technology and Circuits Committee

On December 5, 2015, the VLSI Technology and Circuits Committee met in Washington, D.C., USA, during the 2015 IEEE International Electron Devices Meeting (IEDM) on December 7–9.

The VLSI Technology and Circuits Technical Committee was formed in 1998 under the leadership of Professor Charles G. Sodini (MIT), followed by Dr. H.-S. Philip Wong (IBM), Werner Weber (Infineon), Dr. James A. Hutchby (SRC), and Dr. Bin Zhao (Freescale Semiconductor). Since its formation, the VLSI Committee has made it their mission to identify new technical trends, help foster new technical concepts, and serve the emerging needs of the Electron Devices and Solid-State Circuits communities in VLSI. The committee members include many well recognized technical experts representing a very wide spectrum of technical expertise in VLSI devices, technology, and circuits.

The objective of the *VLSI Technology and Circuits Committee* is to identify new and relevant areas of interest to the Electron Devices and Solid-State Circuits communities. Based on the nature of the areas, the committee recommends any or all of the following:

1. Initiate topical workshops of current interest (attached to existing conferences or incorporated in new ones)
2. Special issues for major publications (e.g., T-ED)
3. Panel session topics, Invited talks and Special sessions for major conferences

The following topics were discussed during the December 5, 2015 meeting:

1. Membership
   a. The committee's current twenty eight geographically diverse members include:
      i. North America ten members
      ii. South America one member
      iii. Europe five members
      iv. Africa one member
      v. Asia eleven members
   b. Candidates for committee members starting in January of 2016 were discussed and agreed upon awaiting further approval.

The committee now has representatives from Asia, North/South America, Africa and Europe.

2. Sub-Committees Roles and responsibilities of the following subcommittees were discussed:
   a. Publication Chair: Steve Chang
   b. Conferences/Workshops Chair: Kaz Ishimaru
   c. Publicity Chair: Seiichiro Kawamura

Discussion was made to make a proposal on a special issue of T-ED on next generation of devices to replace 3-D Tri-Gate transistors and Novel Memories.

Please contact Dr. Kaz Ishimaru (kazu.ishimaru@toshiba.co.jp), conferences/workshops subcommittee chair, or Dr. Shu Ikeda (shu.ikeda@tei-solutions.com), committee chair, for further information.

Reza Arghavani
EDS VLSI TC Committee Member
Lam Research Corporation
Fremont, CA, USA

Standing from left to right – Hitoshi Wakabayashi, Min Yang, Mansun Chan, Steve S. Chung, Simon Deleonibus, Seiichiro Kawamura, Shuji Ikeda, Kazunari Ishimaru, Reza Arghavani, Jacobus Swart, Hiroshi Iwai.

EDS Member and IEEE Fellow Receives Australia's Highest Honor

Chennupati Jagadish

Professor Chennupati Jagadish, of Australian National University, has been awarded Australia's highest honor for his service to physics and engineering in the 2016 Australia Day Honors. Professor Jagadish was appointed a Companion of the Order of Australia (AC) for eminent service to physics and engineering, particularly in the field of nanotechnology, to education as a leading academic, researcher, author and mentor, and through executive roles with national and international scientific advisory institutions. Jagadish said he was humbled, honored and grateful for this honor. *"This is a wonderful recognition for 25 plus years of work with my research group at the ANU,"* said Jagadish, who works on semiconductor optoelectronics and nanotechnology.

With his research in nanotechnology, he is helping to develop a new class of lasers with applications in telecommunications and new lightweight solar cells with increased efficiency. Most interesting is the research on neuromorphic cells – artificial, trainable neurons – or "brain on a chip."

On receiving the honor, Jagadish said *"I feel very, very humbled to receive this honor and I owe it to the teachers in my school days in rural India, who made such a huge difference to my life."* Jagadish and his wife Vidya started the Chennupati and Vidya Jagadish endowment at the Australian National University to support visiting students and researchers from developing nations to visit ANU for 3–4 months, to carry out research in the Research School of Physics and Engineering.

Jagadish, a professor of physics at the Australian National University, is also the vice-president of the Australian Academy of Science and founded the Australian Nanotechnology Network, which has more than 1,400 members. He is a dedicated EDS volunteer and an IEEE Fellow.

M.K. Radhakrishnan
Editor-in-Chief, EDS Newsletter

2016 IEEE EDS Robert Bosch Micro and Nano Electro Mechanical Systems Award Winner

The 2016 IEEE EDS Robert Bosch Micro and Nano Electro Mechanical Systems Award, was presented to Professor Henry Baltes, ETH Zurich, Zurich, Switzerland, at the MEMS2016 Conference in Shanghai, China, on January 26, 2016. This prestigious award recognizes and honors advances in the invention, design, and/or fabrication of micro- or nano-electromechanical systems and/or devices.

For contributions to the exploration and development of CMOS-MEMS, to production using IC foundries and MEMS post-processing, and for inspirational leadership in the worldwide MEMS community

Henry Baltes is Professor Emeritus of ETH Zurich affiliated with Micro- and Nanosystems at the Department of Mechanical and Process Engineering. He was Professor of Physical Electronics at ETH Zurich and Director of the Physical Electronics Laboratory from 1988 to 2006. In 2004–05 he was in charge of starting the new Department of Biosystems Science and Engineering (D-BSSE) of ETH Zurich located at Basel. He is a Member of the Swiss Academy of Technical Sciences and a co-founder of the sensor manufacturer SENSIRION.

He received the Koerber European Science Award, the Wilhelm Exner Medal of the Austrian Trade Association, and the Swiss Technology Award. He holds honorary doctoral degrees of the Universities of Waterloo (Canada), Bologna (Italy), Freiburg (Germany), and University College London (UK).

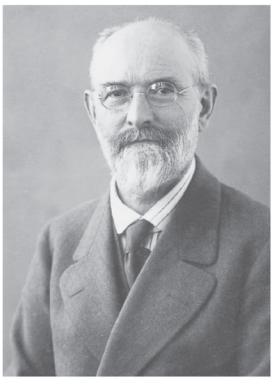
From 1983 to 1988 he held the Henry Marshall Tory Chair in Electrical Engineering at the University of Alberta, Edmonton, Canada. He was acting President of the Alberta Microelectronic Centre and a co-founder and Director of LSI Logic Corporation of Canada. From 1973 to 1982 he worked for a Swiss company and taught at EPF Lausanne. He received the degree of Doctor of Science of ETH Zurich in Physics in 1971.

He served as Co-Chair of the 14th IEEE International Conference on MEMS, held at Interlaken in 2001. He was elected Fellow of the IEEE in 2003 for contributions to the

development and commercialization of CMOS based MEMS and won the IEEE Donald G. Fink Prize Paper Award 2005. He served on the Editorial Board of the Proceedings of the IEEE in 2004–09. He also served on IEEE IEDM, IEEE Sensors, and Transducers conference committees.

Richard Muller
EDS Bosch Award Chair
University of California, Berkeley
Berkeley, CA, USA

IEEE ROBERT BOSCH
MICRO AND NANO ELECTRO MECHANICAL SYSTEMS AWARD



Robert Bosch (1861-1942)
Inventor, Entrepreneur, Founder of Robert Bosch GmbH

The Robert Bosch Micro and Nano Electro Mechanical Systems Award, was established by the IEEE Electron Devices Society in 2014 to recognize and honor advances in the invention, design, and/or fabrication of micro- or nano-electromechanical systems and/or devices. The contributions to be honored by this award should be innovative and useful for practical applications.

This award is sponsored by the IEEE Electron Devices Society with financial support from Robert Bosch LLC. It is intended that the award will be presented annually to an individual or to as many as three individuals whose achievements and contributions are judged to meet the selection criteria for the award. The award will be presented at an IEEE conference of the winner's choice. It is not necessary for the recipient(s) to be a member(s) of IEEE.

The recipient will receive a US$10,000 honorarium (which includes up to $3,000 of travel expenses for international travel and $1,500 of travel expenses for domestic travel), a bronze medal, and a certificate. In the event that more than one awardee is selected, the cash honorarium will be equally divided among the recipients. Each recipient will receive a bronze medal and a certificate.

Please visit the EDS website for more information on this award: http://eds.ieee.org/robert-bosch-micro-and-nano-electro-mechanical-systems-award.html.

Nominations for the 2017 award should be made using our online nomination form (available on the EDS webpage noted above), and submitted before midnight (EST) on October 2nd. Letters of recommendation must be sent directly to l.riello@ieee.org according to the same schedule.

2015 EDS J. J. Ebers Award Winner

The 2015 J. J. Ebers Award, the prestigious Electron Devices Society award for outstanding technical contributions to electron devices, was presented to Dr. Jack Yuan-Chen Sun of TSMC, HsinChu, Taiwan, at the IEEE International Electron Devices Meeting in Washington, DC, on December 7, 2015. This award recognizes Dr. Sun *"For sustained leadership and technical contributions to energy efficient foundry CMOS technologies."*

Dr. Jack Yuan-Chen Sun receiving the J. J. Ebers Award at the 2015 IEDM

Dr. Jack Yuan-Chen Sun received BSEE degree from National Taiwan University and MS and Ph.D. from the University of Illinois. He held research and management positions at IBM T. J. Watson Research Center between 1983 and 1997. He joined TSMC R&D in 1997 as Director of Advanced Module Technology, and then Senior Director of Logic Technology. He became Vice President of R&D in 2006 and Chief Technology Officer at TSMC in 2009.

He made key contributions to the successful energy efficient CMOS logic SOC platforms with highest routed gate density and computation throughput for the foundry/fabless industry at TSMC. He advocated a holistic energy efficient 3D × 3D system scaling concept. Throughout his career, he and his co-workers pioneered and set many world records in CMOS, bipolar, and BiCMOS.

Dr. Sun received a number of technical and management awards from IBM, TSMC, professional societies, and government. He was awarded a TSMC Medal of Honor in 2011. He is an IEEE Fellow for his contributions to CMOS technology. He has authored and co-authored over 200 papers and conference presentations, 12 US patents, and several ROC patents.

Jayant Baliga
EDS J.J. Ebers Award Chair
North Carolina State University
Raleigh, NC, USA

IEEE ELECTRON DEVICES SOCIETY
J.J. EBERS AWARD

Nominate:
J.J. Ebers Award
on-line nomination form:

https://ieeeforms.wufoo.com/forms/xl0lxns05xzwir/

Submission Deadline:
July 1, 2016

Contact:
If you have any questions regarding the EDS J.J. Ebers Award, please contact Laura Riello of the EDS Executive Office at l.riello@ieee.org

Visit:
http://eds.ieee.org/jj-ebers-award.html

CALL FOR NOMINATIONS

The IEEE Electron Devices Society invites the submission of nominations for the 2016 J.J. Ebers Award. This award is presented annually by EDS to honor an individual(s) who has made either a single or a series of contributions of recognized scientific, economic, or social significance to the broad field of electron devices. The recipient(s) is awarded a plaque and a check for $5,000, presented at the International Electron Devices Meeting (IEDM).

ELECTRON DEVICES SOCIETY®

2015 EDS Education Award Winner

The EDS Education Award recognizes an IEEE/EDS Member from an academic, industrial, or government organization with distinguished contributions to education within the fields of interest of the IEEE Electron Devices Society. Roger Howe was recognized at the IEEE International Electron Devices Meeting in Washington, DC on December 7, 2015, as the 2015 EDS Education Award winner. The award cites Professor Howe *"For contributions to mentoring and education in the fields of microelectromechanical systems and nanotechnology."*

Roger Howe receiving the EDS Education Award from Albert Wang, at IEDM

Roger T. Howe received a B.S. degree in physics from Harvey Mudd College in 1979 and an M.S. and Ph.D. degrees in electrical engineering from the University of California, Berkeley in 1981 and 1984. After faculty positions at Carnegie-Mellon University and the Massachusetts Institute of Technology from 1984–1987, he returned to Berkeley where he was a Professor until 2005, when moved to Stanford. He is currently the William E. Ayer Professor in the Department of Electrical Engineering and the Faculty Director of the Stanford Nanofabrication Facility.

His research interests include micro electromechanical system design, micro- and nano-machining technologies. He and his group are currently working on applications in energy conversion and biomolecular sensing. A focus of his research has been processes to fabricate integrated microsystems, which incorporate both silicon integrated circuits and MEMS. Prof. Howe has made contributions to the design of MEMS accelerometers, gyroscopes, electrostatic actuators, and microresonators.

Over the past 25 years, Prof. Howe has helped to run conferences in the MEMS field, including serving as Co-Chair of the 1990 IEEE MEMS Workshop in Napa and Technical Program Chair of the 2003 IEEE International Conference on Solid-State Sensors, Actuators, and Microsystems (Transducers 2003) in Boston. He was elected an IEEE Fellow in 1996 and was the co-recipient (with Prof. Richard S. Muller of Berkeley) of the 1998 IEEE Cledo Brunetti Award and he was also the co-recipient (with Prof. Yu-Chong Tai of Caltech) of the 2015 IEEE EDS Robert Bosch Award – all for his contributions to MEMS processes, devices, and systems. He was elected to the U.S. National Academy of Engineering in 2005. From 2011 – 2015, he was Director of the National Nanotechnology Infrastructure Network (NNIN), which was an NSF-funded collaboration of 14 university nanofabrication facilities.

In addition to his research in micro and nano electromechanical systems, he co-authored an undergraduate electronics textbook, *Microelectronics: an Integrated Approach*, (Prentice Hall, 1997) with Prof. Charles G. Sodini of MIT and co-edits with him the Modular Series of Microelectronic Device & Circuit Design (NTS Press). Through 30 years of serving on the faculty of four outstanding research universities, it has been his privilege to mentor over 40 creative and hard-working Ph.D. students and 15 postdoctoral scholars.

Meikei Ieong
2015 EDS Education Award Chair
TSMC Europe BV
Amsterdam

EDS Members Recently Elected to IEEE Senior Member Grade!

Mark Anders	Woo Young Choi	Heng-Ming Hsu	Sean Lyn	Ionut Radu
Adrijan Baric	Garry Cunningham	Bommanna Raja K	Mohsin Nawaz	Kartik Raol
Anuj Bhatia	Andrea Chetti	Jinfeng Kang	Iulian Nistor	Robert Scott
Scott Butler	David Gibson	Trupti Lenka	Siavash Pourkamali	Stefan Siegel
Zhihong Chen	Pouya Hashemi	Hai Li		

If you have been in professional practice for 10 years, you may be eligible for Senior Membership, the highest grade of membership for which an individual can apply. New senior members receive a wood and bronze plaque and a credit certificate for up to US $25 for a new IEEE society membership. Upon request a letter will be sent to employers, recognizing this new status.

For more information on senior member status, visit: http://www.ieee.org/membership_services/membership/senior/index.html

To apply for senior member status, fill out the on-line application: https://www.ieee.org/membership_services/membership/senior/application/index.html.

You will need to Sign-in with your IEEE account.

Please remember to designate the Electron Devices Society as your nominating entity!

2016 EDS EDUCATION AWARD
CALL FOR NOMINATIONS

The IEEE Electron Devices Society invites the submission of nominations for the EDS Education Award. This award is presented annually by EDS to honor an individual(s) who has made distinguished contributions to education within the field of interest of the Electron Devices Society. The recipient(s) is awarded a plaque and a check for $2,500, presented at the IEEE International Electron Devices Meeting (IEDM).

The nominee must be an EDS member engaged in education in the field of electron devices, holding a present or past affiliation with an academic, industrial, or government organization. Factors for consideration include achievements and recognition in educating and mentoring students in academia or professionals in the industrial or governmental sectors. Specific accomplishments include effectiveness in the development of innovative education, continuing education programs, authorship of text books, presentation of short-courses at EDS sponsored conferences, participation in the EDS Distinguished Lecturer program, and teaching or mentoring awards.

Since this award is solely given for contributions to education, the nomination should exclude emphasis on technical contributions to engineering and physics of electron devices.

Nomination forms can be found on the EDS website: http://eds.ieee.org/education-award.html

The deadline for the submission of nominations for the 2016 award is September 1, 2016.

2015 EDS Early Career Award Winner

The EDS Early Career Award recognizes young IEEE/EDS members who have made outstanding contributions in an EDS field of interest during the early years of their professional career after graduation.

The 2015 EDS Early Career Award was presented to Mayank Shrivastava of the Indian Institute of Science Bangalore, Bangalore, India, at the EDS awards dinner held in conjunction with the IEEE International Electron Devices Meeting in Washington, DC, on December 6, 2015.

Albert Wang presenting the 2015 EDS Early Career Award to Dr. Mayank Shrivastava

Dr. Mayank Shrivastava is an Assistant Professor in the Department of Electronic Systems Engineering, Indian Institute of Science Bangalore, India. He has over 50 publications in international journals and conferences and 25 patents in the areas of Electron Devices and Nanoelectronics. He was among the first recipient of Indian section of American TR35 award. He is also a recipient of multiple awards and honors including excellence award for his PhD thesis in 2010 and industrial impact award from IIT Bombay in 2008.

Dr. Shrivastava was born in Lucknow, India, in the year 1984. He got his Bachelor's degree in Engineering from Rajiv Gandhi Technical University in 2006. He joined IIT Bombay in the year 2006 for the master's program from where he graduated with PhD degree in the year 2010.

Dr. Shrivastava held short term visiting positions at Infineon Technologies, Munich, Germany from April 2008 to October 2008 and again in May 2010 to July 2010. He worked for Infineon Technologies, East Fishkill, New York; Intel Mobile Communications, Hopewell Junction, New York; and Intel Corp., Mobile and Communications Group, Munich, Germany, between 2010 and 2013. He joined Indian Institute of Science as an Assistant professor in the year 2013, where he established the Advance Nanoelectronic Device and Circuit Research Group.

Samar Saha
EDS Early Career Award Chair
Prospicient Devices
Milpitas, CA, USA

CALL FOR NOMINATIONS
2016 IEEE EDS Early Career Award

Description: Awarded annually to an individual to promote, recognize and support Early Career Technical Development within the Electron Devices Society's field of interest

Prize: An award of US$1,000, a plaque; and if needed, travel expenses not to exceed US$1,500 for a recipient residing in the US and not to exceed US$3,000 for a recipient residing outside the US to attend the award presentation.

Eligibility: Candidate must be an IEEE EDS member and must have received his/her first professional degree within the 10th year defined by the August 15 nomination deadline and has made contributions in an EDS field of interest area. Nominator must be an IEEE EDS member. Previous award winners are ineligible.

Selection/Basis for Judging: The nominator will be required to submit a nomination package comprised of the following:

- The nomination form that is found on the EDS web site, containing such technical information as the nominee's contributions, accomplishments and impact on the profession or economy and a biographical description.
- A minimum of two and a maximum of three letters of recommendation from individuals familiar with the candidate's technical contributions and other credentials, with emphasis on the specific contributions and their impacts.

The basis for judging includes such factors as: the demonstration of field leadership in a specific area; specific technical contribution(s); impact on the profession or economy; originality; breadth; inventive value; publications; honors; and other appropriate achievements.

Schedule: Nominations are due to the EDS Executive Office on August 15th each year. The candidate will be selected by the end of September, with presentation to be made in December.

Presentation: At the EDS Awards Dinner that is held in conjunction with the IEEE International Electron Devices Meeting (IEDM) in December. The recipient will also be recognized at the December EDS BoG Meeting.

Nomination Form: Complete the nomination form by August 15, 2016. All endorsement letters should be sent to l.riello@ieee.org by the deadline.

For more information contact: l.riello@ieee.org or visit: http://eds.ieee.org/early-career-award.html

Congratulations to the Newly Elected IEEE Electron Devices Society Fellows

Effective January 1, 2016

Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, Netherlands
for contributions to the design of circuits with organic thin film transistors

Chorng-Ping Chang, Applied Materials, Inc., Santa Clara, CA, USA
for contributions to replacement gate and shallow trench isolation for CMOS technology

Gilles Dambrine, IEMN—Institute of Electronic, CNRS, France
for contributions to the modeling of small signal and noise characteristics in nanoscale high-frequency devices

Ananth Dodabalapur, Univeristy of Texas at Austin, Austin, TX, USA
for contributions to organic electronic devices and circuits

Ravindranath Droopad, Texas State University, San Marcos, TX, USA
for contributions to epitaxial growth of advanced materials for RF and CMOS applications

Mukta Farooq, IBM Corporation, Hopewell Jct, NY, USA
for contributions to 3D integration and interconnect technology

Patrick Fay, University of Notre Dame, Notre Dame, IN, USA
for contributions to compound semiconductor tunneling and high-speed device technologies

Patrick French, TU Delft- Delft University of Technology, Delft, Netherlands
for contributions to micro-electromechanical devices and systems

Tibor Grasser, Technische Universität Wien: TU Wien, Vienna, Austria
for contributions to modeling the reliability of semiconductor devices

Guido.Groeseneken
2015 EDS Fellows Chair

Mark Hersam, Northwestern University, Evanston, IL, USA
for contributions to carbon nanomaterial processing methods and devices

Qing-An Huang, Beijing Institute of Technology, Beijing, China
for contributions to the design and control of biped robots

Qing-An Huang, Southeast University, Nanjing, China
for contributions to modeling and packaging of microsensors and microactuators)

Adrian Ionescu, EPFL—École polytechnique fédérale de Lausanne, Lausanne, Switzerland
for contributions to the development of novel devices for low power applications

Alvin Joseph, IBM Thomas J. Watson Research Center, Yorktown Heights, NY, USA
for contributions to silicon-germanium bipolar-CMOS and RF silicon-on-insulator technology

Jong Ho Lee, Seoul National University, Seoul, Korea
for contributions to development and characterization of bulk multiple gate field effect transistors

Victor Lubecke, University of Hawaii at Manoa, Honolulu, HI, USA
for leadership in the development of microwave transducers for biomedical application

Jian-Guo Ma, Tianjin University, Tianjin, China
for leadership in microwave electronics and RFIC applications

Souvik Mahapatra, IIT—Indian Institute of Technology Bombay, Mumbai, India
for contributions to CMOS transistor gate stack reliability

Sudip Mazumder, University of Illinois at Chicago, Chicago, IL, USA
for contributions to analysis and control of power electronics systems

Ellis Meng, University of Southern California, Los Angeles, CA, USA
for contributions to biomedical microelectromechanical systems

Ajay Poddar, Synergy Microwave Corporation, Paterson, NJ, USA
for contributions to microwave oscillators

Leonard Register, The University Texas At Austin, Austin, TX, USA
for contributions to modeling of charge transport in nanoscale CMOS devices

Akira Toriumi, University of Tokyo, Tokyo, Japan
for contributions to device physics and materials engineering for advanced CMOS technology

Ernest Wu, IBM Microelectronics-Avent, Inc., Essex Junction, VT, USA
for contributions to gate oxide reliability of CMOS devices

Guido.Groeseneken
2015 EDS Fellows Chair
Imec and ESAT Dept, K.U. Leuven
Leuven, Belgium

Status Report from the 2015 EDS PhD Student Fellowship Recipients

Carmen Lilley
EDS Student Fellowship Committee Chair

The EDS PhD Student Fellowship Program is designed to promote, recognize, and support graduate level study and research within the Electron Devices Society's Fields of Interest.

The 2015 EDS PhD Student Fellowship recipients were: **Shahab Akhavan** – Bilkent University, Ankara, Turkey, **Der-Hsien Lien –** National Taiwan University, Taipei, Taiwan, and **Max Shulaker** – Stanford University, Stanford, California, USA. The following are brief progress reports provided by the award winners.

Shahab Akhavan is continuing his research work on solution processed optoelectronic devices such as 0D and 2D materials. Recently, he has been able to successfully synthesized 2D nanomaterials and used them as photoactive layers in light-sensitive nanocrystal skins. 2D materials show superior electronically properties compared to quantum dots. These materials accelerate the recovery time and fasten the response time of fabricated devices. Furthermore, charge trapped mechanism has been heavily studied in stacking and non-stacking mode. As part of his graduate study, he also works on enhancing the non-rdiative energy transfer between nanocrystals via localized surface plasmon. Currently, he is writing his papers and expected to publish them within this year.

Der-Hsien Lien has been making further progress on improving electronic and optical properties of two-dimensional materials. His most recent output has been the development of a technique to improve the quality of MoS_2 that could help to achieve defect-free semiconducting monolayers. This technique could solve degradation problem caused by defects in addition to allowing for new types of low-energy switches. This work is published at Science, 2015 December. He is also exploring the applicability of his technique to device applications as well as other material systems. He is currently on a visiting scholarship at UC Berkeley.

Max Shulaker is currently in the 5th year of his PhD at Stanford University, working under the direction of Professor Subhasish Mitra and co-advised by Professor H.-S. Philip Wong. Max is continuing to make progress on his research towards realizing nanosystems, which leverage the unique properties of emerging nanotechnologies to create new integrated circuit architectures. Currently, Max is focusing on experimentally demonstrating monolithic three-dimensional integrated systems, with vertically-integrated layers of logic, memory, and sensing. To realize such monolithic three-dimensional integrated systems, Max is continuing his work on carbon nanotube-based digital logic, with recent results presented at the 2015 International Electron Devices Meeting.

Carmen Lilley
EDS Student Fellowship Committee Chair
University of Illinois at Chicago
Chicago, IL, USA

2016 PhD Student Fellowship

Description: One year fellowships awarded to promote, recognize, and support PhD level study and research within the Electron Devices Society's field of interest. The field of interest for EDS is all aspects of engineering, physics, theory, experiment and simulation of electron and ion devices involving insulators, metals, organic materials, plasmas, semiconductors, quantum-effect materials, vacuum, and emerging materials. Specific applications of these devices include bioelectronics, biomedical, computation, communications, displays, electro and micro mechanics, imaging, micro actuators, optical, photovoltaics, power, sensors and signal processing.

It is expected that three fellowships will be awarded, with the intention of at least one fellowship being given to eligible students in each of the following geographical regions every year: Americas, Europe/Middle East/Africa, and Asia & Pacific. Only one candidate can win per educational institution.

Prize: US$5,000 to the student and if necessary funds are also available to assist in covering travel and accommodation costs for each recipient to attend the EDS Governance meeting for presentation of the award plaque. The EDS Newsletter will feature articles about the EDS PhD Fellows and their work over the course of the next year.

Eligibility: Candidate must be an IEEE EDS student member at the time of nomination; be pursuing a doctorate degree within the EDS field of interest on a full-time basis; and continue his/her studies at the current institution with the same faculty advisor for twelve months after receipt of award. Nominator must be an IEEE EDS member. Previous award winners are ineligible.

Basis for Judging: Demonstration of his/her significant ability to perform independent research in the fields of electron devices and a proven history of academic excellence.

May 15, 2016 Submission Deadline

Nomination Package

- Nomination letter from an EDS member
- Two letters of recommendation from individuals familiar with the student's research and educational credentials. Letters of recommendation cannot be from the nominator.
- One-page biographical sketch of the student (including student's mailing address and email address)
- Two-page (maximum) statement by the student describing his or her education and research interests, accomplishments and graduation date
- One copy of the student's under-graduate and graduate transcripts/grades. Please provide an explanation of the grading system if different from the A-F format.

Timetable

- Completed nomination packages are due at the EDS Executive Office no later than **May 15, 2016**
- Recipients will be notified by July 15
- Monetary awards will be given by August 15
- Formal award presentation will take place at the EDS Governance Meeting in December

Please submit application packages via e-mail or mail:

Email: edsfellowship@ieee.org

Mail:
IEEE EDS Executive Office
PhD Student Fellowship Program
445 Hoes Lane
Piscataway, NJ 08854 USA

For more information contact:
edsfellowship@ieee.org

Visit the EDS website:
http://eds.ieee.org/eds-phd-student-fellowship.html

2016 Masters Student Fellowship

Description: One-year fellowships awarded to promote, recognize, and support graduate Masters level study and research within the Electron Devices Society's field of interest: all aspects of engineering, physics, theory, experiment and simulation of electron and ion devices involving insulators, metals, organic materials, plasmas, semiconductors, quantum-effect materials, vacuum, and emerging materials. Specific applications of these devices include bioelectronics, biomedical, computation, communications, displays, electro and micro mechanics, imaging, micro actuators, optical, photovoltaics, power, sensors and signal processing.

Three fellowships will be awarded, with the intention of at least one fellowship being given to eligible students in each of the following geographical regions every year: Americas, Europe/Mid-East/Africa, Asia & Pacific. Only one candidate can win per educational institution.

Prize: US$2,000 and a plaque to the student, to be presented by the Dean or Department head of the student's enrolled graduate program.

Eligibility: Candidate must be an IEEE EDS student member at the time of nomination; be accepted into a graduate program or within the first year of study in a graduate program in an EDS field of interest on a full-time basis; and continue his/her studies at a graduate education institution. Nominator must be an IEEE EDS member and preferably be serving as the candidate's mentor or faculty advisor. Previous award winners are ineligible.

Basis for Judging: Demonstration of his/her significant ability to perform research in the fields of electron devices and proven history of academic excellence in engineering and/or physics as well as involved in undergraduate research and/or supervised project.

May 15, 2016 Submission Deadline

Nomination Package

- Nomination letter from an EDS member who served as candidate's mentor or faculty advisor.
- One letter of recommendation from an individual familiar with the student's research and educational credentials. Letters of recommendation cannot be from the nominator.
- One-page biographical sketch of the student (including mailing address and e-mail address)
- Two-page (maximum) statement by the student describing his or her education and research interests, accomplishments and graduation date. This can include undergraduate, graduate and summer internship research work.
- One copy of the student's transcripts/grades. Please provide an explanation of the grading system if different from the A-F format.

Timetable

- Completed nomination packages are due at the EDS Executive Office no later than **May 15, 2016**
- Recipients will be notified by July 15
- Monetary awards will be presented by the Dean or Department Chair of the recipient's graduate program at the beginning of the next academic term.

Please submit application packages via e-mail or mail:

Email: edsfellowship@ieee.org

Mail:
IEEE EDS Executive Office
PhD Student Fellowship Program
445 Hoes Lane
Piscataway, NJ 08854 USA

For more information contact:
edsfellowship@ieee.org

Visit the EDS website:
http://eds.ieee.org/eds-masters-student-fellowship.html

Young Professionals

Reflections from Young Professionals

Mayank Shrivastava

The Young Professional guest in this issue of the Newsletter is Mayank Srivastava, Electron Devices Society's 2015 Early Career Award winner and a faculty member at Indian Institute of Science, Bangalore, India. His perceptions about EDS and views regarding professional development and career growth are reflected in the discussion. Here are the excerpts of the interview made by M.K. Radhakrishnan, the Newsletter Editor-in-Chief, with Mayank Srivastava.

MKR: As a young professional, why do you consider the membership in IEEE and especially in EDS is important?

Mayank: IEEE, being the largest professional organization, gives young professionals an opportunity to stay tuned with the peer groups. It keeps us informed about the scientific and engineering activities around the world, which continuously motivates YPs to work for the betterment of society and mankind in general. Electron devices being my broad area of research, EDS membership eases the interaction with researchers having similar interest and keeps us updated about the cutting edge research. This keeps us on our toes, with a view of giving our best to the society.

MKR: What was the specific temptation, if any, which made you want to join the largest professional organization in the globe, at first?

Mayank: It is in common interest to take the science forward for global good. A closer look reveals a very clear difference in the growth path of IEEE members and non-members. This is attributed to the fact that IEEE provides a wonderful platform to create, showcase or receive knowledge. Knowledge creation and sharing is the key to success in the 21st century. Therefore, it is hard to think of carrier growth without being associated with a professional organization promoting knowledge, and IEEE membership offers everything under one roof.

MKR: Mayank, you won the prestigious EDS 2015 Early Career Award, an honor most of the young professionals aspire. How do you consider this recognition and what are your plans to further develop your research career from here?

Mayank: I am humbled to receive this prestigious accolade, thanks to IEEE and EDS. Such an accomplishment in general motivates to constantly move forward with greater enthusiasm. My contributions so far have been in the field of electron devices for advance system on chip. I work at the two extremes of electron device research, on one hand I work on nanoscale devices/technology, and at the other extreme I have been focusing on electron devices for power electronic applications. My vision is to bring goods of both the extremes together for integration of more complex functionalities inside a single chip.

MKR: As a Professional, what are your interests which coincide with EDS activities and your own technical field? How your professional life blends with the services you perform as an EDS member/volunteer?

Mayank: The opportunity to interact with fellow researchers and easy knowledge sharing are true reflection of my professional interests. EDS has been very active in promoting research and knowledge sharing through a range of activities. As an EDS member, I am able to keep a vigil eye on the ongoing advancement in the cutting edge of electron devices, which keeps me updated and motivated.

MKR: What are your views about the EDS membership and its paybacks? Whether the EDS membership stimulated you at any time in your career growth? If so, how?

Mayank: The payback is in terms of knowledge sharing through our research. The membership certainly stimulates carrier growth, by providing opportunity to interact with fellow researchers and easy knowledge sharing.

MKR: As a YP, how do you consider the ED Society as a focused professional group? What are the changes or developments you would like to see in evolving this professional body as a group devoted to the humanity and its causes?

Mayank: Yes, a highly focused professional group. Electron devices or semiconductor technology has been among the biggest drivers of technological advancements in the past. The future projections are not too different. EDS should promote teaching semiconductor technology at early stages of professional carrier.

MKR: What are your specific suggestions and recommendations for those young professionals who may aspire to join EDS?

Mayank: I would highly recommend the young professionals to be a part of this prestigious community. It will accelerate their career and inspire them to extend their knowledge boundaries and strengthen their professional network through interaction with bright minds globally.

***Mayank Shrivastava** is an Assistant Professor in the Department of*

Electronic Systems Engineering, Indian Institute of Science Bangalore, India. Dr. Shrivastava has over 50 publications in international journals and conferences and 25 patents in the areas of Electron Devices and Nanoelectronics. He was among the first recipients of Indian section of American TR35 award. He is also a recipient of multiple awards and honors, including an excellence award for his PhD thesis in 2010 and industrial impact award from IIT Bombay in 2008, and very recently the prestigious IEEE EDS Early Carrier Award 2015.

Dr. Mayank Shrivastava was born in Lucknow, India, in 1984. He earned his Bachelor's degree in Engineering from Rajiv Gandhi Technical University in 2006. He joined IIT Bombay in 2006 for the master's program from where he graduated with a PhD degree in 2010.

Mayank Shrivastava held short term visiting positions in Infineon Technologies, Munich, Germany, from April 2008 to October 2008 and again in May 2010 to July 2010. He worked for Infineon Technologies, East Fishkill, NY; Intel Mobile Communications, Hopewell Junction, NY; and Intel Corp., Mobile and Communications Group, Munich, Germany between 2010 and 2013. He joined Indian Institute of Science as an Assistant professor in 2013, where he established the Advance Nanoelectronic Device and Circuit Research Group.

EDS Education Programs

Hillsborough High School iSTEM Club

by Jerry Silver and Nagi Naganathan

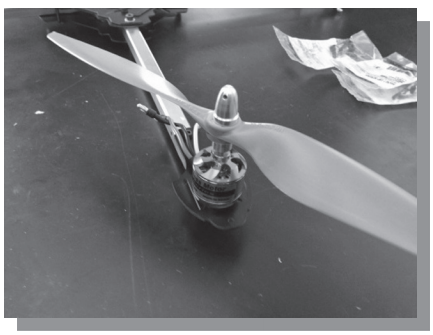
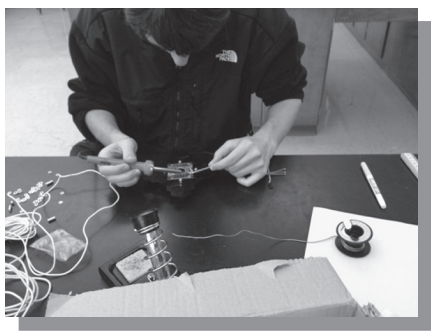
The Hillsborough High School iSTEM club in New Jersey has been holding biweekly meetings for the 2015–2016 academic year.

Our main project this year is building a quadcopter using purchased components such as stepper motors, PWM (pulse width modulated) motor controllers, RF generator and receiver, and frame. Students are assembling the parts and learning how the digital logic is implemented.

Students are continuing basic studies of electrical circuits by building projects using the Snap Circuits kits and Arduino boards acquired in past years. The HHS iSTEM club was very fortunate to have recently received *Circuit Scribe* kits that enable exploration of electronic circuits by forming electrical connections with conductive ink. The club plans to send a group of students to the Princeton University engineering challenge in 2016.

Students are also exploring the various STEM fields by sharing videos found on-line and by inviting speakers (including HHS faculty members) to talk about their experiences in industry. One group of students is planning to document some of our projects in a poster paper.

A few photos of the quadcopter are shown with this report. The HHS iSTEM would like to acknowledge the support provided by the IEEE Electron Devices Society and its EDS-ETC program, with the donation of Circuit Scribe and Snap Circuits kits and the support provided the IEEE Princeton/Central Jersey Section. The club is supported by Mr. Jerry Silver, Physics teacher, who serves as an advisor and Nagi Naganathan, Secretary, IEEE Princeton/Central Jersey Section who serves as an external advisor to the club.

Hillsborough High School iSTEM Club's quadcopter project

Report on EDS-ETC Program at National University of Malaysia (UKM)

By Badariah Bais and Zubaida Yusoff

EDS-ETC Train-the-Trainer (ToT) Sessions

In conjunction with the IEEE Day program at IMEN, UKM, two EDS-ETC Train-the-Trainer (ToT) sessions for were held for postgraduate and undergraduate students October, 1, 2015, at the Institute of Microengineering and Nanoelectronics (IMEN), Universiti Kebangsaan Malaysia (UKM) by EDS volunteers. A total of 5 postgraduates and 11 undergraduates participated in these sessions where they used the donated Snap Circuits kits to create 5 different electronic circuits. These postgraduate and undergraduate students will then facilitate the EDS-ETC sessions for school kids.

EDS-ETC Train-the-Trainer (ToT) session for postgraduates and undergraduates

IEEE Day 2015

IEEE EDS Malaysia – Kuala Lumpur and IMEN, UKM organized an event on IEEE Day 2015 entitled, "Electrical and Electronic Engineering Workshop for Schools," October 6. 2015. This project was partially funded by the IEEE Region 10 Educational Activities Board. A total of 5 primary schools around Bandar Baru Bangi city attended the workshop. Each school comprised of a Science teacher and 4 primary school students aged 12 years. The event kicked off at 9:00 a.m. and was officiated by IMEN Director and IEEE EDS Malaysia Advisor, Prof. Dato Dr. Burhanuddin Yeop Majlis followed by a talk by Dr. Zubaida Yusoff on "What is an Engineer?" Next, Dr. Susi from IMEN who is also IEEE EDS Malaysia Secretary, gave an overview of IEEE, EDS, IEEE Day 2015 and briefed the students on the EDS-ETC kit. Each school assembled components for 5 projects related to electronic circuits i.e., a) Electric Light & Switch, b) DC Motor & Switch, c) Sound Activated Switch, d) Flying Saucer and e) Simple Water Alarm. Upon completion of the circuits, the students answered 15 questions related to the projects. Winners were chosen and hampers were given away by IEEE EDS Malaysia Chair, Dr. Badariah Bais. The workshop was supported by IEEE EDS members, Faculty of Engineering undergraduate students and IMEN postgraduate students who volunteered to be demonstrators of the projects. The University's Community and Transformation Centre (UCTC) assisted us in obtaining approval from the Malaysian Ministry of Education and the Selangor

Participants prior to the workshop at IMEN, UKM

Participants and volunteers assembling the electronic circuits

State Education Department. After lunch, all participants visited IMEN laboratories and the program ended at 2:00 p.m.

The students and volunteers were excited and gained much knowledge about IEEE and electronic circuits. The program had definitely encouraged them to consider electrical and electronic engineering as a career. Three photos and 1 video of the program were submitted to the IEEE Day 2015 online Photo Contest and Video Contest.

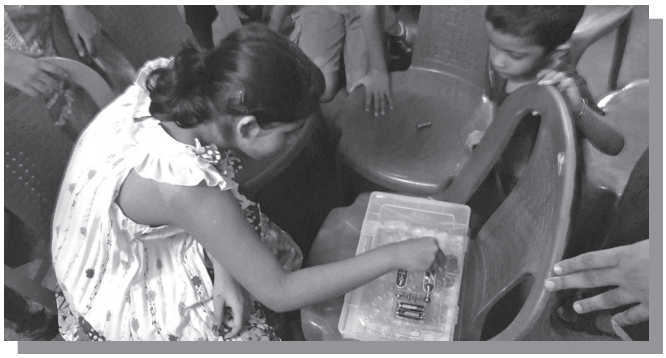
~ P. Susthitha Menon, Editor

EDS-ETC Programs in Calcutta

By Atanu Kundu

The ED Heritage Institute of Technology (HITK) Student Branch Chapter, jointly with the ED Kolkata Chapter, Kasba Social Development Society, Dino Bondhu Trust and Cognizant Technology Solutions Outreach team, organized an EDS-ETC Program October 3 and 5, 2015. The program was organized for the poor, but very meritorious school students from class V to X. The students found it very interesting. A total number of 5 projects were carefully selected and demonstrated to the students with the help of Elenco Snap Circuits kits. There were 20 participants who attended the workshop, which included experiments demonstrating the basic concept of electronic devices and circuits.

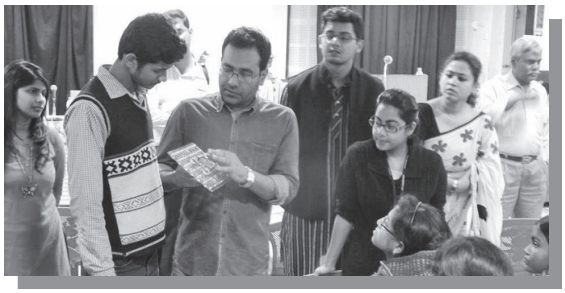
Student instructor helping younger students



Participants of the EDS-ETC Program in Kolkata

The EDS HITK Student Branch Chapter, jointly with IEEE EDS Kolkata Chapter, the NGO 'Aalo', and Cognizant Technology Solutions Outreach team, organized an EDS-ETC Program on January 18, 2016. The program was part of a scholarship program of the NGO 'Aalo'. This scholarship is for the students from class XI and XII of of West-Bengal.

A few projects were demonstrated to the students with the help of the Elenco Snap Circuits kits. There were 50 participants who attended the program. The experiments demonstrated the basic concept of electronic devices and circuits.



Demonstration of the projects with the help of the electronic 'Snap Circuits'

Participants of the EDS-ETC Program

IEEE Hong Kong Education Chapter and EDS Organize Electronic Winter Camp to Foster Future Engineers

By Mansun Chan, EDS Education Committee Chair

With the success of the Electronic Winter Camp hosted by the IEEE ED/SSC Hong Kong Chapter in previous years, EDS has developed standard training material for non-specialists to offer electronic training classes. This year, EDS collaborated with the IEEE Hong Kong Education Chapter to help non-engineering students lead the winter camp based on the pre-defined training material. The winter camp was held on December 28–30, 2015, and attracted over 50 students ranging from 10 to 15 years old. As in previous years, the young children at the camp have to construct various electronic gadgets such as running light, electronic piano, infrared transmitter/receiver and digital counter, on breadboards with generic components. But in this year, the course instructors are coming from non-engineering backgrounds ranging from science to business majors. Both the instructors and the students are learning together, experiencing a very dynamic interaction. Compared with previous winter camps hosted by engineering students, the non-engineering instructors are able to understand the difficulties of the students and add a lot of non-technical components to the teaching, such as magic and music. It has created a very lively interaction out-of-the-class atmosphere between the instructors and the students. The event represents EDS's mission to reach out to the community and young people, in

Winter Camp participants at the Hong Kong University of Science and Technology

addition to serving its members. In addition to stimulating the interest of young children to electronic design, the camp also provided an opportunity for the non-engineering university students to understand how electronic technology is affecting our everyday life.

The camp was a big success with more than 50 participants and the youngest only 10 years old. The participants were excited about the projects and asked many questions, resulting in a lot of discussion. The camp has successfully aroused the interest of the students to electronic engineering and everyone enjoyed the camp with lots of laugher.

Students constructing their circuits during the Electronic Winter Camp

QuestEDS

Interested in knowing why it's not possible to measure the built-in voltage of a PN junction using a voltmeter? Do you need to understand the best way to derive an expression for the average thermal velocity of an electron? Or are you curious about what quantum dots and wires are? The answers to these questions and more are available through the QuestEDS Question and Answer page.

To ask a question not already addressed on the Q&A page, visit www.ieee.org/go/questeds. Technical experts answering the questions posed represent academic, government and industry sectors.

Questions are grouped into five technical categories and two general ones. Technical categories cover subject areas like semiconductor and device physics, process technology, device characterization and quantum electronics. Subject areas addressed are anticipated to expand in the future. Two other categories address questions pertaining to educational activities and general inquiries about society membership. Within a two week time frame from when the question is asked, an answer is posted online. Incoming questions are handled by an editor-in-chief who ensures that they fall within the technical scope of EDS and that they are adequately answered.

For an archive of past questions and answers, visit http://eds.ieee.org/quest-eds/question-and-answer-page.html.

Question 012–07:
When doing device characterization, we often test the linear Vt and saturation Vt, I know the condition for saturation is Vs = Vb = 0,Vd = Vdd,sweep Vg, find the Vt with Gm Max method, but I want to confirm if the condition for linear Vt is Vd = 0.1V? And would you please help to explain why we need test those two item, what is their difference?

Answer 012–07:
In order to extract the linear Vth (Vt, lin) by linear extrapolation method at maximum Gm, the drain voltage must be as small as possible to maintain a uniform charge density in the inversion channel from the source to drain (that is similar to resistor with constant sheet resistance from source to drain) and negligible bulk depletion charge effect due to Vd. Therefore, a small value of Vds = 50 mV is preferred for advanced technologies, though Vds = 100 mV is typically used in practice.

The saturation Vth (Vt, sat) extracted by the quadratic extrapolation method is different from Vt, lin because of the drain induced barrier lowering (DIBL) effect at high Vd, especially, for short channel devices. As a result, the values of Vt, lin and Vt, sat are different. And, the magnitude of (Vt. lin – Vt, sat) is the measure of DIBL effect that contributes to the off-state leakage current in MOSFETs. Therefore, both Vt, lin and Vt, sat need to be measured to check the DIBL effect and robustness of device architecture.

Chapter News

MQ, DL and Conference Reports

2015 IEEE EDS Mini Colloquium in Bangkok, Thailand

By Ekachai Leelarasmee (Chulalongkorn University)

An EDS Mini-Colloquium was organized by the EDS/AP/MTT Chapter of IEEE Thailand Section, August 28, 2015, at Thailand Advanced Institute of Science and Technology (THAIST). The themed event, *"Sensors and Electrostatic Discharge,"* was co-organized by three parties, namely IEEE EDS, THAIST and Western Digital. Speakers were EDS Distinguished Lecturer, Juin J. Liou on *"ESD Protection of IC,"* *followed by* Pornchai Rakpongsiri, ESD Senior Manager of Western Digital Thailand on, *"GMR/TMR ESD Failure Characteristics and ESD Control in Hard Drive Manufacturing."* Two speakers from leading Thai Research Institutes also contributed topics on *"Graphene Printed Electronics"* and *"Highly Sensitive Gas Sensor based on electrolytically-exfoliated graphene-loaded flame-made SnO_2 hybrid composite Film."* The speakers were Dr. Adisorn *Tuantranont* of Thai Organic and Printed Electronics Innovation Center and Dr. Anurat Wisitsora, of the Nanoelectronics and MEMS Lab. of National Electronic and Computer Technology Center. THAIST also demonstrated its work on developing ISFET as a sensor during the lunch and coffee breaks. This event was attended by 40 participants from 11 universities.

Invited speakers and some of the attendees of the EDS Mini-colloquium at THAIST

A meeting between Prof. Juin J. Liou and Prof. WanlopSurakamponthorn of Thailand Advance Institute of Science and Technology

Demonstration of a sensor readout and processing system developed by Prof. ApisakWorapishet of Mahanakorn University of Technology

ED Poland Chapter Plans IEEE EDS Mini-Colloquium on GaN HEMT Technology

In 2016, Instytut Technologii Elektronowej (ITE), Poland (http://www.ite.waw.pl) celebrates 50th Anniversary of its activity. It was established in 1966 as a part of a Polish Academy of Sciences (PAS) in Warsaw. Its scientific activities were focused mainly on basic and applied research in the area of semiconductor electronics and physics. They were based on achievements of a Polish scientist Prof. J. Czochralski and on developments of the Department of Electronics of PAS led by Prof. J. Groszkowski, where in the early 1950s the first Polish germanium point- contact transistors were manufactured.

In 1970, ITE was transformed into an industrial institute and became a part of a Scientific and Production Centre of Semiconductors CEMI. Its objectives at the time were to develop new semiconductor devices and technologies, transfer them into mass production at a semiconductor factory and supervise their production. After leaving CEMI, ITE works as an independent R&D organization with main focus on scientific research and developing advanced semiconductor technologies for innovative products.

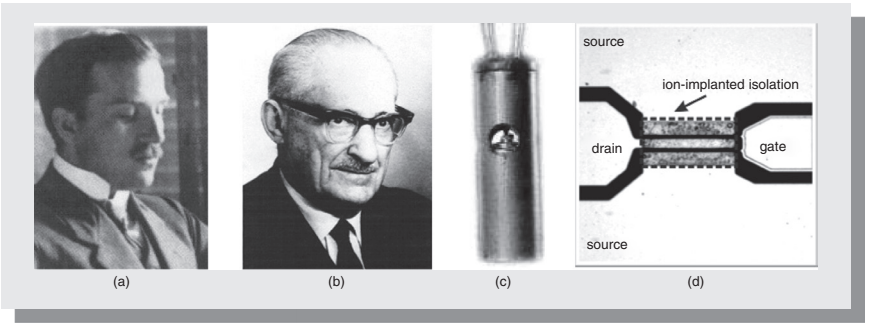


Fig. 1 a) Prof. Jan Czochralski (1885–1953), b) Prof. Janusz Groszkowski (1898–1984), c) first Polish germanium point-contact transistor encapsulated in a brass pipe (after: J.Pultorak, "60 years of polish transistors", Proc. MIXDES'2014, DOI: 10.1109/MIXDES.2014.6872144), d) 2-gate AlGaN/GaN HEMT manufactured within Pol-HEMT project

Currently one of important projects ongoing in ITE aims at developing a new type of microwave S-band HEMT transistor based on AlGaN/GaN structures grown on bulk semi-insulating GaN substrates. Pol-HEMT project (http://www.polhemt.ite.waw.pl/en/home.html) is in its final stage. In order to establish a platform for exchange of experience in the area of GaN HEMT technology, modeling and applications, to share Pol-HEMT team achievements with an international community, and to attract potential interest from other partners an IEEE EDS Distinguished Lecturer Mini-Colloquium on GaN HEMT technology is planned to be held in Lodz, Poland, June 22, 2016. It will be held before the MIXDES conference, organized by the Department of Microelectronics and Computer Science (DMCS), Lodz University of Technology. The 50th Anniversary of ITE and the 20th Anniversary of DMCS are a good opportunity for such an event.

Daniel Tomaszewski
Instytut Technologii Elektronowej
Warsaw, Poland
~ Editor, M. Orlikowski

IMPORTANT REMINDER to Chapter Members

- CHANGES TO CHAPTER OFFICERS NEED TO BE SUBMITTED TO BOTH IEEE AND EDS
- PLEASE REPORT CHANGES TO IEEE VIA THE VTOOLS.OFFICERREPORTING TOOL
- (ACCESS TO THE TOOL REQUIRES USE OF AN IEEE ACCOUNT)
- TO REPORT OFFICER CHANGES TO EDS, PLEASE SUBMIT A CHAPTER CHAIR UPDATE FORM: https://ieeeforms.wufoo.com/forms/pgu6n1i1ixepnu/

IEEE EDS Distinguished Lecture at ED NIT Calicut Student Chapter

by Akshay K. Sivadasan

A talk on the topic *"Engineering Evolution in Electronics and 50 years of Moore"* was conducted on January 19, 2016, at Electronics and Communication engineering department seminar hall, National Institute of Technology Calicut, as a part of the IEEE Electron Devices Society National Institute of Technology Calicut Student Branch. The talk was given by Dr. M. K. Radhakrishnan, Distinguished Lecturer, IEEE Electron Devices Society.

The event began at 02:00 p.m. Dr. Elizabeth Elias, Head of the Department, Dr. Lillykutty Jacob, Chairperson IEEE Malabar subsection, Dhanaraj student branch counselor, M. G. Jayakumoar counselor Electron Devices Society National Institute of Technology Calicut, Rama Komaragiri, advisor Electron Devices Society National Institute of Technology Calicut and many other faculty members were present for the occasion, as well as many PhD scholars, PG and UG students. The total number of members present was 60–70. The talk started at 02:20 p.m, with Dr. Radhakrishnan first presenting an overview of the Electron Devices Society and various activities associated with it, followed by his talk on evolution in the field of electronics engineering.

The talk covered the initial research that has happened in the field of electronics and various inventions in the device industry, which began an electronics era that we are now currently experiencing. From vacuum tubes to the present day ICs, Dr. Radhakrishnan explained many things, such as the interesting fabrication of ICs due to its microscopic internal structure and really complex working. With the statistical data of the growing electronics industry and miniaturization of devices, he explained Moore's law. It was an interactive session with the students asking questions related to important milestones in the electronics device industry. Also he mentioned some of the negative impacts of electronic appliances to the human race. Refreshments were distributed at the conclusion of his talk.

Following the DL, Dr. Radhakrishnan joined members of the executive committee of the student chapter and gave many suggestions for the newly formed group, discussing the various activities that can be conducted as part of the Electron Devices Society. With this meeting the event was concluded at 05:00 p.m.

Attendees with EDS Distinguished Lecturer, M.K. Radhakrishnan (front row, 5th from left), at NIT Calicut

USA, Canada & Latin America (Regions 1-6, 7 & 9)

The IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (IEEE S3S): Enabling Technologies for the IoT

—by Fred Allibert

The 2015 edition of the IEEE S3S took place in beautiful Rohnert Park, California (Sonoma Wine Country). But despite the gorgeous surroundings people remained busy listening to the numerous high-quality talks throughout the conference.

The conference opened with a plenary session featuring Gary Patton (CTO and head of R&D, GLOBALFOUNDRIES), Geoffrey Yeap (VP of Technology, Qualcomm) and Tsu-Jae King Liu (Professor, UC Berkeley), which encompassed discussion of FDSOI, power efficient computing, and novel low power devices.

While the talks and posters presented leading-edge developments in the 3 core technologies of the meeting (SOI, Subthreshold Microelectronics, and 3D integration), the synergy between them was also clear. In all sessions we heard about how these technologies can be used to improve Power, Performance, Area, and Cost (PPAC) for small, off-grid, inexpensive, wireless devices. This synergy makes so much sense that in 2016 the IoT will be official theme of the IEEE S3S Conference.

Below are a few technical illustrations of key features for the IoT technology:

- In his plenary presentation, Dr. Patton discussed the advantages of SOI based technologies, including FDSOI for wearables (as illustrated in the chart below) and RF SOI for Front End Modules.

Dry Creek Valley, by S. Athanasiou

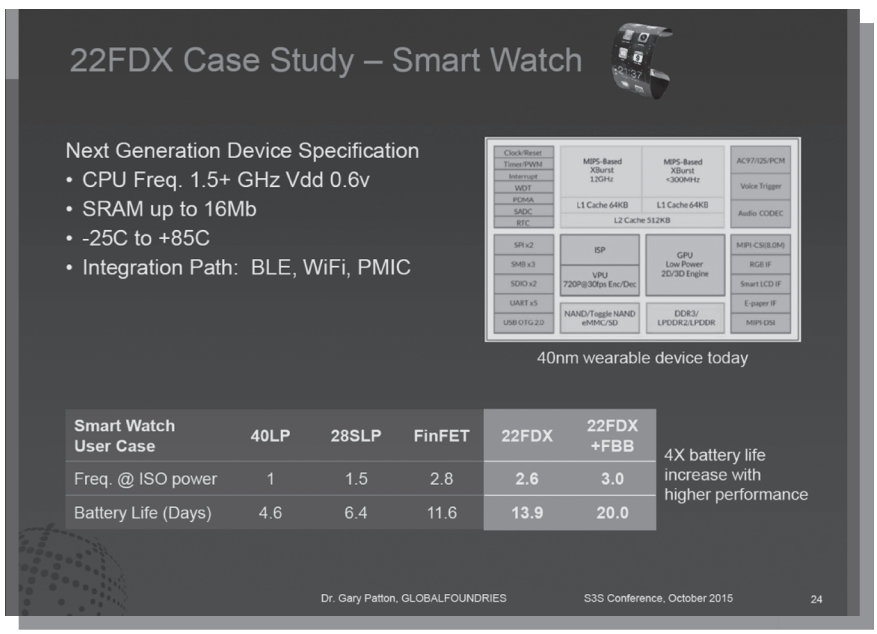


Chart from G. Patton's presentation

- Dr. Burghartz et al. presented a monolithic integration scheme to obtain Ultrathin Chips for Flexible Electronics and 3D ICs.
- Dr Rossi et al. showed a 4-core cluster capable of wide-voltage operating, from extreme energy efficiency (60 GOPS/W at 0.5 V) to high performance (1.8 GOPS at 1.2V).
- Several papers dealt with sensor technologies, a key component of IoT devices, such as the low voltage (0.2–0.5 V) 23 nW CMOS temperature tensor, presented by Kamakshi et al.

If you work in the field of IoT, then you will benefit from knowing more about its enabling technologies: SOI, Subthreshold Microelectronics, and 3D integration. We strongly encourage you to attend the 2016 IEEE S3S conference, and even more to contribute a paper!

2016 IEEE S3S Conference

Location: Hyatt Regency San Francisco Airport

Conference date: October 10–13, 2016

Paper submission deadline: May 18, 2016

Call for papers and more details at: s3sconference.org

~Adam Conway, Editor

ED South-Brazil Chapter University of Sao Paulo, Brazil

—by Joao Antonio Martino, Chapter Chair

The Laboratory of Integrated System (LSI) of Electronic System Department (PSI) of University of Sao Paulo (USP) and Electron Device South-Brazil Chapter organized the First Hands-on on Electrical Characterization of Advanced Transistors of Latin America at the University of Sao Paulo for educational and research applications.

The graduate and undergraduate students had an opportunity to study theoretically and experimentally the main transistors milestone starting with MOSFET and continuing with SOI MOSFET, FinFET and finally Tunnel-FET. After a short theoretical introduction of each device, the participants had a chance to extract experimentally the main electrical and physical characteristics in order to understand each devices behavior.

This hands-on on electrical characterization was held at the University of Sao Paulo on November 23–27, 2015, (40 hours) using also the devices fabricated at USP and the measurements rooms with the state-of-the-art equipment.

This course was free of charge for all Brazilian researches, teachers, graduate and undergraduate students, like design and devices people, which are interested in this subject. This first edition selected people from different parts of Brazil like Rio Grande do Norte, Minas Gerais, Sao Paulo, Santa Catarina and Rio Grande do Sul. This course will be given annually by the University of Sao Paulo. For additional information, contact Professor Joao Antonio Martino at martino@usp.br.

Electrical characterization room at University of Sao Paulo (USP) during the Hands-on on Electrical Characterization of Advanced Transistors

Sunday of the Branches 2015 IEEE Student Branches of Bahia Section Meeting

—by Filipe Campos Pereira, Chair of EDS Student Chapter at UNIVASF

The event took place at the Federal University of Sao Francisco Valley (UNIVASF), located in the state of Bahia, Brazil, from October 31*st* to November 1st. The meeting was attended by the IEEE President of Bahia Section and representatives of some of its student branches, local students, local business people, professors and lectures.

The course organizers, Joao Antonio Martino, Paula Ghedini Der Agopian and Ricardo Rangel from University of Sao Paulo and some of the students

Chapter booth (left to right), Filipe Campos, Jacobus Swart and Isnaldo Coelho

ED Univ Fed do Vale do Sao Francisco Student Branch Chapter presented in its booth the project that is being developed at local schools using the Snap Circuits kits provided by EDS. Jacobus W. Swart, SRC chair for IEEE Region 9 and EDS Distinguished Lecturer, attended the event for two days and presented on November 1st, the lecture: *"IEEE-EDS and Prospects of Semiconductor Engineering in Brazil."*

Altogether, more than 100 people attended the event. More information can be found on the event's official website (www.domingodosramos.com), or on its Facebook page (www.facebook.com/domingodosramos2015).

~ Joao Antonio Martino, Editor

Europe, Middle East & Africa (Region 8)

IEEE ED Poland Chapter

—by Krzysztof Górecki

On November 24, 2015, the chapter held a meeting at Poznań University of Technology, led by Professors Andrzej Napieralski and Andrzej Rybarczyk.

Professor Jerzy Nawrocki, the Dean of the Faculty of Computing of Poznań University of Technology, greeted the guests and gave a brief speech in which he evidenced the meaning of the relationship of investigations concerning electronics (especially microelectronics), with the development of information technology.

Three additional lectures were presented: *"Current-Mode ΣΔ Modulators and possible applications in implantable chips,"* presented by Dr. Paweł Śniatała; *"Challenges in embedded the image processing,"* Dr. Rafał Kapela; and *"Whether one can in Poland not develop microelectronics,"* by Prof. Piotr Grabiec.

Also, a talk was presented by a manufacturers' agent from Antmicro, on *"New technologies in built-in systems."*

All reports resulted in many questions from the interested participants, who presented their own comments on the subjects discussed.

The next meeting will be held during the MIXDES conference, in Łódź, June 23-25, 2016.

~ Mariusz Orlikowski, Editor

ED Dublin/PHO Ireland

—by Patrick McNally

Towards the end of last year, the joint chapter of the Dublin Electron Devices and the Ireland Photonics Societies had the honour of hosting a technical seminar by a renowned expert in the area of Atomic Layer Deposition. Professor David Cameron of Masaryk University, Brno, in the Czech Republic, delivered a seminar entitled *Roll-to-roll Atomic Layer Deposition: a future production technology for flexible optoelectronics* to an audience of more than forty people in the Stokes Building in Dublin City University. This seminar, which was held in November 2015, was also video linked to our colleagues in

Prof David Cameron (picture far left), delivering his technical seminar to an audience in Dublin City University with video linking to National University of Ireland (Galway) and the Tyndall National Institute (Cork)

the National University of Ireland, Galway and the Tyndall National Institute, Cork, bringing the overall audience to nearly sixty attendees.

Atomic layer deposition (ALD) is a chemical vapour deposition technology that enables the formation of ultrathin nanometre-scale films, layer by layer with very high degrees of thickness control, uniformity and conformity. Primary uses of the technology are currently in areas such as high-k gate dielectrics and silicon photovoltaic passivation. Prof. Cameron's talk covered the basic principles of ALD as well as its adaptation to roll-to-roll processing and some of the potential applications. In particular, he highlighted how his team at Masaryk University had recently developed the world's first commercial production-scale roll-to-roll ALD system in collaboration with Beneq Oy, a Finnish ALD equipment manufacturer.

~ Jonathan Terry, Editor

Asia & Pacific (Region 10)

ED Taipei

—by Steve Chung

The ED Taipei Chapter held three invited talks in the fourth quarter of 2015. The first invited speaker, Prof. Toshiro Hiramoto from University of Tokyo, gave a talk November 2nd, entitled, *"Future Prospects of Integrated Nanoelectronics – More Moore and Beyond CMOS."* In his presentation, the historical trend of "More Moore" in the past and the future trend predicted by ITRS are compared in order to look into the technological barriers that should be targeted. Then, the technology trend of "Beyond CMOS" devices is reviewed. Finally, a new concept of "Extended CMOS," in which emerging "Beyond CMOS" devices are merged into the CMOS platform to add new functionalities to VLSI, is proposed for future integrated nanoelectronics. This talk was quite well-attended by more than 60 students, professors/researchers.

The second and third talks were held on November 6, 2015. Dr. Simon Deleonibus, from Leti-CEA, France, gave the first talk, entitled *"More Moore and More than Moore Meeting for 3D Towards Zero Intrinsic Variability and Zero Power."* In the future, growing electronic markets require a drastic power consumption reduction, needing less energy greedy devices, interconnect, computing technologies, and architectures. He discussed three main themes along the road: (1) the scaling of CMOS, (2) Alternative Materials and Architectures Boosters for continued Nanoelectronics scaling, and (3) the discussion on "Will More and More Than Moore meet for 3D?" The third talk, was given by an invited speaker from National University of Singapore, Prof. Albert G.C. Liang. His talk entitled *"Device physics and modeling of low-power consumption devices."* In this talk, therefore, he introduced the current development on the FET-related devices and novel functional devices. Next, a general modeling procedure, self-consistently solving the Non-Equilibrium Green-Function transport formalism and the device electronic structure were presented. Finally, this model was employed to investigate the device physics/performance of conventional FETs, and tunneling FETs, Tunneling FET based on 2D materials. Both talks were attended by more than 40 students and professors/researchers.

The chapter is also co-organizing an international symposium called ISNE, the 5th International Symposium on Next-Generation Electronics, which is scheduled for May 4–5, 2016, at National Tsing Hua University, Hsinchu, Taiwan. The paper submission deadline was January 8, 2016. For more details, please visit the web site: http://www.isne2016.tw. Along with the conference, we encourage participants from around the world, and especially welcome those who are interested in having a business trip to a city where semiconductor manufacturing and IC design companies are located.

~ Mansun Chan, Editor

ED Kansai

—by Michinori Nishihara

The ED Kansai Chapter held a Technical Meeting on November 24, 2015 at

ED Taipei, Invited Talk: (left panel) November 2nd – Simon Deleonibus, Steve Chung (seminar chair), T. Hiramoto (speaker), P.W. Li (seat from left), (right panel) November 6th – Simon Deleonibus (speaker)

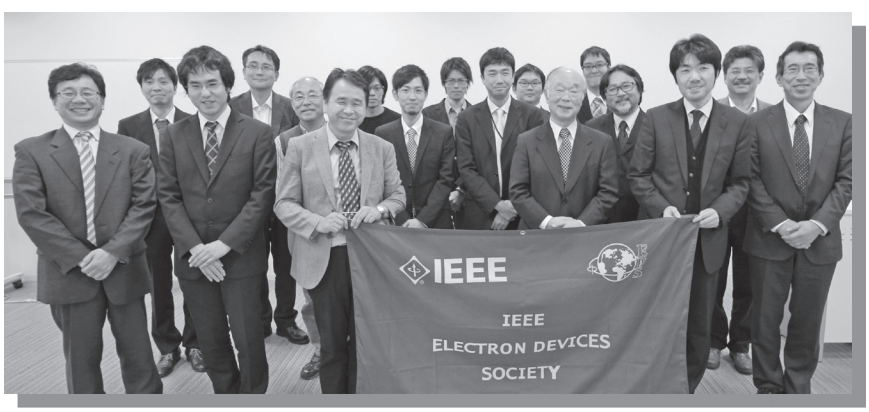
Prof. Hosoi

Prof. Nishimura

Prof. Fujita

Group Photo for Technical Meeting on Nov. 24

Dr. Tanaka



Group Photo for Kansai Colloquium

Osaka University, Osaka, Japan. Fourteen people attended to hear the two prestigious lecturers, Prof. Tadashi Nishimura and Prof. Takuji Hosoi, both from Osaka University.

Prof. Nishimura's lecture entitled, *"Introduction to Power Device."* explained the various needs of high efficiency power devices throughout our industries and emphasized the importance of basic power semiconductor technologies such as Si super junction, SiC, GaN etc.

Prof. Hosoi's lecture was titled, *"Control Technology of SiC MOS Interface."* According to Prof. Hosoi, SiC looks promising over other device technologies but there still are several issues to be solved for better performance and efficiency. He discussed origin of interface states and requirements for good oxidation modeling.

The chapter also hosted the 15th annual Kansai Colloquium Electron Devices Workshop on December 15, 2015, at OIT UMEKITA Knowledge Center, Osaka, Japan. The event attracted 27 participants and 11 excellent papers, with authors from the Kansai area, who also presented at the workshop. The papers were specially selected from major conferences such as IEDM or SSDM and technical papers on electron devices published during the past 12 months.

The program was divided into three sections as follows: (1) Sensor, Solar Cell, and Emerging Devices, (2) Power and Compound Semiconductor Devices, (3) CMOS Process, Device, and Circuit.

The Award Committee selected one paper from student presenters for the 15th IEEE EDS Kansai Chapter MSFK Award. The winner was Dr. Hajime Tanaka of Kyoto University for his paper titled, *"Phonon-limited Electron Mobility in Rectangular Cross-sectional Ge Nanowires."*

Prof. Dr. Asad Madni and the participants after the talk organized by the ED Malaysia Kuala Lumpur Chapter

Prof. Dr. Richard de La Rue delivering his talk at IMEN UKM

The Committee also selected one paper for the IEEE EDS Kansai Chapter of the Year Award. The winning paper was *"Mist Deposition Technology as a Green Route for Thin Film Growth"* by Prof. Shizuo Fujita of Kyoto University.

~ Kuniyuki Kakushima, Editor

ED Malaysia Kuala Lumpur Chapter

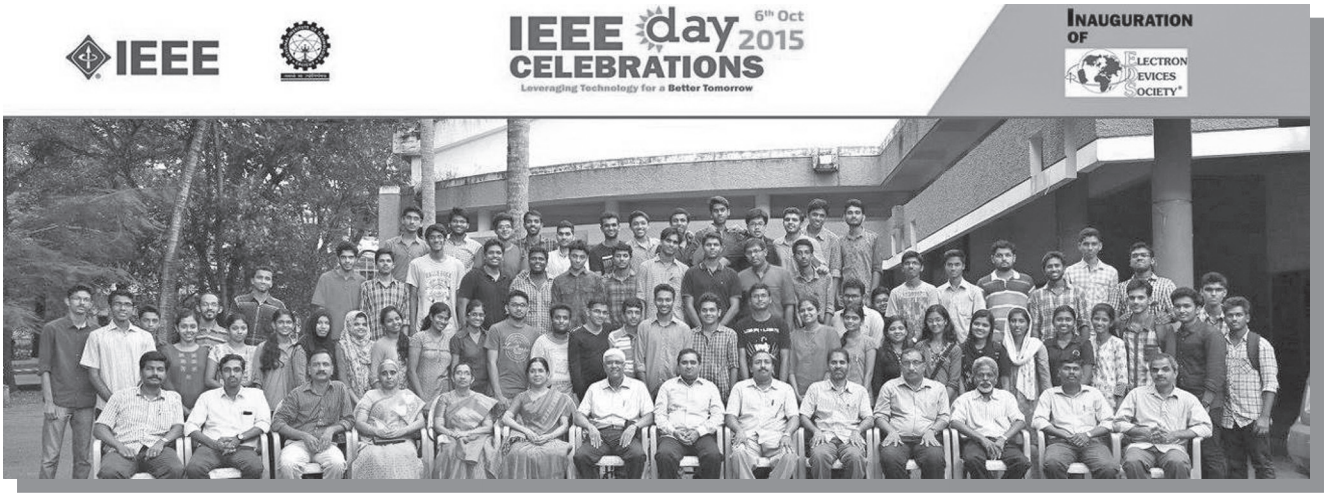
—by Badariah Bais & Zubaida Yusoff

Technical Talk by IEEE Fellow, Prof Asad Madni

The IEEE ED Malaysia Chapter organized two Technical Talks by IEEE Fellow, Prof. Dr. Asad Madni, President, Chief Operating Officer and CTO (Emeritus) of BEI Technologies Inc., Distinguished Adjunct Professor/Distinguished Scientist, Electrical Engineering Department, University of California, Los Angeles, USA, November 4, 2015, at IMEN, UKM. His talks on "IEEE Membership Elevation" and "Key Elements of a Business Plan for a Start-up Company" was attended by IMEN staff and postgraduates. In his talk, Prof.Asad explained about the steps and advantages of being an elevated IEEE Member. He also gave some tips on business start-ups based on his own personal experience.

Technical Seminar by IEEE Fellow, Prof. Richard de La Rue

On December 2, 2015, a technical seminar was held at IMEN, UKM. The



ED NIT Calicut Student Chapter inauguration on IEEE Day 2015

speaker was IEEE Fellow, Prof. Dr. Richard de La Rue from the University of Glasgow, Scotland. About 30 participants attended the talk, which was co-organized by the IEEE EDS Malaysia Chapter and IMEN, UKM. He gave two talks entitled, *"2D Materials"* and *"Nanophotonic Structures for Sensing."*

~P Susthitha Menon, Editor

ED NIT Calicut Student Chapter

—by Akshay K

The inauguration of the chapter was held on October 6, 2015, i.e. IEEE Day, in the presence of Dr. Sivaji Chakravorti, Director NIT Calicut and Chair Elect, IEEE India Council. Mr. Vinod K Jacob, Chairman IEEE NIT Calicut Student Branch read the code of ethics. A technical talk on *"Games People Play with Light"* was delivered by Dr. Subramaniam, Professor, NIT Calicut.

On November 27, 2015, the chapter organized an exam for second year students to motivate them to join EDS. The event was a grand success with more than 100 enthusiastic students coming forward to be a part of the event.

ED NIST Student Chapter

—by Prof. Rutuparna Panda

The Chapter organized a technical lecture series on *"Effective Algorithms for VLSI Circuit Optimization"* on December, 23, 2015, at National Institute of Science & Technology, Palur Hill, Berhampur, for the young faculties/ researchers to enhance their research activity. Prof. Rutuparna Panda explained the need of algorithms to optimize the circuits and different approaches to achieve it. His focus was on Cukoo Search (CS) and by considering a set of constants he demonstrated a new algorithm "Adaptive Cukoo Search (ACS)."

The chapter organized the 5th IEEE ED Mini-Colloquium on Emerging Electron Devices, held December, 19, 2015, at National Institute of Science and Technology, Palur Hills, Berhampur. The event was attended by more than 100 young faculties/ researchers to explore the recent technology and depth concepts on emerging devices. The technical session began with the opening talk on "*Bipolar Transistors*" by Prof. M Jagdeesh Kumar from IIT-Delhi. Prof. M. K. Radhakrishnan discussed "*Engineering Evolution in Electronics,*" to show the road map of the growth of technology for the last 50 years. He focused on the technology nodes and the complexity with scaling down the technology. Prof. G. N. Das delivered his talk on "*Modeling Issues with Graphene FET*" and Prof. Subur Kumar Sarkar gave a talk on "*Power Efficient CMOS Circuit.*"

Technical lecture series at NIT

5th MQ on Emerging Electron Devices, December, 19, 2015

ED/SSC Bangalore Chapter

—by Janakiraman V.

On June 30, 2015, the chapter organized a mini-colloquium which was inaugurated with Dr. Souvik Mahapatra talking about *"Macroscopic and Stochastic Aspects of Negative Bias Temperature Instability in Sub 20 nm devices and circuit."* This session was followed by Dr. Shanthi Pavan's presentation on *"Low Power Continuous-time Delta Sigma Converters,"* which covered all key aspects of Sigma Delta Analog and Digital Converters (ADC), from the very basics to advanced concepts. His talk highlighted techniques that are used to reduce power dissipation with interesting design examples of several state-of-the art ADCs.

ED/SSC Bangalore Chapter Mini-Colloquium Speakers

Talk on Open POWER by Dr. Anand Haridass

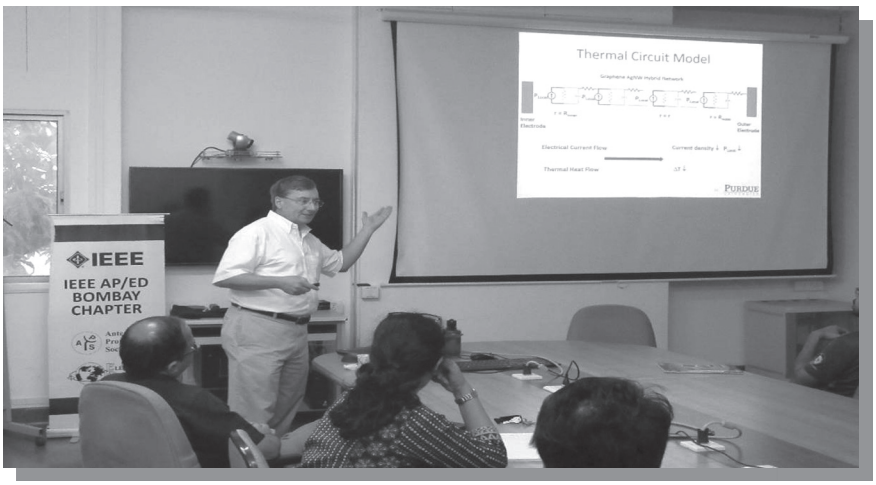
Dr. Jim Warnock interacting with the delegates

The Final session was by Dr. Ram Krishnamurthy on *"Energy efficient circuit technologies for the sub-14 nm era: challenges and opportunities."* He presented some of the prominent barriers to designing energy-efficient circuits in the sub-14nm CMOS technology regime and outlined new paradigm shifts necessary in next-generation multi-core microprocessors and systems-on-chip. He concluded his talk with specific chip design examples and case studies. The mini-colloquium was very well received by the audience including IBM researchers, students and professors from various Bangalore based colleges.

In October 2015, a technical talk was organized as part of a series called "India Chip Series" where Sankhya Labs spoke about their custom IP which caters to Software Defined Radio. The key idea was to provide Indian VLSI Companies a platform to project themselves. This creates good awareness among students who are willing to join.

In November 2015, second technical talk was held on the "*Performance Beyond Moore's Law – OpenPOWER,*" by Anand Haridass, Senior Technical Staff member, IBM Systems, where he covered Moore's law scaling, technology, processors, etc. He also spoke on the OpenPOWER consortium, which is an open development community, using the POWER architecture, dedicated to opening access to every part of the compute infrastructure.

In December 2015, Dr. James Warnock, Distinguished Engineer in IBM's Systems division, a member of the IBM Academy of Technology, and a Fellow of the IEEE, delivered his talk was on "*The 5 GHz IBM z13 Microprocessor and L4 Cache Chips,*" which



Prof. David Janes during his talk at the Bombay Chapter

focused on the circuit and physical aspects of these two chips, and also describing the high-frequency analysis techniques and methodology used to ensure a robust and reliable design.

ED/AP Bombay Chapter

—by V. Ramgopal Rao

The IEEE AP/ED Bombay Chapter during the last quarter, continued to host talks and distinguished lectures by well-known and distinguished fraternity belonging to academia from different parts of the world. Some of the notable speakers were Prof. Siddharth Rajan from Ohio State University, Dr. L. Kazmerski from the University of Colorado, Prof. John A. Rogers from the University of Illinois at Urbana-Champaign, USA, Prof. M. Jamal Deen, McMaster University, Hamilton, Canada; Prof. David Janes, Purdue University and Prof. Thomas Thundat, University of Alberta, Edmonton, Canada.

Prof. Siddharth Rajan in his talk titled, *"Next Generation Gallium Nitride Devices for Optoelectronic and Electronic Applications,"* focused on the benefits of next generation Gallium Nitride devices and the ways to overcome the limitations of present day GAN devices. Prof. John. A. Rogers in his distinguished seminar titled, *"Soft, Bioresorbable Optoelectronic Interfaces to the Brain,"* described the foundational concepts in materials science and assembly processes for developing technologies for optogenetics research and to develop bioresorbable, implantable intracranial sensors for treatment of traumatic brain injury. Prof. M. Jamal Deen, Distinguished University Professor in his talk entitled, *"Low-cost Sensors for Drinking Water Quality Monitoring,"* described his work on developing sensitive, small-size, flexible, easy-to-use, reliable and low-cost pH and chlorine sensing devices.

Prof. David Janes focused on electrical and electro-thermal transport in transparent conductors based on nanostructured networks and also on array-based electrochemical biosensors in his talk titled, *"Transparent Conductors and Array-Based Biosensors employing Nanomaterials."*

ED KGEC Student Chapter, Kalyani

—by Angsuman Sarkar

The IEEE ED Kalyani Government Engineering College Student Branch

Speakers and delegates at the inauguration of the 1-day seminar organized by the IEEE EDS KGEC Student Branch Chapter

Attendees of the 1-day seminar at BITM, Bolpur

Chapter and Department of ECE and EE of Bengal Institute of Technology and Management (BITM), Bolpur, jointly organized a 1-day Seminar on *"Advanced CMOS Devices,"* October 4, 2015, at BITM, Bolpur, Santiniketan, West Bengal, India. Dr. Angsuman Sarkar of Kalyani Government Engineering College, Kalyani, Nadia, delivered his talk on *"Advancement of CMOS devices"* which covered the basic concepts and evolution of CMOS technology.

Another 1-day Seminar on *"Retrospect & Prospects of Radio Science and Microelectronics,"* on October, 8, 2015, at Kalyani Government Engineering College, was jointly organized by the IEEE EDS KGEC SB Chapter in collaboration with the Department of ECE, Kalyani Government Engineering College. Two topics were presented: *"Radio Science in India: Some Early and Present Researches at Calcutta University,"* by Prof. Animesh Maitra, University of Calcutta, Kolkata; and *"Fundamentals of Short Channel Effects in MOSFET and their remedies,"* by Prof. Swapnadip De, Meghnad Saha Institute of Technology, Kolkata.

ED/SSC Bangladesh Chapter

—by Saeed-Uz-Zaman Khan

The IEEE ED/SSC Bangladesh Chapter, Ulkasemi and Department of EEE, BUET, jointly organized a technical workshop on *"Analog/Mixed-signal/RF design and Verification Methodologies"* on November 22, 2015, at the Department of EEE, BUET. The workshop was conducted by Dr. Henry Chang, Co-founder Designer's Guide Consulting, USA. The workshop presented a brief overview of the Semiconductor Industry. Topics ranged from Chip Design Flow to Digital and Analog Verification, Analog Modeling, Flow of Analog Modeling and Verification, Importance of Modeling, Chip Top Level Simulation etc. The workshop also covered languages used for Modeling and Verification and discussed current status of Mixed Signal Verification in the Industry.

Dr. Chang giving his talk in front of the audience at BUET

Photo session with Dr. Chang after the workshop

ED Meghnad Saha Institute of Technology Student Branch Chapter

—by Manash Chanda and Swapnadip De

An IEEE EDS Distinguished Lecture on *"Nanotechnology"* by Prof. C. K. Sarkar, ETCE Department of Jadavpur University, Chairman of IEEE Kolkata Section, was organized by the Department of ECE, Meghnad Saha Institute of Technology, IEEE ED Kolkata Chapter, IEEE ED Meghnad Saha Institute of Technology Student Branch Chapter and the IEEE HITK ED Student Branch Chapter on September 30, 2015.

Dr. Sarkar at HITK

ED Calcutta Chapter

—by Swapnadip De and Soumya Pandit

On October 29, 2015, the Department of ECE, Heritage Institute of Technology,

Attendees of the Lecture Session at HITK

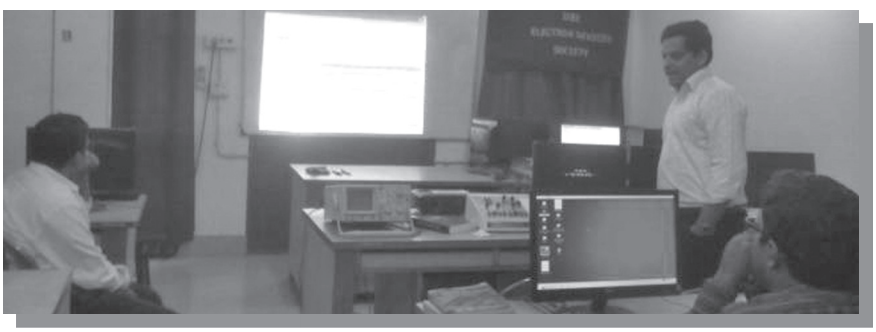
Dr. Hector J. De Los Santos of IntelliSense Corporation speaking at SIMIT in Shanghai, China

in collaboration with IEEE Kolkata Section, IEEE ED HITK Student Branch Chapter, IEEE ED Kolkata Chapter, IEEE ED Meghnad Saha Institute of Technology Student Branch Chapter, IEEE CU ED Student Branch Chapter and IEEE ED KGEC Student Branch Chapter, organized a Lecture Session *"Non-volatile Memory"* by Dr. Writam Banerjee, from Institute of Microelectronics of Chinese Academy of Science, Beijing, China.

ED University of Calcutta Student Branch Chapter

—by Soumya Pandit and Sarmista Sengupta

On October 28, 2015, the chapter jointly organized a technical seminar on *"Non-Volatile Memory"* with IEEE Kolkata Section, ED HIT-K, ED KGEC and ED-MSIT. Dr. Writam Banerjee, Institute of Microelectronics of Chinese Academy of Science delivered his lecture at the IC Design Laboratory, Institute of Radio Physics and Electronics, University of Calcutta. The seminar presented a comprehensive picture of state-of-the-art VLSI devices and its applications in memory technology. His talk gave an introduction on flash memory technology and its market capture, which was followed by the importance of RRAM in memory technology and concluded with an analogy between the RRAM technology and the human brain.



Seminar Lecture delivered by Dr. Writam Banerjee

EDS Chapter of Shanghai Institute of Microsystem and Information Technology Chinese Academy of Sciences (SIMIT)

—by Qisheng He

On November 17, 2015, Dr. Hector J. De Los Santos (IEEE Fellow, IEEE EDS Distinguished Lecturer), IntelliSense Corporation, visited the ED Chapter of Shanghai Institute of Microsystem and Information Technology Chinese Academy of Sciences (SIMIT). He delivered an EDS DL entitled, "*Study of the Mach-Zehnder Interferometric (MZI) Technique for MEMS/NEMS-Based Dielectric Resonator (DR) Tuning,*" which included the latest study of a broadband and high-Q tuning dielectric resonator. He presented the results on a theoretical study and an experimental verification of the intrinsic tuning properties of an MZI-DR-transmission line system, of the type employed in DR oscillators, in particular, dealing with the tuning range and quality factor.

ED Coimbatore Chapter

—by D. Nirmal

The Chapter organized a National level Workshop on Semiconductor Memories which was sponsored by ECE department of Karunya University on September 18, 2015, at Coimbatore. The first session was coordinated by Dr. N. M. Sivamangai of Karunya University Coimbatore, who gave an overview on the Design of Semiconductor Memories and Testing. The next lecture session by Dr. Veer Raghuvulu, from ARM Embedded Technologies, Bangalore, was given through Skype Video conferencing, explaining the industry perspective of memory design. Dr. Raghuvulu also gave a review on the challenges faced in designing as a result of downscale technologies and briefly explained the timing issues related to SRAM.

An afternoon session with hands-on training using cadence tools, was to give the idea on designing of Semiconductor memories. The last session

Participants of the Semiconductor Memory Workshop

At the Science to Engineering – Electronics Kit Demo

was a panel discussion on *"The future of Semiconductor memories – technology driven or application driven which will dominate the new era of computing."*

Around 40 attendees consisting of faculty members and graduate students from various institutions participated, out of which 26 were women.

A "Science to Engineering – Electronics Kit Demo" program was organized by the IEEE Student Branch, Cape Institute of Technology, Levengipuram, in association with the Electron Devices Society, Coimbatore Chapter on September 9th and 12th, 2015, at Govt. High School, Thirupathisaram. The vision of this program is to create awareness about Electronics to the school students. More than 30 students of high school classes attended both programs. The training to the students was given with the kit provided by the Electron Devices Society (EDS), Coimbatore Chapter. Some basic electronic component presentations were given and also an explanation on the importance of electronics which is creating an impact in this technical world.

ED Delhi Chapter

—by Manoj Saxena

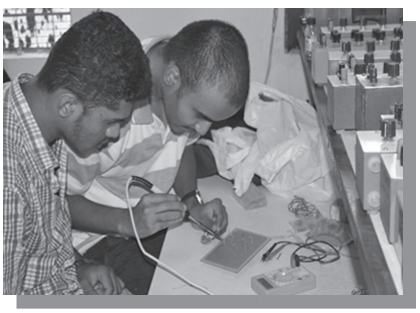
The chapter organized an Interactive session On Career Opportunities in Modern India by Mr. Ramesh Kaza, Senior Vice President, Bank of America and Treasurer on October, 6, 2015, at Department of Electronic Science, University of Delhi South Campus, New Delhi.

The Department of ECE, Maharaja Agrasen institute of Technology, Delhi, organized a seminar on October 16, 2015, on Advanced Electronic Devices and Circuits for Low and High Frequency Applications. The seminar was sponsored by the Society for Micro Electronics & VLSI and the IEEE ED Delhi Chapter. The inaugural talk was delivered by Prof. M. Hashmi, IIIT Delhi, who discussed the importance of Waveform Engineering and its Applications, followed by Prof. D. R. Bhaskar, JMI, Delhi, who delivered his lecture on Analog Circuit Design Using Current Conveyors. D. S. Rawal, Scientist-F, SSPL, Delhi, discussed GaN HEMT Device Technology for Microwave Applications, Dr. A T Nimal, Scientist-F, SSPL, Delhi, spoke on SAW Signal Processing Devices, Sensors and E-NOSE, which was followed by Prof. (Dr.) Asoke De, Director NIT, Patna, who talked about Patch Antenna and its Applications.

On October 28, 2015, the chapter and The National Academy of Sciences, India – Delhi Chapter jointly organized a One Day Symposium to Celebrate the International Year of Light at Deen Dayal Upadhyaya College, University of Delhi. Professor Ajoy Ghatak, (Formerly Professor of Physics @ IIT Delhi) delivered his keynote talk on *"The Year of Light & Fiber Optics."* The talk gave a very brief history on the development of the optical fiber and a few fiber based devices. Professor K. Thyagarajan, Department of Physics, IIT Delhi, gave a talk on *"Quantum Photonics."* He discussed the concept of Entangled photon pairs having application in quantum key distribution, quantum imaging, quantum metrology, quantum teleportation, etc. Mr. Mohammad Yasir Abbas, Senior Application Engineer-Industrial Metrology Business Unit, Nikon India, discussed Fundamental digital microscopy combined with image processing Techniques having a key role to play in ultimate product delivery and its ergonomic adaptability by the target consumer. Ten student groups made technical presentations like Modeling Optical waveguides using VHDL, Development of Mercury Cadmium Telluride Epitaxial Layers using Molecular Beam Epitaxy for Infrared Detector Applications, Homemade low-cost Spectrometer etc.

The chapter also organized an IEEE Distinguished Lecture on *"Outlook and Challenges of Electrostatic Discharge (ESD) Protection of Modern and Future Integrated Circuits,"* by Prof. Juin J. Liou, Pegasus

Mr. Mohammad Yasir Abbas, Senior Application Engineer, Nikon India Private Limited, demonstrates a digitally integrated high accuracy Optical Data Acquisition system



Students at Vacation Project Mania (VPM) 6.0

Professors K. Thyagarajan and Ajoy Ghatak inspecting demonstrative student projects

Distinguished Professor and Lockheed Martin St. Laurent Professor of Engineering, University of Central Florida, Orlando, Florida, USA on December, 14, 2015, at University of Delhi South Campus, New Delhi.

ED Sri Jayachamarajendra College of Engineering Student Branch Chapter

—by C. R. Natraj and S. B. Rudraswamy

The chapter organized Vacation Project Mania (VPM) 6.0 from June 18th to July 1st, wherein the students were taught about soldering techniques.

The second phase of VPM was dedicated to microcontrollers, during which students were taught the MSP430 development board, developed by TEXAS Instruments. The fourth and the final round of VPM (VPM 6.0.4) was the project submission competition. A total of 44 people participated in this competition, among which 26 were IEEE members. A total of 18 teams were present and 11 projects were presented in the competition. The chapter also conducted workshop using Snap Circuits kits where first and second year students were given hands-on sessions of basic electrical and electronic circuit components. A total of 73 students attended the workshop among which 48 were IEEE member and 25 were non-IEEE members.

On August, 20, 2015, the chapter organized a training workshop wherein 79 people attended the session, out of which 51 were IEEE members. Basic concepts of resistor, capacitor, inductor, diode and their various types were taught and later the concept of current, voltage and power rating of the components was also discussed.

On September 10, 2015, another practical electronics session was conducted and the focus was on building small circuits like an LED torch light, a power supply using transformers, diodes and regulators.

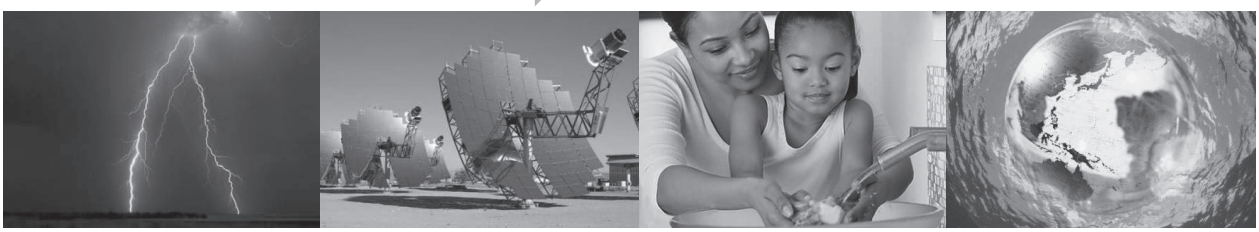
During September 25-27, 2015, the chapter organized a Soldering and Etching Workshop to enhance the practical skills of students in soldering and etching. A total of 132 students attended this workshop.

~ Manoj Saxena, Editor

SIGHT Project Guidelines

IEEE SIGHT

Special Interest Group on Humanitarian Technology



Special Interest Group on Humanitarian Technology

IEEE Special Interest Group on Humanitarian Technology (SIGHT) is an initiative that focuses on creating opportunities for members to devote time and talents to humanitarian work consistent with IEEE's Constitution to "bring the benefits of technology to the entire world."

About SIGHT

The types of projects targeted by SIGHT groups are those that lead to significant impact on eradicating world poverty through growing sustainable benefits in technology-poor areas. The desired result is not to exploit the Base of the Pyramid (BOP) with foreign based and owned enterprises, but to empower people in the BOP to become full participants by helping plant and grow technology enterprises in communities which then become fully self-sustaining and increasingly prosperous. Since IEEE members are critical in creating the major economic drivers of the developed world, they are therefore critical to teaching others in the underdeveloped world how to become full participants, not just as minimum wage workers but as technician, engineers, managers and entrepreneurs in BOP areas globally.

IEEE members come together to form SIGHT groups around the world, promoting and creating a range of projects pointing to this over-arching goal. A number of projects are already underway, some quite large and ambitious, around which new SIGHT groups can organize either as technical development or project support groups, or to expand the reach with new capabilities or synergies with other partners. A few of the major needs that SIGHT groups aim to address are affordable reliable electricity, lighting and power tools, communication and entertainment, clean water, cooling and refrigeration, and remote learning centers for technical education and adult education.

What do SIGHT groups do?

Groups that are involved in the following types of activities can apply to form a SIGHT and gain support from IEEE.

Education, Networking and Preparatory Projects

Various types of activities are of interest for SIGHT development. These initial activities can involve educational goals, such as programs that aim to help local schools in the underserved regions and/or have a good educational value for the participating school's students; they can also involve networking goals, such as initiatives that focus on the organization of conferences or networking workshops to further humanitarian efforts around the world. Besides education and networking, there are SIGHT initiatives that involve other preparatory projects that focus on inspiration, encouragement, and orientation. SIGHT supports projects that orient engineers towards social innovation, entrepreneurship, or humanitarian activities; that awaken interest and create passion for humanitarian work through learning; and that identify opportunities that will result in practical and useful projects.

Major Projects

Major SIGHT projects aims are as follows:

- Support sustainable technology business initiatives seeking to have a measureable impact in alleviating global poverty of energy, health care, sanitation, interconnectivity and other technology-dependent solutions among the BOP's 1.4 billion people;
- Develop open source technology solutions designed to drive down the cost of access to full benefits in technology areas, while avoiding intellectual property restrictions that keep costs artificially high and deny affordable access;

Questions? Contact h.s.brown@ieee.org or sbabu@ieee.org • +1 732 562 5355 • www.ieeehtag.net

- Leverage affordable core technologies like electricity, communications and interconnectivity to bring affordable secondary benefits to the BOP especially education at all levels in rural poor societies; and
- Empower BOP local entrepreneurs and citizens to develop sustainable, scalable profit-making businesses in-country to grow community prosperity exponentially by reinvesting all profits in growth to scale and in improving community infrastructure such as roads, sanitation, health care and education.

Long Range Goals of SIGHT based on IDE

A movement called IDE90 is proposed as a framework for the long range goals of SIGHT, emanating to large degree out of the pioneering work of Paul Polak, a practitioner for three decades in sustainable development and author of "Out of Poverty." The company he founded called International Development Enterprises (iDE) focused on affordable low-tech solutions for poor farmers such as treadle pumps and drip irrigation. Here, IDE is an acronym for **Incubate**, **Demonstrate**, **Educate** - three nested practices that sustain socially equitable, economically prosperous, and environmentally sound community enterprise. Nobel laureate Amartya Sen expands on this triple bottom line of sustainability. He argues that development done well generates human freedom and agency to build community capacity and choice, and thus empowerment[1].

Incubate.
This is the phase of initial ideas for both technical project and the companion business development model. Ideas formulate concepts which are investigated and criticized over the first year. It is relatively simple to develop a technical prototype on this time scale but the marketability of the proposal has to be tested both on paper and with potential business partners, base of pyramid (BOP) customers and communities undergoing throes of change.

Demonstrate.
As the name implies, if the project "gets legs" in the incubate phase a prototype for a pilot demonstration is justified. For this phase IEEE proposes to extend some funding for development and deployment of prototypes in sufficient quantities to test the business model and demonstrate sustainable operation with social equity and environmental sounds over a pilot test period of 1-2 years.

Educate.
Unless there is a local Education component strongly tied to this community enterprise, any genuine sustainability is jeopardized. Education here - both formal and non-formal - gives a community access to the world, establishes broad-based literacy and identity, teaches technology, business, health and sustainability, and creates a critically thinking community. Through Education linked to Incubation and Demonstration, a community learns to collaborate and take entrepreneurial strides to educate all members, not just the privileged few.

[1] Amartya Sen was awarded the Nobel Prize in Economics, 1998 for seminal work on welfare economics.

Prerequisites to form a SIGHT

Six or more IEEE members in good standing and passionate in humanitarian technology activities centered on one or more above interest areas. Three or more of these signatories must be members from two different chapters.

The prospective SIGHT will need to have an affiliation with an IEEE Section or Student Branch. The chair of the Section or the Student Branch Counselor will need to approve the formation.

Students are encouraged to form SIGHTs. The chair must, however, be a professional member, ideally the Student Branch Counselor.

The prospective SIGHT will need to submit an application (petition) requesting for the formation of a SIGHT.

For more information and application

Go to **http://bit.ly/11kykcY** for more information on IEEE SIGHT and how to form a SIGHT group.

Application:

If you are interested in forming a SIGHT group, you may apply by completing the petition (on IEEE SIGHT website above) and submitting the application materials to the SIGHT Steering Committee for review via:

Holly Schneider Brown
E-mail: h.s.brown@ieee.org (preferred method)
Fax: +1 732 463 3657

Mail: SIGHT Steering Committee
445 Hoes Lane
Piscataway, NJ 08854-4141
USA

ATTENTION EDS CHAPTERS:
EDS Chapters who wish to apply to form a SIGHT group must indicate the IEEE Electron Devices Society as their Operating Unit.

IEEE SIGHT
Special Interest Group on Humanitarian Technology

EDS MEETINGS CALENDAR

THE COMPLETE EDS CALENDAR CAN BE FOUND AT OUR WEB SITE: HTTP://EDS.IEEE.ORG. PLEASE VISIT.

2016 IEEE International Reliability Physics Symposium (IRPS)	17 - 21 Apr 2016	Pasadena Convention Center 300 East Green Street Pasadena, CA, USA
2016 IEEE International Vacuum Electronics Conference (IVEC)	19 - 21 Apr 2016	Monterey Marriott 350 Calle Principal Monterey, CA, USA
2016 International Symposium on VLSI Design, Automation and Test (VLSI-DAT)	25 - 27 Apr 2016	Ambassador Hotel Hsinchu 188 Chung Hwa Road, Section 2, Hsinchu, Taiwan Taiwan
2016 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA)	25 - 27 Apr 2016	Ambassador Hotel Hsinchu 188 Chung Hwa Road, Section 2, Hsinchu, Taiwan Taiwan
2016 5th International Symposium on Next-Generation Electronics (ISNE)	4 - 6 May 2016	National Tsing Hua University Hsinchu, Taiwan
2016 16th International Workshop on Junction Technology (IWJT)	9 - 10 May 2016	FuXuan Hotel at Fudan University 400 Guoding Road Shanghai, China
2016 International Siberian Conference on Control and Communications (SIBCON)	12 - 14 May 2016	Ilya A. Ivanov MIEM HSE 34 Tallinskaya Str. Moscow, Russia
2016 IEEE International Memory Workshop (IMW)	15 - 18 May 2016	Paris Marriott Rive Gauche Hotel & Conference Center 7 Boulevard Saint Jacques Paris, France
2016 IEEE International Interconnect Technology Conference / Advanced Metallization Conference (IITC/AMC)	23 - 26 May 2016	DoubleTree Hotel 2050 Gateway Place San Jose, CA, USA
2016 IEEE 43rd Photovoltaic Specialists Conference (PVSC)	5 - 10 Jun 2016	Oregon Convention Center 77 NE Martin Luther King Jr. Blvd. Portland, OR, USA

2016 28th International Symposium on Power Semiconductor Devices and IC's (ISPSD)	12 - 16 Jun 2016	Zofin Palace Slovanský ostrov 226 Prague, Czech Republic
2016 IEEE Silicon Nanoelectronics Workshop (SNW)	12 - 13 Jun 2016	Hilton Hawaiian Village 2005 Kalia Road Honolulu, HI, USA
2016 IEEE Symposium on VLSI Technology	14 - 16 Jun 2016	Hilton Hawaiian Village 2005 Kalia Road Honolulu, HI, USA
2016 23rd International Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD)	6 - 8 Jul 2016	Ryukoku University Avanti Kyoto Hall 31 Nishi Sanno-cho, Higashi Kujo, Minami-Ku, Kyoto, Japan
2016 Lester Eastman Conference (LEC) Abstract submission deadline: 29 Apr 2016 Full Paper Submission deadline: 02 Sep 2016 Final submission deadline: 02 Sep 2016 Notification of acceptance date: 10 Jun 2016	2 - 4 Aug 2016	Dept. of ECE 19 Memorial Drive West Lehigh University Bethlehem , PA, USA
2016 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC) Full Paper Submission deadline: 01 Apr 2016 Notification of acceptance date: 01 Jun 2016	3 - 5 Aug 2016	The University of Hong Kong Hong Kong
2016 IEEE Bipolar/BiCMOS Circuits and Technology Meeting - BCTM Abstract submission deadline: 15 Apr 2016 Final submission deadline: 15 Jul 2016 Notification of acceptance date: 17 Jun 2016	25 - 27 Sep 2016	Hyatt Regency New Brunswick 2 Albany Street New Brunswick, NJ, USA
2016 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)	10 - 13 Oct 2016	Hyatt Regency San Francisco 1333 Bayshore Highway Burlingame, CA, USA
2016 International Semiconductor Conference (CAS) Full Paper Submission deadline: 28 May 2016 Notification of acceptance date: 19 Jul 2016	10 - 12 Oct 2016	Rina Sinaia Hotel 8, Carol I str Sinaia, Romania
2016 16th Non-Volatile Memory Technology Symposium (NVMTS) Abstract submission deadline: 13 Jun 2016 Final submission deadline: 12 Sep 2016 Notification of acceptance date: 05 Jul 2016	17 - 19 Oct 2016	Carnegie Mellon University 5000 Forbes Ave Pittsburgh, PA, USA

Invited Speaker

Dr. Kylie Catchpole
Australian National University

Dr. Catchpole will share her research and experience in the field of photovoltaics through a 35 minute presentation followed by a Q&A session. The event is open and free of cost to PVSC attendees. Lunch will be provided.

Time and Location: Thursday June 9th, from 12pm to 1:30pm, Ballroom 201

Dr. Kylie Catchpole is Associate Professor at the Centre for Sustainable Energy Systems in the Research School of Engineering at the Australian National University. Dr. Catchpole's research focuses on using new materials and nanotechnology to improve solar cells. Her work on plasmonic solar cells was named as one of the top 10 emerging technologies in 2010 by MIT Technology Review, and in 2013 she was awarded a Future Fellowship from the Australian Research Council. In 2015 she was awarded the John Booker Medal for Engineering Science from the Australian Academy of Science. She has over 90 publications and her work has also been featured in the news sections of Science magazine and The Economist.

Dr. Catchpole graduated with a BSc in physics from the Australian National University, winning a university medal. She continued on to complete her PhD at Australia National University (ANU) focusing on thin crystalline solar cells. Her interest in nanophotonics and light trapping started during her postdoctoral fellowship at the University of new South Wales. She spent a year at the Fundamental Research of Matter (FOM) Institute AMOLF in Amsterdam before returning to ANU in 2008.

SIGN UP TO ATTEND

Attendance is limited, so if you would like to attend this event you must sign up at:
http://www.ieee-pvsc.org/PVSC43/events-women-in-pv.php

Tribute to Andy Grove

Passing of Silicon Valley leader, Intel's Andy Grove is felt across the IEEE Electron Devices Society.

Andrew S. Grove, Intel's legendary figure, former CEO and the first person hired by Intel founders Gordon Moore and Robert Noyce, passed away on March 21, 2016 at the age of 79. He was one of the giants of the semiconductor industry who helped to bring about the Digital Computer age.

Grove was a businessman, engineer, author, and a technology pioneer in the Semiconductor industry. He was one of the most influential figures in technology and business, writing best-selling books and widely cited articles and speaking out on an array of prominent public issues. He was Time's 1997 *Man of the Year* who was known for his innovative approach to corporate strategy and leadership that continue to influence prominent thinkers and companies around the world. He inspired generations of technologists, entrepreneurs, and business leaders.

Grove was both an astute engineer and a careful student of business management. To the *Electron Devices* community, his book, *Physics and Technology of Semiconductor Devices*, is one of the pioneering publications in microelectronics device and process engineering. And, his books, *High Output Management* and *Only the Paranoid Survive,* remain as some of the most highly regarded management books.

Salute to Andy.

Samar Saha
IEEE EDS President

EDS Vision and Mission Statements

Vision Statement
Promoting excellence in the field of electron devices for the benefit of humanity

Mission Statement
To foster professional growth of its members by satisfying their needs for easy access to and exchange of technical information, publishing, education, and technical recognition and enhancing public visibility in the field of Electron Devices.

Field of Interest
The field of interest for EDS is all aspects of engineering, physics, theory, experiment and simulation of electron and ion devices involving insulators, metals, organic materials, plasmas, semiconductors, quantum-effect materials, vacuum, and emerging materials. Specific applications of these devices include bioelectronics, biomedical, computation, communications, displays, electro and micro mechanics, imaging, micro actuators, optical, photovoltaics, power, sensors and signal processing.

The society is concerned with research, development, design and manufacture related to the materials, processing, technology, and applications of such devices, and scientific, technical, educational and other activities that contribute to the advancement of this field.