IEEE
ELECTRON DEVICES SOCIETY
Newsletter

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Technical Briefs

Trends in Device Research – IEDM 2015 Highlights

Advanced research trends in devices and their application are always reported at IEDM annually. Scientists and technologists at all levels from industry as well as academia always assemble at IEDM and sharpen their ears to hear the new results and innovations from laboratories around the world. The IEEE EDS Newsletter captures some of the key presentations at IEDM 2015 and is summarized here. These include novel devices using both silicon and hetero structures for various applications including sensing, imaging and Internet of Things (IoT). Full texts of the IEDM papers are available at the IEDM Technical Digest in IEEEXplore (ieeexplore.ieee.org/)

Difficulty seeing nanoscale transistor features? Well, a Penn State researcher has said goodbye to microscopes and hello to atom probe tomography. Tunneling field-effect transistors (TFETs) are promising for ultra-low-power applications, but improvements in their performance and reliability are needed. Critical to TFET performance when they are made from combinations of III–V materials is the need for abrupt and uniform interfaces among the dissimilar materials. Variability at these interfaces, or heterojunctions, reduces device performance and it is difficult to characterize heterojunctions with precision in nanometer-scale devices, but a Penn State team used atom probe tomography and time-of-flight spectroscopy to do so. First they cooled TFET samples to 50° Kelvin. Then, they rapidly heated the heterojunction under study with laser pulses to evaporate layers of atoms from it, one layer at a time. They captured the atoms from each layer in an electric field, and then performed spectroscopic analysis to identify the individual atoms, which constituted each layer. From all this data they built a 3D map of the heterojunction, with a resolution of 2.4 nm. Then, they rested. The study was reported in Paper 14.2, *Tunnel Junction Abruptness, Source Random Dopant Fluctuation and PBTI Induced*

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Your Comments Solicited

Your comments are most welcome. Please write directly to the Editor-in-Chief of the Newsletter at radhakrishnan@ieee.org

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Newsletter Deadlines

Issue	Due Date
January	October 1st
April	January 1st
July	April 1st
October	July 1st

The EDS Newsletter archive can be found on the Society web site at http://eds.ieee.org/eds-newsletters.html. The archive contains issues from July 1994 to the present.

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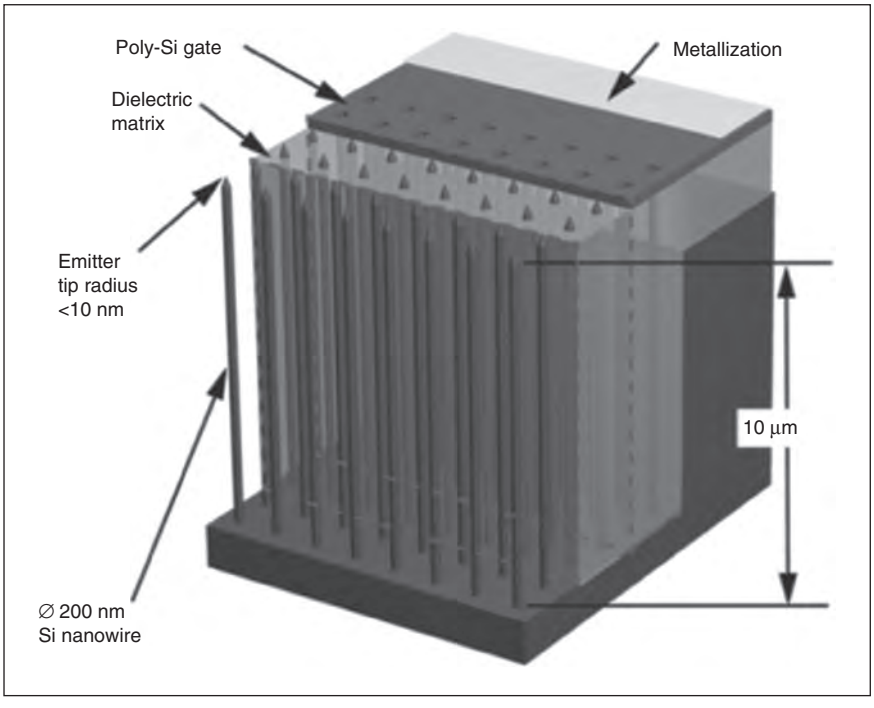
Variability Analysis of GaAs0.4Sb0.6/In0.65Ga0.35As Heterojunction Tunnel FETs; R. Pandey et al, Pennsylvania State University.

Vacuum tubes are making a comeback but in a very tiny way. Tiny electron guns (or nanoscale cold cathodes) were built from arrays of nanowire field emitters (tip diameters as low as 6 nm) that can be integrated on silicon. This means that good times are back since vacuum electronics were synonymous with high power and efficiency but now they are available without compromising the benefits of solid state (i.e. high gain and low noise). The research team from MIT demonstrated emitter arrays as large as 1000 × 1000 (Paper 33.1, *High Performance and Reliable Silicon Field Emission Arrays Enabled by Silicon Nanowire Current Limiters;* Stephen Guerrera et al, MIT).

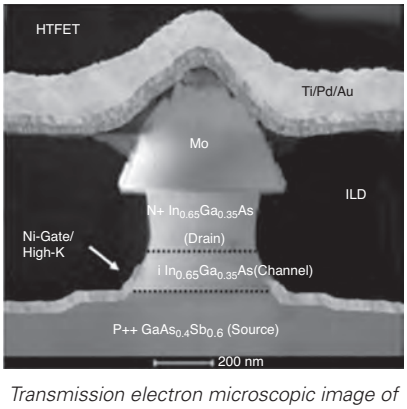
The study demonstrated a current density of >100 A/cm², more than a hundredfold greater than any other field-emission cathode operated in continuous wave mode. The devices also exhibited long lifetimes and low-voltage operation. So, new strides in technology can be taken into making miniature RF amplifiers and smaller sources of terahertz, infrared and X-ray radiation.

Mind-blowing technology also finally debuted at IEDM 2015. Optogeneticsis the study of neurons using visible light to stimulate their constituent proteins. The neural cells aren't damaged by optical stimulation, as they can be when electrically stimulated.

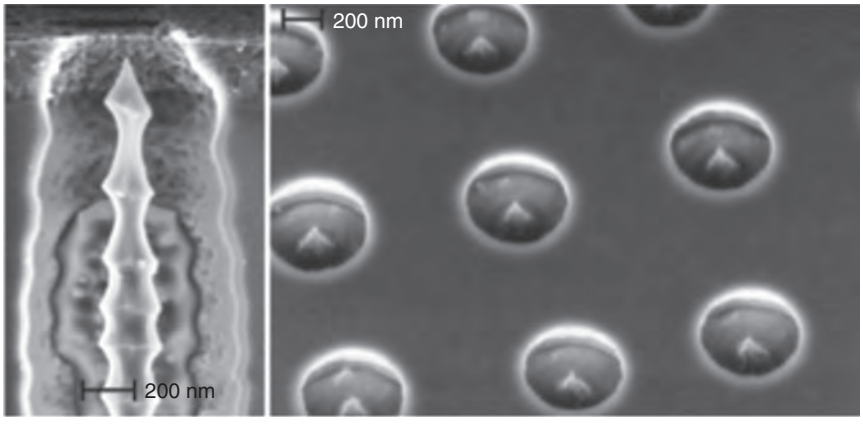
A team led by IMEC proposed an implantable neural probe with the highest reported density of optrodes (light emitters) and electrodes (to record the responses of the neurons



Schematic of the device structure (Ref: S Guerrera, et al., IEDM 2015 paper 33.1)



Transmission electron microscopic image of the cross-section of a fabricated heterojunction TFET with a HfO_2-ZrO_2 bilayer gate dielectric.
(Ref: R. Pandey, et al., IEDM 2015, paper 14.2)



SEM cross-sectional image of silicon nanowire current limiter with gate oxide removed (left), and emitters with 1 um spacing and gate aperture of 350 nm.
(Ref: S Guerrera, et al., IEDM 2015 paper 33.1)

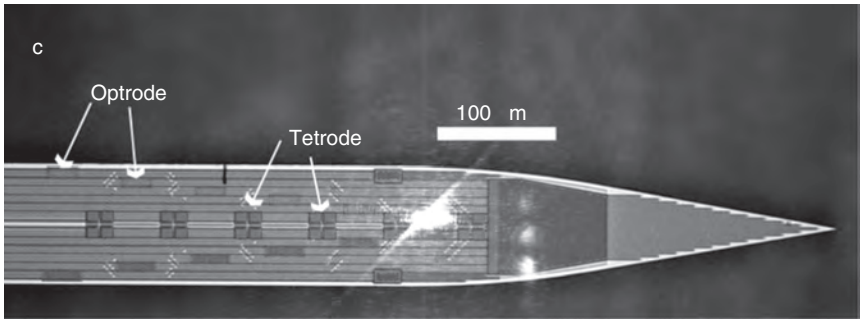
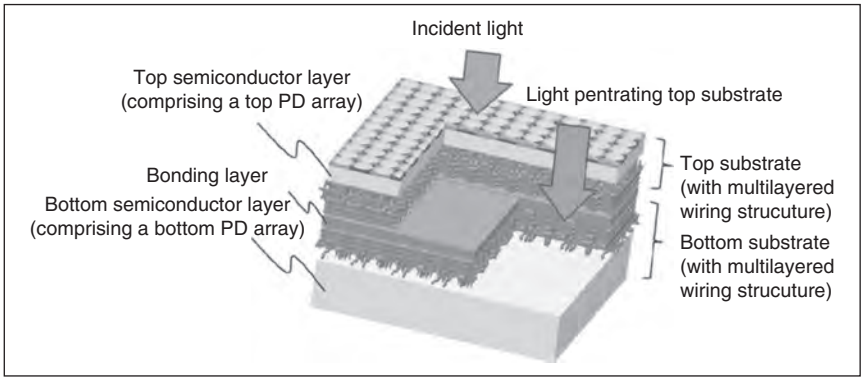


Image of the high-density multi-optrode-electrode probe with a light output activated (Ref: L Hoffman, et al., IEDM 2015, paper 29.5)

once they are stimulated). (Paper 29.5, *High Density Optrode-Electrode Neural Probe Using SixNy Photonics for In Vivo Optogenetics;* Luis Hoffman et al, Imec/KU Leuven). Higher density leads to better spatial resolution and also enables smaller probes that are less likely to damage tissue. To build the probe, the researchers integrated two different CMOS processes (silicon nitride photonics and TiN electrodes). They packaged the circuitry, implanted it in a mouse brain (oh.. it is not yet in human) and successfully demonstrated that it could both drive and record neural activity.

Remember when cameras went from plain black and white images to color? Well, now imagine cameras that can capture color and near-infrared (NIR) light. Medical diagnostics in particular, need the ability to capture all of these wavelengths with one compact device, which would make it easier and less time-consuming to examine different parts of the body. Clinicians would like these cameras to identify and pinpoint pathological lesions. The technical challenge is trying to detect color and NIR on the same chip because the optimizations are orthogonal. At IEDM 2015 in the Displays and Imaging track, researchers at Olympus demonstrated 3D wafer-stacking technology to integrate two separate CMOS imagers into one device, each optimized for either RGB or NIR through a balance of active silicon thickness and pixel size. (Paper 30.1, *Multi-Storied Photodiode CMOS Image Sensor for Multiband Imaging with 3D Technology*; Y. Takemoto et al, Olympus) The top imager is optimized for visible detection with an array of small pixels and a thinned 3 μm active silicon layer. NIR signals pass through it to reach the bottom imager, which is optimized for NIR detection with an array of larger pixels and thick active silicon. The researchers claim there is no degradation in color reproduction, sensitivity or resolution, features that are critical for end applications in the medical field. This should be a boon to physicians trying to make accurate and complete diagnoses.



Schematic of Multi-storied photodiode CMOS imager (Ref: Y. Takemoto et al., IEDM 2015, Paper 30.1)

3D circuits can be made either by stacking separate chips and connecting them through TSVs, or by stacking and bonding wafers where the individual die may be connected with TSVs or other interconnects, or by the use of monolithic 3D integration. In monolithic 3D, devices in adjacent layers are intimately and directly connected, thereby eliminating the need for TSVs which have relatively narrow I/O bandwidth. However, each layer in a 3D device must be annealed to remove stresses in its crystalline silicon structure, and to activate dopants which have been previously implanted. These annealing temperatures are often in excess of 1000C, which can lead to device damage. The current paper by Tsung-Ta Wu et al., NTHU, Taiwan overcomes this issue by using a CO2 far-infrared laser at 400C to selectively pulse-anneal source-drain regions of the silicon. (Paper 25.4, *Low-Cost and TSV-free Monolithic 3D-IC with Heterogeneous Integration of Logic, Memory and Sensor Analogy Circuitry for Internet of Things*; Tsung-Ta Wu et al, National Nano Device Laboratories/National Tsing Hua University). Using this technique, they built a sub-40 nm monolithic IC containing a variety of heterogeneous functions including logic, SRAM, RRAM, sense and logic amplifiers, and gas sensors. The researchers reported no device degradation using this localized annealing method, which they say makes the technique suitable for low-power, low-cost, small-footprint, and heterogeneously integrated devices.

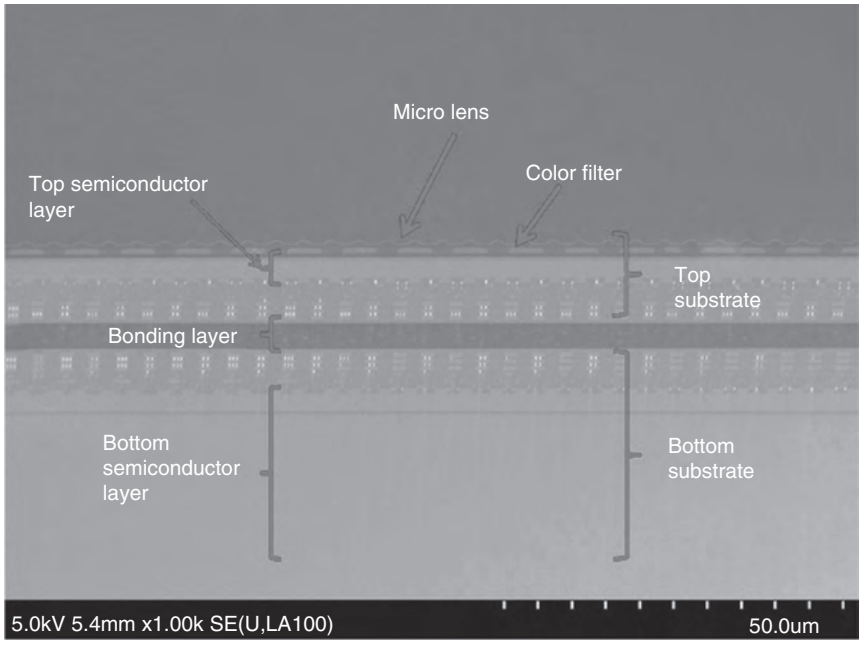
Internet of Things (IoT) applications require high frequency ultra-low power devices and circuits. 20 nm gate-all-around MOSFETs with incredibly low off-state currents of < 0.1 pA with cutoff frequencies exceeding 10 GHz

has been demonstrated by Daisuke Matsubayashi et al from Semiconductor Energy Laboratory Co. Japan. (Paper 6.5, *20-nm-node Trench-Gate-Self-Aligned Crystalline In-Ga-Zn-Oxide FET with High Frequency and Low Off-State Current*; Daisuke Matsubayashi et al, Semiconductor Energy Laboratory Co., LTD). Indium-gallium-zinc-oxide (IGZO) thin film transistors built using a self-aligned process that eliminated overlaps from the gate to the source and drain, rendering the channel immune from short-channel effects that otherwise would degrade performance.

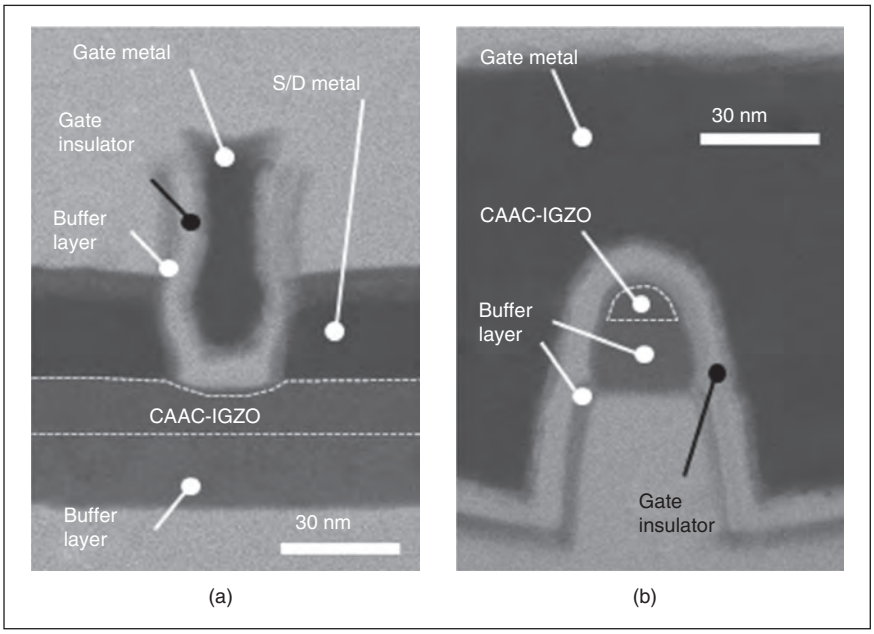
It is reported that the device integrated in a DRAM memory cell to demonstrate extremely low off-current, allowed for data retention of >10 days at 125°C.

Everyone wants a circuit they can bend to their will but although mechanically flexible circuits have the potential to enable revolutions in wearables and biomedical applications, the technology so far has not hit the mark. One reason is higher performance materials like single crystal silicon like to be processed at high temperatures, which is at odds with lower temperature flexible materials. A team led by France's Institutd'Electronique de Microélectronique et de Nanotechnologie proposed the ultimate thinning and transfer-bonding process in the Flexible Electronics session at IEDM 2015. (Paper 15.7, *Application-Oriented Performance of RF CMOS Technologies on Flexible Substrates*; Justine Philippe et al, IEMN/STMicroelectronics/CEA LETI Minatec). They demonstrated that even radio-frequency CMOS silicon circuits can be put onto substrates like polyimide plastic or stainless steel. They first thinned silicon SOI wafers to 30 μm by completely removing the backside and transferred the SOI circuits to plastic using a laminating process. The researchers claim their technique can enable ultra-mechanical flexibility, better heat dissipation and even transparent circuits.

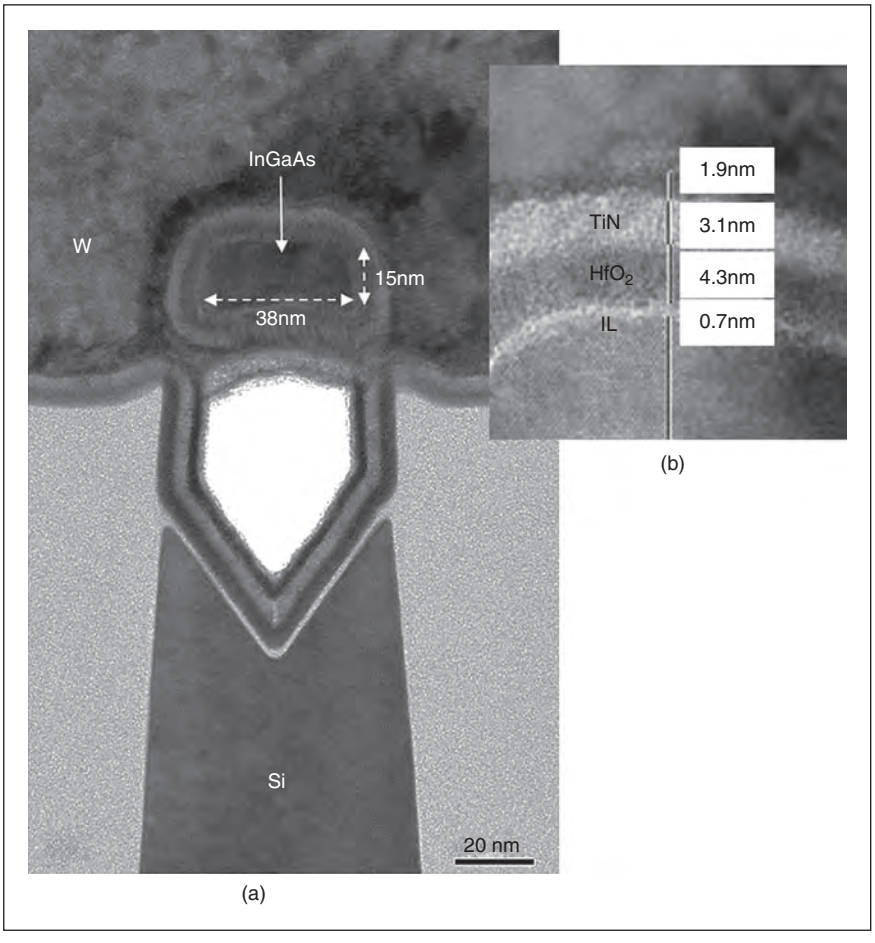
Performance benefits of III–V channels for low-power logic device applications have been demonstrated by the complete integration of these channels in devices made on silicon wafers. In the paper by Waldron et al., from IMEC discussed gate-all-around, high-performance InGaAs nanowire MOSFETs built on 300 mm silicon wafers. (Paper 31.1, *Gate-All-Around InGaAs Nanowire FETS with Peak Transconductance of 2200 μS/μm at 50 nm Lg Using a Replacement Fin RMG Flow*; N. Waldron et al, Imec/ASM). High transconductance (g_m = 2200) of the device indicates that despite having a lattice-mismatched substrate, the InGaAs channel



Cross-section image (SEM) of the device (Ref: Y. Takemoto et al., IEDM 2015, Paper 30.1)



Scanning transmission electron microscope images showing the IGZO device in the channel length direction (a) and in the channel width direction (b).
(Ref: D Matsubayashi, et al., IEDM 2015, paper 6.5)



Transmission electron microscope image of a InGaAs nanowire MOSFET device, while the inset shows the gate stack.
(Ref: N Waldron, et al., IEDM 2015, paper 31.1)

material maintains its high carrier velocity.

3D NAND architectures with gate-all-around (GAA) devices arranged in a vertical channel structure exhibits excellent device performance. However, these devices are highly sensitive to variations in their critical dimensions (CD), and it is difficult to maintain precise dimensional control of these structures at the required high aspect ratios. Macronix researchers described an alternate 3D NAND architecture that mitigates this issue by creating a 2D-like structure in the vertical direction. (Paper 3.2, *A Novel Double-Density, Single-Gate Vertical Channel (SGVC) 3D NAND Flash That Is Tolerant to Deep Vertical Etching CD Variation and Possesses Robust Read-disturb Immunity*; Hang-Ting Lue, Macronix). The structure is a single-gate, flat-cell thin film transistor (TFT) with an ultra-thin body named single-gate vertical channel (SGVC). The design is not as sensitive to CD variation and is reported to have more than four times the memory density of GAA vertical channels at the same scaling node.

Future flash memories may be stackable devices with polysilicon channels running vertically through them. However, grain boundary defects in polysilicon's crystal structure could decrease electrical conductivity by scattering and trapping electrons. A clear understanding of the actual conduction paths in these channels would enable more accurate predictions of how the devices will operate. In the IMEC paper by Robin Degraeve, et al., a new atomistic 3D model of grain boundaries taking into account the specific regions of enhanced scattering in the polysilicon and specific charge defects which can cause local barriers and depletion areas is presented. (Paper 5.6, *Statistical Poly-Si grain boundary model with discrete charging defects and its 2D and 3D implementation for vertical 3D NAND channels*; Robin Degraeve et al, Imec). This model gives statistical insight into the properties of scaled poly-Si channel devices (particularly vertical NAND devices), and their yield and reliability limitations.

*(This article is prepared by the **Editorial team of EDS Newsletter – Karim S. Karim, Mukta G. Farooq and M. K. Radhakrishnan.** The data used for the article has been provided by the IEDM Technical Chair)*

Upcoming Technical Meetings

43rd IEEE Photovoltaic Specialists Conference Preview

It is my distinct pleasure to invite you to be a part of the 43rd IEEE Photovoltaic Specialists Conference, June 5–10, 2016, which I am proud to host at the Oregon Convention Center in Portland, Oregon. This year's conference promises to uphold PVSC's tradition as a premier international conference on the science and technology of photovoltaics by providing an interactive forum for researchers, students, scientists, engineers, technology and business leaders from industry, academia, government in an environment conducive to strengthening collaborations and sharing knowledge across the field of photovoltaics. This year we are joining forces with the American Solar Energy Society to provide an even more varied and diverse meeting with a strong focus on systems and applications in addition to our traditional areas.

From PV discovery to deployment, our vision is to share state-of-the-art research results to hasten the widespread availability of solar electricity. The PVSC technical program covers the full spectrum of basic photovoltaic science, novel PV materials, device and module architectures, device and system performances, novel characterization techniques, component and system deployment and reliability. The 43rd PVSC will host keynote addresses, plenary talks, oral-presentation sessions and poster sessions in all technical areas, which are designed to provide each PV specialist ample opportunity to delve deeper into select topics or to expand their horizons into new PV-related areas. To complement our technical program, PVSC-43 also expects to offer full day short courses and half day tutorials covering a wide range of topics by leading experts, and will host a dynamic Exhibition for companies and research labs to showcase their latest products and innovations ranging from characterization to manufacturing.

Portland is a beautiful city and a home for outstanding science and technology. It is easily accessible from Europe and East Asia by air with direct flights to Tokyo, Ontario, Keflavik Iceland, Frankfurt, and Amsterdam, among others. Portland is the home to many notable local organizations such as the Oregon Museum of Science and Industry (OMSI), and is the home of Intel's research center, Solar World, SoloPower, and many others. Portland is also known for excellent food with a wide variety of outstanding restaurants and food trucks, and gardens. We expect the rose garden to be at the peak of its beauty in June when the conference is there. The region is well known for outdoor activities including hiking, birding, wind surfing, cycling, and many others.

Please join us in continuing the PVSC's tradition as the preeminent conference dedicated to the science and technology of photovoltaics! On behalf of all of the volunteers who comprise the PVSC Organizing, Cherry, and International Committees, I look forward to personally welcoming you in Portland for the 43rd IEEE PVSC!

Angus Rockett
2016 PVSC General Conference Chair

2016 IEEE International Vacuum Electronics Conference (IVEC)

We are pleased to announce that the Seventeenth International Vacuum Electronics Conference (IVEC2016) will be held in Monterey, California, USA, on April 19–21, 2016. The meeting will be held at the Marriott Conference Center only steps away from Fisherman's Wharf in downtown Monterey. Visitors from around the world come to Monterey to experience its natural coastal beauty, visit the renowned Monterey Bay Aquarium, and experience its rich historic past memorialized in the novels of John Steinbeck.

Sunset over California Coast, Photo Credit: istock.com

With sponsorship from the IEEE Electron Devices Society (EDS), the conference will provide a forum for scientists and engineers from around the globe to present the latest developments in vacuum electronics at frequencies ranging from UHF to Terahertz frequency bands, as well as their applications.

IVEC was originally created in 2000 by merging the US Power Tube Conference and the European Space Agency TWTA Workshop. Now a fully international conference, IVEC is held every other year in the US, and in Europe and Asia alternately every fourth year. After a successful and enjoyable IVEC2015 in Beijing, China, IVEC will return to Monterey in 2016. You can learn more about IVEC by visiting VacuumElectronics.org, the EDS Vacuum Electronics Technical Committee website.

IVEC2016 will last three days with one plenary session on the first half day, followed by approximately 25 technical oral and poster sessions planned for the remaining two and a half days. The plenary talks will provide insights into the history, the broad spectrum of fundamental physics, the scientific issues, and the technological applications driving the current directions in vacuum electronics research. Technical presentations will range from the fundamental physics of electron emission and modulated electron beams to the design and operation of devices at UHF to THz frequencies, theory and computational tool development, active and passive components, systems, and supporting technologies.

System developers will find that IVEC provides a unique snapshot of the current state-of-the-art in vacuum electron devices. These devices continue to provide unmatched power and performance for advanced electromagnetic systems, particularly in the challenging frequency regimes of millimeter-wave and THz electronics.

The John R. Pierce Award for Excellence in Vacuum Electronics and a Student Paper Award will also be presented at the conference. As in past conferences, the meeting and social events will provide unique opportunities to renew or establish new friendships with colleagues, interact with customers and end-users, and meet students and academic researchers.

The conference website is the best source of information about IVEC2016 including Technical Subject Categories, Paper Submission, Registration, Accommodations, and other important dates and events. Please visit http://ivec2016.org for more details and the latest news about the conference. To inquire about exhibitor space or conference support, please contact A. Waldron at awaldron@pcm411.com. We look forward to seeing you in Monterey.

David R. Whaley
2016 IVEC General Chair
L-3 Communications
San Carlos, CA, USA

2016 IEEE International Memory Workshop (IMW)

The 8th IEEE International Memory Workshop will be Held at the Paris Marriott Rive Gauche Hotel, Paris, France, May 15–18

In response to the growing global interest in memory technologies, the NVSMW – Non Volatile Semiconductor Memory Workshop – and ICMTD – International Conference on Memory Technology and Design – were merged together in 2008 to incorporate the volatile and non-volatile memory aspects in one forum while maintaining the workshop experience. The workshop is sponsored by the IEEE Electron Devices Society and meets annually in May. In 2016, IMW will take place in Paris, France.

The convergence of consumer, computer and communication electronic systems is leading to an exponential growth in need, mainly for code, computing and data storage. While in the past we could associate a memory technology to a specific

market segment (e.g., RAM to computer, NOR Flash to mobile communication, NAND Flash to consumer SSD), today the new electronic systems stack different memory technologies and use microcontroller to facilitate interfacing and managing the overall memory. Moreover, novel memory technologies are entering in the market, providing opportunities for novel applications and challenges for the technology development. The characteristics of these complex memory systems in terms of density, performance, power consumption, packaging and interfacing become of greater interest. The capabilities provided by the new memory technologies, new concepts and material proposed today will drive the definition of these memory systems in the future. The IMW aims to answer this need, extending the scope from non-volatile memory, which had been successfully discussed in more than 30 years of NVSMW's history, to large memory technologies and design, which were the focus of ICMTD, in the view of systems. Innovation is our tradition: IMW widened its focus while maintaining the positive characteristics of a workshop.

IMW is a unique forum for both specialists in all aspects of microelectronic memory and novices wanting to gain a broader understanding of the field. The workshop is usually attended by a wide international community from North America, Europe, Japan and Asian countries. Attendees include industry leaders, researchers in academia and industry as well as end users of memory products. The number of attendees typically exceeds 250 in recent years, reflecting the growing interest in the workshop. Each year we receive over 80 paper submissions and accept about 35 for oral presentation which corresponds to about 40% acceptance rate. Principal topics for discussion are: device physics, silicon processing, product testing, new technologies including new structures and novel approaches, programmable logic, memory cell design, integrated circuits, solid state disks and memory cards, reliability and new applications. Following the tradition established in previous IMW editions, Sunday, May 15th will be dedicated to a Short Course session. Moreover a poster session for qualified papers is usually held after the panel discussion.

An important goal of IMW is to provide an informal environment to encourage discussions and interactions among participants. There will be morning and afternoon technical sessions, along with a lively evening panel discussion on a hot topic in memory field. Technical interaction among presenters and attendees is encouraged through question and answer sessions and allotting ample time after formal paper presentations for further in-depth discussions. Organized breaks, including snacks and the conference dinner and lunch are provided as opportunities to meet and exchange ideas with colleagues. The morning and afternoon technical sessions are organized in a manner of providing time for the informal exchange and to enjoy the beauty of Paris area. The hotel is conveniently situated in Paris downtown, close to public transportations (subway, train) and it is easily accessible from the international airport (30–45 min). For more information about the conference, please go and register at the website www.ewh.ieee.org/soc/eds/imw.

Looking forward to seeing you next May at IMW 2016 in Paris.

Jing Li
2016 IMW General Chair
University of Wisconsin-Madison

2016 IEEE International Reliability Physics Symposium (IRPS)

The IEEE International Reliability Physics Symposium (IRPS) is the world's premier forum for leading-edge research addressing developments in the Reliability Physics of devices, materials, circuits, and products. IRPS is the conference where **emerging Reliability Physics challenges** and possible solutions to achieve realistic End-of-Life projections are first discussed. This year, the IRPS will be held at the Hilton Pasadena in Pasadena, California, USA, April 19–21, 2016. The IRPS will commence with

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two full days of tutorials and year-in-review on Sunday, April 17th and Monday, April 18th.

The IRPS draws presentations and attendees from industry, academia and governmental agencies worldwide. No other meeting presents as much leading work in so many different areas of reliability of electronic devices, encompassing silicon device, non-silicon device, process technology, nanotechnology, optoelectronics, photovoltaic, MEMS technology, circuits and systems reliability including packaging.

For the IRPS 2016, we are emphasizing **Self-heating effects** on transistors and circuit aging. We are also emphasizing **Systems reliability** comprehending complex applications including Chip-Package interactions and packaging. Finally, we are strongly promoting all reliability works on **Photovoltaics**.

For 54 years, IRPS has been the premiere conference for engineers and scientists to present new and original work in the area of microelectronics reliability. Drawing participants from the United States, Europe, Asia, and all other parts of the world, IRPS seeks to understand the reliability of semiconductor devices, integrated circuits, and microelectronic assemblies through an improved understanding of both the physics of failure as well as the application environment. IRPS 2016 will offer a full slate of tutorials, evening panel debates and workshops, invited plenary talks in addition to an **outstanding technical program**.

The hotel is located in Pasadena's downtown which is best known as the host of the annual Tournament of Roses Parade and Rose Bowl football game. The City also boasts numerous cultural amenities, fine restaurants and top retailers. All this helps Pasadena live up to the true meaning of its name—the Crown of the Valley.

IRPS consists of three days (Tues–Thurs, April 19–21) of plenary and parallel technical sessions presenting original, state-of-the-art work.

Other opportunities at the symposium include:

- Two-Day **Tutorial Program** (Sunday–Monday April 17–18). The IRPS tutorial program is a comprehensive two-day event designed to help both the new engineer and experienced researcher. The tutorial program contains both beginner and expert tracks, and is broken down into topic areas that allow the attendee to participate in tutorials relevant to their work with a minimum of conflicts between subject areas.
- **Year in Review** Session (Monday April 18). These seminars provide a summary of the most significant developments in the reliability community over the past year. This serves as a convenient, single source of information for attendees to keep current with the recent reliability literature. Industry experts serve as the "tour guide" and save you time by collecting and summarizing this information to bring you up to date in a particular area as efficiently as possible.
- Evening **Poster Session**. The poster session will provide an additional opportunity for authors to present their original research. The setting is informal and allows for easy discussion between authors and other attendees.
- Evening Session **Workshops**. These workshops enhance the symposium by providing the attendees an opportunity to meet in informal groups to discuss key reliability physics topics with the guidance of experienced moderators. Some of the workshop topics are directly coupled to the technical program to provide a venue for more discussion on the topic.
- **Vendor Exhibits**. Held in parallel with the technical sessions, the equipment demonstrations provide a forum for manufacturers of state-of-the-art laboratory equipment to present their products. Attendees are encouraged to visit the manufacturers' booths for information and demonstrations.
- **IRPS Paper Awards**. IRPS bestows awards for Best Paper, Outstanding Paper, Best Poster and Best Student Talk. The Best Paper author is typically invited to present the paper at ESREF in October.

For registration and other information, visit the IRPS 2016 home page at http://www.irps.org/. The IRPS committee members look forward to seeing you in April.

Vincent Huard
2016 IRPS Publicity Chair
STMicroelectronics

Chris Henderson
2016 IRPS General Chair
Semitracks, Inc.

EDS Board of Governors Meeting Highlights

In keeping with our long-standing tradition, the EDS Board of Governors once again convened in advance of our flagship conference IEDM to hold the year-end EDS governance meeting series.

The meeting series and the IEDM were held at the Hilton Washington, DC. The Washington Hilton has been the IEDM's East Coast home for many decades but this year marks the final East Coast IEDM for the foreseeable future. After this year, we will host this event in San Francisco each year, as opposed to alternating with Washington, DC.

Beginning on Saturday morning, the weekend kicked-off with spirited committee meetings for each of the society's crucial functional areas: newsletter, publications, conferences and technical activities, education, and regions and chapters. Led by the VPs and chairs of our standing committees, the groups, comprised of not just committee members, but also interested EDS members, reviewed the year's operations and finalized plans for 2016.

Highlights from the committee meetings include:

- Newsletter. The committee stressed the need for growth in participation from chapters in Regions 1-8 and to find ways to better engage and recognize new members in the newsletter. Congratulations to Newsletter Editor-in-Chief MK Radhakrishnan, for his outstanding service to the Society.
- Publications. A pillar of EDS since its inception, EDS's publications continue to thrive. The committee met to address issues relating to Open Access, conference publishing, and ways to maintain the integrity of our publications, while improving the diversity of authors and readers as well as our speed to publication.
- Joint Membership, Education, and Chapters. A large group of volunteers gathered for spirited debate about how we can better attract and retain students and young professionals, as well as continuing to be relevant with established member base.
- Conferences and Technical Activities. Another critical area for the Society, this Conferences and Technical Activities committee met to review the 2015 conferences, discuss plans for extending our partnership with SEMICON West, and strategize how to establish a bigger conference presence in Region 10.

EDS Officers for 2016-2017 (left to right): Subramanian Iyer, Treasurer; Samar Saha, President; Simon Deleonibus, Secretary; and Fernando Guarin, President Elect

Saturday culminated with the working dinner meeting of the EDS Executive Committee (ExCom) to provide a venue for the society's senior volunteer leadership to discuss and refine the strategic vision of the society.

The main EDS Governance meeting took place on Sunday, starting early in the morning and running through the late afternoon. The day was marked by impassioned dialogue and debate about the future of EDS both from a technical and operational perspective. New markets need to be explored, new challenges need to be bested, and EDS is taking bold steps

to ensure its continued relevance and success in the future. And to lead the Society into that bright, promising future, we are pleased to announce the results of the 2016 Officer and Member-at-Large election.

As you may recall, last year we began a pilot program to have 1 Member-at-Large (MaL) selected by the general membership of the Society. This year several thousand EDS members took part in the general election, voting for **Doug Verret**.

The remaining six MaL seats were selected by the sitting Board of Governors. The winners in that election were **Navakanta Bhat, Daniel Camacho, Simon Deleonibus, Meikei Ieong, Murty Polavarapu, and Ravi Todi.**

The EDS officer elections were also held. The incoming Secretary of the Society is **Simon Deleonibus**. The incoming Treasurer is **Subu Iyer**. And last, but certainly not least, the 2016–2017 President Elect is **Fernando Guarin**. Information and biographies of the newly elected officers will appear in the next issue of the EDS Newsletter (April 2016).

Our thanks to all those who took part in the election. We are very fortunate to be blessed with so many talented, dedicated volunteers. In closing, let us congratulate our election winners and wish them great success in their new elected positions.

Christopher Jannuzzi
EDS Executive Director

Message from Outgoing President of EDS

Albert Wang
EDS President
2014–2015

Dear Fellow EDS Members,

The Message that you are reading is the fourth and last President's Message for my two-year term as EDS President. Writing the message in a high-speed train leaving Beijing at a speed of 350 km/hour and watching the flashing scenes through the window, I am quickly recapping what have happened within the EDS community in the past two years. Instead of giving a usual summary of the "achievements" during my term, I would rather talk a little about the challenges that EDS is facing in this Message.

The main challenge is about operations and finance transparency at both IEEE and EDS levels. As I reported before, EDS is one of the five societies initiated the big effort of pushing for IEEE finance transparency and plays a leading role on the ad hoc Fin-Trans committee in the past two years. We presented the EDS financial data several times at the TAB meetings to argue for finance transparency at IEEE level. With the joint efforts, progresses were made and IEEE finance team is opening its finance nutshell, though slowly and with limited contents, to societies for analysis. Are there anything interesting revealed? You bet! For example, the data revealed that a society paid IEEE about $4200 per article in 2015 for published paper and the tax paid to IEEE for its Corporate IT costs increased 25% from 2014 to 2015. What a surprise, or not?! It at least speaks out loudly that it makes sense to keep IEEE finance transparency to the volunteers. Being on the EDS leadership team for many years, I know that local chapters have had difficult times in asking for a few hundred dollars to support some well-planned member activities. Good finance transparency helps volunteer leadership to manage society budget and serve the volunteers better. Keep in mind that volunteers work for FREE and IEEE is a not-for-profit organization.

Of course, operations transparency at EDS level is also needed. During my term, we identified one key area to improve for EDS operations transparency, which is to establish a clear written journal editor-in-chief (EiC) selection procedures that did not exist. Thanks to the great efforts of the Publications and Products Committee (PPC), led by the VP Pubs, as well as contributions from many other volunteers, we are making solid progresses in reforming the way that we selected EiCs for our journals. In the first phase, a transparent temporary EiC selection procedure was used to select the new EiCs for TED and EDL. Both new EiCs are in place to run the Transactions on Electron Devices and the Electron Device Letters. Currently, the PPC is working to finalize the formal EiC Selection Procedures documentation, which shall be completed soon. I consider this being a major achievement in my term that resolved a decades-long problem in EDS operations. In terms of EDS operations, I fully believe that the best way to ensure smooth and transparent operations is to establish a solid "infrastructure" guided by clear-written documentation, hence, everyone can follow the written policies in conducting EDS business. This shall ensure smooth operations of EDS without suffering possible single-event disruption and any individual influences. We have made progresses in this regard. For example, the Charters were drafted for all standing committees. We shall continue this effort in order to ensure long-term health of EDS.

Another truly major challenge is the membership development, which has been a big problem to IEEE as a whole too. While EDS has worked very hard to maintain our around-10000 member pool, what will be the way to grow our community? Unlike the transparency problem that we know how to resolve, there are no "good" solutions to the membership development challenge, at least, not to me. I am calling for any ideas and suggestions from our members. I believe that the key to membership development, or put it in a different word, the survival of EDS and IEEE, depends completely on if our members and potential members will be happy with the society. We ought to keep in mind that IEEE and EDS are volunteer-driven organizations for volunteers only. Should this key point being ignored, there would be no way to survive, not even thinking of growth and prosperity. For this reason, keep IEEE and EDS operations and finance transparency is of vital importance.

Being forward-looking and adaptive is yet another challenge to EDS future. We are living in a fast-changing era where everything moving extremely fast, technically and socially. The traditional mind-sets will not work anymore. We already saw many used-to-be-untouchable giant companies collapsed in seconds in recent years. IEEE and EDS cannot be any exemption. For example, should we adapt the open access (OA) publication model? Maybe nobody knows for sure for now yet, however, we shall not miss the train. Indeed, our JEDS journal is facing tremendous challenge now. However, JEDS may eventually help EDS to survive the OA future. We ought to be brave in doing new experiments in order to ensure our future. Similarly, many traditionally strong conferences, mainly in North America, are facing problems now due to many emerging challenges. For example, the decades-long party of CMOS scaling down is fast approaching its end, non-traditional and non-electronic devices are emerging, internet-of-things technologies are quickly shaping up, semiconductor industry is shifting to Region 10, etc. We have to admit that EDS made some mistakes before that resulted in losing the due ownership of several emerging device domains to others, such as, MEMS, sensors, nano technologies, to name a few. By nature, those are all devices that certainly belong to EDS. Unfortunately, EDS is only playing a side role in many of these emerging device areas now. We cannot afford making any similar mistakes anymore. We have to be more open-minded and absolutely adaptive in order to survive, grow and prosper in this fast-changing era.

Dear colleagues, I really enjoyed being with all of you for years, not just during my Presidency. I certainly appreciate all of your efforts in making EDS being today. I also want to thank my ExCom team (Renuka Jindal, Paul Yu, Samar Saha, Bin Zhao, Leda Lunadi, Mikael Ostling, Xing Zhou, Ravi Todi and Fernando Guarin) for working with me in the past two years to run the society. My special thanks go to our staff team in the Executive Office who worked hard to maintain EDS operations. While I outline some challenges above, I fully believe that challenge also means opportunity. With 10000 members around the globe, the future of EDS shall be bright! Please keep in mind that EDS is a volunteer society and it exists for only one reason: for volunteers!

Sincerely,
Albert Wang
EDS President on his way out

Message from Incoming President of EDS

Samar Saha
EDS President
2016–2017

Dear Fellow Electron Devices Society Members:

I am extremely honored and pleased to assume the duties as President of IEEE Electron Devices Society (EDS). EDS has always led by extraordinary visionary leaders in the past. I take this opportunity to thank the past leadership for making EDS one of the best societies of IEEE. I will continue *building* EDS *on the foundation of the past to meet the challenges of the future*.

EDS is, truly, an international society with more than 10,000 members and 190 chapters worldwide. Over the past *six* decades, EDS has been promoting the advancement of the professional standing of its members and has been enhancing the *quality of life for humanity* through its members' contributions in R & D, manufacturing, and application of electronic and ionic devices. Our Society is an all-volunteer society, driven to excellence by its leadership, with the active participation of all our worldwide members. EDS has always been, clearly, one of the premier societies of IEEE and is by far the best of all professional associations operating in the global device technology arena. So, we are in a very good position. However, as

device technology is approaching to a challenging regime, we cannot sit back and relax on our past.

In the years ahead, *business will not be as usual*. Now, things can change much faster than ever due to Internet. There are ongoing trends in publication business, organization of conferences and exhibitions, content distributions, knowledge access, education, membership models of technical societies, strategic or temporal partnering with other societies or groups, field of standards, and in the knowledge management that may or will affect EDS's operations. In my view, the current areas of focus of our society: (1) membership; (2) publications; (3) conference management; (4) chapters; (5) educational activities; (6) sponsored awards; (7) EDS Mission Fund, and so on are well defined. And, we are in good standing with our definition of *near-future directions and engagements*. However, we must develop strategy for *outreach program* to benefit our Society and define our *future directions* for *smart electronic systems* such as *devices* for *smart-cars* including *self-driving* or *driver-less* cars, *smart-city infrastructure*, *Internet of Things*, and so on. Therefore, my plan is to continue with our current activities and execution processes, and *develop* a suitable *outreach program* and *define the future directions* of our Society. I will discuss some of these programs below and some in due course of time of our engagement.

- ***Membership Growth***: Our Society membership continues to be around 10,000 for a while. In spite of maintaining this overall number, the membership in some geographical regions continues to decline. I intend to develop strategies for membership drive through our Subcommittee for Regions & Chapters volunteers.
- ***Publications Excellence***: It is of paramount importance that we consistently work not only to keep but also to *expand our worldwide leading position* with respect to publications by always operating at the forefront and by keeping the quality of published papers as high as possible. In this respect, I plan to develop EDS Open Access (OA) strategies to make our newly launched the *Journal of Electron Devices Society* (J-EDS) one of the top-tiered topical OA publications in IEEE and competing OA publications on device technology through our Publications and Products volunteers.
- ***Conference Management***: Similar to our publications, it is extremely important to *expand our worldwide leading position* with respect to device conferences. In this context, I intend to drive the *Asia Electron Devices Meeting* and set a realistic schedule for the inaugural conference in Asia. Conference income is the major component of the Society's income. I intend to develop management policies and procedures that will assure the integrity of the income stream and the continued success of our conferences.
- ***Chapter Growth***: Chapters are vital to the overall success of EDS and growth of our Society's membership. We must provide the necessary assistance to our chapters to actively engage in EDS programs. Also, it is extremely critical to plan the growth and development of EDS *Student Chapter*. Today's academic institutions hold the engineering professionals of tomorrow. I intend to continue to be heavily focused on developing programs to benefit today's students and help them prepare for entry into the industry or academia with an objective to strategically add Student Chapters from many of the academic institutions worldwide.
- ***Educational Program***: Our Society has earned praise from 2015 *Five-year Society Review Committee* for our stellar educational programs including Masters Student and PhD Student Fellowships, Distinguished Lectures (DLs), Mini-Colloquia (MQ), Webinar, and so on. Our thanks go out to all involved, *distinguished lecturer* and *volunteers*, in making these programs a high-value benefit for our members. Our topical areas for DLs, MQ, and Webinars provide opportunities to our members for *networking* and *learning* from fellow members and recognized experts in the field. In addition to continuing the existing programs, I intend to explore the feasibility of introducing a *Tutorial Program with leading experts in the field as Tutors.*
- ***Outreach Program***: I plan to actively pursue EDS *Outreach Program*. Being involved in industry as well as in academia, I am aware of most students' thought processes and their views on engineering and technology. Also, being associated with volunteers around the globe, I know that the attitudes of people from different geographical regions are different. So, I plan to engage outreach programs: *Outreach to Youth*, *Outreach to Industry*, and *Outreach to other Societies*. We need to evaluate which strategic or temporal alliances or kind of partnerships will help us to better reach our goals. The EDS *Field of Interest Statement* overlaps with the societies that spawned out of EDS. I think by working with the *Overlapping Societies* we can form a mutually profitable relationship that will increase the membership of EDS and partner Societies while increasing the service and benefits to the members of all the Societies involved.
- ***Future Directions***: In my view, EDS must get involve in *Future Direction* programs. The impact of electronic devices from the component level to system level is more than ever. This is, especially, true for emerging application areas such as automotive industry,

industrial automation, life sciences, security, logistics, mobility, energy saving, social networking, and environmental protection where high growth rates are evident. In all these areas, electron devices are crucial to the competitiveness of companies and entire industry sectors, as these technologies provide pertinent key enabling functionalities and are thus, a driving force behind numerous product innovation activities. In particular, device technologies play a key role in nearly all areas of computers, communications, and social media. Further, the semiconductor industry will continue to evolve in providing *smart-electronic devices* enabling solutions for *smart-cars*, *smart-homes*, *smart-city infrastructure*, *Internet of Things*, and so on. The smart city infrastructure for driverless cars requires smart electronic system along with software codes to communicate cars and urban traffic system for the safety of drivers and pedestrians and maintaining echo systems. The emerging trends will greatly influence the future of our *technical field of interest* and therefore, to the *broad spectrum and the territory of our Society*. This offers EDS opportunity to outreach automobile industry to define device specifications and set standards for smart electronic devices and products and outreach city governance to set strategies for smart-city infrastructure.

Thus, I intend to engage in Future Direction programs through our Technical Committees and volunteers to organize conferences, Webinar, MQ, and DLs, publish Special Issues, and so on.

These are all very worthy goals; so, I urge all EDS members to publicize the benefits our Society offers and help achieving our goals. The most important step to achieve our goals is to *empower* our Executive Committee (ExCom), Board of Governors (BoGs), Technical Committees, and the Membership to involve in the activities of the Society. As mentioned, EDS is an all-volunteer society and thus, the *selfless dedication* of our volunteers is of utmost importance for the well-being of our Society. Our volunteers organize our conferences, workshops, DLs, MQ, Tutorials, and Education programs; they lead our publications and review submitted papers; and they serve on our Local Chapters, Technical Committees, BoGs, and ExCom. So, I encourage all our members to get involved at any level – attending events, volunteering to help with specific activities or joining one of our 14 Technical Committees. Personally, I have been involved with EDS for over 25 years. The knowledge I gained and the life-long friends I met along the way have made EDS membership a tremendous experience for me, both personally and professionally. It has always been a pleasure for me to work with my volunteering colleagues towards the well-being of the *global electron devices community*. So again, get involved and bring along anyone else you know, new to the field, or experienced technologist or researcher, and see what EDS can do for you – you will be glad you did! Together we can continue to make EDS a great Society for all our members. And, I am humbled for the opportunity to lead the way.

Finally, I congratulate the newly elected members of BoGs and Officers and, newly appointed ExCom members and Technical Committee Chairs and Members. The Excellence of our Society has been achieved through the hard work and dedication of our previous Officers, ExCom, BoGs, Technical committees, and our Chapter volunteers. So, my sincere thanks to all those involved. I look forward to working with our new BoGs, ExCom, and Technical Committees to further the great work done to make EDS one of the premiere societies in IEEE. Without the hard work and dedication of these individuals, our membership would not be able to enjoy and benefit from all the activities and resources our Society has to offer. Our Society is here to serve you. If you have ideas for improving EDS, I would love to hear from you. Please do not hesitate to contact me.

Samar Saha
EDS President
Prospicient Devices
Milpitas, CA, USA

Message from Editor-in-Chief

M.K. Radhakrishnan
Editor-in Chief

Dear Readers and EDS members,

Wish you all a Happy New Year 2016.

This issue of the Newsletter has few significant features and the major one is the recap of the IEDM 2015 held from December 7–10, 2015 in Washington, DC. This is the first time EDS Newsletter is giving a technical summary of some of the key presentations at IEDM. With this article as the major technical one in the Technical Briefs section, we are intending to provide an abridged version of some of the key papers depicting the trends in device technology and its applications. IEDM being the major technical event of IEEE and Electron Devices Society and the Newsletter is the medium for the society to communicate with its members at large, the Editorial team considers such an article is the best platform for our readers to

know about the trends and happenings in the field. However, due to various limitations we could capture the gist of some of the key papers from few sessions only.

A summary of the deliberations in the Society's Board of Governors meeting held on December 6, 2015 is given in this issue. Also, the yearly BoG election results are reflected and a write up about the newly elected BoG members will appear in April issue.

In the Chapter News section, we have the Chapter of the year award winners being listed. Also, these winners are asked to provide their mode of operation as a successful chapter. The winner from R10 is featured here and rest will be appearing in April.

A recent survey about the Chapter's visibility in Newsletter shows not much variation in the Chapter's reporting for many years. Among the present 190 EDS Chapters spread over all the Regions, only less than 40 percent of the Chapters are found sending articles and reports to Newsletter, even after repeated requests from Regional Editors. As the Editorial team, we would like to hear the reasons for this inactive approach by our Chapters and if we need to do anything specific, please communicate. However, as EiC, I would like to congratulate two chapters – ED Kansai Chapter and ED Japan Chapter – for regular reporting of activities in every issue of Newsletter for the last 5 years. Kudos to both Kansai and Japan Chapters.

Again, it is our readers' comments, criticisms and suggestions that make this Newsletter strong, and I request all the readers to write their feedback to edsnewsletter@ieee.org OR to me radhakrishnan@ieee.org

MK Radhakrishnan
Editor-in Chief, EDS Newsletter
e-mail : radhakrishnan@ieee.org

EDS Celebrated Members

The EDS Celebrated Member was established in 2010 by the IEEE Electron Devices Society. It is intended to recognize and honor legendary individuals in the field of electron devices.

"For fundamental contributions to the field of electron devices for the benefit of humanity"

Dr. Jayant Baliga
Celebrated Member

Dr. Jayant Baliga is an internationally renowned scientist, author of 19 books and over 550 publications, with 120 U.S. patents to his name. Among his inventions, the Insulated Gate Bipolar Transistor (IGBT) is extensively used around the globe for compact fluorescent lamps, air-conditioning, home appliance controls, robotics, electriccars/bullet-trains, and compact defibrillators projected by the AMA to save 100,000 lives a year. The energy efficiency improvements derived from IGBTs have saved world-wide consumers more than $ 24 Trillion while reducing carbon dioxide emissions by over 100 Trillion pounds during the last 25 years. Dr. Baliga led the development of the IGBT at GE from 1980–1985 resulting in its widespread applications within the company. GE announced the first commercially available IGBT product in July 1983 based up on his design.

In the early 1970s, Dr. Baliga pioneered the growth of semiconductor films by Metal-Organic-Chemical-Vapor-Deposition (MOCVD) with Professor Ghandhi at Rensselaer Polytechnic Institute. In 1979, he developed a theoretical analysis resulting in the Baliga's Figure of Merit (BFOM) which relates the resistance within power rectifiers and FETs to the basic semiconductor properties. He predicted that the performance of Schottky power rectifiers and power MOSFETs could be enhanced by several orders of magnitude by replacing silicon with gallium arsenide and silicon carbide. Under his direction, the first GaAs power devices were demonstrated at GE in the 1980s followed by the first high performance SiC high voltage rectifiers and MOSFETs at NCSU in the 1990s. Wide band gap semiconductors are now the basis for a new generation of power devices in the 21st Century.

Dr. Baliga is also a serial entrepreneur having founded four successful companies in North Carolina with venture capital financing. His inventions, commercialized by these companies, include: the TMBS rectifiers used in solar cell panels and power supplies; the RF super-linear power MOSFETs used in cellular base-station power amplifiers; the SSCFET/JBSFET chip set for voltage regulator modules used to power microprocessors and graphics chips in personal computers, laptops, and servers; and the GD-MOSFETs used in power supplies for data-centers and in automotive electronics.

President Obama presented the National Medal of Technology and Innovation, the highest honor conferred by the United States to an Engineer, to Dr. Baliga in 2011. He received the North Carolina Award for Science, the highest honor given by the state to a civilian, from Governor Purdue in 2012. In 2015, he received

the Global Energy Prize in Saint Petersburg, Russian Federation for the invention, development, and commercialization of the IGBT. He will be inducted into the National Inventors Hall of Fame in 2016 for invention of the IGBT.

Prof. Baliga is a Life Fellow. His IEEE awards include: the 1991 Newell Award, the highest recognition from the Power Electronics Society; the 1993 Morris E. Liebman Award for his contributions to emerging Smart Power Technology; the 1998 J.J. Ebers Award, the highest recognition from the Electron Devices Society; the 1999 Lamme Medal from the Board of Governors; and the highest IEEE award, the IEEE Medal of Honor in 2014.

"For fundamental contributions to the field of electron devices for the benefit of humanity"

Dr. Robert H. Dennard
Celebrated Member

Dr. Robert H. Dennard has been an industry leader in the development of microelectronics in a career that has spanned 57 years. He is responsible for two major milestones in the progress of the industry, the invention of DRAM (Dynamic Random Access Memory) and the development of scaling principles for miniaturization of MOS (Metal Oxide Semiconductor) transistors and their associated integrated circuits.

Dr. Robert Dennard received the B.S. and M.S. degrees in electrical engineering from Southern Methodist University, Dallas, TX, in 1954 and 1956 respectively, and the Ph.D. degree from Carnegie Institute of Technology (now Carnegie Mellon University), Pittsburgh, PA in 1958. He then joined IBM Research Division where his early experience included the study of new digital devices and circuits for logic and memory applications, and the development of advanced data communication techniques. Since 1963 he has been at the IBM Thomas J. Watson Research Center, Yorktown Heights, NY, where he has been involved in microelectronics research and development from the early days onward. His primary work has been in MOS transistors and integrated digital circuits using them. In 1966 he invented the one-transistor dynamic RAM memory cell used in most all computers today. He was also an advocate for word and bit line redundancy for DRAM yield improvement. It was first used in the IBM 64Kbit DRAM and became a standard technique in the DRAM industry since then.

With coworkers he developed the concept of MOS transistor scaling in 1972, which is often cited as a guiding principle for microelectronics. In 1973 he became manager of a research group which developed advanced design concepts for 1-micron NMOS silicon gate technology. This included collaboration with Dr. H.N. Yu in demonstration of an exploratory 8Kbit DRAM chip with dimensions scaled to 1 micron, greatly reducing the chip area using electron-beam pattern definition and the first reported use of reactive ion etching (RIE) in chip fabrication.

Dr. Dennard was appointed an IBM Fellow in 1979 and has continued to develop technical strategy for scaling CMOS logic and memory technologies to very small dimensions, anticipating future scaling challenges and studying new device and circuit approaches to continue progress in microelectronics.

He is an author of over 100 technical papers and an inventor of 67 issued US patents.

Dr. Dennard is a Life Fellow of the Institute of Electrical and Electronics Engineers (IEEE), a member of the National Academy of Engineering, and a member of the American Philosophical Society. He received the IEEE Cledo Brunetti Award in 1982. In 1988 he was awarded the National Medal of Technology by President Reagan for his invention of the one-transistor dynamic RAM cell. He received the IRI Achievement Award from the Industrial Research Institute in 1989 and the Harvey Prize from Technion, Haifa, Israel, in 1990. Dr. Dennard was inducted into the National Inventors Hall of Fame in Akron, Ohio in 1997. In 2001 he received the Aachener and Munchener Prize for Technology and also was awarded the IEEE Edison Medal.

He received the Vladimir Karapetoff Award from Eta Kappa Nu in 2002 and the Lemelson-MIT Lifetime Achievement Award in 2005. Dr. Dennard received NEC's C&C Prize in 2006 and the Benjamin Franklin Medal in Electrical Engineering in 2007. He was awarded the Charles Stark Draper Prize by the National Academy of Engineering in 2009. He also was honored with the 2009 IEEE Medal of Honor. Dr. Dennard received the prestigious Kyoto Prize in 2013.

Dr. Dennard and his wife Jane Bridges live in Croton-on-Hudson, NY. They are active participants in Scottish Country Dancing and choral singing.

EDS Vacuum Electronics Technical Committee Report

The Vacuum Electronics Technical Committee (VETC) (Vacuum Devices) is a long-standing committee within the EDS, originally formed to represent Electron Tubes. Since the beginning, the VETC has made it their mission to identify technical trends, help foster new technical developments in the field, and serve the emerging needs of the vacuum device community at large. The committee members include recognized technical experts who represent a very wide spectrum of interests including but not limited to physical electronics, vacuum electronic technology, devices, and education. They work closely together with IEEE journal editors and conference organizers.

VETC Chair, Dr. Richard True (standing), hosted the VETC Meeting

The annual face-to-face VETC meeting was held jointly with IVEC 2015 in Beijing on April 28, 2015. Dr. Richard True, Committee Chair, presided over the meeting. Seventeen members attended.

In the meeting, Dr. David Abe, General Chair of IVEC2014, gave a summary of the conference, Dr. Jinjun Feng presented the preliminary report on the ongoing IVEC2015, Dr. David Whaley, General Chair of IVEC2016, reported on the progress of the next conference, and Professor Claudio Paoloni described site selection for IVEC2017 in Oxford, United Kingdom. Other topics such as the next IEEE Transactions on Electron Devices Special Issue, the VETC website, and future occurrences of IVEC were also discussed at the meeting.

The VETC would like to express special thanks to Professors Richard Carter and Manfred Thumm for their service as *IEEE Transactions on Electron Devices* Editors and Professor Claudio Paoloni for founding and maintaining of the VETC website http://vacuumelectronics.org.

Jinjun Feng
2015 IVEC Technical Program Chair

Richard True
EDS VTEC Chair

Committee meeting attendees (missing from picture is Prof. Gun-Sik Park, Dr. Armand Staprans, Dr. William Menninger and Prof. Yaogen Ding)

Call For Nominations – IEEE Fellow Class of 2016

IEEE Fellow is a distinction reserved for select IEEE members. The honor is conferred by the Board of Directors upon a person with an extraordinary record of accomplishments in any of the IEEE fields of interest.

If you know of an IEEE colleague who is a Senior Member or Life Senior Member in good standing, has completed five years of service in any grade of IEEE Membership and who has made an outstanding contribution to the electronic or electrical engineering profession in any of the IEEE fields of interest, you can nominate this person in one of four categories: Application Engineer/Practitioner, Educator, Research Engineer/Scientist or Technical Leader.

Nominations for the Fellow Class of 2016 are now being accepted.

To learn more about the Fellow program and the application process, visit the Fellow Web Site at http://www.ieee.org/fellows. The deadline for nominations is 1 March 2015.

2014 EDS George E. Smith Award

Bin Zhao
EDS Vice-President of Publications and Products (2013–2015)

A high priority of the Electron Devices Society (EDS) is to recognize and enhance the quality of papers published in EDS archival literature. The George E. Smith Award was established in 2002 to recognize the best paper appearing in a fast turnaround archival publication of EDS, targeted to the *IEEE Electron Device Letters*. Among other criteria including technical excellence, an important metric for selection for the award is comprehensive and impartial referencing of prior art.

The paper winning the 2014 George E. Smith Award was selected from 397 articles that were published in 2014. The paper is entitled, *"Record Hole Mobility at High Vertical Fields in Planar Strained Germanium on Insulator With Asymmetric Strain."* This paper appeared in the March 2014 issue of the *IEEE Electron Device Letters* and was authored by Winston Chern, Pouya Hashemi, James T. Teherani, Dimitri A. Antoniadis, and Judy L. Hoyt.

The award will be presented at the plenary session of the IEEE International Electron Devices Meeting to be held on December 7, 2015, in Washington, DC. In addition to the award certificate, the authors will receive a check for $2,500 to be shared equally among all authors. On behalf of the Electron Devices Society, I would like to congratulate the authors for this achievement. Brief biographies of the authors follow.

Dimitri A. Antoniadis received his B.S. in Physics from the National University of Athens in 1970 and his M.S. and Ph.D. in Electrical Engineering from Stanford University in 1972 and 1976 respectively. He joined the MIT faculty in 1978 and is currently the Ray and Maria Stata Professor of Electrical Engineering. He is member of the National Academy of Engineering, IEEE Life Fellow, and recipient of several professional awards. He has made seminal contributions in the area of solid-state processes and electronic devices, quantum-effect-devices, and CMOS device engineering. His current research is on technology and modeling of nanoscale electronic devices in Si, Ge, and III–V materials.

Winston Chern is a PhD candidate in Electrical Engineering and Computer Science (EECS) at MIT working with Professors Judy Hoyt and Dimitri Antoniadis. He received his B.S. degree in Materials Science and Engineering at University of Illinois at Urbana-Champaign in 2010, and his M.S. in EECS from MIT in 2012. His research interests include Si/Ge and III–V semiconductor devices and their applications.

Pouya Hashemi received Ph.D. with honors from MIT in 2010 and is

currently a scientist at IBM Research focusing on exploratory CMOS devices and integration of advanced channel-materials for sub-10nm nodes. A member of IEEE EDS, his work has led to 80 publications and over 100 pending or issued patents.

Judy L. Hoyt received the B.S. degree in Physics and Applied Mathematics from the University of California, Berkeley in 1981, and the Ph.D. degree in Applied Physics from Stanford University in December, 1987. From 1988 through 1999 Dr. Hoyt was on the research staff in Electrical Engineering at Stanford University. In January 2000 she became a faculty member in Department of Electrical Engineering and Computer Science, Massachusetts Institute ofTechnology, Cambridge, MA. Prof. Hoyt's primary research interests are in the areas of silicon-germanium heterostructure devices and technology, epitaxial growth, solar cells, Ge-on-Si photodetectors and CMOS front-end processing. She has authored or co-authored over 180 publications in these areas, and holds 6 patents. Prof. Hoyt has served as General Chair of the IEEE International Electron Devices Meeting (2001), is a Fellow of the IEEE, and a member of the American Physical Society. She received the IEEE Paul Rappaport Award in 1989, the IEEE George Smith Award in 2005, and the IEEE Andrew S. Grove Award in 2011. Additional information is available at http://www-mtl.mit.edu/wpmu/jlhoyt/

James Teherani joined the Columbia University's Department of Electrical

Engineering as an assistant professor in July 2015. James received his BS in electrical and computer engineering from the University ofTexas at Austin in 2008, and his MS and PhD degrees in electrical engineering and computer science from the Massachusetts Institute of Technology in 2010 and 2015, respectively. James's research interests include electronic devices, quantum structures, and properties of emerging materials, especially 2D semiconductors and graphene. His work spans the study of fundamental material properties to the optimization of real-world devices.

Bin Zhao
EDS Vice-President of Publications and Products (2013–2015)
Fairchild Semiconductor
Irvine, CA, USA

2014 EDS Paul Rappaport Award

A high priority of the Electron Devices Society (EDS) is to recognize and enhance the quality of papers published in EDS archival literature. Every year, the Society confers its prestigious Paul Rappaport Award to the best paper published in the *IEEE Transactions on Electron Devices*. Among other criteria including technical excellence, an important metric for selection for the award is comprehensive and impartial referencing of prior art.

The winning paper was selected from over 600 articles that were published in 2014. The winning paper is entitled *"Top-Down Fabrication of Epitaxial SiGe/Si Multi-(Core/Shell) p-FET Nanowire Transistors."* This paper was published in the April 2014 issue of the *IEEE Transactions on Electron Devices*, and was authored by Sylvain Barraud, Jean-Michel Hartmann, Virginie Maffini-Alvaro, Lucie Tosti, Vincent Delaye and Dominique Lafond.

The award will be presented at the plenary session of the International Electron Devices Meeting to be held on December 7, 2015, in Washington, DC. In addition to the award certificate, the authors will receive a check for $2,500 to be shared equally among all authors. On behalf of the Electron Devices Society, I would like to congratulate the authors for this achievement. Brief biographies of the authors follow.

Dr. Sylvain Barraud is leading the development of nanowire-based CMOS devices at CEA-LETI. His current research interests include the device physics, the fabrication and characterization of nanowire transistors and single electron nanodevices.

Dominique Lafond joined LETI, in 1978, and now works at the Nanocharacterization Platform (PFNC) as a specialist of electron microscopy. He is currently engaged in the characterisation of semiconductor processes and devices using transmission electron microscopy.

Lucie Tosti has worked on different processing steps for silicon device development, i.e., etching, lithography,

diffusion, etc., during her career. Her research interests include process integration for advanced SOI devices.

Dr. Jean-Michel Hartmann is a CEA-LETI senior scientist. He is specialized in the epitaxial growth and structural characterization of Si/SiGeC heterostructures for nanoelectronics and optoelectronics. He has authored or co-authored close to 400 publications or conference proceedings (h index: 31).

Virginie Maffini-Alvaro received the B.Sc. degree in physics from Heriot-Watt University, Edinburgh, U.K., in 2003. In 2005, she joined CEA-Leti, Grenoble, France, where she is working on advanced CMOS devices with the Innovative Device Laboratory.

Dr. Vincent Delaye, after obtaining his master's degree from "Telecom Saint Etienne", obtained the Ph.D. from

"Grenoble INP" in 2000. Since 2011, he manages the LETI competence center in electron microscopy within the nanocharacterisation platform (PFNC) of MINATEC Campus.

Bin Zhao
EDS Vice-President
of Publications and Products (2013–2015)
Fairchild Semiconductor
Irvine, CA, USA

EDS Members Named Recipients of 2015 IEEE Technical Field Awards

Paul Yu
EDS Awards
Committee Chair
(2013–2015)

Six EDS Members were among the recipients of the 2015 IEEE Technical Field Awards:

Hiroshi Iwai of the Tokyo Institute of Technology, Yokohama, Kangawa, Japan, has been named the recipient of the 2015 IEEE Cledo Brunetti Award. The citation states, *"For contributions to the scaling of CMOS devices."*

Hiroshi Iwai's dedication to pushing the boundaries of integrated circuit scaling broke perceived barriers to enable the continued miniaturization of electronic devices providing higher performance with lower power that are integral to today's mobile electronics. When industry forecasted that complimentary metal-oxide-semiconductor (CMOS) scaling wouldn't go below 1 micrometer due to current leakage and lithography issues, Prof. Iwai provided solutions demonstrating that 25-nanometer (nm) scaling was possible. Among his many innovations, he developed technologies for shallow junctions and optical lithography to allow fabrication of 40-nm gate-length CMOS transistors. He also devised techniques for growing ultra-thin silicon oxide films to overcome leakage issues when using extremely small gate lengths. Overall, Prof. Iwai's contributions demonstrated to industry that sub-50-nm CMOS scaling could be achieved.

An IEEE Life Fellow, Prof. Iwai is a professor with the Tokyo Institute of Technology, Yokohama, Kangawa, Japan.

Masayoshi Esashi of Tohoku University, Sendai, Japan, has been named the recipient of the 2015 IEEE Andrew S. Grove Award. The citation states, *"For developments in micro-electro-mechanical systems (MEMS) used in transportation and industrial electronics."*

A pioneer of micro-electro-mechanical systems (MEMS) technology, Masayoshi Esashi developed ion sensitive FET (ISFET), which was commercialized as pH and CO2 catheters in 1980 and provided an early example of lab-on-a-chip technology. He developed and commercialized many MEMS innovations. His integrated capacitive pressure sensor and MEMS switch for LSI testers are based on wafer level packaging. Dr. Esashi's resonating gyro was extended to yaw rate and acceleration sensors for vehicle stability control (VSC), and his electrostatically levitated rotational gyro, used for vibration measurement in railway cars, enables a more comfortable ride. Dr. Esashi's MEMS-based optical scanner for platform door operation has also improved passenger safety.

An IEEE Member, Dr. Esashi is a professor with the World Premier International Research Center/Advanced Institute for Materials Research (WPI-AIMR), Tohoku University, Sendai, Miyagi, Japan.

Khalil Najafi of The University of Michigan, Ann Arbor, Michigan, USA, has been named the recipient of the 2015 IEEE Daniel E. Noble Award for Emerging Technologies. The citation states, *"For leadership in micro-electro-mechanical systems (MEMS), technologies, and devices and for seminal contributions to inertial devices and hermetic wafer-level packaging."*

The visionary contributions of Khalil Najafi have helped advance the development of micro-electro-mechanical systems (MEMS) technology synonymous with the sensors ingrained in today's automotive, mobile, and biomedical applications. In 1994 he developed the first micromachined vibrating ring gyroscope featuring a high-aspect ratio electroplated nickel process integrated with CMOS electronics. This device was commercialized and became the highest performing automotive gyroscope. His work showing that sensitive multi-axis accelerometers could be fabricated in a system-in-package approach helped the introduction of accelerometers in mobile phones. He also demonstrated wafer-level vacuum encapsulation with a biocompatible glass-silicon package that could remain airtight for 20 years, which paved the way for implantable wireless biomedical devices.

An IEEE Fellow, Dr. Najafi is the Schlumberger Professor of Engineering and Chair of Electrical and Computer Engineering at the University of Michigan, Ann Arbor, Michigan, USA.

Pallab Bhattacharya of the University of Michigan, Ann Arbor, Michigan, USA, has been named the recipient of the 2015 IEEE David Sarnoff Award. The citation states, *"For contributions to near-infrared and visible quantum dot lasers."*

A pioneer of near-infrared and visible quantum dot (QD) laser technology, Pallab Bhattacharya continues to be a leader in developing high-performance lasers impacting optical communication and medical and mobile projector applications. Prof. Bhattacharya was one of the first to demonstrate a room-temperature QD laser in 1996. He then demonstrated the tunnel injection method to enable QD lasers with high-speed modulation and high temperature stability. In 2011, he demonstrated the first nitride-based visible QD lasers with lower threshold than equivalent quantum well lasers. His 630-nm red QD laser is the longest ever emission wavelength achieved with nitride materials. His work on incorporating QD lasers on silicon substrates has important implications for realizing on-chip optical interconnections and signal processing.

An IEEE Life Fellow, Dr. Bhattacharya is a professor of electrical engineering and computer science with the University of Michigan, Ann Arbor, Michigan, USA.

Kaustav Banerjee

Vivek Subramanian

Kaustav Banerjee and **Vivek Subramanian** of the University of California, Santa Barbara, California, USA, have been named the recipients of the 2015 IEEE Kiyo Tomiyasu Award. The citations states, *"For contributions to nano-materials, devices, circuits, and CAD, enabling low-power and low-cost electronics."*

Kaustav Banerjee's and Vivek Subramanian's pioneering use of nanomaterials and radical innovations in devices, interconnects, circuits, and design methods for overcoming power, thermal, and other fundamental challenges in both nanoscale integrated circuits (ICs) and printed electronics have been crucial to the continued scaling of electronic devices, as well as increasing reliability and lowering costs of ICs and large-area printed/flexible electronics. Prof. Banerjee is considered one of the key visionaries behind three-dimensional (3D) IC technology being employed by the semiconductor industry for continued scaling and integration beyond Moore's law, as well as the pioneer behind thermal-aware design methods and tools used in the IC design industry. Prof. Subramanian's innovations to technology have provided pathways for 3D IC fabrication via demonstration of 3D nonvolatile memory and have also driven advances in fabrication techniques for large-area and flexible systems such as displays and RFID tags. Their work is also driving changes in chip architecture, circuit design, design automation, and chip packaging/cooling as well as physical aspects of wafer and display fabrication and interconnection structures. Profs. Banerjee and Subramanian have also made innovative contributions to the development of low-power and low-cost electronic noses and biosensors.

An IEEE Fellow, Dr. Banerjee is currently a professor with the Department of Electrical and Computer Engineering at the University of California, Santa Barbara, California, USA.

An IEEE Member, Dr. Subramanian is currently a professor with the Department of Electrical Engineering and Computer Sciences at the University of California, Berkeley, California, USA.

Paul Yu
EDS Awards Committee Chair
University of California, San Diego
San Diego, CA, USA

2014 IEEE TSM Best Paper Award

HIGH quality scholarship requires technical excellence and also connects the work to the primary references in the field. In this way, the reader advances their knowledge and gains perspective. The Transactions on Semiconductor Manufacturing (TSM) supports these goals by recognizing the best paper chosen by the Associate Editors and reviewers. The winning paper was selected from 59 papers published by the TSM in 2014. The winner is *"Feasibility Evaluation of Virtual Metrology for the Example of a Trench Etch Process"* by Georg Roeder, Sirko Winzer, Martin Schellenberger, Stefan Jank, and Lothar Pfitzner, published in the August 2014 issue of the IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING (10.1109/TSM.2014.2321192). Congratulations to the authors on being selected.

Georg Roeder received the Diploma in material science and the Ph.D. degree in electrical engineering with specialization in control methods for plasma processes, both from the University of Erlangen – Nuremberg, Erlangen, Germany. From 1989 to 1995, he was with the University of Erlangen–Nuremberg. In 1995, he joined the Fraunhofer Institute for Integrated Systems and Device Technology IISB, Erlangen, Germany, where he was involved in the research fields of integrated metrology, advanced process control, and semiconductor manufacturing equipment development, and assessment. He is the coordinator of the VDE/VDI–GMM workgroup 1.2.3 "Deposition and Etch."

Sirko Winzer was born in Berlin, Germany, in 1967. He received the Diploma in mathematics from the Technical University Chemnitz, Chemnitz, Germany, and the Ph.D. degree in numerical mathematics from the Technical University Dresden, Dresden, Germany, in 1991 and 1995, respectively. Since 2004, he has been a System Expert for statistical process control at Infineon Technologies Dresden GmbH in Dresden, Germany.

Martin Schellenberger received the Diploma and the Ph.D. degree, both in electrical engineering in 1998 and 2011, respectively, from the University of Erlangen-Nuremberg, Erlangen, Germany. From 1998 to 2006, he was a Research Assistant at the Fraunhofer Institute for Integrated Systems and Device Technology IISB. Since 2007, he has been Group Manager at Fraunhofer IISB, responsible for equipment and advanced process control. His current research interests include equipment development and optimization for semiconductor processes, manufacturing science solutions for quality control, predictive methods for process control, equipment automation, and productivity enhancement.

Stefan Jank was born in Guben, Germany, in 1977. He received the Diploma (FH) in communication technology from the University of Applied Science Dresden, Dresden, Germany, in 2011. In 1998, he joined Technologies Dresden GmbH in Dresden (former Siemens Microelectronics Center Dresden), Germany, and collected experience in lithography, metrology, and production control. Since 2009, he has been the in charge of advanced process control.

Lothar Pfitzner received the M.S. (Dipl.-Ing.) degree in materials science and the Ph.D. (Dr.- Ing.) degree in electronics engineering, both from the University of Erlangen-Nuremberg, Erlangen, Germany. Since 1985, he has been the Head of the Department of Semiconductor Manufacturing at the Fraunhofer Institute for Integrated Systems and Device Technology IISB in Erlangen, performing research and development in the fields of process development, advanced process control, on-line, and in-situ metrology, integrated vacuum cluster tools, contamination control, and innovative manufacturing methods. Since 1988, he has been a Lecturer on semiconductor manufacturing techniques with the Departments of Mechanical Engineering and Electrical Engineering at the University of Erlangen-Nuremberg, and was promoted to Professor of Microelectronics in 2003.

Anthony J. Muscat,
TSM Editor-in-Chief
Department of Chemical
and Environmental Engineering
University of Arizona, Tucson, AZ, USA

2016 Masters Student Fellowship

Description: One-year fellowships awarded to promote, recognize, and support graduate Masters level study and research within the Electron Devices Society's field of interest: all aspects of engineering, physics, theory, experiment and simulation of electron and ion devices involving insulators, metals, organic materials, plasmas, semiconductors, quantum-effect materials, vacuum, and emerging materials. Specific applications of these devices include bioelectronics, biomedical, computation, communications, displays, electro and micro mechanics, imaging, micro actuators, optical, photovoltaics, power, sensors and signal processing.

Three fellowships will be awarded, with the intention of at least one fellowship being given to eligible students in each of the following geographical regions every year: Americas, Europe/Mid-East/Africa, Asia & Pacific. Only one candidate can win per educational institution.

Prize: US$2,000 and a plaque to the student, to be presented by the Dean or Department head of the student's enrolled graduate program.

Eligibility: Candidate must be an IEEE EDS student member at the time of nomination; be accepted into a graduate program or within the first year of study in a graduate program in an EDS field of interest on a full-time basis; and continue his/her studies at a graduate education institution. Nominator must be an IEEE EDS member and preferably be serving as the candidate's mentor or faculty advisor. Previous award winners are ineligible.

Basis for Judging: Demonstration of his/her significant ability to perform research in the fields of electron devices and proven history of academic excellence in engineering and/or physics as well as involved in undergraduate research and/or supervised project.

May 15, 2016 Submission Deadline

Nomination Package

- Nomination letter from an EDS member who served as candidate's mentor or faculty advisor.
- One letter of recommendation from an individual familiar with the student's research and educational credentials. Letters of recommendation cannot be from the nominator.
- One-page biographical sketch of the student (including mailing address and e-mail address)
- Two-page (maximum) statement by the student describing his or her education and research interests, accomplishments and graduation date. This can include undergraduate, graduate and summer internship research work.
- One copy of the student's transcripts/grades. Please provide an explanation of the grading system if different from the A-F format.

Timetable

- Completed nomination packages are due at the EDS Executive Office no later than **May 15, 2016**
- Recipients will be notified by July 15
- Monetary awards will be presented by the Dean or Department Chair of the recipient's graduate program at the beginning of the next academic term.

Please submit application packages via e-mail or mail:

Email: kellie.gilbert@ieee.org

Mail:
IEEE EDS Executive Office
PhD Student Fellowship Program
445 Hoes Lane
Piscataway, NJ 08854 USA

For more information contact:
edsfellowship@ieee.org

Visit the EDS website:
http://eds.ieee.org/eds-masters-student-fellowship.html

2016 PhD Student Fellowship

Description: One year fellowships awarded to promote, recognize, and support PhD level study and research within the Electron Devices Society's field of interest. The field of interest for EDS is all aspects of engineering, physics, theory, experiment and simulation of electron and ion devices involving insulators, metals, organic materials, plasmas, semiconductors, quantum-effect materials, vacuum, and emerging materials. Specific applications of these devices include bioelectronics, biomedical, computation, communications, displays, electro and micro mechanics, imaging, micro actuators, optical, photovoltaics, power, sensors and signal processing.

It is expected that three fellowships will be awarded, with the intention of at least one fellowship being given to eligible students in each of the following geographical regions every year: Americas, Europe/Middle East/Africa, and Asia & Pacific. Only one candidate can win per educational institution.

Prize: US$5,000 to the student and if necessary funds are also available to assist in covering travel and accommodation costs for each recipient to attend the EDS Governance meeting for presentation of the award plaque. The EDS Newsletter will feature articles about the EDS PhD Fellows and their work over the course of the next year.

Eligibility: Candidate must be an IEEE EDS student member at the time of nomination; be pursuing a doctorate degree within the EDS field of interest on a full-time basis; and continue his/her studies at the current institution with the same faculty advisor for twelve months after receipt of award. Nominator must be an IEEE EDS member. Previous award winners are ineligible.

Basis for Judging: Demonstration of his/her significant ability to perform independent research in the fields of electron devices and a proven history of academic excellence.

May 15, 2016 Submission Deadline

Nomination Package

- Nomination letter from an EDS member
- Two letters of recommendation from individuals familiar with the student's research and educational credentials. Letters of recommendation cannot be from the nominator.
- One-page biographical sketch of the student (including student's mailing address and email address)
- Two-page (maximum) statement by the student describing his or her education and research interests, accomplishments and graduation date
- One copy of the student's under-graduate and graduate transcripts/grades. Please provide an explanation of the grading system if different from the A-F format.

Timetable

- Completed nomination packages are due at the EDS Executive Office no later than **May 15, 2016**
- Recipients will be notified by July 15
- Monetary awards will be given by August 15
- Formal award presentation will take place at the EDS Governance Meeting in December

Please submit application packages via e-mail or mail:

Email: kellie.gilbert@ieee.org

Mail:
IEEE EDS Executive Office
PhD Student Fellowship Program
445 Hoes Lane
Piscataway, NJ 08854 USA

For more information contact:
edsfellowship@ieee.org

Visit the EDS website:
http://eds.ieee.org/eds-phd-student-fellowship.html

Congratulations to the 20 EDS Members Recently Elected to IEEE Senior Member Grade!

Christopher Burton
Barbara De Salvo
Francesco Della Corte
Panagiotis Dimitrakis
Charalabos Dimitriadis
Daniela Dragomirescu
David Dreifus
Thomas Paul Ernst
Oliver Faynot
Mamoru Furuta
Jin-Woo Han
Robert Henderson
Scott Irving
John Jelonnek
Natarajan Krishnaswamy
Pang-Jen Kung
Juergen Lorenz
Despina Moschou
Jun Ohta
Bruce Schmukler

If you have been in professional practice for 10 years, you may be eligible for Senior Membership, the highest grade of membership for which an individual can apply. New senior members receive a wood and bronze plaque and a credit certificate for up to US $25 for a new IEEE society membership. Upon request a letter will be sent to employers, recognizing this new status.

For more information on senior member status, visit: http://www.ieee.org/membership_services/membership/senior/index.html

To apply for senior member status, fill out the on-line application: https://www.ieee.org/membership_services/membership/senior/application/index.html.

You will need to Sign-in with your IEEE account.

Please remember to designate the Electron Devices Society as your nominating entity!

Young Professionals

Reflections from Young Professionals

Sam Vaziri

Our series continues with an interview with Sam Vaziri, an EDS Student Fellowship winner and PhD candidate, studying at KTH Royal Institute of Technology, Stockholm Sweden. As a young professional, his views and perceptions about IEEE and EDS are of significance. Newsletter Editor-in Chief, MK Radhakrishnan has interviewed Sam Vaziri and the excerpts of the interview are given here.

EiC: As a young professional, why do you consider the membership in IEEE and especially in EDS is important?

Sam: There are many reasons why to join EDS. However, personally I think the most important motive is to be connected to this large network of professionals and to be technically updated. Indeed, being an IEEE member facilitates the professional networking which is vital for career development. In addition, IEEE and EDS members are exposed to a variety of resources, technical news, and technical webinars which keep them updated on what is going on in technology and the community. In other words, being an IEEE/EDS member is a professional way to open up so many opportunities.

EiC*:* What was the specific temptation, if any, which made you to join this largest professional organization in the globe at first?

Sam: I believe the senior members and fellows play an important role in presenting this organization to the graduate students and young professionals and to motivate them to join IEEE. For instance, the seniors in our department at KTH Royal Institute of Technology as well as our department head, Professor Mikael Östling who is an IEEE fellow, inspire the students to become an IEEE member and get involved in its professional societies. I think this initial involvement is definitely a great start to become familiar with IEEE and its societies.

Furthermore, as it is the largest professional organization, it gives me the unique opportunity to network with many professionals in my field. In fact, I have had this impression that this is the gate to the professional electrical engineering world.

EiC*:* As a Professional, what are your interests which coincide with EDS activities and your own technical field? How your professional life blends with the services you perform as an EDS member/volunteer?

Sam: I would like to specifically refer to the technical conferences and journals as well as the webinars which are arranged or supported by EDS. In particular, the webinars are great. Well-known scientists giving talks is, indeed, very informative and inspiring.

I, as an engineer, feel the responsibility to be active and play my role in this professional society. I believe EDS has, indeed, provided the platform for its members to be more interactive by serving the society as a volunteer. For me, this has been an honor to serve as a volunteer and I think this is well-aligned with my professional life.

EiC*:* What are your views about the EDS membership and its paybacks? Whether the EDS membership stimulated you at any time in your career growth? If so, how?

Sam: I believe EDS membership is definitely beneficial and valuable. Not only as a communication and information resource, but by providing a platform to get involved its members/volunteers in the society's activities.

Yes, it has always been stimulating and motivating, specifically, during my PhD studies. Now that I am about to graduate in a couple of months, I, as an EDS member, feel the supportive role of the society which gives me encouragement and assurance as I transition toward my future career.

EiC*:* As a YP, how do you consider the ED Society as a focused professional group? What are the changes or developments you would like to see in evolving this professional body as a group devoted to the humanity and its causes?

Sam: I would definitely agree that EDS is a focused professional group with very clear goals. However, the group could perhaps be developed so as to improve connectivity and further involvement by the YP. This could take the form of more direct communication between student members, YPs and senior EDS members to better learn from their experience and shape YP events.

EiC*:* What are your specific suggestions and recommendations for those young professionals who may aspire to join EDS?

Sam: It is a great experience to be a member of ED Society. I suggest to join EDS, and be an active member. This is the best way to communicate with your professional world, to create opportunities and to be more effective.

Sam Vaziri *is currently a PhD candidate in the Department of Integrated Devices and Circuits, at ICT School, KTH Royal Institute of Technology, Stockholm, Sweden. He received his Master of Science in Nanotechnology from KTH in 2011. Previously, he received a Master of Science in Solid State Physics from K.N.Toosi University of Technology, in Tehran, Iran. From the*

master program at KTH to date, his research activities and interests encompass graphene integration technology, novel graphene base hot electron transistors, graphene photodetectors and modulators, graphene-based electromechanical pressure sensors, and graphene inkjet printing. He has published eleven articles in peer reviewed prestigious journals like IEEE T-ED, Nano Letters, and Advanced Materials. He has authored and contributed to more than 10 conference contributions including oral presentations at DRC, ESSDERC and EMRS. His publications have received over 100 citations so far.

EDS-ETC

Engineers Demonstrating Science:
an Engineer Teacher Connection

Report on EDS-ETC Program in Terengganu, Malaysia

By Badariah Bais & Siti Noorjannah Ibrahim

A program called "Fun Time with IEEE EDS Malaysia Chapter" was held August 21, 2015, at Primula Beach Hotel, Kuala Terengganu, with 36 secondary school students from Sekolah Menengah Teknik Kuala Terengganu, participating. The program began with a talk entitled "Life as an Engineer" by Assoc. Prof. Nizar Hamidon from UPM, followed by a talk entitled "Engineering in Turkey" by Prof. Mehmet Ertugrul from Turkey. The program included a session called "Make your own Circuit" where students utilized the donated Elenco Snap Circuits® kits to create 5 electronic circuits. The program ended with the prize giving session to the winners of a quiz.

Organizers and participants of the Educational Program

ED Universidade Estadual de Campinas Student Branch Chapter

By Jacobus W. Swart, University of Campinas (Unicamp)

The ED Universidade Estadual de Campinas Student Branch Chapter in partnership with graduation students, university professors of the University of Campinas (Unicamp) and elementary to high school teachers of Campinas (Brazil), has had great success using the Elenco Snap Circuits® kits donated by the IEEE Electron Devices Society for regional educational outreach.

The Campinas program began in 2013, the period in which our group explored the potential uses of the kits and conducted experiments in different environments, with different types of public. Considering the observed enthusiasm of kids and teenagers while interacting with the kits and the success of our experiences, the present document also presents the opportunity of having Snap Circuits kits being used during the scientific summer camp program hosted every year by Unicamp. Through the regular use of these kits in such activities we aim to reach hundreds of young students yearly.

Since 2013, the ED Student Branch established at Unicamp has built partnerships with graduation students, professors, the IEEE WIE South Brazil Section and elementary to high school teachers to promote demonstration of electronic circuits at the Unicamp Open Doors event for prospective students; Physics classroom activities in a high school; and workshops with children as young as 5 years old. Detailed program descriptions follow.

Assembling their first electric circuit

Physics classroom activities

Electronics Demonstration Sessions at the Unicamp Open Doors Event

Every year, for an entire day, the University of Campinas (Unicamp) opens its doors for visitation to approximately 30,000 pre-university students. Unicamp's School of Electrical and Computer Engineering also opens its laboratories and prepares demonstrations of typical experiments and research projects that are part of engineering students and research scientist's lives. The event is always a great opportunity to promote the interaction of engineering students, scientists and professional engineers with young students that are in the decision path of their future careers.

During August 2014, an entire laboratory was occupied by IEEE ED volunteers to provide demonstrations using the Snap Circuits kits. The objective was not only to demonstrate and talk a little about the underlying concepts of each experiment, but also to let the visitors "put their hands on" the assembled circuits.

Physics Classroom Activities in a High School

From a partnership with a high school Physics teacher, the idea of using Snap

Circuits kits in classroom activities came from the collected perception of students that their science classes typically lack practical activities, turning the classes too abstract and tedious.

The conducted activities embraced teenagers between 15 to 17 years old during their regular Physics classes at school. The activities were guided by the teacher while exploring the "Electricity" subject. Approximately three sessions were performed for each class. In each session, the students were divided into four groups, which was the number of available kits. In total, 60 students participated in the sessions.

A sample of 11 students was selected to check their opinion regarding such classroom activities. When asked about their overall opinion about the kit, 100% of them classified it as "Good". When asked if the activities helped them to understand better the concept of "Electric Circuit", 100% answered "Yes". When asked if the use of the kits sparked their interest in STEM courses, 73% (8 students) answered "Yes", 18% (2 students) answered "No" and 1 subject answered that it was "Indifferent". Finally, two students showed interest to perform further experiments and activities.

Workshops with young children

For young children, "Electricity" is typically shrouded in mystery and danger. These are the perfect ingredients to catch their attention with activities with Snap Circuits kits. From a partnership established with an elementary school, on July, 2015, we used Snap Circuits kits to assemble primitive circuits together with children as young as 5 years old.

Each class was divided into four groups with a maximum of 3 students per group accompanied by a trained adult tutor. The sessions lasted 60 minutes. The first 15 minutes were used to chat about electricity. The volunteers let the children talk about their hypotheses and telling stories about situations in their lives involving electricity. In the following 15 minutes, the session leader asked them to make a drawing as a record of the talk they had. Following, the basic components of the Snap Circuits kits were presented together with some safety warnings and they assembled three circuits with a lamp, the music IC and the fan. All the activities were performed under the careful supervision of an adult tutor. In total, 20 children participated in the sessions.

The amazing aspect of such sessions is the "wow effect" and the excitement of the children when they realize that they built something that plays a song or spins. The adult tutors were responsible for calling the attention to facts like: without batteries the circuit does not work; the switch is responsible for turning "On" and "Off" the experiment; if a circuit component is removed, the electric current does not flow.

Future Project

From our reported experience with the Snap Circuits kits we became encouraged to endeavor new projects with Elementary, Middle School and High School students.

As a future project we plan to use Snap Circuits kits during the scientific summer camp program hosted every year by Unicamp. The project foresees a total of 25 students per session and a same group would interact with the kits in various sessions spread over the summer. Additionally, we plan to expand the offer of workshops in schools around Unicamp.

We conclude that the Snap Circuits kit is a powerful tool to spark curiosity about science and electricity among the youth.

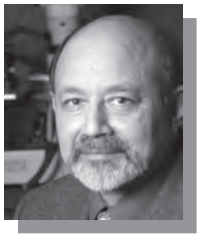
EDS Webinars – Recently Held Events

As part of our commitment to enhancing the value of membership in EDS, we are pleased to invite you to view recently held webinars by these three outstanding members of the EDS community:

To view these newly added webinars and any past events, please visit the EDS Webinar Archive at, http://eds.ieee.org/webinar-archive.html.

Engineering a Sustainable Society with Power Semiconductor Devices Presented by Dr. Jayant Baliga, North Carolina State University

Abstract: Power semiconductor devices are an embedded technology hidden from the eyes of society. Silicon IGBTs are now used in all the major sectors of our economy including transportation, consumer lighting, industrial, medical, and renewable energy generation. The improved efficiency derived from IGBT-based automotive electronic ignition systems has reduced gasoline consumption



Jayant Baliga
North Carolina State University

by 1.5 Trillion gallons over the last 25 years. During this time span, adjustable speed motor drives and compact fluorescent lamps have reduced electricity consumption by 73,000 TWhrs, which is equivalent to eliminating construction of 1366 one-GW coal fired power plants. The social impact includes consumer cost savings of more than $ 23 Trillion and carbon dioxide emission reduction by over 100 Trillion pounds.

This talk reviews the evolution of the IGBT concept and provides examples of its applications in various sectors of the economy. The energy savings and carbon emission reduction enabled by the IGBT will be quantified. In addition, the talk will describe enhancing the performance of silicon power MOSFET products using the charge coupling concept and achieving a quantum leap in power device performance with emerging wide band gap semiconductor based power devices.

Terahertz Electronics for Sensing Applications

Presented by Dr. Michael Shur, Rensselaer Polytechnic Institute

Abstract: Terahertz sensing is enabling technology for detection of biological and chemical hazardous agents, cancer detection, detection of mines and explosives, providing security in buildings, airports, and other public space, short-range covert communications (in THz and sub-THz windows), and applications in radioastronomy and space research. I will review the-state-

Michael Shur
Rensselaer Polytechnic Institute

of-the-art of existing THz sources, detectors, and sensing systems and prospects for novel emerging devices enabling terahertz electronics for sensing applications. Two-terminal semiconductor devices are capable of operating at the low bound of the THz range, with the frequencies up to a few terahertz achieved using Schottky diode frequency multipliers. High-speed three terminal electronic devices (FETs and HBTs) are approaching the THz range (with cutoff frequencies and maximum frequencies of operation above 1 THz and close to 0.5 GHz for InGaAs and Si technologies, respectively). A new approach called plasma wave electronics recently demonstrated terahertz emission and detection in GaAs-based and GaN-based HEMTs and in Si MOS and SOI, including the resonant THz detection. Graphene and 2D materials "beyond graphene" have also emerged as candidates for plasmonic THz detectors, modulators, and emitters. Emerging THz electronic devices have potential to revolutionize THz sensing technology.

Showstoppers and Bottlenecks to Terawatt Solar Photovoltaics

Presented by Dr. Meng Tao, Arizona State University

Abstract: In light of the global energy demands which are predicted to reach

Meng Tao
Arizona State University

46 terawatts by 2100, solar photovoltaics has to be deployed at a scale of tens of peak terawatts in order to meet a meaningful portion of the demands. The enormous scale required creates a number of showstoppers and bottlenecks for solar photovoltaic technologies, which are unprecedented in other semiconductor technologies. Some of the showstoppers and bottlenecks include limited availability of raw materials used in today's solar cells, high energy input for silicon solar cells and modules, recyclability of solar cells and modules, large-scale storage of intermittent solar electricity, and high production and installation costs for solar cells and modules. In this webinar, we will present a quantitative analysis on these showstoppers and bottlenecks for solar photovoltaics under the best scenarios, i.e. the maximum possible wattage from each of the current commercial solar cell technologies. Without significant technological breakthroughs, all the current commercial cell technologies combined would not be able to make a noticeable impact on our energy mix or carbon emission. Based on this analysis, several strategic R&D directions are identified for a scalable and sustainable solar photovoltaic technology.

Chapter News

Chapter of the Year Award

2015 EDS Chapter of the Year Award Winners

The EDS Chapter of the Year Award is presented annually to recognize chapters for the quality and quantity of the activities and programs implemented during the prior July–June period. In 2013, the Society expanded its Chapter of the Year Award to include one chapter in each IEEE Region (1 thru 7, 8, 9 and 10).

The 2015 EDS Chapter of the Year Award winners:

- ED Santa Clara Valley/San Francisco Chapter *(Regions 1-7)*
- ED/AP/MTT/Pho United Kingdom & Ireland Chapter *(Region 8)*
- ED Universidad Santo Tomas (Tunja) Student Branch Chapter *(Region 9)*
- ED Peking University Student Branch Chapter *(Region 10)*

We hope you enjoy reading about your EDS colleagues in the Chapter News articles that follow and how they enhance the member experience for their associates.

Xing Zhou
EDS Vice-President of Regions/ Chapters (2013–2015)
Nanyang Technological University
Singapore

Peking University Student Chapter – Region 10

By Xiaobo Jiang

Ever since its establishment on March 21, 2007, by ten founding student members, the IEEE ED Peking University Student Branch Chapter has been growing steadily, with twenty-five active student members and forty-two alumni members (due to graduation).

Our main objective is to enhance communication and promote harmonious interactions between field experts and young students. We hold more than twenty lectures and seminars every year, including DL talks and MQs. These opportunities of face-to-face communicating with international experts not only provide us technical instructions and inspirations, but also foster our interests and evoke our enthusiasms towards research.

Chair: Xiaobo Jiang (front row, 1st from the left), vice-chair: Weikang Wu (front row, 2nd from the left), Shaofeng Guo (back row, 1st from the left) and other students from the chapter executive committee team

Our secondary goal is to help organizing international conferences or events sponsored by IEEE and provide volunteer opportunities for the students, where we can learn to communicate and coordinate with others, to balance principles and flexibility, and to develop a sense of recognition and cohesion of EDS.

The chapter has been doing the best to achieve these goals for the past years, in line with the tradition of IEEE of advancing technological innovation and global international community. And we believe that the continuous joining of young students will bring new ideas and impetus to this chapter.

IMPORTANT REMINDER to Chapter Members

- CHANGES TO CHAPTER OFFICERS NEED TO BE SUBMITTED TO BOTH IEEE AND EDS
- PLEASE REPORT CHANGES TO IEEE VIA THE VTOOLS.OFFICERREPORTING TOOL
- (ACCESS TO THE TOOL REQUIRES USE OF AN IEEE ACCOUNT)
- TO REPORT OFFICER CHANGES TO EDS, PLEASE SUBMIT A CHAPTER CHAIR UPDATE FORM: https://ieeeforms.wufoo.com/forms/pgu6n1i1ixepnu/

EDS Mini-Colloquium held in Guangzhou, China

The ED Guangzhou Chapter held a mini-colloquium July 30th at the China CEPREI Lab. There were 30 academic staff and graduate students from CEPREI, South China University of Technology, and Xidian University who attended this event. Presentations and invited seminars related to III-V device development and nano-device molding were given by three lecturers, including two Distinguished Lecturers.

Highlight of the seminars included:

- *"Compact Modeling Beyond Device Physics"* presented by Prof. Mansun Chan from Hong Kong University of Science & Technology,
- *"Metamorphic Growth of III-V Devices on Silicon toward Electronic-Photonic Monolithic Integration"* presented by Prof. Kay Mei Lau from Hong Kong University of Science & Technology, Hong Kong, China.

Kong Xuedong
EDS Guangzhou Chair
China CEPREI Lab
Guangzhou, China

Distinguished Lecture Prof. Kay Mei Lau and Prof. Mansun Chan (first row 5th & 6th from left), and attendees of the ED Guangzhou Chapter, on July 30, 2015

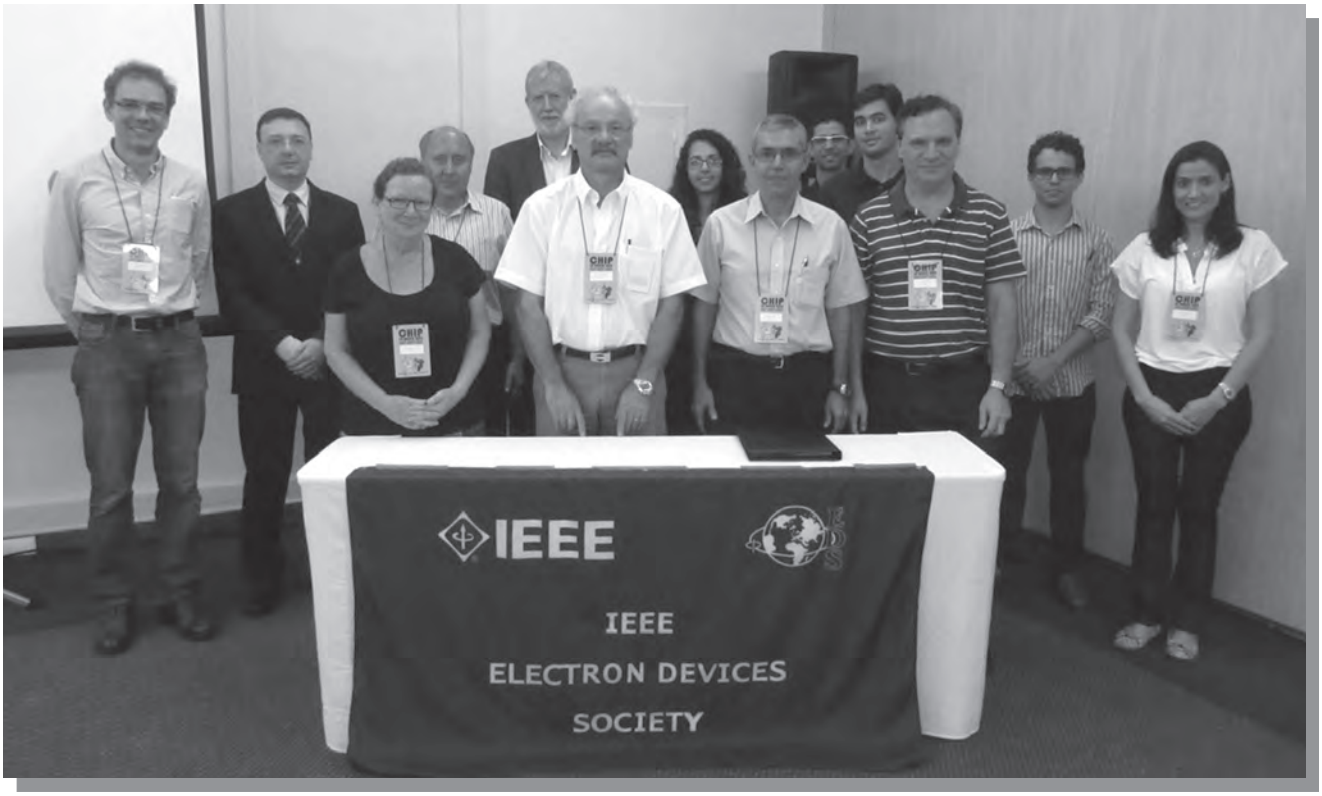
2015 ED Brazil Mini-Colloquium and Report on SBMicro2015

By Marcelo Antonio Pavanello, Michelly de Souza, and Bruna Cardoso Paz

The Centro Universitario da FEI and the IEEE FEI ED Student Branch Chapter organized the 2015 ED Brazil Mini-Colloquium, held in Salvador, Brazil, on September 1st. This Mini-Colloquium was sponsored by the IEEE Electron Devices Society and the Brazilian government research funding agencies CNPq and CAPES. Approximately 60 people attended the Mini-Colloquium, including many EDS members and students.

The program was composed of four distinguished presentations, each one 100 minutes long:

- *"Field Effect Transistor: From MOSFET to Tunnel FET,"* Joao Antonio Martino, University of Sao Paulo, Brazil;
- *"Revisiting Diode and Solar Cell Extraction Methods,"* Adelmo Ortiz-Conde, Universidad Simon Bolivar, Venezuela;
- *"More, Beyond and More than Moore Meeting for 3D,"* Simon Deleonibus, CEA-Leti, France;
- *"Trends and Challenges in Nano-electronic Technologies for New Device Concepts,"* Rita Rooyackers, IMEC, Belgium.



At the 2015 ED Brazil Mini-Colloquium, pictured are the organizers, some of the audience and the EDS Distinguished Lecturers (front row, left to right): Dr. Rita Rooyackers, Dr. Simon Deleonibus, Dr. Adelmo Ortiz-Conde and Dr. Joao Antonio Martino

In the sequence of this Mini-Colloquium and in the same venue, from September 2nd–4th, three EDS Distinguished Lecturers gave Invited Papers at the 30th Symposium on Microelectronics Technology and Devices – SBMicro2015:

- *"CMOS-Compatible Spintronic Devices,"* Siegfried Selberherr, U Wien, Austria;
- *"The smaller the noisier? Low Frequency Noise Diagnostic of Advanced Semiconductor Devices,"* Cor Claeys, IMEC, Belgium;
- *"More Moore and More than Moore Meeting for 3D,"* Simon Deleonibus, CEA-Leti, France.

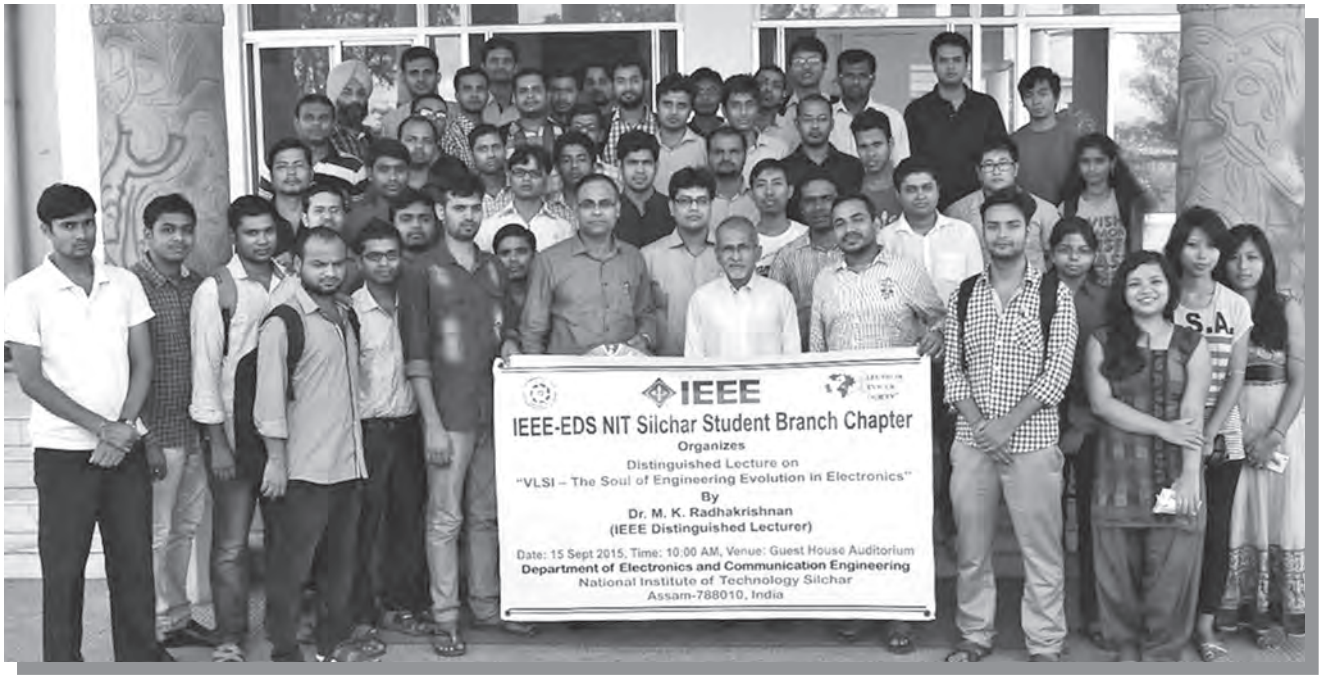
SBMicro is the largest conference in Latin America in the field of micro and nanoelectronics, covering topics such as fabrication technology, sensors, modeling, device characterization and photonics. This year 50 papers were selected by the program committee to be presented both orally and in the Poster Session. About 120 people registered for SBMicro this year. The conference is technically co-sponsored by the IEEE EDS and its proceedings are available in the IEEE Xplore Digital Library.

—Joao Antonio Martino, Region 9 Editor

EDS Distinguished Lectures – ED NIT Silchar Student Branch Chapter

By T R Lenka and Anup Dandapat

The ED NIT Silchar Student Branch Chapter organized two EDS Distinguished Lecture programs by Dr. M.K. Radhakrishnan in September 2015. On **September 15, 2015**, the DL **at National Institute of Technology, Silchar**, was organized in association with the Department of Electronics and Communication Engineering of NIT on the



Participants of DL program at NIT Silchar with Dr. M. K. Radhakrishnan

Participants of DL program at NIT Meghalaya, Shillong, with Dr. M. K. Radhakrishnan

topic *"VLSI – The Soul of Engineering Evolution in Electronics."* At first, Dr. Radhakrishnan gave an overview of the IEEE Electron Devices Society and its membership benefits, followed by the technical talk which covered the history of devices to the latest trends. Challenges in fabrication process of Silicon devices as the dimension shrinks in nanometer regime were discussed. The challenges for 3D IC-integrations were an important part of the talk as well. The talk was attended by about 60 participants including faculty and students both IEEE EDS members and non-members.

The second DL program was at **National Institute of Technology, Meghalaya at Shillong, on September 16th.** The topic of the DL given by Dr. M. K. Radhakrishnan was *"Silicon Nano-Devices – Some of the research trends & Challenges."* The talk emphasized on the limitations in tools to resolve the defects in nanometer scale devices as well as focus on the importance of interface studies related to a number of devices, which dwell mainly on atomic scale interactions. More than 70 participants including faculty members, research scholars and graduate students attended the lecture. The talk concluded with a detailed interaction session on technical aspects as well as discussions on the benefits of ED Society membership.

EDS Distinguished Lecture Held at Xi'an Chapter

By Hongliang Lv

Prof. Albert Chin, from National Chiao-Tung University, Taiwan, visited the ED Xi'an Chapter on September 25, 2015 and delivered an EDS Distinguished Lecture entitled, *"Low-Power and Power-Efficient Green Electronic Devices,"* at Xidian University, Xi'an, China. There were approximately 80 local professionals and students in attendance. This was an excellent lecture including his latest achievements to solve the DC and AC power consumption problems in scaling down devices. The most significant contribution focused on high-κ gate dielectric, such as La_2O_3 and Al_2O_3, to be a solution used for 32~22 nm node CMOS and applied into flash memory to greatly improve its performance. The Ge-on-Insulator CMOS has higher hole and electron mobility that enable the Ge CMOS logic and 3D IC at lower AC power consumption. He also demonstrated a new one-MOSFET device that displays DRAM functions with fast switching, long endurance, low I_{OFF}, and large retention windows with much simpler device process. To save the energy for high-power devices, the high-κ gate dielectric was used in GaN normally-off MOSFET, achieving the highest drive current among all existing power transistors, high breakdown voltage, and very low on-resistance for power/energy saving. The DL received great interest and was highly appreciated, with Prof. Chin answering many valuable questions.

An IEEE EDS DL by Prof. Albert Chin at the ED Xi'an Chapter on September 25, 2015

EDS Distinguished Lectures Organized by ED/SSC Gujarat Chapter

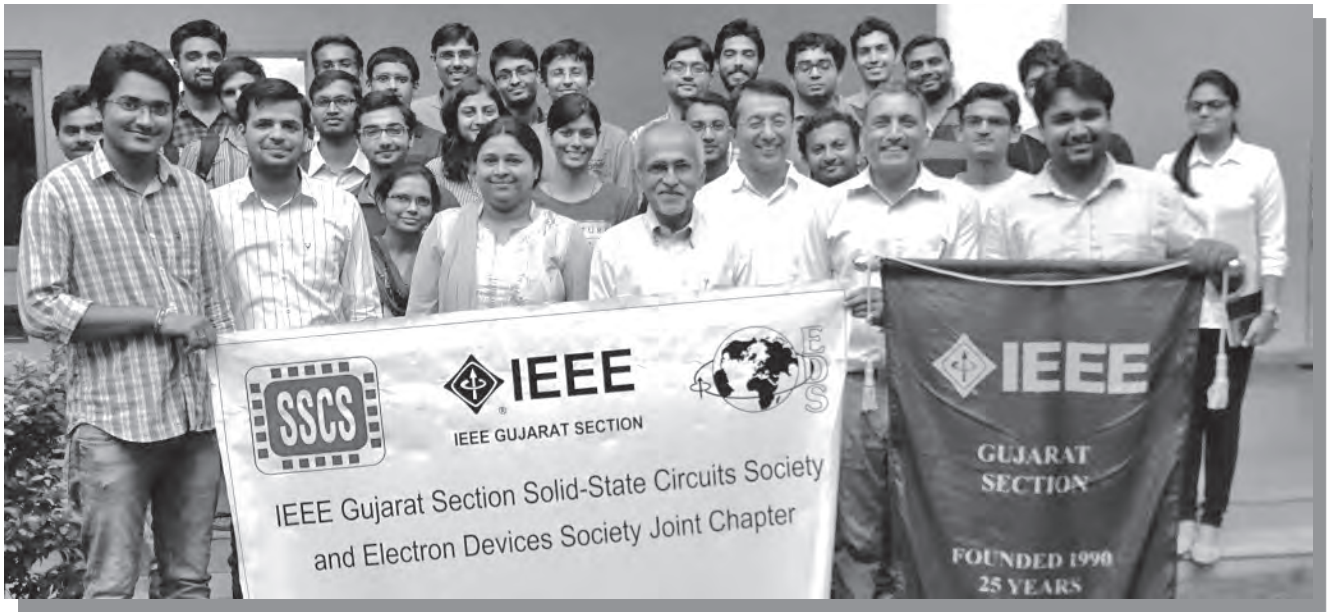
By Ravi Bagree, Chapter Chair

The IEEE ED/SSC Gujarat Chapter in association with IIT Gandhinagar, DA-IICT Gandhinagar and MBICT V V Nagar organized three DL talks by Dr. M. K. Radhakrishnan on October 5, 6 and 7, 2015. During the DL visit, Dr. Radhakrishnan gave many suggestions for various activities for the Chapter to grow in different locations as the geographic spread of the Chapter is hundreds of kilometers wide.

The first DL was held at IIT Gandhinagar on October 5, 2015, and the topic was *"Silicon Nanodevices – Analysis Trends and Challenges."* The talk was attended by more than 40 researchers, faculty and students of the institute including IEEE EDS members and non-members. The major challenges in device analysis as dimensions are in nanometer regime were discussed.

The second DL at DA-IICT Gandhinagar on October, 6, 2015 was entitled, *"VLSI – The Soul of Engineering Evolution in Electronics."* The talk began with an overview of the IEEE Electron Devices Society, its activities and benefits. Later, the speaker presented an interesting insight into the progression of device technology and its transformation from microelectronics to the present stage of nano devices and how it has impacted the evolution of electronics. The objective of the talk was to provide a broad picture of the vast area for study in the field of device technology, where the importance still lies on understanding the fundamentals of device physics, materials and interfaces. The talk was well received by over 35 participants including IEEE members and non-members.

On October 7, 2015, the chapter organized another DL by Dr. M. K. Radhakrishnan on the topic "*VLSI – The*



Speaker and attendees of DL talk at DA-IICT Gandhinagar

DL speaker Dr. M. K. Radhakrishnan with a group of attendees at MBCIT, VV Nagar

Soul of Engineering Evolution in Electronics," at Vallabh Vidya Nagar in association with MBICT. The talk was attended by more than 200 participants including students and faculty members from different engineering colleges of the Vallabh Vidyanagar area. All the participants appreciated the talk as it gave them a new direction to their thought process and made them motivated for their future life as well enlightened their knowledge about various topics in engineering stream.

Report on IEEE-RSM2015 Conference

By Mohd Nizar Hamidon and Badariah Bais

The IEEE Electron Devices Malaysia Chapter organized the 10th IEEE Regional Symposium on Micro and Nanoelectronics (IEEE-RSM2015) at the Primula Beach Hotel, Kuala Terengganu, Malaysia, August 19–21, 2015. The conference was locally co-organized by Universiti Sultan Zainal Abidin (UNISZA). This conference is organized by the ED Malaysia Chapter biannually as a forum for researchers from Malaysia and different parts of the world to share their research findings. RSM2015 had 97 contributed papers for oral presentation in different parallel sessions of Circuits, VLSI & Microwave, Materials & Process, Nanotechnology, MEMS & Microsensors, Materials & Devices and Photonics. More than 80 researchers from 13 different countries attended the conference. The conference opening ceremony as well as the gala dinner was held on the first day where it was officiated by Prof. Dato' Dr. Burhanuddin Yeop Majlis who is the founder Chair of the conference and the Director of the Institute of Microengineering and Nanoelectronics (IMEN), Universiti Kebangsaan Malaysia (UKM).

The first day of the conference had two keynote speakers. Dr. Meyya Meyyappan from NASA Ames Research Centre, who delivered a talk entitled *"Nanotechnology: Development of Practical Systems and Nano-Micro-Macro Integration,"* which was followed by Prof. Dr. Sahbudin Shaari, from the Institute of Microengineering and Nanoelectronics (IMEN) UKM who delivered a speech entitled *"Parallel Injection Current Modulation of Mach-Zehnder Interferometer Modulator on Silicon on Insulator."*

Keynote talks on the second day of the conference started with Prof. Dr. Hirofumi Tanaka, of Kyushu Institute of Technology, Japan delivering the speech entitled *"Brain-like Signal Generating Electric Devices made of Single-Walled Carbon Nanotube and Nanoparticle Complex."* The second talk was by Dr. Hin Tze Yang from Lumileds Malaysia who spoke on *"The Future of Optoelectronics Packaging in High Data Rates Application."*

Participants of RSM 2015 at Kuala Terengganu, Malaysia

Regional News

Europe, Middle East & Africa (Region 8)

MIXDES 2016 Announcement

On June 23–26, 2016, the 23rd International Conference "Mixed Design of Integrated Circuits and Systems" (MIXDES 2016) will be held in Lodz, Poland. The areas of interest are as follows:

- Design of Integrated Circuits and Microsystems
- Thermal Issues in Microelectronics
- Analysis and Modelling of IC and Microsystems
- Microelectronics Technology and Packaging
- Testing and Reliability
- Power Electronics
- Signal Processing
- Embedded Systems
- Medical Applications

The papers submission deadline for the conference is March 1, 2016. We encourage everyone to take part in the conference which is located in Poland's 3rd largest city, a vibrant center of trade, industry, and education.

During the conference, a meeting of the ED Chapter of the Polish Section of IEEE is planned. All people interested in this meeting, in particular all the members of the Polish section of IEEE, are invited to take part in the event. For more information please refer to http://www.mixdes.org.

ED Poland Elections

In September 2015, an election was held to select the new Chair of the Electron Devices Chapter Poland Section. Prof. Andrzej Rybarczyk from Poznan University of Technology was nominated as a chapter chair, Prof. Janusz Zarebski from Gdynia Maritime University remained the chapter's vice-chair and Krzysztof Górecki from Gdynia Maritime University became the chapter secretary. On behalf of all chapter members I would like to congratulate our new officers.

ED/SSC Varna (Bulgaria)

–by Kristina Bliznakova

In September 2015, the International Scientific Conference on Electronics (ET2015) was held in Sozopol, Bulgaria. The event gathers together professionals in the field of electronics, from experienced investigators, industrial professionals and the academic community to students and early stage researchers. To mark the occasion, Dr. Simon Deleonibus, an IEEE EDS Distinguished Lecturer and CEA Research Director in Grenoble, France, was invited by the Bulgarian Joint ED/MTT/AP/CPMT Chapter and the ED/SSC Varna Chapter to present to chapter members and guests. His talk entitled ***"More Moore and more than Moore working on 3D"*** was given before the conference opening ceremony on September 15th.

The event was well attended and was followed by an open discussion about the applications of the presented technologies in high performance computing, information exchanging technologies, and medicine. In his role as IEEE EDS Subcommittee for Regions & Chapters (SRC) Chair of Region 8, Dr. Deleonibus also outlined the benefits of IEEE membership and encouraged the Bulgarian Chapters to continue their work in organizing events in the interest of their members. The chapter would like to thank Dr. Deleonibus for his very enjoyable presentation as well as for taking the time for further discussions, which resulted in the fruitful exchange of knowledge and ideas.

~Mariusz Orlikowski, Editor

ED Dublin/PHO Ireland

–by Patrick McNally

To celebrate the International Year of Light 2015 (IYL 2015), the IEEE Joint Chapter Electron Devices Society (Dublin) / Photonics Society (Ireland) hosted an evening at the UNESCO World Heritage site at Brú na Bóinne, Co Meath, last October. The event consisted of a series of guided tours of the Knowth and Newgrange monolithic sites. The Newgrange site was built around 3200 BC and is considered to be one of, if not the world's first solar observatory.

(left to right) are Kristina Bliznakova (ED/SSC Varna Chapter Chair), Simon Deleonibus and Ivan Buliev

Speakers and attendees at theBrú na Bóinne event (clockwise from bottom left) Prof. Liam Barry (DCU), Dr. Frank Prendergast (DIT), Prof. Tom Ray (DIAS) and a selection of attendees at the reception prior to the talks

The joint chapter would like to express their deep appreciation for the support and efforts of Ireland's Office of Public Works (OPW), which made this event such a huge success. The guided tours were fully subscribed with over 70 people, and these were followed by a reception with food and drinks generously provided by the OPW.

The evening was rounded off with a series of talks by leading Irish experts, Dr. Frank Prendergast (Dublin Institute of Technology), Prof. Tom Ray (Dublin Institute of Advanced Studies) and Prof. Liam Barry (Dublin City University). The speakers explored issues including the influence of light on prehistoric architecture and art, Ireland's historical connections to the use of light in science and technology, and an analysis of the future crucial importance of photonics in our information society.

~ Jonathan Terry, Editor

ED/AES/AP/MTT/GRS/NPS East Ukraine Chapter

–by Nikolay Cherpak, Mikhail Balaban, Ganna Veselovska

In the last few months, members of our chapter took part in several technical meetings organized at O. Ya. Usikov Institute for Radiophysics and Electronics of the National Academy of Sciences of Ukraine (IRE NASU). During the meetings half-hour lectures on electronic devices and signal processing were given.

The Chapter has arranged several meetings in the framework of the "Engineers Demonstrating Science: an Engineer Teacher Connection" (EDS-ETC) program. Our partners are:

- National Technical University "Kharkiv Polytechnic Institute" (www.kpi.kharkov.ua/en),
- National Technical University of Ukraine "Kyiv Polytechnic Institute" (www.kpi.ua/en),
- Open International University of Human Development "Ukraine" (www.en.vmurol.com.ua),
- IEEE Section Ukraine (www.ieee.org.ua)

These events will be organized as a series of two technical meetings for pupils, students, as well as for leading scientists and lecturers of technical Universities of Ukraine. They will be held in Kyiv, capital city, and Kharkiv which is the major scientific, higher education and research center of Ukraine, known as a "smart city" of Eastern Europe.

The technical meetings will be hosted by the Department of Industrial and Biomedical Electronics, National Technical University "Kharkiv Polytechnic Institute" and by the Department of Computer Engineering, Open International University of Human Development "Ukraine", Kyiv. The participants will attend scientific lectures, construct devices according to the proposed schemes and demonstrate industrial and household devices such as alarm systems, a small solar power generator, a FM-radio receiver, etc. We plan such events to be held once a year.

ED/AP/MTT/COM/EMC Tomsk Chapter

–by Oleg Stukach

Siberian Conference on Control and Communications SIBCON

The 11th Siberian Conference on Control and Communications (SIBCON) co-sponsored and organized by the joint EDS Tomsk chapter, took place in Omsk, Russia, on May 21–23, 2015. This biannual meeting was sponsored by the Russian Foundation for Basic Research with technical co-sponsorship of the IEEE Russia Siberia Section.

Papers reporting various scientific topics were presented at the conference. The technical program consisted of contributed papers oral sessions. Various problems related to semiconductor materials, communication and control theory, sensors, and electron devices, with emphasis on both theory and applications, were considered.

The major goal of the conference was to bring together researchers from various fields, in order to present advances in the state-of-the art communication and control theory and technology. The real value of SIBCON is its role as a platform for personal contact and direct information exchange. Unified perspectives in this interdisciplinary field of advanced research were also achieved. The symposium has moreover proved to be particularly rewarding to every participant, in as much as most of them showed interest in

Participants of the SIBCON'2015 Conference

sharing experiences and opinions in a cultural and historical perspective. That brought additional value to the conference which has thus been memorable.

The conference as a whole has demonstrated continuing interest in analysis and control methods for the considered problems. The SIBCON conference has furthermore been a great opportunity to realize a useful and productive bridge between the experienced IEEE members, National Instruments R&D employees, and the new incomers, and a starting point for innovative business ventures and relationships between NI and EDS members.

Omsk, the ancient town of Siberia, witnessed many exciting events in Russian history and still plays a very important role in its scientific and cultural life. The participants have moreover had the opportunity to enjoy the historical sites, as well as the beauties of the city in the famous "Dark Days" season.

We are very pleased that SIBCON conference has already gained the status of a significant and well-known event in Siberia. All information about SIBCON event can be found on our home page: http://chapters.comsoc.org/tomsk/sibcon. We hope you might consider participating at the next SIBCON. Please join us. We are sure you will not be disappointed.

IEEE Republic of Macedonia EDS/IMS/SSCS

–by Goce L. Arsov

Dr. Simon Deleonibus, IEEE Fellow, Region 8 SRC Chair, Chief Scientist of CEA/LETI (France) and IEEE EDS Distinguished Lecturer, visited the University SS Cyril and Methodius in Skopje, on the invitation of the IEEE Republic of Macedonia EDS/IMS/SSCS Joint Chapter Chair, Professor Goce L. Arsov. On September 23rd in the conference room of the Faculty of Electrical Engineering and IT, Dr. Deleonibus gave a DL on More Moore and More than Moore working on 3D, which was organized by the IEEE Republic of Macedonia EDS/IMS/SSCS Joint chapter and co-sponsored by the Republic of Macedonia IES/IAS/PELS Joint Chapter.

Dr. Simon Deleonibus receiving a Certificate of Appreciation from the EDS/IMS/SSCS Chapter Chair, Prof. Goce L. Arsov; University SS Cyril and Methodius in Skopje, September 26, 2015

On the same day the Chapter also organized a DL delivered by Professor Jan Van der Spiegel, Vice President and DL of the IEEE Solid State Circuits Society.

Besides giving the lecture, Dr. Deleonibus was also a keynote speaker at the 12th International Conference on Electronics, Telecommunications, Informatics and Automatics, ETAI2015, held in Ohrid, September, 24–26, 2015.

~Daniel Tomaszewski, Editor

Asia & Pacific (Region 10)

ED University of Chinese Academy of Sciences (UCAS)

–by Lingfei Wang

The Beijing Student Branch Chapter held "The 1st Academic Exchanges Conference for Young Researchers" in UCAS Yanqi Lake campus, August 29–30, 2015. The UCAS is the first graduate school in China with the ratification of the State Council and the newest Yanqi Lake campus employed in 2013, with very beautiful scenery and located near the Asia-Pacific Economic Cooperation

Attendees of event held by the EDS Beijing Student Branch Chapter

(APEC) Summit Venue. It is also very near to the Great Wall, which can be seen from the campus.

The conference included three sections, circuit design, modeling and simulation, devices fabrication, with the teachers of UCAS invited as the section chairs. Eleven student members from the chapter implement their research experiences to achieve targets for better research exchanges, institutional and people linkages across different academic regions. In order to enhance the communication, the students also climbed the Mutianyu Great Wall after the conference was held.

This event is funded by EDS Beijing Student Branch Chapter for the purpose of academic exchanges. It aimed to introduce IEEE EDS, promote communication among members, and lay the foundation for subsequent activities.

Report on the Symposium on Device Technology 2015

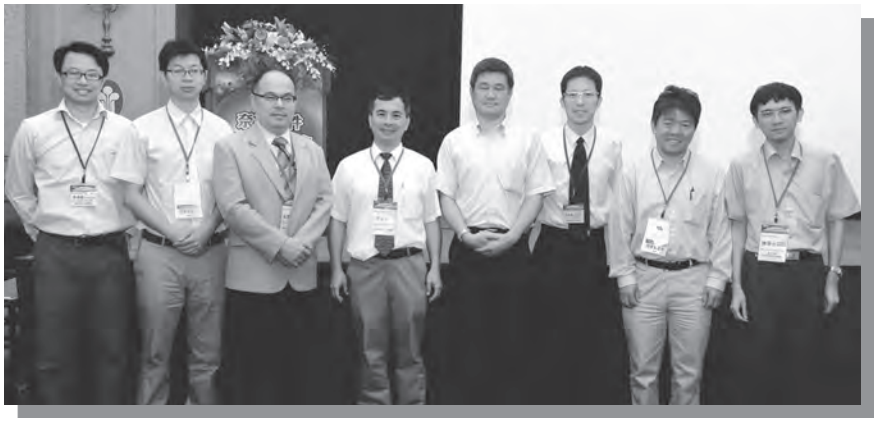
–by Wen-Kuan Yeh

The ED Tainan Chapter co-organized the International Symposium on Nano Device technology (SNDT) at Lakeshore Hotel, HsinChu, Taiwan, September 10-11, 2015. This year's SNDT focused on "The new concept for advanced nano device technology." The following five keynote speakers were invited to give a distinguished lecture:

- *"Recent Evolution of Oxide Semiconductors,"* by Dr. Shizuo Fujita (Photonics and Electronics Science and Engineering Center, Kyoto University, Japan);
- *"Transition Metal Oxides: Insulators, Semiconductors, or Metals?"* by Dr. Ilan Goldfarb (Department of Materials Science and Engineering, Tel Aviv University, Israel);
- *"Growth of InAs-based Quantum Structures and their Electronic Properties Controlled by Strain,"* by Dr. Itaru Kamiya (Toyota Technological Institute, Japan);
- *"STMBE- from the past to the future, "* by Dr. Shiro Tsukamoto (National Institute of Technology, Anan College, Japan); and
- *"Towards Defect-free Heteroepitaxial Crystals on Patterned Si-Substrates,"* by Dr. Hans von Känel (Laboratory for Solid State Physics, ETH Zurich, Switzerland).

Another 15 invited speakers from Taiwan, Japan, and Europe were

Opening ceremony of SNDT 2015: Prof. Wen-Kuna Yeh (center) with all invited speakers and attendees from Taiwan, Japan, and Europe



The invited speakers at SNDT 2015 (left to right) Dr. C. T. Wu (NDL), Prof. Hung-Wei Yen (NTU), Dr. Guo-Wei Huang (NDL), Prof. Wen-Kuna Yeh (Chair of ED Tainan Chapter), Dr. K. L. Lin (NDL), Dr. Hwo-Shuenn Sheu (NSRRC), and Prof. Hou-Guang Chen (ISU)

invited and gave excellent speeches. There were more than 250 attendees, including professors, IEEE members, students and local professionals in Taiwan who attended. For more information on the program, please visit the website at http://sndt.ndl.narl.org.tw/index.php

~Mansun Chan, Editor

ED Malaysia Kuala Lumpur Chapter

–by Badariah Bais & Zubaida Yusoff

IEEE FYP Award 2015

The Chapter participated in the 2015 IEEE Malaysia Final Year Project (FYP) Online Competition held on June 12, 2015 where Track 8 – Micro and Nano Devices was sponsored by the chapter. Lim Weng Chuan from University Tun Hussein Onn Malaysia won the first place with his submission title of "VLSI Design of 4 × 4 Multiplier using Vedic Mathematics and Reversible Logic Gates". Sakina binti Shamim Husain from Universiti Teknologi Malaysia won the second place with her winning entry of "A Computational Study on Electronics &Transport Properties of Armchair Square Graphene Nanoconstriction". The winners received cash prize money, plaques and certificates.

DL Talk at UPM

On August 17, 2015, a DL talk was held at Dewan Taklimat, Tower Building, Faculty of Engineering, Universiti Putra Malaysia (UPM). The speaker was Dr. Meyya Meyyappan from NASA Ames Research Center, United States. He spoke about "Phase Change Memory and Development of Nanoelectronics". About 30 participants attended the talk which was organized

Participants of the DL Talk in UPM

Participants of TPM2015 at UKM

by the Institute of Advanced Technology (ITMA), UPM.

TPM2015

The chapter co-organized the 2nd Topical Meeting on Photonics together with IEEE Photonics Society Malaysia Chapter and Universiti Kebangsaan Malaysia (UKM) in conjunction with "The International Year of Light," which is a global initiative to highlight to the citizens of the world the importance of light and optical technologies in their lives, for their futures, and for the development of society. The event was held on August 17, 2015 at Puri Pujangga UKM. Dr. Meyya Meyyappan, Chief Scientist for Exploration Technology from the NASA Ames Research Center USA, gave the keynote speech entitled "Inorganic Nanowires: Applications in Optoelectronics". Sixteen invited talks were given and the event was attended by about 60 people from academia and industry.

~P Susthitha Menon, Editor

Prof. Perambur S. Neelakantaswamy delivering his lecture at the University of Calcutta

ED NIST Student Chapter, Berhampur, Odisha

–by Ajit Kumar Panda

The IEEE ED NIST Student Chapter organized a technical lecture series on *"Research in Low-power VLSI: Prospective and Approaches"* on September 26, 2015, at the National Institute of Science & Technology, Palur Hill, Berhampur, for the young faculties/researchers to enhance the research activity towards social welfare. Prof. Pandit explained the need of low-power circuits and different approaches to achieve it. He also explained that although industries are moving to new devices like FinFET, many solutions can be achieved by implementing the suitable RTL-level algorithms.

Participants with Professor Soumya Pandit at NIST

ED University of Calcutta Student Branch Chapter

–by Sarmista Sengupta and Soumya Pandit

On July 15, 2015, the chapter organized a technical lecture on *"CMOS Application across THz-spectrum"* by Prof. Perambur S. Neelakantaswamy, Department of Computer and Electrical Engineering & Computer Science, Florida Atlantic University, Boca Raton, USA. He discussed Electromagnetic (EM) wave characterization, EM wave interaction with matter, CMOS geometrical scaling (at THz band), Technology considerations [such as Mobility enhanced FETs, Nano-engineered FETs (graphene FET)]. About 35 students, several Ph.D. research scholars and a few faculty members attended the seminar.

ED Calcutta Chapter

–by Swapnadip De and Soumya Pandit and the

ED Meghnad Saha Institute of Technology Student Branch Chapter

–by Manash Chanda and Swapnadip De

A Technical Talk on *"Tunnel FET"* was delivered by Prof. Santanu Mahapatra, Associate Professor of Nano Scale Device Research Laboratory, Department of Electronic Systems Engineering (formerly CEDT), IISc Bangalore. The talk was organized by the chapter in association with the IEEE Calcutta University EDS Student Branch Chapter, IEEE HITK EDS Student Branch Chapter, IEEE KGEC EDS Student Branch Chapter, IEEE MSIT EDS Student Branch Chapter and the Department of ECE, MSIT on August 7, 2015, and was attended by 66 participants.

An IEEE EDS Distinguished Lecturer by Prof. C. K. Sarkar, Professor of ETCE Department of Jadavpur University was organized by the IEEE EDS Calcutta Chapter in association with the IEEE MSIT Student Branch, IEEE MSIT EDS Student Branch Chap-

Prof. Mahapatra with participants of the Program at MSIT

Prof. C. K. Sarkar with participants of the program

ter and the Department of ECE, MSIT on September 16, 2015. The talk was on *"IC Fabrication"* and it was attended by 67 participants.

ED/SSC Bangalore Chapter

–by Janakiraman

The Chapter organized a mini-colloquium on June 30, 2015, which was inaugurated with **Dr. Souvik Mahapatra** talking about "Macroscopic and Stochastic Aspects of Negative Bias Temperature Instability in Sub 20 nm devices and circuits." The talk dealt with mechanisms of NBTI and it's effect on circuits, which is a crucial reliability concern for modern day state-of-the-art CMOS technologies. This session was followed by

ED/SSC Bangalore Chapter mini-colloquium

Dr. Shanthi Pavan's presentation on *"Low Power Continuous-time Delta Sigma Converters,"* which covered all key aspects of Sigma Delta Analog

and Digital Converters (ADC), from the very basics to advanced concepts. The talk highlighted techniques that are used to reduce power dissipation with interesting design examples of several state-of-the art ADCs.

Final session was by **Dr. Ram Krishnamurthy** *on "Energy efficient circuit technologies for the sub-14nm era: challenges and opportunities."* He presented some of the prominent barriers to designing energy-efficient circuits in the sub-14nm CMOS technology regime and outlined new paradigm shifts necessary in next-generation multi-core microprocessors and systems-on-chip. He has also talked about emerging trends and key challenges in sub-14nm design, including device and on-chip interconnect technology projections, performance, leakage and voltage scalability, special-purpose hardware accelerators and reconfigurable co-processors for compute-intensive signal processing algorithms, fine-grain power management with integrated voltage regulators, and resilient circuit design to enable robust variation-tolerant operation. The mini-colloquium was very well received by the audience including IBM researchers, students and professors from various Bangalore based colleges. The chapter arranged for all the logistics to make the half-day event successful.

ED KGEC Student Branch Chapter, Kalyani

–by Angsuman Sarkar

The IEEE ED Kalyani Government Engineering College SB chapter organized a two-day workshop on *"VLSI & Nanoelectronics,"* August 24–25, 2015, at Language laboratory of Kalyani Government Engineering College, Kalyani, India. The objective of the workshop was to present the topics on Nanoelectronics and Nanodevices,

IEEE EDS members of KGEC during the two-day workshop on "VLSI and nanoelectronics"

IEEE EDS DL Chandan K. Sarkar during his talk at KGEC

to provide greater opportunities for the students and faculty members to be updated with novelties in the modern scientific field, in order to enhance their research activities.

The opening address was followed by a technical talk delivered by Dr. Prasanta K. Basu of University of Calcutta. In his talk on "From Valve to Present Day Nanoelectronics and Beyond," Dr. Basu discussed the basic concepts and evolution of nanoelectronics from valve tubes.

On August 25, 2015, Dr. Chandan K. Sarkar, Chair IEEE, Kolkata section delivered a technical talk on *"Advanced MOS devices,"* in which he discussed advanced nano-scale MOSFET devices and their applications to create a new horizon for electronic industries. The technical talk was followed by hands-on training on "FPGA programming" delivered by Berryline Labs, Kolkata, and was held at the CAD Laboratory, KGEC. This workshop was very well received by more than 65 students and 10 faculty members.

ED National Institute of Technology Silchar Student Branch Chapter

–by T. R. Lenka

The ED NIT Silchar Student Branch Chapter in association with the Department of ECE, NIT Silchar, organized a Distinguished Lecture on "**VLSI - The Soul of Engineering Evolution in Electronics,**" September 15, 2015, by **Dr. M. K. Radhakrishnan**, founder director of *NanoRel*-Technical Consultant Singapore. At first he gave an overview of the IEEE Electron Devices Society and its membership benefits followed by the technical talk on reliability concerns during fabrication process of Silicon-nanodevices, basically the interface physics. The challenges for 3D IC-integrations were an important part of the talk as well which was attended by 56 participants including IEEE EDS members and non-members.

EDS VIT Chapter's one-day training program on September 22nd

ED VIT Chapter

–by Sivasankaran K

The IEEE ED VIT Chapter organized a one-day training program on *"Simulation of Nanoscale Devices using Synopsys TCAD,"* September 22, 2015. Dr. Partha S. Mallick, VIT Chapter Advisor, explained the importance of TCAD in modeling of Nanoscale Transistors and Mr. Sujith, Application Engineer, Eigen Technologies, New Delhi, India, explained the theoretical and practical issues of device design using Sentaurus TCAD. The aim of the training is to create awareness about process and device simulations using Synopsys TCAD.

~Manoj Saxena, Editor

IEEE MCE Conference Education Program

MCE has made the organizing experience easier, more effective and enjoyable by providing learning opportunities for conference organizers of all experience levels, location, Organizational Unit or role.

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If you're interested in the Conference Leadership Workshops, please contact Kevin Hanft, Senior Manager, Conference Organizer Education and Engagement at: <k.hanft@ieee.org> or +1 732 562 5598

EDS MEETINGS CALENDAR

The complete EDS Calendar can be found at our web site: http://eds.ieee.org. Please visit.

2016 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS)	25 Jan - 27 Jan 2016	TU Wien Gusshausstr. 27-29 Wien, Austria
2016 International Conference on Microelectronic Test Structures (ICMTS)	28 Mar - 31 Mar 2016	Mielparque Yokohama 16 Yamashita-cho Naka-ku, Yokohama-shi, Kanagawa Japan
2016 IEEE International Reliability Physics Symposium (IRPS)	17 Apr - 21 Apr 2016	Hilton Pasadena Pasadena, CA, USA
2016 IEEE International Vacuum Electronics Conference (IVEC)	19 Apr - 21 Apr 2016	Monterey Marriott 350 Calle Principal Monterey, CA, USA
2016 International Symposium on VLSI Design, Automation and Test (VLSI-DAT)	25 Apr - 27 Apr 2016	Ambassador Hotel Hsinchu 188 Chung Hwa Road, Section 2, Hsinchu, Taiwan Taiwan
2016 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA)	25 Apr - 27 Apr 2016	Ambassador Hotel Hsinchu Taiwan
2016 International Siberian Conference on Control and Communications (SIBCON) Abstract submission deadline: 11 Feb 2016 Full Paper Submission deadline: 11 Feb 2016 Final submission deadline: 11 Apr 2016 Notification of acceptance date: 11 Mar 2016	12 May - 14 May 2016	Ilya A. Ivanov MIEM HSE 34 Tallinskaya Str. Moscow, Russia
2016 IEEE International Memory Workshop (IMW) Abstract submission deadline: 08 Feb 2016 Full Paper Submission deadline: 08 Feb 2016 Final submission deadline: 15 Mar 2016 Notification of acceptance date: 01 Mar 2016	15 May - 18 May 2016	Paris Marriott Rive Gauche Paris, France
2016 27th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC) Full Paper Submission deadline: 07 Mar 2016 Final submission deadline: 18 Apr 2016 Notification of acceptance date: 08 Jan 2016	16 May - 19 May 2016	Saratoga Springs City Center 522 Broadway Saratoga Springs, NY, USA

2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC) Abstract submission deadline: 08 Jan 2016	22 May - 24 May 2016	Moscone Convention Center 747 Howard St San Francisco, CA, USA
2016 IEEE International Interconnect Technology Conference / Advanced Metallization Conference (IITC/AMC) Abstract submission deadline: 28 Jan 2016 Full Paper Submission deadline: 28 Jan 2016 Final submission deadline: 28 Jan 2016 Notification of acceptance date: 11 Mar 2016	23 May - 26 May 2016	DoubleTree Hotel 2050 Gateway Place San Jose, CA, USA
2016 IEEE 43rd Photovoltaic Specialists Conference (PVSC)	05 Jun - 10 Jun 2016	Oregon Convention Center 77 NE Martin Luther King Jr. Blvd. Portland, OR, USA
2016 28th International Symposium on Power Semiconductor Devices and IC's (ISPSD)	12 Jun - 16 Jun 2016	Zofin Palace Slovanský ostrov 226 Prague, Czech Republic
2016 IEEE Symposium on VLSI Technology	14 Jun - 16 Jun 2016	Hilton Hawaiian Village 2005 Kalia Road Honolulu, HI, USA
2016 Lester Eastman Conference (LEC) Abstract submission deadline: 29 Apr 2016 Full Paper Submission deadline: 02 Sep 2016 Final submission deadline: 02 Sep 2016 Notification of acceptance date: 10 Jun 2016	02 Aug - 04 Aug 2016	Dept. of ECE 19 Memorial Drive West Lehigh University Bethlehem , PA, USA
2016 IEEE Bipolar/BiCMOS Circuits and Technology Meeting - BCTM Abstract submission deadline: 15 Apr 2016 Final submission deadline: 15 Jul 2016 Notification of acceptance date: 17 Jun 2016	25 Sep - 27 Sep 2016	Hyatt Regency New Brunswick 2 Albany Street New Brunswick, NJ, USA
2016 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)	10 Oct - 13 Oct 2016	Hyatt Regency San Francisco Airport 1333 Bayshore Highway Burlingame, CA, USA
2016 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS) Abstract submission deadline: 01 May 2016 Final submission deadline: 15 Jul 2016 Notification of acceptance date: 30 May 2016	23 Oct - 26 Oct 2016	Doubletree by Hilton Austin 6505 N IH 35 Austin, TX, USA

EDS Vision and Mission Statements

Vision Statement
Promoting excellence in the field of electron devices for the benefit of humanity.

Mission Statement
To foster professional growth of its members by satisfying their needs for easy access to and exchange of technical information, publishing, education, and technical recognition and enhancing public visibility in the field of Electron Devices.

Field of Interest
The field of interest for EDS is all aspects of engineering, physics, theory, experiment and simulation of electron and ion devices involving insulators, metals, organic materials, plasmas, semiconductors, quantum-effect materials, vacuum, and emerging materials. Specific applications of these devices include bioelectronics, biomedical, computation, communications, displays, electro and micro mechanics, imaging, micro actuators, optical, photovoltaics, power, sensors and signal processing.

The society is concerned with research, development, design and manufacture related to the materials, processing, technology, and applications of such devices, and scientific, technical, educational and other activities that contribute to the advancement of this field.