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Newsletter

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IEEE

Technical Briefs

Technical Review of the 63rd IEDM Conference

by Barbara De Salvo and Suman Banerjee

The IEEE 63rd IEDM conference (www.ieee-iedm.org) was held December 2–6, 2017 at the Hilton San Francisco Union Square Hotel. Highlights of the conference include the technology platform presentations by Intel and Globalfoundries detailing their competing new 10 nm/7 nm FinFET technology platforms. In addition, AMD President & CEO Lisa Su spoke on multi-chip technologies for high-performance computing. There was also the plenary talk by Nobel Laureate Dr. Hiroshi Amano during Wednesday morning plenary on *"Development of Sustainable Smart Society based on Transformative Electronics."*

Of high interest at the conference was the competing technology platform presentations by Intel and Globalfoundries on FinFETS. FinFETs are high-performance transistors for ultra-dense, powerful integrated circuits (ICs). They have a multi-sided gate surrounding a fin-shaped channel for precise transistor control even at the nanoscale. The most advanced FinFETs in volume production are at the 14 nm/16 nm technology node. FinFETs are a major driver of the continued progress of the electronics industry, and at the IEDM, Intel and Globalfoundries unveiled their forthcoming state-of-the-art integrated FinFET technology platforms.

Intel researchers presented a 10 nm logic technology platform with excellent transistor and interconnect performance and aggressive design-rule scaling. They demonstrated its versatility by building a 204 Mb SRAM having three different types of memory cells: a high-density 0.0312 μm^2 cell, a low voltage 0.0367 μm^2 cell, and a high-performance 0.0441 μm^2 cell. The platform features 3rd-generation FinFETs fabricated with self-aligned quadruple patterning (SAQP) for critical layers, leading to a 7 nm fin width at a 34 nm pitch, and a 46 nm fin height; a 5th-generation high-k metal gate;

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Your comments are most welcome. Please write directly to the Editor-in-Chief of the Newsletter at clilley@uic.edu

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NEWSLETTER DEADLINES

Issue	Due Date
April	January 1st
July	April 1st
October	July 1st
January	October 1st

The EDS Newsletter archive can be found on the Society web site at http://eds.ieee.org/eds-newsletters.html. The archive contains issues from July 1994 to the present.

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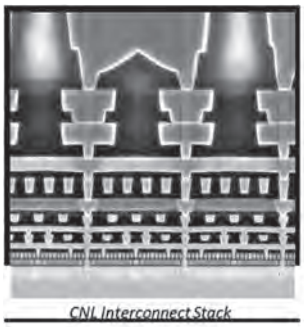
(continued from page 1)

and 7th-generation strained silicon. There are 12 metal layers of interconnect, see Figure 1(a), with cobalt wires in the lowest two layers that yield a 5–10x improvement in electromigration and a 2x reduction in via resistance. NMOS and PMOS current is 71% and 35% greater, respectively, compared to 14 nm FinFET transistors. Metal stacks with four or six workfunctions enable operation at different threshold voltages, and novel self-aligned gate contacts over active gates are employed.

Globalfoundries researchers presented a fully integrated 7 nm CMOS platform that provides significant density scaling and performance improvements over 14 nm. It features a 3rd-generation FinFET architecture with SAQP used for fin formation, and self-aligned double patterning for metallization. The 7 nm platform features an improvement of 2.8x in routed logic density, along with impressive performance/power responses versus 14 nm: a >40% performance increase at a fixed power, or alternatively a power reduction of >55% at a fixed frequency. The researchers demonstrated the platform by using it to build an incredibly small 0.0269 μm^2 SRAM cell. Multiple Cu/low-k BEOL stacks, see Figure 1(b), are possible for a range of system-on-chip (SoC) applications, and a unique multi-workfunction process makes possible a range of threshold voltages for diverse applications. A complete set of foundation and complex IP (intellectual property) is available in this advanced CMOS platform for both high-performance computing and mobile applications.

In addition, the 2017 IEDM featured four Focus Sessions with invited papers from world experts describing the latest research in some of the fastest-growing and futuristic areas of electronics technology. The first focus session was on "3D Integration and Packaging" and featured talks on topics including low-temperature processing, materials, resistance, bandwidth and cost challenges. It also gave an industry perspective on future packaging technologies. As scaling below 7 nm approaches, 3D integration and advanced packaging are key enabling technologies for a host of applications including sensor interfaces, IoT systems, neuromorphic computing, CCD image sensors and on-chip power supplies with integrated magnetics. The session included "*3D Sequential Integration: Application-Driven Technological Achievements and Guidelines*," by Perrine Batude et al, CEA Leti, "*Pixel/DRAM/Logic 3-layer Stacked CMOS Image Sensor Technology*," by Hidenobu Tsugawa et al, Sony Semiconductor Solutions Corp., "*Power Inside - Applications and Technologies for Integrated Power in Microelectronics*," Cian O'Mathuna, University of Cork, "*3D System Package Architecture as Alternative to 3D Stacking of ICs with TSV at System Level*," by Rao Tummala, Georgia Institute of Technology, "*Advanced Packaging Saves the Day! - How TSV Technology Will Enable Continued Scaling*," by Luke England et al, Globalfoundries, "*Advanced Packaging with Greater Simplicity*," by Douglas Yu, TSMC, and "*Towards Cube-Sized Compute Nodes: Advanced Packaging Concepts Enabling Extreme 3D Integration*," by Thomas Brunschwiler et al, IBM Research, Zurich.



Metal Level	Stack A (SoC)	Stack B (HPCs)
1x	M0 - M3	M0 - M3
2x	M4 - M9	M4 - M7
3.2x	M10 - M11	M8 - M11
6.4x	-	M12 - M13
9x	-	M14 - M15
18x	M12 - M13	-
60x	-	M16 - M17

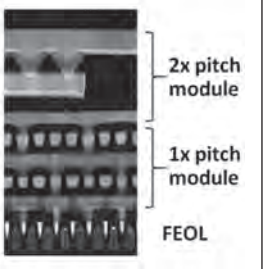


Fig. 1. (a) Micrograph of Intel platform's 12-layer interconnect stack [1]. (b) Micrograph of two BEOL stacks, with the cross-section focused on the 1X and 2X levels from GlobalFoundries [2]

The second focus session was on "Nanosensors for Disease Diagnostics." Today's health-related problems are increasingly complex, multidisciplinary in nature, often ill-defined, and require solutions that cannot be addressed by the medical community on its own. This session reviewed the latest advances in bio-sensing technologies, including the potential of miniaturization in microfluidics to achieve a human organ on a chip; disease models for a "prostate on a chip"; nanoparticle-enabled microscale technologies for the capture of rare circulating tumor cells; a rapid antibiotic susceptibility test system; imaging techniques for in-vivo tissue engineering to track drug penetration; a high-throughput detection system for single bacteria and mammalian cell sizing; and bulk acoustic wave resonators with unique high resonant frequencies >1 GHz to provide a platform for versatile bioactuators. Talks in this session included "*Nanofluidics for Cell and Drug delivery,*" by Mauro

Ferrari et al, Houston Methodist Research Institute, "*Rapid Antibiotic Susceptibility Testing System: Life Saving BioMEMS devices*," by Sunghoon Kwon et al, Quantamatrix and Celemics, "*Development of High Frequency Bulk Acoustic Wave Resonators as Biosensors and Bioactuators*," by Xuexin Duan et al, Tianjin University, "*Encapsulated Organoids and Organ-on-a-Chip for Cancer Modeling,*" by Nathalie Picollet D'hahan et al, CEA, "*A Single Bacterium and Mammalian Cell Analysis by Ionic Current Measurements in a Microchannel*," by Noritada Kaji et al, Nagoya University, "*Tissue Microenvironment and Cellular Imaging*," by Karen Cheung et al, University of British Columbia, and "*Microscale Profiling of Circulating Tumor Cells*" Reza Mohamadi et al, University of Toronto.

The third focus session was on "Modeling Challenges for Neuromorphic Computing." ReRAM is a promising synaptic device that is naturally aligned to brain-inspired cognitive computing applications versus software-based systems implemented in CMOS circuitry that consume higher energy at lower densities. This session had presentations on a comprehensive mix of topics covering critical devices, circuits and applications which included "*Stochastic Synapses as Resources for Efficient Deep-Learning Machines*," by Emre Neftci, University of California at Irvine, "*Attractor Networks and Associative Memories with STDP Learning in RRAM Synapses*," by Elisabetta Chicca et al, University of Bielefeld, "*Energy Use Constrains Brain Information Processing*," by Renaud Jolivet et al, CERN, Switzerland, "*Understanding the Trade-Offs of Device, Circuit and Applications in RRAM-Based Neuromorphic Computing Systems*," by Hai Li et al, Duke University, "*Device and Circuit Optimization of RRAM for Neuromorphic Computing*," by Huaqiang Wu et al, Tsinghua University, "*Challenges and Opportunities Toward Online Training Acceleration Using RRAM-Based Hardware Neural Network*," by Tuohung Hou et al, National Chiao Tung University, and "*Multiscale Modeling of Neuromorphic Computing Devices: From Materials to Device Operations*," by Luca Larcher et al, Universita di Modena e Reggio-Emilia.

The fourth focus session was on "Silicon Photonics: Current Status and Perspectives." Silicon photonics integrated circuits consist of devices such as optical transceivers, modulators, phase shifters and couplers, operating at >50 GHz for use in next-generation data centers. This session describes the latest in photonics IC advances in state-of-the-art 300 mm fabrication technology; integrated nano-photonic crystals with fJ/bit optical links; and advanced packaging concepts for the specialized form factors this technology requires. The talks included "*Developments in 300 mm Silicon Photonics Using Traditional CMOS Fabrication Methods and Materials,*" by Charles Baudot et al, STMicroelectronics, "*Reliable 50 Gb/s Silicon Photonics Platform for Next-Generation Data Center Optical Interconnects,*" by Philippe Absil et al, Imec, "*Advanced Silicon Photonics Technology Platform Leveraging the Semiconductor Supply Chain,*" by Peter De Dobbelaere, Luxtera, "*Femtojoule-per-Bit Integrated Nanophotonics and Challenge for Optical Computation,*" by Masaya Notomi et al, NTT Corporation, and "*Advanced Devices and Packaging of Si-Photonics-Based Optical Transceiver for Optical Interconnection*," by K. Kurata et al, Photonics Electronics Technology Research Association.

There were several other noteworthy talks including a presentation on Lab on Skin™ titled "*Lab On Skin™: 3D Monolithically Integrated Zero-Energy Micro/Nanofluidics and FD SOI Ion-Sensitive FETs for Wearable Multi-Sensing Sweat Applications,*" by F. Bellando et al at EPFL/Xsensio. Hundreds of biomarkers can be tracked in human sweat, and wearable sweat sensors may play a key role in precision healthcare and lifestyle applications. A team led by EPFL reported a novel fully integrated, low-power, multi-sensing smart system that can passively collect sweat and measure its biomarker content in real-time. Called Lab on Skin™, it uses arrays of functionalized sensors to simultaneously detect pH, Na+ and K+ concentrations in sweat. Built using wafer-level techniques, it features the 3D heterogeneous integration of ion-sensitive, fully depleted SOI (FD SOI) FETs and micro/nanofluidic sensing channels created with the commonly used SU-8 negative photo resist. Unlike previous sweat sensors, which required large amounts of sweat, the new system exploits capillary forces to provide zero-energy pumping of tiny amounts into the channels for analysis. The system demonstrated excellent sensitivities (52mV/dec for pH and −37 mV/dec for Na+ sensors) and ultra-low power consumption (<50 nWatts/sensor). It features the integration of miniaturized Ag/AgCl quasi-reference electrodes, paving the way for use in fully wearable flexible patches or as plug-in modules in wrist-based devices.

Additionally, there was a presentation on high-performance devices on paper by S. Park and D. Akinwande at the Univ. Texas-Austin titled "*First Demonstration of High Performance 2D Monolayer Transistors on Paper Substrates*." Paper is a thin, inexpensive and ubiquitous material, making it attractive as a possible substrate for flexible electronic devices for use in nanoelectronic systems, sensors and Internet of Things (IoT) applications. Two-dimensional (2D), or monolayer, semiconductors like graphene and molybdenum disulfide (MoS_2) are attractive potential matches for paper substrates because they are thin and also strong enough to bend without damage, up to a point. Univ. Texas-Austin researchers discussed at the IEDM how they built a variety of high-performance two- and three-terminal graphene and MoS_2 devices on paper for the first time ever. They first coated the paper with polyimide to make

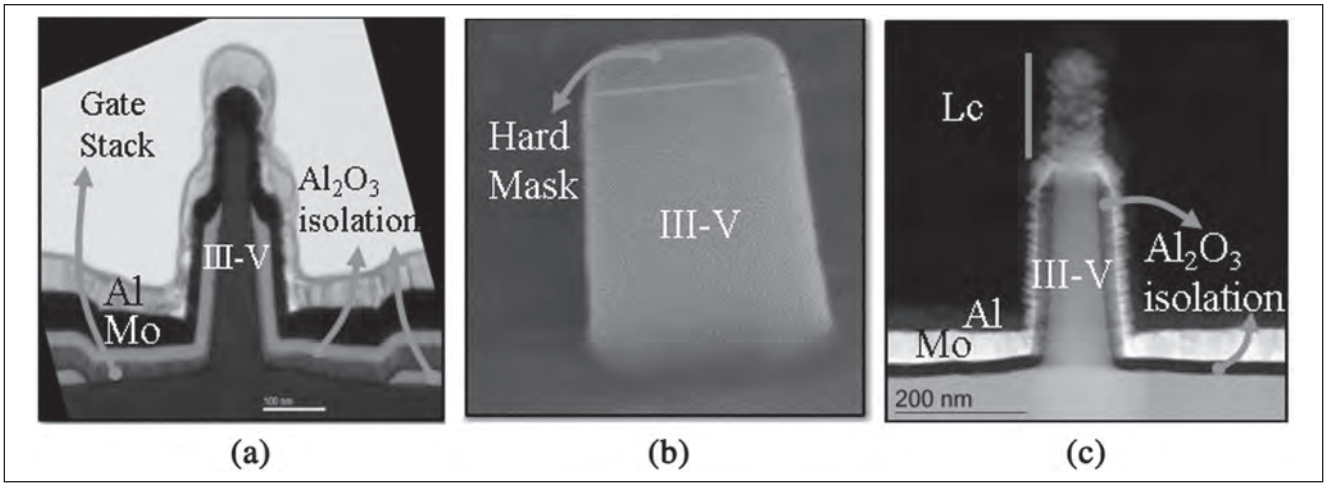


Fig. 2. (a) Electron microscope micrograph with view across the width of a 37 x 480 nm single nanosheet FET device. (b) Electron microscope micrograph of a single vertical nanosheet after dry etch. (c) Electron microscope micrograph of a vertical nanowire resistor after transmission line measurement (TLM) fabrication. [3]

it extremely smooth, and to prepare it for the wet transfer of the high-quality large-area-synthesized 2D films. The graphene or MoS_2 devices were fabricated via CVD. A record 25 GHz cutoff frequency for a graphene device on a paper substrate was demonstrated, and device performance remained high even when the paper was rolled into a 2" diameter roll. Further, it was stable even when the paper was cycled >1,000 times to a bending strain of 0.6%.

A team led by Nanjing University reported on the first steep subthreshold-slope MoS_2 devices ever demonstrated. The paper titled "*Negative Capacitance 2D MoS2 Transistors with Sub-60mV/dec Subthreshold Swing over 6 Orders, 250 μA/μm Current Density, and Nearly Hysteresis-Free*," by Z. Yu et al, Nanjing Univ./Fudan Univ./Hong Kong Polytechnic Univ. They fabricated a negative capacitance FET structure using ferroelectric $HfZrO_x$ (HZO)/AlO_x as the gate stack. The devices exhibited an ultra-low subthreshold swing of 23mV/dec (with sub-60mV/dec for over six orders of magnitude). There was negligible hysteresis, a small threshold voltage loss (<0.4 V) and a high I_{on}/I_{off} ratio ($>10^9$). This all makes the negative-capacitance MoS_2 FET a potential candidate for future ultralow-power applications (sub-0.5 V operation). There was also a presentation on the record performance from vertical III–V nanowire/nanosheet MOSFETs titled "*Computational Study of Gate-Induced Drain Leakage in 2D-Semiconductor Field-Effect Transistors*," by J. Kang et al, Univ. California-Santa Barbara/Micron Technology. High-mobility materials such as III–V compound semiconductors may be well-suited for transistor channels in future low-power logic applications. A vertical architecture is attractive for III–V devices because they normally suffer from higher off-currents than silicon given their narrower bandgaps, and so the ability to relax the gate-length scaling requirement – as can be done in a vertical configuration – is beneficial. A team from KU Leuven and Imec built InGaAs vertical nanowire and vertical nanosheet MOSFETs using a top-down VLSI-compatible fabrication technique. These experimental devices, shown in Figure 2, demonstrated the best performance ever reported for vertical III–V devices – I_{on} = 397 μA/μm and peak transconductance (Gm) = 1.6 S/μm at Vds = 0.5 V – along with impressive subthreshold slope performance (SS = 63 mV/decade). The performance was driven by excellent electrostatic control, an improved process integration scheme versus earlier work, a low-damage dry etch process and optimized surface treatment. The fabrication process did not compromise reliability compared to similar gate stacks, and the researchers say that reducing access resistance and especially contact resistance to the source/drain regions would further improve performance.

In addition the excellent sessions at this year's conference, there were also 90-Minute Tutorials on emerging technologies presented by leading technical experts in each area, with the goal of bridging the gap between textbook-level knowledge and cutting-edge current research. There were day-long Short Courses to provide the opportunity to learn about important developments in key areas, and they enable attendees to network with the industry's leading technologists.

Finally, the plenary sessions included the following presentations: "*Driving the Future of High-Performance Computing*," by Lisa Su, President & CEO, AMD, "*Energy-Efficient Computing and Sensing: From Silicon to the Cloud*, Adrian Ionescu, Professor,

EPFL, "*System Scaling Innovation for Intelligent Ubiquitous Computing*, Jack Sun, VP of R&D, TSMC, and "*Development of a Sustainable Smart Society by Transformative Electronics*, Hiroshi Amano, Professor, Nagoya University. Dr. Amano received the 2014 Nobel Prize in Physics along with Isamu Akasaki and Shuji Nakamura for the invention of efficient blue LEDs, which sparked a revolution in innovative, energy-saving lighting.

In addition, jointly sponsored by IEDM and IEEE EDS Women in Engineering, this year's Entrepreneurs Lunch featured Courtney Gras, Executive Director for Launch League, a local nonprofit focused on developing a strong startup ecosystem in Ohio. The moderator was Prof. Leda Lunardi from North Carolina State University. Gras is an engineer by training and an entrepreneur by nature. After leaving her job as a NASA power systems engineer to work on her own startup company, she discovered a passion for building startup communities and helping technology-focused companies meet their goals. Named to the *Forbes* "30 Under 30" list in 2016, among many other recognitions and awards, Gras enjoys sharing her stories of founding a cleantech company with young entrepreneurs. She speaks on entrepreneurship, women in technology and clean energy at venues such as TEDx Budapest, the Pioneers Festival, and the IEEE WIE International Women's Leadership Conference.

References

[1] C. Auth et al, Intel, "*A 10 nm High Performance and Low-Power CMOS Technology Featuring 3rd-Generation FinFET Transistors, Self-Aligned Quad Patterning, Contact Over Active Gate and Cobalt Local Interconnects*," 2017 IEDM.

[2] S. Narasimha et al, Globalfoundries, "A 7 nm CMOS Technology Platform for Mobile and High-Performance Compute Applications," 2017 IEDM.

[3] S. Ramesh et al, KU Leuven/Imec, "*Record Performance Top-down In0.53Ga0.47As Vertical Nanowire FETs and Vertical Nanosheets*," 2017 IEDM.

Edited by Carmen M. Lilley

Upcoming Technical Meetings

2018 IEEE International Reliability Physics Symposium (IRPS)

The International Reliability Physics Symposium (IRPS) is the world's premier forum for leading-edge research addressing developments in the Reliability Physics of devices, materials, circuits, and products used in the electronics industry. IRPS is the conference where **emerging reliability physics challenges** and possible solutions to achieve realistic End-of-Life projections are first discussed. This year, the IRPS will be held at Hyatt Regency San Francisco Airport, Burlingame, CA. Scheduled for March 11–15, 2018, the IRPS will commence with two full days of tutorials and year-in-review on Sunday, March 11th and Monday, March 12th. This will be followed by three days (Tues–Thurs, March 13–15) of plenary and parallel technical sessions presenting original, state-of-the-art work.

The IRPS draws presentations and attendees from industry, academia and governmental agencies worldwide. No other meeting presents as much leading work in so many different areas of reliability of electronic devices, encompassing silicon device, non-silicon device, process technology, nanotechnology, optoelectronics, photovoltaic, MEMS technology, circuits and systems reliability including packaging.

IRPS 2018 is soliciting increased participation in the following areas: reliability of wide bandgap semiconductor power devices, circuit aging, consumer electronics, reliability of 2D NAND flash replacement technologies, 2.5D & 3D packaging. We are also emphasizing **self-heating effects** on transistors and circuit aging and **systems reliability** comprehending complex applications including chip-package interactions and packaging. In addition, we are strongly promoting all reliability work on **photovoltaics**. Furthermore, three focus sessions composed of worldwide recognized reliability experts will be organized on the following topics: 1) **wide bandgap semiconductors**: reliability issues and standardization status; 2) **2.5D/3D packaging reliability**; 3) **System level reliability**.

The conference hotel is conveniently located near the San Francisco Airport, situated between downtown San Francisco and near many Silicon Valley industries. It is the perfect starting point to explore the many things to do in the Bay Area, including the Golden Gate Bridge, Cable Cars, Alcatraz Island, Lombard Street, shopping in Union Square, dining at Fisherman's Wharf, and many museums, theaters and clubs.

For 56 years, IRPS has been the premiere conference for engineers and scientists to present new and original work in the area of microelectronics reliability. Drawing participants from the United States, Europe, Asia, and all other parts of the world, IRPS seeks to understand the reliability of semiconductor devices, integrated circuits, and microelectronic assemblies through an improved understanding of both the physics of failure as well as the application environment. IRPS 2018 will offer a full slate of tutorials, evening panel debates and workshops, invited plenary talks in addition to an **outstanding technical program.**

Other opportunities at the symposium include:

- Two-Day **Tutorial Program** (Sunday-Monday March 11–12). The IRPS tutorial program is a comprehensive two-day event designed to help both the new engineer and experienced researcher. The tutorial program contains both beginner and expert tracks, and is broken down into topic areas that allow the attendee to participate in tutorials relevant to their work with a minimum of conflicts between subject areas.
- **Year in Review** Session (Monday March 12). These seminars provide a summary of the most significant developments in the reliability community over the past year. This serves as a convenient, single source of information for attendees to keep current with the recent reliability literature. Industry experts serve as the "tour guide" and save you time by collecting and summarizing this information to bring you up to date in a particular area as efficiently as possible.
- Evening **Poster Session**. The poster session will provide an additional opportunity for authors to present their original research. The setting is informal and allows for easy discussion between authors and other attendees.
- Evening Session **Workshops**. These workshops enhance the symposium by providing the attendees an opportunity to meet in informal groups to discuss key reliability physics topics with the guidance of experienced moderators. Some of the workshop topics are directly coupled to the technical program to provide a venue for more discussion on the topic.
- **Vendor Exhibits**. Held in parallel with the technical sessions, the equipment demonstrations provide a forum for manufacturers of state-of-the-art laboratory equipment to present their products. Attendees are encouraged to visit

the manufacturers' booths for information and demonstrations.

- **IRPS Paper Awards**. IRPS bestows awards for Best Paper, Outstanding Paper, Best Poster and Best Student Paper. The Best Paper author is typically invited to present the paper at ESREF in October.

For registration and other information, visit the IRPS-2018 home page at http://www.irps.org/ .

The IRPS committee members look forward to seeing you in March.

Elyse Rosenbaum
2018 IRPS General Chair
University of Illinois

Cathryn Christiansen
2018 IRPS Publicity Chair
GlobalFoundries

2018 IEEE International Memory Workshop (IMW)

The 10th International Memory Workshop (IMW) will be held at the Westin Miyako Hotel in Kyoto, Japan from May 13–16, 2018. The history of the IMW dates back to the NVSMW (Nonvolatile Semiconductor Memory Workshop) which began in 1976 and which later merged with the ICMTD (International Conference on Memory Technology and Design) to become the IMW. The IMW is sponsored by the IEEE Electron Devices Society and meets annually in May. The workshop covers all types of memory technology, is focused on advancing innovation in memory technology, and is organized in a way that provides excellent professional development and networking opportunities for attendees.

The IMW is the premier international forum for both new and seasoned technologists having diverse technical backgrounds to share and learn about the latest developments in memory technology with the global community. The scope of workshop content ranges from new memory concepts in early research to the technology drivers currently in volume production as well as emerging technologies in development. Topics include new device concepts, technology advancements, scaling and integration, circuit design and reliability, as well as emerging applications. Consistent with the increased importance of memory system architecture and integration, the workshop also includes increasing coverage of the systems in which memories are deployed and the co-evolution of memory technology along with memory systems and applications.

The IMW is the preeminent forum covering the latest developments, innovations, and evolving trends in the memory industry. Typical workshop attendance exceeds 250 attendees and the technical program begins with a full day short course given by distinguished experts that provides an excellent professional development opportunity for both new and experienced technologists. The single-track technical program spans three days and also includes an evening poster session for informal technical discussion with authors as well as a panel discussion where experts discuss and debate a current hot topic. The 2017 workshop included invited talks from industry and research leaders from Google, Samsung, Micron, IBM, Western Digital, Panasonic, Everspin, CEA LETI, and IMEC. Highlights included experts sharing their insights and perspectives on a variety of topics including the 3D NAND scaling horizon and potential successors, the latest breakthroughs in RRAM/MRAM/FRAM technology, low latency persistent memory architecture, the prospects of emerging NVM to accelerate deep learning, and the transformative impact that machine intelligence in consumer products is having on memory architecture. The technical program is organized to maximize networking opportunities and facilitate open information exchange among workshop contributors, committee members, and attendees. The program schedule includes ample time dedicated to social events including provided refreshment breaks, a workshop luncheon, and an evening banquet. This year's workshop is located near downtown Kyoto, with opportunities to explore the local temples, shrines, palaces, gardens, and museums that are part of the area's rich cultural heritage.

On behalf of the organizing committee, I cordially invite you to attend the 2018 IMW to participate in the advancement of innovation in the rapidly evolving memory industry. For additional information, including the call for papers, key dates, abstract submission instructions, registration information, and technical program details, please visit the IMW website for the latest updates: http://www.ewh.ieee.org/soc/eds/imw/. I look forward to seeing you in Kyoto this May.

Randy Koval
2018 IMW Publicity Chair
Intel

EDS Board of Governors/Forum December 2 and 3, 2017 Meetings Highlights

Simon Deleonibus
EDS Secretary

The 2017 end of the year EDS Board of Governors/Forum meetings were held in San Francisco, California on December 2nd and 3rd, 2017. Since 2016, this edition of the annual series is held in San Francisco in the same premises as IEDM at the Hilton Union Square. The whole Forum is indebted to the EDS Office members for the wonderful organization of the meetings. This year was marked by the celebration of our very prestigious members Gordon Moore and Simon Sze, on Sunday evening and during the opening session of the IEDM on Monday December 4th.

Yearly updates by the publications and newsletter, education, membership, regions & chapters and conferences and technical activities Standing Committees were given on Saturday, December 2nd and reported by the chairs on Sunday, December 3rd at the Forum meeting. December is also time for the awards, nominations and elections, as well as the Fellow committees to report on the past year results. Officers and members-at-large elections took place at the end of the December 3rd Forum meeting, with the presence of voters only. The ExCom held its meeting on Saturday evening. Significant highlights are given hereafter.

A first report was given by the President on the collection of surveys from our Technical Committees & Conferences, Region and Chapters and Publications Committees supporting our 5-year plan. More discussions will be necessary in the coming months before submitting our 5-year plan to IEEE, for its approval in May 2018.

During Saturday's Committees meetings and Sunday's Forum, we had fervent discussions on the future of EDS policies. Our Standing and Technical Committees efforts constantly need to cover all aspects of knowledge dissemination by taking coordinated and coherent approaches. There are important questions that need to be addressed regarding: 1) our publications leadership in EDS core business, the new web based contents and accessibility of our highlights to the general public; 2) strengthening our conferences by continuing the stimulation of EDS excellence policy and enhanced collaborations between our Standing and Technical Committees; 3) our Education, R&C and Membership policies to attract interest of the younger generations (students or professionals) and female population towards the field of electron device engineering, as well as to develop new education tools; 4) the increasing use of mobile access to 100% web based services to our members, including social media; 5) the efficiency and transparency of our governance; 6) outreach and strategic alliances with other societies, particularly in establishing roadmaps.

The BoG and Forum membership reached a quorum at the meeting. The list of 7 approved motions is given at the end of this article. One motion regarding the revision of Bylaws section 10.4 will be voted by email. The main highlights are reported hereafter.

Newsletter: The newly assigned EDS Newsletter Editor in Chief, Carmen Lilley, has taken full service with the July issue. A strategy to enhance the web based version of the Newsletter, while enhancing the paper version at reduced cost was proposed to the Oversight Committee and Forum. Both bodies approved the proposed path: a motion was approved by the Forum and the various Newsletter formats will be accessible by mid-2018. More changes will be brought to the Newsletter organization: the Forum adopted the definition of two new Associate Editor positions openings to enhance the Technical Content and Professional Development sections. The Technical Content Associate Editor will stimulate the publication of tutorial papers- not in competition with our peer review journals – to widely disseminate the society's updated knowledge. This person will drive increased interactions with our Technical Committees to suggest technical articles subjects. A first initiative has been launched following the MQ "Marvels in Microelectronics" held in Stuttgart in September 2017. The Professional Development Associate Editor will interact mostly with Young Professionals, Women in Engineering, Education Committees, IEEE Collabratec and other member services.

Publications: The initiatives to revamp our journal covers by the means of editor's picks has received positive feedbacks despite the fact that changes are susceptible to creating some controversy. In 2017, we observed a substantial increase in the number of submissions to our journals, while maintaining the selection rates steady and good progression of our bibliometric indices (Impact factors *EDL*: 3.048; *TED*: 2.605; *JEDS*: 3.141). The time from submission to e-publication has decreased noticeably down to 3.6 weeks for *EDL*, 12.7 weeks for TED and remain steady (11.8 weeks) for *JEDS*. These

results are due to all the volunteers and staff efforts to improve our publication service efficiency and outreach. Our bylaws fixing our paper charge strategy (Bylaws section 10.4) need to be updated due to the Society's hybrid policy (volunteer or open access). The page charge influence on our journal's impact factors in the general context of IEEE and the race against competition, without sacrificing our journal's reputations, should not be the only metric to measure their quality. Important aspects such as the type of content and the access to 100% mobile-based publications will be other hot topics in the future. The most efficient way to address plagiarism was questioned through the direct contribution of human intervention: JEDS will dedicate a full-time editor to address this question. The evolution of the type of content (including modifications in our web versions) is among the hot topics to address for our future differentiation. The place of special issues and their relevance in each of our journals was discussed to avoid any internal competition between EDS journals and foster complementarity: *TED* focuses on topical issues whereas JEDS will handle conferences special issues.

Conferences and Technical Committees: The interactions between our 14 Technical Committees, Conferences organizations and the Publication and Products Committee are fruitful through the web and conferences calls. The meeting on Saturday gathered several working groups around the technical committees. These discussions effectively came with outputs for topical and special journals issues ideas or plenary talks. On the financial viewpoint most of our conferences are trying to doing well without sacrificing quality. Updates on our flagship conferences (IEDM, PVSC, VLSI Technology and Circuits Symposia), well established (IVEC, and now 100% sponsored ESSDERC) and recently started (EDTM, ICEE) meetings are good indicators of the vitality in this sector. However, EDS must continue the efforts in avoiding strong overlap and unfruitful competition in the future between newly established conferences.

Regions and Chapters: The number of Chapters has been increasing up to 208. One of our biggest efforts is dedicated to keeping our chapters on the way to sustainability. Reviving chapters and obtaining regular reports is an important task including not only the EDS Office but also the SRC (chairs and co-chairs). The chapters' subsidy is linked to their reporting. The formation of student chapters is strongly dependent on proper faculty approval. These measures contribute in encouraging chapters durability. Our MQ program gaining in popularity will certainly request some evaluation method as far as the meeting and speakers are concerned. As a matter of fact, the number of Distinguished Lecturers has increased to 105, reaching the 1% maximum limit of our members. The method to select new DLs has been discussed among the different bodies and will be deployed soon. Their main guideline was unanimously to maintain a high quality among our DLs, either in the nomination/endorsement process and in the operation of our program.

Education: Our EDS-ETC and EDS Institute programs are expanding and gaining in popularity. As an example, in 2016–2017, 9,744 high school students (50% male, 50% female) participated to our EDS-ETC program in all regions. These programs are continuing their expansion. They will be excellent vehicles in the future to extend electron device popularity to all ages and levels of education from junior high school to higher education levels. Our webinars are including more and more topics from the Diversification domain. Other activities and initiatives such as the Student Fellowships, "Discover the Creative Engineer in You", "Young Engineer Drive" are piloted by the Education Committee with good matching of objectives with our Regions & Chapters and Membership Committees. To recognize the great dedication to the success of these missions, the Education Award Committee has designated Mansun Chan as recipient of the 2017 Education Award.

Membership: Our membership growth by 3% in one year has been confirmed to 10,440 members (as of November 2017). Developing strategies to overcome these numbers will be a major challenge for EDS in the next 5 years. Our recruitment methodology certainly needs to be updated even though membership fee subsidy could help in bringing in new members. The question of future EDS members profile has to certainly be addressed, including searching beyond the electronics and electrical engineers. A good connection with our various social/professional initiatives, such as Young Professionals or Women in Engineering, has to be kept and expanded.

Finally, the Forum and BoG were happy to congratulate the 14 newly elected Fellow members. I wish good luck to the newly elected BoG members and thank the outgoing members for their contributions. As I am terminating my 2 years duty, I wish the best to Jacobus Swart, newly elected EDS Secretary, to whom I leave the floor.

Simon Deleonibus
EDS Secretary (2016–2017)

Motions approved at the December 3, 2017 IEEE EDS BoG meeting in San Francisco.

Motion: To approve the minutes of the last meeting

Motion: For repeat conferences to approve the 2019 financial conferences and to approve the technical cosponsored conferences for 2019

Motion: To approve 100% financial sponsorship for the IEEE International Flexible Electronics Technology Conference starting in 2019

Motion: To approve the 2018 budget

Motion: To transfer remaining funds into the IEEE EDS foundation account with a total of $25K

Motion: To approve new format changes to EDS Newsletter

Motion: To approve two Newsletter Associate Editors

Message from EDS President

Samar K. Saha
EDS President,
2016–2017

Dear Colleagues and Members of the Electron Devices Society:

First of all, I wish you a Happy and Prosperous New Year, 2018! And, I hope everyone had a wonderful holiday season! I am writing this message as I prepare to transition to a *Past President* of the IEEE *Electron Devices Society* (EDS). Please note that I will continue to be active with EDS *promoting excellence in the field of electron devices for the benefit of humanity*!

It has been my great pleasure to serve EDS as the President for the past two years (2016–2017). As I shared in my President's report on December 3rd, 2017 Board-of-Governors (BoG) meeting at San Francisco, the EDS has been on a steady roll with the help of Executive Committee (ExCom), BoG, Technical Committee (TC), and Regions & Chapters (RC) volunteers and EDS Executive Office staff in these two years. Following my pledge to *building* EDS *on the foundation of the past to meet the challenges of the future*, we made some amazing strides with our ongoing programs and new initiatives for our Society with the great support and outstanding team work of volunteers as well as the staff of the Executive Office! Through the selfless dedication, hard-work, passion, and innovative team work of all, we made some extraordinary accomplishments. I sincerely thank the ExCom, BoG, TC, and RC volunteers and Executive Office for their dedicated service for Society's successes. In this message, I will highlight some of the major accomplishments we made together in these past two years:

- ***Membership Growth***: Through our membership drive to grow and retain EDS membership, our overall membership grew by about 3.6% during 2016–2017 (totaling 10,443). It is worthwhile to mention that during the same two year period, the IEEE membership declined by about 1.1%.
- ***Chapter Growth***: The growth of EDS chapters over the past two years modestly reflects the growth of our membership. Considering our primary focus on the growth of student membership and chapters, our worldwide overall chapter growth is about 11.2% in these past two years (totaling 209).
- ***Publications Excellence***: During 2016–2017, we have completed new Editor-In-Chief (EIC) transition for *IEEE Transactions on Electron Devices* (T-ED), *IEEE Electron Device Letters* (EDL), and EIC search and transition for *IEEE Journal of Electron Devices Society* (J-EDS) and EDS *Newsletter*. Through the dedication and relentless pursuit of excellence by new EICs and their editorial boards, our publications continue to excel. The open access (OA) publication, the J-EDS has been the most preferred OA publication for the electron devices community with an impact factor (IF) of 3.14. And, the IF for all our world-class flagship publications, the T-ED and EDL has improved reaching 2.61 and 3.05, respectively. In addition, the EDL submission to online publication is the best in IEEE, averaging about 3.5 weeks. Also, we have published special issues on emerging topical areas including *Solid-State Image Sensors*, *Power Semiconductor Devices and SmartPower IC Technologies*, and *Flexible Electronics* in T-ED and *Ultra-low Power Electronic Devices* as well as extended version of selected top-rated 2017 EDTM (*Electron Devices Technology and Manufacturing*) conference papers in J-EDS. Furthermore, we have created a dedicated *Special Section* with a well-known technical expert in the field as the lead editor to publish the *Display Technology* research papers in the J-EDS.
- ***Conference Management***: We have successfully executed the launching of the first EDTM conference at Toyama, Japan during February 28th–March 2nd, 2017 to strategically position EDS in the manufacturing stronghold in the Asia-Pacific region. And, the EDTM 2018 is scheduled to be held during March 13–16, 2018 at Kobe, Japan. We have initiated the new *IEEE International Flexible Electronics Technology Conference* (IFETC) to be held during August 7–9, 2018 at Ottawa, Ontario, Canada with 100% financial sponsorship from 2019 and beyond. The IFETC is, also, aimed to revitalize EDS activities in Region 7. To strategically position EDS in the Europe and Region 8, we have signed an agreement for 100% financial sponsorship of *European Solid-State Device research Conference* (ESSDERC). Also, to increase the visibility and attendance of our flagship conferences, we have offered options to the newly elected EDS fellows to be recognized at any of our flagship conferences. Accordingly, for the first time, we have recognized EDS Fellows at the opening sessions of 2017 *VLSI Technology Symposium* at Kyoto, Japan and 2017 *Photovoltaic Specialist Conference* (PVSC) at Washington, D.C.
- ***Educational Program***: In addition to our ongoing stellar educational programs such as Masters and PhD Student Fellowships, Distinguished Lectures (DLs), Mini-Colloquia (MQ), EDS-ETC, Webinar, and so on, we have established an *EDS Center of Excellence*. This is the *1st of its kind* educational program in EDS and IEEE and is aimed to attract future

EDS membership and engage high school and undergraduate boys and girls students in electrical engineering and specifically device engineering, and choose device engineering as their professional career.

- ***Outreach Program***: In the past two years, we have established bi-lateral collaboration of mutually beneficial multi-society programs including *Heterogeneous Integration Roadmap* (HIR), *Internet of Things* (IoT), *International Roadmaps for Devices & systems* (IRDS), and *IEEE 5G* initiatives. In addition to multi-Society technical programs, through our outreach program to IEEE Division I societies, we have, also, added new EDS membership (30 in 2017). In our outreach efforts to students and young professionals, we hosted social events at the 43rd PVSC in Portland, Oregon and 44th PVSC in Washington D.C.
- ***Future Directions***: Besides operating business as usual in these two years of my Presidency, we have initiated the EDS *first five-year strategic planning* to meet the challenges of the future. Though the EDS as an organization is in good standing with the Society's near-future directions and engagements by regularly adopting new strategic initiatives, it is necessary to continuously change with the changing technology in the digital era: *"Change is the law of life. And, those who look only to the past or present are certain to miss the future." - John F. Kennedy.* Our first five-year strategic plan is based on thorough self-assessment of Society's current position in 2017 by a survey questionnaire to our members, our values, vision, and mission. We will rigorously review the five-year strategic plan and execute accordingly to position EDS in 2022 and beyond.

In these past two years, we recognized and honored the achievements of our members' and honored our most venerated alumni as *Celebrated Members:* Professor Mildred Dresselhaus in 2016, and Dr. Gordon E. Moore and Professor Simon M. Sze in 2017.

Also, in these past two years, the Society has been in a good financial health. The EDS mission fund for humanitarian activities has grown to about $102 K. We have updated the EDS *Field-of-Interest* in compliance to IEEE Technical Activities Board (TAB) word-count requirement and updated the EDS *Constitution and Bylaws* by resolving the inconsistencies and ambiguities therein by an appointed Ad Hoc committee and got it approved by EDS BoG. Also, Jim Skowrenski was hired as the EDS Operations Director (2016); and EDS flagship publications have been transferred to IEEE publishing operations to ensure IEEE-wide uniform standard for EDS publications.

These are the major highlights of Society's accomplishments in the past two years in addition to our ongoing day-to-day EDS operations. And, these accomplishments were possible through selfless dedication and outstanding team work of volunteers and the staff of the EDS Executive Office. Once again, I sincerely thank each one of our membership and Executive Office staff for the accomplishments of these past two years. And, special thanks to Simon Deleonibus, Fernando Guarin, Subramanian Iyer, Hisayo Momose, Tian-Ling Ren, MK Radhakrishnan, Ravi Todi, Paul Yu, Albert Wang, James Skowrenski, Laura Riello, Stacy Lehotzky, Joyce Lombardini, and Jessica Lotito for their support in Society's success.

Finally, I congratulate the newly elected BoG members and Officers and, newly appointed ExCom members and Technical Committee Chairs and Members. And, I welcome the new EDS President, Fernando Guarin and wish him all the best to take the Society to a new horizon!

Samar K. Saha
EDS President, 2016–2017
Prospicient Devices, CA, USA
samar@ieee.org

IEEE EDS Celebrated Members Recognized in 2017

EDS announced Gordon E. Moore and Simon M. Sze as EDS Celebrated Members

"For fundamental contributions to the Field of Electron Devices for the benefit of humanity."

Dr. Gordon E. Moore, widely known for *Moore's Law*, is the founding father of Silicon Valley and a pioneering architect of the history of computing leading to the digital era. He is the co-founder of Fairchild Semiconductor and Intel.

Gordon and his wife Betty established the Gordon and Betty Moore Foundation in September 2000. The foundation fosters path-breaking scientific discovery, environmental conservation, patient care improvements, and preservation of the special character of the San Francisco Bay Area.

Gordon co-founded Intel in 1968, serving initially as executive vice president. He became president and chief executive officer in 1975 and held that post until elected chairman and chief executive officer in 1979. He remained CEO until 1987 and was named chairman emeritus in 1997, stepping down in 2006.

Gordon is widely known for "Moore's Law," which in 1965 he predicted that the number of components the industry would be able to place on a computer chip would double every year. In 1975, he updated his prediction to once every two years. Because of changing technology, the industry now states approximately every 18 months. "Moore's Law" has become the guiding principle for the industry to deliver ever-more powerful semiconductor chips at proportionate decreases in cost. In practical terms, what this means is faster, cheaper chips with more functionality that allows everything from a laptop computer, cell phones, GPS, cleaner car emissions/skid control/anti-lock brakes, and digital cameras, to medical devices that non-invasively see inside the body, and literally hundreds of thousands of other uses.

Gordon earned a B.S. in chemistry from the University of California at Berkeley and a PhD in chemistry and physics from the California Institute of Technology. He was born in San Francisco, California, on January 3, 1929.

Gordon received the Presidential Medal of Freedom, the nation's highest civilian honor, from George W. Bush in 2002. He received the National Medal of Technology from President George H. W. Bush in 1990. He received the Institute of Electrical and Electronics Engineers (IEEE) *Medal of Honor* in 2008: "For pioneering technical roles in integrated-circuit processing, and leadership in the development of MOS memory, the microprocessor computer and the semiconductor industry." He is also a member of the National Academy of Engineering and a Fellow of the IEEE. He served as chairman of the board of trustees of the California Institute of Technology from 1995 until the beginning of 2001 and continues now as a Life Trustee.

Dr. Simon M. Sze was born in Nanking, China in 1936. He received the B. S. degree from the National Taiwan University in 1957, M. S. from the University of Washington in 1960, and PhD from Stanford University in 1963, all in Electrical Engineering.

Simon was with Bell Laboratories in Murray Hill, N. J., from 1963 to 1989 as a member of the Technical Staff, where he was involved in the study of advanced transistors and the development of novel device concepts. He joined the National Chiao Tung University (NCTU) in Hsinchu, Taiwan from 1990 to 2006 as a Distinguished Chair Professor. At present, he is an Honorary Chair Professor at NCTU. Simon has served as Visiting Professor to many academic institutions including the University of Cambridge, Delft University, Soochow University, Stanford University, Swiss Federal Institute of Technology, and Tokyo Institute of Technology.

He has made fundamental and pioneering contributions to semiconductor devices, especially the metal-semiconductor contacts, microwave devices, and MOSFET technology. Of particular importance is his discovery with Dr. Dawon Kahng of the *floating-gate memory* (FGM) *effect* which has subsequently given rise to a large family of memory devices including EPROM, EEPROM and Flash memory. FGM is a ground-breaking technology for long-term information storage (superseding HDD, optical disk and magnetic tape) and enables the invention of nearly all modern electronic systems such as the digital cellular phone, tablet computer, personal digital assistant, smart IC card, digital camera, digital television, portable DVD, MP3 music player, pacemaker, implantable defibrillator, global positioning system (GPS), and anti-lock braking system (ABS). FGM has also empowered technology for the development of artificial intelligence, big data, cloud computing, internet of things, robotics, and solid-state drive.

Simon has authored or coauthored over 350 technical papers. He has written and edited 16 books. His book "*Physics of Semiconductor Devices*" (Wiley, 1969; 2nd Ed, 1981; 3rd Ed, with Dr. K. K. Ng, 2007) is one of the most cited works in contemporary engineering and applied science publications (over 47,500 citations according to Google Scholar). Simon has received the IEEE J.J. Ebers Award, the National Endowed Chair Professor Award, the Flash Memory Summit Lifetime Achievement Award, and the National Science and Technology Prize. He is a Life Fellow of IEEE, an ITRI Laureate, an Academician of the Academia Sinica, a foreign member of the Chinese Academy of Engineering, and a member of the US National Academy of Engineering.

Message from the Editor-in-Chief

Dear EDS Members and Readers,

Carmen M. Lilley
Editor-in-Chief
EDS Newsletter

It is a pleasure to share with the January newsletter, filled with highlights and summaries of the EDS Board of Governor's meeting held December 2–3 and a technical review article that summarizes high impact news from 2017 IEEE International Electron Devices Meeting (IEDM) Dec. 2–6. Both events took place concurrently in the exciting city of San Francisco, CA. We also have many articles featuring EDS activities from around the globe. I think you will find this newsletter to be full of informative news from EDS. I want to also express my gratitude to Simon Deleonibus, who is completing his term as EDS Secretary and the Chair of the Newsletter Oversight Committee. I worked alongside Simon, Joyce Lombardini, and James Skowrenski, to collect, organize, and analyze the proposed changes to the EDS newsletter that were approved at the December BoG meeting, highlights that you can find in the Secretary's Letter from Simon in this newsletter. I am grateful for all of their contributions in assisting me with the goal to enhance the newsletter for our readers. As always, I invite our EDS members and readers to share with me their ideas on themes they would like to appear in the newsletter and feedback on changes you see in the newsletter.

Sincerely,
Carmen M. Lilley
University of Illinois at Chicago
Editor-in Chief, EDS Newsletter
e-mail: clilley@uic.edu

EDS Members Recently Elected to IEEE Senior Member Grade

Ethem Erkan Aktakka
Abdualah Aljankawey
Mohammad Amin Arbabian
Sergio Bampi
Anirban Bandyopadhyay
Ismail Hakki Batum
Karlheinz Bock
Marc Chappo
Sang Hun Chung
Ryuichi Fujimoto
John George
Adele Gilliland
Guohan Hu
Hazem Khanfar
Rama Komaragiri
Steven Kosier
Felix Levinzon
Gengchiau Liang
Gian Domenico Licciardo
Chun-Yu Lin
Blanka Magyari-Kope
Siegfried Mantl
Mark Martin
Guy Meynants
Tien Khee Ng
Hiroki Noguchi
Guido Notermans
Daniele Passeri
Yi Pei
Peter Ramm
Masa Rao
Dilip Risbud
Tae Roh
Kishore Prabhala
Sneh Saurabh
Jae-Sun Seo
Pankaj Sharma
David Sheridan
Eddy Simoen
P. Sivakumar
Takao Someya
Sergey Tolpygo
Mani Vaidyanathan
Tadaaki Yamauchi
Saul Winderbaum
Hiu Yung Wong
Rajesh Yadav
Yang Yang
Jumril Yunas

If you have been in professional practice for 10 years, you may be eligible for Senior Membership, the highest grade of membership for which an individual can apply. New senior members receive a wood and bronze plaque and a credit certificate for up to US $25 for a new IEEE society membership. Upon request, a letter can be sent to employers, recognizing this new status. For more information on senior member status, visit: http://www.ieee.org/membership_services/membership/senior/index.html

To apply for senior member status, fill out the on-line application after signing in with your IEEE account: https://www.ieee.org/membership_services/membership/senior/application/index.html.

2016 IEEE TSM Best Paper Award

High quality scholarship requires technical excellence but also connects the work to the primary references in the field. In this way the reader advances their knowledge and gains perspective. The *Transactions on Semiconductor Manufacturing* supports these goals by recognizing the best paper chosen by the Associate Editors and reviewers.

The winning paper was selected from 51 papers published by TSM in 2016. The winner is "Risk-Controlled Product Mix Planning in Semiconductor Manufacturing Using Simulation Optimization" by Dr. Kuo-Hao Chang published in the November 2016 issue of *IEEE Transactions on Semiconductor Manufacturing.*

Dr. Chang is a professor of Industrial Engineering and Engineering Manufacturing at National Tsing Hua University in Hsinchu, Taiwan. The paper applies a method developed in another domain to find the optimal product mix in a semiconductor manufacturing line.

On behalf of the associate editors, I congratulate Dr. Chang on being selected.

Anthony J. Muscat,
T-SM Editor-in-Chief
Department of Chemical and Environmental Engineering
University of Arizona
Tucson, AZ, USA

Call for Nominations to IEEE Fellow Class of 2019

IEEE Fellow is a distinction reserved for select IEEE members. The honor is conferred by the Board of Directors upon a person with an extraordinary record of accomplishments in any of the IEEE fields of interest.

If you know of an IEEE colleague who is a Senior Member or Life Senior Member in good standing, has completed five full years of service in any grade of IEEE Membership and who has made an outstanding contribution to the electronic or electrical engineering profession in any of the IEEE fields of interest, you can nominate this person in one of four categories: Application Engineer/Practitioner, Educator, Research Engineer/Scientist or Technical Leader.

Nominations for the Fellow Class of 2019 are now being accepted.

To learn more about the Fellow program and the application process, visit http://www.ieee.org/fellows.

The deadline for nominations is 1 March 2018.

Updates from the 2017 EDS PhD Student Fellowship Recipients

Carmen Lilley
EDS Student Fellowship Committee Chair

The EDS PhD Student Fellowship Program is designed to promote, recognize, and support graduate level study and research within the Electron Devices Society's Fields of Interest. The 2017 EDS PhD Student Fellowship recipients were:

Renjie Chen – University of California, San Diego, USA

Po-Hsun Chen – National Sun Yat-sen University, Taiwan

Hao Yu – imec/Katholieke Universiteit, Leuven, Belgium

Renjie Chen is currently a PhD candidate in the Department of Electrical and Computer Engineering at the University of California, San Diego. He joined Prof. Shadi A. Dayeh's group in 2013, and worked at Center for Integrated Nanotechnologies (a Sandia National Labs affiliated organization) for 3 years as a facility user. Under Prof. Dayeh's supervision, Renjie focused his research efforts on the metallurgy of forming metal contacts to nanoscale semiconductor channels for materials relevant to current and emergent transistors that are only a few atoms across. They devised a variety of fabrication processes to combine precisely controlled nanochannels with in situ TEM (Transmission Electron Microscopy) heating platforms to record the dynamics of metal-semiconductor solid-state reactions.

Po-Hsun Chen is a PhD candidate in the Department of Physics at National Sun Yat-sen University, under the direction of Professor Ting-Chang Chang. His main field of study is in resistive random access memory (RRAM), which is a non-volatile memory for next generation electronic devices. His research focuses on applying transparent conductive oxide (TCO) within the RRAM structure to further enhance device performance and reliability. In addition, he is also working to solve forming voltage issues by introducing a new sidewall spacer in RRAM. Another recent project has him working closely with other researchers to develop vanadium-based selector devices. To date, he has authored 23 peer-reviewed journal papers covering various electron devices.

Hao Yu received his B. S. and M. S. degrees in Microelectronics and Solid-State Electronics from Fudan University in 2010 and 2013, respectively. He is currently a PhD candidate affiliated to imec and Katholieke Universiteit Leuven under supervision of Dr. Nadine Collaert and Prof. Kristin De Meyer, working on metal-semiconductor contact resistances. As high contact resistances become major obstacles that compromise performance of modern CMOS devices, Hao Yu has developed high-accuracy test vehicles and reported multiple contact schemes meeting the 10–9 $\Omega \cdot cm^2$ – contact – resistivity industrial target. He has contributed 14 articles to peer-reviewed journals and 12 to international conferences.

Carmen Lilley
EDS Student Fellowship
Committee Chair
University of Illinois at Chicago
Chicago, IL, USA

2018 PhD Student Fellowship

Description: One year fellowships will be awarded to promote, recognize, and support PhD level study and research within the Electron Devices Society's field of interest. The field of interest for EDS is all aspects of engineering, physics, theory, experiment and simulation of electron and ion devices involving insulators, metals, organic materials, plasmas, semiconductors, quantum-effect materials, vacuum, and emerging materials. Specific applications of these devices include bioelectronics, biomedical, computation, communications, displays, electro and micro mechanics, imaging, micro actuators, optical, photovoltaics, power, sensors and signal processing.

Three fellowships are expected to be awarded to eligible students in each of the following geographical regions for 2018: Americas, Europe/Middle East/Africa, and Asia & Pacific. Only one candidate can win per educational institution.

Prize: US$5,000 to the student and if necessary funds are also available to assist in covering travel and accommodation costs for each recipient to attend the EDS Governance meeting in December 2018 for presentation of the award plaque. The EDS Newsletter will feature articles about the EDS PhD Fellows and their work over the course of the next year.

Eligibility: A candidate must be an IEEE EDS student member at the time of nomination; be pursuing a doctorate degree within the EDS field of interest on a full-time basis; and continue his/her studies at the current institution with the same faculty advisor for twelve months after receipt of award. The nominator must be an IEEE EDS member and preferable be serving as the candidate's faculty advisor. Previous award winners are ineligible.

Basis for Judging: Demonstration of his/her significant ability to perform independent research in the fields of electron devices and a proven history of academic excellence.

May 15, 2018
Submission Deadline

Nomination Package

- Nomination letter from an EDS member
- Two letters of recommendation from individuals familiar with the student's research and educational credentials. Letters of recommendation cannot be from the nominator.
- One-page biographical sketch of the student (including student's mailing address and email address)
- Two-page (maximum) statement by the student describing his or her education and research interests, accomplishments and graduation date
- One copy of the student's under-graduate and graduate transcripts/grades. Please provide an explanation of the grading system if different from the A-F format.

Timetable

- Completed nomination packages are due at the EDS Executive Office no later than **May 15, 2018**
- Recipients will be notified by July 15
- Monetary awards will be given by August 15
- Formal award presentation will take place at the EDS Governance Meeting in December

Please submit application packages via e-mail or mail:

Email: edsfellowship@ieee.org

Mail:
IEEE EDS Executive Office
PhD Student Fellowship Program
445 Hoes Lane
Piscataway, NJ 08854 USA

For more information contact:
edsfellowship@ieee.org

Visit the EDS website:
http://eds.ieee.org/eds-phd-student-fellowship.html

Updates from the 2017 EDS Masters Student Fellowship Winners

Carmen Lilley
EDS Student Fellowship Committee Chair

The EDS Masters Student Fellowship program is designed to promote, recognize, and support Masters level study and research within the Electron Devices Society's Fields of Interest. The 2017 EDS Masters Student Fellowship recipients were as follows:

Abhinandan Borah – Columbia University, New York, USA

Jiabin Wang – Tsinghua University, Beijing, China

Abhinandan Borah is currently pursuing doctoral studies in the Department of Electrical Engineering at Columbia University. He received his bachelor's degree in Electronics and Communication Engineering from National Institute of Technology, Silchar in 2013. After graduation, he worked at IBM India as an Associate Systems Engineer for a year. In 2014, he joined Tata Institute of Fundamental Research (TIFR), Mumbai as a Junior Research Fellow in the Nanoelectronics lab with a fellowship from the Department of Science and Technology, India. At TIFR, his research focus was nanoscale devices with 2D materials. Advancing his interest in unconventional nanoelectronics, his current research at Columbia involves understanding and developing heterostructure devices of 2D semiconductors through both simulations and experiments, in order to contribute towards a post-silicon era in future.

Jiabin Wang received the B.E degree in electronic science and technology from Tsinghua University, Beijing, China, in 2015, where he is currently pursuing the M.E degree

in the Institute of Microelectronics, supervised by Professor Tian-Ling Ren. His research interests include thin film transistors, synaptic devices, neuromorphic computation systems, low-voltage applications, ferroelectric applications, and critical technology for advanced micro- and nano-electronics. His current research topic is developing novel brain-like electron devices and neuromorphic computation system with higher efficiency, low energy consumption, and novel functionality, to build artificial computation systems in high similarity and comparable efficiency with the human brain.

Carmen Lilley
EDS Student Fellowship
Committee Chair
University of Illinois at Chicago
Chicago, IL, USA

2018 Masters Student Fellowship

Description: One-year fellowships will be awarded to promote, recognize, and support graduate Masters level study and research within the Electron Devices Society's field of interest. The field of interest for EDS: all aspects of engineering, physics, theory, experiment and simulation of electron and ion devices involving insulators, metals, organic materials, plasmas, semiconductors, quantum-effect materials, vacuum, and emerging materials. Specific applications of these devices include bioelectronics, biomedical, computation, communications, displays, electro and micro mechanics, imaging, micro actuators, optical, photovoltaics, power, sensors and signal processing.

Three fellowships are expected to be awarded to eligible students in each of the following geographical regions for 2018: Americas, Europe/Mid-East/Africa, and Asia & Pacific. Only one candidate can win per educational institution.

Prize: US$2,000 and a plaque to the student, to be presented by the Dean or Department head of the student's enrolled graduate program.

Eligibility: Candidate must be an IEEE EDS student member at the time of nomination; be accepted into a graduate program or within the first year of study in a graduate program in an EDS field of interest on a full-time basis; and continue his/her studies at a graduate education institution. The nominator must be an IEEE EDS member and preferably be serving as the candidate's mentor or faculty advisor. Previous award winners are ineligible.

Basis for Judging: Demonstration of his/her significant ability to perform research in the fields of electron devices a proven history of academic excellence in engineering and/or physics involvement in undergraduate research and/or a supervised project.

May 15, 2018
Submission Deadline

Nomination Package

- Nomination letter from an EDS member who served as candidate's mentor or faculty advisor.
- One letter of recommendation from an individual familiar with the student's research and educational credentials. Letters of recommendation cannot be from the nominator.
- One-page biographical sketch of the student (including mailing address and e-mail address)
- Two-page (maximum) statement by the student describing his or her education and research interests, accomplishments and graduation date. This can include undergraduate, graduate and summer internship research work.
- One copy of the student's transcripts/grades. Please provide an explanation of the grading system if different from the A-F format.

Timetable

- Completed nomination packages are due at the EDS Executive Office no later than **May 15, 2018**
- Recipients will be notified by July 15
- Monetary awards will be presented by the Dean or Department Chair of the recipient's graduate program at the beginning of the next academic term.

Please submit application packages via e-mail or mail:

Email: edsfellowship@ieee.org

Mail:
IEEE EDS Executive Office
PhD Student Fellowship Program
445 Hoes Lane
Piscataway, NJ 08854 USA

For more information contact:
edsfellowship@ieee.org

Visit the EDS website:
http://eds.ieee.org/eds-masters-student-fellowship.html

Young Professionals

Young Entrepreneur Attracts Record Number of Attendees at Annual IEDM Event

The Entrepreneur Luncheon, sponsored by the IEEE EDS/Women in Engineering and the IEEE International Electron Devices Meeting (IEDM), was held on Tuesday, December 6, 2017, at the 63rd IEDM in San Francisco, California.

Featuring the entrepreneur Courtney Gras (www.courtneygras.com), this annual event attracted a record number of 279 paid participants, who were eager to hear the firsthand account of a remarkably successful engineer and her unconventional trajectory. Ms. Gras gave a brief overview of her career and then began the highly anticipated open forum, moderated by Prof. Leda Lunardi from NC State, the EDS WIE liaison.

Leda Lunardi (left), with Courtney Gras

Prof. Lunardi initiated the conversation inquiring about the benefits an engineering background brings to business. The audience was also encouraged to participate with questions of their own. Ms. Gras engagingly related her experiences about team selection criteria and starting companies while still in school. Proportioning some self-reflective insight, she also illuminated some valuable lessons she learned during her ventures. The conversation was wide-reaching, broaching all topics related to intellectual protection and financing strategies.

She emphasized that being young is not an issue if you can get your technical message across clearly and convince your team. And finally, she addressed being a woman in male-dominated fields. Ms. Gras expressed her optimism in the opportunities and resources available for women and small businesses, encouraging attendees to leave their comfort zones in order to explore their interests.

Leda Lunardi
EDS WIE Liaison
North Carolina University
Raleigh, NC, USA

GaN Transistors – Giving New Life to Moore's Law

New Webinar Available in the EDS Collection

EDS is many things to its members – scientific publisher, technical conference sponsor, networking resource – but at its core EDS is a community of learning. From undergraduate students and PhD candidates to tenured professors and world-renowned researchers, EDS provides device engineers from across the spectrum engaging and enriching educational opportunities.

As part of our commitment to enhancing the value of membership in EDS, we are pleased to present the EDS Webinar Archive. The online collection provides our members with on-demand access to streaming video of past events. The recently held webinar can be accessed at http://eds.ieee.org/webinar-archive.html.

Presented by Alex Lidow

Alex Lidow is CEO of Efficient Power Conversion Corporation (EPC). Prior to founding EPC, Dr. Lidow was CEO of International Rectifier Corporation. A co-inventor of the HEXFET

power MOSFET, Dr. Lidow holds many patents in power semiconductor technology and has authored numerous publications on related subjects. He most recently co-authored, *GaN Transistors for Efficient Power Conversion*, the first textbook on GaN FET technology and applications. Lidow earned his Bachelor of Science degree from Caltech in 1975 and his PhD from Stanford in 1977.

Abstract

GaN Transistors – Giving New Life to Moore's Law

Enhancement-mode gallium nitride transistors have been commercially available for over eight years and have infiltrated many applications previously monopolized by the aging silicon power MOSFET. In this presentation, we will discuss the state-of-the-art and the expected progress of GaN technology over the next few years, showing that Moore's Law is alive and well in the world of power semiconductor technology. We will also enumerate the advantages of GaN over silicon in terms of performance, cost, and reliability.

First NanoBootcamp Young Professionals Colombia Micro & Nano day "Reloaded"

By Fernando Guarin

The first NanoBootcamp – Micro & Nano day "reloaded" was held in Bogota on August 3rd and 4th, 2017, in conjunction with the EDS Colombia Chapters meeting. This YP initiative is aligned with one of the principal cores of Young Professionals Colombia, which is to create, develop and host technical events on high impact subjects, such as the field of Nanotechnology.

The main purpose of this NanoBootcamp was to bring together Young Professionals members from Colombia into an innovative space, where they had the opportunity to learn about new developments in the field of nanotechnology, sharing knowledge with other IEEE members and achieving certification of their knowledge. To successfully develop this event, YP Colombia made three strategic alliances: EDS Society, Pontifica Universidad Javeriana University and Servicio Nacional de Aprendizaje (SENA), which is a governmental organization for non-profit technical education in Colombia.

The event had more than 40 participants, actively discussing the overall growth of professional leaders among the Colombian section and started a closer relationship between nanotechnology development and young professionals.

Leading the project was Jenniffer Zapata Giraldo, Young Professionals Colombia chair, who led the team of Camilo Tellez, Carlos Zambrano, Luis Quevedo, Stephanie Rodriguez, Sebastian Franco, all of them active members and IEEE volunteers from the Colombia Section.

Volunteer organizers and participants of NanoBootcamp held in Bogota, Colombia

~ Joao Antonio Martino, Editor

Educate Children on the Use of Integrated Circuit (IC) Chips on a Beginner Level

By Sang Lam and Mansun Chan

Electronic circuits are versatile and indispensable for transmission, processing as well as storage of information, both analog and digital. They are also used in electrical power management and even for transmission and processing of electrical energy as in wireless power chargers and energy harvesting circuits. Nowadays, electronic circuits are commonly in the form of integrated circuit (IC) chips which have numerous transistors, capacitors, resistors and other devices assembled on a small single semiconductor substrate. The idea of integrating electronic circuits on a small semiconductor chip was first conceived in 1958 [1]. Forty-one years later, the Nobel Prize in Physics was awarded in 2000 for the invention of ICs [2]. Seventeen years have passed and the use of ICs is even more pervasive. The importance of ICs and their easy applications in circuits can be introduced to schoolchildren even before they learn about semiconductor physics, not to mention the more complicated quantum mechanics.

As the second tutorial article on organizing electronic circuit exploration workshops for schoolchildren, we have a small project building an electronic circuit using an IC to introduce the simple idea of ICs. When children successfully use an IC to build a circuit, they are expected to gain confidence in using ICs to build other electronic circuits. After using more and more ICs to build circuits, they may become interested in knowing more about ICs by asking "How they are made and what devices they have inside?". Since a light-emitting diode (LED) in series with a resistor or a variable resistor was introduced in the first tutorial article [3], we continue electronic circuit construction related to LEDs. A running light indicator circuit is a good choice because it uses essentially one IC, several LEDs and resistors as well as a switch. The young students should be familiar with LEDs following the first tutorial and their use with a resistor connected in series to control the electric current and hence the brightness. The IC is the only new component in the circuit.

In the actual delivery of the circuit construction session, the circuit schematic diagram (Fig. 1a) can be first shown to tell the students what circuit is to be built. The children may not understand what the circuit is by looking at the circuit diagram. To ease possible confusion, a photo of the neatly assembled circuit (Fig. 1b) can then be shown to tell them what the circuit is like. With the photo shown or the actual circuit for demonstration, the instructor can briefly tell what the circuit can do by saying that each LED will be turned on sequentially by pressing the push-button switches. Such a brief explanation or demonstration should give a child encouragement in attempting the circuit construction. Having visual effects controlled by a switch is part of the reason for choosing such a circuit for the workshop. It is possible that the children may not be impressed by the demonstration of the circuit and not know the use of the circuit. To arouse their interest, the instructor can tell examples of application of such LED display circuits. One common example for children living in large cities is the route map panel with LED indicators showing the metro stations. The circuit (Fig. 1a) can also be adapted to make traffic lights. If the workshop time allows, the engineering advantages of using LEDs for displaying information related to fixed positions and information that remains unchanged for months or even a few years can be reviewed.

After giving the students an overall idea about the LED light indicator circuit and its extended applications in daily life, the instructor can move on to explain a general idea of a circuit schematic diagram or schematic for short. A few key points can be covered quickly in a concise way. First, the circuit schematic is the language of representing the actual electronic circuits in written form showing the connections of various devices and components. Second, it is common that the schematics may not show the devices and components as they are in the actual circuits. They are drawn in a way for easy reading. The pin orientation of the ICs is a typical example as in the LED light indicator circuit. One key idea in reading a schematic can be highlighted at this stage is that the positive power supply is usually at the top while the negative supply is at the bottom. In-depth details should be avoided in teaching the ideas above. Rather, it is better for children to pick up the ideas through the hands-on circuit construction process.

On reading the circuit schematic, children should notice a rectangular box with 16 connections that represents the IC chip of the CMOS 4017 decade counter [4] to be used. Although it can be explained that a decade counter is a digital circuit which counts from zero to nine, there is no need to explain the operation principles. They can get a basic idea after they successfully build the circuit and see the effects. It is more important for them to learn to mount the IC chip correctly onto the breadboard and connect the circuit. The first hands-on task is to have the student mount the IC chip onto the breadboard, with the two columns of pins straddling the middle channel/track of the breadboard. The

instructor can remind the students that the legs of the IC should fit very well the pin holes of the breadboard in terms of the pin spacing and positions. No strong force is needed. Afterwards, the next technique is lifting up gently the inserted IC using a pair of forceps to take it off from the breadboard.

After the students learn how to gently mount and dismount the IC, they should be instructed to place the IC at an exact position and with a specific orientation on the breadboard. To achieve this, they need to know first how the IC pins are identified and oriented. The instructor can ask the students to look closely at the IC chips to see if they can find any index marks like a notch and a dimple on the surface of the IC package. With the IC oriented in such a way that the notch at the top, the IC pin on the left-handed side closest to the notch is pin 1 and the rest of the pins are numbered counterclockwise. For the 16-pin decade counter IC, the bottom pin on the left-handed side is pin 8 while the bottom pin and top pin on the right-handed side are respectively pins 9 and 16. In some ICs, there is also a dimple on the package and it is always pin 1. The students can be reminded that the pin numbering is like labeling the multiple exits of a metro station using alphabets for easy referencing. Using unique numbers to represent objects for identification purposes is very common in engineering practice. The students should then be asked to mount the 4017 decade counter IC with pin 1 at the 8th pinhole counting from the top on the breadboard (which has the middle dividing channel/track oriented vertically). By so doing, the bottom space of the breadboard can be used to build another circuit so that the children do not need to dismantle the LED light indicator circuit to give space for other circuit construction. For this hands-on task, student helpers should double-check whether the children have properly mounted the IC with the correct position and orientation to avoid chances incorrect

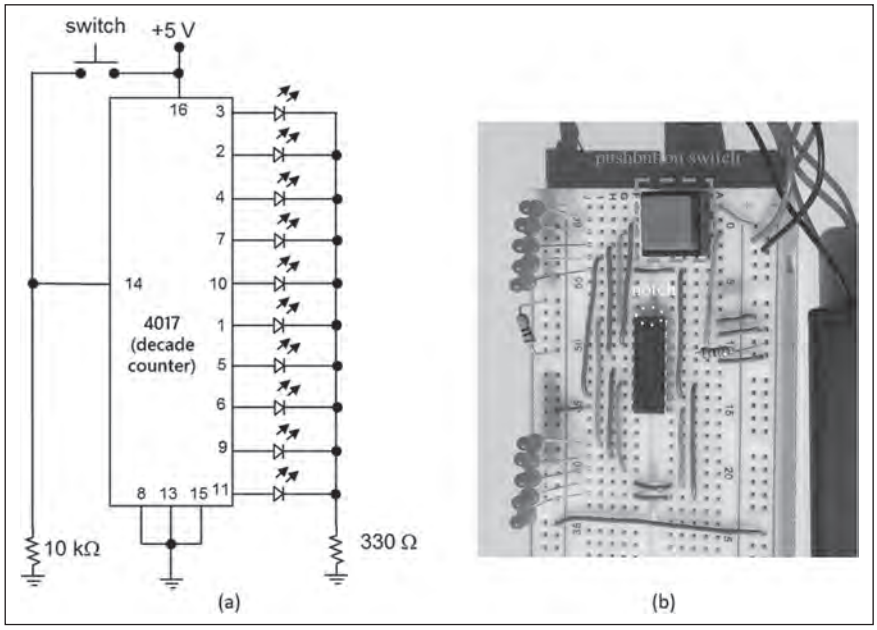


Fig. 1. LED running light indicator circuit using a CMOS 4017 decade counter IC: (a) schematic diagram; (b) circuit constructed on a breadboard

circuit connections later, and thus saving much troubleshooting time. The student helpers should guide the kids to follow closely the instructions given by the instructor in a synchronized way to avoid chaos in large class if many children ask for troubleshooting help later due to minor mistakes.

In the schematic (Fig. 1a), since the 16-pin decade counter IC is not oriented in the same way as how the actual IC looks, the whole circuit may not seem easy to be built when the children see it at the beginning. In fact, the pins of the IC in the schematic are not grouped together sequentially. A typical engineering technique, namely "divide and conquer", can be shared with the young students. The construction of the apparently difficult circuit would be much easier by dividing the circuit connections into simpler parts then building one by one (Fig. 1). All electronic circuits need electrical power to function. It is sensible to build the circuit starting from the power supply connections (Fig. 1a) and the ground counterpart too (Fig. 1b). In the LED running light circuit, the power supply connection part involves pins 16 and 14. With the 4017 IC correctly oriented and mounted on the breadboard, pin 16 is the top pin on the right-handed side of the IC. Using the wire cutting and stripping techniques taught in the beginning session [3], a hook-up wire of suitable length can be used be used to insert one end to a pinhole in the same horizontal row of pin 16 and the other end to a pin hole in one of those two vertical columns on the right-handed edge of the breadboard. In Fig. 1b shown here, the inner vertical column at the edge is used for the positive power supply connections and the outer vertical column of pin holes is used for the ground connections. The instructor can show the step by highlighting the connection both in the schematic and the actual wire hook-up on breadboard displayed on a projection screen. The next step is to connect pin 14 to a pushbutton switch and then to the positive power supply. Hook-up wires of suitable length are needed again to connect pin 14 to the switch and from the switch to the vertical column of pin holes used for positive power supply connections. Depending on the type of actual pushbutton switch used,

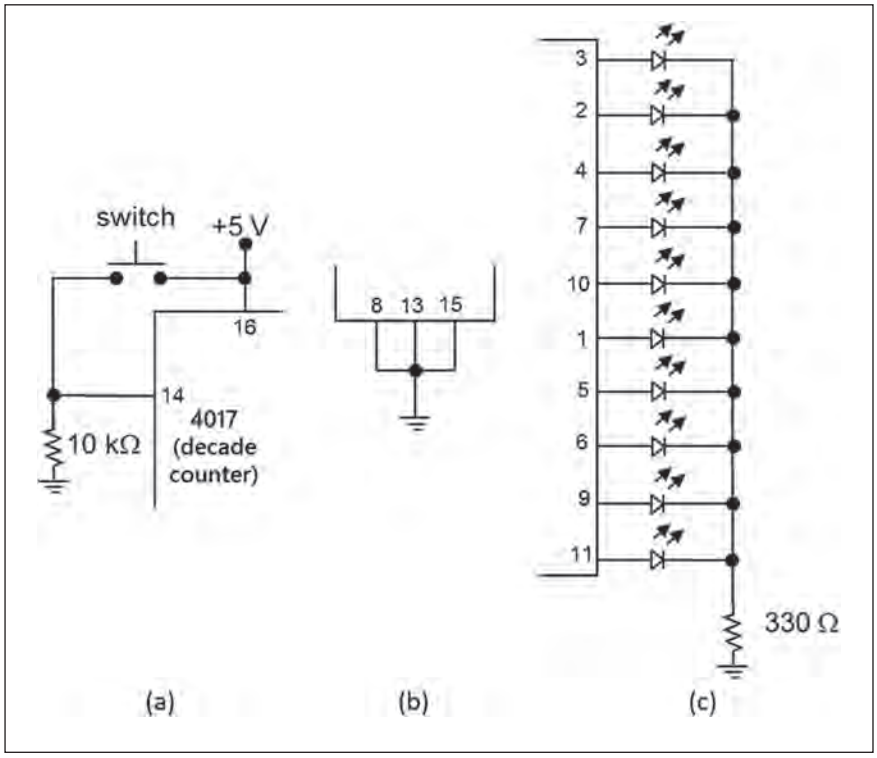


Fig. 2. Construction of the LED running light indicator circuit divided into three parts: (a) power supply part, (b) pin connections directly to ground, and(c) decade counter output pins connected to 10 LEDs in sequence

caution is needed in the inserting the pins of the switch into the pinholes on breadboard. One common mistake is that the two pins of the switch are inserted to the same row of pin holes on the breadboard and thus short-circuiting the switch. In some pushbutton switches, the legs are underneath and thus are not viewable when they are mounted onto the breadboard. Thus, a child may mistakenly make wire connections to the pins. The switches are less prone to hook-up mistakes in using a resistor to connect pin 14 to ground.

After the positive power supply connections (Fig. 2a), the next part is the connections from pins 8, 13 and 15 to ground (Fig. 2b). Since pins 13 and 15 are both on the right-handed side, their connections to the vertical column of pin holes reserved for ground are straightforward using hook-up wires of suitable length. As for pin 8, it is at the bottom on the left-handed side. The pin 8 connection uses the vertical inner column of pin holes at the left-handed edge so that later the 10 LEDs can have enough pin holes for convenient connections. The ground connection of pin 8 is first horizontally to the inner vertical column of pin holes at the left-handed edge and then a long hook-up wire is used to bridge the ground rails at the left-handed and right-handed edges.

The remaining connections of 10 LEDs are the final part of the circuit construction (Fig. 2c). The LED connections to pins 3, 2, 4 and 7 should be done first as a group because all four pins are on the same left-handed side of the IC. In the LED connections, the students should be reminded again the difference in the electrodes, namely the cathode and anode, of an LED. Since all 10 LEDs have their cathodes tied together, the vertical outer column of pin holes at the left-handed edge can be used as the common rail. The LED connecting to pin 3 is mounted at the top with the cathode pin inserted to a top pin hole at the outer common rail at the left-handed edge and the anode pin inserted to a pin hole of a top row. Then a hook-up wire of suitable length is used to connect that top row in a vertical fashion to the pin hole row of pin 3. The steps are more or less the same for the LED connections to pins 2, 4 and 7.

The fifth LED connection is to pin 10 which is on the right-handed side of the IC. It needs two hook-up wires. One wire in the vertical orientation is to connect the pin hole row of pin 10 to an upper row which is horizontally aligned to the pin hole row of the fifth LED's cathode. The second wire is to bridge the two horizontally aligned pin hole rows on the left and the right separated by the middle channel or track. Up to this point, it can be seen that the wire connections are horizontal and vertical. Hook-up wires jumping from one pinhole to another directly is avoided. Such neat wiring is encouraged to for considerably easier troubleshooting when the circuit turns out not working properly.

As for the remaining five LED connections, the LEDs can be stacked in the same way from top to bottom as in the first five LEDs. The cathode pins of the remaining five LEDs are all inserted to the pin holes of the vertical outer common rail. The sixth, seventh and eighth LEDs can be connected easily to pins 1, 5 and 6 respectively using wires of suitable length vertically bridging the pin hole rows of the IC pins to those of the anode pins of the three LEDs. To connect the last two LEDs, one hook-up wire in the vertical fashion and the other in the horizontal orientation are used for each LED as pins 9 and 11 are on the right-handed side of the IC while the LED are on the left-handed side. This is the same wiring technique for connecting the fifth LED to pin 10. After the connections of 10 LEDs, the common cathode can be connected to ground by mounting a 330-Ω resistor in a nearly vertical fashion with one lead wire inserted into an upper pin hole of the outer

Table 1. Key steps in the construction of LED running light indicator circuit with the underlying engineering concepts and the components or tools used			
Step or Task	**Component**	**Engineering Concept**	**Tool**
Reading circuit schematic diagram		Positive power supply and ground	
Mounting & dismounting IC chip	4017 decade counter IC chip	Standards of IC pin spacing & position	A pair of forceps & a breadboard
Pin identification of packaged ICs	16-pin decade counter IC	Index marks (notch & dimple) & pin numbering	
Circuit construction part 1	IC, pushbutton switch, resistor, hook-up wires	Divide and conquer; pin connections one by one	A wire stripper
Circuit construction part 2	Hook-up wires	Neat wiring for easy trouble-shooting later	
Circuit construction part 3	10 LEDs, resistor	Common rail tied together	
Final circuit construction	Battery box, capacitor, resistor	Noise in switching & filtering	

vertical common rail and the other lead wire into a lower pin hole of the inner vertical rail used as ground.

The final step is to connect the battery box's lead wires to the power and ground rails on the breadboard, namely the two vertical columns of pin holes at the right-handed edge in the circuit construction here. Now, the pushbutton can be pressed repeatedly to see the effect of the running LED light indicators. There may be noise in the switching action that can cause instability in the digital IC. A capacitor of 1 μF and a resistor of 91 Ω connecting the positive power supply to pin 14 will help filter the noise arising from the switching action as the capacitor is parallel to the switch. The connections can be done quite easily by first replacing the hook-up wire connecting pin 14 to one end of the switch. The 91-Ω resistor is used to connect to pin 14 and one unused row of pin holes from where one end of the switch is connected by a short wire and the positive power rail by the 1 μF capacitor. A mica capacitor is used here as it has no difference in the electrodes. If an electrolytic capacitor is used, the positive electrode must be connected to a higher voltage terminal and the negative electrode to a lower voltage one. The use of capacitors and their basic ideas will be covered at a later part of the circuit construction workshop. The related project circuit will be detailed in an article in the next newsletter issue.

References

[1] Nobelprize.org. Nobel Media AB. "The History of the Integrated Circuit", https://www.nobelprize.org/educational/physics/integrated_circuit/history/, 5th May 2003 [accessed on 23rd October 2017].

[2] Nobelprize.org. Nobel Media AB. "Jack S. Kilby - Nobel Lecture: Turning Potential into Reality: The Invention of the Integrated Circuit", http://www.nobelprize.org/nobel_prizes/physics/laureates/2000/kilby-lecture.html, 2014 [accessed on 23rd October 2017].

[3] Sang Lam and Mansun Chan, "Organizing IEEE EDS STEM Workshops for Kids to Build Electronic Circuits", *IEEE Electron Devices Society (EDS) Newsletter*, vol. 24, no. 4, pp. 18–20, October 2017.

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Chapter News

2017 EDS Chapter of the Year Award Winners

The EDS Chapter of the Year Award is presented annually to recognize chapters for the quality and quantity of the activities and programs implemented during the prior July–June period. In 2013, the Society expanded its Chapter of the Year Award to include one chapter in each IEEE Region (1 thru 7; 8, 9 and 10).

The 2017 EDS Chapter of the Year Award winners:

ED Schenectady Chapter (Regions 1–7) – EDS President, Samar Saha, presented the award at the EDS Board of Governors Awards Dinner, December 3, 2017

ED/MTT/AP/CPMT/SSC West Ukraine (Lviv) Chapter (Region 8) – award presentation to be decided

ED South Brazil Chapter (Region 9) – award presentation to be decided

Samar Saha (middle), presenting award, with Fernando Guarin (left)

ED Delhi Chapter (Region 10) – award presentation to be decided

We hope you enjoy reading about our EDS chapters and activities in this section, and learn how EDS chapters serve the community to enhance their member experiences.

M. K. Radhakrishnan
EDS Vice-President of Regions/Chapters
Email: radhakrishnan@ieee.org

IEEE Africa Initiative, 2016–2017: Courses delivered by EDS Distinguished Lecturers

By David Pulfrey and Anil Kottantharayi

The IEEE Technical Activities Board Strategic Planning Committee (TAB SPC) Ad Hoc Committee on Africa, chaired by Rabab Ward (FIEEE, Signal Processing President), has over the last two years organized lectures/courses/workshops/tutorials/seminars on engineering education and professional development in Ghana, Kenya, Rwanda, Uganda, Zambia and Zimbabwe. The programs in Ghana, Rwanda, and Uganda were co-sponsored this year by the IEEE Ad Hoc Committee on Activities in Africa. Two participants in this Africa Initiative are EDS members David Pulfrey (IEEE Life Member, Ad-Hoc Committee member 2000–2006, EDS Distinguished Lecturer 2002, EDS Education Award Winner 2009), and Anil Kottantharayil (IEEE Senior Member, EDS Distinguished Lecturer).

Dr. Pulfrey lectured on *"Solar Cells and Light-Emitting Diodes: theory, design and implementation for sustainable electricity generation and lighting"* in Kenya, Uganda and Rwanda in 2016, and in Zimbabwe and Zambia in 2017. The attendees were: faculty and graduate students, often from several universities within each country; engineers mainly from the power field; administrators with an interest in energy policy.

Each course was spread over two days, with four 90-minute lectures on each day. The lecture titles were:

1) Solar Cells and LEDs: environmental benefits.
2) Semiconductor diode theory.

Attendees of Dr. Pulfrey's (4th from left), lecture at Jomo Kenyatta University in Nairobi

3) LEDs: principles of operation, materials, efficiencies.
4) Solar Cells: principles of operation, materials, efficiency.
5) Solar Cells: components and sizing of a stand-alone system.
6) Solar Cells: options for utility-scale photovoltaics.
7) LEDs: white-light generation and application to street lighting.
8) LEDs and Solar Cells: life-cycle analyses.

The intent was to provide attendees with enough theoretical, practical and environmental information for them to be able to give authoritative lectures or opinions on the cost-effectiveness and sustainability of using solar cells for electricity generation, and light-emitting diodes for general-purpose lighting. The premises were that photovoltaic power generation (PV) is greener than coal-fired electricity generation, and that LEDs are greener than other forms of white-lighting as currently used for interior lighting (kerosene lamps and incandescent bulbs) and exterior lighting (high-pressure sodium lamps). The greenness (environmental desirability) was evaluated over the entire life-cycle (cradle-to-grave) of solar cell systems and LED luminaires. The courses were rigorous in that the technical details required to understand the operation and limitations of solar cells and LEDs began at the fundamental level of electrons and holes in semiconductors, and progressed through practical diodes to working systems.

Feedback from the course has been very positive and consultations with several interested attendees are ongoing. After two IEEE-sponsored sorties to Africa, Pulfrey can report that that there is both need and enthusiasm for education in sustainable electricity generation and lighting. Amongst the engineers there is the desire to avoid the polluting and wasteful habits that "First World" countries have practised hitherto in electricity generation and lighting. Amongst the teachers and students there is an excitement to understand the details of photovoltaic power generation and of solid-state white lighting so that they might make contributions to teaching and research in these areas. Complementing these attitudes is the huge abundance of the solar resource in Africa: it begs that PV be used for electricity generation, and that PV-powered LEDs be used for interior and exterior lighting.

Dr. Kottantharayil lectured on *"Photovoltaic Technology"* in Rwanda and Uganda in 2017. The attendees were University students from Bachelor to PhD level, faculty members, practicing engineers and aid workers.

Each course was spread over two days with lectures from 9:30 AM to

Attendees of Dr. Kottantharayil's lecture at the University of Rwanda

5:30 PM and covered the following topics.

1) Introduction to the course: The present context of photovoltaics
2) Science and technology of solar cells
3) Introduction to photovoltaic modules
4) Performance losses in modules: Degradation of module performance – Losses due to soiling
5) Lead acid batteries for PV systems
6) Maximum power point tracking and power converters
7) PV system design considerations
8) PV system design examples
9) Quality standard spreadsheet
10) Social entrepreneurship in the PV sector - examples from India

The course was well received in both the countries. The active participation of practicing engineers in the course exposed the University folks to several practical problems from the field. This complemented the theoretical emphasis of the course. During the course, I had several opportunities to discuss various aspects related to electricity access in Africa with the participants of the workshop. I am convinced that photovoltaics is a highly relevant topic for these countries and could be the enabling technology for providing wider access to quality electricity. IEEE should continue to contribute to capacity building and research in this sector in Africa.

2018 EDS Chapter of the Year Award – Call for Nominations

The EDS Chapter of the Year Award is given each year based on the quantity and quality of the activities and programs organized by the chapters for the benefit of members and professionals during the prior July 1st – June 30th period.

Each year EDS will award one Chapter from each of the following Regions:

- **Regions 1–7**
- **Region 8**
- **Region 9**
- **Region 10**

Nominations for the awards can only be made by SRC Chairs/Vice-Chairs, Regions/Chapters Committee Members or self-nominated by Chapter Chairs. Please visit the EDS website to submit your nomination form (http://eds.ieee.org/chapter-of-the-year-award.html).

Each winning chapter will receive a plaque and check for $500 to be presented at an EDS chapter meeting of their choice. Travel reimbursement will not be provided. A chapter that wins the Chapter of the Year Award is eligible for nomination after a lapse of 3 years only.

The schedule for the award process is as follows:

Action	Date
Call for nominations e-mailed to chapter chairs, SRC Chairs, SRC Vice-Chairs and Regions/Chapters Committee	June 1st
Deadline for nominations	September 15th
Regions/Chapters Committee & SRC Chairs & Vice Chairs selects winners	Early-October
Award given to chapter representative at requested chapter meeting	Open

Your Chapter Could Be Missing Important Notices and Funding Opportunities!

Please remember, whenever there is a change to Chapter Officers, both IEEE *and* EDS must be notified. Please follow these two steps:

1) Report officer changes to IEEE via the vTools Officer Reporting form: https://officers.vtools.ieee.org/ *(access to vTools requires use of an IEEE account)*.
2) Report officer changes to EDS by completing the Chapter Chair Update Form: https://ieeeforms.wufoo.com/forms/pgu6n1i1ixepnu/

Thank you in advance for your assistance.

EDS-ETC Program for Students of SM Kepala Batas, Penang

By Norhayati Soin, Noorjannah Ibrahim & Aliza Aini Md Ralib

An EDS-ETC program was held for secondary school students of Sekolah Menengah Kepala Batas on August 25th, at the Golden Sand Resort Penang by Shangri La, Batu Feringgi, Penang, Malaysia. Prior to the EDS-ETC session, the students were given motivational talks by Prof. Tanaka from Japan and Dr. Nizar. They were briefed on the career path and challenges to become an electrical engineer. A total of 30 students participated in the event. The students' feedback was positive in that they could understand the basic theory of constructing simple electronic circuits.

~ P Susthitha Menon, Editor

Participants of the EDS-ETC Session in Penang

IEEE EDS Vancouver Mini-Colloquium at Simon Fraser University

By Michael Adachi and Bonnie Gray

The EDS Vancouver Chapter hosted four EDS Distinguished Lecturers on the topic of "Nano/Micro Electronic and Related Devices" at Simon Fraser University, Burnaby, Canada on October 2, 2017. Lectures included *"Something different: Nanoscale Vacuum Electronics"* by Dr. Meyya Meyyappan, NASA AMES Research Center; *"Highly repeatable room temperature negative differential resistance in AlN/GaN resonant tunneling diodes"* by Prof. Paul Berger, The Ohio State University; *"Gallium Nitride Based Integrated Microsystems"* by Prof. Mina Rais-Zadeh, University of Michigan; and *"Theory of Nano-Electron-Fluidic Logic (NFL): A New Digital "Electronics" Concept"* by Dr. Héctor J. De Los Santos, Nano-MEMS Research, LLC. The mini-colloquium attracted about 50 participants consisting of undergraduate and graduate students, as well as researchers from multiple departments, and representatives from local industry and government. Four social activities (breakfast, lunch, coffee break, and dinner) were held to encourage discussions and new connections between different universities and with industry.

~ Michael Adachi, Editor

Attendees and DLs at the EDS Vancouver Mini-Colloquium held on October 2, 2017, at Simon Fraser University, Canada

Dear EDS Chapters:

When planning your upcoming chapter meetings, workshops, etc., please remember to visit the EDS website for a recent list of EDS Distinguished Lecturers and lecture topics.

✓ **Checklist**

- Chapter contacts EDS DL to check availability, confirms date/location of lecture, discusses DL funding needs and determines chapter funding
- EDS DL completes EDS DL Activity Log and Funding Request Form
- If applicable, obtain EDS funding approval
- Chapter publicizes lecture via web, email, etc. Obtain a chapter member list via SAMIEEE (http://www.ieee.org/about/volunteers/samieee/index)
- If applicable, DL submits an IEEE expense report to Laura Riello, to receive reimbursement
- Chapter Chair/DL Coordinator submits an EDS DL/MQ Feedback Form

If you have any questions and/or need more information, please do not hesitate to contact Laura Riello, EDS Executive Office.

Thank you for your continued support of the Society.

ED Brazil Mini-Colloquium and Report of SBMicro 2017

By Joao Martino

The ED South Brazil Chapter and University of Sao Paulo organized the ED Brazil Mini-Colloquium, held in Fortaleza, Brazil, on August 29, 2017, co-sponsored by the IEEE Electron Devices Society.

The Mini-Colloquium was composed of four presentation given by EDS Distinguished Lecturers:

- *"Transistor Evolution: From MOSFET to Tunnel-FET,"* Dr. Joao Antonio Martino, University of Sao Paulo, Brazil
- *"Evolution of Materials and Process Modules for future CMOS Technologies,"* Dr. Cor Claeys, imec/KU Leuven, Belgium
- *"Unprecedented Vision: From Quantum Dots to Silicon Imagers,"* Dr. M. Jamal Deen, McMaster University, Canada
- *"Recent advances in integrating III–V and Si photonics technology platforms,"* Dr. Mircea Guina, Tampere University of Technology, Finland

Approximately 70 people attended the Mini-Colloquium, including EDS members and students.

In the sequence of this Mini-Colloquium and in the same venue, on August 30th and September 1st, three EDS Distinguished Lecturers gave keynotes and invited papers at the 32th Symposium on Microelectronics Technology and Devices – SBMicro 2017:

- Keynote 1: *"Challenges for Advanced End of the Roadmap, Beyond Si and Beyond CMOS Technologies,"* Dr. Cor Claeys
- Keynote 2: *"Smart Sensors - Research, Trends and Opportunities,"* by Dr. Jamal Deen

EDS DL by Cor Claeys at the ED Brazil Mini-Colloquium

ED Brazil Mini-Colloquium 2017 organizers and Distinguished Presenters (left to right) Newton Frateschi, Jamal Deen, Paula Agopian, Cor Claeys, Joao Martino and Mircea Guina

- Invited presentation: *"Advances in multi-junction solar cells: the 50% conversion efficiency horizon,"* by Dr. Mircea Guina

SBMicro is the largest conference in Latin America in the field of micro and nanoelectronics, covering topics such as fabrication technology, sensors, modeling, device characterization and photonics. This year 50 papers were selected by the program committee and presented both orally and in the Poster Session. About 180 people registered for the conference, which is technically co-sponsored by the IEEE EDS. The SBMicro proceedings are available in the IEEE *Xplore* Digital Library.

~Joao Antonio Martino, Editor

Report on the 11th IEEE Regional Symposium on Micro & Nanoelectronics (RSM2017)

By Mohd Nizar Hamidon, Zubaida Yusof & Aliza Aini Md Ralib

The IEEE Electron Devices Society Malaysia Chapter organized the IEEE Regional Symposium on Micro and Nanoelectronics (RSM2017) at the Golden Sands Resort by Shangri La, Batu Feringgi, Penang, Malaysia, August 23–24, 2017. The conference was technically sponsored by the IEEE Electron Devices Society and the IEEE Malaysia Section, and was co-organized by the Institute of Advanced Technology, Universiti Putra Malaysia (UPM) and Universiti Sains Malaysia. This bi-annual technical conference since 1997 aims at bringing together researchers from industry and academia to gather and explore various issues and trends in the field of semiconductor electronics. Over the last eleven years, RSM conference series has become the prominent international forum on semiconductor electronics embracing all aspects of the semiconductor technology from circuit device, modeling and simulation, photonics and sensor technology, MEMS technology, process and fabrication, packaging technology and manufacturing, failure analysis and reliability, material and devices and nanoelectronics.

There were four main clusters in RSM2017, namely MEMS & Nanoelectronics, Nanophotonics, IC Design & Manufacturing as well as Material, Process & Product. A total of 66 papers were presented and more than 85 participants attended the symposium. On the first day of RSM2017, Prof. Dr. Ru Huang who is an IEEE EDS Distinguished Lecturer, IEEE Fellow and Region 10 SRC Chair who hails from the Institute of Microelectronics Beijing, Peking University, China, delivered her keynote speech entitled *"Steep-Slope Devices for Future Ultra-Low Power Applications."* Then, Professor El- Sayed Negim from Kazakh-British Technical University (KBTU), School of Chemical Engineering Almaty, Kazakhstan, presented the 2nd keynote speech entitled *"Photoluminescence studies on Dy(III)-dibenzoylmethane Ternary Complexes with 1, 10-Phenanthroline Derivatives"* through a video conference. The third keynote, Mr. Fakhrozi Che Ani who is a Senior Advanced Technology Engineer

A few committee members of IEEE RSM 2017 (from left) Dr. Jahariah, Dr. Noor Jannah, Dr. Norhayati, Dr. P. Susthitha and Dr. Mohd Nizar Hamidon

Participants of IEEE RSM 2017

Conference student travel grant award winners

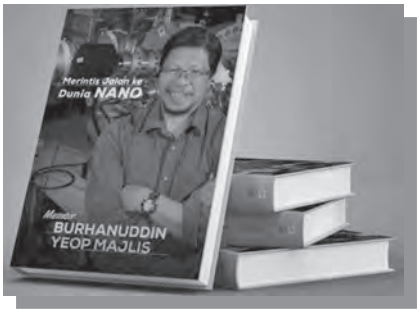
with Jabil Circuits Sdn Bhd Penang, gave his insights on the trend and development in flexible and stretchable printable electronic for IOT sensing applications. The fourth keynote, Prof. Ibrahim Ahmad from the Department of Electronics and Communication Engineering, Universiti Tenaga Nasional (UNITEN) gave his speech entitled, *"Development of Thin-Film CIGS Solar Cell Technology in Malaysia."*

During the conference, the EDS UKM Student Branch organized a membership drive utilizing the IEEE Conference Member Recruitment (CMR) program, and advertised EDS activities at a membership booth to encourage more participants to join the society.

This year, the chapter and the RSM2017 committee offered the inaugural Student Travel Grants to selected IEEE EDS student members, to attend the conference. In addition, academicians and industry personnel gave invited talks to impart their knowledge and experience to participants. Best Student Paper Awards as well as Best Student Presenter Awards were also given away to selected participants. We hope all these efforts will enhance the interest in electron devices research in Malaysia. The complete list of award winners are as follows:

RSM2017 Conference Student Travel Grant Award:

1) Nurul Hidah Sulimai, Universiti Teknologi MARA



The book launching by IEEE EDS Malaysia Advisor

2) Norliana Yusof, Universiti Kebangsaan Malaysia
3) Ma Li Ya, University of Malaya

Best Student Paper Award:

- *"Impacts of fin width scaling on the electrical characteristics of 10-nm FinFET at different metal gate work function,"* by Nurul Aida Farhana Othman, Sharifah Fatmadiana Wan Muhamad Hatta and Norhayati Soin (MEMS & Nanoelectronics Cluster)
- *"Graphene-based Surface Plasmon Resonance Urea Biosensor using Kretschmann configuration,"* by Nur Akmar Jamil, P. Susthitha Menon, Fairus Atida Said, Kalaivani Tarumaraja, Gan Siew Mei Burhanuddin Yeop Majlis (Nanophotonics Cluster)
- *"Deposition Temperature Dependence of ZnO Nanostructures Growth using TCVD for EGFET pH Sensor,"* by Aimi bazilah Rosli, Zaiki Awang , Shafinaz Sobihana Shariffudin and Sukreen Hana Herman (Material, Process & Product Cluster)
- *"Assessing the NSOP (non stick on pad) bond pad by EDX, XPS and TofSIMS analysis,"* by Lai Chin Yung , Ho Ing Hong and Cheong Choke Fei (IC Design & Manufacturing Cluster)

Best Presenter Awards:

- Hoe Chee Ling, for the presentation of the paper entitled *"DNA/AuNP-Graphene Back-gated Field Effect Transistor as a Biosensor for Lead (II) Ion Detection"*
- Nurul Hidah Sulimai, for the presentation of the paper entitled *"One Step Precipitation of CaCO3 Nanoparticles assisted by Drying and Hydrothermal Method"*
- Adilah Ayoib, for the presentation of the paper entitled *"Low Cost Design and Fabrication of PDMS Microfluidics Micromixers for DNA Extraction"*
- Sharifah Fatmadiana Wan Muhamad Hatta, for the presentation of the paper entitled *"The influence of shallow trench isolation angle on hot carrier effect of STI-based LDMOS transistors"*

Congratulations to all winners!!

~ P Susthitha Menon, Editor

Regional News

Europe, Middle East & Africa (Region 8)

ED Scotland

—by Marc Desmulliez

In November of last year, the Scottish Chapter of the IEEE Electron Devices Society was very pleased to host a lecture by Professor Kunihiro Asada, Director of the VLSI Design and Education Center (VDEC) at the University of Tokyo. Professor Asada presented the exciting work going on within the VDEC research facility to an audience of academics, industrialists and research students at the University of Edinburgh's Institute for Integrated Micro and Nano Systems (IMNS). In particular, he spoke on two of his current research interests. The first of these was the development of integrated magnetic sensors that enable the diagnosis of semiconductor devices. He then went on to describe his laboratory's work on single photon avalanche diode (SPAD) arrays with fast access circuits. The chapter would like to thank Professor Asada for his stimulating talk and for taking the time after his presentation to discuss his work further with interested members of the audience.

Professor Kunihiro Asada of the University of Tokyo with former ED Scotland Chair Professor Anthony Walton of the University of Edinburgh

~ Jonathan Terry, Editor

ED/AP/MTT/COM/EMC Tomsk Chapter

—by Oleg Stukach

Our Tomsk Chapter has regularly organized conferences on various fields not only in the Siberia region. First Euro-Asian Conference on Future Energy together with International Siberian Conference on Control and Communications (SIBCON) was held in June in Astana, capital of Kazakhstan with EDS technical co-sponsorship. The financial support was provided by Saken Seifullin Kazakh Agrotechnical University. Since 1995, SIBCON has been organized biannually. It focuses on advances in devices for control, communications and technology innovations from different points of view, in order to improve the understanding in the field. Our goal is also a propagation of EDS development by formation of the chapters. We believe that it is necessary to form chapters in big academic and industrial cities of Kazakhstan by fields of strategic activities: communication, control, future green agriculture, energetics.

Representatives of different Kazakh, Siberian, foreign academia, and R&D companies participated in the conference. A high professional activity was demonstrated by participants. The invited and regular papers were presented in 32 oral sessions organized in 8 tracks. The sessions addressed key problems of modern electronic devices, modern manufacturing technologies, as well as some related topics. Different types of presentations were made, namely ordinary presentations, new ideas, valuable conclusions from experience, the state-of-the art and instructive survey communications. All presented papers were published in IEEE *Xplore*. Several active conference participants, both engineers and students, received best paper awards.

A tutorial on the modern level of technical and information means usage in measurement services was also organized by R&D branch of National Instruments Russia. The conference included also the special session "Join the IEEE" demonstrating the Institute membership benefits.

One of the best traditions of Tomsk conferences, the social program, was particularly rich and included the banquet with Astana street seeing tour. Astana is a brilliant city merging historical and modern objects. It is a new

Participants of the SIBCON 2017 Conference

venue for the IEEE events due to luxurious places, the exotic culture, and excellent service. An increased interest in the Tomsk Chapter conferences was clearly observed. We cordially invite you to the Moscow Workshop on Electronic and Networking Technologies (MWENT) in March 14–16, 2018. For more information visit, http://mwent.hse.ru.

Finally, the Tomsk Chapter thanks EDS for sponsorship and hopes for the continuation of mutually advantageous cooperation.

MTT/ED/AP/EP/SSC West Ukraine Chapter

(XXII International Seminar/Workshop DIPED-2017)

—by Mykhaylo Andriychuk

The XXII International Seminar/Workshop on Direct and Inverse Problems of Electromagnetic and Acoustic Wave Theory (DIPED-2017) was organized by the MTT/ED/AP/EP/SSC West Ukraine and MTT/ED/AP Georgian Chapters. This year, DIPED was held at Oles Honchar Dnipro National University (DNU), Dnipro, Ukraine, on September 25–28. Besides DNU, DIPED-2017 was co-organized by Ivane Javakhishvili Tbilisi State University (TSU) and Pidstryhach Institute for Applied Problems of Mechanics and Mathematics, NASU, Ukraine. The IEEE Electron Devices Society, Antennas & Propagation Society, and Microwave Theory & Techniques Society provided the technical co-sponsorship for the Seminar/Workshop. The IEEE Solid State Circuits Society and IEEE Ukraine Section were the supporting IEEE institutions.

Prof. Oleg O. Drobakhin, Chairman of the Organizing Committee, Dr. Tamar Gogua, IEEE MTT/ED/AP Georgian Chapter Secretary, and Prof. Kakhaber Tavzarashvili, IEEE MTT/ED/AP Georgian Chapter Chairman, expended alot of effort for the general and local organization of the event.

The DIPED-2017 technical program consisted of 57 papers, including 5 invited talks. Scientists from Georgia, Germany, Greece, Israel, Russia, South Africa, Turkey, and Ukraine brought forward their works. The papers were arranged at the following sections:

- Diffraction and Scattering,
- Waveguide and Layered Structures,
- Inhomogeneous Media,
- EM Field Applications,
- Antenna Design,
- Numerical Computational Techniques,
- Acoustics and Application.

Prof. Oleg O. Drobakhin, DIPED-2017 Organizing Committee Chairman, presenting the historical overview about the Department of Applied and Computer Radiophysics at the Oles Honchar Dnipro National University

Like previous years, many regular students, PhD students and young scientists attended the Seminar/Workshop. The Best Young Speaker Awards were granted to five researchers:

- Mr. Giorgi Kapanadze (Ivane Javakhishvili Tbilisi State University, Tbilisi, Georgia) for *"ELF Radio Emission Associated With Strong M6.0 Earthquake"*;
- Mr. Vyacheslav Gorev (Oles Honchar Dnipro National University, Dnipro, Ukraine) for *"On the Kinetics of a Many-Body Dissipative System Placed in a Random Field"*;
- Mr. Pavle Tsotskolauri (Ivane Javakhishvili Tbilisi State University, Tbilisi, Georgia) for *"Tbilisi State University Extremely Low Frequency Radiation Research Net (ELFTSU Net): the First Measurements at Station Locations"*;
- Mr. Mykola Medvedev (V. N. Karazin Kharkiv National University, Kharkiv, Ukraine) for *"Electromagnetic Near-Field of Arc Slot, Cut in Coaxial Line Shield"*;
- Mr. Evhen Shulga (O. Ya. Usikov Institute of Radiophysics and Electronics, NASU, Kharkiv, Ukraine) for *"Interaction of Eigen Oscillations in a Cylindrical Cavity with Composite Material"*

The recipients of the Awards were recognized with a special certificate from the Program Committee and a financial grant from the Organizing Committee.

Following the DIPED tradition, free lobby discussions were a considerable part of the conference.

An excursion tour to the Aero Cosmic National Center in Dnipro, where the latest achievements in the field of rocket engineering and space technology of the former Soviet Union and independent Ukraine are demonstrated, and a bus tour to the ancient Cossack fortress, Kodak, were organized in the framework of the Seminar/Workshop social program.

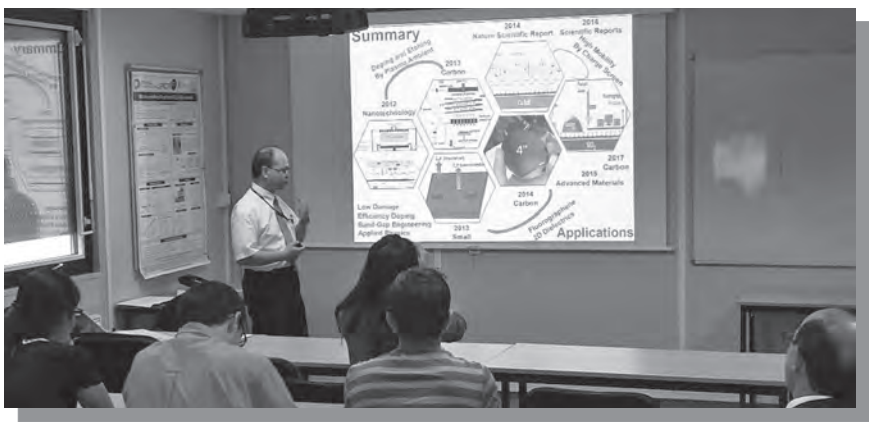
The traditional Seminar/Workshop dinner was held after closing of the technical program and included presentations of the The Best Young

Speaker Awards, Discussions were held on the improvement of the Seminar/Workshop format, with comments and recommendations of the participants taken into consideration.

It was announced by the organizers that the next XXIII International Seminar/Workshop DIPED will be held at the Samtskhe-Javahheti State University, Akhaltsikhe, Georgia, on September 24–27, 2018. Previous attendees and new participants are cordially invited. The reports on previous DIPED editions and information about forthcoming events are available at the following websites: http://www.ewh.ieee.org/soc/cpmt/ukraine/ and http://ewh.ieee.org/r8/ukraine/georgian/DIPED/.

~ Daniel Tomaszewski, Editor

(left to right): Dr. Mohamed Boutchich, Assoc. Prof. in El. Eng., University Pierre and Marie Curie, Prof. C. - S. Lai, Chang Gung University, Taiwan, Dr. Pere Roca I Cabarrocas, Head of LPICM Lab Ecole Polytechnique, CNRS, France



Prof. Chao-Sung Lai during his distinguished lecture

EDS Distinguished Lecture – Chao Sung Lai, "Graphene with Flourine and Nitrogen Doping for Transistors and its Applications"

—by Mohamed Boutchich

At the invitation of Dr. Mohamed Boutchich from University Pierre and Marie Curie and the Labex Nano-Saclay, Prof. Chao-Sung Lai presented his current achievements on graphene with fluorine and nitrogen doping for transistors and its applications. The seminar was held on July 11, 2017 at Ecole Polytechnique Palaiseau, France, in The Laboratory of Physics of Interfaces and Thin Films (LPICM, headed by Dr. Pere Roca I Cabarrocas).

In his talk, Prof. Lai promoted the IEEE Electron Devices Society to researchers and students. There were about thirty attendees and we had a fruitful discussion on the functionalization of graphene and the electronic properties suitable for various devices including memories. Prof. Lai presented a novel graphene based insulator, fluorographene applied as gate dielectric in the field effect transistor with data on the dielectric quality, dielectric constant, breakdown electric field and thermal stability. He also presented a scalable single-step fabrication process of single atomic-layer transistors by the selective fluorination of graphene using a low-damage CF_4 plasma treatment, where the generated fluorine radicals preferentially fluorinated the graphene at low temperature (T < 200 °C) while defect formation was suppressed by screening out the effect of ion damage.

The fluorographene was also implemented as a passivation layer to decouple graphene from its substrate and the mobility was substantially improved. At the end, Prof. Lai presented the integration of graphene nano discs (GNDs), functionalized using NH_3 plasma to be implemented as charge trapping sites (CTSs) for non-volatile memory applications. A GND density as high as 8×10^{11} cm^{-2} and a diameter of approximately 20 nm were achieved. This inherently enhances the density of CTSs in the GNDs and as a result, the charge loss is less than 10% for a 10-year data retention testing, making this low-temperature process suitable for low-cost non-volatile memory applications on flexible substrates.

EDS Distinguished Lecture – Reliability of Scaled Metal Gate/ High-K CMOS Devices at the CAS/ED Switzerland Chapter

—by Shih-Chii Liu

Andreas Kerber from GlobalFoundries recently gave an IEEE EDS Distinguished Lecture on high-k CMOS devices. The talk was presented on November 27, 2017, at IBM Zurich, Switzerland, under the auspices of Jean Fompeyrine.

Andreas Kerber giving his DL talk at IBM Zurich

Prof. Vijay K. Arora, Wilkes University, gave an IEEE EDS Distinguished Lecture at Tohoku University in Sendai, Japan on October 27, 2017

Dr. Kerber's lecture on the aggressively scaled transistor technologies with metal gate/high-k stacks was an excellent overview on reliability issues on HKMG, in particular useful for non-experts in the field. He discussed how to obtain stochastic BTI data for discrete SRAM and logic device beyond 3s, address device-to-circuit correlations using ring-oscillators and explore self-heating effects in FinFET and SOI devices.

There was a lot of interaction between the speaker and audience during and after the presentation. A list of other DLs organized by the CAS/ED Chapter can be found on https://www.ieee.ch/chapters/cas-ed/cas-ed-news/.

~ Jan Vobecky, Editor

Attendees with Dr. Arora, Tohoku University in Sendai, Japan

Asia & Pacific (Region 10)

EDS Distinguished Lecture at ED Japan Chapter

—by Masaaki Niwa and Takahiro Shinada

The EDS Japan Joint Chapter (Chair: Masaaki Niwa) held an EDS Distinguished Lecturer program on October 27th in Sendai, Japan, co-hosted with Center for Innovative Integrated Electronic Systems (Director: Tetsuo Endoh), Tohoku University. Prof. Vijay K. Arora, Wilkes University, lectured on "Ohm to Arora: A New Paradigm for Nanoscale Devices and Circuits", in which a newfangled paradigm through deployment of the nonequilibrium Arora's distribution function (NEADF) for resistance surge in low-dimensional nano-resistors were introduced. After his talk, a wide range of issues from basic sciences to engineering were discussed with the attendees.

~ Kuniyuki Kakushima, Editor

EDS Distinguished Lecture – ED Dalian Chapter

- by Zhengxing Huang

As a national integrated circuit international talent training base, the ED Dalian Chapter is supported by the State Administration of Foreign Experts Affairs (SAFEA). On August 24th, our chapter organized a seminar about IC talent training. Dr. Yu introduced main efforts and some progress has been made in our chapter.

IC talent training session at ED Dalian Chapter

President Su Guangming shared some good advice.

EDS Distinguished Lectures at ED/SSC Shenzhen Chapter

—by Qian Li

The ED/SSC Shenzhen Chapter of the IEEE Beijing Section held two invited talks during the past quarter. On April 13, 2017, by Prof. Deji Akinwande from University of Texas, Austin. His talk titled, *"From Ordinary to Extraordinary: 2D Materials, Devices and Systems,"* presented his latest research advances on 2D nanomaterials towards greater scientific understanding and advanced engineering applications. In particular, the talk highlighted their work on flexible devices and nanoelectronics, wearable sensors, straintronics, topological insulators, 2d memory and nonvolatile switches, and new transistor concepts. This talk was organized by Prof. Min Zhang, attended by Prof. Qian Li, Prof. Hailong Jiao and about 20 graduate students.

On May 8, 2017, Prof. Charles Surya from Hong Kong Polytechnic University gave a talk titled, *"Investigation of High Efficiency Perovskite-based Solar Cells."* He presented an overview of different approaches to accomplish high PCE in PSCs including: i.) improvement of the absorber layer; ii.) enhancement in the device structure; and iii.) incorporation of the light trapping structures. He began by presenting different growth techniques reported for the cultivation of high quality MAPI films including: i.) solvent engineering; ii.) vapor assisted process (VASP); and iii.) hybrid chemical vapor depositions (HCVD) technique. Experimental studies conducted in their group demonstrate that significant improvement in the PCE can be achieved by dry O_2 treatment of the MAPI layer. Experimental results on photothermal deflection spectroscopy (PDS) show that O_2 annealing leads to significant reduction in the localized states in the MAPI layer, which is shown to be the key factor underlying the observed enhancement in the PCE. He has presented a detailed discussion on the HCVD growth process that utilizes a N_2/O_2 carrier gas resulting in significant enhancement in the PCE.

(Middle) Prof. Charles Surya (speaker), Prof. Shengdong Zhang, Prof. Min Zhang, Prof. Xinnan Lin, Prof. Qian Li, Prof. Hang Zhou and graduate students

This talk was organized by Prof. Qian Li, attended by Prof. Shengdong Zhang, Prof. Min Zhang, Prof. Xinnan Lin, Prof. Hang Zhou and more than 30 graduate students.

EDS Distinguished Lecture – ED Tsinghua University Student Branch Chapter

—by Yancong Qiao

The EDS Tsinghua University Student Branch Chapter organized a few DLs during the month of July, with the first held DL on July 22nd. Prof. Peide D. Ye, from the School of Electrical and Computer Engineering, Purdue University,

Prof. Deiji Akinwande and organizer Prof. Min Zhang (middle), with Prof. Qian Li, Prof. Hailong Jiao and graduate students

Photos from the three events organized by the ED Tsinghua University Chapter

USA, gave a talk titled, *"2D Materials and Devices."* He reviewed the state-of-the-art 2D semiconductor materials research and development in recent years and highlighted a couple of new breakthroughs in his research group such as: (1) integration of CMOS compatible ferroelectric $HfZrO_2$ gate stack on 2D materials to realize steep slope negative capacitance field-effect transistors, (2) realization of black phosphorus 2D transistors with record drain currents beyond 1A/mm, and (3) exploration of a new class of 1D van der Waals materials – Te and Se – which has narrow bandgap, high carrier mobility and air stability. This talk was attended by about 20 graduate students, professors, and post-doc researchers.

The student branch chapter held its second DL on July 24th, with Prof. H.-S. Philip Wong, from the School of Electrical Engineering, Stanford University, USA. His talk titled, *"Reaching for the N3XT 1.000X of Computing Energy Efficiency,"* was attended by around 20 graduate students, professors, and post-doc researchers.

The third DL on July 5th, by Prof. Mansun Chan, from the Department of Electronic and Computer Engineering at Hong Kong University of Science & Technology was titled, *"Nano-device challenges in the Post-Moore Era."* Prof. Chan's talk was attended by around 20 graduate students, professors, and post-doc researchers.

EDS Distinguished Lecture – ED Harbin Chapter

—by Dongpeng Kang

Prof. Dongpeng Kang, the secretary of the ED Harbin Chapter invited Dr. Feihu Xu, Massachusetts Institute of Technology, to give a DLon July 21, 2017. The talk was titled *"Quantum Communication and Imaging with Photons."* Dr. Xu first introduced the basics of quantum key distribution (QKD) to the audience and addressed a list of the most frequently asked questions about QKD: (i) What quantum code-breaking can do? (ii) What QKD (code-making) can do? (iii) How to achieve perfect security in a quantum world? He then further presented their recent developments in Si integrated photonic-chip based QKD and measurement-device-independent QKD (MDI-QKD).

Dr. Feihu Xu (6th from the front right) pictured with audience after the talk

In the second part of the talk, Dr. Xu presented how to perform accurate 3D imaging or remote sensing with a single-photon camera at a light level of one photon per pixel and how to perform non-line-of-sight (NLoS) imaging. He showed their novel photon-efficient imaging algorithm and systems that can achieve long-range dynamic sensing, robust NLoS imaging and push the limits of imaging technology in widespread applications. Dr. Xu had a discussion with our faculty and students after the talk.

EDS Distinguished Lecture – ED Beijing Chapter

—by Kangwei Zhang

On July 21st, Prof. H.-S. Philip Wong visited the ED Beijing Chapter. He delivered a DL titled *"Phase Change Memory"* hosted by Prof. Ming Liu, the Chapter Chair. More than 30 local professionals and graduate students attended the meeting.

Prof. Wong explained that Phase-change memory (PCM) has undergone significant academic and industrial research in the last 15 years. After much development, it is now poised to enter the market as a storage class memory (SCM), with performance and cost between that of NAND flash and DRAM. In this talk, Prof. Wong reviewed the history of phase-transforming chalcogenides leading up to our current understanding of PCM as either a storage-type SCM, with high-density and better than NAND flash endurance, write speeds, and retention, or a memory-type SCM, with fast read/write times to function as a non-volatile DRAM. Several of the key findings from the community relating to device dimensional scaling, cell design, thermal engineering, material exploration, and storing multiple levels per cell (MLC) was discussed. These areas have dramatically impacted the course of development and understanding of PCM.

On August 29th, Dr. Yang Chai visited the chapter and delivered a DL titled *"Two-Dimensional Layered Materials for Nanoelectronics – Interconnect and Transistor."* The DL was hosted by Prof. Hangbing Li and attracted more than 30 local professional and graduate students attendees.

Distinguished Lecture at ED Beijing Chapter

Graphene has ultra-thin thickness (<1 nm), single-crystal hexagonal structure, high impermeability, excellent electrical conductivity and high thermal stability. These properties make graphene-based materials promising for the barrier of a Cu interconnect. The density function theory calculation from Dr. Chai suggests that Cu species can penetrate graphene nanosheets through defects that are larger than 0.25 nm^2. The intrinsic defects in as-grown graphene can be avoided by layer-by-layer graphene transfer process. As a result, the thickness of graphene barrier for completely blocking Cu migration can be 5 times smaller than that of conventional TaN barrier. The graphene barrier also inhibits electrochemical reactions and reduces Cu ion density at the interface between Cu and SiO_2. The crystal structure and physical properties of two-dimensional transition metal dichalocogenides (TMDs) are substantially dependent on the filling of *d*-orbitals of transition metal. Group-10 TMDs have been revealed with widely tunable bandgap, high mobility and good stability. Dr. Chai demonstrated layer-dependent semiconductor-to-semimetal evolution of 2D $PtSe_2$. Few-layer $PtSe_2$ field-effect transistor shows high room-temperature mobility (~210 $cm^2V^{-1}s^{-1}$) in a back-gated configuration on SiO_2/Si,

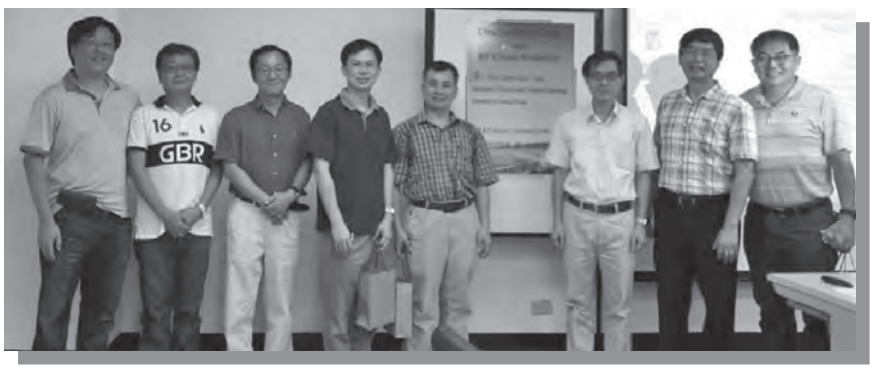
Dr. Yang Chai (6th from left) pictured with the audience after the talk

comparable to that of BP. Bulk $PtSe_2$ device exhibits the metallic-like conductivity (6.64×10^5 S/m). The characteristics of widely tunable bandgap of $PtSe_2$ allows it to be effectively response to near-infrared light. Furthermore, the results showed that $PtSe_2$ has much better air-stability (over 1 year) than BP.

EDS Distinguished Lecture – ED Tainan Chapter

—by Wen-Kuan Yeh

The EDTainan Chapter held one Distinguished Lecture in Pingtung, Taiwan, on August 16, 2017. Dr. Jiann-Shiun Yuan, Professor of Electrical Engineering, University of Central Florida, gave the talk at National Pingtung University (NPTU). The talk titled, *"Ultra-Low Power Design and RF Circuit Reliability,"* focused on the Design and reliability of Low-Power Devices on IoT Applications. About 50 students and several professors of local universities attended.



(from right to left) Dr. Po-Ying Chen (professor of NCUT), Prof. Jiann-Shiun Yuan (DL Speaker), Dr. Prof. Lung-Jen Wang (Dean of CS, NPTU), Prof. Wen-Kuan Yeh (Chair of EDS Tainan Chapter) and Prof. Ting-Kuo Kang (Professor of CSU), and some attendees

EDS Exploration Camp – EDS UCAS Student Chapter and ED Beijing Chapter

—by Tiancheng Gong

The first IEEE Electronic Exploration Camp in IMECAS, Beijing, China, was launched on July 15–18, 2017, at the Institute of Microelectronics of Chinese Academy of Sciences by the IEEE EDS UCAS Student Chapter and the ED Beijing Chapter. The camp was led by Tiancheng Gong, a student volunteer with the help of Prof. Baoqin Chen and Prof. Ming Liu of IMECAS. Prof. Mansun Chan from Hong Kong University of Science and Technology, gave us a lot of training and suggestions on this activity and came on the first day to give a welcome to all the students. About 40 students from Beijing, Xi'an, Nanjing et. al, attended the 4-day camp where they constructed a DIY running light, electronic piano, infrared detector and digital counter, with the help of 6 volunteers.The camp has successfully stimulated the interest of the participants on electronic technology

2017 IEEE Electronic Exploration Camp participants

and cultivated their ability in problem solving. The parents of these students were satisfied with all the arrangements of the schedule, the design of the courses, and gave a good evaluation of this camp. We expect to host a larger scale electronic camp in the near future.

~ Ming Liu, Editor

ED Malaysia Kuala Lumpur Chapter

—by Norhayati Soin, Noorjannah Ibrahim & Aliza Aini Md Ralib

DL Talk by Dr. Ru Huang

The Chapter organized an EDS Distinguished Lecture by Prof. Dr. Ru Huang on August 21, 2017, at the Institute of Microengineering and Nanoelectronics (IMEN), Universiti Kebangsaan Malaysia. The talk was co-organized by the IEEE EDS UKM Student Branch. Prof. Dr. Ru Huang is an IEEE Fellow and EDS Region 10 SRC Chair, who hails from the Institute of Microelectronics Beijing, Peking University, China. Her talk on *"Steep-Slope Devices for Future Ultra-Low Power Applications"* successfully attracted about 20 participants from IMEN staff, postgraduates and researchers. The talk mainly touched on a new kind of device with injection-tunneling hybrid-control mechanism, which is different from traditional tunneling FET, called the Multi-finger Schottky barrier TFET (MFSB-TFET). The device in circuit level shows different power reduction degrees under various operating frequencies, compared to the traditional TFET and MOSFET-based circuits. After the talk, Dr. Huang discussed various issues with the Chapter and Student Branch committee members and recommended some improvement plans.

Technical Visit to NTU and SUTD Singapore

The ED Malaysia Chapter, the UKM EDS Student Branch and students from UiTM Shah Alam, organized a technical visit to the School of Electrical and Electronic Engineering, Nanyang Technology University and Singapore University of Technology and Design (SUTD) Lab, July 9–11,2017. SUTD was established to advance knowledge and nurture technically grounded leaders and innovators to serve societal needs, through a focus on design and multi-disciplinary curriculum and research. The objective of this program was to give motivation and exposure to all 25 participants on the recent research conducted in SUTD Lab and NTU.

Industrial Visit to Jabil Circuits Penang

The Chapter organized a technical visit to Jabil Circuits Sdn Bhd Penang

Participants of the DL talk of Prof. Ru Huang

Participants of the technical visit to NTU and SUTD Lab

Participants of industrial visit to Jabil Circuits

on August 22nd. The objective of this program was to strengthen industry linkages and to understand the trend of development in flexible and stretchable printable electronic in IOT sensing applications at Jabil Circuits. Seven EDS members, including DL Lecturer Prof. Ru Huang, participated in the industrial visit.

2017 EDS Malaysia Chapter Postgraduate Awards

During the RSM2017 Conference Dinner on August 23rd, the 2nd IEEE EDS Malaysia Postgraduate Awards were given away to shortlisted IEEE EDS student members who are pursuing their MSc and PhD research in Malaysia. The winners were Mohamad Faris bin Mohamad Fathil from UNIMAP with his PhD project "*Electrical Label-Free Sensing of Cardiac Troponin Biomarker: ZnO-NPs FET based Integration with Substrate-gate Coupling*"(MEMS & Nanoelectronics cluster);, Fairus Atida Said from UKM with her PhD project "*SPR-based Sensor for Urea Detection on Nanolaminated Gold Film Using Kretschmann Configuration*" (Nanophotonics Cluster); and Kang Chun Hong from UTP with his PhD project "*Development of Carbon Nanotube-Graphene Composite as Transparent Conductive Electrode for GaN-based LED*" (Material, Process & Product cluster). Each winner received an honorarium of RM100, a certificate and plaque. During the conference dinner, EDS Malaysia Advisor, Prof. Dato Dr. Burhanuddin Yeop Majlis also launched his memoir cum autobiography entitled, *"Merintis Jalan ke dunia NANO" (Pioneering the way to the NANO world).*

~P Susthitha Menon, Editor

Conference Dinner Attendees and one of the Award winners (right photo)

EDS MEETINGS CALENDAR

THE COMPLETE EDS CALENDAR CAN BE FOUND AT OUR WEB SITE: HTTP://EDS.IEEE.ORG. PLEASE VISIT.

2018 18th International Workshop on Junction Technology (IWJT)	08 Mar - 09 Mar 2018	Fudan University 220 Handan Road Shanghai, China
2018 IEEE International Reliability Physics Symposium (IRPS)	11 Mar - 15 Mar 2018	Hyatt Regency San Francisco Airport 1333 Bayshore Highway Burlingame, CA, USA
2018 19th International Symposium on Quality Electronic Design (ISQED)	13 Mar - 14 Mar 2018	Santa Clara Convention Center 5001 Great America Pkwy Santa Clara, CA, USA
2018 IEEE 2nd Electron Devices Technology and Manufacturing Conference (EDTM)	13 Mar - 16 Mar 2018	Kobe International Conference Center 6-9-1 Minatojima-nakamachi Chuo-ku Kobe, Japan
2018 Moscow Workshop on Electronic and Networking Technologies (MWENT)	14 Mar - 16 Mar 2018	Ilya Ivanov 34 Tallinskaya Str. Moscow, Russia
2018 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS)	19 Mar - 21 Mar 2018	Hotel Abba Granada Avenida Constitucion, 21 Granada, Spain
2018 IEEE International Conference on Microelectronic Test Structures (ICMTS)	26 Mar - 29 Mar 2018	Courtyard Marriott Downtown 300 E 4th St. Austin, TX, USA
2018 International Symposium on VLSI Design, Automation and Test (VLSI-DAT)	16 Apr - 19 Apr 2018	Ambassador Hotel Hsinchu 188 Chung Hwa Road, Section 2, Hsinchu, Taiwan Hsinchu, Taiwan
2018 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA)	16 Apr - 19 Apr 2018	Ambassador Hotel Hsinchu 188 Chung Hwa Road, Section 2 Hsinchu, Taiwan
2018 IEEE International Vacuum Electronics Conference (IVEC)	24 Apr - 26 Apr	Monterey Marriott 350 Called Principal

2018 IEEE International Vacuum Electronics Conference (IVEC)	24 Apr - 26 Apr 2018	Monterey Marriott 350 Called Principal Monterey, CA, USA
2018 29th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC)	30 Apr - 03 May 2018	Saratoga Springs City Center 522 Broadway Saratoga Springs, NY, USA
2018 7th International Symposium on Next Generation Electronics (ISNE)	07 May - 09 May 2018	GIS TAIPEI TECH Convention Center (Building Everlight)2~3F., Ln. 193, Sec. 3, Zhongxiao E. Rd., Da'an Dist., Taipei City 106, Taiwan Taipei, Taiwan
2018 IEEE 30th International Symposium on Power Semiconductor Devices and IC's (ISPSD)	13 May - 17 May 2018	Palmer House Hilton 17 East Monroe Street Chicago, IL, USA
2018 IEEE International Memory Workshop (IMW)	13 May - 16 May 2018	Westin Miyako Kyoto 1 Awataguchi Kachocho,Higashiyama-ku Kyoto 605-0052 Kyoto, Japan
2018 National URSI Symposium (URSI)	15 May - 17 May 2018	Poznan Congress Center Glogowska 14 Poznan, Poland
2018 IEEE International Interconnect Technology Conference (IITC)	03 Jun - 07 Jun 2018	To Be Determined Burlingame, CA, USA
2018 IEEE 45th Photovoltaic Specialists Conference (PVSC)	10 Jun - 15 Jun 2018	Hilton Waikoloa Village 69-425 Waikoloa Beach Dr Waikoloa Village, HI, USA
2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)	10 Jun - 12 Jun 2018	Philadelphia Convention Center 1101 Arch St Philadelphia, PA, USA
2018 IEEE Symposium on VLSI Technology	18 Jun - 22 Jun 2018	Hilton Hawaiian Village Honolulu, HI, USA
2018 25th International Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD)	03 Jul - 06 Jul 2018	Ryukoku University Avanti Kyoto Hall 31 Nishi Sanno-cho Higashi Kujo Minami-ku Kyoto, Japan
2018 International Flexible Electronics Technology Conference (IFETC)	07 Aug - 09 Aug 2018	Delta Hotels Ottawa City Centre 101 Lyon St N Ottawa, ON, Canada

2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)	14 Oct - 17 Oct 2018	San Diego, CA, USA
2018 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)	05 Nov - 08 Nov 2018	Hilton San Diego Resort and Spa 1775 East Mission Bay Drive San Diego, CA, USA
2018 IEEE International Electron Devices Meeting (IEDM)	29 Nov - 07 Dec 2018	Hilton San Francisco San Francisco, CA, USA
2018 IEEE 49th Semiconductor Interface Specialists Conference (SISC)	05 Dec - 08 Dec 2018	Catamaran Resort Hotel 3999 Mission Boulevard San Diego, CA, USA

IEEE Journal of the Electron Devices Society

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Inaugural Ceremony of IEEE 'EDS Center of Excellence' at Heritage Institute of Technology, Kolkata, India On 21 December 2017

The IEEE **EDS Center of Excellence** at the Heritage Institute of Technology (HITK) was formally inaugurated on 21st December 2017. The ceremony began with a briefing about the proposed activities of the Center followed by a welcome address by Prof. Pranay Chaudhuri, Principal, Heritage Institute of Technology.

The Head of the Department of Electronics and Communication Engineering, Prof. Prabir Banerjee expressed his best wishes to the faculty coordinators, Prof. Mousiki Kar and Prof. Atanu Kundu for establishing this EDS Center of Excellence.

The inauguration was formally done by singing the Saraswati Vandana and lighting of the sacred lamp by the dignitaries, viz. Prof. B.R. Saha, Registrar, Prof. B.B. Paira, Advisor-Higher Education, Mr. Probir Roy, Director, Mr. P.K. Agarwal, Chief Executive Officer, and Prof. Pranay Chaudhuri, Principal, HITK, Prof. Subhashis Majumder, Dean (UG), Prof. N.P. Nayak, Dean (Student Affairs), Prof. Atanu Kundu, Chairman, IEEE ED Kolkata Chapter and Advisor, IEEE ED HIT Student Branch Chapter, Prof. Mousiki Kar, Treasurer, IEEE ED Kolkata Chapter and Branch Counselor, IEEE ED HIT SBC, and the Chief guest Prof. Sujit Biswas, Chairman, IEEE Kolkata Section.

The Chief Guest congratulated the initiative and remarked that it shall be a valuable addition to the activities of the IEEE Kolkata Section. He was presented with an Institute memento and a small token of appreciation from the IEEE ED HIT SBC by Prof. Atanu Kundu.

Inauguration by lighting of lamp by the dignitaries present

A message sent by Prof. Samar K. Saha, IEEE EDS President, was read to the participants who received it with warmth and regards.

The event wrapped up with a vote of thanks by Prof. Mousiki Kar to the faculty, staff, other participants, and everybody who made the establishment of the Center possible.

Mousiki Kar
ED Kolkata Chapter
Heritage Institute of Technology
Kolkata, India

Group photo with all the participants of the Inaugural ceremony

EDS Vision, Mission and Field of Interest Statements

Vision Statement
Promoting excellence in the field of electron devices for the benefit of humanity.

Mission Statement
To foster professional growth of its members by satisfying their needs for easy access to and exchange of technical information, publishing, education, and technical recognition and enhancing public visibility in the field of Electron Devices.

EDS Field of Interest
The EDS field-of-interest includes all electron and ion based devices, in their classical or quantum states, using environments and materials in their lowest to highest conducting phase, in simple or engineered assembly, interacting with and delivering photo-electronic, electro-magnetic, electromechanical, electro-thermal, and bio-electronic signals. The Society sponsors and reports on education, research, development and manufacturing aspects and is involved in science, theory, engineering, experimentation, simulation, modeling, design, fabrication, interconnection, reliability of such devices and their applications.