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Technical Briefs

Marvels in Process Technology Before and During Moore's Law Era

By Joachim N. Burghartz, Institut für Mikroelektronik Stuttgart (IMS CHIPS), Germany

Process technology has always been the guiding and decisive factor in keeping Moore's Law going. Since the 1980's, the semiconductor roadmap helped us looking at the processing needs ahead—this was well coordinated 'engineering on demand' by semiconductor manufacturers, equipment vendors and academics with countless brillant efforts and results on the way. However, there were also marvels in process technology that came out of the blue or with an impact that was not foreseen at all. This third article of the series on 'Marvels of Microelectronics Engeneering' will highlight a few of those.

One might think that in the years before Moore's Law was formulated technology progress in semiconductors was solely based on marvellous discoveries. According to Adolf Goetzberger, former director of the Fraunhofer Institute for Applied Solid State Physics and retired founding director of the Fraunhofer Institute for Solar Energy Systems in Freiburg, Germany, this was, however, not the case in the old days. Goetzberger worked with Shockley from 1958 to 1963 after in 1957 the 'Traitorous Eight' left Shockely Laboratories in Palo Alto. In my recent personal conversation with him he rememberd about Shockley: "We had agreed that I would be in charge of the experiments and he would do the theory. This turned out to become a very good collaboration". Apparently, the theoretical work by Shockley came first and experiments followed to demonstrate the theories. This approach might have been triggered by

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Marvels in Process Technology before and during Moore's Law Era

(continued from page 1)

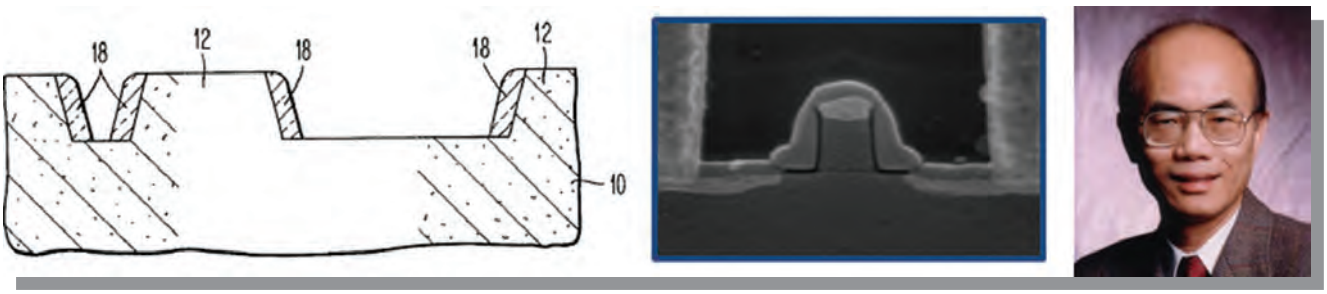
Former Shockley Laboratories in Palo Alto (left) and Adolf Goetzberger, research staff at Shockley Labs in the 1960's (Images provided by Adolf Goetzberger)

Shockely's personal experience from the demonstration of the first transistor by Bardeen and Braittain in 1947; it was just after the transistor was demonstrated experimentally that Shockley could complement that birth of semiconductors by his transistor theory.

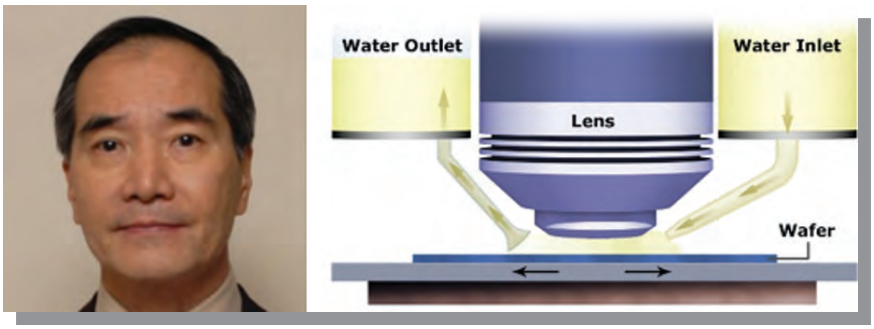
However, also at Shockley Labs there were instances where experimental success came first. Goetzberger: "In the old Labs in San Antonio Road, diffusion furnaces were set up in a former barn. We did not know about clean work conditions. The pn junctions we fabricated were generally not ideal. More or less by accident, but also by my structured follow-up on observations and reproduction of experiments, I found a technology which gave us perfect junctions every time. This is the gettering step which has been customary in semiconductor technology for several decades". Goetzbergers discovery of metal gettering is a true marvel in semiconductor process technology. He and Shockley published this in the Journal of Applied Physics in 1960. For many years highly doped p-type silicon wafers with lower doped epitaxial device layers had been used to getter metal precipitates and achieve ideal pn junctions. Adolf Goetzberger received the 1983 J.J. Ebers Award in honor of this achievement.

While Goetzbergers discovery was accidental and provided a solution to a known problem, another great invention in microelectronics—the sidewall spacer—showed up as an artifact of anisotropic dry etching. Etching in a gaseous atmosphere instead of in liquid chemicals gained attention when both more accurate transfer of lithographic pattern and high selectivity to underlying layers became crucial. In 1975, Texas Instruments demonstrated the first all-dry-etched device, a CCD shift register. However, with the anisotropic nature of the so-called reactive ion etch (RIE) a problem arised: film removal at a steep sidewall became very difficult; only a substantial overetch could remove the undesired residues. It took about five years until Bernie Pogge at IBM thought of making use of this previously undesired sidewall feature. In 1981, he filed US patent 4,256,514 in which he decribed that sidewall to be used as a lateral spacer with its dimension being controlled by the thickness of the previously deposited film. IBM Fellow Tak Ning remembers: "Once the concept was out, many companies explored using sidewall spacer to improve devices or to come up with novel device structures".

First was Ning's invention of the double-poly self-aligned bipolar transistor which he presented in a Late News paper at the 1980 IEDM. He placed a sidewall spacer inside the lithographically defined emitter window and, thus, achieved a sub-lithographic emitter leading to a much reduced intrinsic base resistance. The sidewall also provided a self-aligned isolation of the emitter



Schematic illustration of the sidewall spacer from Bernie Pogge's US Patent 4,256,514 (left) and SEM cross section of a MOS gate with an LDD spacer (middle), and Tak H. Ning, inventor of the double-poly self-aligned bipolar transistor (right). (Images from J.N. Burghartz, "Guide to State-of-the-Art Electron Devices," Wiley)



Burn Lin, inventor of immersion lithography (left), schematic of practical implementation of immersion lithography in a commercial step-and-repeat equipment (right)

polysilicon contact to the extrinsic base polysilicon. Ning's double-poly self-aligned bipolar transistor became a standard in semiconductor industry and—in its general form—is still in manufacturing, though today with an epitaxial SiGe:C rather than an implanted Si intrinsic base (see EDS Newsletter Ocober 2018). Tak Ning received the 1989 J.J. Ebers Award partly for his pioneering contribution to bipolar technology.

Next was the lightly-doped drain (LDD) structure using source/drain implants before and after formation of a sidewall-spacer around the gate contact of a MOS device. Ning: "Seiki Ogura's LDD concept was reported in 1981 at IEDM. It was quite effective in suppressing the hot-carrier effect, but only for 5 V designs. Once voltage was scaled down to 2.5 V hot-carrier effect was no longer an issue, and LDD was no longer needed. I would say that LDD was used in high-speed CMOS logic for less than 10 years by the industry".

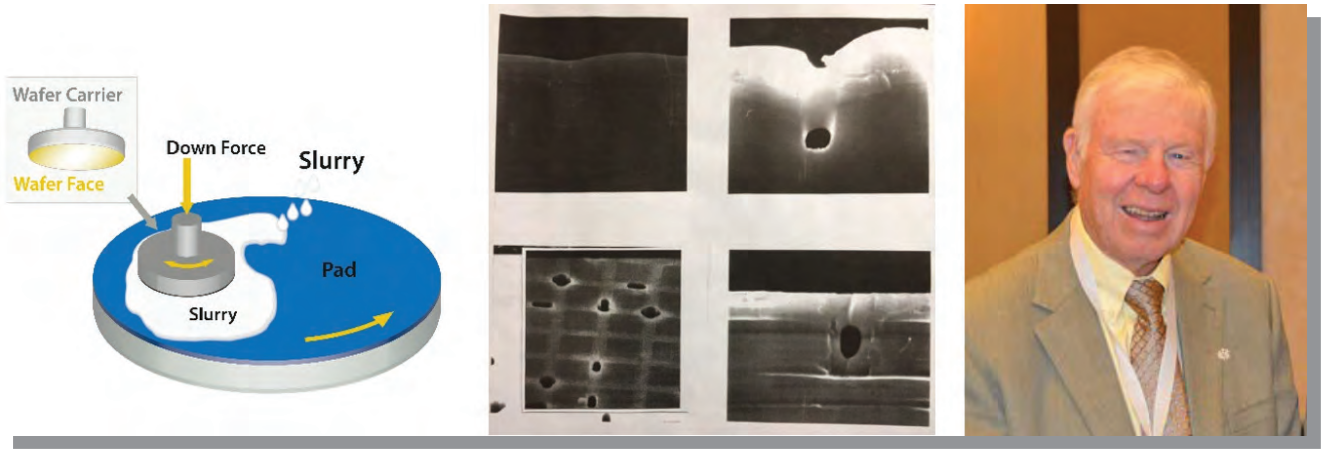
Another application with high impact was the self-aligned silicide (salicide) process introduced by a team at Texas Instruments, which provides self-aligned metallization at the source, drain and gate contacts of a MOS transistor. The late Roger A. Haken, in whose memory the IEDM named its Best Student Paper Award, was a member of that pioneering team. They published this breakthrough in the 1985 February issue of the IEEE Transactions on Electron Devices.

The sidewall spacer also affected the art of lithographic patterning in different ways. In the 1970's, that was used to form a sub-lithographic feature, e.g. a gate contact of a MOSFET. The dummy feature, at which the sidewall spacer was formed and which was removed later on, was called mandrel. Since the sidewall spacer was formed around the mandrel, it had partly to be etched off. This technique was known as sidewall image transfer (SIT). The interest in SIT disappeared with the progress made in lithography but SIT returned in recent years with use in double- and multiple-patterning.

Progress in photolithography was often based on concerted engineering actions but in a few cases innovations appeared as true marvels. Photolithography was introduced in 1958 by Lathrop and Nall from Army Research Laboratories in the US. It became an integral part of the planar process technology, invented by Jean Hoerni in 1957, and the planar integrated circuit, invented by Bob Noye, both with Fairchild at that time and two of those Traitorous Eight whose sudden leave brought Adolf Goetzberger to Shockley Labs.

Tim Brunner, a Globalfoundries Fellow, who spent his professional life in photolithography, mentiones a few milestones: "The chemically amplified photoresist process, invented in late 1980's by Grant Willson and Hiroshi Ito, was essential to high volume manufacturing for three decades. Step-and-scan exposure tools, invented by Perkin-Elmer/SVG in 1973 and then perfected by Nikon and ASML, advanced data-preparation methods, such as Optical Proximity Correction (OPC) and Sub-Resolution Assist Features (SRAF), and computational lithography methods like Source Mask Optimization (SMO) need to be mentioned". He also points to Extreme Ultra Violett (EUV) lithography as an "incredible engineering tour-de-force that will soon emerge as production-worthy". To him, however, "193 nm immersion lithography was a true marvel that came out of the left field to defeat the crappy 157 nm exposure technology".

Immersion lithography, using water instead of air between lens and wafer, was introduced in 1987 by Burn Jeng Lin, then at IBM, at the Microcircuit Engineering Conference on the future of subhalf-micrometer optical lithography. He remembers: "In that presentation, I told the audience that immersion lithography would be a way to extend optical lithography. There was no immediate follow up because there were many easier ways to extend optical lithography". Lin further: "By 2002, the wavelength has been reduced from 436 nm to 365, 248, 193 and heading to 157 nm. The numerical aperture of the imaging lens had been increased from 0.18, through many steps, to 0.93. Most resolution enhancement techniques had been implemented. That is: unwanted reflections and vibrations in the imaging system have been managed, phase shifting masks were used, off-axis illumination was implemented, and optical proximity correction was introduced. We were facing the limit of Moore's law scaling at the 65 nm logic node and could at most stretch to the 55 nm half node. Reducing the wavelength to 157 nm seemed to be the last resort to improve the resolution but that ran into tremendous difficulties". Burn Lin explains further: "My solution to the above problems was to stay away from the 157 nm wavelength. The vacuum wavelength of 193 nm light becomes 134 nm in water due to its refractive index of 1.44 at the 193 nm



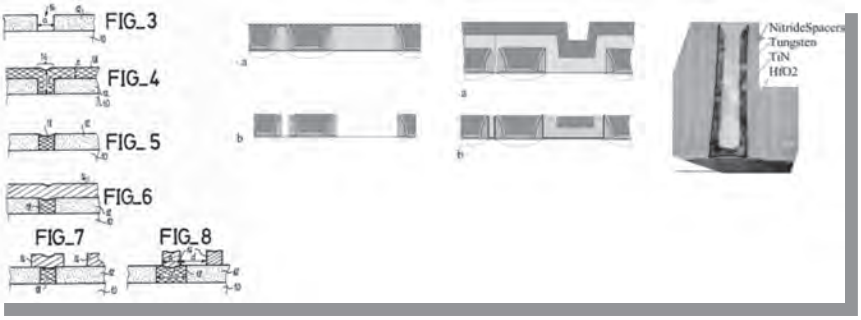
Schematic illustration of chemical-mechanical polishing (CMP) (left), images from the first device experiments (middle) and CMP inventor Klaus Beyer (right). (Photographs provided by Klaus Beyer)

vacuum wavelength. This wavelength is much shorter than 157 nm and can keep the entire optical train in 193 nm. This includes the light source, the illuminator, the mask, the pellicle, the imaging lens, and the environment. One only has to keep the space between the last element of the imaging lens and the photoresist immersed in water and the actinic wavelength will be 134 nm. This configuration is, of course, immersion lithography. At that time the entire lithography community including suppliers and users were all concentrating on making 157 nm work. One billion dollars was estimated to have been spent on this effort". Lin, who was 16 years with TSMC, as senior director and vice president, remembers: "A more difficult task followed. We had to turn the industry around from 157 nm conventional to 193 nm immersion, technically, politically, and commercially". Burn Lin received the 2013 IEEE Jun-Ichi Nishizawa Medal for his pioneering work and his leadership in immersion lithography.

Immersion lithography turned out to carry the 45 nm, 40 nm, 32 nm, 28 nm, 20 nm, 16 nm, 14 nm, 10 nm, and 7 nm nodes in a span of about 12 years. Besides immersion, also those many other 'tricks' mentioned have to employed to arrive at such small dimensions. One of those extras is double- and multiple patterning, taking advantage of patterning two or more masks to reduce the combined pitch or the SIT enabled by the sidewall spacer, the other marvel in microelectronics we mentioned. This is not the only entanglement of marvellous inventions in microelectronics.

Photolithography also has a close relationship with another marvel in microelectronic engineering, i.e. chemical-mechanical polishing (CMP). This process is applied numerous times in the course of circuit integration to return to a perfectly planar wafer surface. This allows to arrive at an optimum resolution in a trade-off against a small depth-of-focus (DOF).

CMP on device structures was invented by IBM Fellow Klaus Beyer. Beyer was assigned by his manager the task of finding a way to eliminate silicon wafer surface scratching caused primarily by the traditional brush cleaning method used to remove the colloidal silica polishing slurry. In the course of his investigations Beyer started to successfully use megasonic cleaning to remove those residues. In a personal communication Klaus Beyers said: "The first CMP application to silicon surfaces was achieved by Walsh and coworkers at Monsanto Corp. in 1962. Approximately in 1973 Monsanto engineers installed their CMP process at IBM. On March 20, 1983, at the 1983 American Chemical Society Meeting in Seattle/Washington, I showed voltage breakdown measurements of oxides grown on silicon surfaces cleaned by megasonic cleaning of colloidal silica covered silicon surfaces. I mentioned the possibility of this process for device applications". About 12 months earlier he was approached by a development manager and asked to also work on trench refill using glass reflow. His then two managers made a deal and had him work half-time on each of those tasks. At 1.5-μm trench width the glass trench refill process caused unwanted mounds after reflow at random locations. Out of desperation, on a day in January 1983 Klaus Beyer applied his meanwhile scratch-free polishing process from his other job assignment with the result that the device structures became perfectly planar. This was the birth hour of CMP on device structures. Beyer remembers the difficulties they had at IBM before CMP was applied to multi-level interconnects: "A very important problem was also the wiring of computer chips. The extension from three- to four-level wiring was very difficult. Planarization of interlevel oxides was done by applying photoresist as a planarization medium with a subsequent RIE etchback. However, this only worked for certain layout configurations." In 2002, Klaus Beyer retired from IBM



Contact/Via plug principle: detail of France/EU patent: 84.05906 (US patent #: 4,592,802) filed on April 13, 1984 by Simon Deleonibus and Guy Dubois, for Thomson Semiconductors (now ST Microelectronics) (left). First publication of totally self aligned damascene metal gate last/ HiK CMOS integration at IEDM 2002 by CEA, LETI and STMicroelectronics (3 images on right side). (Images provided by Simon Deleonibus)

after having received a major invention award fom IBM's CEO Lou Gerstner, and in 2015, he received a Lifetime Achievement Award from the International Conference on Planarization/CMP Technology (ICPT).

CMP was also instrumental in enabling Cu damascene, optimized tungsten contact/via plug formation in aluminum multi-level interconnects in the 1990's and to realize metal replacement gates in the 2000's. The plug concept goes back to work at ST Microelectronics in 1983/84 by IEEE Fellow Simon Deleonibus and Guy Dubois. Simon Deleonibus explains: "I was hired by Thomson Semiconductors in 1981, after my PhD. We tried to increase, as much as possible, the step coverage of sputtered or evaporated aluminum in high-aspect-ratio contacts to avoid high contact resistance and reliability issues. We tried several solutions to smoothen the contact opening topography and came to the conclusion that refilling the contact with a metal by a conformal deposition would solve both step coverage and reliability problems. We filed the basic generic patent on the contact/via plug principle in early 1984 (France/EU patent: 84.05906, US patent 4,592,802). Our patent covered any conformally deposited metal and any type of removal process. It also offered to reduce the metal levels contacted pitches. I joined CEA, LETI in 1986 and continued my work with my colleagues there. Finally, we published the contact/via plug for 16Mb EPROM at IEDM 1989, featuring W as refill material, TiN/Ti barrier/contact metal stack. W and TiN/Ti were smoothened and etched back by RIE at that time. CMP of W was applied much later by the mid 1990s when the cost-of-ownership was less an issue in synergy with interlevel dielectric planarization and later on Cu integration. The whole microelectronics business is using the plug principle at the sub-10 nm level and has extended it to Through Silicon Vias (TSV). The French Academy of Technologies awarded me with their 2005 Grand Prix for the invention and development of the plug principle, a major innovation for the industry".

Simon Deleonibus continues: "By 1995, I started to develop the damascene metal-gate-last integration. The plug principle was of great inspiration to apply a low thermal budget process on the metal gate material. Annealing before metal deposition was necessary to self-align sources and drains to gate, protect salicided junctions from degradation, keep the metal workfunction value stable and avoid any reaction with the underlying gate dielectric. In 1996, I and François Martin, both with CEA, LETI, filed the patent (France/EU patent 96.15436, US patent 6,346,450) showing the way to integrate the gate-last metal with total self alignment, thanks to the use of a replacement material and the planarization of the final metal by CMP. We published the first results using a W/TiN/HiK(Hf02 deposited by Atomic Layer Deposition) gate stack at IEDM 2002. Today, the damascene gate is massively used by Intel and other manufacturers!".

The gettering technique, the sidewall spacer with its impact on self-aligned bipolar technology, LDD, sacilide and lithographic multiple patterning, immersion lithography, CMP and the via/contact plug principle with extension to damascene gate are true marvels in semiconductor process technology. They all had tremendous impact on keeping Moore's Law to go on.

A Review of the 2018 IEEE International Electron Devices Meeting (IEDM)

By Kirsten Moselund and Rihito Kuroda

The 64th Annual IEDM conference (www.ieee-iedm.org), sponsored by the IEEE Electron Devices Society, was held December 1–5, 2018, at the Hilton San Francisco Union Square Hotel. Special Focus Sessions of invited papers explored some of today's most important areas of research and included topics on quantum computing, 5G wireless communications, wide-bandgap power devices, and the future of interconnects.

Some highlights of the conference in the area of Neural Networks, Artificial Intelligence and Neuromorphic Computing included a talk on "*Exploiting Hybrid Precision for Training and Inference: A 2T-1FeFET-Based Analog Synaptic Weight Cell*," by X. Sun et al. from Arizona State Univ., Univ. Notre Dame, and Georgia Institute of Technology. This team of university researchers participating in the SRC/DARPA-sponsored ASCENT program described an in-memory computing architecture in which computing is done at the location of the data storage to accelerate training. This approach also trades unnecessarily high levels of precision during inferencing for greater speed and energy efficiency. Previous such "in-memory computing" approaches have made use of various non-volatile memories (NVMs), but their overall accuracy has suffered. Here, the team proposed a novel compact analog synaptic weight cell consisting of two MOSFETs and one ferroelectric transistor (2T-1FeFET) to handle both the training and inferencing functions. They used an experimentally calibrated FeFET SPICE model to validate the device performance and embedded it in a convolutional neural network using both the MNIST and CIFAR-10 training datasets, and achieved accuracies of ~97.3% and ~87%, respectively. Another highlight is on an Electrochemical Synaptic Cell titled "*ECRAM as Scalable Synaptic Cell for High-Speed, Low-Power Neuromorphic Computing," by* J. Tang et al. from IBM. Various non-volatile memory technologies such as RRAM and PCM are being investigated for use as synaptic cells for neuromorphic computing, but they tend to have non-ideal switching characteristics (e.g., asymmetric weight update, limited endurance, and elevated levels of stochasticity, or random behavior). Instead, IBM researchers described a novel scalable electrochemical random access memory (ECRAM) device based on lithium (Li) ion intercalation in tungsten oxide (WO_3) that can be used as a scalable synaptic cell, see Figure 1. These non-volatile ECRAMs showed high levels of switching symmetry and linearity, good data retention, and up to 1,000 discrete conductance levels useful for multi-level operation in large memory arrays. The researchers demonstrated successful high-speed programming, using 5ns pulse widths with 300 x 300 nm^2 ECRAM devices. Ultra-low switching energy of 1 fJ is projected for scaled 100 x 100 nm^2 devices. MNIST image-recognition simulations based on experimental data showed 96% accuracy.

In the area of Memory Technology, a highlight was Intel's presentation on the integration of e-MRAM With 22 nm FinFETs in the talk titled "MRAM as Embedded Non-Volatile

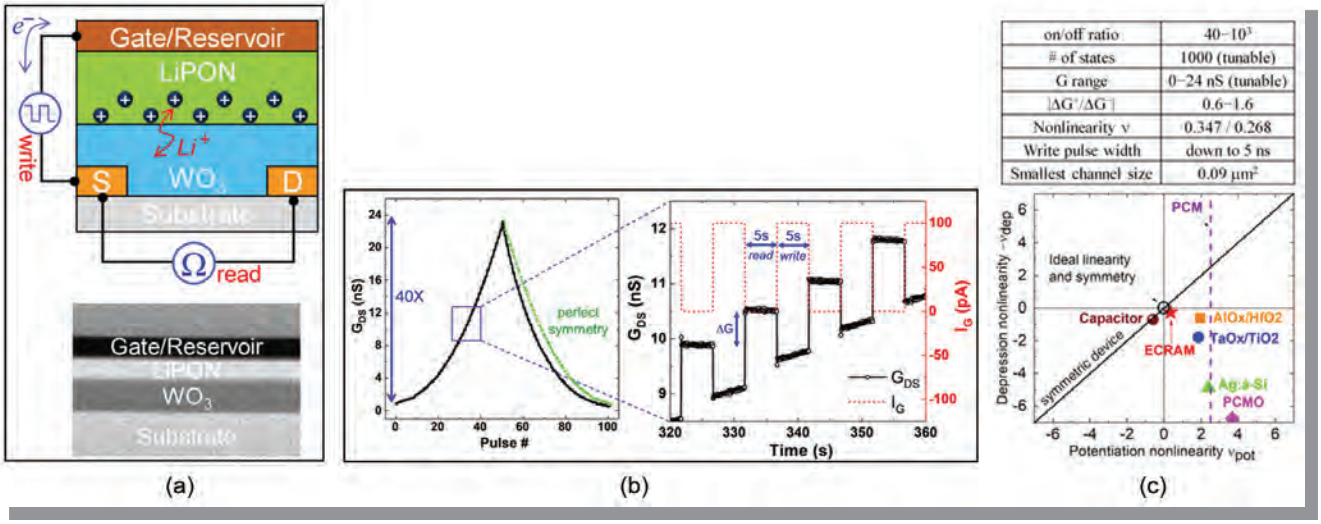


Figure 1. (a) The left image below shows a schematic of the ECRAM device (on top) and a cross-sectional electron microscope image (below it). (b) In the middle is a plot of the source-drain conductance (GDS) during gate current pulses, showing good symmetry and a large on-off ratio (~40). (c) To the right is a table summarizing key ECRAM metrics for neuromorphic computing, and a comparison with other technologies.

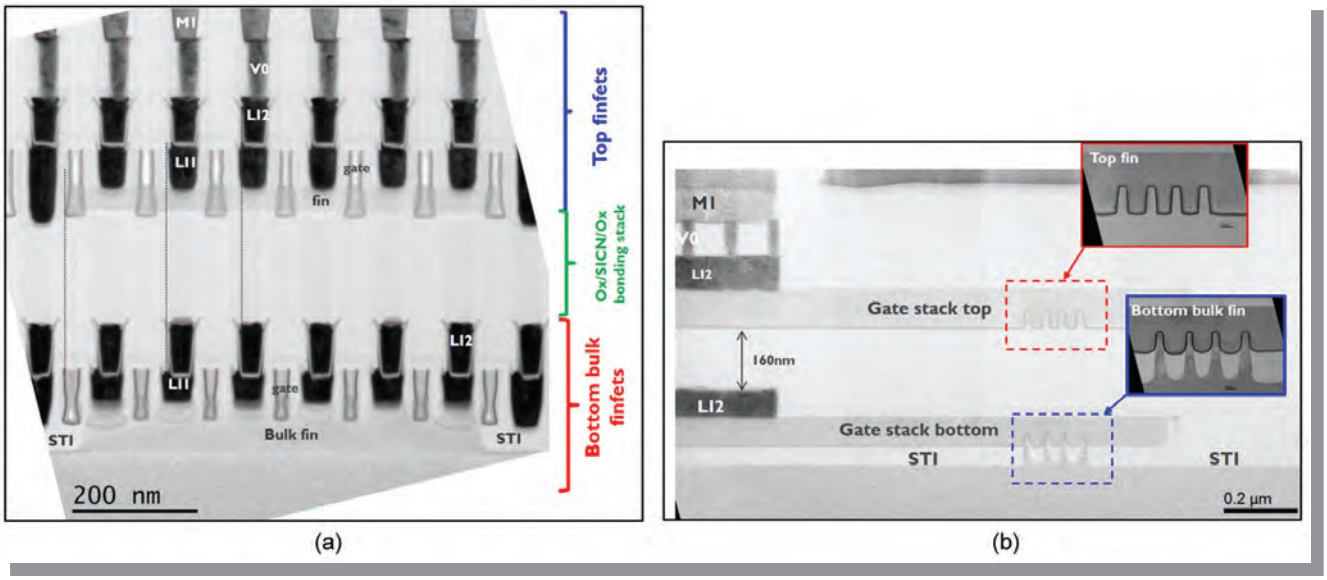


Figure 2. Highest-Density 3D Sequentially Stacked FinFETs. (a) At left above is a cross-sectional electron microscope image of the fabricated 3D stacked FinFETs along fins and across gates, showing the tight alignment achieved by the top processed layers (Gate Li1, Li2) toward the bottom layers. (b) At right is a cross-sectional image of the final devices across fins with the gates covering the fins.

Memory Solution for 22 FFL FinFET Technology," by O. Golonzka et al. from Intel. Embedded non-volatile memory (e-NVM) technologies, which retain data when power is turned off, are essential for Internet of Things (IoT), mobile and other applications, but the dominant embedded technology, e-flash, suffers from cost and scaling issues. Embedded MRAM (magnetoresistive random access memory), with its low manufacturing costs and high data retention and switching endurance, is a compelling alternative. It also has the potential to replace other types of embedded memory besides e-flash, and to serve as a building block for future logic devices as well. Integrating MRAM with mainstream CMOS technology has been problematic for various reasons, but here Intel researchers described the successful integration of embedded MRAM into the company's ultra-low-power 22 nm FinFET CMOS technology on full 300 mm wafers. The work represents a major step forward toward commercial use of the technology for high-performance, low-power applications. The magnetic tunnel junction-based memory cells are built from dual MgO magnetic tunnel junctions (MTJs) separated by a CoFeB-based layer in a 1 transistor-1 resistor (1T-1R) configuration in the interconnect stack. To demonstrate their performance, Intel built 7.2 Mb MRAM arrays which achieved industry-leading data retention (10 years with <1e-6 error rate at 200°C) and endurance (>10^6 write endurance). Another highlight was on highly integrated self-aligned 3D Crosspoint Storage-Class Memory (SCM) in the paper "High-Performance, Cost-Effective 2z nm Two-Deck Crosspoint Memory Integrated by Self-Align Scheme for 128 Gb SCM" by T. Kim et al. at SK Hynix. Storage-class memories are an evolving class of high-density solid-state devices that attempt to combine the speed and small footprints of "working" computer memory such as DRAM with the non-volatility of flash memory at a low cost per bit. Researchers from SK Hynix discussed a novel 3D crosspoint memory cell for use in SCMs that is built from phase-change materials integrated with a chalcogenide selector device. The researchers fabricated the cells using self-aligned processes and precise materials-engineering techniques to preserve the electrical characteristics of these sensitive materials, which were integrated into a high-density 2z nm two-deck architecture for the first time. The devices demonstrated a read latency of <100 ns in a 16 Mb test array, which the researchers say is suitable for use in a 128 Gb SCM.

A few highlights for the area of advances in CMOS technology include the presentation by Imec researchers on highest-density 3D sequentially stacked FinFETs in the paper titled "First Demonstration of 3D Stacked FinFETs at a 45 nm Fin Pitch and 110 nm Gate Pitch Technology on 300 mm Wafers," by A. Vandooren et al. The Imec researchers reported on 3D sequentially stacked FinFETs that have the tightest pitches ever reported in such a stacked architecture—45 nm fin pitch and 110 nm gate pitch, see Figure 2. The 3D architecture makes use of a sequential integration process yielding tight alignment between very thin top and bottom Si layers. The junctionless devices in the top layer were fabricated and transferred using low-temperature (≤525 °C) processes to avoid performance degradation, and a 170 nm dielectric was used to bond the two wafers. The top layer is so thin that the bottom layer could

be patterned right through it by means of 193 nm immersion lithography, which connects the two via local interconnect. The researchers evaluated various gate stacks, ultimately choosing TiN/TiAl/TiN/HfO_2 with a $LaSiO_x$ dipole inserted into the stack. The combination demonstrated good threshold voltage tuning, reliability and low-temperature performance. In addition, the paper "High-Performance InGaAs Gate-All-Around Nanosheet FET on Si Using Template-Assisted Selective Epitaxy" by S. Lee et al. from IBM focused on InGaAs Channels for High-Mobility N-FET Nanosheets. IBM researchers looked to III-V materials as a replacement for Si channels. They monolithically integrated high-performance InGaAs gate-all-around nanosheet N-FETs on Si using what they call a "Template-Assisted-Selective-Epitaxy" (TASE) process designed to integrate high-mobility material formed into nanoscale sheets. The nanosheets are scaled to 10 nm thicknesses and the transistors have <40 nm gate lengths, with the gate metal wrapping around the channel for optimal gate control. The devices demonstrated excellent current drive capability (I_{on} = 355 μA/μm), as well as subthreshold swing of 72 mV/decade. The researchers say device performance can be further improved by scaling gate length/nanosheet dimensions. The devices are compatible with current silicon manufacturing tooling.

In the area of photonics, one highlight is on Ge-on-Si lock-in pixels for distance ranging in the paper titled "*High-Performance Germanium-on-Silicon Lock-In Pixels for Indirect Time-of-Flight Applications*" by N. Na et al. from Artilux. Range-imaging is key to many electronics applications such as hand tracking, facial recognition, localization/mapping for navigation, object detection/ranging for autonomous driving, and many others. However, new technologies are needed to enable accurate range-imaging at wavelengths beyond the visible range, in order to ensure eye safety and for better performance. One approach is to develop better "lock-in" pixels for use in image sensor arrays. Lock-in pixels provide distance information indirectly, using the time-of-flight (TOF) principle. TOF systems determine the distance of an object by shining light on it, reflecting that light to the pixel and noting when it arrives, and calculating the distance light would have traveled in that time. Artilux, Inc. researchers reported the first Ge-on-Si lock-in pixels for indirect TOF measurements for such uses. These Ge-on-Si pixels demonstrated both high sensitivity (quantum efficiency >85% and >46% at 940 nm/1550 nm wavelengths, respectively) and high resolution (demodulation contrast >0.81 at 300 MHz), a significant improvement from their pure Si pixel counterparts. The technology may open new routes to high-performance indirect TOF sensors and imagers, as well as the potential adoption of eye-safe lasers for consumer electronics. The researchers say the lock-in pixels were developed via a foundry's image sensor platform technology and hence may be ready for mass production in the near future. In addition, the paper titled "Quadratic Electro-Optical Silicon-Organic Hybrid RF Modulator in a Photonic Integrated Circuit Technology" by P. Steglich et al. from IHP/Technical University of Applied Sciences Wildau discussed a Si-Organic electro-optical modulator for low-power photonic ICs. The team of researchers led by IHP reported on a hybrid silicon-organic electro-optical (EO) modulator for RF photonic ICs that takes advantage of the quadratic EO effect, opening a path to ultra-low-power photonic building blocks such as tunable filters, switches and RF modulators. Existing hybrid silicon-organic EO modulators have high loss and modulation bandwidth limitations along with reliability and stability issues because they are based on the linear EO effect, which requires a high voltage to initially "pole" (i.e., activate) the EO material. They also require periodic re-poling, which reduces reliability. The researchers investigated a spin-coated organic polymer that employs the quadratic EO effect instead of the linear effect. It doesn't require post-process poling, and with it the researchers reported an ultra-low per-bit energy consumption of 87 aJ/bit and modulation at just 1 V-cm, which would lead to RF modulators that operate at CMOS-compatible driver voltages.

Other noteworthy presentations included CMOS-compatible Graphene interconnects in "*CMOS-Compatible Doped-Multilayer-Graphene Interconnects for Next-Generation VLSI*" by J. Jiang et al. from Univ. California-Santa Barbara. Integrating graphene into the interconnect scheme holds the promise of increasing performance and limiting power consumption in next-generation CMOS ICs, as graphene offers high conductivity and is not prone to electromigration. One of the main challenges for practical implementations are the high temperatures typically needed to form graphene (800–1000 °C), which would damage the active devices already fabricated at the front-end-of-the-line. University of California-Santa Barbara researchers reported on a new approach in which a low-temperature (300 °C) pressure-assisted solid-phase diffusion process enables the growth and doping of multi-level CMOS-compatible graphene nanoribbons, see Figure 3. These nanoribbons demonstrated a markedly lower contact resistance (<20 Ω-μm) than a copper interconnect, yielded a ~4x increase in device performance, and showed negligible electromigration under 100 MA/cm^2 at >100 °C. These results point to a practical and industry-compatible approach toward exploiting the unique electrical properties of graphene in silicon-based CMOS ICs. Another highlight was on nanoelectromechanical

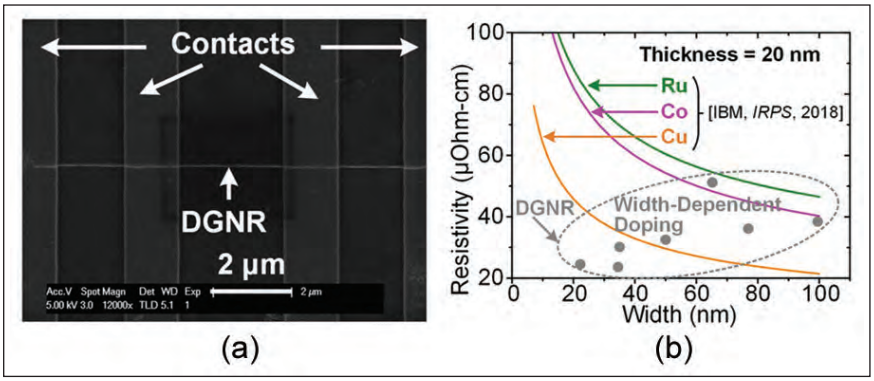


Figure 3. Above are (a) an electron microscope image of 20-nm-wide doped graphene nanoribbon (DNGR) in a four-probe test structure; and (b) the measured resistivity of the DGNR vs. wire width from 4-probe measurements. Reported resistivities of Cu, Co and Ru wires (with liners/barriers) are plotted, assuming 20-nm wire thickness.

switches for ultra-low-power computing by Z.A. Ye et al. from the Univ. of California-Berkeley in the talk "Demonstration of 50-mV Digital Integrated Circuits with Microelectromechanical Relays." ICs made from nanometer-scale mechanical relays are intriguing for some ultra-low-power digital computing applications because, in principle, they can achieve zero off-state leakage current, resulting in zero static power consumption. They also offer abrupt switching characteristics, but although in principle they can be operated with a very low gate voltage swing, in practice hysteretic switching behavior often requires the use of higher bias levels. Researchers from the University of California-Berkeley have overcome this in a novel relay design, and reported a 50-mV operation of digital ICs at room temperature for the first time. To reduce switching hysteresis losses and further enable low gate voltage operation of these relay-based ICs, a body-biasing design was employed to reduce the number of relay contacts and a self-assembled monolayer molecular coating (PFOTES) for low adhesion was used. Finally, the presentation titled "Highly Performant Integrated pH Sensor Using the Gate-Protection Diode in the BEOL of Industrial FDSOI" by G.T. Ayele et al. from STMicroelectronics/Universite de Lyon/Universite de Sherbrooke looked at a pH sensor in the BEOL. The STMicroelectronics-led team reported a novel and highly sensitive pH sensor fabricated in the BEOL using a mainstream fully depleted FDSOI CMOS process. The pH sensing exploits the drain-induced barrier lowering (DIBL) effect with respect to a floating gate, via a gate protection diode in the interconnect stack. The current in the diode, which varies according to the pH in the fluid under study, turns the transistor on or off. The device demonstrated a sensitivity of 1.25 decade/pH and the researchers say 6.6 decade/pH is achievable, or more than 7x better than existing state-of-the-art solid-state pH sensors.

In addition to the many exciting technical talks, there were also 90-minute tutorials bridging the gap between textbook-level knowledge and leading-edge current research on "Reliability Challenges in Advanced Technologies" by Ryan Lu at TSMC, "STT-MRAM Design and Device Requirements" by Shinichiro Shiratake at Toshiba Memory, "Quantum Computing Primer" by Mark B. Ritter at IBM, "Power Transistors in Integrated BCD Technologies" by Hal Edwards at Texas Instruments, "Design-Technology Co-optimization at RF and mmWave" by Bertand Parvais at Imec, and "Emerging Device Technologies for Neuromorphic Computing" by Damien Querlioz at CNRS. In addition, there were full-day short courses on "It's All About Memory, Not Logic!" organized by Nirmal Ramaswamy at Micron and "Scaling Survival Guide in the More-than-Moore Era" organized by Jin Cai at TSMC. Monday's Plenary Presentations were on "Future Computing Hardware for AI" by Dr. Jeffery Welser, Vice President, IBM Research-Almaden, "4th Industrial Revolution and Foundry: Challenges and Opportunities" by Dr. Eun Seung Jung, President of Foundry Business, Samsung Electronics, and "Venturing Electronics into Unknown Grounds" by Prof. Gerhard P. Fettweis, TU Dresden. Tuesday's career-focused luncheon event featured industry and scientific leaders talking about their personal experiences in the context of career growth. It was moderated by Curtis Tsai of Intel, and the speakers were Veena Misra, Distinguished Professor and Director of the ASSIST Center at NC State University, and John Chen, Vice President of Technology and Foundry Management at Nvidia. The Tuesday evening panel session was on "The Next 25 years in Electronics." The panelists focused on how the semiconductor technology will evolve and what new life-changing technologies it will enable in 25 years from today (circa 2045). The group included industry leaders, long-tenured professors, and government participants from the early days of DARPA for this 25-year look-back and 25-year look forward. Finally, there was a vendor exhibition, a poster session on MRAM technology organized by the IEEE Magnetics Society, and a student research showcase hosted by the Semiconductor Research Corporation.

Edited by Carmen M. Lilley

Upcoming Technical Meetings

2019 IEEE Electron Devices Technology And Manufacturing Conference (EDTM)

SINGAPORE TOURISM PROMOTION BOARD

It is our great pleasure to invite you to the 2019 IEEE Electron DevicesTechnology and Manufacturing (EDTM) conference. It will be held March 12–15, 2019, at the iconic Marina Bay Sands Convention Centre in Singapore.

Launched in 2017 and sponsored by the IEEE Electron Devices Society (EDS), EDTM is rapidly becoming a premier conference for the electron devices community. EDTM provides a unique forum for discussion of a broad range of device-related topics including materials, processes, devices, packaging, modeling, reliability, manufacturing, and yield. The conference location rotates among countries in Asia, coming to Singapore for the first time in 2019.

EDTM 19 conference will kick off on the first day with 4 tutorial sessions and 4 short courses. The 4 tutorial sessions cover topics ranging from front-end CMOS process to back-end-of-line, packaging and non-volatile memory technology. These tutorials sessions are catered towards students and young engineers in the industry and are intended to give a comprehensive overview of the domain presenting a roadmap of the evolution of the technology over the past two decades. For the 4 short courses lined up for you, they cover the latest advancements in niche application areas of interest, which include hardware security, sensors for IoT, flexible and wearable electronics as well as heterogeneous integration of different device technologies. The short courses are aimed at educating our attendees with the latest ongoing applied research in these four areas that will pave way for the successful realization of internet of everything (IoE), Industry 4.0 and an AI-driven economy.

We are also pleased to announce that the Technical Program Committee has prepared an outstanding technical program. There will be 3 Plenary Talks by distinguished speakers from the industry and academia covering exciting topics in "Differentiated Foundry Solutions for a Connected Future", "Technologies Toward Three-Dimensional Brain-Mimicking IC Architecture" and "Enabling manufacturing of sub-10 nm generations of integrated circuits with EUV lithography." The 3 days technical program will include a total of 112 regular and invited oral presentations organized into several parallel sessions and 60 poster presentation sessions. On top of all these, as a tradition of EDTM, the conference will also include a Women In Engineering (WIE) event to celebrate the contributions of women in the field of electron devices and manufacturing.

http://ewh.ieee.org/conf/edtm/2019/index.html

On behalf of the organizing and international committees, we look forward to seeing you at the 2019 EDTM in Singapore, where the excitements and hospitalities await you!

Geok Ing Ng
General Co-chair of EDTM 2019
Nanyang Technological University

MK Radhakrishnan
General Co-Chair of EDTM 2019
NanoRel Technical Consultants

2019 IEEE International Memory Workshop (IMW)

The 11th International Memory Workshop (IMW) will be held at the Hyatt Hotel in Monterey, California, USA, from May 12–15, 2019. The history of the IMW dates back to the NVSMW (Nonvolatile Semiconductor Memory Workshop) which began in 1976 and which later merged with the ICMTD (International Conference on Memory Technology and Design) to become the IMW. The IMW is sponsored by the IEEE Electron Devices Society and meets annually in May. The workshop covers all types of memory technology, is focused on advancing innovation in memory technology, and is organized in a way that provides excellent professional development and networking opportunities for attendees.

The IMW is the premier international forum for both new and seasoned technologists having diverse technical backgrounds to share and learn about the latest developments in memory technology with the global community. The scope of workshop content ranges from new memory concepts in early research to the technology drivers currently in volume production as well as emerging technologies in development. Topics include new device concepts, technology advancements, scaling and integration, circuit design and reliability, as well as emerging applications. Consistent with the increased importance of memory system architecture and integration, the workshop also includes increasing coverage of the systems in which memories are deployed and the co-evolution of memory technology along with memory systems and applications.

The IMW is the preeminent forum covering the latest developments, innovations, and evolving trends in the memory industry. Typical workshop attendance exceeds 250 attendees (350 last year) and the technical program begins with a full day short course given by distinguished experts that provides an excellent professional development opportunity for both new and experienced technologists. The single-track technical program spans three days and also includes an evening poster session for informal technical discussion with authors as well as a panel discussion where experts discuss and debate a current hot topic. The 2018 workshop included invited talks from industry and research leaders from Toshiba, Micron, NXP, FMC, LETI, SONY, Applied Materials, Avalanche and Panasonic. Highlights included experts sharing their insights and perspectives on a variety of topics including the 3D NAND scaling horizon, scaling challenges of embedded memories, opportunities for emerging memories and innovation (PCM, RRAM, MRAM, FeRAM…) for storage class memories, data centric architectures, tremendous growth of connected objects, and neuromorphic circuits. The technical program is organized to maximize networking opportunities and facilitate open information exchange among workshop contributors, committee members, and attendees. The program schedule includes ample time dedicated to social events including provided refreshment breaks, a workshop luncheon, and an evening banquet.

On behalf of the organizing committee, I cordially invite you to participate in the 2019 IMW to continue to participate in the advancement of innovation in the rapidly evolving memory industry. For additional information, including the call for papers, key dates, abstract submission instructions, registration information, and technical program details, please visit the IMW website for the latest updates: http://www.ewh.ieee.org/soc/eds/imw/. I look forward to seeing you in Monterey this May.

Gabriel Molas
CEA Leti
2019 IMW Publicity Chair

Society News

Message from EDS President

Dear EDS Colleagues:

Fernando Guarin
EDS President
(2018–2019)

As we are ending 2018, I would like to take this opportunity to thank our many volunteers that are the lifeblood that energizes our society. It was my distinct honor and privilege to have served as the Electrons Devices Society as your 2018 President. I would like to share with you the many accomplishments and challenges;

We have completed the definition stage of our future strategy, with a very clear objective "To collaborate, network, and be the center of excellence in electron device technology." I would like to express our sincere gratitude to the Past President Samar Saha and the members of his strategy committee, for their leadership in the definition and outline of our future strategy. Now we move to the next phase to set up the infrastructure to implement and monitor our progress on this important endeavor.

In the publications arena, under the leadership of outgoing chair Hisayo Momose, the submission to publication time of EDS journals maintained a best in class record pace, TED submission stands at 13.1 Weeks, EDL is still the fastest in IEEE with 4 weeks. JEDS continues to solidify our leadership position in Open Access. I would like to thank our outgoing EDL EiC Tsu-Jae King Liu and welcome Jesus del Alamo to this key role.

Our conference portfolio remains very strong and we continue to look for new opportunities. The EDTM2018 with 100% EDS ownership was a success and is emerging as an EDS flagship conference in Asia; EDTM2019 is on track in Singapore.

We continue to maintain very close collaborations with EDS conferences: PVSC, IEDM, EDTM, IRPS, ISPSD, IVEC, VLSI, IFETC, etc., and continue to sponsor Special Issues based on best conference papers and highly relevant topics for TED and JEDS.

Our membership continues to be close to 10K as of November we showed a decreased of 2.7% while our student membership was up by 1.2%. For 2018 *EDS Celebrated Member* honoree Martin Green was announced at the June World Conference on Photovoltaic Energy Conversion (WCPEC-7). The June BoG meeting was held in Cartagena de Indias, Colombia, where the EDS C&B changes were approved and subsequently accepted by IEEE. They have now been updated on our website. The EDS education activities best practices presentation at TAB led to formation of a TAB ad hoc committee to use across IEEE.

The first draft of new social media platform (Facebook, LinkedIn, Twitter and IEEE Collabratec) was successfully rolled out at the YP/WIE breakfast networking event prior to the IEDM 2018 plenary session. I invite you to join us and participate at:

Facebook https://www.facebook.com/IEEE-Electron-Devices-Society-1581398582006248

LinkedIn https://www.linkedin.com/company/edsglobal

Twitter https://twitter.com/IEEEEDS

Our EDS web site is currently undergoing redesign for Desktop version: https://invis.io/FJO2G98EBC6 and Mobile version: https://invis.io/PJOSFIG6CVA

I would like to extend our sincere gratitude for the efforts of many dedicated volunteers that have positioned EDS on solid ground in the technical and financial areas. As a volunteer-led, volunteer-driven organization, we rely on the dedication of individuals like you who share their time, talent, and energy to help make EDS the premier global society devoted to advancing the field of electron devices for the benefit of humanity. I invite you to become an engaged member of our Society, and play a vital role as we shape the future of our society.

Fernando Guarin
EDS President

Report on the EDS Board of Governors Meeting in San Francisco, USA

Jacobus W. Swart
EDS Secretary

The EDS BoG Meeting was held in San Francisco, USA, on December 2nd, before the IEDM 2018 conference, and following the EDS ExCom and technical committees meetings the day before. There were enough members present to form the needed quorum defined by the Constitution and Bylaws. The picture shows the meeting room during EDS President, Fernando Guarin's overview talk at the beginning of the meeting. After the welcome words by the president, many reports were presented and motions discussed and approved.

EDS President Fernando Guarin began his speech with the moto "… building EDS on the foundation of the past to meet the challenges of the future." He highlighted the following achievements:

- T-ED continues an IEEE-best journal, with submission-online and a 13 weeks cycle time. The submission-to-publish journals maintained a record of 4 weeks for EDL. Two new editors were selected for T-ED and EDL, respectively Giovanni Ghione and Jesus del Alamo. The impact factors off the three 100% EDS journals (T-ED, EDL and J-EDS) are all close to 3.0.
- The conference EDTM held in Tokyo is a huge success as an EDS flagship conference in Asia. EDTM 2019 is on track to be held in Singapore. A new EDS conference, called LAEDC, will start in 2019 in Region 9. The first edition will be held in Colombia in February, in conjunction to the conference LASCAS sponsored by CAS.
- The changes voted on during the previous BoG meeting were all approved by IEEE and are already updated on the EDS webpage.
- The first versions of a new social media platforms (Facebook, LinkedIn, Twitter and IEEE Collabratec) were created and launched at the IEDM 2018 opening as an initiative by the EDS Young Professionals and WIE committees:
  - Facebook: https://www.facebook.com/IEEE-Electron-Devices-Society-1581398582006248/;
  - LinkedIn: https://www.linkedin.com/company/edsglobal/;
  - Twitter: https://twitter.com/IEEEEDS
  - The EDS website is currently undergoing a redesign:
  - Desktop: https://invis.io/FJO2G98EBC6
  - Mobile: https://invis.io/PJOSFIG6CVA
- EDS financials remain healthy, with a small loss in 2017 and positive numbers for 2018, with revenues and expenses of approximately 6.7 million dollars.
- The EDS Mission Fund has been established to support EDS mission-driven humanitarian, educational, and research initiatives. The current mission fund has a budget of US$129,000 and can support new proposals.
- The total number of EDS members remains over 10,000 with a slight decrease of higher grade and increase of student members in 2018. A campaign to increase memberships will continue an important effort.
- The number of EDS chapters continues to increase slightly every year, with a total of 211 chapters worldwide in 2018.
- Educational activities included a series of 6 webinars during 2018, among other initiatives, like EDS-ETC program, online international college student competition and others.
- The Strategy Plan for the next five years has been outlined, and its implementation will start in 2019. An Ad Hoc committee is being formed to track progress and to make adjustments when applicable.

After the presentation by the president, many other VP's and chairs presented their updates, new ideas and additional details to the broader overview described.

EDS President-Elect, Meyya Meyyappan, proposed the idea of offering an EDS Summer School. This could be one per year, with preference on a topic not regularly taught at EE courses. A motion was approved about the idea of offering a summer school starting in 2020. The budget will be discussed in future BoG meeting.

M.K. Radhakrishnan, EDS VP of Regions & Chapters, reported that out of the 211 chapters, 69 of the chapters are student chapters, 3 of which started in 2018. The total of subsidies amounted US$47,500.00 in 2018. A total of 14 Mini-Colloquia (MQ) were supported by EDS with a total amount of US$51,030.00. The number of Distinguished Lectures delivered (not including MQ) was 132, with total support of US$61,500.00. A motion was approved about updated EDS Regions & Chapters charter.

Bin Zhao reported in name of Ru Huang, EDS VP of Membership and Services, about membership development and recruiting campaigns. Besides the statistics presented, IEEE OU Analytics, a new visual business intelligence tool was announced, already available in vTools, for designated volunteer officers to access membership data: https://tblanalytics.ieee.org.

Ravi Todi, VP of Technical Committees and Meetings, reported about the over 100 conferences sponsored/

EDS Board of Governors meeting during the general overview speech by EDS President Fernando Guarin

co-sponsored by EDS and about the different technical committees. Some of the highlights were about the close collaborations between EDS conferences, the special issues produced for TED and JEDS, the active committees and volunteer participation with a balanced committee membership. The most prominent conferences were also described and discussed.

The treasurer report was presented by VP Subu Iyer. Healthy budgeted details were presented and discussed. Through a motion the budget for 2019 was approved, with a total expenses of US$6,695,000.00.

Hisayo Momose, Interim VP of Publications & Products reported on EDL, TED, JEDS and other co-sponsored publications. Noticeable are the acceptance rates of the EDS publications: 19.8, 28,2 and 44.0% for EDL, TED and JEDS respectively. Also the time between submission and publication are very good, respectively 4.0, 13.1 and 10.6 weeks. Discussion started on the proposal of a new publication, the Flexible Electronics Journal.

The last item on the agenda was the election of new BoG members. Among the 22 BoG members, 7 ended their 3-year term. Among these, 2 were reelected (one reelection term is allowed in one's lifetime) and 5 new names were elected.

Jacobus W. Swart
EDS Secretary
State University of Campinas
Brazil

Are You Trying to Grow Your Chapter Membership?

Applications Now Accepted for the 2019 EDS Membership Fee Subsidy Program!

Our society continually works to increase the value of EDS membership and our colleagues enjoy an incredible array of members-only benefits. One EDS initiative to encourage newcomers and assist EDS chapters stay strong and vibrant, is the **EDS Membership Fee Subsidy Program (MFSP)**. This program offers the generous incentive of one-year complimentary IEEE and EDS memberships (sponsored by EDS), to help launch new chapters or enable existing ones, in low-income geographical areas to grow their memberships.

This special offer is available to students currently enrolled in an accredited course of study, and to those professionals who qualify for reduced IEEE membership fees (i.e., unemployed, retired, or meet a minimum income threshold).

The EDS Membership Fee Subsidy Program policy is as follows:

- EDS will cover the cost of IEEE and EDS membership for up to 15 applicants per chapter. Please note that this is a one-time benefit, per applicant. Past recipients of the EDS membership fee subsidy benefit do not qualify
- **Five** of the fifteen members each year must be new IEEE members
- Applicants must apply through a local EDS chapter
- Current elected officials on record, of eligible EDS chapters will be emailed instructions
- Each applicant must indicate in their IEEE account prior to applying for EDS Membership Fee Subsidies that they qualify for reduced IEEE membership fees.

EDS has chapters around the world that organize events to benefit your professional development

- For a complete list of special circumstances eligible for reduced IEEE membership fees: https://www.ieee.org/membership/special-circumstances.html.

If you wish to apply for IEEE membership and not eligible for the EDS Membership Fee Subsidy, we encourage you to try the IEEE Electronic Membership option, which is open to new and renewing members who reside in countries where the per capita Gross National Income (GNI) is US$15,000 or less. Please visit the IEEE website for more details on IEEE Electronic Membership, at https://www.ieee.org/membership/join/emember-countries.html

Chapter Chairs: To submit your chapter's list of applicants for the 2019 EDS Membership Fee Subsidy, please contact Joyce Lombardini (j.lombardini@ieee.org), in the EDS Executive Office.

There are other EDS membership recruitment campaigns scheduled for 2019 and Joyce can provide information upon request.

EDS Members Recently Elected to IEEE Senior Member Grade

Rosminazuin Ab Rahim
Laurie Calvet
Yuri Chaplygin
Wanzhao Cui
Gerard Cummins
Peng Fang
Brad Hoff
Balaji Jayaraman
Sourabh Khandelwal
Daisuke Kobayashi
Rosa Letizia
Sylvain Marsillac
Nelidya Md. Yusoff
Abdul Rahman Mohmad
Arash Salemi
Juan Sanchez
Ioannis Savidis
Mustafa Yelten
Shinji Yuasa
Vimala Palanichamy
Ashraful Bhuiyan
Lining Zhang
Azrul Hamzah
Maizatul Zolkapli
Mohamad Radzi Ahmad
Yoshitaka Kurosaka
Wen-Sheng Zhao
Chuanxin Lian
Michael Kane
Joseph Bardin
Euisik Yoon
K. Michael Han
Cormac O'Connell
Jonas Jonsson
Lionel Trojman

If you have been in professional practice for 10 years, you may be eligible for Senior Membership, the highest grade of membership for which an individual can apply. New senior members receive a wood and bronze plaque and a credit certificate for up to US$25 for a new IEEE society membership. Upon request, a letter can be sent to employers recognizing this new status. For more information on senior member status, visit: http://www.ieee.org/membership_services/membership/senior/index.html

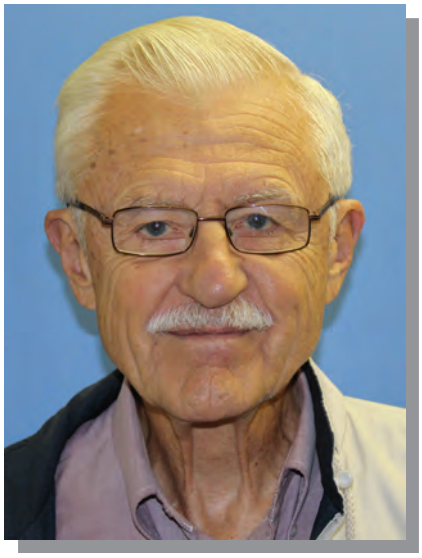
To apply for senior member status, fill out the online application after signing in with your IEEE account: https://www.ieee.org/membership_services/membership/senior/application/index.html.

In Memory—Dennis D. Buss (1942–2018)

Dennis Buss, a pioneer of HgCdTe monolithic infrared focal plane technology and corporate technology leader, passed away while on a bird-watching vacation with his wife, Alenya Buss, in rural Ecuador.

Dennis Buss received his BS, MS and PhD in Electrical Engineering from MIT in 1963, 1965 and 1968, respectively. In 1969, he began a distinguished industrial career joining the Central Research Laboratories of Texas Instruments. His early research dealt with narrow-gap semiconductors, PbTe and HgCdTe, and the development of charge-coupled devices for analog signal processing, digital memory and IR imaging. In 1978, he became a TI Fellow and in 1980 he was named Vice President and Director of TI's Semiconductor Process and Design Center. Between 1987 and 1997, Dennis was VP of Technology at Analog Devices. He returned to TI in 1997 as VP of Si Technology Development and in 2007, he became TI Chief Scientist. In 2010, Dennis retired from TI but remained as consultant to TI. He served twice on the Electrical Engineering faculty at MIT in 1968-1969 and 1974-1975.

Along the way, Dennis received numerous technical awards. He was elected IEEE Fellow in 1985 "for leadership in VLSI technology research and development." He received the 1985 IEEE Herschel Award and in 1997, together with Richard Chapman and Michael Kinch, the IEEE Jack A. Morton Award "for the demonstration and development of mercury cadmium telluride monolithically-integrated



charge-coupled device focal plane arrays." In 2000, he was selected by the IEEE Electron Devices Society for the IEEE Third Millennium Medal.

Dennis' extraordinary technical accomplishments have also been recognized through his numerous keynote, plenary and invited talks at major international conferences, such as the 2000 IEEE Emerging Technologies Symposium, 2001 IEEE International Conference on Electronics, Circuits and Systems, 2002 IEEE International Solid-State Circuits Conference, 2005 International Symposium on Low Power Electronics and Design, 2007 IEEE International Symposium on Circuits and Systems, and 2011 IEEE International Electron Devices Meeting, to name just a few. He published numerous invited papers and was Guest Editor of special issues in IEEE publications. His witty and effusive personality and his deep knowledge and experience made him a frequent leader for panel discussions at major conferences, such as ISSCC 1975 and IEDM 1979.

Starting in 2007, Dennis became Visiting Scientist at MIT's Microsystems Technology Laboratories with responsibility for managing joint research programs between TI and MIT. In this capacity, he assembled a rich research portfolio in areas as diverse as secure ID tags, magnetic field sensors, speech recognition, machine learning, gallium nitride transistor reliability, and power management systems. He served as co-advisor in several master's and PhD theses. He instituted the TI Fellowship for Women in Microelectronics in the Department of Electrical Engineering and Computer Science.

Dennis had a passion for history, nature, and mountaineering, as well as an enduring sense of adventure. He was most proud of his climb of McKinley (6,190 m) in 1986 and Aconcagua (6,961 m) in 2000.

Those of us that have had the good fortune of knowing Dennis for some time had come to appreciate his ebullient personality, his deep technological insights, and his vast perspective about microelectronics and electrical engineering education. Most of all, throughout the years, Dennis was an approachable colleague generous in sharing his wisdom through kind and constructive advice.

Jesús A. del Alamo
Massachusetts Institute of Technology

EDS Members Named Recipients of 2019 IEEE Technical Field Awards

Two EDS Members were among the recipients of the 2019 IEEE Technical Field Awards:

2019 IEEE Cledo Brunetti Award

Daniel C. Edelstein of IBM, Yorktown Heights, NewYork, has been named co-recipient of the 2019 IEEE Cledo Brunetti Award. The citation states, "For contributions to manufacturable, reliable, and scalable Cu interconnect and low-k dielectric technology for CMOS".

The combined efforts of Daniel C. Edelstein, Alfred Grill, and C-K Hu in making the benefits of copper (Cu) interconnect technologies a feasible reality forever changed semiconductor manufacturing and allowed the continued scaling of microelectronics. Their pioneering work overcame the manufacturing and reliability challenges of introducing a new material process to replace aluminum interconnect. Edelstein described a qualified and commercial Cu interconnect technology. His dual damascene structure yielded unique microstructures in electroplated Cu nanowires, making it possible to study effects of nanoscale surfaces and interfaces on electron resistivity and mass transport in Cu lines. Grill's development of silicon-carbon-oxygen-hydrogen (SiCOH) dielectrics provided a unique class of low-k dielectrics with strong chemical bonds, offering a distinct molecular structure that strengthened the thermomechanical properties of porous low-k materials. Hu's work on electromigration of Cu interconnects provided insights to understanding the basic scaling law for predicting the degradation of electromigration lifetime and development of new materials for future technology nodes.

An IEEE Senior Member, Edelstein is an IBM Fellow at the IBM T.J. Watson Research Center, Yorktown Heights, NY, USA. Grill is an IBM Fellow Emeritus at the IBM T.J. Watson Research Center, Yorktown Heights, NY, USA. Hu is a research staff member at the IBM T.J. Watson Research Center, Yorktown Heights, NY, USA.

2019 IEEE Andrew S. Grove Award

Digh Hisamoto of Central Research Laboratory, Hitachi, Ltd., Tokyo, Japan, has been named the recipient of the 2019 IEEE Andrew S. Grove Award. The citation states, "For pioneering work in the manufacturing of three-dimensional double-gate MOSFET devices."

Without Digh Hisamoto's development of the three-dimensional (3D) double-gate metal-oxide-silicon field effect transistor (MOSFET) in 1989, many of today's advanced logic products likely would not exist. With conventional planar MOSFET scaling becoming more difficult due to challenges including short-channel effects, Hisamoto's DELTA 3D MOSFET was instrumental in allowing miniaturization to continue. He was the first to recognize that it was possible to solve process issues if the channel was formed in vertical "fin" surfaces. His 3D MOSFET featured strong immunity to short-channel effects, high mobility, and reduced threshold voltage variation. Important to its realization, he demonstrated that his double-gate structure could be fabricated using a conventional self-aligned silicon process. Today's FinFET advanced logic technologies exhibit most of the principal operating concepts introduced by Hisamoto's thin-body vertical-channel FET work.

An IEEE Fellow, Hisamoto is senior chief researcher, Hitachi, Ltd., Tokyo, Japan.

Samar Saha
EDS Awards Chair
Prospicient Devices
Milpitas, CA, USA

Announcement of the 2018 EDS PhD Student Fellowship Winners

Carmen M. Lilley
EDS Student Fellowship Committee Chair

The Electron Devices Society PhD Student Fellowship Program was designed to promote, recognize, and support PhD level study and research within the Electron Devices Society's field of interest.

EDS proudly announces three EDS PhD Student Fellowship winners for 2018: **Chen Jiang**—University of Cambridge, England; **Junkai Jiang**, University of California, USA; **Yuanyuan Shi**, Rovira I Virgili University, Spain. Brief biographies of the recipients appear below. Detailed articles about each PhD Student Fellowship winner and their work will appear in forthcoming issues of the EDS Newsletter.

Chen Jiang received the B.S. degree in engineering from Shanghai Jiao Tong University, China, in 2014. Since then, he has been pursuing his Ph.D. degree in engineering at the University of Cambridge, UK, and has worked on exploring novel electronic devices for low-power, low-cost electronics, encompassing device fabrication, and device physics and modeling. His research interests include novel electronic device architectures, printable large-area electronics, and low-power high-gain amplifiers for wearable sensor interface circuits and systems. He was a recipient of the Cambridge International Scholarship Scheme and the China Scholarship Council Scholarship, and was also the winner of the Cambridge Society for the Application of Research Award 2018.

Junkai Jiang joined UCSB as a MS/PhD student under the supervision of Prof. Kaustav Banerjee, upon completing his BS degree in microelectronics from Peking University, Beijing, China. Mr. Jiang's research is focused on modeling, design and characterization of interconnect materials/structures and monolithic-3D integration based on graphene and beyond-graphene two-dimensional materials. His doctoral work spanned fundamental materials modeling, compact modeling, device/circuit design and finally experimental demonstration of applications uniquely enabled by these materials. His research contributions have appeared in leading IEEE conferences and journals, including IEDM, IRPS, S3S and IEEE T-ED, as well as in Nature Electronics and Nano Letters.

Yuanyuan Shi is currently pursuing her PhD degree in Nanoscience at Rovira i Virgili University, under the supervision of Prof. Mario Lanza. She worked 12 months at Stanford University (H.-S. Philip Wong's group) on 2D materials based electronic synapses for neuromorphic applications, and her results were published in Nature Electronics and IEDM 2017. Yuanyuan has published 38 articles, one book chapter, and two international patents (one of them received 1 M$ investment). She has attended 12 international conferences, and in 6 of them gave an oral presentation. She is a student member of IEEE, EDS, and RSC, and she serves as an active reviewer for several international journals, such as Scientific Reports, Thin Solid Films and ChemElectroChem.

Carmen M. Lilley
EDS Student Fellowship
Committee Chair
University of Illinois at Chicago
Department of Mechanical Engineering
Chicago, IL, USA

Call for Nominations—EDS Newsletter Regional Editor

The society currently has opportunities available to join the EDS Newsletter editorial board. This position requires only a few volunteer hours on a quarterly basis, but plays a vital society communication role.

We would appreciate if this volunteer opportunity was promoted at your next chapter meeting. Please send nominations or self-nominations to j.lombardini@ieee.org.

Announcement of the 2018 EDS Masters Student Fellowship Winners

Carmen M. Lilley
EDS Student Fellowship Committee Chair

The Electron Devices Society Masters Student Fellowship Program was designed to promote, recognize, and support Masters level study and research within the Electron Devices Society's field of interest.

EDS proudly announces the winners of the 2018 EDS Masters Student Fellowship.

Neel Chatterjee is currently pursuing a Master's in Electrical Engineering at University of Minnesota working with Professor P. Paul Ruden and Professor Sarah Swisher on numerical modelling and simulation of charge transport in inorganic thin film transistors. He has also worked on fabricating self-assembly structures for biomedical applications under the guidance of Professor Jeong-Hyun Cho. Neel did his undergraduate in Electronics and Communication engineering from Amity University where he worked on design and simulation of nanowire field effect transistors with Professor Sujata Pandey and published papers in IEEE conferences like IEEE TENCON and INDICON. His current research interests also include solution processed dielectrics and DFT calculations of 2D materials heterostructures.

Yu-Chieh Chien received his B.S. degree in materials and optoelectronic science at National Sun Yat-Sen University, Taiwan, in 2018, where he is currently pursuing the M.S. degree, supervised by Prof. Ting-Chang Chang and Prof. Tsung-Ming Tsai. His research interests include oxide TFTs, flexible electronics, and GaN HEMT. His current research focuses on optimizing the reliability and developing the potential application in oxide TFTs. Yu-Chieh Chien has proposed degradation mechanisms for oxide TFTs under moist environment to improve stability of the devices. In addition, he has demonstrated an ultra-high sensitivity UV sensor based on oxide TFTs. To date, he has authored 4 articles to peer-review journals and 2 to international conferences.

Carmen M. Lilley
EDS Student Fellowship
Committee Chair
University of Illinois at Chicago
Department of Mechanical Engineering
Chicago, IL, USA

Call For Nominations— IEEE Fellow Class of 2020

IEEE Fellow is a distinction reserved for select IEEE members. The honor is conferred by the Board of Directors upon a person with an extraordinary record of accomplishments in any of the IEEE fields of interest.

If you know of an IEEE colleague who is a Senior Member or Life Senior Member in good standing, has completed five full years of service in any grade of IEEE Membership and who has made an outstanding contribution to the electronic or electrical engineering profession in any of the IEEE fields of interest, you can nominate this person in one of four categories: Application Engineer/Practitioner, Educator, Research Engineer/Scientist or Technical Leader.

Nominations for the Fellow Class of 2020 are now being accepted.

To learn more about the Fellow program and the application process, visit the Fellow Web Site at http://www.ieee.org/fellows where you can also find three important Fellow Guides that can help you write an effective nomination. There are some novelties in the nomination process and a summary of them can be found in The Institute article "It's Now Easier to Nominate a Potential Fellow"

The deadline for nominations is March 1, 2019.

2019 PhD Student Fellowship

Description: One year fellowships will be awarded to promote, recognize, and support PhD level study and research within the Electron Devices Society's field of interest. The field of interest for EDS is all aspects of engineering, physics, theory, experiment and simulation of electron and ion devices involving insulators, metals, organic materials, plasmas, semiconductors, quantum-effect materials, vacuum, and emerging materials. Specific applications of these devices include bioelectronics, biomedical, computation, communications, displays, electro and micro mechanics, imaging, micro actuators, optical, photovoltaics, power, sensors and signal processing.

Three fellowships are expected to be awarded to eligible students in each of the following geographical regions for 2018: Americas, Europe/Middle East/Africa, and Asia & Pacific. Only one candidate can win per educational institution.

Prize: US$5,000 to the student and if necessary funds are also available to assist in covering travel and accommodation costs for each recipient to attend the EDS Governance meeting in December 2019 for presentation of the award plaque. The EDS Newsletter will feature articles about the EDS PhD Fellows and their work over the course of the next year.

Eligibility: A candidate must be an IEEE EDS student member at the time of nomination; be pursuing a doctorate degree within the EDS field of interest on a full-time basis; and continue his/her studies at the current institution with the same faculty advisor for twelve months after receipt of award. The nominator must be an IEEE EDS member and preferable be serving as the candidate's faculty advisor. Previous award winners are ineligible.

Basis for Judging: Demonstration of his/her significant ability to perform independent research in the fields of electron devices and a proven history of academic excellence.

May 15, 2019 Submission Deadline

Nomination Package

- Nomination letter from an EDS member
- Two letters of recommendation from individuals familiar with the student's research and educational credentials. Letters of recommendation cannot be from the nominator.
- One-page biographical sketch of the student (including student's mailing address and email address)
- Two-page (maximum) statement by the student describing his or her education and research interests, accomplishments and graduation date
- One copy of the student's under-graduate and graduate transcripts/grades. Please provide an explanation of the grading system if different from the A-F format.

Timetable

- Completed nomination packages are due at the EDS Executive Office no later than **May 15, 2019**
- Recipients will be notified by July 15
- Monetary awards will be given by August 15
- Formal award presentation will take place at the EDS Governance Meeting in December

Please submit application packages via e-mail or mail:

Email: edsfellowship@ieee.org

Mail:
IEEE EDS Executive Office
PhD Student Fellowship Program
445 Hoes Lane
Piscataway, NJ 08854 USA

For more information contact:
edsfellowship@ieee.org

Visit the EDS website:
http://eds.ieee.org/eds-phd-student-fellowship.html

2019 Masters Student Fellowship

Description: One-year fellowships will be awarded to promote, recognize, and support graduate Masters level study and research within the Electron Devices Society's field of interest. The field of interest for EDS: all aspects of engineering, physics, theory, experiment and simulation of electron and ion devices involving insulators, metals, organic materials, plasmas, semiconductors, quantum-effect materials, vacuum, and emerging materials. Specific applications of these devices include bioelectronics, biomedical, computation, communications, displays, electro and micro mechanics, imaging, micro actuators, optical, photovoltaics, power, sensors and signal processing.

Fellowships are expected to be awarded to eligible students in each of the following geographical regions for 2019: Americas, Europe/Mid-East/Africa, and Asia & Pacific. Only one candidate can win per educational institution.

Prize: US$2,000 and a plaque to the student, to be presented by the Dean or Department head of the student's enrolled graduate program.

Eligibility: Candidate must be an IEEE EDS student member at the time of nomination; be accepted into a graduate program or within the first year of study in a graduate program in an EDS field of interest on a full-time basis; and continue his/her studies at a graduate education institution. The nominator must be an IEEE EDS member and preferably be serving as the candidate's mentor or faculty advisor. Previous award winners are ineligible.

Basis for Judging: Demonstration of his/her significant ability to perform research in the fields of electron devices a proven history of academic excellence in engineering and/or physics involvement in undergraduate research and/or a supervised project.

May 15, 2019
Submission Deadline

Nomination Package

- Nomination letter from an EDS member who served as candidate's mentor or faculty advisor.
- One letter of recommendation from an individual familiar with the student's research and educational credentials. Letters of recommendation cannot be from the nominator.
- One-page biographical sketch of the student (including mailing address and e-mail address)
- Two-page (maximum) statement by the student describing his or her education and research interests, accomplishments and graduation date. This can include undergraduate, graduate and summer internship research work.
- One copy of the student's transcripts/grades. Please provide an explanation of the grading system if different from the A-F format.

Timetable

- Completed nomination packages are due at the EDS Executive Office no later than **May 15, 2019**
- Recipients will be notified by July 15
- Monetary awards will be presented by the Dean or Department Chair of the recipient's graduate program at the beginning of the next academic term.

Please submit application packages via e-mail or mail:

Email: s.lehotzky@ieee.org

Mail:
IEEE EDS Executive Office
PhD Student Fellowship Program
445 Hoes Lane
Piscataway, NJ 08854 USA

For more information contact:
Stacy Lehotzky
Email: s.lehotzky@ieee.org

Visit the EDS website:
http://eds.ieee.org/eds-masters-student-fellowship.html

EDS Young Professional and Women in Engineering Breakfast Meetup

Young engineering professionals attending the IEDM in San Francisco were treated to a fun, networking event. The early morning breakfast meetup, sponsored by EDS, kicked-off the conference. About 60 university students, recent graduates, and young professionals had the opportunity to meet some of the top researchers in electron devices. These invited guests shared their best practices, via video interviews and in-person, on how to get the most from the IEDM. The relaxed atmosphere made it possible for the students and young researchers to approach and make connections with well-known experts of industry and academia. Our honored guests were generous with their time and knowledge, and we hope the experience helped to forge valuable new contacts for everyone.

The event, promoted with live updates on Facebook, LinkedIn and Twitter, showed attendees having fun connecting with each other using colored LED lights. The delicious breakfast, stimulating conversations, and group picture taking, helped to create a lively, interactive event for all.

The society is planning more of these networking events at major EDS sponsored conferences in the coming year. Join the EDS community on Facebook, Twitter and LinkedIn to view videos and pictures from the IEDM event, and for future meetup announcements.

A special thanks to all the volunteers and EDS committee members who gave their valuable time and advice. Without you, this event would not have been such a success.

New Webinars Available in the EDS Collection

EDS is many things to its members–scientific publisher, technical conference sponsor, networking resource–but at its core EDS is a community of learning. From undergraduate students and PhD candidates to tenured professors and world-renowned researchers, EDS provides device engineers from across the spectrum engaging and enriching educational opportunities.

As part of our commitment to enhancing the value of membership in EDS, we are pleased to present the EDS Webinar Archive. The online collection provides our members with on-demand access to streaming video of past events. Recently held webinars can be accessed here, http://eds.ieee.org/webinar-archive.html

Next-generation Electronics with 2D Materials—from atoms to applications

Presented by: Kaustav Banerjee

Abstract

Two-dimensional (2D) van der Waals materials such as graphene and various transition metal dichalcogenides (such as MoS2) possess a wide range of remarkable properties that make them attractive for a number of applications, including sub-5 nm VLSI (Physics Today, Sept. 2016). I will highlight the prospects of 2D materials for innovating energy-efficient transistors, sensors, interconnects, and passive devices targeted for next-generation electronics needed to support the emerging paradigm of the Internet of Things (IoT). More specifically, I will bring forward a few applications uniquely enabled by 2D materials and their heterostructures that have been demonstrated in my lab for realizing ultra-energy-efficient electronics. This includes the invention of the highest inductance-density materials ever made that helped

overcome a 200- year old limitation of the Faraday-inductor and has opened up a new pathway for designing ultra-compact IoT systems (Nature Electronics 2018). Other innovations from my lab are the world's thinnest channel (only two atomic layers of MoS2) band-to-band tunneling transistor that overcame a fundamental power consumption challenge in all electronic devices since the invention of the first transistor (Nature 2015), the first 2D-semiconductor channel based FET-biosensor with unprecedented sensitivity and promise of single-molecule detection (ACS Nano 2014), as well as a breakthrough interconnect technology based on doped-graphene-nanoribbons, which overcomes the fundamental limitations of conventional metals and provides an attractive pathway toward energy-efficient and highly reliable interconnects for next-generation integrated circuits (Nano Letters 2017). I will conclude with the prospects of monolithic 3D integration with 2D materials for realizing 3D ICs of ultimate thinness and integration density (IEEE S3S 2018).

Five Non-Volatile Memristor Enigmas Solved

Presented by: Leon Chua

Abstract

Numerous publications on non-volatile memristors made from disparate materials (from inorganic to organic) share many qualitatively similar memory switching and unique V-I phenomena that have hitherto defied a unified physical explanation.

This talk will address the definitive solution to the following 5 unsolved enigmas observed in all non-volatile memristors, regardless of their material composition and structure: (1) All non-volatile memristors have continuum memories. (2) The conductance of all non-volatile memristors can be tuned by applying single voltage pulses. (3) Faster switching can always be achieved by increasing the pulse amplitude. (4) Periodic unipolar input gives non-periodic finger-like multi-prong-pinched hysteresis loops. (5) DC V–I curves of non-volatile memristors are fakes.

Hybrid Systems-in-Foil: Enabler of Flexible Electronics

Presented by: Joachim N. Burghartz

Abstract

Flexible electronics add mechanical flexibility, shape adaptivity and stretchability as well as large-area place ability to electronic systems, thus allowing for conquering fundamentally new markets in consumer and commercial applications. Hybrid assembly of large-area devices and ultra-thin silicon chips on flexible substrates is viewed as an enabler to high-performance and reliable industrial solutions as well as to high-end consumer applications of flexible electronics. This talk discusses issues in ultra-thin chip fabrication, device modeling and circuit design, as well as assembly and interconnects for thin chips embedded into foil substrates in which flexible large-area components are implemented for an overall optimized Hybrid System-in-Foil (HySiF).

Chapter News

2018 EDS Chapter of the Year Award Winners

The EDS Chapter of the Year Award is presented annually to recognize chapters for the quality and quantity of the activities and programs implemented during the prior July-June period. In 2013, the Society expanded its Chapter of the Year Award to include one chapter in each IEEE Region (1 thru 7, 8, 9 and 10).

The 2018 EDS Chapter of the Year Award winners

- **ED/CAS North Jersey Chapter** (Regions 1-7)—EDS President, Fernando Guarin, presented the award to Durgamadhab Misra, at the EDS Board of Governors Awards Dinner, December 2nd
- **ED/SSC University of Nis Student Branch Chapter** (Region 8)—award presentation to be decided
- **ED/RA Tunja Chapter** (Region 9)—award presentation to be decided
- **ED Malaysia Chapter** (Region 10)—award presentation to be decided

EDS President, Fernando Guarin (left), presenting the Regions 1-7 award to Durga Misra, Chair of the ED/CAS North Jersey Chapter

M. K. Radhakrishnan
EDS Vice-President of Regions/Chapters
Email: radhakrishnan@ieee.org

ED Malaysia Kuala Lumpur Chapter—2018 EDS Chapter of the Year Award Winner for Region 10

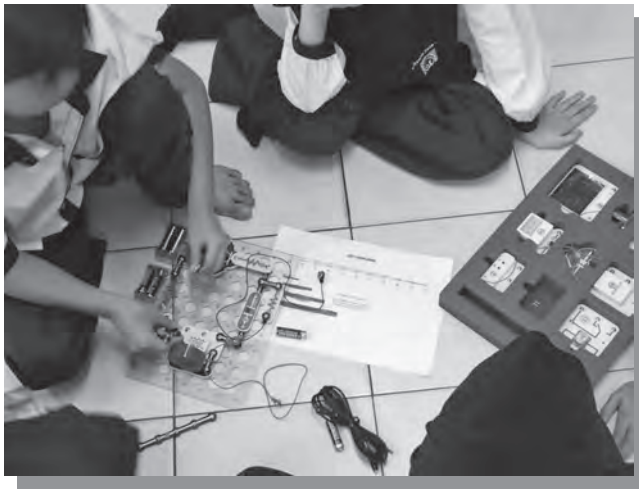
By Aliza Aini Md Ralib & Afishah Alias

Engineers Demonstrating Science: an Engineer Teacher Connection (EDS-ETC) by ED Malaysia Chapter

The ED Malaysia Chapter is committed in promoting the EDS-ETC program by conducting a fun and exciting event with primary school students (Year 4) at Sekolah Islam Adni Ampang, Selangor. A total of 30 students participated in the event. With the theme of "Material Diversity," the students were introduced to graphite material that can be used as an electrical conductor. They were guided to explore on graphite (from 2B pencil leads) as part of snap circuit elements which can produce different sounds at different lengths of graphite. From the experiment, they understand that graphite is a type of nanomaterial that can produce graphene which has so many outstanding characteristics. Students are all excited to try their hands on snap circuits and explore new things especially on graphite. The school management welcomes IEEE EDS-ETC engagement in school activities to stimulate creative young minds especially in the field of electronics. —Reported by Dr. Rosminazuin Ab Rahim

Hiking at Broga Hill

The IEEE ED Malaysia Chapter organized a hiking activity as part of the



Participants of the EDS-ETC event at Sekolah Islam Adni Ampang

Participants of the Broga Hill hiking trip

program planned for the Social and Community Portfolio, July 21, 2018 at Broga Hill. The IEEE EDS Hiking 2018 program welcomed the participation of EDS members together with their respective families. This program was held mainly to reconnect and foster good relations among EDS members as well as to promote a healthy lifestyle among members. The participants were enjoying the nice view at the top of Broga Hill. A total of 10 participants took part in this event.

Delegation of EDS Malaysia & UKM Student Branch Chapter at Institute Technology Bandung, Indonesia

On August 25, 2018, a Lab Visit to Institute of Technology Bandung (ITB), Indonesia was conducted with the cooperation of EDS Malaysia, EDS UKM Student Branch and FKEPS, UiTM Shah Alam. This trip was led by Dr Ahmad Sabirin, Associate Professor Dr. Norhayati Soin and 6 others from the ED Malaysia and ED UKM Student Branch Chapter, with the cooperation of ED Indonesia Chapter Chair, Professor Basuki Alam(ITB). The delegation were given the opportunity to visit the lab and being exposed to the developing research in Indonesia.

Mini-Colloquium at IMEN, UKM

A EDS Mini Colloquium was conducted August 13, 2018, at the Research Complex of Universiti Kebangsaan Malaysia (UKM). Sixty participants attended the MQ to hear 4 Distinguished Lecturers share their research expertise on applications of semiconductor devices:

- Dr. M. K. Radhakrishnan (NanoRel Technical Consultants), "*Interface Physics and Analysis Challenges in Si Nanodevices*,
- Dr. Navakantha Bhat (IISc Bangalore), "*PathShodh : A Journey from science to product*,"
- Dr. Samar K. Saha (Prospicient Devices, USA) "*Emerging Field-Effect Transistors for Ultra-Low Power VLSI Circuits at Nanometer Nodes*," and
- Dr. Edward Yi Chang (National Chiao Tung University, Taiwan) "*Nano-scale InGaAs FinFETs and Negative Capacitance InGaAs*

EDS Malaysia and EDS UKM SB delegation to EDS Indonesia

IEEE Malaysia Section and EDS Malaysia at the TISP program in Kelantan with Snap Circuits kits

IEEE EDS Malaysia Chapter Postgraduate Award recipient (a) Ahmad Anwar Zainuddin from IIUM (b) Intan Helina Hasan from ITMA UPM (c) Noor Hidayah Binti Mohd Yunus from IMEN UKM

MOSFETs for Low Power High Speed Post-Si Applications."

The event concluded with the presentation of the EDS Malaysia Postgraduate Award.

2018 IEEE EDS Malaysia Chapter Postgraduate Awards

During the mini-colloquium on August 13, 2018, the 3rd IEEE EDS Malaysia Postgraduate Awards was conducted concurrently, where awards were given away to shortlisted IEEE EDS student members who are pursuing their MSc and Phd research in Malaysia. The winners were Ahmad Anwar Zainuddin from IIUM with his PhD project "*Integrated Electrochemical and Mass Biosensor for early Dengue Detection*" (MEMS & Nanoelectronics cluster), Intan Helina Hasan from ITMA UPM with her PhD project "*Polycrystalline Ferrites Based Thick Film Paste for Improved Microstrip Patch Antenna*" (Material, Process & Product cluster) and Noor Hidayah Binti Mohd Yunus from IMEN UKM with her PhD project "*Ultra Low Power RF Energy Harvester for Battery-less Remote Control*" (IC Design cluster). Each winner received an honorarium of RM100, certificate and a plaque. Congratulations to all winners. The prizes were given away by EDS Vice President, Dr. M. K. Radhakrisnan.

EDS ETC and IEEE Teacher-In-Service Program (TISP) at Kelantan

The ED Malaysia Chapter is committed in promoting EDS-ETC events by participating in Science, Technology, Engineering & Mathematics (STEM) Teachers Colloquium organized by the Malaysian Ministry of Education on August 14, 2018, at Universiti Malaysia Kelantan, Malaysia. An exhibition booth was set up to promote the IEEE Teacher-In-Service Program (TISP) as well as Snap Circuits® kits among teachers and students. A total of 1,000 teachers and students attended the event. It is hoped by participating in this event, the visibility of IEEE and EDS-ETC events can be realized and the objective of EDS-ETC to engage young students in the field of electrical and electronics engineering can be achieved.

~P Susthitha Menon, Editor

2019 EDS Chapter of the Year Award—Call for Nominations

The EDS Chapter of the Year Award is given each year based on the quantity and quality of the activities and programs organized by the chapters for the benefit of members and professionals during the prior July 1st–June 30th period.

Each year EDS will award one Chapter from each of the following Regions:

- **Regions 1–7**
- **Region 8**
- **Region 9**
- **Region 10**

Nominations for the awards can only be made by SRC Chairs/Vice-Chairs, Regions/Chapters Committee Members or self-nominated by Chapter Chairs. Please visit the EDS website to submit your nomination form (http://eds.ieee.org/chapter-of-the-year-award.html).

Each winning chapter will receive a plaque and check for $500 to be presented at an EDS chapter meeting of their choice. Travel reimbursement will not be provided. A chapter that wins the Chapter of the Year Award is eligible for nomination after a lapse of 3 years only.

The schedule for the award process is as follows:

Action	Date
Call for nominations e-mailed to chapter chairs, SRC Chairs, SRC Vice-Chairs and Regions/Chapters Committee	June 1st
Deadline for nominations	September 15th
Regions/Chapters Committee & SRC Chairs & Vice Chairs selects winners	Early-October
Award given to chapter representative at requested chapter meeting	Open

EDS-ETC Program—An Educational Outreach Resource for EDS Chapters

My name is Luis Miguel Quevedo, global representative for the EDS-ETC program, a complimentary resource for all EDS chapters through which we donate instructional electronic kits incentivizing the study of electronic engineering to children worldwide. I invite you to learn more by visiting the following link https://eds.ieee.org/the-eds-etc-program.html, and request that your EDS chapter obtain some of the kits so that you can perform activities in your local communities, helping bring the world of electronics to a wider audience.

Chapters Bogota Colombia

University of Nis, Serbia

Hong Kong, China

Patos de Minas / MG / Brazil

Penang, Malaysia

Please inform us of when you perform these activities by filling out the report at the following link https://ieeeforms.wufoo.com/forms/edsetc-event-report/ this will help us track all sessions performed and with your feedback improve where needed. All regions are invited to participate and make use of these kits, I look forward to hearing about your events and how we expand our impact. Don't hesitate to contact Joyce Lombardini with any further questions or comments j.lombardini@ieee.org

I invite you to create competitions that incentivize the development of local technological solutions to daily issues, above please find some leading examples.

Luis Miguel Quevedo was born in Bogota, Colombia. He received his B.S. degree in mechatronic engineering from the University of San Buenaventura, Bogota, in 2015 and the specialization degree in business and services of telecommunications from the same University in 2016. He is a member of committee of student activities in the IEEE Colombia Section.

~ Edmundo Guiterrez-D., Editor

2nd IEEE Electronic Exploration Camp—ED UCAS Student Chapter and ED Beijing Chapter

By Tiancheng Gong

The 2nd IEEE Electronic Exploration Camp in IMECAS, Beijing, China was launched on July 18–21, 2018 at the Institute of Microelectronics of Chinese Academy of Sciences (IMECAS) by the ED UCAS Student Chapter and ED Beijing Chapter.

Prof. Ming Liu, Prof. Baoqin Chen from IMECAS and Prof. Mansun Chan from HKUST came on the first day of this camp to give a warm

2nd IEEE Electronic Exploration Camp participants Group Photo

Closing Ceremony of 2nd IEEE Electronic Exploration Camp

welcome to all the 50 participants from all over the country.

During the 4-day camp, the students constructed DIY running light, shining stars and a cleaning robot with the help of 9 volunteers. Furthermore, they took part in the magic cube talks which were presented by Prof. Baoqin Chen. They also attended science lectures on semiconductor physics in the University of Chinese Academy of Sciences, Yanqi Lake Campus.

On the last day of the camp, Prof. Toshio Fukuda from BIT came to give a scientific report titled, "Today and Tomorrow of Robot." Prof. Fukuda also accepted the invitation to become the Distinguished Professor of IEEE Electronic Exploration Camp.

The camp has successfully stimulated the interest of the participants on electronic technology and cultivated their ability in problem solving. The parents of these students are satisfied with all the arrangement of the schedule and the design of the courses and give a good evaluation of this camp.

IEEE Electronic Exploration Camp— ED/SSC Hong Kong Chapter

By Yang Chai

To inspire schoolchildren to study and work in areas of related to electron devices and circuits, the ED/SSC Hong Kong Chapter organized a 3-day Electronic Exploration Day Camp on August 27–29, 2018, at the Hong Kong Polytechnic University (PolyU), with the Department of Applied Physics at PolyU.

Prof. Yang Chai served as the Chairman of the organization committee with solid support from Prof. Mansun Chan. Thirty-six schoolchildren came to PolyU to explore and enjoy the fun of electronic circuit construction. Through learning and trying to build a few interesting electronic circuits, they learned some basic electronic engineering concepts such as voltage and current, signals, electrical measurements, clock generation and use, the use of mathematics in engineering etc. During the lab tour they were also exposed to cross-disciplinary technologies such as control and robotic systems, with the kind arrangement efforts of the Department of Mechanical Engineering.

Apart from the education of the schoolchildren, the event also helped develop abilities of the eight student helpers who gave instructional guidance to the 36 schoolchildren in the electronic circuit construction and other educational activities over the three days. They are all science and engineering undergraduates. They were supervised from the preparation stage and they learned event organization, task management and problem solving. They experienced the importance of being able to communicate technical ideas in a concise manner throughout the process of guiding the kids to construct the electronic

Schoolchildren getting to the campus of PolyU for the exciting three days of learning and fun

Both boys and girls took pleasure in the electronic circuit construction with instructional guidance by university student helpers

circuits. Despite the challenges of instructing the kids and maintaining classroom discipline, none of them gave up and helped bring the day camp to successful completion.

To help those from underprivileged families, which may have economic difficulty in paying the camp fees, a fee-waiving scholarship was also arranged after its introduction last December. Four schoolchildren were awarded the scholarship for joining this IEEE Electronic Exploration Day Camp. The administrative support was provided by a new contractor which is keen to reach out to underprivileged kids in Shum Shui Po districts. With their excitement and skill in electronic circuit construction developed in the three-day event, both the scholarship recipients and other schoolchildren have been encouraged to explore more about STEM areas in the future, including their pursuit of related studies and application of the learned concepts in daily life.

~ Ming Liu, Editor

Mini-Colloquia and Distinguished Lectures

IEEE EDS Schenectady 2018 Mini-Colloquium on Future Electronics

By Katharine Dovidenko

EDS Schenectady and the IEEE student branch (Union College) co-hosted a mini-colloquium (MQ) with the theme "Future Electronics" on May 25, 2018 at Union College, Schenectady, New York. Approximately 80 participants including faculty, students and industry attended the event. The MQ kicked-off with Dr. Katharine Dovidenko (vice-chair for the Schenectady Chapter) and Prof. Luke Dosiek (ECE, Union College) introducing EDS, Union College and the invited speakers. The technical program included 4 speakers from the Capital District Region, with contributions from industry and academia:

- Dr. Isabelle Ferain, Globalfoundries—"A Giant Leap in the Nanotechnology World"

Participants of the Mini-Colloquium on Future Electronics at Union College, Schenectady, New York

- Dr. Dechao Guo, IBM Research–"An Overview of Semiconductor Technology: History, Challenges and Opportunities"
- Dr. Ljubisa Stevanovic, GE Global Research Center—From SiC MOSFET Devices to MW-Scale Power Converters"
- Prof. Mona Hella, Rensselaer Polytechnic Institute—"TeraWaves: New Opportunities for Silicon Integration"

The technical program gave a broad overview of core and differentiated technologies that will be driving the next wave of innovations in electronics. These talks were followed by lively technical discussions and networking between the invited speakers and participants.

~ Rinus Lee, Editor

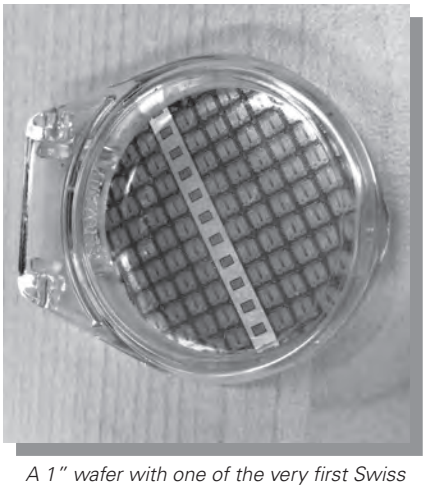
IEEE LM Workshop on History of Microchips in Switzerland

By Hugo Wyss

The Swiss IEEE LM organized a local workshop on "History of microchips in Switzerland," on October 30, 2018. This workshop is a follow-on of the IEEE Milestone celebration of February 22, 2018 in Neuchatel, and was held in the historical building which housed the Centre Electronique Horloger, CEH at its inception in 1962.

An article on this celebration has been published in the Region 8 news of September 2018. In this article the remarkable achievement of Dr. Kurt Hubner, an alumnus of William Shockley in Mountain View from 1958 to 1962, was highlighted and marks the early entrance of microchip/silicon

The IEEE Milestone for the developments of Swiss quartz watch (Uni. Neuchatel at Rue A.L. Breguet 2)



A 1" wafer with one of the very first Swiss integrated circuits

J.-D. Chauvy's lecture in Session 1: From Germanium to Silicon, 1955–1970; chaired by H. Wyss, IEEE LM (sitting at far right)

bipolar IC technology in Continental Europe and particularly Switzerland.

Kurt Hubner began working at CEH in May 1963 and already by July 1964 a full working waferfab produced the first silicon intergrated circuit. This was only 4 years after the first silicon IC (a 4 transistor flip-flop) was produced in May 1960 at the waferfab of Fairchild Semi by Bob Noyce.

The year 2019 marks 60 years from the date of two fundamental patents, which today are still the pillars of the whole digital world: Jean A. Hoerni (a Swiss physicist) planar patent based on the properties of Silicon Dioxide/Silicon interface, and Robert Noyce patent on monolithic silicon integrated circuits.

The event was organized and chaired by Hugo Wyss, IEEE LM. It contained two sessions. The first session dealt with the topic, "From Germanium to Silicon, 1955–1970" with speakers W. Grabinski (EDS), M. Lamoth (Favag), J.-D. Chauvy (CEH), H. Wyss (IEEE LM), and E. Vittoz (early CEH period). The second session contained the topic, "From Bipolar to CMOS, 1970–1980" with speakers H. Wyss (IEEE LM), N. de Rooji (IMT), Claude Bourgeois (CEH), P.-R. Beljean (AMSTN), and others (open discussion).

~ Mike Schwarz, Editor

Mini-Colloquium and 8th SINANO Modeling Summer School in Tarragona, Spain

A Mini-Colloquium on Semiconductor Device Modeling, organized by the ED Spain Chapter, was held the morning of September 25th at the Campus of the University Rovira I Virgili (URV), in Tarragona, Spain. The Chair of the MQ was Prof. Benjamin Iñiguez, from URV. It consisted of four talks given by EDS Distinguished Lecturers (DLs).

Prof. Sorin Cristoloveanu (MINATEC, France), addressed characterization techniques for ultrathin materials and devices. Prof. Jamal Deen (McMaster University, Hamilton, ON, Canada) targeted the compact modeling of organic transistors. Prof. Tibor Grasser conducted a lecture about multiscale reliability modeling. Finally, Dr. Wladek Grabinski (GMC, Switzerland) talked about FOSSTCAD/EDA tools for compact modeling.

This Mini-Colloquium was held prior to the 8th SINANO Modeling Summer School, which took place in Tarragona from the afternoon of September 25 to September 28, and was organized by the Department of Electronic, Electrical and Automatic Control of the University Rovira i Virgili. Both events integrated the SINANO Multiscale Modeling Summer School. 50 people attended this event. Prof. Benjamin Iñiguez was also the Chair of the 8th SINANO Modeling Summer School.

(left to right) DLs Wladek Grabinski, Sorin Cristoloveanu, Jamal Deen, Tibor Grasser and Benjamin Iñiguez, at the URV Campus (Tarragona, Spain) during the MQ on September 25, 2018

The SINANO Modeling Summer School is a European bi-annual comprehensive set of lectures aimed at doctoral or postdoctoral level researchers from both industry and academia. It was established in 2005, under the umbrella of the SINANO Network of Excellence (funded by EU's Seventh Framework Programme for Research (FP7)). The previous editions were held in Glasgow (2005) and in Bertinoro, Italy (2016, 2014, 2012, 2010, 2008, 2006).

The 8th SINANO Modeling Summer School in Tarragona included 19 lectures conducted by top researchers in areas related to semiconductor device modeling. The lectures addressed modelling, simulation and characterization of different types of semiconductor devices for nanoelectronics, flexible electronics and photonics. Very hot topics, such as devices for quantum computing, neuromorphic computing, THz electronics and printed electronics were also targeted.

~ Mike Schwarz, Editor

Mini-Colloquium on Advanced Materials and Devices: Challenges and Opportunities

By Lluis F. Marsal

(left) Prof. T. Otsuji, (center) Prof. F. Schwierz, and (right) Prof. F.J. García-Sánchez, Prof. B. Iñiguez, Prof. F. Guarin and Prof. L. F. Marsal

On Tuesday, November 13, 2018, the Electron Devices Spain Chapter organized a mini-colloquium linked to the 12th Spanish Conference on Electron Devices (CDE), held in Salamanca, November 14–16, 2018. The Chair of the mini-colloquium was Prof. Lluís F. Marsal (ED Spain Chapter Chair) from Universitat Rovira i Virgili (URV), Tarragona, Spain. Six invited speakers, all of them EDS Distinguished Lecturers, contributed talks ranging from advanced materials and semiconductor device technologies to design, compact modeling and reliability. A total of 40 students and researchers participated the MQ.

Prof. Frank Schwierz from the Technische Universitaet Ilmenau, Germany, gave a talk titled "The prospects, merits, and limitations of 2D electronics," Prof. Taiichi Otsuji from the Tohoku University, Japan, presented a talk on "Recent advances in 2D electronic and plasmonic terahertz devices utilizing graphene-based 2D materials," Prof. Fernando Guarin, from GlobalFoundries, New York, USA, presented his lecture titled "Leveraging semiconductor technology for the benefit of society. Prof. E. Miranda, from the Autonomous University of Barcelona (UAB), targeted the "Recent advances in compact modeling of ReRAM devices", Prof. B. Iñiguez from the Universitat Rovira i Virgili (URV), Spain addressed "The compact modeling and parameter extraction of Amorphous Oxide TFTs". Finally, Prof. L. F. Marsal from the Universitat Rovira i Virgili (URV), Spain gave a talk titled "Fabrication and characterization of high efficiency polymer solar cells".

~ Mike Schwarz, Editor

Distinguished Lecture at ED/MTT/AP/EMC Czechoslovakia Chapter

By Marcin Janicki

The Czechoslovakia Chapter and Czech Technical University in Prague organized two IEEE Distinguished Lectures on September 3 and 4, 2018.

The first was a CAS and EDS Distinguished Lecture by Dr. Rajiv Joshi, research staff member and key technical lead at T. J. Watson Research center, IBM. The lecture titled, Technology Circuit Co-Design for Nano-Scale Era, focused on technology pros and cons, variability impact, methods to evaluate it and circuit aspects in co-design and also on clever usage of TCAD to predict device and circuit capacitances.

The second lecture was an EDS Distinguished Lecture by Prof. Muhammad

Mustafa Hussain, fellow of American Physical Society and Institute of Physics, and an editor of *IEEE Transaction on Electron Devices (T-ED)*. The title of the lecture was: Manufacturable Heterogeneous Integration of Compliant CMOS Electronics for Interactive Electronic Systems. The lecturer addressed questions such as: Can CMOS technology be expanded further to achieve new features in CMOS electronics while maintaining and/or strengthening existing attributes? Will the functionalities over cost be advantageous? Can the existing applications be further strengthened and/or diversified? What potential applications may emerge?

He discussed also the rational design of materials, processes and devices to develop robust manufacturing processes through heterogeneous integration of state-of-the-art CMOS technologies to transform conventional high performance but rigid CMOS electronics into fully compliant one; various printing techniques (inkjet for interconnects, 3D printing for encapsulation); electrochemical deposition (ECD) for through polymer via (TPV); automated transfer; Lego like lock and key assembly; non-functionalized household papers and other responsive materials based sensors and actuators, respectively and finally their roll-to-roll processing to achieve nature inspired fully compliant in-plane and out-of-plane CMOS electronics for emerging IoE applications.

Dr. Joshi and Dr. Voves

Prof. Hussain during his lecture

EDS Distinguished Lecture at Japan Chapter

By Akira Nishiyama and Yuichiro Mitani

Prof. Ravinder Dahiya, University of Glasgow

The EDS Japan Joint Chapter (Chair: Akira Nishiyama) held an EDS Distinguished Lecturer program on September 3rd in Tokyo, Japan, co-hosted with Department of Electrical and Electronic Engineering (Prof. Takao Someya), The University of Tokyo. Prof. Ravinder Dahiya, University of Glasgow, lectured on "Large Area Flexible Electronic Skin," in which various approaches for obtaining distributed electronics and sensing components on flexible and conformable substrates were introduced, especially in context with tactile or electronic skin (e-skin). After his talk, the detailed processes and the outlook of this technology were discussed with the attendees.

Attendees of the IEEE EDS Distinguished Lecture held at The University of Tokyo in Tokyo, Japan on September 3, 2018. [front row from center to right] Prof. Ravinder Dahiya, Prof. Takao Someya (Professor of Department of Electrical and Electronic Engineering, The University of Tokyo), Dr. Akira Nishiyama (Chair of IEEE EDS Japan Joint Chapter)

~ Kuniyuki Kakushima, Editor

USA, Canada & Latin America (Regions 1–6, 7 & 9)

ED/PHO Columbus

—by Paul R. Berger

The ED/PHO Chapter of Columbus, Ohio Section organized two talks in 2018. The first talk was delivered by our IEEE EDS President, Dr. Fernando Guarín of GlobalFoundries. He presented an overview of how technological innovations benefit humanity with a talk on "Leveraging Semiconductor Technology for the Benefit of Society." Dr. Guarín described the challenges of clean energy and clean water access, especially in remote corners of the world. He then pointed towards the advancements in photovoltaics and clean energy driven by the EDS community to address this global crisis. For instance, EDS Celebrated Member (2015) and IEEE Fellow B. Jayant Baliga's contributions to the insulated-gate bipolar transistor (IGBT) has resulted in tremendous energy savings worldwide. This is an example of how an EDS member can make a lasting impact. Additionally, Prof. Michael Shur of Rensselaer Polytechnic Institute presented a lecture on Terahertz Plasmonic Devices," detailing terahertz operation with semiconductor technologies and its ability to sense the environment. Plasmonically enhanced devices could lead to tremendous advancements in terahertz technology. Prof. Shur highlighted the field and showed its historical progress leading to today's opportunities. The greater Columbus, Ohio was invited through electronic bulletin boards, which lead to each lecture being cross-listed as a continuing education event for the IEEE community. Each lecture was followed by a reception where students and professionals could mingle with the speakers and engage the speakers in a more informal setting.

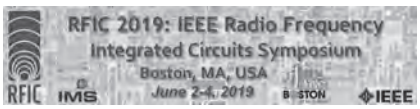
The ED/PHO Columbus Chapter, Ohio Section, organized one additional talk in Autumn 2018. This talk was delivered by Prof. Francesca Iacopi of University of Technology Sydney, who presented a view of wafer-scale graphene, titled "Graphene on silicon carbide: a versatile material system for integrated photonics and energy storage." Prof. Iacopi is also a core member of Australia's Centre for Clean Energy Technology. Prof. Iacopi brought an accompanying delegation from the Australian (Dr. Dennis Delic) and American (Dr. John Boeckl) Defense Research Labs, exploring collaborative US—Australia opportunities. As

Paul Berger and Fernando Guarin at the IEEE EDS event in Columbus, Ohio

Michael Shur presenting his lecture

Francesca Iacopi, Dennis Delic and John Boeckl

a member of the IEEE EDS Electronic Materials Subcommittee, Prof. Iacopi discussed with Prof. Berger, as the Chair of that Subcommittee, the potential launch of a Special Issue in Transactions on Electron Devices, focusing on "low temperature processing" to achieve state-of-the-art semiconductor device performance.



The 2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC 2019) will be held 2–4 June 2019 at the Boston Convention and Exhibition Center in Boston, MA, USA. The symposium starts on Sunday, June 2, 2019 with workshops and short courses, followed by two plenary talks and a reception featuring our top industry and student papers. Monday, June 3rd and Tuesday, June 4th will be comprised of oral presentations, an interactive forum, and panel sessions. The symposium solicits papers describing original work in all areas related to RF and millimeter-wave integrated circuits and systems. Work should be demonstrated through integrated-circuit hardware results. Original contributions are solicited in areas including but not limited to the following: Wireless Cellular and Connectivity, Low Power Transceivers, Receiver Components and Circuits, Analog and Mixed-Signal Blocks and SOCs, Reconfigurable and Tunable Front-Ends, Transmitter Sub-Systems and Power Amplifiers, Oscillators, Frequency Synthesis, Device Technologies, Packaging, Modeling, and Testing, Millimeter- and Sub-Millimeter Wave Communication and Sensing Systems, Emerging Circuit Technologies (NEW This Year): RF circuits and systems incorporating MEMs sensors and actuators, heterogeneous and 3D ICs, silicon photonics, quantum computing ICs, hardware security, and machine learning applications, Wearable systems, Biomedical applications, autonomous systems e.g. automotive and drones Implantable systems. For details please see the Call for Papers at the RFIC website rfic-ieee.org.

1st IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium

—by Peter Magnée and Brian Moser

From October 14 to 17, the first IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS) was held at the Sheraton San Diego Hotel and Marina, San Diego, California. After 39 years for the Compound Semiconductor Integrated Symposium (CSICS) and 32 years for the Bipolar/BiCMOS Circuit and Technology Meeting (BCTM), the two organizations merged and brought both communities together in one joint event. The Symposium was attended by close to 200 people, ranging from experts of both industry and academia, as well as a large number of students. In keeping up with good traditions from both parenting conferences, the event began with a short course on Sunday, titled "Phased Arrays and Massive MIMO: Technology and Systems." This course was provided by three well-known speakers: Mark Rodwell (UCSB), Gabriel Rebeiz (UCSD), and Amitava Ghoush (Nokia).

Since both CSICS and BCTM traditionally had a large student attendance, BCICTS wants to ensure the new merged symposium remains attractive for students and young professionals. Hence, on Monday morning the conference continued with so-called "primer-courses," with a more educational purpose (more basic than the short course) on specific topics relevant in the scope of the main symposium. This year the two primer courses, delivered by Pascal Chevalier, from ST-Microelectronics, and Shahriar Shahramian, from Bell Labs/Nokia, focused on "SiGe Technology and mmW Layout Techniques."

The main symposium began on Monday afternoon with a plenary session, and four invited presentations. In total, the conference had 20 sessions, divided over 3 days, delivering 66 papers with 16 of these invited, well-known experts in the field:

- P.1 Ullrich R. Pfeiffer, Institute for High-Frequency and Communication Technology, University of Wuppertal, Current Status of Terahertz Integrated Circuits—from Components to Systems.
- P.2 Jonathan Klamkin, University of California Santa Barbara, Indium Phosphide Photonic Integrated Circuits: Technology and Applications.
- P.3 Matthew Morton, Raytheon Company, The RF Sampler: Chip-scale Frequency Conversion and Filtering Enabling Affordable Element-level Digital Beamforming.
- P.4 Alvin Joseph, GLOBALFOUNDRIES, Technology Positioning for mmWave Applications: 130/90 nm SiGe BiCMOS vs. 28 nm RFCMOS.
- 1.1 Jonas Weiss, IBM Research—Zurich, Switzerland, Analog Optical RF-Links for Large Radio Telescopes.
- 2.1 Haedong Jang, Wolfspeed CREE Inc., Nonlinear Embedding of FET Devices for High Efficiency Power Amplifier Design.
- 4.1 Pascal Chevalier, STMicroelectronics, SiGe BiCMOS Current Status and Future Trends in Europe.
- 5.1 Alberto Valdes-Garcia, IBM T. J. Watson Research Center, Scaling Millimeter-wave Phased Arrays: Challenges and Solutions.
- 6.1 Sourabh Khandelwal, Macquarie University, Non-linear RF Modeling of GaN HEMTs with Industry Standard ASM GaN.
- 7.1 Dylan Williams, National Institute of Standards and Technology, On-Wafer Transistor Characterization to 750 GHz –the approach, results, and pitfalls.
- 9.1 E.A. Fitzgerald, Dept of Materials Science and Engineering,

During a session of the 1st IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium

MIT, Materials, Processes, and Markets for Monolithic III-V Devices in Silicon Integrated Circuits.

- 9.3 Tomio Satoh, Sumitomo Electric Device Innovations, Inc., GaN HEMT for Space Applications.
- 11.4 Steven Callender, Intel Corporation, FinFET for mmWave—Technology and Circuit Design Challenges.
- 12.1 Mark Lundstrom, Purdue University, Carrier Transport in BJTs: From ballistic to diffusive and off-equilibrium.
- 14.1 Mark van der Heijden, NXP Semiconductors, SiGe HBT PA design for 5G (28 GHz and beyond)—Modeling and Design Challenges.
- 16.1 P. Parikh, Transphorm Inc., 650 Volt GaN: Highest Quality-Highest Performance drives market ramp.

In total, out of the 50 unsolicited papers, 24 were delivered by students, and the last 3 sessions contained 9 Late-News papers, sharing breaking results that were obtained past the regular submission deadline. By audience voting, 2 papers were selected, and announced at the closing of the symposium, as Best Paper and Best Student Paper 2018:

- Best Paper: Alireza Zandieh, University of Toronto, 128-GS/s ADC Front-End with over 60-GHz Input Bandwidth in 22-nm Si/SiGe FD-SOI CMOS.
- Best Student Paper: Hasan Al-Rubaye, University of California San Diego, A DC-60 GHz I/Q Modulator in 45 nm SOI CMOS for Ultra-Wideband 5G Radios.

Besides the Technical Sessions, the BCICTS also hosted an exhibition, where 8 exhibiting companies presented their offerings to have more in-depth discussions with visitors. The exhibitors of the 2018 BCICTS were Virginia Diodes Inc., Silvaco, National Instruments, Advanced Test Equipment Rentals, Cadence, Maury Microwave, Stratedge Inc., and Presidio. Due to the close proximity to the technical sessions, and the informal atmosphere in the exhibition area, it was well-visited, creating high-quality traffic for exhibitors. The attendees also had a chance to interact and network at the Tuesday evening banquet at Tom Ham's Lighthouse with beautiful views of the water and the San Diego skyline.

After a total of 4 days, the first BCICTS can be considered a great success, and merging CSICS and BCTM has not only created a new conference, but also brought two strongly linked communities closer together to bring all the experts on dedicated, non-baseline CMOS, RF technology and circuit design closer together to discuss all trends in the industry and academic world. San Diego has once again, proven itself as an excellent location for a great event, and we look forward to the next edition of BCICTS, November 3–6, 2019, in Nashville, Tennessee. The 2019 BCICTS paper submission deadline will be May 3, 2019. Please go to the website bcicts.org for more details on submitting your work or about the symposium itself.

~ Rinus Lee, Editor

Europe, Middle East & Africa (Region 8)

14th International Seminar on Power Semiconductors (ISPS 2018)

—by Marcin Janicki

The 14th International Seminar on Power Semiconductors (ISPS 2018) was held in Prague, August 29–31, 2018. This conference provides a forum for technical discussion in the area of power semiconductor devices and their applications. It is a small conference with the special flair of an atmosphere of searching deeper

Poster session of the ISPS

Plenary session of the ISPS

insight and intensive discussion. The Conference was organised by IET Czech Network in co-operation with the IEEE Czechoslovakia Section and has been co-sponsored by the Faculty of Electrical Engineering, Department of Electrotechnology, Czech Technical University in Prague. The chairman of the conference was Prof Nando Kaminski from University of Bremen, GER and co-chairmens were: Prof Sankara N. Ekkanath Madathil, University of Sheffield, GBR, Prof Pavel Hazdra, Czech Technical University in Prague, CZE and Prof Josef Lutz, Chemnitz University of Technology.

Papers oriented in the field of power semiconductors were presented in sessions: Device Physics and Technology, Power Bipolar Devices, Voltage Controlled Power Devices, Wide Bandgap Power Devices, Power Integration, Advanced Applications and Packaging, Reliability & modelling. The opening lectures were given by Phil Rutter: "Life in the trenches—confessions of a Low Voltage Power MOSFET" and Gerhard Wachutka: "Virtual Prototyping of High Power Semiconductor Devices Based on Predictive Computer Simulation."

The invited lectures were: Fabrication of IGBTs Using 300 mm MCZ Substrates (Hans-Joachim Schulze, H. Öfner, F.-J. Niedernostheide); Multidirectional Development of IGBTs and Diodes: Low loss and Tough but Gentle (User-friendly) power device (Shigeto Honda, T. Minato, K. Shimizu, A. Furukawa, Y. Terasaki, K. Hatade and Y. Takata); SiC MOSFET Performance and Ruggedness for Demanding Applications (Ljubisa Stevanovic, Alex Bolotnikov, Pete Losee, Reza Gandhi, Maja Harfman Todorovic, and Arun Gowda); and Packaging Technology for a Highly Integrated 10kV SiC MOSFET Module (Bassem Mouawad, Christina DiMarino, C Mark Johnson). The conference was attended by 51 participants (including 17 IEEE members).

~ Marcin Janicki, Editor

2018 ESSDERC/ESSCIRC

The 48th European Solid-State Device Research Conference (ESSDERC) and 44th European Solid-State Circuits Conference (ESSCIRC), a forum for the presentation and discussion of recent advances in solid-state devices and circuits, was held September 4–6, 2018, in Dresden at the TU Dresden.

The ESSDERC conference was financially sponsored by the IEEE Electron Devices Society and ESSCIRC supported by SSCS. General sponsors have been:

- Diamond: Robert Bosch GmbH
- Platinum: Texas Instruments
- Gold: Global Foundries, Infineon, Melexis
- Silver: XFab, Mentor, Micron
- Bronze: Commsolid, CoolSilicon, fast, Fraunhofer Mikroelektronik, LFoundry, nature electronics, River Publishers, Rohde&Schwarz, Silicon Saxony

The conference was opened by the general co-chair of ESSDERC, Prof. Thomas Mikolajick (NaMLab and TU Dresden, DE), and the general co-chair of ESSCIRC Prof. Frank Ellinger (TU Dresden, DE), who welcomed the more than 600 attendees.

Prof. Thomas Mikolajick introduced into the procedure of both conferences by offering separate Technical Program for ESSDERC and ESSCIRC and encouraged the attendees to visit any of the scheduled parallel sessions, regardless to which conference they belong. Additionally he highlighted the Plenary Keynote Presentations and Joint Sessions bridging both communities.

Furthermore, Prof. Mikolajick highlighted the workshops and tutorials in the timeframe of the conference, which were held on September 3rd. The workshops were:

- Bosch Semiconductors
- SINANO NEREID

A few minutes before the conference opening ceremony, Dresden on September 4, 2018

Dr. Udo-Martin Gómez (Robert Bosch GmbH) held a talk titled "Smart Connected Sensors—Enablers for the IoT, Dresden on September 4, 2018

- MOS-AK
- SUPERAID7

While the tutorials offered were:

- Autonomous Driving: IC Robustness/Reliability/Readiness, Sensing & Mobility
- Sensors and Energy Harvesting
- Automotive IC Design

After the introduction and conference opening the first highlights of the conference, the joint plenary presentations of Udo-Martin Gómez (Robert Bosch GmbH) and Gary Patton (Global Foundries), followed. Udo-Martin Gómez held a talk titled "Smart Connected Sensors—Enablers for the IoT," which gave the attendees a vision of the upcoming IoT technologies provided by MEMS sensors. Gary Patton's talk "Unleashing Technology Solutions for a New Era of Connected Intelligence" offered the strategies of different use cases for FDSOI technologies. Two additional joint plenary presentations followed, one given by Baher Haroun (Texas Instruments) titled "Autonomous Vehicles Sensor Needs," and one by Evangelos S. Eleftheriou (IBM) with a vision how to accelerate AI application of mainframe technology by "In-memory Computing: Accelerating AI Applications."

In addition, three ESSDERC keynote presentations were offered by Shinichi Takagi (University of Tokyo) on "MOS Device Technology using Alternative Channel Materials for Low Power Logic LSI," by Louis Hutin (CEA Leti) on "Si MOS Technology for Spin-Based Quantum Computing" and by Debbie G. Senesky (Stanford University) on "GaN for the Future."

ESSCIRC offered three keynote presentations by Borivoje Nikolic (University of California Berkeley) on, "Generating the Next Wave of Custom Silicon," by Georg Sigl (TU München and Fraunhofer AISEC) on "Where Technology Meets Security: Key Storage and Data Separation for System-on-Chips" and by Aaron Partridge (SiTime Corp.) on "It Is Time for Time Itself to Come From Silicon."

On top of that, 128 contributed papers with deep insights and high-level technical content were presented during the conference and can be found in the proceedings.

The conference also held social activities such as a welcome reception at the "Gläserne Manufaktur," a VW showcase production fab for electric vehicles, next to the "Großer Garten" and a Gala Dinner at the "Albertinum," a museum hosting the New Masters Gallery.

In Summary, ESSDERC/ESSCIRC 2018 was an inspiring event similar to the last Editions in Lausanne and Leuven in 2016 and 2017. The ESSDERC/ESSCIRC community is looking forward to another exciting edition in Cracow, September 23–26, 2019 (https://esscirc-essderc2019.org/).

~ Mike Schwarz, Editor

2018 International Seminar/ Workshop on Direct and Inverse Problems of Electromagnetic and Acoustic Wave Theory

—by Kakhaber Tavzarashvili and Mykhaylo Andriychuk

The XXIII International Seminar/ Workshop on Direct and Inverse Problems of Electromagnetic and Acoustic Wave Theory (DIPED-2018) was organized by the IEEE MTT/ED/AP Georgia and MTT/ED/AP/EP/SSC West Ukraine Chapters. This year, DIPED was held at the Ivane Javakhishvili Tbilisi State University (TSU), Tbilisi, Georgia, on September 24–27, and it was dedicated to 100th anniversary of TSU and 80th anniversary of Prof. Revaz S. Zaridze, one of founders of the DIPED Seminar/ Workshop. The IEEE Ukraine Section and Pidstryhach Institute for Applied Problems of Mechanics and Mathematics, NASU, Ukraine, were the co-organizers of DIPED-2018. IEEE Electron Devices, Microwave Theory & Techniques, and Antennas & Propagation Societies provided the Technical Co-Sponsorship for the Seminar/Workshop. Prof. Revaz S. Zaridze, Chairman of the Organizing Committee, Dr. Tamar Gogua, IEEE MTT/ED/AP Georgian Chapter Secretary, and Prof. Kakhaber Tavzarashvili, IEEE MTT/ED/AP Georgian Chapter Chairman, put a lot of effort for the general and local organization of the event.

The DIPED-2018 technical program consisted of 50 papers, including 7 invited talks. Scientists from Georgia, Germany, Greece, Israel, Japan, Philippines, Poland, Russia, Tunisia, Turkey, USA, and Ukraine submitted their papers. The papers were arranged at the following sections:

- Diffraction and Scattering,
- Waveguides and Transmission Lines,
- Analytical and Numerical Techniques,
- Inverse Problems and Synthesis,
- Antenna Design,
- Medical and Geophysical Applications,
- Modeling in Electronics,
- Acoustics and Applications.

A large group of regular students, Ph.D. students and young scientists attended DIPED-2018. The following participants were granted by the DIPED-2018 Best Young Speaker Award:

- Mrs. Dariia Yevtushenko (Kharkiv National University of Radio Electronics, Kharkiv, Ukraine) for the presentation "Optical Diffraction Radiation of a Beam of Particles Flowing Near a Circular Silver Nanowire;"
- Mr. Ivan Petoev (Tbilisi State University, Tbilisi, Georgia) for the presentation "Localization of the

DIPED-2018 participants after opening ceremony

Scattered Field's Singularities Using the Method of Auxiliary Sources;"

- Mr. Ihor Zhbadynskyi (Pidstryhach Institute for Applied Problems of Mechanics and Mathematics, NASU, Lviv, Ukraine) for the presentation "Acoustic Filtering Properties of 3D Elastic Metamaterials Structured by Crack-Like Inclusions;"
- Mr. Vakhtang Barbakadze (Tbilisi State University, Tbilisi, Georgia) for the presentation "Directed Circular Polarized Antenna;"
- Mrs. Tamar Nozadze (Tbilisi State University, Tbilisi, Georgia) for the presentation "Mobile Phone Antenna's EM Exposure Study on a Homogeneous Human Model inside the Car."

The recipients of the Award were recognized with a special certificate from the Program Committee and a financial grant from the Organizing Committee.

Following the DIPED tradition, the conference participants spent alot of time in free lobby discussions. The concert of folk ensemble of TSU students, bus excursion to Mtsheta, first capital of Georgia, walking tour of Tbilisi were organized within the social program of the Seminar/Workshop. It was connected with acquainting with most interesting architectural sights of the Georgian capital city.

After the Seminar/Workshop technical program was completed, a traditional dinner was held. The Best Young Scientist Awards were presented there. The future improvement of the Seminar/Workshop format was discussed and participant suggestions were taken into consideration. It was announced that the next XXIVth DIPED-2019 Seminar/Workshop will be held at the Pidstryhach Institute for Applied Problems of Mechanics and Mathematics, NASU, Lviv, Ukraine, in mid-September, 2019. The previous attendees and new participants are cordially invited.

~ Daniel Tomaszewski, Editor

Asia & Pacific (Region 10)

EDS Mini-Colloquia Meeting—ED/SSC Nanjing Chapter

—by Weifeng Sun

The Nanjing EDS/SSCS Chapter held a special Mini-Colloquia Meeting including three invited Distinguished Lectures on July 11, at the College of Electronic Science and Engineering, Southeast University, hosted by Profs. Weifeng Sun and Wangran Wu. The three experts are all from National Chiao Tung University, Taiwan. About 20 senior graduate students and 5 professors attended the event.

The first lecture was given by Prof. H.-C Lin titled, "CMOS Technology: The present and the Future." Prof. Lin reviewed the evolution and important milestones of CMOS transistors and addressed the technological trends and major obstacles of state-of-the-art FinFETs and Gate-all-around nanowire/nanosheet FETs.

The second talk by Prof. Steve C. Chung, titled "The Development of OTP (One Time Programming) Memory for Embedded Applications in HKMG Generation and Beyond" gave a background review on the importance of HKMG NVM for the generations beyond 28 nm including NAND

ED/SSC Nanjing, Mini-Colloquia Meeting on July 11—(1st row, left) Steve Chung (4th, speaker), H. C. Lin (5th, speaker), P-W Li (6th, speaker), Wangran Wu (7th, seminar chair)

and NOR flash. Prof. Chung proposed a unique cell design of OTP, which is suitable for embedded NVM, using a specific fused-programming scheme for high density, high performance data storage applications. His team demonstrated a real macro chip design of the proposed OTP cell based on the current 28 nm HKMG generations.

The final talk given by Prof. Pei-Wen Li, titled "Back to the Future: Germanium Reemerges as the Savior of Si opto-electronics," gave a background review on the important milestones of Ge for semiconductor electronic and photonic devices. Prof. Li presented recent advances in Ge devices (MOSFETs, light emitter, modulators, and photodetector) supporting the Si nanoelectronics and photonics. Her team has successfully exploited a CMOS-compatible fabrication processes approach to create new classes of exciting photonic and electronic devices.

EDS Distinguished Lecturer—ED Tainan Chapter

—by Wen-Kuan Yeh

The ED Tainan Chapter held one Distinguished Lecture on August 30, 2018. Dr. Albert Chin (Professor of Electronics Engineering, Chiao-Tung University, Taiwan) gave one talk at National Cheng-Kung University, Taiwan, titled, "Ultra-low power & energy-efficient devices," which focused on ultra-low power device design for related applications. About 30 students and several professors from local universities attended.

ED Tainan, DL Talk on August 30th (front left to right) Dr. Prof. Jyi-Tsong Lin (Professor of NSYSU), Prof. Albert Chin (DL Speaker), Prof. Wen-Kuan Yeh (Chair of EDS Tainan Chapter), and some of the attendees

ED Beijing Distinguished Lecture on August 31st with Prof. Steve S. Chung

EDS Distinguished Lecture—ED Beijing Chapter

—by Kangwei Zhang

The ED Beijing Chapter invited EDS Distinguished Lecturer, Prof. Steve S. Chung from National Chiao Tung University to give a talk on August 31, 2018. Prof. Chung's talk, titled, "Embedded Flash Memory Technologies: Enabler for smart Phone, Automotive MCU, AI etc.," gave an overview on the current status of the embedded flash memory development. Then, he described two fundamental solutions for the embedded flash memory in terms of Resistance-based architecture which was feasible for the 28 nm CMOS compatible technology and beyond. Both are promising solutions for the future NVM technology, which do not need to have a concern of charge loss issue (in the current charge-based flash) and the sneak path problem. At last, he introduced the study of AI based on the resistance memory or logic-based high-end logic.

EDS Distinguished Lecture—ED Tsinghua Student Chapter

—by Yancong Qiao

The ED Tsinghua Student Chapter held one invited talk on July 12, 2018. The invited lecturer, Prof. Tawfique, ECTM Laboratory Technische Universiteit Delft, Netherlands, spoke on, "Printing Electronic." He discussed key ink formulation strategies of the novel 2D materials and printed devices and showed that the choice of unique solvent blends allowed engineering counteracting the Marangoni flows in drying droplets. This enabled uniform, reliable inkjet printing towards scalable development of printed electronic, photonic and optoelectronic devices of a range of 2D materials. At last, he moved into printing on conformable substrates as well as scalable, large format print technologies and showed that a combination of advanced materials printed by traditional graphics printing and contemporary electronics could promote simple and inexpensive, yet powerful technologies.

EDS Mini-Colloquia Meeting—ED Hangzhou Chapter

—by Lingling Sun

A Mini-Colloquium, jointly organized by the ED/MTT Hangzhou Chapter and the School of Microelectronics,

ED Hangzhou, MQ on July 9th-(First row from left) H. C. Lin (2nd, speaker), P.W. Li (3rd, speaker), Steve Chung (4th, speaker), Yi Zhao (6th, workshop chair) with attendances

Zhejiang University, was held on July 9, 2018 at Zhejiang University. Three Distinguished Lecturers from National Chiao Tung University, Hsinchu, Taiwan, were invited to give a brief view on the current status of advanced front-end devices and more-than-Moore technologies. Prof. Yi Zhao served as the workshop chair. Prof. Horng-Chih Lin, IEEE Senior Member and IEEE EDS Distinguished Lecturer, reviewed the current status of CMOS transistor manufacturing as well as addressing the technological trends and the major obstacles of FinFETs and Gate-all-around nanowire/nanosheet FETs. Prof. Steve Chung, IEEE Fellow, presented the strategies and solutions for the design of high-performance Si/SiGe based Tunneling FET for More-than-Moore and IoT applications. Prof. Pei-Wen Li, IEEE Senior Member and IEEE EDS Distinguished Lecturer, discussed a key enabler for the monolithic integration of Ge electronics and photonics including Junctionless FETs, photo MOSFETs and light emitter on Si-platform in CMOS technology for functionally-diversified applications in data transfer, IoT, and quantum computing. This event attracted about 30 graduate students and professors.

EDS Distinguished Lecture—ED UCAS Shanghai Student Branch Chapter

—by Binbin Pei

The EDS/UCAS Shanghai Student Chapter held an invited academic report on July 5th, at the Shanghai Institute of Microsystem and Information Technology, University of Chinese Academy of Sciences, hosted by Prof. Yuelin Wang. The report given by Dr. Limei Tian, from the University of Illinois at Urbana-Champaign, was titled "Bioplasmonics and Epidermal Electronics for Advanced Health Care."

EDS UCAS Shanghai Student Branch chapter, on July 5th—(left) Yuelin Wang (2nd), Dr. Limei Tian (3rd, speaker) with attendances

In Dr. Tian's lecture, she presented the design and implementation of plasmonic biosensors that rely on artificial antibodies as recognition elements Publicity and recruitment. In the second part of the talk, she discussed the recent advances in the design and fabrication of skin-interfaced wearable medical devices capable of continuously measuring and wirelessly transmitting biophysical and biochemical information.

~ Ming Liu, Editor

13th IEEE-International Conference on Semiconductor Electronics (ICSE 2018)

—by Burhanuddin Yeop Majlis, Azlan Azrul Hamzah & Khairul Nisha Mohd Kharuddin

The 2018 IEEE International Conference on Semiconductor Electronics (ICSE2018) was successfully held August 15–17, 2018, at the Pullman Hotel and Residences Kuala Lumpur City Centre. The conference was organized by the IEEE Electron Devices Malaysia Chapter, IEEE Malaysia Section and Institute of Microengineering and Nanoelectronics (IMEN), UKM and chaired by IMEN Founder Director/IEEE EDS Malaysia Advisor; Prof Dato Dr Burhanuddin Yeop Majlis. Themed "At the Edge of Nanotechnology," there were 80 papers presented at the conference with 120 participants attending. The conference kicked off on the 14th of August with two tutorial sessions presented by Dr. Samar K. Saha from Prospicient Devices, Milpitas, USA, with his session titled "*Advanced Silicon Devices*" and Dr. M.K. Radhakrishnan from NanoRel LLP, Singapore, with his session titled "*Building Reliability in Devices—Challenges and Progression.*"

ICSE2018 was proud to feature Prof. Dr. Jackie Y. Ying from NanoBio Lab A*STAR Singapore and Prof. Dr. Edward Chang from National Chiao Tung University, Taiwan, as the plenary speakers. Prof. Jackie

ICSE2018 conference committee, speakers and participants

Y. Ying delivered a plenary lecture on "*Nanosystems for Food, Drug and Biomedical Applications*" while Prof. Edward Chang lectured on "*High-performance E-mode GaN MIS-HEMT for Power Switching Applications.*" The keynote sessions featured prominent researchers namely Prof Navakantha Bhat from the Indian Institute of Science (IISc), Bangalore, India (Keynote title: *Tunable Steep Slope MoS_2 Transistor*), Prof. Jang-Kyoo Shin from Kyungpook National University, South Korea (Keynote title: *CMOS Pixel-Aperture and Offset Pixel-Aperture Techniques for 3-Dimensional Imaging*), Prof. Kevin Homewood from Hubei University, Rep. of China (Keynote title: *Band Edge Modified Rare Earths- A Route to the Mid Infrared in Silicon*) and Assoc. Prof. Dr. Tomas Blecha from West Bohemia University, Czech Republic (Keynote title: *Smart Firefighter Protective Suit—Functional Blocks and Technologies*). This is the 13th conference in the ICSE series which started since 1992 to gather semiconductor micro and nanoelectronics researchers from academia and industry.

The conference also featured an Industrial Session sponsored by IEEE Malaysia Section in an effort to expose participants to current industry trends. The speakers were Dr. Mohamad Jamil Sulaiman, Vice President for SIRIM Industrial Research and Mr. Ahmad Rizan Ibrahim, President & CEO of MIMOS Berhad. They shared the latest research being undertaken in their respective companies and industries and urged participants to collaborate for mutual research and development. During the conference dinner, ICSE2018 was proud to be officiated by UKM's Deputy Vice Chancellor, Prof. Mohd Ekhwan Toriman who also witnessed the signing ceremony of a Letter of Intent (LOI) and a Memorandum of Understanding (MoU). The LOI and MOU were signed between IMEN, UKM and University System of Taiwan as well as University of West Bohemia, Czech Republic respectively.

ICSE2018 offered Invited Papers to Academicians, Best Paper and Best Presenter Awards to student presenters as well as Best Industry paper for industrialists. The awards were accorded based on four main clusters and papers were evaluated by the session chairs and Technical Program Commitee. Overall the conference achieved its main objective of bringing together researchers from industry and academia to gather and explore various issues and trends in the field of semiconductor electronics. Results of the Best paper/best presenter awards are as follows:

- "*Comparative Study of Si Based Micromachined Patch Antenna Operating at 5 GHz for RF Energy Harvester*" by Noor Hidayah Mohd Yunus et al., UKM (Best paper Cluster 1)
- "*Photonic crystal embedded waveguide for compact C-band band-pass filter*" by Mohd Nuriman Nawi et al., UKM (Best paper Cluster 2)
- "*Effect of Different Metal Contact Distance and Light on Electrical Properties of Calcium Carbonate*

Thin Film" by N. H Sulimai et al., UiTM (Best paper Cluster 3)

- *"Dielectrophoresis: Iron Dificient Anemic Red Blood Cells for Artificial Kidney Purpose*" by Farahdiana Wan Yunus et al., UKM (Best paper Cluster 4)
- "*Comparative study of the Calcium Ferrite Nanoparticles (Ca-Fe2O4-NPs) Synthesis Process*" by Noor Sulaiman, UKM (Best presenter Cluster 1)
- "*Taguchi optimization of graphene-based Surface Plasmon Resonance-Kretschmann biosensor using FDTD*" by Nur Akmar Jamil, UKM (Best presenter Cluster 2)
- "*Design of Phase Frequency Detector (PFD), Charge Pump (CP) and Programmable Frequency Divider for PLL in 0.18 um CMOS Technology*" by Anim Arifah Ahmad, UKM (Best presenter Cluster 3)
- "*Modeling, Simulation and Optimization of 14 nm High-K/Metal Gate NMOS with Taguchi Method*" by S.K.Mah, UNITEN (Best presenter Cluster 4)
- "*Characterization of SOI Film Thickness, Oxide Thickness and Charges with C-V Measurement*" by Ke Kian Seng Joseph, Infineon Technologies (Kulim) Sdn Bhd (Best Industry Paper Cluster 1)
- "*Corner Mismatch Model for Fast Non-Monte Carlo Best and Worst Cases Simulation*" by Chiew Ching Tan, Silterra Malaysia Sdn. Bhd., MALAYSIA (Best Industry Paper Cluster 4)

~ P. Susithitha Menon, Editor

IEEE ED NIT Silchar Student Branch Chapter

—by T. R. Lenka

The ED NIT Silchar Student Branch Chapter organized an EDS Distinguished Lecture (DL) by Prof. Vijay K. Arora on December 20, 2017, in association with Dept. of ECE, NIT Silchar. Prof. Arora from Wilkes University, USA presented his research work titled: "*Research Methodology in Nanoscience.*" He provided insightful ideas on current scenario on nanoscience and distributed books authored by him among the attendees. There were about 40 IEEE EDS members/ student members comprising of faculty from NIT Silchar as well as graduate and undergraduate students from Dept. of ECE attended the DL Talk.

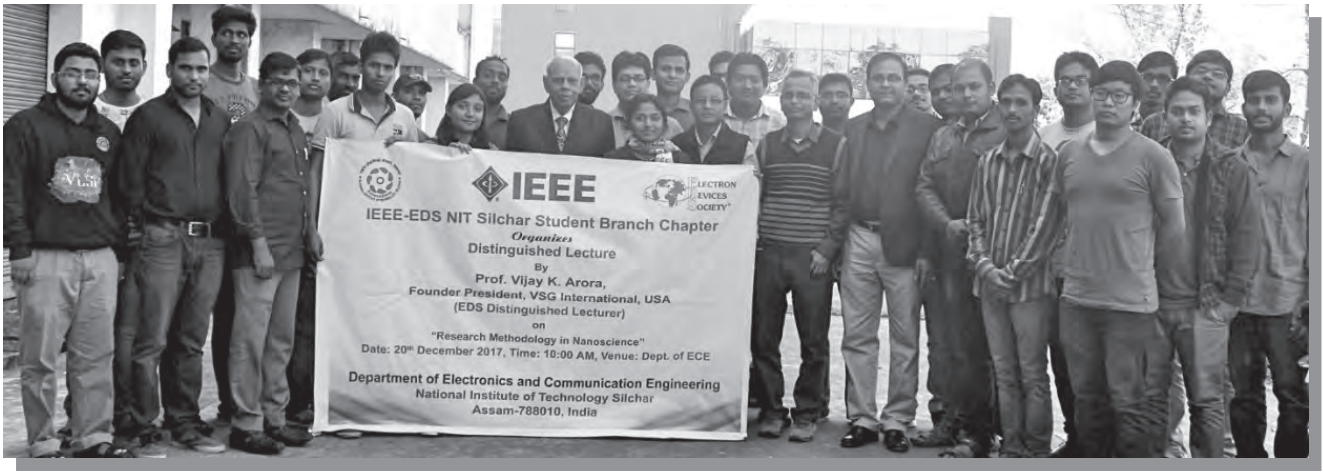
Department of of ECE, NIT Silchar organized, the Three-Day National Workshop on "CMOS MEMS Integration: Devices to Application," April 12–14, 2018 in association with the ED NIT Silchar Student Branch Chapter. The workshop was sponsored by DST-SERB (Science and Engineering Research Board) Govt. of India, and NIT Silchar.

The workshop focused on enlightening the research in the field of MEMS and CMOS technologies. The workshop was intended to end up with in depth knowledge of advantages of MEMS-CMOS integration and its applications. Six eminent personalities such as Dr. KJ Rangra, CSIR-CEERI Pilani, Dr. K. Srinivasa Rao, KL University, Dr. Roy Paily Palathinkal, IIT Guwahati, Dr. Prasanta Kumar Guha, IIT Kharagpur, Dr. Jyotirmoy Dutta, FTD Infocom Pvt. Ltd, India delivered invited lectures in the workshop. There were around 50 participants comprising of IEEE members and non-members from different institutions of North East India attended the workshop and acquired knowledge in both MEMS and CMOS Technology.

ED NIST (National Institute of Science & Technology) Student Branch Chapter

—by Ajit K Panda

The ED NIST Student Branch Chapter organized a five-day technical lecture series, April 22–26, 2018, at Electronics Center of Excellence (e-COE), DCB-621, DLF Cyber City, Patia, Bhubaneswar for the B. Tech graduates, Post Graduates and diploma students. The lecture series topic "CMOS Analog IC and Two-port Network Synthesis," attracted



Attendees of the EDS DL talk at NIT Silchar, (from left) Dr. V. K. Arora (EDS DL: Front middle position), Prof. S. Baisya (Senior Member, IEEE), Prof. F. A. Talukdar (Branch Counsellor, ED NIT Silchar SBC), Dr. T. R. Lenka (Faculty Advisor, ED NIT Silchar SBC), Mr. Soumyaranjan Routray (Student Chair)

(left to right): Dr. K L Baishnab (Co-convener), Dr. R. H. Laskar, Mrs. Madhumita Paul, Prof. F. A. Talukdar (HOD, Branch Counselor), Prof. Sivaji Bandyopadhyay (Director, NIT Silchar), Prof. S. Baishya (Chairman of workshop), Dr. Koushik Guha (Convener of workshop), Dr. T. R. Lenka, (Faculty Advisor)

more than 20 participants from different institutes and universities in and around Odisha. Mr. Ranjit Dash discussed analog IC design, two-port models, and synthesis of basic RC Networks. He emphasized working hands-on with RLC networks and most importantly selection of components based on specifications and applications. Students were given basic components to design and allowed to measure the parameters using high-end measuring instruments set at the center.

The chapter also organized a four-week technical lecture series from May 19 to June 16, 2018, at NIST, Palur Hill, and Berhampur for the 2nd and 3rd year B. Tech graduates on "VLSI Circuits and Role of Modern CAD Tools." More than 30 participants attended from the Odisha area. Dr. A. K. Panda delivered an IEEE Distinguished Lecture on recent trends in VLSI industries and job opportunities for the fresher. In his discussion, he pointed out the change in circuit complexity and saturation in terms of new design. CAD tools plays the major role in analyzing the complex circuits and helps students to get jobs in silicon industries. He also emphasized on free tools for use at the student level. The technical lecture concluded with the development and understanding of efficient models that make the simulations more realistic. The team also demonstrated the Tanner EDA, TINA-TI, and XILINX, followed by a practice session.

Mr. Ranjit Dash's lecture at NIST

Attendees of Dr. Panda's Distinguished Lecture at NIST

ED Uttar Pradesh Section—Kanpur Chapter

—by Yogesh Singh Chauhan

The ED Kanpur Chapter and the Department of Electrical Engineering, IIT Kanpur on June 25, 2018, organized a technical talk on Process Variability Modeling and Low Leakage Device Design in IoT Design Space, by Dr. Soumya Pandit, Institute of Radio Physics and Electronics, University of Calcutta. He discussed, in a comprehensive manner, the sources of process variability the strategies to incorporate the effects of process variability in circuit simulation. His talk introduced a new type of planar MOSFET structure targeted towards low cost applications. Epitaxial delta doped channel (EδDC) MOS transistor, based on planar MOS technology,

Participants of the EDS Lecture at IIT Kanpur

reduces the threshold voltage variability due to random discrete dopant (RDD) effect, through vertical channel engineering. The basic idea of drain current mismatch due to RDD was introduced and the ways to reduce the effects of drain current mismatch was discussed in a comprehensive manner. This talk was attended and nicely received by over 35 students and faculty members, which included 20 IEEE members.

ED Netaji Subhash Engineering College Student Branch Chapter

—by Saheli Sarkhel

The ED NSEC Student Branch Chapter co-organized with the Alumni Association of National Gems (AANG), a workshop for the students of class XII of National Gems Higher Secondary School. The event held on August 24th was titled, "*Familiarization with various electronic components using Snap Circuits® Kits*" as an activity of the EDS-ETC (Engineers Demonstrating Science: an Engineer Teacher Connection). The initiative to impart the knowledge of electronics among school students and inspire them to join electrical and electronics engineering. The workshop commenced with an introduction to the wide platform provided by the field of electronics, followed by an interactive session where basic circuits were built using the components of the Snap Circuits® Kits provided by the IEEE Electron Devices Society. The following circuits were demonstrated to the students present: NPN amplifier, AND-OR Gate, Battery Polarity Checker, Simple Water Alarm and Voice Controlled Rays. As the operating principles of the circuits were explained, students also became familiar with working of diodes and transistors. Almost 35 enthusiastic students participated in the workshop. The Chapter, in association with the Department of Electronics and Communication Engineering, also organized a one-day seminar on "*Security in SDF/NFV and 5G networks-Opportunities and Challenge*" on August 4, 2018. Prof. Ashutosh Dutta, Senior Wireless Communication Systems Research Scientist at Johns Hopkins University Applied Physics Labs (JHU/APL) presented his valuable lecture on the aforementioned topic.

EDS-ETC Workshop with students from class XII of National Gems Higher Secondary School

Prof. Dutta holds the respected positions of Director of Industry Outreach and IEEE 5G Initiative Co-chair apart from being an eminent Distinguished Lecturer of IEEE ComSoc. The lecture session commenced with a brief introduction to IEEE membership and its benefits for students and professionals, followed by the evolution of network technology from 1G to 4G and exposing the loopholes in these which could lead to security breaches. The second part of the talk primarily focused on the new opportunities and challenges in dealing with 5G technology. Almost 45 participants including students and faculty members showed up for the event along with the 13 members of the chapter.

A one day seminar was organized by the ED NSEC Student Branch Chapter in association with the Department of Electronics and Communication Engineering on May, 3rd. Prof. Abhijit Biswas of Institute of Radio Physics and Electronics under Calcutta University, presented his valuable lecture on "*Conventional MOSFETs and Emerging Hybrid CMOS devices*."

After introducing the operation of a conventional long channel MOSFET, a need for scaling was discussed paving the way for short channel MOSFETs. Various challenges of short channel devices were discussed,

Prof. Dutta and attendees of 5G technology lecture

including their possible solution approaches highlighting the concepts of channel material engineering (using GeSn as channel material) and Hybrid CMOS technologies. Almost 70 participants, including students and faculty members, showed up their interest along with the 15 members of this chapter.

Prof. Abhijit Biswas and attendees of lecture on MOSFETs

ED Delhi Chapter

—by R. S. Gupta and Sneha Kabra

The Department of Instrumentation, Shaheed Rajguru College of Applied Sciences for Women (University of Delhi), in collaboration with the ED Delhi Chapter, organized a talk on Emerging Semiconductor Devices and its applications by Dr. D. Nirmal, ED Coimbatore Chapter Chair and Associate Professor, Department of Electrical Sciences, Electronics and Communication Engineering, Karunya Institute of Technology and Sciences, in Coimbatore. The event was held on April 4th and attracted around 85 participants, including students, research scholars and faculty members. The talk described the types of Semiconductor Devices—High Power Devices, Low Power Devices and Optical Devices, and explained the latest material technologies which are used in the production of Semiconductor Materials, concept of Scaling of Semiconductor Devices, Dual Gate MOSFET, Fin-FET, Gate-All-Around MOSFET and Junctionless transistor.

IIT Delhi in collaboration with the ED Delhi Chapter organized a Distinguished Lecturer by Vikram L. Dalal, Anson Marston Distinguished Professor of Engineering, Iowa State University, United States, on April 11 2018 at IIT, Delhi. His talk, titled "*New Directions in Photovoltaic Science and Technology*," emphasized on new photovoltaic energy conversion technologies, ranging from

Dr. D. Nirmal with participants on Emerging Semiconductor Devices

organic and inorganic perovskites and other materials systems that can be used to increase the efficiency of Si-based systems to >30% from the present 20%.

ED Heritage Institute of Technology Student Branch Chapter

—by Atanu Kundu

In order to spark an interest among the undergraduate students for research in the domain of electron devices, the Department of Electronics and Communication Engineering in collaboration with the ED HIT Student Branch Chapter, organized a lecture session by IEEE EDS Distinguished Lecturer, Prof. Yogesh Singh Chauhan from Indian Institute of Technology, Kanpur. The lecture held on April 12, 2018, was titled "Negative Capacitance Transistors—Physics, Modeling and Processor Performance," and attracted 191 undergraduate student participants.

(left) Felicitation of the Speaker IEEE EDS DL Prof. Yogesh Singh Chauhan, by Branch Advisor Prof. Atanu Kundu; (right) audience of the DL session

ED Nepal Chapter, Kathmandu

—by Bhadra Prasad Pokharel

The ED Nepal Chapter organized an EDS Distinguished Lecture at Pulchowk Campus, Institute of Engineering, Tribhuvan University, Lalitpur on May 4th. Dr. Ajit Kumar Panda, National Institute of Science and Technology, Berhampur, Odisha, India, gave his presentation "*Beyond CMOS: HEMT is a Prospective Device*." Before the delivery of his talk Prof. Panda presented a slideshow on the Society. The talk was very interesting, containing both historical development and research of semiconductor devices. The EDS overview slides were of interest to those students who did not know about IEEE and EDS and made them curious. According to Prof. Panda, HEMT is considered to a potential device to use in high frequency communication circuit where CMOS has the limitation. He explained a self-consistent charge control model to solve Poisson's equation and Schrodinger's wave equation self consistently. Total participant in the program were 24, including 8 IEEE members and 16 students and faculty. The program was partially supported by the Materials Science and Engineering Program, Pulchowk Campus.

The chapter also organized an "*MSc thesis competition in Materials Science and Engineering Theme*." The selection committee comprised of Prof. Ajit Kumar Panda, NIST Orrissa, India; Prof. Pradeep Bhattarai: President, Nepal Physical Society; and Prof. Sitaram Prasad Byahut, EDS Nepal Chapter. On May 18th the competition prizes were given to the winners: Mr. Rameswor Poudel, GoldenGate Int'l College; Ms. Purnima Mulmi, Pulchowk Campus, IOE; Mr. Arjun Subedi, Central Department of Physics; Mr. Megh Raj Khadka and Mr. Ganesh Raj Bajgai.

~ Manoj Saxena, Editor

Selection committee and winners of MSc thesis competition

EDS MEETINGS CALENDAR

THE COMPLETE EDS CALENDAR CAN BE FOUND AT OUR WEB SITE: HTTP://EDS.IEEE.ORG. PLEASE VISIT.

2019 20th International Symposium on Quality Electronic Design (ISQED)	06 Mar - 07 Mar 2019	Santa Clara, CA USA
2019 Electron Devices Technology and Manufacturing Conference (EDTM)	12 Mar - 15 Mar 2019	Singapore, Singapore
2019 China Semiconductor Technology International Conference (CSTIC)	17 Mar – 18 Mar 2019	Shanghai, China
2019 IEEE International Reliability Physics Symposium (IRPS)	31 Mar - 4 April 2019	Monterey, California, USA
2019 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS)	01 April – 03 April 2019	Grenoble, France
2019 International Siberian Conference on Control and Communications (SIBCON)	18 April - 20 April 2019	Tomsk, Russia
2019 International Vacuum Electronics Conference (IVEC)	28 April - 1 May 2019	Busan, Korea (South)
2019 30th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC)	06 May - 09 May 2019	Saratoga Springs, NY USA
2019 IEEE 11th International Memory Workshop (IMW)	12 May - 15 May 2019	Monterey, California, USA

2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)	02 Jun – 04 Jun 2019	Boston, MA USA
2019 International Interconnect Technology Conference (IITC)	02 Jun – 06 Jun 2019	Brussels, Belgium
2019 Silicon Nanoelectronics Workshop (SNW)	09 Jun – 10 Jun 2019	Kyoto, Japan
2019 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)	12 Jun – 14 Jun 2019	Xi'an, China
2019 IEEE 46th Photovoltaic Specialists Conference (PVSC)	16 Jun - 21 Jun 2019	Chicago, Illinois
2019 20th International Conference on Solid-State Sensors, Actuators and Microsystems & Eurosensors XXXIII (TRANSDUCERS & EUROSENSORS XXXIII)	23 Jun - 27 Jun 2019	Berlin, Germany
2019 26th International Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD)	02 Jul - 05 Jun 2019	Kyoto, Japan
2019 IEEE BiCMOS and Compound semiconductor Integrated Circuits and Technology Symposium (BCICTS)	03 Nov – 06 Nov 2019	Nashville, TN USA
2019 IEEE International Electron Devices Meeting (IEDM)	09 Dec – 11 Dec 2019	San Francisco, CA
2019 IEEE 50th Semiconductor Interface Specialists Conference (SISC)	11 Dec – 14 Dec 2019	San Diego, CA

Message from Editor-in-Chief

Dear Readers,

I would like to warmly wish you a Happy New Year! In 2019, we will be celebrating the 25th year anniversary of renewed publishing of the EDS newsletter. Be on the lookout for our July Issue, which will be our 100th issue. I would like to thank all of the contributions from our authors for technical review articles, the Regional Editors from around the world who work to report on EDS activities and news, our chapters and members who submit articles, and the various people who make this newsletter successful. I would also like to thank Joyce Lomabardini at IEEE headquarters, who always puts in extra effort in completing all the tasks that are required to issue the newsletter on a quarterly basis. I hope you enjoy reading the newsletter as much as I did to learn about marvels within EDS both old and new in the technical briefs, learn about the Board of Governor's meeting and EDS news from around the world. We look forward to hearing from other readers in the future. If you have any feedback or suggestions for the newsletter, please send them to me at clilley@uic.edu.

Sincerely,
Carmen