IEEE
ELECTRON DEVICES SOCIETY
Newsletter

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EDS President's Message

Renuka P. Jindal
EDS President

On January 1 2010, I became the 22nd President of the Electron Devices Society. Being EDS President is a great honor and I want to take a few moments to share with you, the members of EDS, my vision for the Society and outline what we can together hope to achieve in the coming years.

First and foremost, **EDS serves its members**. The fundamental question we must ask ourselves before starting any new initiatives is, "what is the value of this effort to our members?" The mission statement we officially adopted at our December Administrative Committee (AdCom) Meeting embodies this "members first" philosophy: *To foster professional growth of its members by satisfying their needs for easy access to and exchange of technical information, publishing, education, and technical recognition and enhancing public visibility in the field of Electron Devices.*

This is an important point to remember because, although EDS clearly conducts business,

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2010 IEEE International Integrated Reliability Workshop (IIRW)

© Vance Fox Photography

The main lodge at the Stanford Sierra Conference Center. The center provides lodging, meals and meeting facilities as well as excellent recreation including hiking in the Desolation Wilderness and boating on Fallen Leaf Lake

The 2010 IEEE International Integrated Reliability Workshop (IIRW), sponsored by the IEEE Reliability Society and the IEEE Electron Devices Society, will be held at the Stanford Sierra Conference Center on the shore of Fallen Leaf Lake near South Lake Tahoe, California, October 17–21, 2010. This workshop provides a unique forum for open and frank discussions of all areas of reliability research and technology for present and future semiconductor applications.

Hot reliability topics include: transistor reliability including hot carriers and NBTI/PBTI, high-k and nitrided SiO_2 dielectrics, SiGe and strained Si, III-V, SOI, novel device reliability, organic electronics,

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Your Comments Solicited
Your comments are most welcome. Please write directly to the Editor-in-Chief of the Newsletter at ninoslav.stojadinovic@elfak.ni.ac.rs

ELECTRON DEVICES SOCIETY

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EDS AdCom
Elected Members-at-Large
Elected for a three-year term (maximum two terms) with 'full' voting privileges

2010	Term	2011	Term	2012	Term
J. N. Burghartz	(2)	G. Baccarani	(2)	R. Huang	(2)
M. J. Chan	(2)	M. J. Deen	(2)	S. S. Iyer	(1)
S. Ikeda	(2)	S. Deleonibus	(1)	M. Meyyappan	(1)
R. J. Nikolic	(2)	F. Guarin	(1)	H.S. Momose	(2)
T. L. Ren	(1)	S. Saha	(1)	A. Nathan	(1)
R. M. Todi	(1)	H. Shang	(2)	M. Shur	(1)
J. J. Welser	(2)	J. W. Swart	(2)	B. Zhao	(1)
		P. K. L. Yu	(1)		

NEWSLETTER EDITORIAL STAFF

CONTRIBUTIONS WELCOME

Readers are encouraged to submit news items concerning the Society and its members. Please send your ideas/articles directly to either the Editor-in-Chief or appropriate Editor. The e-mail addresses of these individuals are listed on this page. Whenever possible, e-mail is the preferred form of submission.

NEWSLETTER DEADLINES

Issue	Due Date
January	October 1st
April	January 1st
July	April 1st
October	July 1st

The EDS Newsletter archive can be found on the Society web site at https://www.ieee.org/portal/pages/society/eds/pubs/newsletters/newsletter.html. The archive contains issues from July 1994 to the present.

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EDS President's Message

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quite a lot of business, we are not a business. We serve our members by keeping a healthy bottom line. From a financial standpoint the good news is, serving our members first is in fact a prudent business model. This is evidenced by our strong financial performance in 2009, in which we posted healthy gains from both operations and investments…this despite the impact of the recent world economic situation.

Secondly, **EDS is a member-led, member driven society**. We are extremely fortunate to have a talented and committed corps of volunteer leaders to manage the affairs of the Society. From the executive team, to the Elected Members-At-Large, to those who chair and serve on our myriad committees, each of us relies on the dedication of the others to share their time, abilities, and energy to help make EDS all that it is today. It is a great privilege to serve as their President. Each and every volunteer will enjoy my full support as well as that of the EDS Executive Office and the EDS staff whose dedicated services make it all possible.

Moreover, we encourage anyone who wants to become involved to do so now! There are many such opportunities through our AdCom. The EDS AdCom is comprised of many standing and technical committees, each with a dedicated area of interest. The standing committees deal with functional areas of the society, such as publications, meetings and conferences, and educational outreach. The technical committees focus on specific areas of electron devices within EDS field of interest. EDS is your Society, so get involved today!

Think global, act global. For EDS to be a truly global society we must be prepared to meet wherever our members are. With over 10,000 members and nearly 150 chapters on six continents, that can be just about anywhere. Throughout the course of my tenure as President, I plan to visit and meet with as many of our members and volunteers as possible.

Looking Ahead. While my time as President will complete in less than two years, I realize that the work we undertake now will impact the Society long after my tenure as President is over. With all of the important new initiatives we are launching, this lasting impact is something I take very seriously. I hope that as you learn more about these efforts you will see that they not only embody the guiding principles outlined above, but will add value and benefit to EDS for years to come, encouraging you to get involved.

- **New Journal Dealing with Photovoltaics Devices.** Working closely with key volunteers from our Photovoltaics Technical Committee, and in conjunction with members of the planning committee for our Photovoltaics Specialists Conference (PVSC), I am very pleased to announce that we plan to launch the *IEEE EDS Journal of Photovoltaics* in 2011. For many years, the PVSC has enjoyed significant growth, paralleling the growth in photovoltaics in general. As such, the time is ripe to create a new publication, designed to be the premiere archival venue for documenting advances in the broad field of photovoltaics.
- The proposal development was led by Tim Anderson of the University of Florida and Steve Ringel, chair of EDS's Photovoltaic Devices technical committee. Tim and Steve worked closely with many key volunteers, including EDS Publications V-P Samar Saha, Chennupati Jagadish, Herb Bennett, and our President-Elect, Paul Yu. Also involved in the development of the proposal were Doug Verret and Yuan Taur, the Editors-in-Chief of our flagship publications, *Transactions on Electron Devices* (T-ED) and *Electron Device Letters* (EDL), respectively. Doug and Yuan's contributions were extremely important to helping ensure that we not only put forth a top notch proposal, but also that the new journal's scope fit within the framework of EDS existing family of publications. This is a very exciting effort for EDS and one that will surely be of great interest to all of the IEEE in the years ahead.
- **Changes to Our Existing Publications.** EDS has many reasons to be proud of its major publications. Over the years, going back to the 80's, by consistent attention to manuscript page length and other cost control measures, they have slowly emerged as financially robust. Now they are the largest line item on the EDS budget helping to support our various initiatives and member services. The "formula" for the success has been our ability to continually build on the good work of the past and never resting on our well-earned laurels. In keeping with this tradition, we will be launching several new initiatives in 2010 and 2011 to help ensure that our existing publications will continue to be successful in the years to come.

  We recently completed the migration of T-ED to IEEE Manuscript Central to help modernize the manuscript submission and editorial process for the publication. This is the long-awaited, next logical step in the computer based manuscript handling system that I developed back in 1990 as Editor-In-Chief of T-ED. With

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Upcoming Technical Meetings

2010 IEEE International SOI Conference

The premier conference dedicated to current trends in silicon-on-insulator technology will be held October 11–14th, 2010, at the Catamaran Resort & Spa located on Mission Bay in beautiful San Diego. The conference will be preceded by a one-day tutorial short course on Monday, October 11th and will also feature a half-day educational class focusing on the fundamentals of SOI technology.

The conference was established with the support of the IEEE Electron Devices Society to provide a forum for open discussion in all areas of silicon-on-insulator technologies and their applications. Ever increasing demand and advances in this technology make it essential to meet to discuss new gains and accomplishments, as well as to consider the new developments introduced in original papers presented at the conference.

Professor Chenming Hu from University of California Berkeley and NASA JPL Jupiter/Europa Mission Lead, Karla Clark, will open the 36th annual IEEE International SOI Conference. The plenary talks will be followed by two days of oral sessions, a poster session and a late news session. Two best paper awards will be presented; one for the best oral presentation and one for the best student paper presented at the conference.

Participants are free on Wednesday afternoon to indulge in the water sports offered on Mission Bay, explore the myriad delights of San Diego, get a little work done, or just plain relax. Alternatively, participants may choose additional education with the optional, intermediate-level class intended for individuals from a variety of fields including circuit design, material scientists/engineering, process technology, modeling,

Catamaran Resort in San Diego, California

and device design. This will be the fourth SOI fundamentals class offered by the conference and is meant to increase participant's understanding of the theory of carrier transport based on quantum mechanics for nanoscale si and beyond-si devices as well of SOI-based rf/analog design fundamentals including impact of both active and passive device characteristics on various design parameters and performance. An evening discussion panel where attendees are encouraged to share their opinions and expertise, will round off Wednesday evening.

The 2010 SOI Conference seeks previously unpublished papers on a wide range of SOI technology including:

- DEVICE PHYSICS and MODELING
- SUBSTRATE ENGINEERING (III-V advanced substrates, hybrid Si and III-V integration)
- NEW DEVICE / PHYSICS USING ADVANCED SUBSTRATES (III-V CMOS, hybrid SI and III-V)
- MANUFACTURABILITY and PROCESS INTEGRATION of SOI DEVICES
- LOW-POWER SOI TECHNOLOGY and CIRCUIT DESIGN INFRASTRUCTURE
- SOI CIRCUIT APPLICATIONS (high-performance MPU, SRAM, ASIC, high-voltage, RF, analog, mixed mode, etc.)
- SOI DOUBLE and MULTIPLE GATE/VERTICAL CHANNEL STRUCTURES; OTHER NOVEL SOI STRUCTURESNEW SOI STRUCTURES, CIRCUITS, and APPLICATIONS (displays, microactuators, novel memories, optics, etc.)
- SOI RELIABILIITY ISSUES (hot-carrier effects, radiation effects, high-temperature effects, etc.)
- MATERIAL SCIENCE / MODIFICATION, SOI CHARACTERIZATION, MANUFACTURE
- SOI SENSORs, MEMs, and RFIDs TECHNOLOGY and APPLICATIONS
- 3D INTEGRATION (imagers, power devices, wafer-to-wafer and die to wafer 3D integration)
- SILICON or SOI PHOTONICS

Abstracts for the 2010 SOI Conference should be submitted in PDF format, no later than May 14, 2010, to the conference manager, via e-mail only: soipapers@bacminc.com.

Late news papers with exceptional merit will be considered for the late news session if submitted on or before August 30, 2010.

Once again, the popular one-day tutorial short course will be offered preceding the conference. The course is intended to educate attendees in details about current trends and issues in the SOI industry. The 2010 tutorial short course is entitled "a comprehensive view of building integrated solutions using SOI" and will provide a comprehensive look at the essential aspects of technology, design, design tools and applications of SOI. Experts

from all these areas will give a detailed tutorial on wide range of topics such technology characteristics, advanced circuit design techniques and tools needed for full soc implementations. The short course will provide invaluable insight into all aspects of the growing list of current applications and also give a forward looking vision of how FDSOI will change the future of the semiconductor market.

For registration forms and additional information, please go to the conference web site www.soiconference.org, or contact the 2010 IEEE International SOI Conference at 578 Washington Blvd., #350, Marina Del Rey, CA, 90292, Tel: 310-305-7885; Fax: 310-305-1038; E-mail: bobbi@bacminc.com.

Mario Pelella
2010 SOI Publicity & Development Chair
Tau-Matrix, Inc.
Santa Clara, CA, USA

2010 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)

The 2010 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) will be held October 4–6, 2010, at the Radisson Hotel & Suite Austin-Town Lake. It includes a one day short course followed by two days of conference.

Anyone interested in leading edge processes, devices, and circuits used in state of the art telecommunication systems and power control systems will not want to miss this conference. Bipolar and BiCMOS technologies, particularly SiGe HBT BiCMOS technologies, continue to play a key role in these systems.

Papers covering the design, performance, fabrication, testing, modeling, and application of bipolar and BiCMOS integrated circuits, bipolar phenomena, and discrete bipolar devices will be presented.

© Radisson Hotel and Suites Austin

The Radisson Hotel and Suites Austin – Town Lake

Located in Central Texas on the eastern edge of the American Southwest, Austin is the fourth-largest city in Texas and the 15th-largest in the United States. It was the third-fastest-growing large city in the nation from 2000 to 2006. Residents of Austin are known as "Austinites" and include a diverse mix of university professors, students, politicians, musicians, state employees, high-tech workers, blue-collar workers, and white-collar workers. The main campus of the University of Texas is located in Austin. The city is home to development centers for many technology corporations and has adopted the nickname "Silicon Hills". Additionally, the city's official slogan promotes it as "The Live Music Capital of the World", a reference to the many musicians and live music venues within the area.

The conference starts with a one day short course followed by two full days of contributed and invited papers including keynote speaker and a special session on Emerging Technologies. On Tuesday evening, we will have our Gala Dinner, an annual highlight of the conference which offers attendees a great opportunity to catch up with old colleagues and make new friends.

The short course features three renowned experts on "Si/SiGe circuit design applications from GHz to THz". Short course invited talks include: "Designs and Applications in SiGe Technology", Peter Gammel (SiGe Semiconductors), "Development of 60 GHz Phased-array Systems and W-band Imaging Circuits in SiGe", Scott Reynolds (IBM), and "Design of Silicon Integrated THz Circuits", Ulrich Pfeiffer (University of Wuppertal).

We are fortunate to have Dr. Thomas Lee from Stanford University as this year's keynote speaker. Dr. Lee will discuss "The Fourth Age of Wireless: The Last and Best?" This is a great

opportunity to meet Dr. Lee and learn about the latest trends in advanced communication technologies.

Three leading experts from the electronics community will share their visions during the special Emerging Technologies session. The first speaker is Professor Frank Schwierz from Technische Universitat Ilmenau, who will present "Graphene Applications and with Special Focus on the Graphene Transistors." Our next speaker, Dr. Christian Person of Lab-STICC Laboratory/Telecom Bretagne, will give some insights on "Silicon Antenna." And our special session will be completed with "The Future of Medical Electronics" presented by Dr. Karthik Vansath, TI's Medical Business.

Two days of technical paper sessions, a luncheon with guest speaker Andrew Keys of NASA, and the evening banquet roll out the program. We look forward to welcoming you at BCTM 2010. Find full details and registration information for the conference on the BCTM web page (http://www.ieee-bctm.org/).

See you in Austin!

David Ngo
2010 BCTM General Chair
RFMD
Greensboro, NC, USA

The 2010 IEEE Compound Semiconductor IC Symposium (CSICS)

We cordially invite you to the 2010 IEEE Compound Semiconductor IC Symposium (CSICS) being held October 3–6, 2010, in beautiful Monterey, California. Over the last 32 years the Symposium has been and continues to be the preeminent international forum in which advances in semiconductor circuit and device technology are presented, debated, and discussed. The scope of the Symposium encompasses devices and circuits in GaAs, SiGe, InP, GaN, and InSb as well as RF/mm-wave and high-speed digital CMOS to provide a truly comprehensive conference. This is the ideal forum for presentation of the latest results in microwave/mm-wave, high-speed digital, analog, mixed mode, and optoelectronic integrated circuits.

The 2010 CSIC Symposium is comprised of a full 3-day technical program, 2 short courses, a primer course, and technology exhibition. The technical program consists of approximately 60 high quality state-of-the-art technical papers, 4 panel sessions, and an Industry Exhibit. The short courses, which run in parallel on Sunday, October 3, are titled "High Performance Linear Transceiver MMIC Design" and "High-Speed and mm-wave Digital-Rich Transceiver Design" and provide the attendees with a unique chance to learn from ten world-renowned instructors in their respective areas of expertise. The Symposium will also be offering the popular annual introductory level primer course on "Basics of Compound Semiconductor ICs." This year the Symposium will feature approximately 15 invited papers on a wide range of important topics encompassing device engineering to circuit application using advanced compound and other related semiconductor technologies. In addition, the Symposium will continue the tradition of including important "late breaking news" papers.

The technology exhibition will be held on Monday and Tuesday. The exhibition will feature informative and interesting displays with corporate representatives on hand. The list of exhibitors can be found in the CSICS advance program which will be published and distributed in late June.

To complement the Symposium, there are several social events which include the Sunday Evening CSICS Opening Reception, the Monday CSICS Exhibition Opening Reception, the CSICS Tuesday evening theme party, and the CSICS Exhibition Luncheon on Tuesday. Breakfast and coffee breaks will also be served on Monday, Tuesday, and Wednesday.

The Symposium will be held at the Portola Hotel located in downtown Monterey. Situated 115 miles south of San Francisco and 350 miles north of Los Angeles, Monterey features a stunning waterfront, a lush urban forest, a rich array of historic and cultural resources, museums, gardens, recreational activities and a

wide variety of special events scheduled throughout the year. Monterey is the home of the world-class Monterey Bay Aquarium located on the street immortalized in John Steinbeck's novel Cannery Row. Monterey's rich history includes Spanish exploration dating back to 1542, and the establishment of the San Carlos Cathedral by Father Junipero Serra in 1770. It was the site of Alta California's capital under Spain and later Mexico, and the place where California statehood began in 1849.

For registration and further information please visit the CSICS website at http://www.csics.org. Further questions may be addressed to the Symposium Chair: Dave Halchin, telephone +1 336 678-8123 or e-mail dhalchin@rfmd.com.

We hope you can attend.

Charles F. Campbell
2010 CSICS Publicity Chair
TriQuint Semiconductor
Richardson, TX, USA

Photos courtesy of the Monterey County Convention and Visitor's Bureau

2010 IEEE International Integrated Reliability Workshop

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emerging memory technologies and future "nano" technologies, Cu interconnects and low-k dielectrics, product reliability and burn-in, impact of transistor degradation on circuit reliability, reliability modeling and simulation, optoelectronics, single event upsets, NEMS/MEMS, and photovoltaics. The complete Call for Papers can be found at www.iirw.org. Please submit abstracts to the Technical Program Chair, Rolf Geilenkeuser, Global Foundries (rolf.geilenkeuser@globalfoundries.com) until the submission deadline of July 17, 2010.

The IIRW is quite a bit different from a typical technical conference. From the moment you arrive, you realize that you are taking part in something special. Located 6000ft high in the Sierra Nevada Mountains, the Stanford Sierra Conference Center provides an ideal atmosphere for a relaxing yet informative workshop. All aspects of the workshop, including the physical isolation of the location, the absence of distractions such as in room phones and television sets, and the format of the technical program encourage extensive interaction among the workshop attendees. You feel yourself drawn into technical discussions from the start.

Nestled throughout the pines and cedars along the shoreline of Fallen Leaf Lake, attendees stay in cabins furnished in the rustic style of an alpine resort. All rooms have decks with magnificent views of Fallen Leaf Lake and the surrounding Sierra peaks. Comfortable, informal dress is encouraged, affiliations are downplayed, and meals are provided family-style in the lodge dining room. This peaceful setting, free from the distractions of modern life, presents a terrific opportunity to get to know your colleagues, including internationally renowned experts. This is an opportunity not usually available at larger, more hectic conferences. Instead of watching TV, participants spend their evenings at informal poster sessions, discussion groups, and special interest groups, all with refreshments and snacks provided

to stimulate discussions. At the end of the day, attendees are free to relax in front of a roaring fireplace in the rustic Old Lodge.

One advantage of the IIRW is the moderated **Discussion Groups** that are held in the evenings, organized this year by Ricki Southwick, Boise State University. Following up on the Discussion Groups are the **Special Interest Groups**, which are composed of small groups of attendees who want to continue their discussions on a particular topic of interest which often continues even after leaving the workshop.

Yet another advantage of attending the IIRW is the extensive collection of **Tutorials**, presented by leading experts and included at no additional cost. This year the tutorials are jointly organized by Tibor Grasser, TU Wien and Jim Lloyd, SUNY Albany and cover diverse reliability issues related to NBTI, Electromigration, Reliability and variability of FinFETs, soft errors and irradiation, reliability of III-V semiconductors, hot carriers, and the implications of TDDB for high-k. Check the IIRW website for updates on tutorial presenters.

One unique aspect of the workshop is the opportunity for any attendee to present a walk-in poster of their latest work. No matter how far along your research is, your ideas will be accommodated. This is a great way to share that new project you are working on and to get world-class feedback.

Finally, attendees have Wednesday afternoon off to enjoy a variety of outdoor activities such as hiking, volleyball, sailing or kayaking, biking, walking, or simply continuing that intriguing conversation from the night before. This free afternoon is a great way to not only network, but also to build long-lasting friendships.

Additional information about the workshop is available on the IIRW website at www.iirw.org, or by contacting Chadwin Young of SEMATECH, 2010 IIRW General Chair, (chadwin.young@sematech.org). Note: If you want to take part in this event, please register early as space at the Stanford Sierra Conference Center is limited to roughly 120 attendees and the workshop has sold out in the past.

On behalf of the 2010 IIRW Committee, I look forward to meeting you in Lake Tahoe!

Jason T. Ryan
2010 IIRW Communications Chair
NIST
Gaithersburg, MD, USA

EDS President's Message

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this migration complete, all of EDS publications are now on the Manuscript Central system. The migration was completed without issue and in fact we have already seen a significant increase in the number of manuscripts submitted. That is great news for EDS, and a welcome challenge for the T-ED Editorial Board!

We will also be taking steps to help improve the turnaround time of EDL, which already enjoys one of the fastest "sub-to-pub" times in all of the IEEE family. We are working with the IEEE's editorial and publications groups to institute a new section of EDL called *Electron Device Express* (EDX). This new feature in EDL will offer authors an express publication option for short research articles reporting on cutting-edge results critical to industry's development of advanced integration processes for electron devices.

To foster continuous quality enhancement of our publication process, we recently instituted an author feedback module on Manuscript Central. The first statistics extracted are very gratifying. The survey tracks responses on a scale of 1–5 (poor to very good), with 5 being the highest. The response rate was extremely high, with nearly 30% of 1400+ authors voluntarily completing the survey. Of those who responded, 94% rated their overall experience 4 or 5. When asked how they would rate the likelihood of submitting again, 95% responded 4 or 5. The overall average for all questions answered was 4.3. These are extremely encouraging statistics although we need to involve the rest of the 70% in the feedback process.

- **Member Recognition.** Our members do important work, impacting nearly every facet of life around the world. Recognizing the accomplishments of EDS members is a vital part of why we choose to be a part of the Society. Being a financially healthy society, we give out more than $35,000.00 in awards every year. As President, I will work with our Executive Committee to increase the engagement in and prestige of our many awards and fellowships for our student, Graduate Of The Last Decade (GOLD) and regular members.

  One such example of this initiative is the EDS Celebrated Member effort which we will institute this June at the PVSC conference in Hawaii. George

Smith, along with past fellow EDS members Willard Boyle and Charles Kao, is the co-winner of 2009 Nobel Prize for Physics. He is also the founding editor of EDL, and we are honored that he will be joining us at the PVSC. George will become the inaugural Celebrated EDS Member.

As fellow members of the Electron Devices Society, each of us can take pride in the accomplishments of Kao and Boyle and Smith. We should draw from them inspiration to advance our field because it is not only their work, but ours as well, that can help transform the world around us. This is a great testimony to EDS recently adopted vision of "Promoting excellence in the field of electron devices for the benefit of humanity." We salute Bill, Charlie and George for their contributions.

- **New EDS Web Site.** Working with President-Elect, Paul Yu and other key members of our Executive Committee, Chris Jannuzzi, our new Executive Director, has begun a project to completely redesign the EDS web site. The aim here is to provide more benefits to our members through enhanced "members-only" features, more content, and to create an effective communication hub for EDS news and upcoming events. In addition, we will install a new content management system which will afford us great autonomy and flexibility in terms of updating the site on an as-needed basis. The project is in nascent stages, so look for more information and opportunities to get involved as the project gets rolling this year.
- **Committee Appointments.** EDS has a host of standing and technical committees that are important venues for members to become more engaged in the working of the Society. These committees are a wonderful opportunity for EDS members to meet colleagues with similar interests and build the types of personal and professional networks that are the lifeblood of our individual careers and the industry as a whole. The focal point of my presidency will be to increase volunteer involvement in the work of the committees, and to help foster the development of the next generation of EDS leaders.
- **Chapter Activities.** Thanks to the efforts of our volunteer leaders and efficient and enthusiastic staff, EDS now has 150 chapters around the world. Keeping this family close-knit and vibrant provides significant opportunities. The key stakeholders in this are our SRC Chairs, Vice-Chairs, Chapter Partners, Chapter Chairs and their executive teams. Using the new EDS web portal under construction, we plan to pull all EDS chapters into a seamless global entity comprising EDS. My vision is that with a few clicks of the button, our new website will bring the EDS world to your door step. This will take a redefinition and re-affirmation of the roles and responsibilities of all stakeholders which I hope to report to you next time.
- **Education and Training.** An important part of our member benefit package is education and training. This year we plan to invest approximately $45,000 to support our Distinguished Lecturer and Mini-colloquia programs as a reach out to our members worldwide. We plan to aggressively create new opportunities as well. An example of this is the newly released 2008 IEDM short course on 22 nm CMOS technology. This is about to hit the stands and will be made available to you, our members, at an affordable price of $29.99. To encourage our student members to invest in their future, we will make it available to them at a give-away price of $9.99 US dollars. Please visit www.ieee.com and click on the "shop" link to order your copy. Depending on response, we plan to extend this DVD library feature to short courses offered at other EDS conferences. To serve our members better, work is also on the drawing board to look for training opportunities by partnering with other professional organizations around the globe. Any ideas you have are welcome.

In closing, let me again thank you for the opportunity to serve as President of the Electron Devices Society. I started as a student member of EDS. From the, I became an author, a reviewer, an editor, the Editor-in-Chief of T-ED, and eventually the Vice-President of Publications. All told, EDS has been my professional home for 34 years… and counting. Becoming President of this outstanding organization is a great honor and responsibility, one that I do not take lightly. Over these years I have developed a deep sense of loyalty to the Society and hope that I can ignite this flame in each one of you. I know I speak for all EDS volunteer leaders when I say that we will devote the time and energy needed to raise the Society to the next higher level of performance in serving its global membership leveraging technology to the fullest extent.

Renuka P. Jindal
EDS President
University of Louisiana at Lafayette
Lafayette, LA, USA

Society News

Summary of Changes to the EDS Constitution and Bylaws

On December 6, 2009, the EDS Administrative Committee (AdCom) approved changes to the EDS Constitution and Bylaws. These amendments were then approved in January 2010 by the Chair of the IEEE Technical Activities Board (TAB) and later at the IEEE Technical Activities Board Meeting in February 2010. The changes will take effect 30 days following their publication in this issue of the Newsletter (distributed to all EDS members), unless objections are received from at least 5% of the EDS membership. The following is a summary of the changes:

Officer and Member-at-Large Election

- To require any Officer or Elected Member-at-Large to have previously served as an AdCom Member for at least one year
- To change the terms of the Secretary and Treasurer positions from a one-year term to a two-year term

The complete EDS Constitution and Bylaws may be obtained from the EDS Executive Office or on the Society website at www.ieee.org/eds/ (click on Administrative Committee).

Renuka P. Jindal
EDS President
University of Louisiana at Lafayette
Lafayette, LA, USA

Announcement of Newly Elected AdCom Members

Cor L. Claeys
EDS Chair of Nominations & Elections

On December 6, 2009, The Eds AdCom held its annual election of officers and members-at-large. The following are the results of the election and brief biographies of the individuals elected.

I. Officers

The following individuals were elected as officers beginning 1/1/2010:

Renuka P. Jindal (President) received his Ph.D. degree in Electrical Engineering from the University of Minnesota in 1981. Upon graduation, he joined Bell Laboratories at Murray Hill, New Jersey. In fall 2002, Dr. Jindal accepted the position as Board of Regents Eminent Scholar Endowed Chair at the University of Louisiana, Lafayette. In 1991, he was elected a Fellow of the IEEE. From 1990 to 2000 he served as Editor-in-Chief of the *IEEE Transactions on Electron Devices*. In December 2000, he received the IEEE 3rd Millennium Medal. From 2000 to 2008, he was EDS Vice-President of Publications. He served as President-Elect from 2008 to 2009. Beginning in January 2010, Dr. Jindal is now the President of the IEEE Electron Devices Society.

Paul Yu (President-Elect) received a Ph.D. in applied physics from Caltech, Pasadena, California in 1983. Since then, he has been a faculty at the ECE Department at the University of California, San Diego, where he is currently the Associate Vice Chancellor for Research Initiatives. His research work is mainly in the area of opto-electronic semiconductor devices for digital and analog communication and signal processing. He has authored and co-authored more than 130 journal papers and several book chapters. He is presently the President-Elect and an AdCom member of the IEEE Electron Devices Society, as well as a Fellow of the IEEE.

Stephen A. Parke (Treasurer) Dr. Parke received the AA degree from Olivet Nazarene University in 1980 and in 1984 the BS and MS degrees in electrical engineering from Purdue University. In 1984, he joined the IBM Microelectronics Division in Essex Junction, Vermont, where he worked

in advanced DRAM process and silicon device design on IBM's 4 MB, 16 Mb, and 64 Mb DRAM designs. In 1989, he was awarded an IBM Ph.D. Fellowship, and joined the UC Berkeley Device Research group. In 1993, he received the Ph.D. and joined the IBM Semiconductor R&D Center in Fishkill, New York where he worked in the Triad 256 Mb DRAM process development alliance between IBM, Toshiba, and Infineon. In 1996, he joined the Electrical Engineering faculty of Boise State University at the inception of its new College of Engineering. He helped lead the development of the ECE Department at BSU over its first ten years. Dr. Parke also founded and directed the Idaho Microfabrication Lab at BSU. In 2006, Dr. Parke joined Tennessee Tech University as ECE Professor and Chair. Dr. Parke's research is in the areas of double-gated nanoscale SOI transistors, Ultra-Low-Power and non-volatile memories. He holds twelve US patents and has published and/or presented 40 papers. He is also active in the IEEE Electron Devices Society, currently serving as the Treasurer. He received the IEEE Millennium Medal in 2000 for his service.

James L. Merz (Secretary) Dr. Merz received the B.S. degree in Physics from the University of Notre Dame in 1959, and attended the University of Göttingen, Germany, 1959–60. He received his M.A. degree in 1961 and Ph.D. in Applied Physics in 1967 from Harvard. He joined Bell Laboratories in 1966, and in 1978 moved to UCSB as a Professor of Electrical Engineering. He was appointed Department Chair in 1982, Associate Dean for Research for Engineering from 1984 to 1986, and Associate Vice Chancellor from January to September, 1988. He was Director of the Center for Quantized Electronic Structures (QUEST), a NSF Science and Technology Center, from 1989 until he moved to Notre Dame in 1994, where he served as VP for Graduate Studies and Research from 1996 to 2001. He also served as Interim Dean of Engineering, July 2006 to January 2008.

Dr. Merz was awarded an Honorary Doctorate by Linköping University, Sweden, in 1993. He is a Fellow of the APS, IEEE, MRS, and AAAS. He was awarded the IEEE Third Millennium Medal in 2000, and received an Alexander von Humboldt Award to carry out research in Germany in 2002. He served for five years as Secretary of the Electron Devices Society of the IEEE and a member of its Executive Committee, and resumed that duty in December 2007. He is currently a member of the Board of Directors of the Tyndall National Institute in Cork, Ireland.

II. Adcom Members-At-Large

A total of seven persons were elected to three-year terms (2010–2012) as members-at-large of the EDS AdCom. Two of the seven individuals were re-elected for a second term, while the other five were first-time electees. The backgrounds of the electees span a wide range of professional and technical interests.

A. Second Term Electees

Ru Huang is currently a Professor and Head of Department of Microelectronics, Peking University, China. Her research interests focus on nano-scaled devices, new nonvolatile memory devices, devices for harsh environment applications and device characterization technology. She holds 21 granted patents, and has authored/co-authored 4 books, over 190 papers, including IEDM, VLSI, EDL and T-ED papers and many conference invited papers.

She serves as an editor of *"IEEE Transactions on Electron Devices"* and the associate chief editor of "*Science in China"*. She was the Technical Program Committee Co-Chair of ICSICT 2004 and ICSICT 2008, and committee members of many other conferences and symposia.

Hisayo Momose joined Toshiba Corporation, Japan, in 1984, where she was engaged in the research and development of CMOS/Bi-CMOS LSIs and small geometry devices, including oxynitride MOSFETs, Ni salicide MOSFETs, ultra-thin gate oxide MOSFETs and analog CMOS devices. She is currently engaged in the research and development of CMOS imaging devices. She has authored or co-authored more than 100 papers published in technical journals or presented at international conferences.

Dr. Momose is an IEEE Fellow and an EDS Elected AdCom Member. Since 2005, she has served as an Editor of the *Transactions on Electron Devices* and the *Microelectronics Reliability*.

B. First-Time Electees

Subramanian S. Iyer is Distinguished Engineer and Chief Technologist at the IBM-SRDC, and is responsible for technology development strategy, embedded memory and 3 Dimensional Integration. He joined the IBM T. J. Watson Research Center in 1981 and founded SiBond LLC to manufacture SOI. He has been with the IBM Systems and Technology Group since 1997. He has received awards for the development of the Salicide process, the first SiGe HBT, eDRAM and eFUSE technology.

He holds over 40 patents and is an IBM Master Inventor. He received the Distinguished Aluminus award from IIT, Bombay.

Meyya Meyyappan is Chief Scientist for Exploration Technology at NASA Ames Research Center in Moffett Field, California. Until June 2006, he served as the Director of their Center for Nanotechnology. He has authored 190 articles in peer-reviewed journals and made over 200 Invited/Keynote/Plenary talks. His research interests include carbon nanotubes and inorganic nanowires, and applications in chemical and biosensors, instrumentation, electronics and optoelectronics.

Dr. Meyyappan is a Fellow of IEEE, ECS, AVS, and MRS. He is currently an EDS Distinguished Lecturer and Vice-President for Educational Activities. For his contributions and leadership in nanotechnology, he has received: a Presidential Meritorious Award; NASA's Outstanding Leadership Medal; Arthur Flemming Award by the Arthur Flemming Foundation; IEEE Judith Resnick Award; IEEE-USA Harry Diamond Award; AIChE Nanoscale Science and Engineering Forum Award. For his sustained contributions to nanotechnology, he was inducted into the Silicon Valley Engineering Council Hall of Fame in February 2009. For his educational contributions, he has received: Outstanding Recognition Award from NASA; Engineer of the Year Award (2004) by AIAA; IEEE-EDS Education Award; and the IEEE-EAB Meritorious Achievement Award in Continuing Education.

Arokia Nathan holds the Sumitomo/STS Chair of Nanotechnology at the London Centre for Nanotechnology, University College London. He is also the CTO of Ignis Innovation Inc., Waterloo, Canada, a company he founded to commercialize technology on thin film silicon backplanes on rigid and flexible substrates. He has held Visiting Professor appointments at the Physical Electronics Laboratory, ETH Zürich and the Engineering Department, University of Cambridge, UK. He received his Ph.D. in Electrical Engineering from the University of Alberta. He held the DALSA/NSERC Industrial Research Chair, was a recipient of the 2001 Natural Sciences and Engineering Research Council E.W.R. Steacie Fellowship, and was awarded the Canada Research Chair. He has published extensively in the field of sensor technology and CAD, and thin film transistor electronics, and has over 45 patents filed/awarded. He is a co-author of two books, Microtransducer CAD and CCD Image Sensors in Deep-Ultraviolet, and serves on technical committees and editorial boards of professional societies at various capacities. He is a Fellow of the IET (UK) and IEEE.

Michael Shur received MSEE degree (with honors) from LETI (St. Petersburg), Ph.D. and Dr. Sc. degrees from Ioffe Institute. He is Patricia W. and C. Sheldon Roberts Professor, Acting Director of Center for Integrated Electronics and Director of the NSF I/UCRC at RPI. He is also co-founder and Vice-President of Sensor Electronic Technology, Inc. His area of expertise is physics of semiconductor devices. Dr. Shur is Foreign Member of the Lithuanian Academy of Sciences and Fellow of IEEE, APS, IET, ECS, MRS, and AAAS. He received IEEE and other awards and holds Honorary Doctorate from St. Petersburg Technical State University.

Bin Zhao received the BSEE degree from Tsinghua University, Beijing, China and the Ph.D. degree from California Institute of Technology. He has been with SEMATECH, Rockwell International, Conexant Systems, Skyworks Solutions, and Freescale Semiconductor. His past work and experience have been involved with both VLSI technology development and analog/mixed-signal/RF IC design. Currently he is the Director of Southern California Development Center, Freescale Semiconductor, Irvine, California, where he leads IC design and product development for consumer electronics and mobile communications. He is an IEEE Distinguished Lecturer and the IEEE EDS Vice-President of Meetings. He is a recipient of the ECE Reader Award (2008), the Hearst Semiconductor Applications Award (2008), and the EDN Innovation Award (2009).

Cor L. Claeys
EDS Chair of Nominations and Elections
IMEC
Leuven, Belgium

Call for Nominations – EDS AdCom Members-at-Large

Cor L. Claeys
EDS Chair of Nominations & Elections

The Electron Devices Society of the IEEE invites the submission of nominations for election to its Administrative Committee (AdCom). Presently, the AdCom meets twice per year and is composed of 22 members. Seven members will be elected this year for a term of three years, and a maximum of two consecutive terms is allowed. In 2010, the election will be held after the AdCom meeting on Sunday, 5 December. Electees begin their term in office on 1 January 2011. For your information, the nominees do not need to attend the AdCom Meeting/Election to run.

Nominees are being sought to fill the slate of candidates. Nominees may be self-nominated, or may be nominated by another person; in the latter case, the nominee must have been contacted and have agreed to serve if elected. Any member of EDS in good standing that has previously served for at least one year as an EDS AdCom Member (Standing and Technical Committee VPs and Members, Publication Editors & Representatives) is eligible to be nominated. *The nominees do not need to attend the AdCom Meeting/Election to run. On the other hand, if elected, the nominees are expected to attend the two AdCom meetings a year. While the December meeting is organized in connection with the IEEE International Electron Devices Meeting, the Spring meeting is frequently held outside the US. In general, the travel and accommodation costs to attend these meetings are borne by the elected member*.

All nominees must be endorsed by one 'full' voting member, i.e., one of the four officers (President, President-Elect, Treasurer or Secretary), the Jr. or Sr. Past President or one of the 22 current AdCom Members-at-Large.

Please send your nominee's name, address, endorsement letter and supporting information to the EDS Executive Office Sr. Administrator, Laura J. Riello, IEEE, 445 Hoes Lane, Piscataway, NJ 08854, Fax: 732-235-1626, E-mail: l.riello@ieee.org, in time to be received by the deadline of **15 October 2010**. It is very desirable that submissions include a biographical summary in a standard two-page format. The EDS Executive Office can provide you with an example of the format. If you have any questions regarding the nomination requirements or process, feel free to contact Laura Riello (l.riello@ieee.org).

Cor L. Claeys
EDS Chair of Nominations & Elections
IMEC
Leuven, Belgium

EDS Administrative Committee Election Process

The Members-at-Large (MAL) of the EDS AdCom are elected for staggered three-year terms, with a maximum of two consecutive terms. The 1993 Constitution and Bylaws changes mandated increasing the number of elected MAL from 18 to 22, and required that there be at least two members from both IEEE Region 8 (Europe, Middle East & Africa) and Region 10 (Asia & Pacific). In 2003, EDS made changes to its Constitution and Bylaws to require that at least one elected AdCom member is a Graduate of the Last Decade (GOLD member). A GOLD member is defined by IEEE as a member who graduated with his/her first professional degree within the last ten years. It is also required that there be at least 1.5 candidates for each opening. In 2010, seven positions will be filled.

Each nominee needs to be endorsed by a 'full' voting member, i.e., one of the four officers (President, President-Elect, Treasurer or Secretary), the Jr. or Sr. Past President or one of the 22 current AdCom Members-at-Large. The endorser needs to submit an email to Laura Riello (l.riello@ieee.org) stating that they would like to endorse the candidate.

Effective with the 2010 election, the EDS AdCom approved a change to now require that each nominee must have previously served for at least one year as an EDS AdCom Member (Standing and Technical Committee VPs and Members, Publication Editors & Representatives).

The election procedure begins with the announcement and Call For Nominations in the *EDS Newsletter*. The slate of nominees is developed by the EDS Nominations Committee and includes the non-Committee and self-nominations received. Nominees are asked to submit a two-page biographical resume in a standard format.

Nominations are closed on 15 October, and the biographical resumes and endorsement letters are distributed to the 'full' voting members of AdCom prior to the December AdCom meeting. The election is then held after the conclusion of the meeting. *The nominees do not need to attend the AdCom Meeting/Election to run. On the other hand, if elected, the nominees are expected to attend the two AdCom meetings a year. While the December meeting is organized in connection with the IEEE International Electron Devices Meeting, the Spring meeting is frequently held outside the US. In general, the travel and accommodation costs to attend these meetings are borne by the elected member.*

A continuing flow of new AdCom members who are interested in working for the improvement of the Society and its related technical areas is essential for the continued development of EDS and the field of electron devices. Those interested in the field, the Society, and its operations are encouraged to attend AdCom meetings, become involved in Society activities, and consider running for election to AdCom.

Cor L. Claeys
EDS Chair of Nominations & Elections
IMEC
Leuven, Belgium

EDS Compound Semiconductor Devices and Circuits Technical Committee

Giovanni Ghione
EDS CSDC
Committee Chair

The EDS Compound Semiconductor Devices and Circuits Committee Chair for 2010 is Prof. Giovanni Ghione (Fellow, IEEE), from Politecnico di Torino, Torino, Italy, where he is a Full Professor in Electronics since 1992. Prof. Ghione's research field is in the modeling and design of active and passive components for RF, microwave and millimeter wave integrated circuits, mainly on compound semiconductors, also including widegap materials such as GaN, SiC and diamond. Research also included the physics-based numerical noise modelling of microwave active components in small- and large-signal regime and the modeling of high-speed optoelectronic devices (mainly detectors and electrooptic and electroabsorption modulators). Prof. Ghione has authored or co-authored more than 200 research papers on the above subjects and five books. He was a member of the QPC subcommittee of the IEDM in 1997–1998 and 2006–2007, as well as serving as the Chair in 2008; he currently is the EU Arrangement Chair of the IEDM. He was also the Chair for the 2003 GAAS conference and a subcommittee chair on several SCs of the European Microwave Week beginning in the year 2000. Since 2007, he is the Head of the Department of Electronics, Politecnico di Torino.

Research on compound semiconductor devices and circuits continues to be a very active and exciting field. Besides steady progress in the traditional domain of high-frequency devices, where novel structures have been recently demonstrated (such as InGaAs FinFETs by Purdue, see Y.Q. Wu et al., IEDM Tech. Dig., 2009, pp. 323–326), significant advances have been achieved in the development of Ge or InGaAs channel MOSFET as the potential successor to Si MOSFET. Using an In_{0.7} Ga_{0.3}As quantum-well FET and high-k gate dielectric technology, excellent sub-threshold swing close to Si MOSFET was reported by Intel at 75 nm gate length. Besides, high drive current was reached even at a small voltage of 0.5 V; such a low voltage operation can significantly reduce the chip power consumption beyond the one obtained using strained Si. Key challenges remain (but not limited to) in the Fermi-level depinned dielectric-semiconductor interface, and in a true scalability (not only concerning the gate length) of III-V MOSFETs.

Wide-bandgap semiconductor electronics shows continuous progress, with the development of AlGaN/GaN HEMT-based RF/microwave power amplifiers and robust low-noise receivers in a steady upward trend. Research on devices continues with the extension of AlGaN/GaN HEMTs (mainly on SiC substrates) to millimeter wave frequencies and the introduction of InGaN/GaN HEMTs and AlGaN/GaN MISFETs for microwave power applications.

However, wide-bandgap semiconductors such as SiC and GaN also offer outstanding properties for power conversion devices, high breakdown fields, high carrier saturation velocities, thermal stability, and high thermal conductivity. New excitement comes from the exploitation of GaN and SiC electronics in power and energy management (in connection with the increasing global demand for high-efficiency green energy technologies) to enable ultra-high-efficiency power electronics modules that minimise energy losses and that are capable of

operating at high-temperatures. Both GaN and SiC are viable semiconductor technologies for high-efficiency, high power and high-speed switching applications, with SiC having the added advantage of SiO_2 as a reliable native gate dielectric that enables the realisation of SiC-based metal-oxide-semiconductor field-effect transistors (MOSFETs) that are technologically similar to their Si-based counterparts. Efficient Power Conversion (EPC) has recently announced GaN power transistors based on Si substrates that are claimed to provide significant performance advances, see http://compoundsemiconductor.net/csc/features-details.php?cat=features&id=19658920.

The 2010 EDS Compound Semiconductor Devices and Circuits Technical Committee members are: G. Ghione (Chair, Politecnico di Torino, Italy), S. Bandyopadhyay (Virginia Commonwealth University), K. Chen (Hong Kong Univ. Of Science and Technology), A. Chin (National Chiao Tung University, Taiwan), S. A. Dayeh (Los Alamos National Laboratory), L. Faraone (University of Western Australia), G. Meneghesso (University of Padova, Italy), F. Ren (University of Florida) and M. Schlechtweg (Fraunhofer Institute, Freiburg, Germany).

Among future activities, the Committee would like to actively propose special issues in EDS periodicals focused on the most recent developments in the area.

Giovanni Ghione
EDS CSDC Technical Committee Chair
Politecnico di Torino
Torino, Italy

Message from the EDS Newsletter Editor-in-Chief

Ninoslav D. Stojadinovic
EDS Newsletter Editor-in-Chief

I am writing this message after a lapse of more than a year. It is sometimes astonishing to see how quickly time goes by. As professionals, all of us are very busy in our work. I hope that this issue comes at a very prosperous time in your career.

I would like to take this opportunity to thank two outgoing Regional Editors for outstanding service to the Newsletter and Electron Devices community. They are Cora Salm (Region 8 – Western Europe) and Xing Zhou (Region 10 – Australia, New Zealand & South Asia). Their outstanding voluntary contributions for the past six years, as regional editors, are exemplary to the rest of us.

Replacing Cora and Xing on the Newsletter Editorial Staff is Jan Vobecky and M.K. Radhakrishnan, whose biographies follow. It is my pleasure to welcome them as new editors for the *EDS Newsletter*.

Jan Vobecký (M'91, SM'00) received the Electrical Engineer (MSc.) in Electrotechnology and the Ph.D. degree in Microelectronics from Czech Technical University in Prague, Faculty of Electrical Engineering, Czechoslovakia, in 1981, 1988, respectively. He has been working mainly in the field of simulation and characterization of high-power devices including the control of carrier lifetime and defect engineering. In 1992, 1999, 2000, he received Associated Professor, Doctor of Science (DrSc.) and Full Professor degrees, respectively. From 1995–2006 he was the project manager of numerous University R&D projects with industrial partners (Motorola, Freescale, ABB, ON-Semiconductor, etc.). Since 2007, he is with ABB Switzerland Ltd. Semiconductors, Lenzburg, where he is engaged in the development of technologies for next generation Bipolar and Bi-MOS devices.

From 1996–1999, Dr. Vobecký was the committee member of the MTT/AP/ED CzechoSlovakia (CS) Chapter, representing EDS. In 2002–2003 and 2004–2005 he served as the IEEE CS Section Chair and Vice-Chair, respectively. Since 2007, he has served as one of the three Vice-Chairs of the EDS Subcommittee for Regions and Chapters (SRC) in Region 8 as well as the Chapter Partner of CAS/ED Switzerland, ED Central & South Italy, AP/ED/MTT Northern Italy and ED/SSC Croatia.

He regularly serves as a reviewer of several international journals, including *IEEE Transactions on Electron Devices, IEEE Electron Device Letters, IEEE Transactions on Power Electronics, Microelectronics Reliability, Microelectronics Journal, Japanese Journal of Applied Physics*, etc.

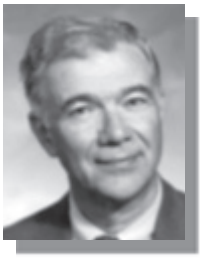
M.K. Radhakrishnan (M-81, SM-94) received his Ph.D. in semiconductor physics from the University of Cochin, India in 1981. Currently he manages *NanoRel – Technical consultants,* a technical consultancy firm he founed in Singapore which serves the microelectronics industries as well as higher education institutions. As a

professional in the microelectronics area for the last 30 years, Dr. Radhakrishnan has worked with many organizations including ST Microelectronics, Philips, ISRO, Institute of Microelectronics and the National University of Singapore at various senior positions. He was the Chairman of the IEEE international conference IPFA in 1999 and the General Chair of IEEE IEDST 2009, as well as serving as the Chapter Chair for the IEEE Rel/CPMT/ED Singapore Chapter in 2000–01. He is an IEEE EDS Distinguished Lecturer and serves as a IEEE EDS Regions/Chapters committee member and a member of the IEEE IPFA Board. Radhakrishnan serves as an Editorial Advisory Board Member for the *Microelectronics Reliability Journal*, the Editor of *Journal of Semiconductor* Technology and Science (JSTS) and Guest Editor to *IEEE TDMR*. His research interests are in device failure analysis, gate dielectrics and ESD, with more than 60 research publications. He is a Fellow of IETE, a Member of the ESD Association and a Member of EDFAS.

Once again, I thank the outgoing editors for their dedicated service to the Newsletter and welcome the new editors and wish them success. Please contact your respective Regional Editor directly with news items. A listing of EDS Regional Newsletter Editors is available on page two of this publication.

Ninoslav D. Stojadinovic
EDS Newsletter Editor-in-Chief
University of Nis
Nis, Serbia

EDS Members Named Recipients of 2010 IEEE Technical Field Awards



Alfred U. Mac Rae
EDS Vice-President
of Awards

Three EDS Members were among the recipients of the 2010 IEEE Technical Field Awards. They are:

Bijan Davari of IBM Corporation, Yorktown Heights, New York, USA, has been named the recipient of the 2010 IEEE Andrew S. Grove Award. His citation states, "For contributions to high performance deep-submicron CMOS technology."

Bijan Davari's pioneering work in miniaturization of semiconductor devices changed the world of computing. Dr. Davari's efforts during the mid 1980's led to the first generation of high-performance, low-voltage deep-submicron complementary metal-oxide semiconductor (CMOS) technology that enabled higher-speed computers and the portable computers and battery-powered handheld electronics we know today. His accomplishments displaced bipolar technology in IBM mainframes and enabled new high-speed UNIX servers, setting the standard for performance-optimized, low-power CMOS. Dr. Davari and his team demonstrated the first shallow-trench-isolation process in 1989, which helps prevent electrical current leakage between semiconductor devices on an integrated circuit. He also led the development of innovations such as low-voltage switches, copper interconnect, silicon-on-insulator technology and high-performance logic-based embedded memory, making possible the computers that serve as the backbone of Internet data centers. An IEEE Fellow and IBM Fellow, Dr. Davari is currently vice president of Next Generation Computing Systems/Technology at the IBM T.J. Watson Research Center, Yorktown Heights, New York.

Akio Nakagawa of Semiconductor Company, Toshiba Corporation, Kawasaki, Japan, has been selected to receive the 2010 IEEE William E. Newell Power Electronics Award. His citation states, "For development of non-latch-up IGBTs."

Akio Nakagawa's development of the non-latch-up insulated-gate bipolar transistor (IGBT), which switches power at high speed, created an indispensable power device now used in applications ranging from air conditioners to hybrid vehicles. Before Dr. Nakagawa's pioneering work in 1984, IGBTs of that time were prone to failure or even destruction due to latch-up (a type of short circuit) caused by the parasitic thyristor of the IGBT. His invented design principles completely suppressed the latch-up even under high-voltage and large-current operating conditions. The ability to withstand the "load-short-circuit" condition for more than 20 µs exceeded the capability of existing bipolar transistors. This set the global standard for IGBT design and enabled its successful commercialization. Dr. Nakagawa's other important contributions include the first two-dimensional power device simulator, developing high-voltage IGBTs and demonstrating the first 500-V silicon-on-insulator device. An IEEE Senior Member, Dr. Nakagawa is currently Technical Consultant of Nakagawa Consulting Office. He previously served as Chief Fellow of Toshiba

Corporation Semiconductor Company, Tokyo, Japan from 2005 to 2009.

Mark J.W. Rodwell of the University of California, Santa Barbara, California, USA, has been named the recipient of the 2010 IEEE David Sarnoff Award. His citation states, "For development of millimeter-wave and sub-millimeter-wave InP bipolar transistors and integrated circuits."

Mark J.W. Rodwell's development of millimeter- and sub-millimeter-wave indium phosphide (InP) heterojunction bipolar transistors (HBTs) has extended the limits of high-frequency radio, high-speed optical communications and powerful imaging applications. During the mid 1990's, Dr. Rodwell sought a breakthrough in the InP HBT fabrication process to boost the device's maximum frequency of oscillation and extend its circuit applications beyond microwave frequencies. Transistors and a series of circuits fundamental to high-frequency communications were subsequently demonstrated, establishing the feasibility of transistors with operating frequencies as high as 1–3 terahertz. Dr. Rodwell's work has enabled development of ultra-high speed wireless radios/links in the previously never reached spectra of the "Terahertz Gap" for short-distance and portable communications and high-resolution cameras/imagers for detecting concealed objects. An IEEE Fellow, Dr. Rodwell is currently a professor in the Department of Electrical and Computer Engineering and director of the Nanofabrication Laboratory at the University of California, Santa Barbara.

Alfred U. Mac Rae
EDS Vice-President of Awards
Mac Rae Technologies
Berkeley Heights, NJ, USA

Status Report from the 2009 EDS PhD Student Fellowship Winners

Agis A. Iliadis
EDS PhD Student Fellowships Chair

In 2000, the IEEE approved the establishment of the Electron Devices Society PhD Student Fellowship Program. The Program is designed to promote, recognize, and support graduate level study and research within the Electron Devices Society's Fields of Interest: which include: All aspects of the engineering, physics, theory, experiment and simulation of electron and ion devices involving insulators, metals, organic materials, plasmas, semiconductors, quantum-effect materials, vacuum, and emerging materials. Specific applications of these devices include bioelectronics, biomedical, computation, communications, displays, electro and micro mechanics, imaging, micro actuators, optical, photovoltaics, power, sensors and signal processing.

In deference to the increasing globalization of our Society, at least one fellowship is to be awarded to students in each of three geographical regions: Americas, Europe/Middle-East/Africa, and Asia & Pacific.

In July 2009, EDS announced the winners of the 2009 Fellowships'. The four winners were:

- Faisal Amir, The University of Manchester, Manchester, UK
- Pierre-Yves Delaunay, Northwestern University, Evanston, IL, USA
- Ximeng (Simon) Guan, Tsinghua University, Beijing, China
- Rinus Lee Tek Po, National University of Singapore, Singapore

The winners are pursuing distinctly different research topics for their doctoral degrees and the following are brief progress reports written by the award winners.

Faisal Amir is pursuing his Ph.D. under the supervision of Professor Mohamed Missous in the School of Electrical and Electronic Engineering, University of Manchester, United Kingdom. He is using physically based, predictive modelling of advanced graded gap gun diodes for use in millimetre waves and terahertz frequencies. Gunn diode models for 77 & 125 GHz second harmonic and 100 GHz fundamental have been realized for the first time and agree extremely well with experimental data. These high frequencies have, hitherto, been outside the capabilities of conventional GaAs Gunn diodes. He has authored or co-authored ten scientific papers which have appeared in top-tier journals and international conferences.

Pierre-Yves Delaunay received the IEEE EDS fellowship in 2009 and is now pursuing his research on infrared cameras based on type-II InAs/GaSb superlattices. He further improved the sensitivity of the imager using new processing techniques. Thanks to the addition of a custom-designed anti-reflective coating, the pixels are now converting 90% of the incoming infrared

radiation. He also demonstrated that this technology does not suffer from low frequency noise. As a result, the camera does not have to be frequently calibrated. Pierre-Yves is now attempting to fabricate detectors that are sensitive to two different spectral windows.

Ximeng Guan His Ph.D. research focuses on the simulation of carbon based nanoelectronic devices. After the research projects on graphene nanoribbon MOSFETs, metal-graphene contacts and carbon-based resistive memory, which were reported at the IEDM in 2007, 2008 and 2009 respectively, he is now working on the simulation of tunneling devices with graphene or graphene naonribbons as channel materials. The purpose of the work is to explore the possibility of achieving manufacturable low-power transistors with a steep subthreshold slope not restricted by the 60 mV/dec limit at room temperature. His Ph.D. thesis is expected to be completed in 2010.

Rinus Tek Po Lee His research interests focus on the application of novel source and drain contact solutions to multiple-gate transistors. In the course of his research, he has published more than 30 technical articles in top-tier journals and international conferences. His Ph.D. thesis titled, advanced source and drain contact engineering for multiple-gate transistors, has been reviewed and will be expected to receive his Ph.D. degree from the National University of Singapore in July 2010.

Agis A. Iliadis
EDS PhD Student
Fellowships Chair
University of Maryland
College Park, MD, USA

IEEE Nanotechnology Council Announces 2010 Award Winners

The IEEE Nanotechnology Council Awards Committee (Chaired by Prof. Laurie Faraone) announced its 2010 award winners for IEEE Nanotechnology Pioneer Award, IEEE NTC Distinguished Service Award and the IEEE NTC Early Career Award. These awards will be presented at IEEE NANO 2010 in Seoul, Korea, August 2010.

Nanotechnology Pioneer Award

The NTC Pioneer Award in nanotechnology is to recognize individuals who by virtue of initiating new areas of research, development or engineering have had a significant impact on the field of nanotechnology. The winner of the 2010 award is:

Dr. Phaedon Avouris, IBM Watson Research Centre, *"For pioneering contributions to the science and technology of carbon-based electronics and photonics."*

Distinguished Service Award

The purpose of the Distinguished Service Award is to recognize an individual who has performed outstanding service for the benefit and advancement of the IEEE Nanotechnology Council. The winner of the 2010 award is:

Professor Aristides Requicha, University of Southern California, *"For leadership excellence as Editor-in-Chief of IEEE Transactions on Nanotechnology."*

Nanotechnology Early Career Award

The purpose of the Nanotechnology Early Career Award is to recognize individuals who have made contributions with major impact on the field of nanotechnology. he winner of the 2010 award is:

Professor Ali Javey, University of California, Berkeley, *"For creative research on nanomaterials and nanotechnologies for electronic applications."*

Congratulations to all the winners!

Laurie Faraone
2010 IEEE NTC Awards
Committee Chair
University of Western Australia
Perth, Australia

Congratulations to the 36 EDS Members Recently Elected to IEEE Senior Member Grade!

Alberto Oscar Adan
Lay-Kee Ang
Jin-Ping Ao*
Carlos Araujo
Olivier Bonnaud
M Scott Burroughs
Luigi Colombo
Yanqing Deng
Gerd Hechtfischer
Aaron Ho Pui Ho
Syed K. Islam
Takuo Kashiwa
Ioannis Kymissis*
Sungjae Lee
Xian Liu
M. Madheswaran
Partha Mallick
Lingyun Miao*
Enrique Alberto Miranda*
Barry Muffoletto
Ciaran Ruairi O'Cochlain
Michael Parker
Vijay K. Reddy
Sean L. Rommel
Nikita M. Ryskin*
Nayanathara Sattiraju
Keyhan Sinai
Bhaskar Srinivasan*
Munehiro Tada*
Tsuyoshi Tanaka*
Thy N. Tran*
David Whaley
Robert Wisnieff
Qun Xiao
Mingwei Xu*
Tetsuo Yamada*

* = Individual designated EDS as nominating entity

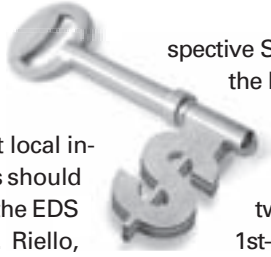
If you have been in professional practice for 10 years, you may be eligible for Senior Membership, the highest grade of membership for which an individual can apply. New senior members receive a wood and bronze plaque and a credit certificate for up to US $25 for a new IEEE society membership. Upon request a letter will be sent to employers, recognizing this new status. For more information on senior member status, visit http://www.ieee.org/web/membership/senior-members/status.html

To apply for senior member status, fill out an application at http://www.ieee.org/organizations/rab/md/smelev.htm

EDS Chapter Subsidies For 2011

The deadline for EDS chapters to request a subsidy for 2011 is September 1, 2010.

For 2010, the EDS AdCom awarded funding to 75 chapters, with most amounts primarily ranging from US $250 to US $1,000. In June, Chapter Chairs were sent an e-mail notifying them of the current funding cycle and providing them with a list of guidelines. In general, activities which are considered fundable include, but are not limited to, membership promotion, travel allowances for invited speakers to chapter events, and support for student activities at local institutions. Subsidy requests should be sent via e-mail or fax to the EDS Sr. Administrator, Laura J. Riello, IEEE, EDS Executive Office, 445 Hoes Lane, Piscataway, NJ 08854, l.riello@ieee.org or fax 732 235 1626.



Prior to the submission of the subsidy request, the Chapter Chair must submit a chapter activity report to its respective SRC Chair and Laura Riello of the EDS Executive Office by July 1st. This report should include a general summary of chapter activities (one to two pages) for the prior July 1st–June 30th period. You must also attach a copy of the activity report to your chapter subsidy request. Final decisions concerning subsidies will be made by the EDS SRC Chairs/Vice Chairs in December. Subsidy checks will be issued by late December.

EDS Senior Member Program

Albert Wang
EDS Vice-President of Membership

The Electron Devices Society established the EDS Senior Member Program to both complement and enhance the IEEE's Nominate-a-Senior-Member Initiative and make IEEE/EDS members aware of the opportunity and encourage them to elevate their IEEE membership grade to Senior Member. This is the highest IEEE grade for which an individual can apply and is the first step to becoming a Fellow of IEEE. If you have been in professional practice of 10 years, you may be eligible for Senior Membership.

New Senior Members receive an engraved wood and bronze plaque and a credit certificate for US$25 to be used towards a new IEEE society membership. Upon your request, the IEEE Admission & Advancement Department will send a letter to your employer recognizing this new status as well. The URL to request this letter is http://www.ieee.org/web/membership/senior-members/notification.html.

As part of the IEEE's Nominate-a-Senior-Member Initiative, the nominating entity designated on the member's application form will receive US$10 from IEEE for each application approved for Senior Member grade when there are at least five approved applications. **As an EDS member, we would appreciate it if you could indicate on your Senior Member application form that EDS is your nominating entity.**

Please be aware that even if you decide to list EDS as your nominating entity, you still need to have an IEEE member nominate you along with two other references. Your nominator and your references all must be active IEEE members holding Senior Member, Fellow or Honorary Member grade.

For more information concerning Senior Membership, please visit http://www.ieee.org/membership_services/membership/senior/senior_requirements.html. To apply for Senior Member grade, please complete an application form, which is available at http://www.ieee.org/membership_services/membership/senior/senior_application.html. You can also request a hard copy Senior Member packet via mail or fax by contacting IEEE Admissions and Advancements Department, Attn: Denise Howard, 445 Hoes Lane, Piscataway, NJ 08854, USA, Fax: +1 732 463 9359, E-mail: d.howard@ieee.org.

We strongly encourage you to apply for IEEE Senior Membership to enhance your career. At the same time, you'll be helping EDS.

Thank you for supporting IEEE and EDS.

Albert Wang
EDS Vice-President of Membership
University of California
Riverside, CA, USA

EDS President Visits Chapters in India

The Electron Devices Society President, Renuka Jindal, visited two EDS Chapters in India during the South Asia Chapters meeting along with South-Asia coordinator, M.K. Radhakrishnan. On April 8, 2010, the visit to the SJCE Student Chapter at Mysore had three sessions comprised of Distinguished Lectures and separate meetings with EDS student members and Faculty members. Two Distinguished Lectures were given, "From Millibits to Terabits and Beyond – Over 60 years of Innovation," by Renuka Jindal and "Lightning Hits VLSI Devices," by M.K. Radhakrishnan. More than 100 participants attended the meeting with EDS student members exchanging ideas and views with the Society President to enhance the visibility of students in various society activities and to benefit student careers.

A regional meeting of EDS members was organized by the India Council Chapter at Salem, Tamil Nadu, South India, April 9, 2010. EDS President, Renuka Jindal, was the Chief Guest. The meeting attracted more than 60 EDS members from the IEEE Madras Section, residing at various locations in Tamil Nadu, as well as more than 100 IEEE student members. After the Distinguished Lecturers by Renuka Jindal and M.K. Radhakrishnan, two separate sessions were organized to encourage interaction between EDS members, IEEE student members and the Society President. Major issues

Renuka Jindal (EDS President), B. G. Sangameswara (Principal SJCE), M.K. Radhakrishnan (EDS Chapter Partner) and C. R. Venugopal (EDS Chapter mentor), along with EDS members at the ED SJCE Student Chapter, Mysore, India.

EDS members of IEEE Madras Section with Renuka Jindal, M.K. Radhakrishnan and India Council Chapter Chair, M. Madheswaran (3rd, 4th & 5th from left, front row), at the EDS members regional meeting at Salem, Tamil Nadu, India

discussed included the benefits that EDS provides to its members and how much the members are aware of and utilize them. A better understanding was created. Possibilities of initiating new EDS Chapters at locations where sufficient member concentration exists, as well as plans for providing direction and support to members through the programs of the India Council Chapter.

Many activities for the betterment of the members, including initiating EDS Webinars, providing educational materials, etc., were planned during these meetings.

M.K. Radhakrishnan
EDS Chapter Partner
NanoRel
Koramangla, Bangalore, India

EDS Distinguished Lecturer Visits the ED Santa Clara Valley Chapter

Jayasimha Prasad, IEEE Fellow and EDS Distinguished Lecturer, gave an excellent presentation on "High Frequency Characterization of Transistors" at the ED Santa Clara Valley Chapter, February 16, 2010. As CMOS devices continue to scale, the high-frequency performance of CMOS is becoming comparable to SiGe HBTs. People are now looking for analog applications in CMOS. The high frequency figures of merit such as Ft, Fmax and Noise Figure are becoming very important. The lecture by Prasad focused on how to measure Ft and Fmax and how this helps in developing a device model. This was very timely and useful, as many of the companies in the Silicon Valley are involved in Analog and Mixed Signal ICs.

The talk began with a very brief introduction to S-parameters and the Smith Chart. This was to bring everyone in the diverse audience to the same level. Next, Prasad talked about the vector network analyzer, calibration and de-embedding using test structures. Then he discussed about the extraction of Ft and Fmax from the measured S-parameters. Prasad described the various definitions of gain, namely, Maximum Available Gain (MAG), Maximum Stable Gain (MSG) and Mason's Gain (U). He showed how they influence the extraction of Fmax. Towards the end, Prasad showed how to extract the series resistances and capacitances of the device for developing a device model. About 50 people attended and everyone enjoyed this very informative talk.

Jayasimha Prasad, IEEE Fellow and EDS Distinguished Lecturer at the ED Santa Clara Valley Chapter

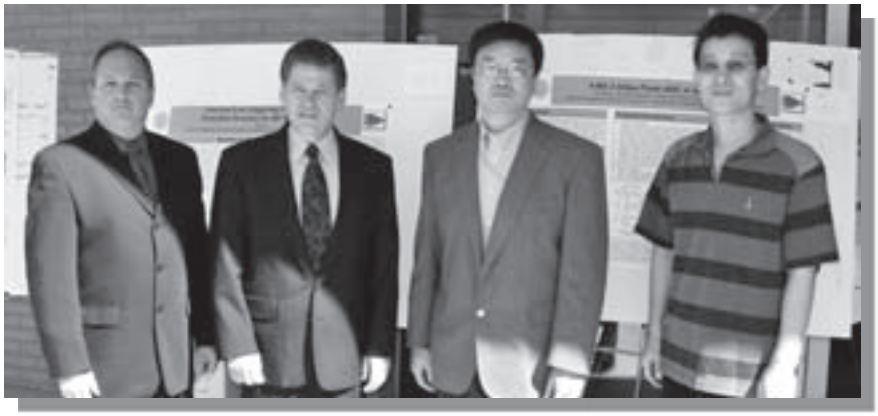
Prior to this lecture, Prasad showed a presentation on the organization and mission of EDS and the benefits of becoming an EDS member. Prasad also encouraged many non-EDS members in the audience to become members of the Society.

Prasad Chaparala
ED Santa Clara Valley Chapter Chair
National Semiconductor Corp.
Santa Clara, CA, USA

Report on 2nd IEEE EDS Mini-Colloquium on MicroElectronics and 2nd IEEE Student Research Symposium at University of California – Riverside (ISRS-UCR)

On April 2, 2010, the 2nd IEEE EDS Mini-Colloquium on Microelectronics and 2nd IEEE Student Research Symposium were held successfully at University of California, Riverside (UCR). This was the 2nd mini-colloquium since the first occurrence held in April 2009.

Two IEEE Fellows and EDS Distinguished Lecturers, Dr. Steven Voldman (IBM) and Dr. Bin Zhao (FreeScale Semiconductor Corp.), presented at the mini-colloquium and were joined by distinguished lecturer, Dr. Nate Peachey (RFMD), from the Board of Directors for the



The three Distinguished Lecturers, (left to right) Dr. Steven Voldman, Dr. Nate Peachey, Dr. Bin Zhao and ED UCR Student Branch Faculty Advisor, Prof. Albert Wang, standing in front of the student poster displays

Some of the participants attending the mini-colloquium along with the three invited lecturers

Dr. Steven Voldman and Prof. Albert Wang presenting Certificate to the winner of the Best Student Paper (graduate level)

Dean of EE department and Prof. Albert Wang present Certificate to the Best Student Paper Award (undergraduate) winner

ESD Association. Each of these lecturers gave the following excellent speeches: *"ESD's Middle Earth – Neither Device nor System Testing,"* by Dr. Nate Peachey, *"The Importance of ESD in the Electronic Industry - From today's microelectronics to future nano-structures,"* by Dr. Steven Voldman, and "*LED Backlighting Solutions for Energy Efficient Display,"* by Dr. Bin Zhao.

The event began with an opening speech by Prof. Albert Wang, an IEEE Fellow and the faculty advisor for the IEEE EDS University of California Riverside Chapter. The three invited DLs presented their speeches and introduced how EDS affects everyday life and the future display of LED. During the poster session, both undergraduate and graduate students presented their ideas and shared what they had researched. The student research covered a wide range: electrical engineering, physics, materials and chemical engineering. More than 40 posters were displayed, which included submissions from approximately 24 graduates and 20 undergraduates. Finally, the Distinguished Lecturers and the dean of the Electrical Engineering department were invited to present the Best Student Paper Awards. The graduate and undergraduate students were awarded cash prizes and certificates, with first place receiving $100 and second place, $50.

Overall, there were 100 students who attended the symposium. They listened to the speeches, communicated with the Distinguished Lecturers and presented their posters. All of our students enjoyed this symposium very much.

He Tang
ED University of California Riverside
Student Branch Chapter Chair
University of California Riverside
Riverside, CA, USA

Report on the IEEE EDS Mini-Colloquium Held in Palma de Mallorca, Spain

An IEEE EDS Mini-Colloquium was held in Palma de Mallorca, Spain, April 11–14, 2010, as a part of the Second International Symposium on Flexible Electronics (ISFE). The ISFE Symposium was organized by the Engineering Conferences International (ECI) Foundation, Universitat Rovira i Virgili (URV, Tarragona, Spain), and the Universitat de les Illes Balears (UIB, Illes Balears, Spain). UIB also organized the IEEE EDS Mini-Colloquium that was integrated into the ISFE Symposium. The Chairman of ISFE and the IEEE EDS Mini-Colloquium was Prof. Rodrigo Picos, from UIB. Prof. Michael Shur (RPI, Troy, NY) and Prof. Benjamin Iñiguez (URV, Tarragona, Spain) were the Conference Co-Chairs.

EDS Distinguished Lecturers at the mini-colloquium held in Palma de Mallorca, (from left to right): Lluis Marsal, Arokia Nathan, Michael Shur, Jacobus Swart, Benjamin Iñiguez, and Rodrigo Picos, ISFE Symposium Chair

The goals of the conference and the IEEE EDS Mini-Colloquium were to present and discuss recent advances in all topics related to flexible electronics, with topics ranging from materials to circuits and systems, including devices, fabrication methodologies, and also modeling techniques. Partial financial support for both the Symposium and the Mini-Colloquium was obtained from the IEEE EDS Distinguished Lecturer Program, the Govern de les Illes Balears (Conselleria d'Innovació, Interior i Justícia, Direcció General d'Innovació, Desenvolupament Tecnologic i Justícia), the European FEDER funds, and the Universitat de les Illes Balears).

Five EDS Distinguished Lecturers gave talks at the IEEE EDS Mini-Colloquium, regarding different topics in the field of Flexible Electronics. Prof. Lluis Marsal (URV, Spain) talked about "P3HT Nanopillar Arrays on ITO Substrates for Developing P3HT Nanostructured Solar Cells." Professor Arokia Nathan (University College London, UK) addressed in his talk the issues in "Low Stress TFTs on Transparent Plastic." Prof. Michael S. Shur (Rensselaer Polytechnic Institute, Troy, NY) conducted a lecture presenting a "Compact Modeling of Advanced Thin Film Transistors: Issues and Challenges." Prof. Jacobus W. Swart (Centro de Tecnologia da Informação Renato Archer (CTI), Brazil) explained some of the problems and solutions regarding "Flexible Optoelectronic Device Fabrication." Finally, Prof. Benjamin Iñiguez (URV, Tarragona, Spain) presented a work entitled "Polymeric Thin Film Transistors: A Review on Fabrication and Modeling", which was carried out with the collaboration of the group led by Prof. Magali Estrada (EDS Distinguished Lecturer) in CINVESTAV (Mexico).

The ISFE and the IEEE EDS Mini-Colloquium were attended by more than 40 people, coming from both academia and industry. The social program included a gala dinner and a tourist visit of the historical downtown of Palma, which was one of the most important cities in the Roman Empire, and is nowadays one of the leading tourist cities in the Mediterranean basin. Attendees considered the conference as very successful in terms of organization, technical quality of the contributions and opportunities for discussions. As a result of this positive impression, it is planned to organize again the ISFE Symposium and the related IEEE EDS Mini-colloquium in 2012.

Rodrigo Picos
2010 ISFE Symposium Chair
Universitat de les Illes Balears
Palma de Mallorca
(Illes Balears), Spain

Report on the IEEE EDS Mini-Colloquium Held in Orlando, Florida

Slavica Malobabic

On March 25th and 26th, the ED Orlando Chapter and IEEE Student Chapter hosted the EDS Mini-Colloquium in Orlando at the University of Central Florida (UCF).

On the opening session, Dr. Issa Batarseh, Director of School of Electrical Engineering and Computer Science, gave an overview of the school. Dr. Juin J. Liou, IEEE EDS Vice President of Regions/Chapter, gave an overview of EDS and the benefits of the membership.

The technical program consisted of the following nine, one-hour talks given by internationally recognized lecturers in the field of electron devices:

- Dr. Tom Sah and Dr. Bin Jie (CTSAH Associates, USA) – Bipolar MOS Field-Effect Transistor Characteristics Operation in the Unipolar Current Mode
- Dr. Jean-Jacques Hajjar (Analog Devices, USA) – Challenges of CDM ESD events simulations
- Dr. Vlad Vashchenko (National Semiconductor Corporation, USA) – ESD for Analog IC Design
- Dr. Tim Maloney (Intel, USA) – Charged Device Model ESD from Factory to Testing
- Dr. Weng Hong Teh (Intel and SEMATECH, USA) – To 3D or Not to 3D
- Dr. Fernando Guarin (IBM, USA) – Microelectronic Reliability Topics for Advanced CMOS and SiGe Technologies
- Dr. Steven Voldman (Intersil,USA) – ESD Protection on Systems
- Dr. Adelmo Ortiz-Conde (Simon Bolivar University, Venezuela) – Recent Applications of the Lambert Function in Device Modeling
- Dr. Hemanth Jagannathan (IBM, USA) – High-k/Metal Gate Technology for Si CMOS Applications – From Inception to Realization

The approximately 60 attendees of the colloquium, mostly students of UCF, socialized with the speakers during the lunches and coffee breaks. At the banquet dinner on the 25th, the speakers sat down with the organizing committee and the IEEE UCF Student Branch in a relaxed atmosphere, and on the 26th, the speakers were invited on an airboat tour of St. John's River.

The detailed program and the presentation slides are posted on the UCF website, (http://esd.eecs.ucf.edu/index.pl/Seminars) starting May. The colloquium was co-sponsored by the IEEE Electron Devices Society, IEEE Student Chapter of UCF, Student Government Association of UCF, and UCF School of Electrical Engineering and Computer Science.

Slavica Malobabic
ED Orlando Chapter Chair
University of Central Florida
Orlando, FL, USA

Speakers and some of the organizing committee members

New IEEE Master Brand + Tagline Graphic Now Available for Download

Images of the IEEE Master Brand + Tagline graphic are now available online in the IEEE Brand Identity Toolkit, under the Master Brand and logos section. Use the IEEE Master Brand + Tagline graphic on materials when no other logo or logo with a tagline exists, as well as on all promotional items. Use the IEEE Master Brand graphic (without tagline) for all other applications. Learn more about the tagline at http://www.ieee.org/tagline.

Visit: http://www.ieee.org/go/brand.

Contact: corporate-communications@ieee.org with questions.

Report on the IEEE EDS Mini-colloquium Held in Guangzhou, China

The ED Guangzhou Chapter started this year's first mini-colloquium on January 8 at South China University of Technology (SCUT). Two EDS Distinguished Lecturers, Prof. Cary Y. Yang of the Center for Nanostructure, Santa Clara University (also former EDS President) and Prof. Wong Hei of City University of Hong Kong, were invited to give the DL talks. More than 40 university academic staff and graduate students attended this event.

Prof. Yang presented his talk entitled, "Transport Phenomena in Carbon Nanostructures," where he introduced the electrical and thermal transport in carbon nanofiber interconnect test structures based on current stress experiment and heat transport modeling. Prof. Wong presented a talk entitled, "Growth of Dielectric -Embedded Silicon Nanocrystallites for Light-Emitting Device Applications," where he described the formation of dielectric-embedded Si-nano-crystals using the Si fabrication technology with phase separation reaction. The chapter also received constructive advice from the DLs and discussed planned activities for the coming year.

Organizers of the EDS Guangzhou Mini-Colloquium, with EDS Distinguished Lecturers, Prof. Cary Y. Yang (3rd from left) and Prof. Hong Wei (5th from left)

Kong Xuedong and
Yang Shaohua
ED Guangzhou Chapter

Electron Devices Society Chapter of the Year Award Call for Nominations

The EDS Chapter of the Year Award is given each year based on the quantity and quality of the activities and programs implemented by the chapters during the prior July 1st–June 30th period. Nominations for the award can only be made by Chapter Partners, SRC Chairs/Vice-Chairs, or self-nominated by Chapter Chairs. The nomination form is available at http://www.ieee.org/portal/pages/society/eds/awards/chapter_award.html or by contacting Laura Riello (l.riello@ieee.org), EDS Executive Office.

The winning chapter will receive a certificate and check for $1,000 to be presented at the IEEE International Electron Devices Meeting (IEDM).

The schedule for the award process is as follows:

Action	Date
Call for Nominations E-mailed to Chapter Chairs, Chapter Partners, SRC Chairs & SRC Vice-Chairs	June 1
Deadline for Nominations	September 15
Regions/Chapters Committee Selects Winner	Early–October
Award given to Chapter Representative at the IEDM	First week of December

EDS South-Asia Chapters Meeting

The Electron Devices Society South-Asia Chapter Chairs and Partners Meeting was held in Bangalore, India, April 10, 2010, and hosted by the IEEE ED/SSCC Bangalore Chapter. Most of the EDS Chapters in the South Asia region were represented at the meeting. EDS President, Renuka Jindal, presided over the meeting and described various activities and future plans of the Electron Devices Society, especially in the region. He congratulated the Chapters for the excellent performance in yester years and for the successful cooperation in organizing the EDS AdCom Meeting held May 2009, in Mumbai. During the last year, two new EDS Chapters – ED Nepal and the VCET Student Chapter at Erode – were started.

Front row, from left: M Madheswaran (ED India Council Chapter), Navakant Bhat (Chapter Partner) R. S. Gupta (Delhi Chapter), M.K. Radhakrishnan (Chapter Partner & South Asia Coordinator), Renuka Jindal (EDS President), Kasi Rajagopal (IEEE India Council Chair), Sunit Tyagi (Chapter Partner). Second Row from left : K. S. Sankara Reddy (Bangalore Chapter), Dipankar Saha (Bombay Chapter), B. P. Harish (Bangalore Chapter), Partha Mallick (NIST Bhubaneswar Chapter), Anisul Haque (Bangladesh Chapter), Bhadra Pokharel (Nepal Chapter), Vikram Divakar & Ajay Patil (SJCE Mysore Chapter)

Activities of all Chapters during the last year were reviewed, showing all Chapters successfully organizing Distinguished Lecturers and Technical Talks. A closer collaboration and communication in terms of future organization of DL-MQs as well as similar activities were planned to organize activities more effectively. The year 2009 was very active, with excellent joint activities reaching out to members. The Bombay Chapter hosted the EDS AdCom last year and was congratulated at the meeting. IEDST 2009, the second occurrence of the EDS conference in Asia, was organized by the ED Bombay Chapter and IIT Bombay, with support by the ED Bangalore Chapter. It was held in conjunction with the EDS AdCom Series and enjoyed very good participation from device researchers in the region. Chapters in Bangalore, Mysore and Delhi organized WIMNACT-18, an EDS DL-mini-colloquia on the sidelines of the EDS AdCom meetings in June. The ED Nepal Chapter was officially inaugurated and organized WIMNACT-19 and the ED Bangladesh Chapter organized WIMNACT-20 in June 2009. The Calcutta Chapter organized DL-MQs at remote locations of Tamil Nadu and Andamns and helped in spreading the EDS activities effectively.

One of the highlights of the All India Chapters Meeting was a special session with the India Semiconductor Association (ISA) in which ISA President, Poornima Shenoy, and EDS President, Renuka Jindal, exchanged their views and found a synergy in working together for the betterment of EDS professionals in the region. Details of the possible collaboration is being worked out which can help in spreading the EDS message to many professionals.

More joint activities, including out-reach programs, are planned for the coming years. In order to effectively utilize the programs, especially DL mini-colloquia, it was decided that any Chapter requesting funding from the EDS Executive Office must send a copy of the request to the Chapter Partners, all other Chapter Chairs in the region and the South-Asia Chapter coordinator. It was suggested that an EDS level award be instituted to encourage student papers in the region. Based on the enthusiasm from EDS members at different locations, the possibility of initiating new EDS Chapters is being sought. All the Chapter Chairs will help in promoting this activity along with the Chapter's coordinator.

M.K. Radhakrishnan
EDS Chapter Partner
NanoRel
Koramangla, Bangalore, India

Regional and Chapter News

USA, Canada & Latin America (Regions 1–6, 7 & 9)

ED Vancouver

- by Durga Misra

On Wednesday April 28, 2010, on the sideline of the EDS sponsored International Symposium on "Dielectrics for Nanosystems," which was held in collaboration with the Electrochemical Society (ECS) in Vancouver, Canada, EDS Subcommittee for Regions and Chapters (SRC) North America East Chair, Durga Misra, EDS Past President, Hiroshi Iwai and EDS Vancouver local Chapter Chair, Bonnie Gray, held a dinner meeting to discuss the Vancouver Chapter activities and plans for 2011.

During the meeting several plans were discussed to have continued sustained chapter activities that contribute substantially to the vitality of the Electron Devices Society, especially bringing students from various local educational institutions together to technical meetings. In 2010, the Vancouver Chapter hosted a Distinguished Lecturer talk by Prof. Juin J. Liou, EDS Vice-President of Regions/Chapters. In addition to several technical meetings it was planned that the Vancouver Chapter should hold a mini-colloquium in the Spring of 2011. Chapter Chair Prof. Bonnie Gray, has agreed to start the planning process. If the colloquium is planned for in conjunction with other conferences in Canada the excellent speakers (DLs) can attend the mini-colloquium with minimum cost. Prof. Hiroshi Iwai will help identify some DLs from Japan who may be traveling to Canada during that time.

It was also discussed how the EDS community can provide additional support to schedule more technical meetings and improve the member benefits.

~ Jamal Deen, Editor

ED Student Chapter at UNICAMP

- by J. W. Swart

A two week Summer course on Microfabrication is held annually at the State University of Campinas, Brazil, since 1999 and always in January during the Summer season of the southern hemisphere. This year it received partial support from EDS, through grant fellowships to two master students from countries of Region 9. After sending out a call for candidates to all region chapters, two masters students from Colombia were selected: Francisco Carlos Calderon B. and Juan Carlos Ortiz P., respectively from Pontificia Universidad Javeriana Bogotá and the Universidad de los Andes.

The course is hands-on where students fabricate MOS and other basic devices and circuits. This course gives students a better view about microfabrication techniques and principles and also motivates students for experimental work. Such hands-on experience also helps to disseminate this knowledge to other students with whom they have contact with at their universities and regions. This means it has a potential multiplication effect. Additionally, it helps to integrate students from different regions. In the past it was restricted to universities in Brazil, but now includes students from other Region 9 countries. The students have always reported very positive feedback about the course, including the present two students from Colombia, indicating the success of this effort.

~ Francisco J. Garcia Sanchez, Editor

(left to right): Hiroshi Iwai, Bonnie Gray and Durga Misra, discussing chapter business in Vancouver, Canada

Students, Calderon and Ortiz with Prof. Diniz (right), coordinator of the course

Europe, Middle East & Africa (Region 8)

ED Poland

- by Zygmunt Ciota

A joint meeting was held on December 4, 2009, in Wroclaw, Poland between the IEEE ED Poland Chapter, and the Microelectronics and Microsystems Sensors Committee of Electronics and Telecommunication, Polish Academy of Science.

The meeting started with Dr. Rafał Walczak's presentation entitled, *"Veterinary and Medical Lab-on-chip Microsystems"*. During the discussion a development of non-commercial IC fabrication center was presented. Furthermore, the project of a national design center of micro- and nanosystems based on Cadence facilities

Participants of the meeting during a presentation at Wroclaw University laboratories

was discussed. Participants also had an opportunity to visit the new high technology laboratories established at the Faculty of Microsystem Electronics and Photonics of Wrocław University of Technology.

~ Zygmunt Ciota, Editor

ED/MTT/AP/CPMT/SSC Nizhny Novgorod

- by Georgy L. Pakhomov

The XIV Nanophysics and Nanoelectronics Symposium was held near the city of Nizhny Novgorod (Avtomobilist sanatorium), March 27–31, 2010. The Symposium was organized by the Institute for Physics of Microstructures of the Russian Academy of Sciences (IPM RAS) and partly sponsored by IEEE. There were about 300 scientists from academia, institutions and industry (including members of IEEE) representing 36 cities, mainly from the Russian Federation. This is an increase from 2009, despite economical factors implying a possible attendance downturn.

The XIV Symposium followed the same format as the preceding conferences: its scope is consistent with the current R&D activities at IPM RAS. These can be divided into five directions: 1) Superconductivity; 2) Magnetic nanostructures; 3) Semiconducting micro- and nanostructures (including methods, electronic and optical properties); 4) General properties of nanostructures and analytic methods for surface studies and 5) Multilayer X-ray optics. The technical program consisted of 11 Plenary and 62 invited talks, accompanied by 118 oral and 153 poster contributions. Several distinguished scientists, such as M.V. Koval'chuk (Director of the RAS Institute of Crystallography and Director of Russian Scientific Centre "Kurchatov Institute") or Academician M.V. Alfimov (Director of the RAS Photochemistry Center) gave comprehensive and cutting edge lectures, which had particular impact for more than 120 young specialists attending the Symposium.

Traditionally, best young students' reports have been selected during the sessions and awarded, again partly using the support from IEEE. At the end, participants concluded about the success of the meeting and decided to continue this series in the next year. The support of IEEE through the Nizhny Novgorod Chapter is greatly acknowledged by the Organizing Committee.

MTT/ED/AP/CPMT/SSC West Ukraine

- by Mykhaylo Andriychuk

The International Conference on Modern Problems of Radio Engineering, Telecommunications and Computer Science (TCSET-2010) was held in the mountain resort of Slavsko, Ukraine, February 23–27, 2010. The Conference was organized by the Ministry of Education and Science of Ukraine, Lviv Polytechnic National University, in technical co-sponsorship with the IEEE Electron Devices Society, and in co-operation with the IEEE MTT/ED/AP/CPMT/SSC West Ukraine Chapter.

The plenary and 7 regular sessions were held at the Conference:

- Signal theory and simulation of electronic circuits
- Antennas, radio-electronic devices and system
- Biotechnical and medical electronic devices and systems
- Telecommunication and information networks and systems
- Digital signal processing
- Computer simulation of electrotechnical and electro-energetic systems
- Electronics: micro- and nanotechnologies, systems and devices.

More than 300 papers from authors visiting from 14 countries were included in the conference program. The most interesting invited papers

Directors Alfimov (PC RAS) Gaponov (IPM RAS) and Litvak (IAP RAS) at Nanophysics and Nanoelectronics Symposium

Prof. Yevhen Yashchyshy, presenting the contribution to photonic antennas at TCSET 2010

presented at the Plenary Session were:

- Zigmunt Bluvband (IAQ, Tel Aviv, Israel), "Quality, Reliability and Safety – 100 Years of the Unity and Struggle of Opposites;"
- Y. Yashchyshyn, J. Modelski (WUT, Poland), A. Chizh, S. Malyshev (IP, Belarus), "Technologies and Applications of Microwave Photonic Antennas;"
- M. Samoylovich, A. Belyanin, N. Tcherniega (CRTI, Russia) "Acoustic Metamaterials – New Materials for Acoustic Electronics."

~ Tomislav Suligoj, Editor

EDS Distinguished Lecturer, Prof. Steve S. Chung (5th from left)

EDS Distinguished Lecturer, Prof. Jordi Suñé (4th from left)

Asia & Pacific (Region 10)

ED Shanghai

In March 2010, the ED Shanghai Chapter held two EDS Distinguished Lectures (DL) at Fudan University. On March 18th, Prof. Steve S. Chung from National Chiao Tung University (Taiwan) gave a DL seminar on the "Development on interface and reliability characterizations of CMOS devices with gate oxide down to 1 nm." As the thickness of gate dielectric of CMOS devices is scaled down to the nanometer regime, conventional capacitance-voltage method has faced increasing difficulties. During the seminar, Prof. Chung provided an overview of conventional and other recently developed techniques, such as charge pumping, gated diode, DCIV methods for CMOS gate dielectric quality characterization. Prof. Chung also presented recent results on gate dielectric reliability study using these new methods. The study includes hot carrier reliability, negative bias temperature instability, oxide interface trap profiling and Hot Carrier stress for CMOS devices with gate oxide thickness less than 2 nm on conventional and strained Si CMOS devices for 90 nm and beyond. The results demonstrated the usefulness of these methods for gate dielectric process and reliability characterization in state-of-the-art CMOS devices.

On March 23rd, Prof. Jordi Suñé from the Universitat Autònoma de Barcelona (Spain) gave a DL on the "Breakdown statistics of advanced gate dielectrics." Reliability assessment of advanced gate dielectrics is more complicated than that of traditional SiO_2 because of the difficulty to integrate multilayer stack dielectrics and the appearance of progressive breakdown. During the seminar, Prof. Suñé presented the recent results on the modeling of gate dielectric breakdown distribution. A compact analytical model was proposed to explain the experimentally observed breakdown distribution of stack dielectrics, including metal-gate PFETs and NFETs with small EOT Hf-based dielectric stacks. The model was also validated by kinetic Monte-Carlo simulation of percolation in gate dielectric.

Both seminars were well attended by graduate students and professors, including both IEEE members and non-members, from Fudan University as well as other nearby institutions. Besides delivering the academic speeches, the two DLs also gave an introduction to the EDS organization and the activities at their home institutions.

ED Xi'an

- by Yimen Zhang

Prof. Albert Chin, from National Chiao-Tung University, Taiwan, visited the ED Xi'an Chapter, March 24, 2010. He delivered a distinguished lecture entitled,"Low-Power High-Performance Electronic Devices for SoC" at Xidian University, Xian, China. The DL audience was comprised of about 50 local professionals and students. This was an excellent lecture that included his latest achievements to solve the power consumption problem in scaling down devices. The most significant contribution focused on high-κ gate dielectric research, such as La_2O_3 and Al_2O_3, to be a solution used for 32~22 nm node CMOS, and the Ge-on-Insulator, to be very useful for low-voltage high-performance Ge logic. Also the MONOS NVM with high-k trapping engineering was presented to achieve fast speed and very low write voltage. To improve the power loss for devices on VLSI-standard Si wafer, ion-implantation was used to form semi-insulating Si substrate. And high performance RF inductors, filters and antennas on Si

operating up to 100 GHz were realized for the first time. Prof. Chin's talk was highly appreciated and was received with great interest. The professor answered many valuable questions.

~ Mansun J. Chan, Editor

Prof. Albert Chin (3rd from left), with (left to right) Prof. Xinbo Gao, Director of the Office of International Cooperation and Exchanges; Prof. Yimen Zhang, ED Xi'an Chapter Chair; and Prof. Yuming Zhang, Vice Dean of the School of Microelectronics

ED/REL/CPMT Singapore

- by Andrew Tay

The ED/REL/CPMT Singapore Chapter is involved in the organization of the 17th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA 2010), held July 5–9, 2010. IPFA 2010 is technically co-sponsored by the IEEE Electron Devices Society, the IEEE Reliability Society and supported by the Singapore Exhibition and Convention Bureau. As in the previous IPFA's the Symposium will have tutorials during the first two days, followed by a three day conference. The tutorial speakers include: David Albin (National Renewable Energy Laboratory, USA), Jeffrey Gambino (IBM, USA), D.S. Ang (Nanyang Technology University Singapore) and Hans-Juergen Engelmann (Globalfoundries, Germany). The two keynote addresses at the conference will be presented by Krishna Saraswat, Stanford University and Rob Steeman, Renewable Energy Corporation.

A technical talk on "Effect of Pulse DC and AC on the Reliability of Dielectric Breakdown in Damascene Cu and Solder Bump Electromigration," was held, January 20, 2010, and the speaker was Professor Young-Chang Joo from Seoul National University, Korea.

The Chapter will organize a Workshop and IEEE EDS Mini-colloquium on NAnometer CMOS Technology (WIMNACT) on July 26, 2010, jointly with three chapters in Perth, Canberra, and Melbourne, Australia from July 27 to August 2, 2010. Four EDS distinguished lecturers are participating in the joint event with sponsorship from the EDS, and the chapter is co-sponsoring local hospitality for WIMNACT-Singapore as well as partial support for the travel to Australia. Experts from Singapore will also be invited for the 1-day WIMNACT on July 26th.

ED SJCE Mysore

- by Vikram and C. R. Venugopal

With the endless pursuits of the chapter members of the ED SJCE Chapter, we organized a series of workshops and talks, thus standing true to the chapter's motto *"Redefining Technicality."* ED SJCE, which has always strived to hone the technical skills of the students, has now proved to be a forum to celebrate the spirit of technology.

The Chapter organized workshops for the students, by the student members. The most important among the two workshops was the robotics workshop called, Workshop on Line following Robots. This workshop was conducted on the March 12 and 13, 2010, with participation of more than 120 attendees from many engineering colleges in and around the city. The workshop, which catered to the 2nd year student's itinerary, included an introduction to robotics and microcontrollers, followed by a hands-on practical session of programming and interfacing. The second day and session involved making the participants build and program a line-following robot. The event aimed at providing a stepping stone to the field of robotics and to publicize EDS and its activities to all.

The second workshop covered the basics of soldering and its applications. This was another initiative taken by the EDS student members to spread awareness among circuit branches and others alike, on the ease and importance of soldering, which is not part of the curriculum. This workshop received a very good response from the students and was an enjoyable experience to the Chapter to organize.

The Chapter also aided the IEEE Photonics Society in conducting a one-day seminar series on recent trends in the field of Photonics.

Participants of the Robotics Workshop

The ED SJCE Student Chapter was pleased to be a part of CYBERIA-10, the annual National level technical fest conducted by the IEEE -SJCE Student Chapter ,organized on of March 19–21, 2010. The SJCE chapter also successfully conducted two events namely, AMAZE – A line maze solving robot building competition and EMBED ME, A 8051 programming competition. The events were a grand success as teams from numerous colleges all over the state participated with great fervor.

~ M.K. Radhakrishnan, Editor

The prize winners of the 2009 EDS Japan Chapter Student Award with guests and chapter executive

Committee meeting participants: (front row, left to right) Prof. A. Toriumi, Prof. H. Iwai, Dr. S. Kimura, Prof. M. Koyanagi, Dr. A. Kurobe, (back row, left to right) Dr. K. Torii, Prof. T. Tanaka, Prof. K. Kita and Prof. K. Tsutsui

ED Japan

- by Shin'ichiro Kimurar

On January 20, 2010, the annual meeting of the ED Japan Chapter was held in Tokyo. Prof. Mitsumasa Koyanagi, Japan Chapter Chair reported the 2009 activities and the 2010 plans for the Chapter. At the meeting, the 2009 EDS Japan Chapter Student Award was presented to the following twelve students for their outstanding activities in the research of electron devices last year:

Miyuki Kouda (Tokyo Tech.) "Charged Defects Reduction in Gate Insulator with Multivalent Materials" (2009 Symposium on VLSI Technology)

Ken Shimizu (Univ. of Tokyo) "Physical Understandings of Si (110) Hole Mobility in Ultra-Thin Body pFETs by <110> and <111> Uniaxial Compressive Strain" (2009 IEDM)

Makoto Suzuki (Univ. of Tokyo) "Post-Fabrication Self-Convergence Scheme for Suppressing Variability in SRAM Cells and Logic Transistors" (2009 Symposium on VLSI Technology)

Tsunaki Takahashi (Tokyo Tech.) "Direct Observation of Subband Structures in (110) pMOSFETs under High Magnetic Field: Impact of Energy Split Between Bands and Effective Masses on Hole Mobility" (2009 IEDM)

Kiichi Tachi (Tokyo Tech.) "Relationship Between Mobility and High-k Interface Properties in Advanced Si and SiGe Nanowires" (2009 IEDM)

Shuhei Tanakamaru (Univ. of Tokyo) "A 0.5V Operation, 32% Lower Active Power, 42% Lower Leakage Current, Ferroelectric 6T-SRAM with VTH Self-Adjusting Function for 60% Larger Static Noise Margin" (2009 IEDM)

Jiezhi Chen (Univ. of Tokyo) "High Hole Mobility in Multiple Silicon Nanowire Gate-All-Around pMOSFETs on (110) SOI" (2009 Symposum on VLSI Technology)

Kohei Nakanishi (Univ. of Tsukuba) "Self-Consistent Monte Carlo Device Simulations Under Nano-Scale Device Structures: Role of Coulomb Interaction, Degeneracy, and Boundary Condition" (2009 IEDM)

Arifin Tamsir Putra (Univ. of Tokyo) "A New Methodology for Evaluating VT Variability Considering Dopant Depth Profile" (2009 Symposium on VLSI Technology)

Kiyohito Morii (Univ. of Tokyo) "High Performance GeO/Ge nMOSFETs with Source/Drain Junctions Formed by Gas Phase Doping" (2009 IEDM)

Keita Yamaguchi (Univ. of Tsukuba) "Atomistic Guiding Principles for MONOS-Type Memories with High Program/Erase Cycle Endurance" (2009 IEDM)

Distinguished lecture meeting on February 17, 2010, at Tokyo Institute of Technology. Dr. T. Gutt and Prof. H.M. Przewlocki and Mr. K. Nayak (5th, 6th and 8th from left, back row)

Choong Hyun Lee (University of Tokyo) "Record-high Electron Mobility in Ge n-MOSFETs Exceeding Si Universality" (2009 IEDM)

Following the annual meeting, the 2009 IEDM Report Session was held. Six speakers, all IEDM subcommittee members, gave summary talks on the following technology fields: "Summary of the 2009 IEDM and CMOS technologies" by K. Imai, (NEC Electronics), "Memory technologies" by N. Takaura (Hitachi), "Power Devices" by K. Imai (Panasonic), "Nano-devices" by A. Kinoshita (Toshiba), "3D stack technologies" by T. Fukushima (Tohoku Univ.). The annual IEDM Report Session has gained widespread popularity among people who were not able to attend the IEDM. It was very successful with around 100 participants at this year's session.

The committee meeting of the EDS Japan chapter was also held at the same day. The guests: Prof. H. Iwai, EDS Past President; Prof. K. Tsutsui, EDS Newsletter Regional Editor, Dr. A. Kurobe; Past EDS Japan Chapter Chair, were welcomed by 2010 EDS Japan Chapter Executives: Dr. S. Kimura; EDS Japan Chapter Chair, Prof. A. Toriumi; Vice Chair, Dr. K. Torii; Secretary, and Dr. K. Kita; Treasurer. The 2009 activities and the 2010 plan of the Chapter were approved at the meeting.

On February 17, 2010, a distinguished lecture was held at Tokyo Institute of Technology, Yokohama. Prof. H.M. Przewlocki (Inst. of Electron Technology, Poland) gave a lecture entitled, "Zero photocurrent measurement methods of MOS system parameters." Following the DL, two additional speakers made presentations: Mr. K. Nayak (Indian Inst. of Technology, Bombay) spoke on "Emerging Nanoscale MOS Transistors" and Dr. T. Gutt (Inst. of Electron Technology, Poland), on the "Effect of SiO_2 and CeO_2 interlayer in La_2O_3 based gate stack on some electrical characteristics of MOS capacitors"

ED Kansai

- by Michinori Nishihara

The ED Kansai Chapter held a Technical Meeting at Kansai University, Osaka, Japan, January 26, 2010, with 28 participants from academia and industries. It was intended to provide feedback from IEDM 2009 to ED Kansai members. Two prestigious lecturers reported on device technology trends reviewing papers presented at the 2009 IEDM.

The first talk was on the latest compound and power semiconductor device and process technology trends by Dr. Kazuki Ota from NEC Nano Electronics Research Labs.

Dr. Ota reported several interesting papers such as a paper from Panasonic which integrated 6 GaN transistors into one chip providing 700V off-state breakdown voltage (7.6) or a paper from IMEC which demonstrated normally-off GaN-on-Si power switching devices (7.4). He also noted that there were many MOSFET papers in III-V Logic Transistors at the Advanced Gate Stack Session and introduced a paper from Intel on In0.7Ga0.3As quantum well FET with TaSiOx high-K gate (13.1) and a paper from IMEC on InGaAs/Ge MOSFET with Al2O3 gate (13.3) and others.

The second speaker, Prof. Kentaro Shibahara from Hiroshima University reported on Silicon Devices and Processes. He reported steady progress in Si Technology in deep submicron from 32nm (28.1) to 16nm (28.7) from industry leaders such as Intel and IBM and also from academia.

Prof. Someya giving a distinguished lecture at Kansai University

Immediately after the IEDM reporting meeting the ED Kansai annual general assembly was held and many subjects were reported and discussed including the following major items: Activity report for 2009, Activity plan for 2010, IMFEDK planning status, nomination activity for IEEE senior members and fellows, updates on Committee Chairs and members, etc.

The Chapter also held a DL Meeting with an invitation to Prof. Takao Someya of the University of Tokyo. The DL held at Kansai University on February 25th attracted 26 attendees. He is a very famous researcher on flexible electronics such as flexible sensor/display membrane explained the history and most recent achievements of flexible electronics, which impressed the audience.

~ Kazuo Tsutsui, Editor

IEDM Feedback Meeting held for ED Kansai chapter members

EDS MEETINGS CALENDAR
(As of 09 April 2010)

The complete EDS Calendar can be found at our web site:
http://www.ieee.org/society/eds/meetings/meetings_calendar.xml. Please visit!

July 2 - 2, 2010, T **International Workshop on Compact Thin-Film Transistor Modeling for Circuit Simulation**, Location: Sala de Graus, Univ. Rovira i Virgili, Tarragona, Spain, Contact: Benjamin Iñiguez, E-mail: benjamin.iniguez@urv.cat, Deadline: 5/7/10, www: http://www.compactmodelling.eu/an_details.php?anID=13

July 5 - 9, 2010, T **American Electromagnetics Conference**, Location: Fairmont Chateau Laurier, Ottawa, Canada, Contact: Shelly Girardin, E-mail: shelly@ee.umanitoba.ca Deadline: 1/5/10, www: http://antem.ee.umanitoba.ca/antem_amerem2010

July 5 - 9, 2010, T **IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits**, Location: Suntec Singapore Int'l Convention & Exhibit. Ctr., Singapore, Singapore, Contact: Jasmine Leong, E-mail: ipfa@pacific.net.sg, Deadline: 1/18/10, www: http://ewh.ieee.org/reg/10/ipfa

July 11 - 13, 2010, * **IEEE/SEMI Advanced Semiconductor Manufacturing Conference**, Location: San Francisco Marriott, San Francisco, CA, USA, Contact: Margaret Kindling, E-mail: mkindling@semi.org, Deadline: 2/2/10, www: http://www.semi.org/asmc2010

July 26 - 30, 2010, @ **IEEE International Vacuum Nanoelectronics Conference**, Location: Sheraton Palo Alto Hotel, Palo Alto, CA, USA, Contact: Ralph Nadell, E-mail: rnadell@pcm411.com, Deadline: 3/31/10, www: http://www.ivnc2010.org/

August 3 - 5, 2010, T **Lester Eastman Biennial Conference on High Performance Devices**, Location: Renssalaer Polytechnic Institute (RPI), Troy, NY, USA, Contact: Greg DeSalvo, E-mail: Greg.DeSalvo@NGC.com, Deadline: 5/25/10, www: http://www.ecse.rpi.edu/conf/LEC2010/

August 17 - 20, 2010, T **IEEE Conference on Nanotechnology**, Location: KINTEX, Ilsan, Gyeonggi-Do, Korea, Contact: Hyelee Lee, E-mail: happy4535@lycos.com, Deadline: 3/1/10, www: http://www.ieeenano2010.org/

August 18 - 20, 2010, T **International Symposium on Low-Power Electronics and Design**, Location: TBD, Austin, TX, USA, Contact: Vojin Oklobdzija, E-mail: vojin@ieee.org, Deadline: 3/5/10, www: http://www.islped.org

August 25 - 27, 2010, T **Mediterranean Microwave Symposium**, Location: Middle East Technical Univ-Northern Cyprus Campus, Guzelyurt, Turkey, Contact: Mohammad Essaaidi, E-mail: m.essaaidi@ieee.ma, Deadline: 5/16/10, www: http://www.mms.ncc.metu.edu.tr/

September 6 - 10, 2010, @ **IEEE World Conference on Photovoltaic Energy Conversion**, Location: Feria Valencia, Valencia, Spain, Contact: Americo Forestieri, E-mail: pvsc@wowway.com, Deadline: 1/30/10, www: http://www.wcpec.org

September 6 - 9, 2010, T **Symposium on Microelectronics Technology & Devices**, Location: Bourbon Conventional Ibirapuera, Sao Paulo, Brazil, Contact: João Antônio Martino, E-mail: martino@lsi.usp.br, Deadline: 3/19/10, www: http://www.sbmicro.org.br/sbmicro

September 6 - 8, 2010, T **International Conference on Simulation of Semiconductor Processes and Devices**, Location: Royal Hotel Carlton, Bologna, Italy, Contact: Rita Mambelli, E-mail: rmambelli@arces.unibo.it, Deadline: 3/6/10, www: http://sispad2010.arces.unibo.it

September 6 - 8, 2010, T **International Conference Mathematical Methods in Electromagnetic Theory**, Location: National Technical Univ.-Kiev Polytechnic Inst., Kyiv, Ukraine, Contact: Oksana Shramkova, E-mail: O.Shramkova@gmail.com, Deadline: 7/12/10, www: http://www.mmet.org/

September 8 - 10, 2010, T **International Conference on Electrical Engineering, Computing Science and Automatic Control**, Location: Instituto Tecnológico de Tuxtla Gutiérrez, Tuxtla Gutiérrez, Mexico, Contact: Judith Esparza-Azcoitia, E-mail: cce@cinvestav.mx, Deadline: 5/24/10, www: http://cce.cinvestav.mx/

September 13 - 17, 2010, T **International Crimean Microwave Conference "Microwave & Telecommunication Technology"**, Location: Sevastopol National Technical University, Sevastopol, Ukraine, Contact: Sergey Smolskiy, E-mail: smolskiysm@gmail.com, Deadline: 5/20/10, www: http://www.crimico.org/en/

September 13 - 16, 2010, T **European Solid-State Device Research Conference**, Location: Hotel Barcelo Renacimiento, Sevilla, Spain, Contact: Angel Rodríguez-Vázquez, E-mail: angel@imse-cnm.csic.es, Deadline: 4/10/10, www: http://www.essderc2010.org

September 13 - 17, 2010, T **International Conference on Hot-Wire (Cat-CVD) Process**, Location: Ecole Polytechnique, Palaiseau, France, Contact: Jean-Eric Bourée, E-mail: jean-eric.bouree@polytechnique.edu, Deadline: 4/1/10, www: http://hwcvd6.polytechnique.fr/

September 19 - 21, 2010, T **IEEE Conference on Intelligent Transportation Systems (ITSC)**, Location: Tivoli Ocean Park Hotel, Madeira Island, Portugal, Contact: ITSC 2010 Secretariat, E-mail: itsc2010@isr.uc.pt, Deadline: 3/15/10, www: http://itsc2010.isr.uc.pt

September 19 - 22, 2010, T **IEEE Custom Integrated Circuits Conference**, Location: Double Tree, San Jose, CA, USA, Contact: Melissa Widerkehr, E-mail: melissaw@widerkehr.com, Deadline: 04/19/2010, www: http://www.ieee-cicc.org

September 20 - 24, 2010, T **International Conference on Electromagnetics in Advanced Applications**, Location: SMC Conference and Function Centre, Sydney, Australia, Contact: Roberto Graglia, E-mail: roberto.graglia@polito.it, Deadline: 2/26/10, www: http://www.iceaa-offshore.org/

September 22 - 24, 2010, T **International Conference on Actual Problems of Electronic Instrument Engineering**, Location: Novosibirsk State Technical University, Novosibirsk, Russia, Contact: Alexander Gridchin, E-mail: ieeensk@yandex.ru, Deadline: 5/15/10, www: http://www.nstu.ru/apeie

September 22 - 24, 2010, T **International Conference on Solid-State Devices and Materials**, Location: The Tokyo University, Tokyo, Japan, Contact: Shoji Tajima, E-mail: ssdm_secretariat@intergroup.co.jp, Deadline: 5/7/10, www: http://www.ssdm.jp

September 27 - 30, 2010, T **IEEE International Seminar/Workshop on Direct and Inverse Problems of Electromagnetic and Acoustic Wave Theory**, Location: Tbilisi State University, Tbilisi, Georgia, Contact: Mykhalyo Andriychuk, E-mail: andr@iapmm.lviv.ua, Deadline: 8/1/10, www: http://ewh.ieee.org/r8/ukraine/georgian/DIPED/

September 27 - 28, 2010, T **IEEE European Microwave Integrated Circuits Conference**, Location: CNIT, Paris, France, Contact: Gilles Dambrine, E-mail: gilles.dambrine@iemn.univ-lille1.fr, Deadline: 2/7/10, www: http://eumw2010.iemn.univ-lille1.fr/

September 28 - October 1, 2010, T **International Conference on Advanced Thermal Processing of Semiconductors**, Location: Hilton University of Florida Conference Center, Gainesville, FL, USA, Contact: Bo Lojek, E-mail: blojek@atmel.com Deadline: 5/31/10, www: http://www.ieee-rtp.org/

October 3 - 8, 2010, T **Electrical Overstress/ Electrostatic Discharge Symposium**, Location: John Ascuaga Nugget Hotel, Reno, NV, USA, Contact: Lisa Pimpinella, E-mail: lpimpinella@esda.org, Deadline: 1/29/10, www: http://www.esda.org/

October 3 - 6, 2010, * **IEEE Compound Semiconductor IC Symposium**, Location: Portola Hotel, Monterey Convention Center, Monterey, CA, USA, Contact: Lisa Boyd, E-mail: l.boyd@ieee.org, Deadline: 5/7/10, www: http://www.csics.org/

October 4 - 6, 2010, * **IEEE Bipolar/BiCMOS Circuits and Technology Meeting**, Location: Radisson Hotel & Suites, Austin, TX, USA, Contact: Janice Jopke, E-mail: ccsevents@comcast.net, Deadline: 5/3/10, www: http://www.ieee-bctm.org/

October 7 - 7, 2010, T **Workshop on Compact Modeling for RF/Microwave Applications**, Location: Radisson Austin Hotel, Austin, TX, USA, Contact: Ramses Van Der Toorn, E-mail: ramses.van.der.toorn@ieee.org, Deadline: 5/3/10, www: http://cmrf.ewi.tudelft.nl

October 11 - 15, 2010, T **European Symposium on Reliability of Electron Devices, Failure Physics and Analysis**, Location: Summit Hotel, Gaeta, Italy, Contact: Giovanni Busatto, E-mail: busatto@unicas.it, Deadline: 3/14/10, www: http://www.esref2010.unicas.it

October 11 - 14, 2010, * **IEEE International SOI Conference**, Location: Catamaran Resort & Spa, San Diego, CA, USA, Contact: Bobbi Armbruster, E-mail: bobbi@bacminc.com, Deadline: 5/14/10, www: http://www.soiconference.org/

October 11 - 13, 2010, * **International Semiconductor Conference**, Location: Hotel Sinaia, Sinaia, Romania, Contact: Cristina Buiculescu, E-mail: cas@imt.ro, Deadline: 6/1/10 www: http://www.imt.ro/cas/

October 12 - 15, 2010, T **IEEE Nanotechnology Materials and Device Conference**, Location: The Clement Monterey, Monterey, CA, USA, Contact: Xiaoping Yun, E-mail: yun@ieee.org, Deadline: 6/15/10 www: Not Available

October 14 - 16, 2010, T **International Vacuum Electron Sources Conference**, Location: Southeast University, Nanjing, China, Contact: Mengqi Zhou, E-mail: zhoumq@public3.bta.net.cn, Deadline: 5/15/10, www: Not Available

October 17 - 21, 2010, * **IEEE International Integrated Reliability Workshop**, Location: Stanford Sierra Camp, S. Lake Tahoe, CA, USA, Contact: Chadwin Young, E-mail: Chadwin.Young@sematech.org, Deadline: 7/16/10, www: http://www.iirw.org/

October 18 - 20, 2010, @ **IEEE International Symposium on Semiconductor Manufacturing**, Location: Hyatt Regency Tokyo, Tokyo, Japan, Contact: Naoko Tani, E-mail: naoko.tani@semiconportal.com, Deadline: 4/12/10, www: http://www.semiconportal.com/issm/

October 25 - 27, 2010, T **International Conference on Advanced Semiconductor Devices and Microsystems**, Location: Smolenice Castle, Smolenice, Slovakia, Contact: 2010 Information Contact ASDAM, E-mail: asdam@asdam.stuba.sk, Deadline: 5/15/10, www: http://www.kme.elf.stuba.sk/asdam/index.php

October 27 - 29, 2010, T **International Workshop on Computational Electronics**, Location: CNR Auditorium, Pisa, Italy, Contact: Massimo Macucci, E-mail: iwce2010@mercurio.iet.unipi.it, Deadline: 6/14/10, www: http://paine.iet.unipi.it/iwce2010

November 1 - 4, 2010, T **International Conference on Solid-State & Integrated Circuits Technology**, Location: Hotel Equatorial, Shanghai, China, Contact: Mengqi Zhou, E-mail: zhoumq@public3.bta.net.cn, Deadline: 7/15/10, www: http://www.icsict2010.com

November 3 - 3, 2010, T **IEEE Electron Devices Activities in Western New York Conference**, Location: Rochester Institute of Technology, Rochester, NY, USA, Contact: Karl Hirschman, E-mail: kdhemc@rit.edu, Deadline: Not Available, www: http://www.rit.edu/kgcoe/ue/eds.php

November 4 - 5, 2010, @ **International Symposium on Next-Generation Electronics**, Location: National Sun Yat-Sen University, Kaohsiung, Taiwan, Contact: Juin Liou, E-mail: liou@ucf.edu Deadline: 6/4/10, www: http://www.isne2010.org

November 7 - 11, 2010, T **IEEE International Conference on Computer Aided Design**, Location: Double Tree Hotel San Jose, San Jose, CA, USA, Contact: Kathy Embler, E-mail: kathy@mpassociates.com, Deadline: 4/19/10, www: http://www.iccad.com/2010/index.html

November 25 - 26, 2010, @ **International Electron Devices and Materials Symposia**, Location: National Central University, Jhongli, Taiwan, Contact: Jin-Wei Shi, E-mail: jwshi@ee.ncu.edu.tw, Deadline: 7/15/10, www: http://www.iedms2010.ee.ncu.edu.tw

December 2 - 4, 2010, * **IEEE Semiconductor Interface Specialists Conference**, Location: The Catamaran Hotel, San Diego, CA, USA, Contact: Martin Frank, E-mail: mmfrank@us.ibm.com, www: http://www.ieeesisc.org/

December 6 - 8, 2010, * **IEEE International Electron Devices Meeting**, Location: Hilton San Francisco, San Francisco, CA, USA, Contact: Phyllis Mahoney, E-mail: phyllism@widerkehr.com, Deadline: 6/25/10, www: http://www.ieee.org/conference/iedm

December 8 - 10, 2010, T **International Conference on Field-Programmable Technology**, Location: Tsinghua University, Beijing, China, Contact: Jinian Bian, E-mail: bianjn@tsinghua.edu.cn, Deadline: 2/28/10, www: http://166.111.68.91/fpt2010/index.htm

December 11 - 15, 2010, T **International Conference on Fibre Optics and Photonics**, Location: Indian Institute of Technology Guwahati, Guwahati, India, Contact: Sunil Khijwania, E-mail: skhijwania09@gmail.com, Deadline: 7/30/10, www: http://www.iitg.ernet.in/photonics2010/

December 12 - 15, 2010, T **Conference on Optoelectronic and Microelectronic Materials & Devices**, Location: Australian National University, Canberra, Australia, Contact: Hark Hoe Tan, E-mail: hoe.tan@anu.edu.au, Deadline: 7/9/10, www: http://commad2010.anu.edu.au/

December 19 - 22, 2010, T **International Conference on Microelectronics**, Location: Sofitel El Gezirah, Cairo, Egypt, Contact: Mohab Anis, E-mail: manis@vlsi.uwaterloo.ca, Deadline: 6/14/10, www: http://www.ieee-icm.com

January 20 - 21, 2011, T **Dielectric Thin Films for Future ULSI Devices: Science and Technology**, Location: Tokyo Institute of Technology, Tokyo, Japan, Contact: Koji Kita, E-mail: kita@adam.t.u-kokyo.ac.jp, Deadline: 9/25/10, www: http://home.hiroshima-u.ac.jp/iwdtf/

EDS Distinguished Lecturers Participate in the 22nd WIMNACT – Yokohama, Japan

On March 5, 2010, the 22nd WIMNACT (Workshop and IEEE EDS Mini-colloquium on NAnometer CMOS Technology) was held at Tokyo Institute of Technology, Yokohama, attracting more than 40 attendees.

Three Distinguished Lecturers gave the following talks: "Guidelines for Developing Nanoscale CMOS devices with Process-Induced Strain Technology: The Strategies and Reliability Issues," by Prof. Steve Chung (National Chiao Tung University, Taiwan); "R&D of Semiconductor Technology in Dalian University of Technology," by Prof. Zhenan Tang (Dalian University of Technology, China); "Performance of Gate and Channel Engineered Double Gate MOSFET Structures and their Applications," by Prof. Chandan Kumar Sarkar (Jadavpur University, India).

In addition to the Distinguished Lecturers, Prof. Yi Shi (Nanjing University, China) gave a presentation entitled, "Semiconductor Nanowires and their applications in optoelectronics".

All of the speakers happened to be from Asia, so this was a good opportunity to exchange information on the Asian semiconductor industry and academics.

Shin'ichiro Kimura
ED Japan Chapter Chair
Hitachi Ltd.
Tokyo, Japan

The 22nd WIMNACT held March 5, 2010. Invited Distinguished Lecturers: Prof. Z. Tang and Prof. S. Chung (3rd and 5th from left, front row), Prof. Y. Shi and Prof. C. K. Sarkar (6th and 7th from left, front row)