IEEE
ELECTRON DEVICES SOCIETY
Newsletter

JULY 2011 VOL. 18, NO. 3 ISSN: 1074 1879 EDITOR-IN-CHIEF: NINOSLAV D. STOJADINOVIC

Table of Contents

Your Comments Solicited

Dear IEEE EDS Newsletter reader:

Renuka P. Jindal
EDS President

In an attempt to reach out to our global readership and initiate a dialog, we are launching a "Letters to the Editor" section in the Newsletter. This will be a forum to communicate on topics primarily of general interest related to the Electron Devices Society in particular and IEEE in general, addressing issues that are on your mind. Please make use of this opportunity.

We look forward to hearing from you.

Thank you.

Renuka P. Jindal
President
IEEE Electron Devices Society

2011 IEEE Compound Semiconductor IC Symposium (CSICS)

October 16–19, on Hawaii's Big Island

Photo courtesy of the Hilton Waikoloa Village

We cordially invite you to the 2011 IEEE Compound Semiconductor IC Symposium (CSICS) being held October 16–19, at the Hilton Waikoloa Village located on Hawaii's Big Island. Over the last 33 years the Symposium has been and continues to be the preeminent international forum in which advances in semiconductor circuit and device technology are presented, debated, and discussed. The scope of the Symposium encompasses devices and circuits in GaAs, SiGe, InP, GaN, and InSb as well as RF/mm-wave and high-speed digital CMOS to provide a truly comprehensive conference. This is the ideal forum for presentation of the latest results in microwave/mm-wave, high-speed digital, analog, mixed mode, optoelectronic integrated circuits, and power conversion.

The 2011 CSIC Symposium is comprised of a full 3-day technical program, 2 short courses, a primer course, and a technology exhibition. The technical program consists of approximately 60 high

(continued on page 4)

Your Comments Solicited

Your comments are most welcome. Please write directly to the Editor-in-Chief of the Newsletter at ninoslav.stojadinovic@elfak.ni.ac.rs

ELECTRON DEVICES SOCIETY

IEEE prohibits discrimination, harassment, and bullying. For more information, visit http://www.ieee.org/web/aboutus/whatis/policies/p9-26.html.

EDS AdCom
Elected Members-at-Large
Elected for a three-year term (maximum two terms) with 'full' voting privileges

2011	Term	2012	Term	2013	Term
G. Baccarani	(2)	R. Huang	(2)	Arturo Escobosa	(1)
M.J. Deen	(2)	S.S. Iyer	(1)	Juin Liou	(1)
S. Deleonibus	(1)	M. Meyyappan	(1)	Mikael Ostling	(1)
F. Guarin	(1)	H.S. Momose	(2)	M.K. Radhakrishnan	(1)
S. Saha	(1)	A. Nathan	(1)	Ravi Todi	(2)
H. Shang	(2)	M. Shur	(1)	Albert Wang	(1)
J.W. Swart	(2)	B. Zhao	(1)	Xing Zhou	(1)
P.K.L. Yu	(1)				

NEWSLETTER EDITORIAL STAFF

Contributions Welcome

Readers are encouraged to submit news items concerning the Society and its members. Please send your ideas/articles directly to either the Editor-in-Chief or appropriate Editor. The e-mail addresses of these individuals are listed on this page. Whenever possible, e-mail is the preferred form of submission.

Newsletter Deadlines

Issue	Due Date
January	October 1st
April	January 1st
July	April 1st
October	July 1st

The EDS Newsletter archive can be found on the Society web site at https://www.ieee.org/portal/pages/society/eds/pubs/newsletters/newsletter.html. The archive contains issues from July 1994 to the present.

IEEE Electron Devices Society Newsletter (ISSN 1074 1879) is published quarterly by the Electron Devices Society of the Institute of Electrical and Electronics Engineers, Inc. Headquarters: 3 Park Avenue, 17th Floor, New York, NY 10016-5997. Printed in the U.S.A. One dollar ($1.00) per member per year is included in the Society fee for each member of the Electron Devices Society. Periodicals postage paid at New York, NY and at additional mailing offices. Postmaster: Send address changes to IEEE Electron Devices Society Newsletter, IEEE, 445 Hoes Lane, Piscataway, NJ 08854.

Upcoming Technical Meetings

2011 IEEE International Integrated Reliability Workshop (IIRW)

The 2011 IEEE International Integrated Reliability Workshop (IIRW), sponsored by the IEEE Reliability Society and the IEEE Electron Devices Society, will be held at the Stanford Sierra Conference Center on the shores of Fallen Leaf Lake near South Lake Tahoe, California, October 16–20, 2011. This workshop provides a unique forum for open and frank discussions of all areas of reliability research and technology for present and future semiconductor applications.

Hot reliability topics include: transistor reliability including hot carriers and NBTI/PBTI, high-k and nitrided SiO_2 dielectrics, SiGe and strained Si, III-V, SOI, novel device reliability, organic electronics, emerging memory technologies and future "nano" technologies, Cu interconnects and low-k dielectrics, product reliability and burn-in, impact of transistor degradation on circuit reliability, reliability modeling and simulation, optoelectronics, single event upsets, NEMS/MEMS, and photovoltaics. The complete Call for Papers can be found at www.iirw.org. Please submit abstracts to the Technical Program Chair, Andrew Turner, IBM (aaturner@us.ibm.com) until the submission deadline of July 16, 2011.

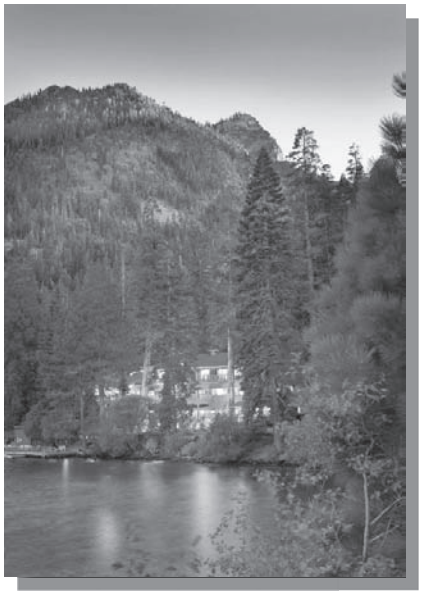
The IIRW is quite a bit different from a typical technical conference. From the moment you arrive, you realize that you are taking part in something special. Located 6000 ft high in the Sierra Nevada Mountains, the Stanford Sierra Conference Center provides an ideal atmosphere for a relaxing yet informative workshop. All aspects of the workshop, including the physical isolation of the location, the absence of distractions such as in room phones and television sets, and the format of the technical program encourage extensive interaction among the workshop attendees. You feel yourself drawn into technical discussions from the start.

Nestled throughout the pines and cedars along the shoreline of Fallen Leaf Lake, attendees stay in cabins furnished in the rustic style of an alpine resort. All rooms have decks with magnificent views of Fallen Leaf Lake and the surrounding Sierra peaks. Comfortable, informal dress is encouraged, affiliations are downplayed, and meals are provided family-style in the lodge dining room. This peaceful setting, free from the distractions of modern life, presents a terrific opportunity to get to know your colleagues, including internationally renowned experts. This is an opportunity not usually available at larger, more hectic conferences. Instead of watching TV, participants spend their evenings at informal poster sessions, discussion groups, and special interest groups, all with refreshments and snacks provided to stimulate discussions. At the end of the day, attendees are free to relax in front of a roaring fireplace in the rustic Old Lodge.

One advantage of the IIRW is the moderated **Discussion Groups** that are held in the evenings, organized this year by Ricki Southwick, Boise State University. Following up on the Discussion Groups are the **Special Interest Groups**, which are composed of small groups of attendees who want to continue their discussions on a particular topic of interest which often continues even after leaving the workshop.

Yet another advantage of attending the IIRW is the extensive collection of **Tutorials**, presented by leading experts and included at no additional cost. This year the tutorials are jointly organized by Tibor Grasser, TU Wien and Jim Lloyd, SUNY Albany and cover diverse reliability issues related to NBTI, Electromigration, Reliability and variability of FinFETs, soft errors and irradiation, reliability of III-V semiconductors, hot carriers, and the implications of TDDB for high-k. Check the IIRW website for updates on tutorial presenters.

One unique aspect of the workshop is the opportunity for any attendee to present a walk-in poster of their latest work. No matter how far along your research is, your ideas will be accommodated. This is a great way to share that new project



Vance Fox Photography

The main lodge at the Stanford Sierra Conference Center. The center provides lodging, meals and meeting facilities as well as excellent recreation including hiking in the Desolation Wilderness and boating on Fallen Leaf Lake.

you are working on and to get world-class feedback.

Finally, attendees have Wednesday afternoon off to enjoy a variety of outdoor activities such as hiking, volleyball, sailing or kayaking, biking, walking, or simply continuing that intriguing conversation from the night before. This free afternoon is a great way to not only network, but also to build long-lasting friendships.

Additional information about the workshop is available on the IIRW website at www.iirw.org, or by contacting Rolf Geilenkeuser of Globalfoundries, 2011 IIRW General Chair, (rolf.geilenkeuser@globalfoundries.com). Note: If you want to take part in this event, please register early as space at the Stanford Sierra Conference Center is limited to roughly 120 attendees and the workshop has sold out in the past.

On behalf of the 2011 IIRW Committee, I look forward to meeting you in Lake Tahoe!

Andreas Aal
2011 IIRW Communications Chair
Melexis
Erfurt, Germany

2011 IEEE Compound Semiconductor IC Symposium (CSICS)

(continued from page 1)

quality state-of-the-art technical papers, 4 panel sessions, and an Industry Exhibit. The short courses, which run in parallel on Sunday, October 16th, are titled "Radar Fundamentals, Systems, and Circuits" and "Stability Techniques for Microwave and RF Amplifier Design" and provide the attendees with a unique opportunity to learn from ten world-renowned instructors in their respective areas of expertise. The Symposium will also be offering the popular annual introductory level primer course on "Basics of Compound Semiconductor ICs." This year the Symposium will feature approximately 15 invited papers on a wide range of important topics encompassing device engineering to circuit application using advanced compound and other related semiconductor technologies. In addition, the Symposium will continue the tradition of including important "late breaking news" papers.

The technology exhibition will be held on Monday and Tuesday. The exhibition will feature informative and interesting displays with corporate representatives on hand. The list of exhibitors can be found in the CSICS advance program which will be published and distributed in late June.

To complement the Symposium, there are several social events which include the Sunday Evening CSICS Opening Reception, the Monday CSICS Exhibition Opening Reception, the CSICS Exhibition Luncheon on Tuesday, and a Luau on Tuesday evening. Breakfasts and coffee breaks will also be served on Monday, Tuesday, and Wednesday.

The Symposium will be held at the Hilton Waikoloa Village Resort. This 62-acre oceanfront resort blends contemporary facilities with the graceful Hawaiian culture and is a destination within itself. Three towers occupy a protected oasis woven around tropical gardens which abound with the subtle elegance of Hawaiian splendor. The property boasts two championship golf courses, a seaside putting course, eight world-class tennis courts, the luxurious Kohala Spa, nine restaurants featuring all sorts of international cuisine, shops, a Museum Walkway lined with authentic treasures, and a Camp Menehune children's program. Activities at the resort include the famous Dolphin Quest Dolphin Swim and Encounter and snorkeling in a four acre saltwater lagoon with the honu (sea turtles) by the waterfall. On the big island one can tour the Hawaii Volcanoes National Park on a Twilight Tour or take a scenic drive along the Hamakua Coast.

For registration and further information, please visit the CSICS website at http://www.csics.org. Further questions may be addressed to the Symposium Chair: Dan Scherrer, Phone: 1-310-812-5892, E-mail: dan.scherrer@ngc.com. We hope you can attend.

Harris (Chip) Moyer
2011 CSICS Publicity Chair
HRL Laboratories, LLC
Malibu, CA, USA

Society News

Announcement Of Newly Elected AdCom Members

Cor L. Claeys
EDS Chair of Nominations and Elections

On December 5, 2010, the EDS AdCom held its annual election of members-at-large. The following are the results of the election and brief biographies of the individuals elected.

ADCOM MEMBERS-AT-LARGE

A total of seven persons were elected to three-year terms (2011–2013) as members-at-large of the EDS AdCom. One of the seven individuals was re-elected for a second term, while the other six were first-time electees. Their backgrounds span a wide range of professional and technical interests.

SECOND TERM ELECTEES:

Ravi M. Todi received his Master's and Doctoral degree in Electrical Engineering from the University of Central Florida. His graduate research work was focused on gate stack engineering, with emphasis on binary metal alloys as gate electrode and on high mobility Ge channel devices. His research interest includes semiconductor process integration and device technology for non-conventional CMOS scaling. Since 2007, he is working as Advisory Engineer/Scientist at Semiconductor Research and Development Center at IBM Microelectronics Division focusing on high performance eDRAM integration on 45 nm and 22 nm SOI logic platforms. Ravi is former Editor-in-Chief for *IEEE Potentials*, Chair of the EDS GOLD Committee and is an IEEE EDS Distinguished Lecturer. He has also served on the IEEE-USA Board of Directors, the IEEE-Region 1 Board and the IEEE Publications Board.

FIRST-TIME ELECTEES:

Arturo Escobosa was born in Culiacan, Mexico. He received a degree in Communications and Electronics Engineering from the National Polytechnic Institute, Mexico in 1978. He was granted a Masters in Science diploma in Electrical Engineering from Cinvestav, Mexico, also in 1978. He received his Ph.D. degree from the Aachen Technical University, Germany in 1983, due to his work at the Institute of Semiconductor Electronics, in the field of ohmic contacts on GaAs MOCVD epitaxial layers. Since 1983, he has been working as full professor at the Solid State Electronics Group of the Electrical Engineering Department of Cinvestav, México. His research interests include MOCVD Epitaxial Growth of III-V Compounds, Optical Characterization of Semiconductors, X-Ray diffraction for Crystal Characterization.

Juin J. Liou received the Ph.D. degree from the University of Florida, Gainesville in 1987. He is now with the School of EECS at the University of Central Florida. Dr. Liou has been awarded 6 U.S. patents, and has published 8 books, 240 journal papers, and 190 papers in conference proceedings. Dr. Liou was awarded the UCF Pegasus Distinguished Professor in 2009 – the highest honor bestowed to a faculty member at UCF, and the IEEE Joseph M. Biedenbach Outstanding Engineering Educator Award in 2004. His other honors are Fellow of IEEE, Fellow of IET, and Chang Jiang Endowed Professor of Ministry of Education – the highest honorary professorship in China. Dr. Liou served as the IEEE EDS Vice-President of Regions/Chapters, IEEE EDS Treasurer, IEEE EDS Administrative Committee Elected Member, and IEEE EDS Educational Activities Committee Member.

Mikael Östling received his MSc degree in engineering physics and Ph.D. degree from Uppsala University in 1980 and 1983, respectively. He holds a position as professor in solid state electronics and is appointed Dean of the School of Information and Communication Technology, KTH. He was a senior visiting Fulbright Scholar with the Center for Integrated Systems (CIS) at Stanford University, and a visiting professor with the University of Florida, Gainesville. In 2005, he co-founded the company TranSiC, which was acquired by Fairchild Semiconductor in 2011. In 2009, he received the first ERC award for advanced investigator grant. His research interests are silicon/silicon germanium devices and

process technology for very high frequency, as well as device technology for wide bandgap semiconductors with special emphasis on silicon carbide for high power applications. He has supervised 30 Ph.D. theses works, and authored about 400 scientific papers published in international journals and conferences. He is an editor of the *IEEE Electron Device Letters* and a Fellow of the IEEE.

M.K. Radhakrishnan is Chief Technical Consultant NanoRel, Singapore and Visiting Professor Department of Electronics, Cochin University of Science and Technology, India. During the past 30 years he worked with ST Microelectronics, Philips, ISRO, Institute of Microelectronics and National University of Singapore at various senior positions. He was Technical Chair IEEE IPFA 1995–97, IPFA General Chair 1999, IPFA Board member, IEEE IEDST General Chair 2009 and Chairman IEEE Rel/CPMT/ED Singapore Chapter 2000–01. He is an EDS Distinguished Lecturer, EDS Newsletter Editor and SRC Vice-Chair for Region 10. Radhakrishnan is an Editorial Board Member of Microelectronics Reliability Journal. He provides technical training in device analysis area to practicing engineers for past two decades and doing research in the area of physical failures including gate dielectrics. He is a Fellow IETE, Member ESD Association and Member EDFAS.

Albert Wang received BSEE from Tsinghua University and Ph.D. from the State University of New York at Buffalo. He is a Professor at the University of California. His research covers Design-for-Reliability, RF/analog ICs and SoCs, CAD and Modelling, Nano Devices and Circuits, etc. He published one book and 160+ papers. Wang has been on the editorial board for *IEEE Electron Device Letters, Transactions on Circuits and Systems II, Journal of Solid-State Circuits, Transactions on Circuits and Systems I* and *Transactions on Electron Devices*. He is a Distinguished Lecturer and Membership Vice President for the IEEE Electron Devices Society. He is a Fellow of IEEE and AAAS.

Xing Zhou received his B.E. degree in electrical engineering from Tsinghua University in 1983, M.S. and Ph.D. degrees in electrical engineering from the University of Rochester in 1987 and 1990, respectively. He is currently a tenured Associate Professor in the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore. His past research interests include Monte Carlo simulation of photo carrier transport and ultra fast phenomena as well as mixed-mode circuit simulation and CAD tool development. His recent research mainly focuses on nanoscale CMOS device compact modeling. He is an editor for *IEEE Electron Device Letters*, Chair of the EDS Asia Pacific Subcommittee for Regions/Chapters, a member of the EDS Compact Modeling Committee as well as Membership, Publications, and Educational Activities Committees, an EDS Distinguished Lecturer and a Senior Member of the IEEE.

Cor L. Claeys
EDS Chair of Nominations and Elections
IMEC
Leuven, Belgium

Call for Nominations – EDS AdCom Members-at-Large

Cor L. Claeys
EDS Chair of Nominations and Elections

The Electron Devices Society of the IEEE invites the submission of nominations for election to its Administrative Committee (AdCom). Presently, the EDS AdCom meets twice per year and is composed of 22 members. Eight members will be elected this year for a term of three years, and a maximum of two consecutive terms is allowed. In 2011, the election will be held after the AdCom Meeting on Sunday, December 4th. Electees begin their term in office on January 1, 2012. For your information, the nominees do not need to attend the AdCom Meeting/Election to run.

Nominees are being sought to fill the slate of candidates. Nominees may be self-nominated, or may be nominated by another person; in the latter case, the nominee must have been contacted and have agreed to serve if elected. Any member of EDS in good standing that has previously served for at least one year as an EDS AdCom Member (Standing and Technical Committee VPs and Members, Publication Editors, Representatives & Chapter Chairs) is eligible to be nominated. The nominees do not

need to attend the AdCom Meeting/ Election to run. On the other hand, if elected, the nominees are expected to attend the two AdCom Meetings a year. While the December meeting is organized in connection with the IEEE International Electron Devices Meeting, the Spring meeting is frequently held outside the US. In general, the travel and accommodation costs to attend these meetings are borne by the elected member.

All nominees must be endorsed by one 'full' voting member, i.e., one of the four officers (President, President-Elect, Treasurer or Secretary), the Jr. or Sr. Past President or one of the 22 current AdCom Members-at-Large.

Please send your nominee's name, address, endorsement letter and supporting information to the EDS Executive Office Sr. Administrator, Laura J. Riello, IEEE, 445 Hoes Lane, Piscataway, NJ 08854, Fax: 732-235-1626, E-mail: l.riello@ieee.org in time to be received by the deadline of **October 15, 2011**. It is very desirable that submissions include a biographical summary in a standard two-page format. The EDS Executive Office can provide you with an example of the format. If you have any questions regarding the nomination requirements or process, feel free to contact Laura Riello (l.riello@ieee.org).

Cor Claeys
EDS Chair of Nominations
& Elections
IMEC
Leuven, Belgium

EDS Administrative Committee Election Process

The Members-at-Large (MAL) of the EDS AdCom, are elected for staggered three-year terms, with a maximum of two consecutive terms. The 1993 Constitution and Bylaws changes mandated increasing the number of elected MAL from 18 to 22, and required that there be at least two members from both IEEE Region 8 (Europe, Middle East & Africa) and Region 10 (Asia & Pacific). In 2003, EDS made changes to its Constitution and Bylaws to require that at least one elected AdCom member is a Graduate of the Last Decade (GOLD member). A GOLD member is defined by IEEE as a member who graduated with his/her first professional degree within the last ten years. It is also required that there are at least 1.5 candidates for each opening. In 2011, eight positions will be filled.

Each nominee needs to be endorsed by a 'full' voting member, i.e., one of the four officers (President, President-Elect, Treasurer or Secretary), the Jr. or Sr. Past President or one of the 22 current AdCom Members-at-Large. The endorser needs to submit an email to Laura Riello (l.riello@ieee.org) stating that he/she would like to endorse the candidate.

Effective with the 2010 election, the EDS AdCom approved a change to now require that each nominee must have previously served for at least one year as an EDS AdCom Member (Standing and Technical Committee VPs and Members, Publication Editors, Representatives & Chapter Chairs).

The election procedure begins with the announcement and Call for Nominations in the *EDS Newsletter.* The slate of nominees is developed by the EDS Nominations Committee and includes the non-Committee and self-nominations received. Nominees are asked to submit a two-page biographical resume in a standard format.

Nominations are closed on October 15th, and the biographical resumes and endorsement letters are distributed to the 'full' voting members of AdCom prior to the December AdCom Meeting. The election is then held after the conclusion of the meeting. The nominees do not need to attend the AdCom Meeting/ Election to run. On the other hand, if elected, the nominees are expected to attend the two AdCom meetings a year. While the December meeting is organized in connection with the IEEE International Electron Devices Meeting, the spring meeting is frequently held outside the US. In general, the travel and accommodation costs to attend these meetings are borne by the elected member.

A continuing flow of new AdCom members who are interested in working for the improvement of the Society and its related technical areas is essential for the continued development of EDS and the field of electron devices. Those interested in the field, the Society, and its operations are encouraged to attend AdCom meetings, become involved in Society activities, and consider running for election to AdCom.

Cor Claeys
EDS Chair of Nominations
& Elections
IMEC
Leuven, Belgium

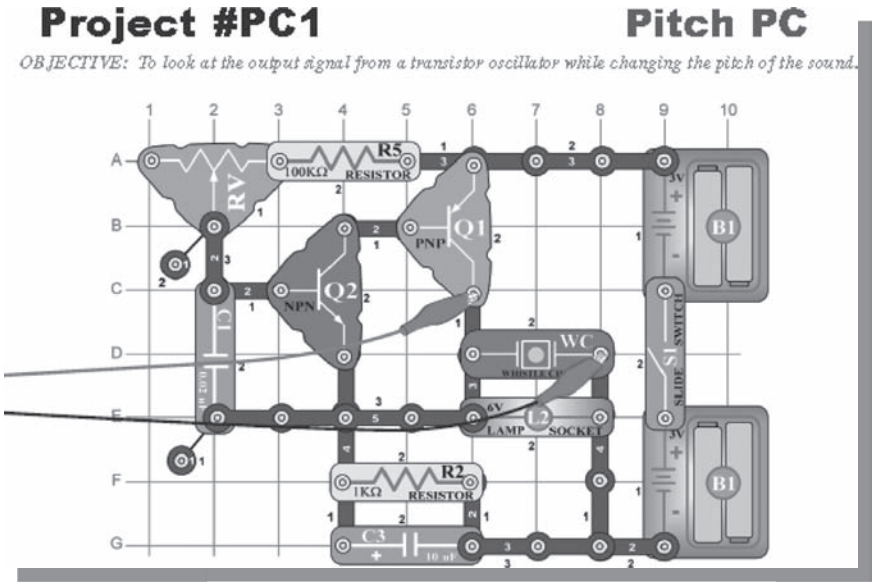
EDS-ETC (Engineers Demonstrating Science: an Engineer Teacher Connection)

As part of the EDS strategy on rejuvenating chapter activities in the United States and the rest of the world the newly created program "EDS-ETC (Engineers Demonstrating Science: an Engineer Teacher Connection)," will be formally introduced in the near future. Activities in this area date back to several years carried out by the ED Mid-Hudson Valley Chapter under my stewardship as EDS Chapter Chair. In 2008, when Renuka Jindal visited our chapter, he was very supportive of this effort. Since then, with strong support from him as EDS President, the effort is being expanded. The program has been designed with the help of volunteers from the Rochester, Boise and the Mid-Hudson Valley Chapters. These dedicated volunteers have run initial evaluations working with their local science teachers ranging from the 4th through 12th grade levels. In the first phase of this project, EDS plans to make this offering available to our chapters in the United States. Based on this experience the Society plans to roll it out to EDS chapters around the globe. In anticipation, we have recruited the ED Colombia Chapter to run a pilot program in Bogota with the participation of two major universities partnering with local schools.

EDS-ETC
Engineers Demonstrating Science:
an Engineer Teacher Connection

Elenco Snap Circuits® Kit

Fernando Guarin (4th from left) with members of the ED Colombia Chapter



The goal of the program is to enable chapter members to visit local schools or host events designed to engage young students in the field of electrical engineering. By utilizing the easy-to-use Elenco Snap Circuits® kits, students learn about electronic circuits using a "hands-on" approach to experience the exciting and creative field of electronics. We hope to encourage them to consider electrical and electronic engineering as a career. This versatile tool, along with your enthusiasm and expertise, will be used to demonstrate the many applications and motivate young students into the electron devices field. Stay tuned for a formal announcement and full program details.

Fernando Guarin
ED Mid-Hudson Chapter
IBM Microelectronics
Hopewell Junction, NY, USA

EDS President Visits Purdue University

On Friday, March 4, 2011, Dr. Renuka Jindal, President of the IEEE Electron Devices Society, visited Purdue University's College of Electrical and Computer Engineering (ECE), Network for Computational Nanotechnology (NCN) and the Birck Nanotechnology Center (BNC) in West Lafayette, Indiana. Purdue's College of ECE has over 65 undergraduate and graduate students in the Micro and Nanotechnology (MN) area, which is primarily focused on electron devices (EDs). An important objective of Dr. Jindal's visit to Purdue was to encourage students to achieve their personal best, instill a desire to give back to their communities, to realize the benefits of being an active member of professional organizations and to discuss plans for the establishment of an EDS chapter at Purdue.

One of the exciting ways MN students are giving back to their community is through Purdue University's Nanodays 2011. This K-12 outreach activity that has been organized by the students, with the help of faculty and staff of BNC and NCN. So far more than 170 graduates, undergraduates, faculty and staff from many areas have volunteered to help with this two day event. Over 26 interesting micro and nanotechnology related activities and demonstrations will be featured. These activities range from thermoelectricity to piezoelectricity to photovoltaics to carbon nanotubes devices. Based on the number of groups that have signed up to attend, more than 1,000 K-12 students, teachers and parents from the local community are expected to attend this year's event.

An equally fantastic outreach resource NanoHUB.com, is being led by Purdue's Network for Computational Nanotechnology (NCN), which was established with funding from the National Science Foundation. MN students are contributing to this website, which is free and open to the public. The website contains video courses, simulation tools, animations and many other teaching materials. Over 165,000 users visit this site annually.

Birck Technology Center

BNC gowning area

As part of his visit, Dr. Jindal toured the Birck Nanotechnology Center. This building is an impressive 187, 000 sq. ft facility that was completed in July of 2005. In the heart of the building is the 25,000 sq. ft Scifres Nanofabrication Laboratory, which is a nanofabrication cleanroom. For more information about BNC, please visit http://www.purdue.edu/discoverypark/nanotechnology

During lunch, Dr. Jindal led a discussion on the responsibility that each of us has in the field of electron devices to strive to reach our personal best in our studies and future work, as well as our responsibility to give back to our communities and mentoring others. Many of the discoveries made in the electron devices field have led to important breakthroughs in technology. Following lunch, Dr. Jindal gave two seminars. The first one was geared towards graduate and undergraduate students and focused on the benefits of starting and joining an IEEE EDS Chapter. It is important that students realize the value of being contributing members of EDS and IEEE. The second was a fascinating seminar on his research of Nano-FET Fluctuation Physics.

John Wilcox
Purdue University
West Lafayette, IN, USA

Message from the EDS Newsletter Editor-in-Chief

Ninoslav D. Stojadinovic EDS Newsletter Editor-in-Chief

I would like to introduce a new addition to the EDS Newsletter Editorial Staff, Fernando Guarin, of IBM Microelectronics, New York, whose biography follows. Dr. Guarin will now be coordinating news for the Eastern, Northeastern & Southeastern USA (Regions 1, 2 & 3). It is my pleasure to welcome him as a new editor for the *EDS Newsletter.*

Fernando Guarin is a Senior Engineer/Scientist at the IBM Microelectronics Semiconductor Research Development Center SRDC in New York State. He received his BSEE from the "Pontificia Universidad Javeriana", in Bogotá, Colombia, the M.S.E.E. degree from the University of Arizona, and the Ph.D. in Electrical Engineering from Columbia University. His doctoral research studied the Molecular Beam Epitaxial growth of Silicon based alloys for device applications. He has been actively working in microelectronic reliability for 30 years.

From 1980 until 1988 he was a member of the Military and Aerospace Operations division of National Semiconductor Corporation where he held positions both in engineering and management. In 1988 he joined the IBM microelectronics division where he has worked in the reliability physics and modeling of Advanced Bipolar, CMOS and Silicon Germanium BiCMOS technologies. He has been the team leader for the qualification of several of IBM's leading edge CMOS and SiGe technologies. He holds 9 patents, one trade secret, has published more than 65 papers and delivered 4 tutorials at the IEEE's International Reliability Physics Symposium.

Dr. Guarín is an IEEE Fellow, Distinguished Lecturer for the IEEE Electron Devices Society, a member of the IEEE EDS AdCom and Education Committees. He is the past Chair for the Electron Devices Society in the IEEE's Mid-Hudson Valley Chapter, and past president of the Society of Hispanic Professional Engineers SHPE for the Mid Hudson Valley Region.

Once again, I welcome the new editor and wish him success. Please contact your respective Regional Editor directly with news items. A listing of EDS Regional Newsletter Editors is available on page two of this publication.

Ninoslav D. Stojadinovic
EDS Newsletter Editor-in-Chief
University of Nis
Nis, Serbia

EDS Members Named Recipients of 2011 IEEE Technical Field Awards

Seven EDS Members were among the recipients of the 2011 IEEE Technical Field Awards:

David J. Frank and **Steven E. Laux** of IBM T.J. Watson Research Center, Yorktown Heights, New York, USA, have been named two of the three co-recipients of the 2011 IEEE Cledo Brunetti Award. The citation states, "For contributions to the fundamental understanding of the physics, design and scaling of nanosized electronic devices."

The insight provided by Massimo V. Fischetti, David J. Frank and Steven E. Laux in understanding the physical effects that occur in electronic devices at small dimensions has been key to silicon technology evolving at a rapid pace. Their collective work on the development and application of modeling and simulation tools over the past 20 years has provided guidance during the early stages of the design cycle, reducing R&D costs for future nanotechnology. Drs. Fischetti and Laux developed the full-band Monte Carlo simulation program DAMOCLES, which shed light on the physics governing electron transport in semiconductor devices. The tool is considered the gold standard for device modeling with its ability to capture realistic physical properties in small silicon transistors, explaining key phenomena and suggesting new directions for research. Drs. Fischetti, Frank and Laux demonstrated 30-nm gate lengths in silicon transistors in 1992, at a time when industry thought it difficult to scale to transistor gate lengths below 100 nm. With impact still being felt today, their work sparked worldwide interest in pursuing the double-gate transistor structure as the ultimately scaled silicon transistor. A Fellow of the American Physical Society,

Dr. Fischetti is the Texas Instruments Distinguished Chair in Nanoelectronics with the Materials Science and Engineering Department at the University of Texas at Dallas. AIEEE Fellows, Drs. Frank and Laux are research staff members at the IBM T.J. Watson Research Center, Yorktown Heights, New York.

Judy L. Hoyt and **Eugene A. Fitzgerald** of the Massachusetts Institute of Technology, Cambridge, Massachusetts, USA, have been named the recipients of the 2011 IEEE Andrew S. Grove Award. Their citation states, "For seminal contributions to the demonstration of Si/Ge lattice mismatch strain engineering for enhanced carrier transport properties in MOSFET devices."

Judy L. Hoyt and Eugene A. Fitzgerald, researchers whose groundbreaking contributions involving strained silicon semiconductor materials has enabled the continued shrinking of integrated circuits and faster chips and devices, are being honored by IEEE with the 2011 IEEE Andrew S. Grove Award. IEEE is the world's largest technical professional association.

The award, sponsored by IEEE Electron Devices Society, recognizes Hoyt and Fitzgerald for seminal contributions to the demonstration of silicon germanium (SiGe) lattice mismatch strain engineering for enhanced carrier transport properties in metal-oxide field-effect transistor (MOSFET) devices. The award will be presented on 6 December 2011 at the IEEE International Electron Devices Meeting in Washington, D.C.

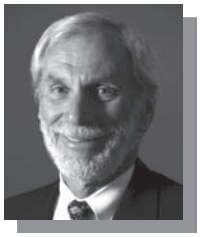
Utilizing materials breakthroughs involving the joining of Si and SiGe and the creation of strained silicon developed by Fitzgerald in 1990, Hoyt and colleagues at Stanford pioneered the application of such strained silicon to increase carrier transport properties in Si MOSFETs. Hoyt demonstrated that MOSFETs based on strained silicon have improved drive current due to higher electron mobility (lower resistance) in the transistor channel. Strained silicon transistors lower energy consumption and enable faster circuits. The work of Hoyt and Fitzgerald inspired the use of strained Si technology in mainstream devices, technology that has been key to the further shrinking/scaling of integrated circuits. Strained Si was behind the industry's 2003 release of the 90-nm generation of semiconductor technology, which featured a 50% shrinkage in size and 30% improvement in performance, and subsequent generations have continued to rely on its performance-boosting capabilities.

In 1992, working with Jeff Welser and James Gibbons at Stanford University, Hoyt demonstrated for the first time the use of strain to enhance current drive in MOSFETs. Using thin strained layers of Si on top of a relaxed SiGe artificial substrate, a materials technique pioneered by Fitzgerald, Hoyt demonstrated fully functioning strained-channel MOSFETs. Hoyt also showed that strain substantially improves very short channel MOSFETs and demonstrated, with Ken Rim, the first deep-submicron strained-channel devices. This showed the potential for the strain-engineered high-performance MOSFETs and inspired industry to develop approaches to harness strain in modern Si integrated circuits.

It was Fitzgerald's development of high-mobility strained silicon using low-defect relaxed SiGe on silicon in 1990 that spurred Hoyt's work. Fitzgerald was able to solve defect-formation problems to allow the joining of Si and Ge. He then demonstrated that highly strained materials could be deposited in small areas or, alternatively, strain-free SiGe could be deposited over large areas with a very low defect density. The ability to engineer highly relaxed and highly strained levels on Si led to Fitzgerald creating the first high-quality strained Si material and measuring the first high-mobility strained Si with his colleague Ya-Hong Xie at AT&T Bell Laboratories. Fitzgerald's breakthrough work on compressive strain in SiGe and Ge defined the upper limits of hole mobility enhancements in long-channel MOSFETs in the SiGe materials system.

An IEEE Fellow, Hoyt is also a member of the American Physical Society. Her awards include the IEEE Paul Rappaport Award and the IEEE George E. Smith Award. She received her bachelor's degree in physics and applied mathematics from the University of California, Berkeley and her doctorate in applied physics from Stanford University, Calif. Hoyt is Professor of Electrical Engineering and Computer Science at the Massachusetts Institute of Technology (MIT), Cambridge, and associate director of MIT's Microsystems Technologies Laboratories.

An IEEE Member, Fitzgerald is the recipient of the IEEE George E. Smith Award. He received his bachelor's degree from the Massachusetts Institute of Technology, Cambridge and doctorate from Cornell University, Ithaca, New York, both in materials science and engineering. Fitzgerald is the Merton C. Flemings-Singapore MIT Alliance Professor of Materials Engineering with the Massachusetts Institute of Technology.



Ronald E. Reedy of Peregrine Semiconductor, San Diego, California, USA, has been named a co-recipient of the 2011 IEEE Daniel E.

Noble Award for Emerging Technologies. His citation states, "For basic research and development of silicon on sapphire technology culminating in high-yield, commercially viable integrated circuits."

The persistence and contributions of Mark L. Burgener and Ronald E. Reedy overcame barriers to make silicon on sapphire (SOS) technology commercially feasible for wireless communications. Drs. Burgener and Reedy stood by SOS technology that, despite great promise, had initially been abandoned by semiconductor market leaders. First discovered during the 1960s, SOS technology presented manufacturing problems that prevented companies from pursuing commercialization. The efforts of Drs. Burgener and Reedy during the 1980s and 1990s overcame these obstacles, making SOS commercially viable for producing integrated circuits with improved speed, lower power consumption and more isolation compared to bulk silicon circuits. Even after demonstrating viable SOS circuits, the pair had to erase the stigma associated with the earlier problems. They co-founded Peregrine Semiconductor in 1990 to spur their commercialization efforts. They developed the UltraCMOS process, which solved critical manufacturing issues and made SOS cost-effective. After an initial shipment of 100 chips in 1995, today Peregrine has sold over 500 million UltraCMOS integrated circuits. Both IEEE Members, Dr. Burgener is vice president of advanced research and Dr. Reedy is the chief operating officer at Peregrine Semiconductor Corporation, San Diego, California.

Willy Sansen of Katholieke Universiteit Leuven, Leuven, Belgium, has been named the recipient of the 2011 IEEE Donald O. Pederson Award in Solid-State Circuits. His citation states, "For leadership in analog integrated circuit design."

Willy Sansen has provided the leadership necessary to establish analog integrated circuits as a crucial component of the microelectronics industry. Focusing on the design of analog integrated circuits, Dr. Sansen grew his research group (ESAT-MICAS) at the Katholieke Universiteit Leuven, Belgium, into one of Europe's largest and best known. Designs originating from his group have been incorporated by companies worldwide for use in chips for wireless communications, consumer electronics and sensors for cochlear implants and telemetry systems. Dr. Sansen was a pioneer of using computer tools for symbolic analysis of circuits, providing greater insight during the design process compared to purely numerical analysis methods. Known for excellence in teaching and the ability to inspire, his doctorate students have progressed to hold highly regarded positions in both industry and academia worldwide. His collaborative efforts with industry have also resulted in successful spin-off companies. An IEEE Life Fellow, Dr. Sansen is Professor Emeritus at the Katholieke Universiteit Leuven.

John D. Cressler of Georgia Institute of Technology, Atlanta, Georgia, USA, has been named the recipient of the 2011 IEEE Leon K. Kirchmayer Graduate Teaching Award. His citation states, "For inspirational teaching and student mentoring in the field of advanced microelectronic devices and circuits."

John D. Cressler believes that today's engineering students require more than just a strong technical background in the traditional core courses, so he includes unique design experiences within his courses so that students gain exposure to real-world challenges. As a result, his graduate students enter the professional world both technically strong and, importantly, aware of the social implications of the technology they develop. Considered a leading expert in silicon-germanium heterojunction bipolar transistor technology, Dr. Cressler instills his passion for social awareness within his students, examining both the positive and negative aspects of the micro- and nanoelectronics revolution and inspires them to use technology to help build a better world. He also serves as faculty mentor for Georgia Institute of Technology's SURE program, which incorporates top-notch minority undergraduates into research teams for an early taste of what graduate school is really like. An IEEE Fellow, Dr. Cressler is currently the Ken Byers Professor of Electrical and Computer Engineering at Georgia Institute of Technology.

Marvin H. White
EDS Vice President of Awards
Ohio State University
Columbus, Ohio, USA

IEEE Nanotechnology Council Announces 2011 Award Winners

IEEE Nanotechnology Council Awards Committee (Chaired by Prof. James E. Morris) announced the 2011 winners for the IEEE Nanotechnology Pioneer Award, IEEE NTC Distinguished Service Award and IEEE NTC Early Career Award. These awards will be presented at IEEE NANO 2011 in Portland, Oregon, in August 2011.

Nanotechnology Pioneer Award

The NTC Pioneer Award in nanotechnology is to recognize individuals who by virtue of initiating new areas of research, development or engineering have had a significant impact on the field of nanotechnology. The winners of the 2011 award are:

Professor Alexander A. Balandin, University of California, Riverside

"For pioneering contributions to nanoscale phonon transport with applications in nanodevices, grapheme devices, thermoelectric and thermal management of advanced electronics" and

Dr. Meyya Meyyappan, NASA Ames Research Center, Moffett Field, California

"For carbon nanotube application development and leadership in nanotechnology"

Distinguished Service Award

The purpose of the Distinguished Service Award is to recognize an individual who has performed outstanding service for the benefit and advancement of the IEEE Nanotechnology Council. The winner of the 2011 award is:

Professor Chennupati Jagadish, Australian National University, Canberra

"For his distinguished services in enhancing the reputation and influence of the Nanotechnology Council during his term as the President of the Council"

Nanotechnology Early Career Award

The purpose of the Nanotechnology Early Career Award is to recognize individuals who have made contributions with major impact on the field of nanotechnology. The winner of the 2011 award is:

Professor Ali Khademhosseini, Harvard-MIT Division of Health Sciences and Technology, Cambridge, Massachusetts

"For outstanding nano- and micro-engineering innovations for controlling the cellular environment for tissue engineering and regenerative medicine"

Congratulations to all the winners.

James E. Morris
2011 IEEE NRC Awards
Committee Chair
Portland State University
Portland, OR, USA

Status Report from the 2010 EDS Ph.D. Student Fellowship Winners

Agis A. Iliadis
EDS Ph.D. Student Fellowships Chair

In 2000, the IEEE approved the establishment of the Electron Devices Society Ph.D. Student Fellowship Program. The Program is designed to promote, recognize, and support graduate level study and research within the Electron Devices Society's Fields of Interest, which include: All aspects of the engineering, physics, theory, experiment and simulation of electron and ion devices involving insulators, metals, organic materials, plasmas, semiconductors, quantum-effect materials, vacuum, and emerging materials. Specific applications of these devices include bioelectronics, biomedical, computation, communications, displays, electro and micro mechanics, imaging, micro actuators, optical, photovoltaics, power, sensors and signal processing. In deference to the increasing globalization of our Society, at least one fellowship is to be awarded to students in each of three geographical regions: Americas, Europe/Mid-East/Africa, and Asia & Pacific.

In July 2010, EDS announced the 2010 Fellowship winners. The three winners were: Can Bayram, Guruprasad Katti and Jing Zhuge. The winners are pursuing distinctly different research topics for their doctoral degrees and the following are brief progress reports written by them.

Can Bayram is continuing his Ph.D. degree in Electrical Engineering at Northwestern University as an IBM Fellow and Link Foundation Energy Fellow working at Center for Quantum Devices. His research interests include development

of energy-efficient environmental semiconductor devices, exploring gap-engineered wide band gap semiconductors in pursuit of higher performance from ultraviolet towards terahertz wavelength optoelectronic devices, and novel micro/nano electromechanical systems (MEMS/NEMS), and fast electron devices. He has co-authored 25 journal articles, mostly in Applied Physics Letters, and made more than 50 scientific contributions. He is a reviewer of high impact journals including Applied Physics Letters and Optics Express. He is a member of the IEEE, SPIE, OSA, MRS, APS, AAAS, ECS, IOP, ICDD and ACS.

Guruprasad Katti has continued upon his research work in 3D ICs-Technology, Design and VLSI CAD/EDA arena during his Ph.D. work at IMEC and Katholieke Universiteit Leuven (KUL). Over the last year his major research contributions have been the development of temperature based Through Silicon Via (TSV) capacitance model in addition to the assessment of TSV technology to achieve minimum TSV capacitance. He is also analyzing the clock distribution in 3D ICs by developing in-house 3D Design infrastructure using existing 2D design tools. He would be defending his Ph.D. Thesis tentatively in September 2011.

Jing Zhuge received a B.S. degree in Physics from School of Physics, Peking University, Beijing, China, in 2006. She is pursuing her Ph.D. degree in Microelectronics and Solid-State Physics in the Institute of Microelectronics, Peking University, under the supervision of Prof. Yangyuan Wang and Prof. Ru Huang. Her research interests include the simulation and optimization of nano-scaled CMOS devices, and the experimental characterization on low frequency noise and variability, with a particular focus on gate-all-around silicon nanowire transistors.

From November 2009 to August 2010, she was a visiting researcher at the NCAIS group of IMEC, supported by the China Scholarship Council. Her project at IMEC is on the design and optimization of Tunnel FETs for low power applications, under the guidance of Prof. Guido Groeseneken and Dr. Anne S. Verhulst.

She has authored or co-authored 23 papers in international technical journals and conferences. She has been an IEEE student member since 2006.

Agis A. Iliadis
EDS Ph.D. Student
Fellowships Chair
University of Maryland
College Park, MD, USA

Congratulations to the 17 EDS Members Recently Elected to IEEE Senior Member Grade!

Takashi Ando
Kadoor Seetharama Bhat*
Christopher A. Bozada
Jeffrey Brown
Ming Cai
Kenneth Goodson
Wladyslaw Grabinski
Valerio Grassi
Lihong Jiao
Carl Pettiford
Khem Poudyal
Robert Stepenson
Yuji Suzuki*
Larry Wang
Richardt Wilkinson
Tien-Chun Yang
Xiaodong Yang*

* = Individual designated EDS as nominating entity

If you have been in professional practice for 10 years, you may be eligible for Senior Membership, the highest grade of membership for which an individual can apply. New senior members receive a wood and bronze plaque and a credit certificate for up to US $25 for a new IEEE society membership. Upon request a letter will be sent to employers, recognizing this new status. For more information on senior member status, visit http://www.ieee.org/web/membership/senior-members/status.html

To apply for senior member status, fill out an application at http://www.ieee.org/organizations/rab/md/smelev.htm

EDS Senior Member Program

Albert Wang
EDS Vice-President of Membership

The Electron Devices Society established the EDS Senior Member Program to both complement and enhance the IEEE's Nominate-a-Senior-Member Initiative and make IEEE/EDS members aware of the opportunity and encourage them to elevate their IEEE membership grade to Senior Member. This is the highest IEEE grade for which an individual can apply and is the first step to becoming a Fellow of IEEE. If you have been in professional practice of 10 years, you may be eligible for Senior Membership.

New Senior Members receive an engraved wood and bronze plaque and a credit certificate for US$25 to be used towards a new IEEE society membership. Upon your request, the IEEE Admission & Advancement Department will send a letter to your employer recognizing this new status as well. The URL to request this letter is http://www.ieee.org/web/membership/senior-members/notification.html.

As part of the IEEE's Nominate-a-Senior-Member Initiative, the nominating entity designated on the member's application form will receive US$10 from IEEE for each application approved for Senior Member grade when there are at least five approved applications. As an EDS member, we would appreciate it if you could indicate on your Senior Member application form that EDS is your nominating entity.

Please be aware that even if you decide to list EDS as your nominating entity, you still need to have an IEEE member nominate you along with two other references. Your nominator and your references all must be active IEEE members holding Senior Member, Fellow or Honorary Member grade.

For more information concerning Senior Membership, please visit http://www.ieee.org/membership_services/membership/senior/senior_requirements.html. To apply for Senior Member grade, please complete an application form, which is available at http://www.ieee.org/membership_services/membership/senior/senior_application.html. You can also request a hard copy Senior Member packet via mail or fax by contacting IEEE Admissions and Advancements Department, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331 USA, Fax: +1 732 562-6528, E-mail: senior-member@ieee.org.

We strongly encourage you to apply for IEEE Senior Membership to enhance your career. At the same time, you'll be helping EDS.

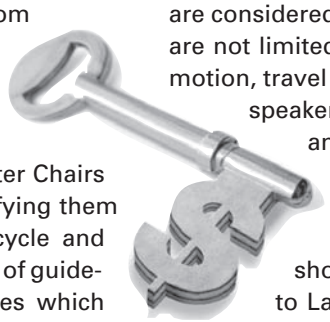
Thank you for supporting IEEE and EDS.

Albert Wang
EDS Vice-President of Membership
University of California
Riverside, CA, USA

EDS Chapter Subsidies For 2012

The deadline for EDS chapters to request a subsidy for 2012 is September 1, 2011.

For 2011, the EDS AdCom awarded funding to 76 chapters, with most amounts primarily ranging from US$250 to US$1,000. In June, Chapter Chairs were sent an e-mail notifying them of the current funding cycle and providing them with a list of guidelines. In general, activities which are considered fundable include, but are not limited to, membership promotion, travel allowances for invited speakers to chapter events, and support for student activities at local institutions.



Subsidy requests should be sent via e-mail to Laura J. Riello, l.riello@ieee.org of the EDS Executive Office by July 1st along with your completed chapter activity report. Final decisions concerning subsidies will be made by the EDS SRC Chairs/Vice Chairs in December. Subsidy checks will be issued by late December. Please visit the EDS website for more information: http://eds.ieee.org/chapter-subsidy-program.htm.

The IEEE Electron Devices Society and its Program for Young Professionals

Ravi Todi
EDS GOLD
Committee Chair

EDS GOLD Committee

The EDS GOLD AdHoc Committee is dedicated to better serving students and young professionals. This committee strives to:

- better serve the needs of students and recent graduate professionals
- get young members involved in society activities
- effectively bridge the gap between student, GOLD and senior members
- increase and provide sustained membership growth
- help young professionals with career opportunities within EDS' field of interest

The committee (when fully formed) will be composed of 20 members, with 14 serving on technical subcommittees, 1 student representative, and 1 representative serving on each of the following existing standing committees:

- Educational Activities
- Meetings
- Membership
- Publications
- Regions/Chapters

EDS Student/GOLD Ambassador Lecturer Program

The Student/GOLD Ambassador Program is a joint initiative from EDS GOLD and Education committees. The key objectives of this program are to increase student branch chapters and provide sustained growth in membership by better serving the needs of students and young professionals.

One ambassador will be appointed for each of the five following geographical areas (same as subcommittees for Regions/Chapters): North America East (Regions 1–3 & 7); North America West (Regions 4–6); Europe, Middle-East & Africa (Region 8); Latin America (Region 9); and Asia & Pacific (Region 10). More details on this program are to be made available on the EDS web page in the future.

IEEE Electron Devices Society Early Career Award

EDS approved the establishment of an Early Career Award, at its June 2008 AdCom Meeting, and the first award was presented in 2009.

The EDS Early Career Award is awarded annually to promote, recognize and support Early Career Development within the Electron Devices Society's field of interest.

To be eligible, the candidate must be an IEEE EDS GOLD member at the time of nomination and is making contributions in an EDS field of interest area. The nominator must be an IEEE EDS member. Previous award winners are ineligible. A stipend of US$1,000, a certificate; and if needed, travel expenses not to exceed US$1,500 for a recipient residing in the US and not to exceed US$3,000 for a recipient residing outside the US to attend the award presentation at the annual EDS GOLD Lecture held in conjunction with the IEEE International Electron Devices Meeting (IEDM).

Any initiative is only as successful as volunteers make it. So if you are interested in becoming active and get involved with any of these new initiatives, please contact me immediately. Please send me an e-mail indicating what you would like to be involved with, including your short bio. If you are interested in serving on the GOLD Committee, you will be expected to attend at least one meeting a year, and typically there is no financial support available to attend this meeting. For any additional information, please contact Ravi Todi (rtodi@ieee.org).

Ravi M. Todi
EDS GOLD Committee Chair
IBM Microelectronics
Hopewell Junction, NY, USA

IEEE EDS Distinguished Lecturers Participate in the Mini-Colloquium Held at the University of California, Riverside

An IEEE Electron Devices Society Mini-Colloquium on Microelectronics was held, April 11, 2011, at the University of California, Riverside (UCR). It was held jointly with the 3rd IEEE Student Research Symposium at UCR (ISRS-UCR), a student-run research symposium at UCR, which provides an interactive forum for both undergraduate and graduate students to share their research experiences and outcomes. The events were organized by the IEEE Electron Devices Society UCR Student Branch Chapter, and jointly sponsored by EDS and UCR.

The MQ featured lectures by three IEEE Distinguished Lecturers: Prof. Ya-hong Xie (UCLA) discussed

Attendees, lecturers and organizers at the MQ site

Best Student Paper Winners and EDS Judges

Prof. Stephen Parke (right) evaluating student posters

Prof. Xie (right) in discussion with student a author

"Critical Assessment of Graphene for FET Applications," Prof. Stephen Parke (Northwest Nazarene University) lectured on "Quest for the Ultimate Nanoscale Silicon CMOS Transistor," and Dr. Ravi Todi (IBM) presented "Advanced CMOS Process Integration: looking beyond conventional scaling." Another EDS DL who planned to attend, Prof. Mikael Ostling from KTH Royal Institute of Technology, Sweden, was unfortunately not able to make it to the MQ due to a last minute glitch back home.

The EDS MQ was followed by the 3rd ISRS-UCR, which drew about twenty graduate student papers and forty undergraduate student papers for poster presentations. Our EDS DL speakers also served as the judges to select the Best Student Paper winners. The events were well received by more than seventy attendees who enjoyed both the presentations and the interactions with our DL speakers and student presenters.

Hui Zhao
ED UCR Chapter Chair
University of California, Riverside
Riverside, CA, USA

Report on the 26th WIMNACT Held in Tianjin, China

The 26th Workshop and IEEE EDS Mini-colloquium on NAnometer CMOS Technology (WIMNACT) was held, December 29, 2010, at the School of Electronic Information Engineering (EIE), Tianjin University, China. This was a follow-up event to the 21st WIMNACT for the joint Peking and Tsinghua Universities' Student Branch Chapters held January 7, 2010, at which it was decided to

WIMNACT-26 speakers and participants (front row, from right): Tian-Ling Ren (2nd), Jianguo Ma (4th), Xing Zhou (5th), Guoxuan Qin (6th)

organize similar activities in the Beijing/Tianjin area. The WIMNACT was hosted by Prof. Jianguo Ma, Dean of the School of EIE at Tianjin University, who is also working on forming a new ED chapter at the university. Prof. Tian-Ling Ren of Tsinghua University (ED Beijing Chapter Chair) and Prof. Xing Zhou of Nanyang Technological University (Chair, SRC-AP), both EDS Distinguished Lecturers, participated in the event.

After introducing the audience to IEEE and EDS benefits, Prof. Zhou gave a DL on "*Unified Regional Modeling Approach to MOS Compact Modeling*," followed by the DL of Prof. Ren on "*On-Chip Integrated Magnetic Micro-Inductor for RFIC*." A third talk was given by Prof. Guoxuan Qin of the School of EIE entitled, "*High Speed Flexible Electronics Based on Single-Crystalline Nanomembranes.*" The half-day event concluded with a talk by Prof. Ma on "*Investigating the Global Trend of Semiconductor Industry by Reviewing the Digital-Analog Converters*." It was a very fruitful event and it was agreed to continue organizing such joint events in the Beijing/Tianjin area to promote EDS activities.

Xing Zhou
Nanyang Technological University
Singapore

Tian-Ling Ren
Tsinghua University
Beijing, China

Jianguo Ma
Tianjin University
Tianjin, China

Report on the 27th WIMNACT and TJNWND 2011

The 27th WIMNACT was held at Tokyo Institute of Technology, Yokohama, Japan, February 9, 2011, and jointly organized by the IEEE ED Taipei and Japan Chapters. The event was sponsored by the ED Japan Chapter, Co-sponsored by Global COE Photonics Integration-Core Electronics (PICE) and Frontier Research Center, Tokyo Institute of Technology, with technical co-sponsorship by IEEE EDS.

After the introduction of EDS by Dr. S. Kimura, ED Japan Chapter Chair, Prof. H. Iwai of TIT, Japan, gave an introductory talk, "Future of Nano CMOS Technology," followed by the following six lectures:

- "The future of Nanoelectronics by Scaling of CMOS and Functional Diversification," by Dr. S. Delelonibus, Leti, France
- "SOI opportunities to speed up, save energy and memorize," by Prof. S. Cristoloveanu, IMEP, GPI, France
- "The Case for Modeling and Simulation," by Prof. C. Fiegna, University of Bologna, Italy
- "Advanced simulation of nano-transistors," by Prof. F. Gamiz, University of Granada, Spain
- "Methods for Improving Electrical Properties of La2O3-based Gate Dielectric Films" by Prof. H. Wong, City University of Hong Kong
- "Memory Effects in SOI-FinFET with ONO Buried Insulator," by Prof. J-H Lee, Kyungpook National University, Korea

Finally, Prof. C., K. Sarkar, Jadavpur University, India, spoke on "Nano-Electronic Devices based on Silicon MOS Structure" and closed the MQ with a summary of the 8 lectures. It was a very good opportunity for speakers and audience, coming from 8 countries, to get together and discuss the frontier of Nano CMOS technology.

TJNWND 2011 (Taiwan Japan Workshop on Nano Devices 2011; Joint MQ between Taipei and Japan Chapters) was held at Tokyo Institute of Technology, Yokohama, Japan, March 3, 2011, and co-organized by NCS Taiwan, JST, Japan. This workshop was also held as an IEEE EDS Mini-Colloquium, co-organized by the ED Taipei and Japan Chapters, with co-sponsorship by Global COE Photonics Integration-Core Electronics (PICE) and Frontier Research Center, Tokyo Institute of Technology.

Opening Remarks were given by Dr. W-C Chang, Deputy Minister, NSC, and Mr. A. Takamatsu, Executive Director, JST. The introduction of the Taipei and Japan Chapters was given by Prof. E. Chang, NCTU, and Prof. A.

Toriumi, University of Tokyo, followed by 7 talks:

- "High Performance Green Electronic Devices on Glass/Plastics," by Prof. A. Chin, NCTU, and Dr. T. Kanayama, AIST
- "III-V MOSFETs for Next Generation-Fabrication of III-V MOS Capacitor," by Prof. E. Chang, NCTU and Prof. H. Iwai, TIT
- "Nanoparticle-based Plasmonic Devices," by Prof. S-Jr Gwo, NTHU, and Prof. H. Sugimura, Keio University
- "Au-in-Ga2O3 peapod nanodevices and their plasmonic application," by Prof. L-J Chou, NTHU, and Prof. M. Suzuki, Kyoto University
- "Nano-photonic devices for manipulation of light," by Prof. S-C Wang, NCTU, and Prof. Koyama, TIT
- "Understanding Optoelectronic Nano-Devices Composed of Organic Molecules and Polymer Materials" by Prof. W-G Diau, NCTU and Prof. N. Ohta, Hokakido University
- "Development of nano-devices based on carbon nanofibers/nanotubes for sensing and optoelectronic applications," by Prof. Y-Y Li, NCCU and Prof. H. Fujita, University of Tokyo

Forty-five poster presentations were given within a 2 hour period, with Mr. H. Sano and Mr. S. Sato, both from TIT, receiving best poster awards. Wrap up speeches were given by Professors. E. Chang and H. Iwai. This workshop/MQ was an excellent way for the leading researchers in Taiwan and Japan to share their research results and for the opportunity to have these discussions in front of so many young researchers and students.

Hiroshi Iwai
IEEE Division I Director
Tokyo Institute of Technology
Yokohama, Japan

Shinichiro Kimura
ED Japan Chapter Chair
Hitachi, Ltd., Sendai, Japan

Report on the 28th WIMNACT Held in India

The 28th IEEE EDS Mini-colloquium on NAnometer CMOS Technology (WIMNACT), was held in India and consisted of a series of three EDS Mini-Colloquia (MQ) with invited EDS Distinguished Lectures. The MQs were organized by the IEEE ED/AP Bombay Chapter at IIT Bombay, College of Engineering Pune and IIT Madras. These MQs followed soon after the EDS South Asia Chapters Meeting held in Mumbai, India.

MQ-1 at IIT Bombay

The first in the series of MQs was organized by the IEEE AP/ED Bombay Chapter and co-hosted by the Department of Electrical Engineering, Indian Institute of Technology, Bombay, April 18, 2011, at the IIT Victor Menezes Convention Center. Prof. Ramgopal Rao of IIT Bombay and ED SRC Vice-Chair welcomed the DL speakers and attendees, followed by a short address by Professor Juzer Vasi, IIT Bombay.

There were 6 technical talks in the program, with Professor Renuka Jindal, EDS President, giving the first DL on "Nano FET Fluctuation Physics," beginning with an introduction to the IEEE Electron Devices Society and its benefits to members. There were more than 50 researchers, working in devices and related areas, who attended. After Prof. Jindal's presentation the remaining lecturers gave their talks:

- Professor Jason Woo, University of California Los Angeles, "Device design and optimization of nanoscale CMOS technologies"
- Dr. Chandrasekhar Narayan, IBM Research, Almaden, USA, "Nanotechnology storage"
- Dr. Vivek De, Director of Circuits Research Lab, Intel, USA, "Energy efficient designs with wide dynamic range"

A group of attendees and DL speakers at MQ-1, IIT Bombay

Attendees and DL speakers of MQ-2 paused under the shades of a banyan tree on the COEP campus

DL speakers Guido Groeseneken, Renuka Jindal and M. K. Radhakrishnan (back row, 2nd, 3rd and 4th from left) with the attendees of MQ-3 at IIT Madras

- Dr. Jakub Kedzierski, MIT Lincoln Labs, "The world's most successful nanotechnology – silicon CMOS – and its future"
- Dr. M. K. Radhakrishnan, NanoRel, "Challenges in nanoscale fault localization and analysis in advanced CMOS devices"

MQ-2 at COE Pune

The second mini-colloquium in this series, organized by the IEEE AP/ED Bombay Chapter, was held at one of the oldest and prestigious engineering colleges in India at Pune, on the campus of the College of Engineering Pune (COEP), April 19, 2011. The full-day program featured 6 lectures and was attended by more than 140 participants, including faculty and students from various engineering colleges in Pune, as well as engineers and managers from industry and research institutions. The felicitation function at the start of the event was presided over by Professor Sahasrabudhe, Director of COEP, with Professor Arun Chandorkar of IIT Bombay introducing the DL team and Renuka Jindal, the President of EDS who described the mission and vision of the IEEE ED Society.

The program began with the Distinguished Lecture by Professor Renuka Jindal, EDS President and Professor at the University of Louisiana at Lafayette, USA, on "From millibits to terabits per second and beyond – over 60 years of innovation." The program continued with Distinguished Lecturers:

- Dr. M.K. Radhakrishnan, NanoRel-Technical Consultants, "Challenges in nanoscale fault localization and analysis in advanced CMOS devices"
- Dr. Jakub Kedzierski, MIT Lincoln Labs, "The world's most successful nanotechnology – silicon CMOS – and its future"
- Professor Arun Chandorkar, IIT Bombay, "Process variability and its influence on circuit parameters of scaled down MOS structures"
- Professor Maryam Shojaei, IIT Bombay, "Aspects of system integration in CMOS-based nano scale technologies"
- Professor Jason Woo, UCLA, USA, "Graphene channel MOSFETs for VLSI, is it for real"

The interaction with participants was very encouraging, initiating short technical discussions during the break.

MQ-3 at IIT Madras

The Mini-colloquium held at the Indian Institute of Technology Madras, April, 20, 2011 was jointly organized

by the new IEEE ED Madras Chapter and IEEE AP/ED Bombay Chapter. The event hosted by IIT Madras was the first of its kind organized by the ED Madras Chapter. Professor Amitava Dasgupta of IIT Madras welcomed the DLs and the gathering at the IC & SR Auditorium of IIT and Dr. Mohankumar, ED Madras Chapter Chair, briefed the audience on the formation of the new chapter.

Three DL talks were given beginning with Dr. Renuka Jindal, University of Louisiana at Lafayette USA, on "NanoFET Fluctuation Physics," followed by Dr. Guido Groeseneken, IMEC, Belgium, on "Trends and Perspectives for Electrical Characterization and Reliability Assessment in Advanced CMOS Technologies." The third talk was given by Dr. M. K. Radhakrishnan, NanoRel, on "Challenges in Nanoscale Fault Localization & Analysis in Silicon CMOS Devices." More than 40 people, including faculty members and students, attended the lecturers. In the afternoon there was an interaction session in which the EDS President and the other Distinguished Lecturers answered questions by the attendees, especially on career prospects in the electron devices area, as well as technical aspects including new technology developments and research prospects.

M. K. Radhakrishnan
EDS Region 10 SRC Vice-Chair
NanoRel
Bangalore, India

Ramgopal Rao
EDS Region 10 SRC Vice-Chair
IIT
Bombay, India

Report on the IEEE EDS Mini-Colloquium Held in Bogota, Colombia

On February 22, 2011, the ED Colombia Chapter held an IEEE EDS Mini-Colloquium at the Pontificia Universidad Javeriana. The total attendance was 70, mostly students. After an introductory overview of EDS, the MQ began with Dr. Fan Ren's talk on "Excimer UV Laser Process for Semiconductor Electronic and Photonic Devices." We were impressed by the resume of the speaker and great contrast with his clarity as a panelist that allowed him to reach all audience participants. He has very clear knowledge of the subject area that is at the forefront of technology.

EDS Distinguished Lecturers at Pontificia Universidad Javeriana, (left to right) Dr. Fan Ren, Dr. Subramanian Iyer and Dr. Fernando Guarin

The second talk was delivered by Fernando Guarin on, "SiGe Heterojunction Bipolar Transistor "HBT" Reliability Overview with a comparison to III-V HBT's." In addition to his extensive knowledge on the subject, the speaker gave his talk in Spanish making it easier for many of the students. The speaker's ability to adapt to the audience was admirable and motivated the participants to join the IEEE.

Dr. Robinson Pino delivered a speech titled, "High Resistivity III–V Antimonide Based Compounds: Bulk Crystal Growth and Characterization," which was very appropriate for the area of ED. The speaker showed the results beyond a judicious and systematic research methodology, by giving a clear approach on how to elaborate a doctoral thesis; very enlightening for the large group of students attending the lecture.

The session ended with Dr. Subramanian Iyer's talk, "Memory, Semiconductors and Microelectronics at IBM in the last one hundred years." Given that much of the audience was comprised of students, it was a most appropriate historical account of the development of reports up to current technology. The speaker in addition to his extensive knowledge seduced the listeners with his enthusiasm.

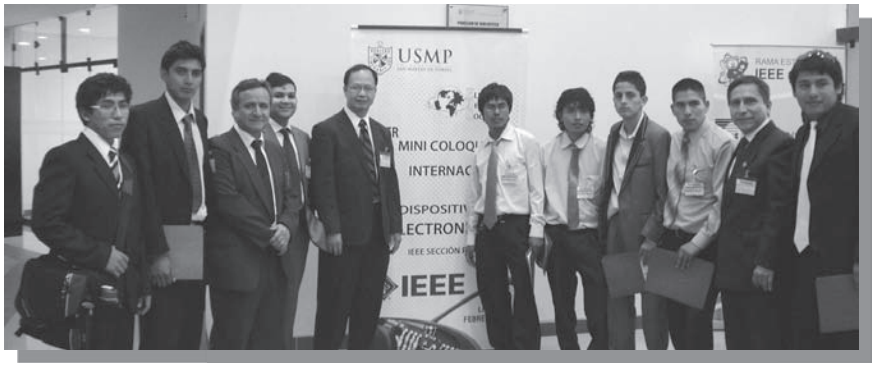
Fernando Guarin
ED Mid-Hudson Chapter
IBM Microelectronics
Hopewell Junction, NY, USA

Report on the IEEE EDS Mini-Colloquium Held in Lima, Peru

The ED Peru Chapter, founded in 2008, organized its first international IEEE EDS Mini-Colloquium, at the Engineering and Architecture Faculty of the "Universidad de San Martín de Porres" in the Capital City of Lima, Peru, February 26, 2011. The event offered valuable knowledge, with presentations by five internationally renowned IEEE EDS Distinguished Lecturers, who spoke on several topics in the EDS fields of interest.

Jorge Tejada, ED Peru Chapter Chair, opened the mini-colloquium program by welcoming the organizing assistants and sharing recent chapter activities. Fernando Guarín, Ph.D., IBM Microelectronics Research and Development Center, presented on the activities and opportunities in becoming an IEEE EDS member. Six lectures followed the opening presentations:

- "*Advanced CMOS Process Integration: Looking Beyond Conventional Scaling*," by Ravi M. Todi, Ph.D., IBM Research and Development Center
- "*Outlook and Challenge in Electrostatic Discharge (ESD) Protection of Modern and Future Integrated Circuits*," by Juin J. Liou, Ph.D., EDS Vice-President Regions/Chapters, University of Central Florida, USA
- "*Semiconductor Reliability Topics for Advanced CMOS Technologies*," by Fernando Guarín, Ph.D., IBM Microelectronics
- "*Polymeric Thin Film Transistors: A Review On Fabrication and Modeling*," by Magali Estrada, Ph.D, EDS Chair Subcommittee for Regions/Chapters-Latin America, CINVESTAV, Mexico
- "*Compact Model for Symmetric Doped Double-Gate MOSFETS New Developments*," by Antonio Cerdeira, Ph.D., CINVESTAV, Mexico.
- "*Leadership Skills for Young Engineers and Scientist in 21st Century*", was offered by Ravi M. Todi as an IEEE EDS GOLD talk.



EDS Distinguished Lecturers, Fernando Guarin, Ravi Todi and Juin Liou (3rd, 4th & 5th, from left), with some attendees

The first EDS Mini-Colloquium to be held in Peru was a successful event, with a total attendance of 105 professionals, members, students and staff. At the end of a long work day, all showed their full satisfaction with the quality of the event. The charisma and the willingness of the lecturers to share their knowledge and expectations gave the attendees the opportunity to ask questions and interact with them throughout the day.

The event was fully funded by the IEEE EDS and Universidad de San Martín de Porres.

Jorge Tejada
ED Peru Chapter Chair
Universidad de San Martín de Porres
Lima, Perú

Report on EDS Mini-Colloquium and Distinguished Lecture Programs in India

Several IEEE EDS Chapters from the eastern and southern parts of India (Calcutta, Bhubaneswara, National Institute of Science and Technology (NIST), Berhampur Student Chapter and the newly formed Madras Chapter), have shown a great interest in organizing DL and MQ programs with a motivation to spread the objective of IEEE and the Electron Devices Society. The Nano-electronics theme of these DL/MQ are trying to focus and update the state of scientific and technical knowledge among the academic and student communities and also among the people in industry. These events will give them an opportunity to enhance their understanding and knowledge so that it may be effectively utilized in their respective working domains.

DL talk at Muthayammal Engineering College (MEC), Rasipuram, Tamil Nadu

Prof. Iwai (middle, first row) DL talk at SKP Eng. College, Thiruvannamalai, Tamuil Nadu

MQ in Bhubaneswara

On December 28, 2010, the first MQ was jointly organized by the ED Bhubaneswar Chapter, the ED Calcutta Chapter and ED NIST Student Chapter, under the direction of the IEEE Calcutta Section and the ED Madras Chapter of the IEEE Madras Section. Prof. Partha Sarka, Chair of the Bhubaneswar Chapter and the Principal of the Gandhi Institute of Technology and Management, Bhubaneswar, took impressive efforts to organize the MQ and it was a great success. The event was supported by Mr. C. D Panda Chairman of the Governing Body of the GITAM, Er. P. Mishra and Prof. Jitendriya Kumar Satpathy (Vice-Chancellor BPUT). The invited speakers were Prof. Hiroshi Iwai, Tokyo Institute of Technology, Japan; Prof. Ramgopal Rao IIT Bombay, India; Prof Chandan Sarkar, Jadavpur University Kolkata, India; and Prof Mohan Kumar, SKP Eng. College, Thiruvannamalai, Tamil Nadu. The event was well attended by more than 160 participants, travelling from Bhubaneswar and beyond. All attendees received certificates to recognize their participation.

MQ in NIST Berampur

On December, 30, 2010, the ED NIST Student Chapter organized a Nano electronics themed MQ, inviting the same speakers who presented in Bhubaneswara. In addition to Prof. Majhi (NIST), Prof Ajit Panda, Dean, Academic, was the main person behind the event with full cooperation from

the College Principal, Prof S. Mudali and his administration and it too was a great success. The MQ was well attended by more than 200 academics and students, who were given recognition certificates. Prof. Panda hoped to rejuvenate the chapter with the organization of this MQ event.

DL Program in Tamil Nadu

Prof. Iwai gave several DLs during his visit to various institutes in Tamil Nadu and motivated the academic communities with his high caliber deliberations. He delivered a DL talk at Muthayammal Engineering College (MEC), Rasipuram, January 7, 2011, arranged by Dr. M. Madheswaran, Principal, MEC, Prof. K. Gunasekaran, MEC, and Prof. Mohan Kumar, SKP. Prof. Iwai also gave a DL at SKP Eng, College Thiruvannamalai, January 8, 2011.

In conclusion, the EDS chapters of eastern and southern India are working together to organize these important initiatives with the objective of expanding the IEEE EDS outreach.

Article contributions by:
Hiroshi Iwai
IEEE Division I Director

Chandan K.Sarkar
IEEE Calcutta Section Vice-Chair

Partha Sarkar
ED Bhubaneswar Chapter Chair

Ajit Panda
ED NIST Student Chapter Chair

Mohan Kumar
ED Madras Chapter

M. Madheswaran
ED India Chapter Chair

Ramgopal Rao
Vice-Chair SRC-AP

Call for Nominations - EDS Chapter of the Year Award

The EDS Chapter of the Year Award is given each year based on the quantity and quality of the activities and programs implemented by the chapters during the prior July 1st – June 30th period. Nominations for the award can only be made by Chapter Partners, SRC Chairs/Vice-Chairs, or self-nominated by Chapter Chairs.

The nomination form is available at http://eds.ieee.org/chapter-of-the-year-award.html or by contacting Laura Riello (l.riello@ieee.org) from the EDS Executive Office.

The winning chapter will receive a certificate and check for $1,000 to be presented at the IEEE International Electron Devices Meeting (IEDM).

The schedule for the award process is as follows:

Action	Date
Call for Nominations E-mailed to Chapter Chairs, Chapter Partners, SRC Chairs & SRC Vice-Chairs	6/1
Deadline for Nominations	9/15
Regions/Chapters Committee Selects Winner	Early-October
Award given to Chapter Representative at the IEDM	1st week of December

Report on the EDS South-Asia Chapters Meeting

The IEEE Electron Devices Society South-Asia Chapters Meeting was held at IIT Bombay in Mumbai, India, April 17, 2011, and hosted by the IEEE AP/ED Bombay Chapter. Most of the EDS Chapters in the South Asia region were represented at the meeting, which was lead by EDS President, Renuka Jindal. He described various activities and future plans of the Electron Devices Society, especially in the region and congratulated the Chapters for their past good performances. Two new chapters were started this past year – ED Madras and VIT Student Chapter at Vellore.

All chapter activities for the last year were reviewed, with many successful Distinguished Lecturer and Technical Talk programs organized. The ED Bangalore Chapter successfully hosted the 2011 IVEC conference, sponsored by EDS. Two chapters, the ED Bhubaneswar Chapter and NIST Student Chapter at Behrampur, which were dormant for some time, were vibrantly revived in 2010 and organized DL-MQs. The VIT Student Chapter and ED Madras Chapter had their formal

Sitting from left: Jason Woo (DL-UCLA), Mridula Gupta (Delhi Chapter), Renuka Jindal (EDS President), M.K. Radhakrishnan (Region 10 SRC Vice-Chair), Jakub Kedzierski (DL-MIT). Standing from left: Anil Kotantharayil (IITB), Partha Sarkar (Bhubaneswar Chapter), Bhadra Pokheral (Nepal Chapter) Ajit Panda (NIST Chapter), Mariam Shojaei (IITB), Sankara Reddy (Bangalore Chapter), M. Madheswaran (ED India Council Chapter), R. Ramgopal Rao (Region 10 SRC Vice-Chair), N. Mohankumar (Madras Chapter), Chandan Sarkar (Calcutta Chapter) and M. Kameswari (IITB)

inauguration by Prof. Ramgopal Rao, Region 10 SRC Vice-Chair. A closer collaboration and communication between all Chapters is planned to organize future DL-MQs and similar activities more effectively.

During April 18-20, the ED/AP Bombay Chapter organized WIMNACT-28, with three MQs: MQ-1 at IIT Bombay, MQ-2 at the College of Engineering Pune and MQ-3 at IIT Madras, with the cooperation of the ED Madras Chapter and IIT Madras. A report on WIMNACT 28 appears separately in this newsletter.

More joint activities including out-reach programs are planned for the coming years. In order to effectively utilize these programs, especially the DL Mini-colloquia, it was decided that any chapters requesting funding to the EDS Headquarters must send a copy of the request to the Region 10 SRC Chair and Vice-Chairs, as well as all other Chapter Chairs in this regional group.

M.K. Radhakrishnan
Region 10 SRC Vice-Chair
NanoRel
Bangalore, India

Regional and Chapter News

USA, Canada & Latin America (Regions 1–6, 7 & 9)

ED Mid-Hudson

Fernando Guarin, Subramanian Iyer and Ravi M. Todi

On Monday January 31, 2011, the ED Mid-Hudson Valley Chapter, New York, hosted Professor Pei-Wen Li from the Department of Electrical Engineering, National Central University, ChungLi, Taiwan, R. O. C.

Dr. Li delivered a talk entitled "Ge Quantum Dots Nano Electronics and Photonics," where she explained how the newly emerging field of zero-dimensional quantum dots (QDs), enabled by materials nanoscience and nanotechnology, has opened up access to wide-ranging applications in computing, photovolatics, photonics, as well as in energy harvesting and conversion. It was shown that among the possible materials choices for QDs, Ge-based QDs were particularly attractive since they exhibit considerable quantum confinement effect, which are much stronger than those of their counterpart Si QDs because of Ge's larger exciton Bohr radius. Thus, in principle, the electronic structure around the band gap of Ge QDs should be more easily modified than for Si QDs, making them attractive for use in advanced optoelectronics applications.

A novel, CMOS compatible approach for the generation of Ge QDs through selective thermal oxidation of SiGe-on-insulator layers was also presented. The feasibility of Ge QD single electron transistors (SETs), floating-dot memory, and photo-detecting devices were demonstrated. Her team's Ge QD SETs exhibited significant Coulomb-blockade oscillations with a peak-to-valley ratio (PVCR) of 750 and negative differential conductances with a PVCR of 12 at room temperature. Incorporating dense Ge QDs arrays into the gate dielectrics of poly-Si thin-film transistors significantly enhances the photoconductivity in the wavelength of 350–450 nm as well as the thermal stability and transient responsivity, offering potential applications for optical modulators, sensors, and switches.

On Friday, March 4, 2011, Professor Edmundo Gutierrez from the Electronics Department at the National Institute of Astronomy, Optics, Physics and Electronics (INAOE), in Puebla, Mexico, visited our EDS Chapter and delivered an engaging talk titled "Quantum confinement in nano-metric devices under a magnetic environment at room and cryogenic temperatures." He presented Experimental, theoretical, and simulation work on the electro-magnetic behavior of MOSFETs, Tri-gate FinFet's, and SiGe HBT's. Showing that the combined effect of a magnetic field B, at different operating temperatures (300 K down to 77 K), induces an extra quantum confinement in regions as narrow as 1 nm or less. This extra confinement of electrons leads to a better physical insight of the principle of uncertainty, which is observed by strong current oscillations and transmission/reflections of electrons. Under these operating conditions the electrical performance of these devices switches between a classical (analog) and quantum (digital) behavior. A hypothesis, based on wave-guide behavior device, was introduced, which serves to predict the development of a full digital semiconductor device.

~Fernando Guarin, Editor

ED Central Texas

–by Thuy Dao

The ED Central Texas Chapter held the 3rd annual 1 day Solar Technology Workshop on September 16, 2010, at Freescale Semiconductor in Austin, Texas. The workshop is dedicated to bringing together experts in the convergence area of microelectronics and solar energy and was established with the support of the IEEE Central Texas Section and Freescale Semiconductor to provide a forum for learning and for open discussion in all areas of Solar Technologies and their applications. The goals in developing this workshop are three-fold: 1) provide background understanding of the current and future solar technologies focusing on the fundamentals through invited papers and tutorials, 2) provide a forum for discussion to foster interaction and ideally generate insight to create breakthrough solutions to pressing problems, and 3) provide a venue for attendees to network with others having similar interests. The workshop was attended by 109 engineers from academia and industry. The seminars given at the workshop included:

- "Advances in Silicon PV Production Technologies" by Dr. Gopalan Rajeswaran, CEO, Moser Baer Tech. & Group Chief Tech. Officer, Moser Baer India
- "Unlocking the Potential of Distributed Generation" by Ron Van Dell, CEO, SolarBridge Technologies
- "Reliability Challenges for Solar Microinverters" by Paul Parker, Director of Product Qualification & Reliability, SolarBridge Technologies
- "A Green Campus & PV Research" by Prof. Paul Yu, Associate Vice Chancellor of Research Initiatives, University of California at San Diego
- "Overview of Konarka's Manufacturing Capability and Product

EDS President-Elect, Paul Yu, talks with attendees at the Solar Technology Workshop

Applications" by Dr. Stuart Spitzer, VP, Engineering, Konarka Technologies Inc.

- "Advanced Solar Technologies" by Dr. Betty Prince, CEO of New Energy Strategies International
- "Plan for 100 GW of Solar in the Western US" by Mark Kapner, Senior Strategy Engineer, Austin Energy
- "The University of Texas Solar Vehicles Team" by Prof. Gary Hallock and Archie W. Straiton, Endowed Faculty Fellowship in Engineering, The University of Texas in Austin

For more information on this event, please see the workshop website: http://www.ieee.org/stw. Next year's workshop is planned for September 16, 2011.

ED Phoenix

–by Charles Weitzel

Dieter Schroder Arizona State University

On Thursday, March 24, 2011, the IEEE Wave's and Devices Phoenix Chapter was delighted to have Professor Dieter Schroder give a seminar on Failure Analysis of Semiconductor Devices. Dr. Schroder has worked with semiconductor material and device electrical characterization for the last 40 years. In 1981, he joined Arizona State University, where his current interests are semiconductor devices, defects in semiconductors, semiconductor material and device characterization, low power electronics, photovoltaics and device modeling. He has written two books, Advanced MOS Devices and Semiconductor Material and Device Characterization, edited 11 books, has written over 180 papers and 10 book chapters, holds 5 patents, supervised 105 graduate students.

Prof. Schroder discussed how the first task during failure analysis is failure site location. This becomes progressively more difficult as the feature size of today's devices continue to shrink, the device structure becomes more complex, consisting of many metal layers, flip-chip bonding, etc., pushing many existing characterization tools to the limits. Hi talk gave relevant examples of a variety of techniques including: IDDQ testing, laser stimulated defect localization methods, emission microscopy, microprobing, voltage contrast, optical beam induced resistance change, and picosecond imaging circuit analysis. It also described the way in which well established techniques like mechanical probing have taken on a second life as scanning probes with submicron mechanical resolution have been developed.

ED Santa Clara Valley

–by Prasad Chaparala

Tsu-Jae King Liu Dept. of EECS, UC Berkeley

During the first Quarter of 2011, the IEEE ED Santa Clara Valley Chapter held three seminar meetings: Prof. Tsu-Jae King Liu, EECS Dept. of UC Berkeley, Dr. Glenn Alers, UC Santa Cruz and Dr. Geert Vandenberge, IMEC.

In January, Prof Liu's seminar entitled, "Mechanical Computing Redux: Relays for Integrated Circuit Applications," explained how power density has grown to be the dominant challenge for continued CMOS technology scaling. As a result, there has been renewed interest in mechanical computing, particularly for very-low-power integrated circuit applications. Her presentation began with an overview of a reliable micro-relay technology that has been developed recently at UC Berkeley. Relay-based circuit design was discussed, and demonstrations of functional relay logic circuits were presented. Finally, relay scaling for improved device density and performance was described, and the energy efficiency benefit of a scaled relay technology vs. a CMOS technology with comparable minimum dimensions was discussed.

At the February meeting, a seminar entitled "Photovoltaic Module Reliability and Failure Analysis: Enduring a storm," by Prof. Alers from UC Santa Cruz, described the challenges associated with solar panel operation over large variations in environment and weather conditions., i.e. withstanding 0–100% humidity at –20 C to 100 C with voltages in excess of 1000 V and thousands of thermal cycles. Therefore, predicting lifetime is no better than predicting the weather. His tutorial reviewed several of the qualification procedures used for assuring reliability of photovoltaic panels and the failures that result from

these tests. The wide range of indoor and outdoor failure modes were summarized along with the failure analysis techniques that are commonly used to detect the failures.

At the third meeting held in March, Dr. Vandenberghe from IMEC, Belgium, gave a talk entitled, "Lithography Options for 22 nm and Beyond." In his presentation, the status and critical challenges of multiple patterning with 193 nm immersion lithography and EUV lithography were reviewed. The scaling race according to Moore's law is continuing without any slow-down. The critical layers in 45 nm technology are done by 193 nm immersion lithography. For 32 nm, it has become quite clear that also here 193nm immersion litho will expose the critical layers, but already may require double patterning. For 22 nm, two candidates remain: Multiple patterning with 193 nm immersion lithography and all the possible resolution enhancement tricks or EUV lithography.

~Adam M. Conway, Editor

EUROPE, MIDDLE EAST & AFRICA (REGION 8)

AP/MTT/ED Portugal

The AP/MTT/ED Portugal Chapter is mainly focused on high frequency circuits and systems, with key members being engineers and university professors that work on radio frequency systems.

The group has been quite active in recent years, promoting the study of high-frequency electronic circuits by organizing several symposia and meetings; the most recent ones, IEEE MTT – International Workshop Series on "RF Front-ends for Software Defined and Cognitive Radio Solutions," held at Aveiro University, and the International Workshop on Antenna Technology – iWAT, held at the Technical University of Lisbon.

Moreover the chapter is also involved in sharing the organization of certain events, for instance some meetings are co-organized with the European Community COST Actions, where several events have been deployed in Portugal.

ED/CAS Switzerland

–by Shih-Chii Liu

Shih-Chii Liu (ED Swiss Chapter Chair)

Tobi Delbruck (ED Swiss Chapter Treasurer)

The IEEE ED/CAS Switzerland Chapter has elected two new officers. Shih-Chii Liu (http://www.ini.ethz.ch/~shih/) and Tobi Delbruck (http://www.ini.uzh.ch/~tobi/) from the Institute of Neuroinformatics, University of Zurich and ETH Zurich, are now the Chair and Treasurer of the Chapter, respectively. They replace Hanspeter Schmid, the past ED/CAS Chair and Andreas Koschak, the former Treasurer.

Hanspeter Schmid was chosen as a Distinguished Lecturer of the IEEE Circuits and Systems Society and in March 2011 gave lectures on "The Current-Mode Story" at ETH Zurich and on "Electrical and Human Feedback" at Fachhochschule NordWest Schweiz (FHNW) Windisch.

2011 IVNC

–by Soichiro Tsujino

The 24th International Vacuum Nanoelectronics Conference (IVNC 2011) will be held in Wuppertal, Germany, July 18–22, 2011, under the expert direction of Conference Chairman, Dr. Günter Müller and the IVNC International Steering Committee.

The IVNC is an important forum for actual reports and mutual discussions on the latest experimental and theoretical advances and recent developments in the field of vacuum micro and nanoelectronics. The conference topics will focus on physics, chemistry, material science and fabrication techniques of cold electron sources for novel device applications. The schedule with a four-day scientific program will consist of an invited plenary, ten oral and two poster sessions. Several awards for outstanding contributions will be given to young researchers.

For further information, visit the conference website, http://www.ivnc2011.uni-wuppertal.de/ocs/index.php/IVNC2011/IVNC2011.

~Jan Vobecky, Editor

ASIA & PACIFIC (REGION 10)

ED Peking University

–by Runsheng Wang

The ED Peking University (PKU) Student Chapter held 2 DL talks recently. On March 7, 2011, Prof. Juin J. Liou of University of Central Florida was invited to deliver a DL lecture and short course entitled "Outlook and Challenges in Electrostatic Discharge

Prof. Albert Chin (5th from right) pictured with Prof. Ru Huang (5th from left), the Chapter Advisor, Dr. Runsheng Wang (6th from right), the Chapter Chair and other members of the ED Peking Student Chapter

(ESD) Protection of Modern and Future Integrated Circuits." In this 3-hour short course, he first showed the ESD fundamentals and testing, and then presented the ESD protection designs and challenges for data communication transceivers, high-voltage IC, low-voltage RFIC, nanowire technology and organic technology. There were about 60 attendees at the talk. Afterwards, Prof. Liou shared his research experience with our chapter members and attending students.

On March 17, 2011, Prof. Albert Chin of National Chiao-Tung University delivered a DL lecture entitled "Low-Power High-Performance Logic & Memory Devices for SoC." In his talk, he shared with the audience the pioneer work of this group on small-EOT high-k, Ge CMOS, MONOS flash memory and RRAM technologies. There were about 50 attendees who engaged in a one-hour discussion with Prof. Chin after the talk.

2011 NVMTS

—by Shi Luping

The 2011 Non-Volatile Memory Technology Symposium (NVMTS 2011) will be held November 7–9, 2011, at the Shanghai Institute of Microsystem and Information Technology, CAS, (SIMIT) in Shanghai, China. The symposium will include reports on the latest research in non-volatile memory during its three-day program of speeches, invited papers and contributed papers. On November 9th, there will be a poster session aimed towards graduate students and post-doctoral researchers.

Shanghai skyline at night

This symposium fills the need for a conference that focuses on emerging nonvolatile memory technologies and advances in existing nonvolatile memory technologies, rather than on a single selected technology. The purpose of this conference is to bring together leading researchers in academia and industry with innovative technologists and investing stakeholders in order to nurture a free exchange of triumphs and challenges of a variety of technologies. We hope to provide a forum for discussing all aspects of novel memory concepts.

The conference site is 1 hour from Pudong International Airport and 15 minutes from Hongqiao International Airport directly all by subway. Attendees can make use of the city's excellent subway system to travel from the airport to the site.

ED Taipei

–by Steve Chung

The ED Taipei Chapter held an invited talk on March 23rd for Prof. Edwin Kan from Cornell University, who was visiting as the Cornell delegate to Taiwan, pursuing student exchange programs and meeting with company leaders of semiconductor corporations. The title of his talk was on "CMOS Biosensing: Lots of Problems, Lots of Opportunities." He motivated the subject by introducing very recent researches in biosensing based on CMOS technology. With mass production fast marching to 22 nm CMOS technology and beyond, we are approaching the information resolution of the biological systems such as DNA and ion channels. Many aspects of fundamental understanding on CMOS interface with bio-molecules and cells are still lacking. In his talk he addressed device operations of chemoreceptive MOS for monitoring ions, biomarker proteins, specific pathogen DNA, cellular action potentials, and exocytosis. Future directions in co-location of electrochemical and optical sensors and in nanowire membrane penetration were also introduced. The talk had 70 participants, including students and 10 professors from local universities.

There were three major events held in Taiwan:

1) The 2011 VLSI-TSA, sponsored by the IEEE EDS and SSCC was held in Hsinchu, Taiwan, April 25–27, 2011. It is the largest annual VLSI-related conference in Taiwan. It consists of two and a half days of technical paper presentations and a half-day workshop. The online paper submission deadline was October 31, 2010. For more information, please refer to http://vlsit-sa.itri.org.tw/2011/General/.
2) The 4th IEEE International Nano-Electronics Conference (INEC) was held at Chang Gung University,

The ED Taipei invited talk on March 23rd, (from the right) Prof. T-H. Hou, Seminar Chair (7th from right), Prof. Edwin C. Kan, Speaker (middle) and participating professors and student

Tao-Yuan, Taiwan, June 21–24, 2011. This major event is co-sponsored by the IEEE EDS with local EDS members organizing it. More information can be found on the conference website, http://www.inec2011.org.tw/index.html.

3) The ED Taipei Chapter assisted in organizing the EDS June AdCom Meeting Series. The three-day event consisted of the MQ series, WIMNACT-29, held at National Chiao Tung University, in the neighborhood of Science Park on May 27th and on May 28–29th the EDS AdCom Meeting Series, which included the EDS ExCom Meeting, EDS Region 10 Chapters Meeting, and EDS AdCom Meeting, all held at the Grand Hotel in Taipei.

~Mansun J. Chan, Editor

ED/SSC Bangalore

–by Sankara Reddy

The ED/SSC Bangalore Chapter organized two technical talks and one Distinguished Lecture during the first quarter of 2011. The DL by Prof. Pinaki Mazumder, University of Michigan, USA, on "Beyond CMOS Technology and Evolutionary Architectures," was attended by more than 50 people. Dr. Deepak Sekar Principal Engineer at NuPGA Corporation, USA, gave a talk on "Resistive RAM: Technology and Market Opportunities." And the third technical talk on "TCAD: Present State and Future Challenges," was delivered by Terry Ma, Engineering Vice President of Synopsys, USA.

The XII IEEE International Vacuum Electronics Conference 2011 (2011 IEEE IVEC) was organized at Bangalore by EDS and was held at JN Tata Auditorium, Indian Institute of Science, Bangalore. The conference, co-hosted by the ED Bangalore Chapter was a great success, attracting vacuum electronics researchers from all over the world. In conjunction with the conference, the IEEE EDS Vacuum Electronics Committee held its meeting at IISc.

IEEE EDS Vacuum Electronics Committee members at the 2011 IVEC

Terry Ma, with the audience of his technical talk at the ED/SSC Bangalore Chapter

ED Calcutta

–by Atanu Kundu and C.K. Sarkar

The Department of Electronics & Communication Engineering, Heritage Institute of Technology, Kolkata and the IEEE ED Calcutta Chapter jointly organized the 2011 IEEE EDS Student Paper Conference (IESPC'11) at Heritage Institute of Technology, April 18, 2011.

The IESPC is a new initiative to foster technological innovation and excellence among the Undergraduate (UG) & Postgraduate (PG) Electronics Engineering students and to encourage young engineers into research activities related to electronics engineering.

The program began with the inaugural ceremony which was graced by the presence of Prof. B. B. Paira (Director, Heritage Institute of Technology), Prof. Chandan Kumar Sarkar (Chair, IEEE EDS, Calcutta Section), Prof. Probir Roy (Executive Director, Kalyan Bharti Trust), Prof. Dulal Chandra Ray (Joint Director, HITK), Prof. Sobhen Ray (Registrar, HITK), Prof. Bhaskar Gupta (HOD, Department of E.T.C.E., Jadavpur University), Prof. Anutosh Chatterjee (Ex. Professor, HITK), Prof. Rabindranath Nandi (Department of E.T.C.E., Jadavpur University), Prof. Chayanika Bose (Department of E.T.C.E., Jadavpur University) and the faculty & staff of the Department of ECE, HITK.

The conference consisted of paper presentation in 5 tracks: Embedded Systems, Microwave Engineering,

The patron of the event, Prof. B. B. Paira, HITK, and EDS Calcutta Chair, Prof. C. K. Sarkar, displaying the IESPC'11 memento for the session chairs

Wireless Communication, VLSI and Devices and Evolutionary Computing. A total of 37 papers were presented by UG and PG students from engineering colleges across India. Five students were awarded the best paper award, one in each track. The event concluded with the valedictory session and offers of thanks by Mr. Atanu Kundu, HITK.

The conference was extremely successful in bringing together engineering students from various disciplines of ECE and electron device specialization. This platform enabled them to showcase their research work and gave them the opportunity to interact with experts in the field.

ED Delhi

–by Manoj Saxena

The ED Delhi Chapter, together with Deen Dayal Upadhyaya College, Delhi, organized a three day workshop on Frontiers of Physics, January, 21–23, 2011, at the University of Delhi, south campus. More than 300 participants from various institutions attended the 11 expert lectures at the workshop.

ED India

–by M. Madheswaran

The ED India Chapter organized a conference on Nanoelectronics, ICONE 2011, held at Muthayammal Engineering College, Rasipuram, TamilNadu, India, February, 24–25, 2011. The conference, attended by more than 150 participants, consisted of 5 invited talks and 40 paper presentations, including posters. The speakers invited were: Dr Hoe Tan, Australian National University Canberra; Dr. P. Chakraborti, Banaras Hindu University Varanasi; Dr. M.K. Radhakrishnan, NanoRel Bangalore; Dr. MykunthReddy, UNSW Australia and Dr. Mohankumar ED Madras Chapter. All participants and invitees appreciated the floral welcome spread made of different types of food grains and which used no artificial colors to match the IEEE and Society logos.

Other events organized by the Chapter included an EDS Distinguished Lecture by Prof. Hiroshi Iwai, Tokyo Institute of Technology on Nanoelectronics, January, 2, 2011 and Dr Anand Mohan of ECIL Bangalore on CMOS VLSI Analog Filters, February, 26, 2011. The Chapter sponsored a series of activities at various institutions in India, which included International Conference ICMARS 2011 at the International Center for Radio Science, Rajastan; the National Conference on Emerging Trends in VLSI at Sathyabama University, Chennai, January, 27–28, 2011, the National Seminar on Nanoelectronics at CMS Engineering College, Namakal, March, 5, 2011 and the National Conference on Electronics Technology at Goa Engineering College, April, 17–18, 2011.

ED Madras

–by N Mohankumar

The new ED Madras Chapter was formally inaugurated by Prof. Ramgopal Rao, IIT Bombay and Region 10 SRC Vice-Chair on September 24, 2010. Professors Amitava Dasgupta, Nandita Dasgupta and Enakshi Bhattacharrya of IIT Madras, as well as Prof. Chandan Sarkar of Jadavpur University, attended the function held at Hotel Accord, Chennai.

Formal inauguration of the ED Madras Chapter

ED VIT Student Chapter

–by Partha Mallick

The VIT Student Chapter, Vellore, organized a one-day training program on "Technology CAD," January 8, 2011. Mr. Amit Saini, Sr. Executive, Integrated Microsystems, Bangalore, India and Dr. Partha S. Mallick, of VIT, were the speakers who explained the theoretical and practical issues of device design using TCAD-Silvaco. Most of the participants were either from the ED VIT Student Chapter or the IEEE ED Madras Chapter.

~M.K. Radhakrishnan, Editor

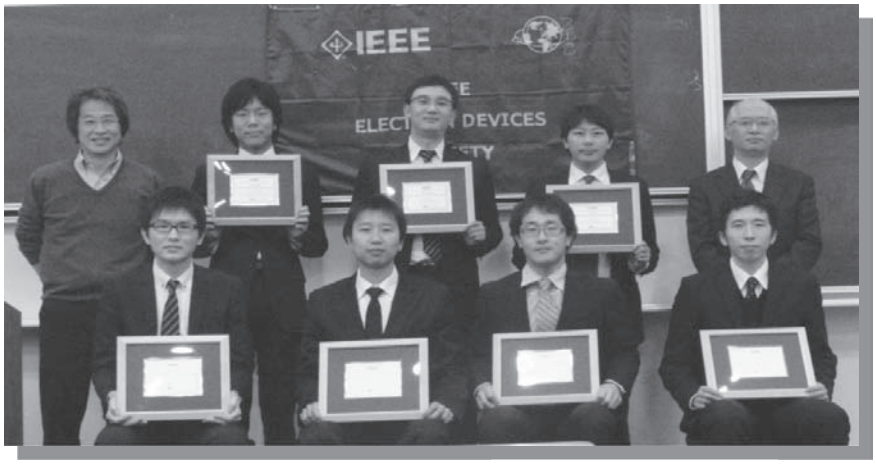
ED Japan

–by Shin'ichiro Kimura

First of all, on behalf of the IEEE ED Japan Chapter, we appreciate the heartfelt condolences to Japan and the Japanese people sent from the IEEE and Electron Devices Society.

On January 27, 2011, the annual meeting of the ED Japan Chapter was held in Tokyo. Dr. Shin'ichiro Kimura, Japan Chapter Chair reported on 2010 chapter activities and plans for 2011. At the meeting, the 2010 EDS Japan Chapter Student Award was presented to 7 students who gave excellent presentations at the IEDM or Symposium on VLSI Technology held in 2010. The award winners are posted on the Japan Chapter's homepage,

Invited Speakers and Guests in front of the 2011 ICONE floral welcome



Winners of the ED Japan Chapter Student Award

DL by Prof. John Robertson (first row, center) at Tokyo Institute of Technology, February 16, 2011

(http://www.ieee-jp.org/japancouncil/chapter/ED-15/ed15_award.htm).

The chapter meeting also included the IEDM 2010 Report, with six Japanese members of the IEDM program committee reporting on summary, topics and research trends of their committees. This report is done for the benefit of members who were not able to attend the IEDM and attendance included about sixty members and non-members.

On the evening of January 27th, the EDS Japan Chapter held an executive meeting, welcoming Mr. Matt Loeb, Staff Director and Mr. Iwao Hyakutake, Director, Japan Operations. This was a good opportunity to discuss issues, the status quo and future prospects for our chapter.

Prof. John Robertson, Cambridge University, UK, gave a DL talk at Tokyo Institute of Technology, Yokohama, February 16, 2011. His talk entitled, 'Electronic Structure of Ge:GeO_2 interfaces for future CMOS,' included his recent research results and encouraged many discussions with the audience.

ED Kansai

–by Michinori Nishihara

The ED Kansai Chapter held a feedback meeting from the 2010 IEDM at Kansai University, Kansai University Centenary Memorial Hall, Osaka, Japan, January 25, 2011, with 13 participants from academia and industries.

Dr. Hidekazu Umeda of Panasonic reported on the Quantum Power and Compound Semiconductor Devices sessions. He reported that there were no SiC papers this year and a smaller number of papers on new device structure, but pointed out there were more reliability related papers, which indicates researchers are shifting to a volume manufacturing phase. He also stated that there was a single session devoted to Graphene Devices, aiming for high frequency applications.

Dr. Toshiaki Iwamatsu from Renesas Electronics covered Si related sessions. There were more papers from industries than academia: 17 from IBM, 12 from TSMC, with Panasonic and Renesas, Japan, presenting 8 papers each. There was a single session devoted to SOI and FinFET, which coincided with the direction of the ITRS roadmap. 3D technology was also featured in a single session while HiK technology was migrated into a platform session. He noticed that there were more electrical characteristics discussions than just structure and process related matters in the 3D technology session.

After the IEDM feedback meeting we held the annual general meeting to review activities of ED Kansai in 2010 and to discuss the one for 2011. We also elected new chapter executive officers for 2011 and 2012 as follows: Dr. Akira Takahashi of Sharp Corporation, Chapter Chair; Prof. Shigehiko Sasa of Osaka Institute of Technology (OIT), Vice Chair; Dr. Hiroshi Kotaki of Sharp Corporation, Secretary and Prof. Toshihiko Maemoto of OIT as Treasurer.

~Kazuo Tsutsui, Editor

Feedback meeting from IEDM 2010 held at Kansai University on January 25, 2011

ELECTRON DEVICES SOCIETY®

Photo Courtesy of DOE/NREL

IEEE Journal of Photovoltaics

Electronic Version FREE to EDS Members

Journal of Photovoltaics (J-PV)

The IEEE *Journal of Photovoltaics* is a peer-reviewed, archival publication reporting original and significant research to advance the field of photovoltaics (PV).

The PV field is diverse in its science base ranging from semiconductor and PV device physics to optics and the materials sciences. The journal publishes articles that connect this science base to PV science and technology. The intent is to publish original research results that are of primary interest to the PV specialist.

Subject areas include *fundamentals and new concepts, crystalline, amorphous, nanostructured, and film Si, thin films, III-V, concentrator, space and organic PV, characterization, balance of systems, systems control, and systems-grid interaction.* Regular, Briefs, Review and Correspondence papers are now being accepted. Please submit your manuscripts for the *J-PV* at http://eds.ieee.org/jpv.html. The inaugural edition of the *J-PV* will be released in the summer of 2011.

IEEE
Advancing Technology for Humanity

EDS MEETINGS CALENDAR

(As of 31 May 2011)

The complete EDS Calendar can be found at our web site: http://eds.ieee.org/eds-meetings-calendars.html Please visit!

July 4 - 7, 2011, T **IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits**, Location: Songdo Conventia, Incheon, Korea, Contact: Jeongkyoung Kim, E-Mail: ipfa2011@gmail.com, Deadline: 1/17/11, www: http://www.ieee.org/ipfa

August 1 - 3, 2011, T **International Symposium on Low-Power Electronics and Design**, Location: Fukuoka Convention Center, Fukuoka, Japan, Contact: Hiroshi Nakamura, E-Mail: hiroshi@ieee.org, Deadline: 3/7/11, www: http://www.islped.org/

September 7 - 10, 2011, T **International Conference on Simulation of Semiconductor Processes and Devices**, Location: Tokyo International Exchange Center, Tokyo, Japan, Contact: Akira Hiroki, E-Mail: hiroki@kit.ac.jp, Deadline: 3/1/11, www: http://www.si.eei.eng.osaka-u.ac.jp/sispad/2011/

September 11 - 16, 2011, T **Electrical Overstress/Electrostatic Discharge Symposium**, Location: Disneyland Hotel, Anaheim, CA, USA, Contact: Lisa Pimpinella, E-Mail: lpimpinella@esda.org, Deadline: 1/14/11, www: http://www.esda.org

September 12 - 17, 2011, T **International Conference on Electromagnetics in Advanced Applications**, Location: Torino Incontra Conference Center, Torino, Italy, Contact: Roberto Graglia, E-Mail: roberto.graglia@polito.it, Deadline: 2/25/11, www: http://www.iceaa.net

September 12 - 16, 2011, T **European Solid-State Device Research Conference**, Location: Finlandia Hall, Helsinki, Finland, Contact: Tomi Mantyla, E-Mail: esscirc@utu.fi, bgt@it.utu.fi, Deadline: 4/11/11, www: http://www.essderc2011.org

September 15 - 16, 2011, T IEEE **International Siberian Conference on Control and Communication**, Location: Siberian Federal University, Krasnoyarsk, Russia, Contact: Oleg Stukach, E-Mail: tomsk@ieee.org, Deadline: 5/10/11, www: http://conf.sfu-kras.ru/sibcon

September 18 - 21, 2011, T **IEEE Custom Integrated Circuits Conference**, Location: Double Tree Hotel, San Jose, CA, USA, Contact: Melissa Widerkehr, E-Mail: melissaw@widerkehr.com, Deadline: 6/1/11, www: www.ieee.cicc.org

September 26 - 29, 2011, T **IEEE International Seminar/Workshop on Direct and Inverse Problems of Electromagnetic and Acoustic Wave Theory**, Location: PIAPMM, Lviv, Ukraine, Contact: Mykhalyo Andriychuk, E-Mail: andr@iapmm.lviv.ua Deadline: 7/10/11, www: http://www.ewh.ieee.org/soc/cpmt/ukraine/

September 27 - 28, 2011, T **Semiconductor Conference Dresden (SCD)**, Location: Technische Universität Dresden, Hörsaalzentrum, Dresden, Germany, Contact: Georg Schmidt, E-Mail: georg.schmidt@gerotron.com, Deadline: 4/4/11 www: http://www.gerotron.de/html/messen/scd.htm

September 28 - 30, 2011, T **International Conference on Solid-State Devices and Materials**, Location: Aichi Industry & Labor Center, Aichi, Japan, Contact: Shigeru Asari, E-Mail: ssdm_secretariat@intergroup.co.jp, Deadline: 5/13/11, www: http://www.ssdm.jp/

October 3 - 6, 2011, * **IEEE International SOI Conference**, Location: Tempe Mission Palms Hotel & Conference Center, Tempe, AZ, USA, Contact: Joyce Hooper, E-Mail: Joyce@imf.la, Deadline: 5/6/11, www: http://www.soiconference.org

October 9 - 11, 2011, * **IEEE Bipolar/BiCMOS Circuits and Technology Meeting**, Location: Global Learning Center, Atlanta, GA, USA, Contact: Janice Jopke, E-Mail: ccsevents@comcast.net, Deadline: 5/2/11, www: http://www.ieee-bctm.org/

October 9 - 14, 2011, T **IEEE European Microwave Integrated Circuits Conference**, Location: Manchester Central, Manchester, United Kingdom, Contact: Ian Hunter, E-Mail: i.c.hunter@ee.leeds.ac.uk, Deadline: 2/14/11, www: http://www.eumweek.com

October 16 - 19, 2011, * **IEEE Compound Semiconductor IC Symposium**, Location: Hilton Waikoloa Village, Waikoloa, HI, USA, Contact: Lisa Boyd, E-Mail: l.boyd@ieee.org, Deadline: 5/8/11, www: http://www.csics.org/

October 16 - 20, 2011, * **IEEE International Integrated Reliability Workshop**, Location: Stanford Sierra Conference Center, South Lake Tahoe, CA, USA, Contact: Rolf Geilenkeuser, E-Mail: rolf.geilenkeuser@globalfoundries.com, Deadline: 6/16/11, www: http://www.iirw.org

October 17 - 19, 2011, * **International Semiconductor Conference**, Location: Hotel Sinaia, Sinaia, Romania, Contact: Cristina Buiculescu, E-Mail: cas@imt.ro, Deadline: 6/1/11, www: http://www.imt.ro/cas

November 7 - 9, 2011, @ **IEEE International Conference on Microwaves, Communications, Antennas and Electronic Systems**, Location: David Intercontinental Hotel, Tel Aviv, Israel, Contact: Ortra Ltd., E-Mail: comcas@ortra.com, Deadline: 6/15/11, www: http://www.comcas.org

November 30 - December 3, 2011, * **IEEE Semiconductor Interface Specialists Conference**, Location: Key Bridget Marriott Hotel, Arlington, TX, USA, Contact: John Robertson, E-Mail: jr@eng.cam.ac.uk, Deadline: 7/24/11, www: http://www.ieeesisc.org/

December 5 - 7, 2011, * **IEEE International Electron Devices Meeting**, Location: Hilton Washington and Towers, Washington, DC, USA, Contact: Phyllis Mahoney, E-Mail: phyllism@widerkehr.com, Deadline: 6/24/11, www: http://www.his.com/~iedm/general/future.html

December 12 - 14, 2011, T **International Conference on Field-Programmable Technology**, Location: India Habitat Center, New Delhi, India, Contact: Kolin Paul, E-Mail: kolin@cse.iitd.ac.in, Deadline: 6/8/11, www: http://www.cse.iitd.ernet.in/~icfpt11/index.html

March 19 - 22, 2012, @ **IEEE International Conference on Microelectronic Test Structures**, Location: Catamaran Hotel, San Diego, CA, USA, Contact: Wendy Walker, E-Mail: wendyw@widerkehr.com, Deadline: 9/16/11, www: http://www.see.ed.ac.uk/icmts

April 15 - 19, 2012, * **IEEE International Reliability Physics Symposium**, Location: Hyatt Regency Orange County, Garden Grove, CA, USA, Contact: David Barber, E-Mail: dbarbsta@aol.com, Deadline: Not Available, www: http://www.irps.org

June 3 - 8, 2012, * **IEEE Photovoltaic Specialists Conference**, Location: TBD, Austin, TX, USA, Contact: Americo Forestieri, E-Mail: pvsc@wowway.com, Deadline: Not Available, www: http://www.ieee-pvsc.org

June 12 - 14, 2012, @ **IEEE Symposium on VLSI Technology**, Location: Hilton Hawaiian Village, Honolulu, HI, USA Contact: Phyllis Mahoney, E-Mail: phyllism@widerkehr.com, Deadline: Not Available, www: http://www.vlsisymposium.org


questEDS
www.ieee.org/go/questeds