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EDS WEBINAR ARCHIVE LIVE ON THE EDS SITE!

In July of 2011, EDS launched its first ever webinar. That event featured Chenming Hu of UC Berkeley giving a fascinating talk to hundreds of members about his work with FinFETs.

Since then, the EDS Webinar program has grown considerably, reaching thousands of members and non-members alike, and covering a wide range of topics and disciplines, from organic electronics to the advantages of pursuing an advanced degree in electrical engineering.

But for many busy EDS members, attending live events is not always feasible. Also, our geographic diversity is another challenge for many. Therefore, as part of our commitment to enhancing the value of membership in EDS we are pleased to present the EDS Webinar Archive. This online collection provides our members with on-demand access to streaming video of our past events... 24 hours a day, 7 days a week. Just visit <http://eds.ieee.org/webinar-archive.html>.

Please note: as this is a members-only benefit, you will need your IEEE web account login to access the Archive. If you're not an EDS member and you would like to view the content in the Archive, please consider joining today! Email us at eds@ieee.org for more info.

2013 IEEE INTERNATIONAL S3S CONFERENCE



Hyatt Regency Hotel and Spa, Monterey, California

In October 2013, an exciting new event named IEEE S3S (SOI-3D-Subthreshold Microelectronics Technology Unified Conference) will take place in Monterey, California. This industry-wide event is founded upon the co-location of two IEEE conferences which have been at the leading edge of CMOS technology: **The IEEE International SOI Conference** and the **IEEE Subthreshold Microelectronics Conference**. An additional third track on 3D Integration is also being included which will emphasize invited talks from world-renowned experts in 3D technology as well as contributed talks from leading research groups and industry.

If you wonder why these conferences have merged, the answer is straightforward: today SoCs are everything about further integration and lower power. More integration is achieved by shrinking the technology nodes trying to follow Moore's law and adding the third dimension (more than Moore). Reducing the power consumption on such advanced nodes requires designing circuits at the lowest possible power-supply voltage.

(continued on page 5)

EDS MID YEAR BoG MEETING SERIES

Our thanks to EDS volunteer Mansun Chan of the Hong Kong Univ. of Sc. & Tech. for organizing an outstanding BoG meeting series in Hong Kong. Look for in depth coverage of the event on the EDS website and in the next edition of the Newsletter.

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EDS AdCom Elected Members-at-Large

Elected for a three-year term (maximum two terms) with 'full' voting privileges

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		E. Sangiorgi	(1)		

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CONTRIBUTIONS WELCOME

Readers are encouraged to submit news items concerning the Society and its members. Please send your ideas/articles directly to either the Editor-in-Chief or appropriate Editor. The e-mail addresses of these individuals are listed on this page. Whenever possible, e-mail is the preferred form of submission.

NEWSLETTER DEADLINES

ISSUE	DUE DATE
January	October 1st
April	January 1st
July	April 1st
October	July 1st

The EDS Newsletter archive can be found on the Society web site at <http://eds.ieee.org/eds-newsletters.html>. The archive contains issues from July 1994 to the present.

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UPCOMING TECHNICAL MEETINGS

2013 IEEE COMPOUND SEMICONDUCTOR IC SYMPOSIUM (CSICS)

We cordially invite you to the 2013 IEEE Compound Semiconductor IC Symposium (CSICS) being held October 13–16 at the Portola Hotel & Spa located in beautiful Monterey, California. Over the last 35 years the Symposium has been and continues to be the preeminent international forum in which advances in semiconductor circuit and device technology are presented, debated, and discussed. The scope of the Symposium encompasses devices and circuits in GaAs, SiGe, InP, GaN, and InSb as well as RF/mm-wave and high-speed digital CMOS to provide a truly comprehensive conference. This is the ideal forum for presentation of the latest results in microwave/mm-wave, high-speed digital, analog, mixed mode, optoelectronic integrated circuits, and power conversion and connecting with industry and academic top researchers.

The 2013 CSIC Symposium is comprised of a full 3-day technical program, 2 short courses, a primer course, and a technology exhibition. The technical program typically consists of approximately 60 high quality state-of-the-art technical papers, 2–4 panel sessions, and an Industry Exhibit. The short courses, which run on Sunday, October 13th, typically provide the attendees with a unique opportunity to learn from world-renowned instructors in their respective areas of expertise. The Symposium will offer an all new

primer course, "Introduction to Si RFIC Design," an introductory-level class intended for those wishing to obtain a broad and fundamental understanding of the growing Sibased RFIC and High-Speed Analog-Mixed Signal technology. This year the Symposium will feature invited papers on a wide range of important topics encompassing device engineering to circuit application using advanced compound and other related semiconductor technologies. In addition, the Symposium will continue the tradition of including important "late breaking news" papers.

The technology exhibition will be held on Tuesday. The exhibition will feature informative and interesting displays with corporate representatives on hand. The list of exhibitors will be published and distributed in late June. To complement the Symposium, there are several social events which include the CSICS Opening



Reception, and the CSICS Exhibition Luncheon on Tuesday. Breakfasts and coffee breaks will also be served on Monday, Tuesday, and Wednesday.

The Symposium will be held at the Portola Hotel & Spa. Set against the picturesque backdrop of Monterey Bay, the Four

Diamond Portola Hotel & Spa reflects the captivating spirit of a rich, historical setting surrounded by everything that the Monterey Peninsula has to offer. Portola Hotel & Spa is the only Silver LEED-EB certified hotel on the central coast of California and boasts 379 guestrooms—including 10 suites, 50,000 square feet of meeting space with the adjacent Monterey Conference Center, an award winning full service day spa, two on site eateries, and a variety of other amenities, perfect for both group and leisure travelers. For registration and further information please visit the CSICS website at <http://www.csics.org>. Further questions may be addressed to the Symposium Chair: Francois Colomb, Phone: (978) 684-5435; E-mail: fcolomb@raytheon.com. We hope you can attend,

2013 IEEE CSICS Organizing Committee



2013 IEEE INTERNATIONAL INTEGRATED RELIABILITY WORKSHOP (IIRW)

The 2013 IEEE International Integrated Reliability Workshop (IIRW), sponsored by the IEEE Reliability Society and the IEEE Electron Devices Society, will be

held at the Stanford Sierra Conference Center on the shores of Fallen Leaf Lake near South Lake Tahoe, California, October 13–17, 2013. This workshop

provides a unique forum for open and frank discussions of all areas of reliability research and technology for present and future semiconductor applications.

Some of the highlights of this year's technical program will include:

- A keynote address given by Anthony Oates (TSMC)
- A strong collection of invited speakers including: Michael Fritze (University of Southern California), Paul Hurley (Tyndall National Institute), Luca Larcher (University of Modena), Pat Lenahan (Penn State University), William McMahon (GlobalFoundries), David Meyer (Naval Research Lab), Chandra Mouli (Micron), Ennis Ogawa (Broadcom), Guido Sasse (NXP), Jurriaan Schmitz (University of Twente), Ron Schrimpf (Vanderbilt University), Ernest Wu (IBM), and Chad Young (UT Dallas)
- A tutorial program (organized by Richard G. Southwick, III, IBM and Jim Lloyd, SUNY Albany CNSE) composed of such interesting and diverse reliability topics as lead free interconnects (Minhua Lu, IBM), the role of atomistic modeling in reliability (Franz Schanovsky, Tech. University of Wien), GaN HEMTs (Matteo Meneghini, University of Padova), and chip package interactions (Thomas M Shaw, IBM).

The IIRW is also an excellent forum to present new and original technical works. Hot reliability topics for this year's workshop include: SiGe and strained Si, III-V, SOI, high-k and nitrided SiO₂ gate dielectrics, reliability assessment of novel devices, organic electronics, emerging memory technologies (RRAM etc.) and future "nano"-technologies, NEMS/MEMS, photovoltaics, transistor reliability including hot carriers and NBTI/PBTI, Cu interconnects and low-k dielectrics, product reliability and burn-in strategy, impact of transistor degradation on circuit reliability, reliability modeling and simulation, optoelectronics, single event upsets, as well as



View from the ski dock at the Stanford Sierra Conference Center. The Stanford Sierra Conference Center provides lodging, meals and meeting facilities as well as excellent recreation including hiking in the Desolation Wilderness and boating on Fallen Leaf Lake.

the traditional topics of wafer level reliability (WLR) and built-in reliability (BIR). The Call for Papers can be found at our newly redesigned web address (www.iirw.org). The abstract submission deadline is July 12, 2013. Contact the Technical Program Chair, Tibor Grassner, TU Wien (grassner@iue.tuwien.ac.at) for further details. Also, visit www.iirw.org for continued updates about the conference. Also note that all attendees have the opportunity to present a "walk-in" poster of their latest work. This is a great way to share that new project you are working on and to get world-class feedback.

IIRW is fairly different from a typical technical conference. Located 6000 ft. high in the Sierra Nevada Mountains, the Stanford Sierra Conference Center provides an ideal atmosphere for a relaxing yet informative workshop. Nestled throughout the pines and cedars along the shoreline of Fallen Leaf Lake, attendees stay in cabins furnished in the rustic style of an alpine resort. All cabins have decks with magnificent views of Fallen Leaf Lake and the surrounding Sierra peaks. Comfortable, informal dress is encouraged, affiliations are downplayed, and meals are provided family-style in the lodge dining room.

All aspects of the workshop, including the physical isolation of the

venue, the absence of distractions such as in-room phone and televisions, and the format of the technical program encourage extensive interaction among the workshop attendees. Such opportunity is seldom available at most other conferences. Participants spend their evenings at poster sessions, discussion groups, and special interest groups, all complemented with refreshments and snacks. The evening moderated discussion groups (organized this year by Wayne Ellis, Rambus) provide a forum with unparalleled access to world experts to discuss a

wide array of relevant reliability issues. Often these discussions lead to the formation of a smaller special interest group, whose discussions extend long after the conclusion of the workshop.

The technical program is purposely kept open for Wednesday afternoon to allow attendees to enjoy a variety of the outdoor activities which the Stanford Sierra Conference Center location has to offer. These include hiking, sailing or kayaking, walking, or simply continuing that intriguing conversation from the night before. This free afternoon is a great way to not only network, but also to build long-lasting friendships.

Additional information about the workshop is available on the IIRW website at www.iirw.org, or by contacting Jason Campbell of NIST, 2013 IIRW General Chair, (jason.campbell@nist.gov). Note: If you want to take part in this event, please register early as space at the Stanford Sierra Conference Center is limited to roughly 120 attendees and the workshop has sold out in the past.

On behalf of the 2013 IIRW Committee, I look forward to meeting you in Lake Tahoe!

James Wu

*2013 IIRW Communications Chair
PMC-Sierra, Inc.
Burnaby, BC, Canada*

2013 IEEE INTERNATIONAL S3S CONFERENCE

(continued from page 1)

So all-in-all, attendees will be able to access essentially three conferences with one registration fee, covering three topics at the heart of today's semiconductor industry plans:

Silicon on Insulator (SOI) Ever increasing demand and advances in SOI and related technologies make it essential to meet and discuss new gains and accomplishments in the field. For over 35 years the SOI conference has been the premier meeting of engineers and scientists dedicated to current trends in Silicon-on-Insulator technology, including CMOS, photonics, sensors, NEMS and more. The conference will cover topics spanning from material engineering to circuits and applications, through devices and modeling. As fully-depleted devices are currently the golden choice for 16 nm and below CMOS processes, there is no better place to understand the underlying physics of FinFET and FDSOI planar devices.

3D Integration 3D Integration allows us to scale Integrated circuits "orthogonally" in addition to classical 2D device and interconnect scaling. A dedicated session will address the unique features of such stacking with special emphasis on wafer level bonding as a reliable and cost effective method, similar to the creation of SOI wafers. Fabrication techniques, bonding methods as well as design and test methodologies will be covered. Novel inter-strata interconnect schemes will also be discussed.

Subthreshold Microelectronics Ultra-low-power microelectronics will expand the technological

capability of handheld and wireless devices by dramatically improving battery life and portability. Ubiquitous sensor networks (Internet of Things), RFID tags, implanted medical devices, portable biosensors, handheld devices, and space-based applications are among those that would benefit from extremely low power circuits. One of the most promising methods of achieving ultra-low-power microelectronics is to reduce the operating voltage to below the transistor threshold voltage, which can result in energy savings of more than 90% compared to conventional low-power microelectronics.

Conference format This year, the conference will run two parallel sessions for SOI and Subthreshold Microelectronics after the common plenary session opening the conference. A joint SOI/3D technical session will focus on 3D integration. The joint poster session will give you the opportunity of an open discussion with their authors. A live panel session will gather renowned experts.

Socializing has always been a tradition. The welcome reception and cookout are excellent opportunities for people from different backgrounds to meet in a friendly atmosphere. There will be specialists from the different fields described above, representatives from established industries as well as startups, professors and scientists from universities and research institutes all over the world.

Optional classes On top of the regular sessions, the conference will offer to the attendees the possibility to follow either a one-day SOI or 3D short course as well as either a

half-day SOI or Subthreshold Microelectronics fundamental class.

Location This year, the conference will take place in the splendid Hyatt Regency Monterey Hotel and Spa, located in Monterey, California, a beautiful waterfront community on the central coast of California. This area offers breathtaking sceneries and a profusion of indoor and outdoor activities.

Important dates:

Paper submission, deadline:	May 31, 2013
Notification of acceptance:	June 30, 2013
Short course date:	October 7, 2013
Conference dates:	October 7–10, 2013

Late news papers with exceptional merit will be considered for the Late News session if submitted on or before August 23, 2013.

More details are available on the website of the conference: <http://s3s.conference.org>.

For registration forms and additional information please go to the conference website. You may also contact the conference manager, Joyce Hooper, by e-mail at manager@s3sconference.org or at the following coordinates: IEEE S3S Conference, 6930 De Celis Place, #36, Van Nuys, CA 91406 USA, Telephone: 818-795-3768, Fax: 818-855-8392.

Jean-Luc Pelloie
2013 IEEE S3S General Chair
ARM
Grenoble, France

SOCIETY NEWS

MESSAGE FROM THE EDITOR-IN-CHIEF



M.K. Radhakrishnan
Editor-in-Chief

EDS is one of the vibrant societies of IEEE with a wide field of interest and technical activities catering to the members with chapters spread all over the globe. It is an honor for me to start serving as the Editor-in-Chief (EIC) of the EDS Newsletter, which is currently in its 20th year of publishing. However, it is a challenging task to inhabit a position occupied by Prof. Ninoslav Stojadinovic during the past decade, where he transformed the Newsletter to one of the luminous magazines to cover society information.

As we all have seen, the Newsletter has progressed year by year under Nino's leadership wrapping information necessitated by the members and keeping abreast in this advanced age of communication. On behalf of all

EDS members, readers of the Newsletter and our editorial team and staff, I would like to thank Nino for the untiring dedication and effort throughout the years. A job well done. I would like to repeat Nino's words when he took over from the founding EIC, Prof. Krishna Shenai *"a difficult task to maintain the level of the Newsletter and try improving it further."*

In the first issue of EDS Newsletter in 1994, Mike Adler—then outgoing President of EDS—wrote *"the Society is on a track to grow in member technical services and become a truly global society."* Our President Paul Yu in his incoming President's message wrote in the 2012 April issue *"In EDS, our diversity is one of our greatest strengths. Our members and chapters are located in 84 countries around the globe. But this diversity also presents some significant challenges."*

Yes. Now, EDS is truly a global society. One of the challenges we all face now is to reduce the time gap

in communicating society related information to the members. As EIC one of my top priorities will be to bring the news as fast as possible and to make the Newsletter a unique window for members in line with the Society's mission.

We all—the team of Editorial Board members (Fernando Guarin, Peyman Servati, Adam Conway, Francisco Garcia Sanchez, Tomislav Suligoj, Zygmunt Ciota, Jonathan Terry, Jan Vobecky, Kuniyuki Kakushima, Mansun Chan and M.K. Radhakrishnan) and the editorial staff—are looking forward to work with all the EDS members and Chapters to achieve the key aspects of Society's mission *"to foster professional growth of its members and to enhance visibility in the field"* through our Newsletter.

M.K. Radhakrishnan
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ANNOUNCEMENT OF NEWLY ELECTED BoG (FORMERLY AdCom) MEMBERS

On December 9, 2012, the EDS BoG (formally AdCom) held its annual election of members-at-large. The following are the results of the election and brief biographies of the individuals elected.

BoG (formally AdCom) MEMBERS-AT-LARGE

A total of seven persons were elected to three-year terms (2013–2015) as members-at-large of the EDS BoG (AdCom). Five of the seven individuals were re-elected for a second term, while the other two have

joined the board for the first time. The backgrounds of the electees span a wide range of professional and technical interests.

Second Term Electees



Subramanian S. Iyer is an IBM Fellow at the Systems & Technology Group, and is responsible for technology strategy and competitiveness, embedded memory and three-

dimensional Integration. He obtained his B.Tech at IIT-Bombay, and Ph.D. at UCLA. His key technical contributions have been the development of the world's first SiGe base HBT, electrical Fuses, eDRAM and 45nm technology used at IBM and IBM's development partners. His current technical interests and work lie in the area of 3-dimensional integration for memory sub-systems and the semiconductor roadmap. He is a Distinguished Alumnus of IIT Bombay and received the IEEE Daniel Noble Medal for emerging technologies in 2012.



Meyya Meyyappan is Chief Scientist for Exploration Technology at NASA Ames Research Center in Moffett Field, California. Until

June 2006, he served as the Director of their Center for Nanotechnology. He has authored 190 articles in peer-reviewed journals and made over 200 Invited/Keynote/Plenary talks. His research interests include carbon nanotubes and inorganic nanowires, and applications in chemical and biosensors, instrumentation, electronics and optoelectronics.

Dr. Meyyappan is a Fellow of IEEE, ECS, AVS, and MRS. He is currently an EDS Distinguished Lecturer and VP for Educational Activities. For his contributions and leadership in nanotechnology, he has received: a Presidential Meritorious Award; NASA's Outstanding Leadership Medal; Arthur Flemming Award by the Arthur Flemming Foundation; IEEE Judith Resnick Award; IEEE-USA Harry Diamond Award; AIChE Nanoscale Science and Engineering Forum Award. For his sustained contributions to nanotechnology, he was inducted into the Silicon Valley Engineering Council Hall of Fame in February 2009. For his educational contributions, he has received the Outstanding Recognition Award from NASA; Engineer of the Year Award (2004) by AIAA; IEEE EDS Education Award; IEEE EAB Meritorious Achievement Award in Continuing Education.



Arokia Nathan holds the Chair of Photonic Systems and Displays in the Department of Engineering, Cambridge University. He received his

Ph.D. in Electrical Engineering from the University of Alberta. Following post-doctoral years at LSI Logic Corp., USA and ETH Zurich, Switzerland,

he joined the University of Waterloo. In 2006, he moved to the UK to take up the Sumitomo Chair of Nanotechnology at the London Centre for Nanotechnology, University College London. He has published over 400 papers in the field of sensor technology and CAD, and thin film transistor electronics, and is a co-author of four books with over 50 patents filed/awarded. He is a Chartered Engineer (UK), Fellow of the Institution of Engineering and Technology (UK), Fellow of IEEE (USA), and an IEEE/EDS Distinguished Lecturer.



Michael Shur received the MSEE degree (with honors) from LETI (St. Petersburg), Ph.D. and Dr. Sc. degrees from Lofte Institute. He is a Patricia

W. and C. Sheldon Roberts Professor, Acting Director of Center for Integrated Electronics and Director of the NSF I/UCRC at RPI. He is also co-founder and Vice-President of Sensor Electronic Technology, Inc. His area of expertise is physics of semiconductor devices. Dr. Shur is Foreign Member of the Lithuanian Academy of Sciences and Fellow of IEEE, APS, IET, ECS, MRS, and AAAS. He received IEEE and other awards, and holds an Honorary Doctorate from St. Petersburg Technical State University.



Bin Zhao received the BSEE degree from Tsinghua University, Beijing, China and the Ph.D. degree from California Institute

of Technology. He has been with SEMATECH, Rockwell International, Conexant Systems, Skyworks Solutions, and Freescale Semiconductor. His past work and experience have involved with both VLSI technology development and analog/mixed-signal/RF circuit design. Currently he is the Director of Southern California Development Center, Fairchild Semiconductor, Irvine, California,

where he leads IC design and product development for consumer electronics and mobile solutions. He has authored more than 200 journal publications and conference presentations, has written three book chapters, and holds more than 60 issued US patents. He is an IEEE Fellow, an IEEE Distinguished Lecturer, and the IEEE EDS Vice President of Conferences. He is a recipient of the ECE Reader Award (2008), the Hearst Semiconductor Applications Award (2008), and the EDN Innovation Award (2009).

First-Time Electees



Daniel Mauricio Camacho received his BSEE for Pontificia Universidad Javeriana, in Bogota, Colombia in 2007, and his

Masters degree from Southern Methodist University in Dallas, Texas in 2009. In 2008 he was awarded the IEEE EDS Masters Student Fellowship for his research work. He joined Intel in 2010, where he has been since then. His area of expertise is design of high-performance analog and mixed signal circuits. He is also the current chairman of the EDS Graduates of the Last Decade (GOLD) Committee.



Douglas Verret is Program Manager for Embedded Flash Technology in Texas Instruments, Inc., where he led the development of 0.8 um,

130 nm and 65 nm technologies and currently is Program Manager for TI's latest embedded flash project. Prior to that he led a world-wide yield improvement team, led the development of FPGA technology as well as BiCMOS and digital bipolar technologies which are used to manufacture high performance logic devices. He was assigned to SEMATECH, a Semiconductor Consortium in Austin, Texas, from 1988–1990 where he served as the Director

of Manufacturing Techniques and Standards and led the development of 0.5 um digital CMOS technology.

He has a MS in Physics (1974) from Purdue University and was a NSF Fellow. He has a Ph.D. in Solid State Physics (1978) from the University of New Orleans, was a Dana Fellow

and recognized by Sigma Xi with an award for Outstanding Graduate Research (1977). He is an IEEE Fellow, a Texas Instruments Fellow and was Editor-in-Chief of the *IEEE Transactions on Electron Devices* from 2000–2011. In 2012 he was awarded the EDS Distinguished Service Award.

I welcome all to the EDS Board and urge them to truly get engaged in the affairs of the EDS.

Renuka Jindal
EDS Nominations and Elections
Chair
University of Louisiana at Lafayette
Lafayette, LA, USA

EDS BoG (FORMERLY AdCom) MEMBERS-AT-LARGE

The IEEE Electron Devices Society invites nominations for election to its Board of Governors—BoG (formerly AdCom). The next election will be held after the BoG meeting on Sunday, December 8, 2013. This time, seven out of twenty-two members will be elected for a 3-year term, with a maximum of two consecutive terms. Electees begin their term in office on January 1, 2014. The nominees need not be present to run for the election. Self-nominations are allowed.

Any EDS member who has previously participated in EDS activities as a Standing and Technical Committee member, Vice-President, Publication Editor, Representative or Chapter Chair for a minimum of one year is eligible to be nominated. The electees

are expected to attend both BoG Meetings every year. While the December meeting is organized in connection with the IEEE International Electron Devices Meeting, the mid-year meeting is frequently held outside the US. Budgeted travel support is available to attend both of these meetings.

All nominees must be endorsed by a 'full' voting member, i.e., one of the four officers (President, President-Elect, Treasurer or Secretary), the Jr. or Sr. Past President or one of the 22 current BoG Members-at-Large. It is the responsibility of the endorser to make sure that, if elected, the nominee is willing to actively serve in the position as a BoG member. In the unlikely event that a nominee must withdraw their name from

the election ballot, they must do so by November 1, 2013.

Please send your nominee's name, address and a brief endorsement note to the EDS Executive Office, Laura J. Riello, e-mail: l.riello@ieee.org by October 15, 2013. The submissions must also include a biographical summary of the nominee in a standard two-page format. A sample of the format is available from the EDS Executive Office. If you have any questions, please feel free to contact Laura Riello (l.riello@ieee.org) with a copy to me at r.jindal@ieee.org.

Renuka Jindal
EDS Chair of Nominations & Elections
University of Louisiana at Lafayette
Lafayette, LA, USA

IEEE ANNUAL ELECTION—DID YOU VOTE YET?

This is a reminder for EDS members to vote in the 2013 IEEE Annual Election for the following positions and candidates.

Listed below are the positions and candidates that will appear on the 2013 IEEE Annual Election ballot.

Position	Candidate
IEEE President-Elect, 2014	Tariq S. Durrani (Nominated by IEEE Board of Directors) Howard E. Michel (Nominated by IEEE Board of Directors)
IEEE Region 1 (Northeastern US) Delegate-Elect/Director-Elect, 2014–2015	Ali Abedi (Nominated by IEEE Region 1) Ronald A. Tabroff (Nominated by IEEE Region 1)
IEEE Region 3 (Southern US) Delegate-Elect/Director-Elect, 2014–2015	James M. Conrad (Nominated by IEEE Region 3) John E. Montague (Nominated by IEEE Region 3) Gregg L. Vaughn (Nominated by IEEE Region 3)
IEEE Region 5 (Southwestern US) Delegate-Elect/Director-Elect, 2014–2015	Francis B. Grosz (Nominated by IEEE Region 5) Edge Nowlin (Nominated by IEEE Region 5)
IEEE Region 7 (Canada) Delegate-Elect/Director-Elect, 2014–2015	Robert L. Anderson (Nominated by IEEE Region 7) Jeremy A. Gates (Nominated by IEEE Region 7) Witold M. Kinsner (Nominated by IEEE Region 7)

IEEE Region 9 (Latin America) Delegate-Elect/Director-Elect, 2014–2015	Cesar G. Chamocho (Nominated by IEEE Region 9) Antonio C. Ferreira (Nominated by IEEE Region 9)
IEEE Standards Association President-Elect, 2014	Dennis B. Brophy (Nominated by IEEE Standards Association) Bruce P. Kraemer (Nominated by IEEE Standards Association)
IEEE Standards Association Board of Governors Member-at-Large, 2014–2015	Farooq Bari (Nominated by IEEE Standards Association) Robert S. Fish (Nominated by IEEE Standards Association)
IEEE Standards Association Board of Governors Member-at-Large, 2014–2015	Herbert S. Bennett (Nominated by IEEE Standards Association) Glenn W. Parsons (Nominated by IEEE Standards Association)
IEEE Technical Activities Vice President-Elect, 2014	James D. Isaak (Nominated by IEEE Technical Activities) Douglas N. Zuckerman (Nominated by IEEE Technical Activities)
IEEE-USA President-Elect, 2014	Peter Alan Eckstein (Nominated by IEEE-USA) James A. Jefferies (Nominated by IEEE-USA)
IEEE-USA Member-at-Large, 2014–2015	Thomas G. Habetler (Nominated by IEEE-USA) Scott M. Tamashiro (Nominated by IEEE-USA)

Balloting period starts on 15 August and ends at 12:00 noon, Central Time USA (17:00 UTC) on 1 October. All eligible voting members should look for their ballot to arrive via postal mail or access their electronically at www.ieee.org/elections. Forward election questions to corp-election@ieee.org.

2013 PVSC WILLIAM R. CHERRY AWARD WINNER



Keith Emery

This award is named in honor of William R. Cherry, a founder of the photovoltaic community. In the 1950's, he was instrumental in establishing solar cells as the ideal power source for space satellites and for recognizing, advocating, and nurturing the use of photovoltaic systems for terrestrial applications. The William R. Cherry Award was instituted in 1980, shortly after his death. The purpose of the award is to recognize engineers and scientists who devote a part of their professional life to the advancement of the technology of photovoltaic energy conversion.

This award is presented at each IEEE/EDS Photovoltaic Specialists Conference. The recipient is selected

by the William R. Cherry Committee composed of past PVSC chairpersons and past recipients of the award.

Keith Emery established and has managed the Cell and Module Performance Characterization team at NREL since 1980. The team established the procedures for calibrating cells and modules that have since been codified in standards and adopted by the international PV community. He received his B.S. physics and M.S.E.E. from Michigan State in 1979 and worked on a Ph.D. at Colorado State in 1979-1980 and 1982. His graduate thesis work was in the area of comprehensive modeling of the pulsed HF laser, electron and laser beam vapor phase epitaxy of oxides and nitrides, and ion beam sputtering of tin oxide on Si. He has 308 publications and 5 chapters in PV books to date. His ISO 17025 PV accredited calibration group provides the community

with reference cell calibrations and efficiency certification. He is also active in PV standards development and consulting on PV performance rating hardware, solar simulation, current versus voltage measurement software and procedures. He is a life time member of the Colorado Renewable Energy Society (CRES), senior member of IEEE, member of the ASTM E44 and IEC TC-82 PV standards committees. He is an associate editor of the *IEEE Journal of Photovoltaics* and on the editorial board of *Progress in Photovoltaics*, *Open Applied Physics Journal*, and *Renewable Energy*. He is co-awardee of two R&D 100 awards, and recipient of the 2007 Paul Rappaport, 2009 Harold M. Hubbard Award, and the 2012 World Renewable Energy Network Pioneer Award.

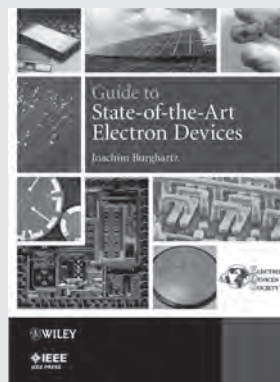
John D. Meakin
University of Delaware

EDS GUIDE TO STATE-OF-THE-ART ELECTRON DEVICES

To commemorate our 35th Anniversary, the IEEE Electron Devices Society is proud to announce the *EDS Guide to State-of-the-Art Electron Devices*.

This comprehensive full-color publication was edited by EDS Vice-President of Technical Activities, Joachim Burghartz. In addition to the foreword by Nobel Laureate and EDS Celebrated Member George E. Smith, the book contains 21 chapters by 70 contributors. A historical timeline runs throughout the book, highlighting three key time periods/eras in the electron device field.

Look for more information on the EDS website, www.ieee.org/eds.



IEEE NANOTECHNOLOGY COUNCIL ANNOUNCES 2013 AWARD WINNERS

The IEEE Nanotechnology Council Awards Committee (Chaired by Prof. James E. Morris) has announced its 2013 award winners for the IEEE Nanotechnology Pioneer Award, and the IEEE NTC Early Career Award. These awards will be presented at IEEE NANO 2013 in Beijing, China in August 2013.

Pioneer Award in Nanotechnology:

Charles M. Lieber
Mark Hyman Professor of Chemistry,

Department of Chemistry & Chemical Biology,
Harvard University, 12 Oxford Street,
Cambridge, MA 02138

"For pioneering contributions to nanometer diameter wire synthesis and applications, and defining leadership in nanotechnology."

Early Career Award in Nanotechnology:

Masahiro Nakajima
Center for Micro-nano Mechatronics,

Nagoya University, Furo-cho, Chikusa-ku,
Nagoya 464-8603 Japan

"For achievements in bio-nano-manipulation systems."

Congratulations to all the winners.

James E. Morris

2013 IEEE NTC Awards Committee

Chair

Portland State University,
Portland, OR, USA

EDS MEMBERS NAMED RECIPIENTS OF 2013 IEEE TECHNICAL FIELD AWARDS

Four EDS Members were among the recipients of the 2013 IEEE Technical Field Awards:

Giorgio Baccarani of the University of Bologna, Bologna, Italy, has been named the recipient of the IEEE Clelio Brunetti Award. The citation states, "For contributions to scaling theory and modeling of metal oxide

semiconductor (MOS) devices."

A world-renowned expert on semiconductor device physics and modeling, Giorgio Baccarani's contributions to scaling theory have been pivotal to the continued



miniaturization of electronic devices from micrometer to nanometer scales. Baccarani's generalized scaling theory published in 1984 has provided the theoretical foundations to help engineers understand earlier scaling rules for electronic components. He has provided the tools needed to predict, interpret, and understand the characteristics of miniaturized MOS

transistors. Baccarani provided one of the first transistor models where surface potential is accurately calculated using an iterative procedure. This work is considered the forerunner of today's PSP (Penn State Philips) model for simulating behavior of future MOS transistors. He also developed physical models for numerical device simulation that have been incorporated into commercial technology computer-aided design (TCAD) tools for modeling semiconductor fabrication. Baccarani also created numerical modeling techniques of electron devices in two and three dimensions. An IEEE Life Fellow, Baccarani is a professor with the University of Bologna, Italy.



John H. Lau of the Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan, has been named the recipient of the IEEE Components, Pack-

aging and Manufacturing Technology Award. The citation states, *"For contributions to the literature in advanced solder materials, manufacturing for highly reliable electronic products, and education in advanced packaging."*

One of the most well-known authors in electronics packaging, John H. Lau's leading-edge research has driven reliability improvements and advancements with his extensive research on solder-joint reliability, environmentally friendly solder alternatives, and advanced interconnect techniques. Dr. Lau led an international team to study solder-joint reliability issues and published the first book on the subject in 1991. He published additional influential research addressing reliability in lead-free solder processes and advanced interconnect methods such as flip-chip technology. Dr. Lau has influenced the adoption of lead-free solder processes as the industry shifts to more environmentally friendly interconnect

methods, publishing a book providing manufacturing guidelines and parameters in 2003. He was also responsible for converting Agilent Technologies' entire product line to lead-free.

Dr. Lau's recent work has provided extensive publications on advanced interconnect methods that have helped shape the landscape of 3D integrated-circuit integration technologies.

An IEEE Fellow, Dr. Lau is an ITRI Fellow with the Industrial Technology Research Institute, Hsinchu, Taiwan.



Shinichi Takagi of The University of Tokyo, Tokyo, Japan, has been named the recipient of the IEEE Andrew S. Grove Award. The citation states, *"For*

contributions to the understanding of transport properties in inversion layers of high-performance MOSFETs."

Shinichi Takagi has driven performance improvements in metal oxide semiconductor field-effect transistor (MOSFET) technology with his insight on behavior of carriers in semiconductor devices. Dr. Takagi's "universal mobility model" has been a key enabler of the continued scaling of electronic components. First presented in 1988, his model has provided a common framework for understating the transport mobility of carriers in the MOSFET inversion layer. The model has become a world standard highly cited in research and an important component of device simulators. His work on sub-band engineering of inversion layers focusing on strained silicon MOSFETs has important implications for sub-100-nanometer technology nodes. Dr. Takagi is also among the pioneers investigating higher-mobility materials such as germanium that will help the continued scaling of MOSFET devices when silicon technologies reach their scaling limits.

An IEEE Member, Dr. Takagi is a professor with the Department of

Electrical Engineering and Information Systems in the School of Engineering at the University of Tokyo, Japan.



Anantha P. Chandrakasan of Massachusetts Institute of Technology, Cambridge, Massachusetts, USA, has been named the recipient of the IEEE

Donald O. Pederson Award in Solid-State Circuits. The citation states, *"For pioneering techniques in low-power digital and analog CMOS design."*

Anantha P. Chandrakasan's pioneering work on low-power circuit design methods has helped overcome one of the most important design constraints in developing integrated circuits. Dr. Chandrakasan has published the most comprehensive body of work in the low-power circuit field, enabling reduction in energy storage requirements that constrain chip and device size. In 1994, Dr. Chandrakasan presented a complete low-power chip set for multimedia applications requiring just 5 mW of power, at a time when chips required 100 times that level. A radical concept that is now commonplace, the work resulted in a tablet computer that was the precursor to today's handheld multimedia devices. He has continued to impact today's low-power circuit design with key contributions to dynamic voltage scaling, ambient energy scavenging, ultra-low-power analog-to-digital conversion, and micro-power radios.

An IEEE Fellow, Chandrakasan is the Joseph F. and Nancy P. Keithley Professor of Electrical Engineering and the Department Head of Electrical Engineering and Computer Science at the Massachusetts Institute of Technology, Cambridge.

*Marvin H. White
EDS Vice President of Awards
Ohio State University
Columbus, OH, USA*



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Prof. Renuka P. Jindal

Univ. of Louisiana at Lafayette

Lafayette, LA USA.

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January 2013

Submit Manuscripts at:

<http://mc.manuscriptcentral.com/jeds>

The **IEEE Journal of Electron Devices Society** (J-EDS) is a peer-reviewed, **open-access**, fully electronic scientific journal publishing papers ranging from applied to fundamental research that are scientifically rigorous and relevant to electron devices.

Please submit your manuscripts for consideration of publications in J-EDS at <http://mc.manuscriptcentral.com/jeds>. The inaugural issue of the J-EDS was published in January 2013.

The J-EDS publishes original and significant contributions relating to the theory, modelling, design, performance, and reliability of electron and ion integrated circuit devices and interconnects, involving insulators, metals, organic materials, microplasmas, semiconductors, quantum-effect structures, vacuum devices, and emerging materials with applications in bioelectronics, biomedical electronics, computation, communications, displays, microelectromechanics, imaging, microactuators, nano-devices, optoelectronics, photovoltaics, power IC's, and micro-sensors. Tutorial and review papers on these subjects are, also, published.

The open-access publication, J-EDS is intended to provide the electron devices community:

- Faster speed of publication;
- Free access to readers globally;
- Worldwide audience;
- Increased dissemination;
- High impact factor (IF),
 - Articles can be cited sooner;
 - Articles potentially cited more frequently.

Publication charge for authors:

US \$1350 per article up to eight published pages;

US \$120 per page, over eight published pages.

For more information:

Visit: www.ieee.org/eds

Contact: eds@ieee.org



STATUS REPORT FROM THE 2012 EDS PH.D. STUDENT FELLOWSHIP WINNERS



Agis A. Iliadis
EDS Ph.D. Student
Fellowships Chair

In 2000, the IEEE approved the establishment of the Electron Devices Society Ph.D. Student Fellowship Program. The Program is designed to promote, recognize, and support graduate level study and research within the Electron Devices Society's Fields of Interest, which include: All aspects of the engineering, physics, theory, experiment and simulation of electron and ion devices involving insulators, metals, organic materials, plasmas, semiconductors, quantum-effect materials, vacuum, and emerging materials. Specific applications of these devices include bioelectronics, biomedical, computation, communications, displays, electro and micro mechanics, imaging, micro actuators, optical, photovoltaics, power, sensors and signal processing. In deference to the increasing globalization of our Society, at least one fellowship is to be awarded to students in each of three geographical regions: Americas, Europe/Mid-East/Africa, and Asia & Pacific.

The 2012 EDS Ph.D. Student Fellowship winners were: Bin Gao, Peking University; Jacopo Franco, IMEC/Katholieke Universiteit; and Shimeng Yu, Stanford University. The following are brief progress reports provided by the award winners.

Shimeng Yu is continuing his research work on the resistive switching



memory and its applications at Department of Electrical Engineering, Stanford University. His recent research interests include the fundamental physics exploration of the emerging device technologies and their applications for future computing paradigms, such as 3D memory integration, embedded memory, logic-in-memory, reconfigurable computing, bio-inspired neuromorphic computing, etc. He is looking for academic jobs right now, and will defend his Ph.D. thesis in May 2013 and graduate the summer of 2013.



Jacopo Franco recently defended his Ph.D. dissertation entitled "Reliability of High Mobility (Si)Ge Channel pMOSFETs for Future CMOS Application—Toward Reliable Ultra-Thin EOT Nanoscale Transistors," receiving the Congratulations of the Board of Examiners (a honor granted to less than 5% of the Ph.D. students at KU Leuven—Belgium). The main results of his research about the reliability of Ge-based channel devices have been collected in a two-part paper recently published in *IEEE Transactions on Electron Devices*, Vol. 60, no. 1 (Jan. 2013), entitled "SiGe Channel Technology: Superior Reliability Toward Ultrathin EOT Devices—Part I: NBTI;

Part II: Other Reliability Issues." His latest research about time-dependent variability in deeply-scaled MOSFETs has been presented at the IEEE International Reliability Physics Symposium 2013, held last April in Monterey, California. After his graduation, Jacopo is going to continue working as a Researcher with IMEC—Belgium, focusing on the same research fields explored during his Ph.D.



Bin Gao has continued pursuing his Ph.D. research at Peking University, making further contribution to his work on resistive switching memory. Also, he

has been studying about RRAM based synapse for neuromorphic systems. His recent outputs have been the simulation and measurement of 3D vertical RRAM array, and the development of an analytical model to characterize the disorder degree of oxygen vacancies in RRAM, which led to submissions to the 2013 VLSI Symposium. To date, he has published 5 journal papers and 7 conference papers as first author. He is the author and co-author of 12 IEDM and VLSI papers. One of his EDL papers has been cited more than 60 times. He is now writing his Ph.D. Thesis and expecting to defend his it in June 2013.

Agis A. Iliadis
EDS Ph.D. Student Fellowships
Chair
University of Maryland
College Park, MD, USA



CONGRATULATIONS TO THE 7 EDS MEMBERS RECENTLY ELECTED TO IEEE SENIOR MEMBER GRADE!

John Graham
James Gregory
Jr-Hau He

Saptharishi Sriram
Timothy Stanley

Steven Walstra
Kejun Xia

* Individual designated EDS as nominating entity.

If you have been in professional practice for 10 years, you may be eligible for Senior Membership, the highest grade of membership for which an individual can apply. New senior members receive a wood and bronze plaque and a credit certificate for up to US\$25 for a new IEEE society membership. Upon request a

letter will be sent to employers, recognizing this new status.

Please remember to designate the Electron Devices Society as your nominating entity!

For more information on senior member status, visit: http://www.ieee.org/membership_services/membership/senior/index.html

To apply for senior member status, fill out the on-line application: https://www.ieee.org/membership_services/membership/senior/application/index.html

You will need to Sign-in with your IEEE account.

EDS SENIOR MEMBER PROGRAM



Jamal Deen
EDS Vice-President
of Membership

members aware of the opportunity and encourage them to elevate their IEEE

The Electron Devices Society established the EDS Senior Member Program to both complement and enhance the IEEE's Nominate-a-Senior-Member Initiative and make IEEE/EDS mem-

bership grade to Senior Member. This is the highest IEEE grade for which an individual can apply and is the first step to becoming a Fellow of IEEE. If you have been in professional practice of 10 years, you may be eligible for Senior Membership.

Benefits of Senior Membership¹

- **Recognition:** The professional recognition of your peers for technical and professional excellence.

- **Senior member plaque:** Since January 1999, all newly elevated Senior members have received an engraved Senior Member plaque to be proudly displayed for colleagues, clients and employers to see. The plaque, an attractive fine wood with bronze engraving, is sent within six to eight weeks after elevation.

¹IEEE.org, http://www.ieee.org/membership_services/membership/senior/index.html

- **US\$25 coupon:** IEEE will recognize all newly elevated Senior members with a coupon worth up to US\$25. This coupon can be used to join one new IEEE society. The coupon expires on 31 December of the year in which it is received.
- **Letter of commendation:** A letter of commendation will be sent to your employer on the achievement of Senior member grade (upon the request of the newly elected Senior member).
- **Announcements:** Announcement of elevation can be made in section/society and/or local newsletters, newspapers and notices.
- **Leadership Eligibility:** Senior members are eligible to hold executive IEEE volunteer positions.
- **Ability to refer other candidates:** Senior members can serve as a reference for other applicants for senior membership.
- **Review panel:** Senior members are invited to be on the panel to review senior member applications.
- **US\$25 referral coupon:** Newly elevated Senior members are encouraged to find the next innovators of tomorrow and invite them to join IEEE. Invite them to join and the new IEEE member will receive \$25 off their first year of membership.

As part of the IEEE's Nominate-a-Senior-Member Initiative, the nominating entity designated on the member's application form will receive US\$10 from IEEE for each application approved for Senior Member grade when there are at least five approved applications. As an EDS member, we would appreciate it if you could indicate on your Senior Member application form that **EDS** is your nominating entity.

Please be aware that even if you decide to list EDS as your nominating entity, you still need to have an IEEE member nominate you along with two other references. Your nominator and your references all must be active IEEE members holding Senior Member, Fellow or Honorary Member grade.

For more information on the criteria for elevation to Senior Member, please visit the Senior Membership Portal: http://www.ieee.org/membership_services/membership/senior/index.html.

We strongly encourage you to apply for IEEE Senior Membership to enhance your career. At the same time, you'll be helping EDS. Thank you for supporting IEEE and EDS.

*Jamal Deen
EDS Vice-President of Membership
McMaster University
Ontario, Canada*



EDS CHAPTER SUBSIDIES FOR 2014

The deadline for EDS chapters to request a subsidy for 2014 is September 1, 2013. For 2013, the EDS AdCom awarded funding to 63 chapters, with most amounts primarily ranging from US\$250 to US\$750. In June, Chapter Chairs were sent an e-mail notifying them of the current funding cycle and providing them with a list of

guidelines. In general, activities which are considered fundable include, but are not limited to, membership promotion, travel allowances for invited speakers to chapter events, and support for student activities at local institutions.

Chapter Subsidy requests can be applied for, by completing a chapter

activity report. Please note that the report needs to be submitted by September 1st.

Final decisions concerning subsidies will be made in December. Subsidy checks will be issued by late December/early January. Please visit the EDS website for more information.

CALL FOR NOMINATIONS FOR THE EDS CHAPTER OF THE YEAR AWARD

The EDS Chapter of the Year Award is given each year based on the quantity and quality of the activities and programs implemented by the chapters during the prior July 1st – June 30th period.

At the June 2012 EDS BoG (AdCom) Meeting, the BoG (AdCom) approved to increase the number of awards we give out in a given year, starting with the 2013 Award. We will award one Chapter from each of the following Regions:

- Regions 1–7
- Region 8
- Region 9
- Region 10

Nominations for the awards can only be made by SRC Chairs/Vice-Chairs, or self-nominated by Chapter Chairs. Please visit the EDS website to submit your nomination form.

Each winning chapter will receive a plaque and check for \$500 to be presented at an EDS Conference or Chapter Meeting of their choice. Travel reimbursement will not be provided.

The schedule for the award process is as follows:

Action

Call for Nominations E-Mailed to Chapter Chairs,

SRC Chairs & SRC Vice-Chairs

Deadline for Nominations

Regions/Chapters Committee Selects Winners

Award given to Chapter Representative at IEDM

Date

June 1

September 15

Early-October

First week of December

EDS-ETC

Engineers Demonstrating Science:
an Engineer Teacher Connection

EDS-ETC REPORT FROM THE ED PUEBLA CHAPTER

By CLAUDIA REYES-BETANZO, ED PUEBLA CHAPTER AND PATRICIA GÚZMAN, IEEE PUEBLA SECTION

The IEEE Puebla Section in collaboration with the EDPuebla Chapter, implemented an Educational Project for elementary schools in the region, using Elenco Snap Circuits® kits, kindly donated by the IEEE Electron Devices Society.

On February 9, 2013, students in social service organized a workshop

titled, “*Electronics Initiation*” for 70 children in the San Gregorio Zacatechpan and Benito Juárez communities. The participating students expressed a big interest in the kits

and how electronics work. One objective of this project is to introduce students to electronics and motivate them to take part in the next generation of successful engineers.





2013 IEEE International Electron Devices Meeting

*The annual meeting of the Electron Devices Society
will be held at the Washington Hilton, Washington, DC, December 9-11, 2013*

Late news papers:

Deadline for receipt of abstracts is September 11, 2013.

A very limited number of late news papers will be accepted. Late News Papers are not eligible for travel assistance or the student paper award.

Authors are asked to submit late news abstracts announcing only very recent developments. PDF files should be in the same format as a regular abstract and should be emailed to Polly Mahoney at the Conference Office. ACCEPTED LATE NEWS PAPERS AND ACCOMPANYING FIGURES WILL BE PRINTED AS RECEIVED IN THE TECHNICAL DIGEST. SUBMISSION OF A LATE NEWS PAPER FOR REVIEW WILL BE CONSIDERED BY THE REVIEW COMMITTEE AS CONSENT FROM THE AUTHOR FOR ITS PUBLICATION IF ACCEPTED. Length of the late news presentation will be ten minutes, with an additional five minutes for questions.

Meeting Highlights

- Three plenary presentations by prominent experts.
- Invited papers on all aspects of advanced devices and technologies.
- Special focus sessions covering topics in
 - BioMEMS
 - Analog devices and circuits
 - Advanced semiconductor manufacturing
 - Terahertz devices.
- Two evening panel discussions.
- Presentation of IEEE/EDS awards.
- IEDM luncheon presentation will be held on Tuesday, December 10.
- Entrepreneur's lunch at IEDM on Wednesday, December 11.
- 90 minute tutorial sessions will be offered on emerging topics, on Saturday afternoon, December 7.
- Two short courses will be held on Sunday, December 8.

www.ieee-iedm.org

REGIONAL AND CHAPTER NEWS

USA, CANADA & LATIN AMERICA (REGIONS 1-6, 7 & 9)

2013 Berkeley E3S Symposium

—by Janny Peng

The Organizing Committee cordially invites you to participate in the 3rd Berkeley Symposium on Energy Efficient Electronic Systems on October 28–29, 2013, in Berkeley, California. Established in 2009, the Berkeley E3S Symposium biennially brings together researchers who are working on breakthrough improvements in energy efficiency for information processing systems. To allow the attendees to gain an integrated perspective of the challenges and advances in this domain of technology, the sessions will cover the entire food chain, from devices to systems.

- Ultra Low Voltage Nanoelectronics
- Milli-Volt Nanomechanical Logic
- Spin Based Computation
- Energy Efficient Memory Devices and Storage Systems
- Optical Chip Scale Interconnect
- Low Voltage CMOS Circuits and Architectures
- Energy Efficient Computing Systems

The program will have invited talks and contributed oral and poster papers. The Organizing Committee has issued a Call for Papers with a submission deadline of August 8th.

The NSF Center for Energy Efficient Electronics Science is the lead sponsor, and the IEEE Electron Devices Society is a technical co-sponsor.

The academic setting of the University of California, Berkeley is expected to encourage open exchanges of ideas, and foster closer cooperation and collaborations among the researchers.



Berkeley Sather Tower

For more information, please visit www.e3s-center.org/symposium.

ED UCA, Riverside

—by Li Wang

On April 2, 2013, Prof. Mikael Östling from KTH, Royal Institute of Technology, Sweden, and his wife, Dr. Carina Zaring, visited the EDS Student

Chapter at the University of California, Riverside. Prof. Östling, an EDS Distinguished Lecturer (DL), delivered a seminar talk entitled “SiC device technology—present status, applications and future perspective.” The DL lecture covered recently technology advances in SiC based wide bandgap semiconductor devices, circuits and



Prof. Mikael Östling (front row, 4th from left) and Prof. Albert Wang (1st from left) with the students



applications, and was well received by a group of more than twenty undergraduate and graduate students at UC Riverside. The lecture served well to expose the students to new developments in high-power high-temperature semiconductor technologies. After the DL, Prof. Östling toured the Laboratory for Integrated Circuits and Systems, and the University of California Center for Ubiquitous Communications by Light. During the seminar and tours, Prof. Östling had discussions with the students on various research topics and also met with Prof. Albert Wang at UC Riverside to discuss various issues of the Electron Devices Society business.

~ Adam M. Conway, Editor

2013 WiPDA

—by Jin Wang

The 1st IEEE Workshop on Wide Bandgap Power Devices and Applications

The IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA) provides a forum for researchers, circuit designers, and application engineers from the Electron Device Society and Power Electronics Society to share technology updates, research findings, development experience and potential applications. The technical topics of the workshop range from material growth, device fabrication, and circuit topology, to system integration in varied applications.

The inaugural edition of this annual workshop will be held in Columbus, Ohio, USA, Sunday, October 27 through Tuesday, October 29, 2013.

Technical sessions will be held on the afternoons of October 28th and 29th. Four short courses will be offered by experts from CREE, EPC, Infineon, and Oak Ridge National

Laboratory on October 27th. Two keynote sessions with six leading experts will be held on the mornings of the October 28th and 29th. A panel session with participants from government agencies, leading industries, and academia is scheduled for late in the morning on the 29th. The workshop poster session and banquet will be hosted in the evening of the 28th at The Huntington Club, located in the historic OSU football stadium, "The Horseshoe."

For more information, please visit the workshop's website at <http://www.wipda2013.org/>.

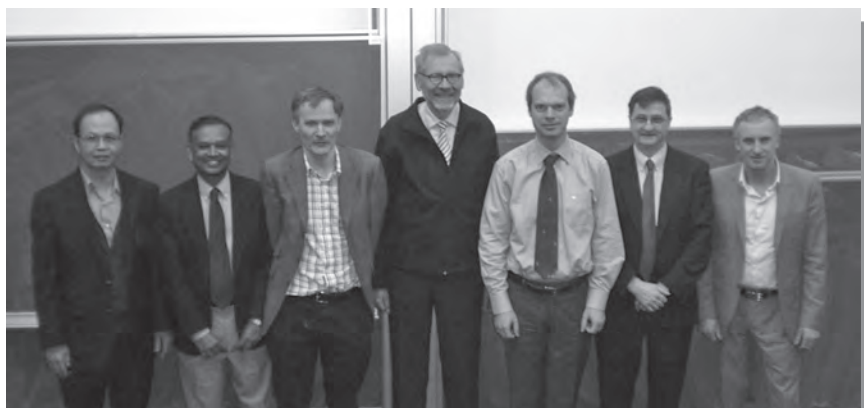
EUROPE, MIDDLE EAST & AFRICA (REGION 8)

Report on the IEEE EDS Mini-Colloquium Held in Edinburgh, Scotland

The IEEE EDS Mini-Colloquium on Microsystems was held April 19, 2013, at the James Clerk Maxwell Building on the King's Buildings

campus of the University of Edinburgh, Scotland, United Kingdom. The event was held to celebrate the formation of the new Scottish chapter of the Electron Devices Society. The all-day event saw both oral and poster presentations and was attended by a total of 60, with representatives from industry and academia throughout the UK and beyond. The meeting began with a welcome address from the Chapter Chair of ED Scotland, Professor David Cumming of the University of Glasgow, which was followed by an overview of the activities of the Electron Devices Society given by Dr. Meyya Meyyappan of NASA Ames Research Center, who is EDS Vice President for Educational Activities. The key talks were given by four IEEE EDS Distinguished Lecturers (DL) and four invited experts in the field of Microsystems.

In the first session, Dr. Werner Weber (DL) of Infineon Technologies gave a talk "3D stacking of silicon chips—an industrial viewpoint," which introduced the concept of more-than-Moore technology before examining different 3-D integration trends. This was followed with a talk by Dr. Simon Deleonibus (DL) of CEA-Leti entitled "Perspectives of Future Nanoelectronics Heterogeneous co-Integration," which considered the pitfalls involved in scaling of nanoelectronics as well as the heterogeneous co-integration of scalable



Speakers at the Edinburgh EDS MQ (from left to right), Prof. Juin Liou (EDS DL), Dr. Meyya Meyyappan (EDS DL), Prof. David Cumming (ED Scotland Chapter Chair), Dr. Werner Weber (EDS DL), Prof. Jurriaan Schmitz, Prof. Richard Syms, and Prof. Andrew Richardson



Dr. Darren Cadman of the leMRC with poster prize winner, Miss Kirsty Rew of the University of Glasgow

devices. The session was brought to a close with a talk by Professor Richard Syms of Imperial College London, "Microfabricated Detectors for Internal Magnetic Resonance Imaging," describing his groundbreaking research to address the common problem of signal-to-noise ratio in the resolution of MRI images by closer proximity to the target tissue. The improved resolution and contrast of images achievable is key to early diagnosis, especially of cancer.

A poster session highlighting the work of Ph.D. students in Scotland provided the backdrop to an enjoyable lunch and networking opportunity. The second session started with a talk from Professor Jurriaan Schmitz of Twente University on "CMOS post-processing for more-than-Moore," giving examples of a number of recent technological breakthroughs in this diverse field. Next came a talk from Dr. Sara Pellegrini of ST Microelectronics on "SPAD-based time-of-flight sensors for mobile/consumer applications" describing the work of the company's Imaging Division into advanced image sensing with single photon avalanche diodes. Dr. Meyyappan (DL) returned to the podium to close the session with a talk on "Nanotechnology in Nanoelectronics and Sensor Development," examining the use of nanowires and carbon nanotubes in a range of future device applications. A break for coffee then allowed attendees a further look at the innovative work detailed in the displayed posters.

The final session of the event saw two talks, the first from Professor Andrew Richardson of Lancaster University entitled "Towards Fault Tolerant Smart Microsystems for Sensing Applications," which described his work building the capabilities of self-test and self-repair into micro and nanosystems. The final talk of the day was given by Professor Juin Liou (DL) of the University of Central Florida on "Recent developments on electrostatic discharge protection of RF integrated circuits," an interesting overview of the present state-of-the-art in ESD prevention. All the talks were very well received and followed by lively Q&A sessions.

The day finished with the presentation of the poster prize, sponsored by the EPSRC-funded Innovative Electronics Manufacturing Research Centre (leMRC) based at the University of Loughborough. The prize of a certificate and a £50 voucher were awarded by Dr. Darren Cadman of leMRC to the winner, Miss Kirsty Rew, a Ph.D. student at the University of Glasgow, for her poster entitled "Nanophotonics for digital imaging." Runners up prizes of pens with integrated memory sticks, provided by the IEEE UK & RI Section, were awarded to Miss Li Li of Strathclyde University and to Mr. Neale Dutton and Mr. Aleksandr Tabasnikov of the University of Edinburgh.

As well as thanking all the speakers for their excellent, thought provoking presentations, ED Scotland would especially like to thank Dr. Jonathan Terry of the University of Edinburgh for organizing the event. They would also like to acknowledge the assistance of Tarek Al Abbas, Carsten Schumacher and Aravind Venugopalan Nair Jalajakumari of the IEEE University of Edinburgh Student Branch who helped in the smooth running of the event.

*David Cumming
ED Scotland Chapter Chair
University of Glasgow
Scotland, United Kingdom*

ED Manchester University

—by Emerson Sinulingga

The IEEE ED University of Manchester Student Chapter has had a busy first six months of operation, in which it has organized a number of successful events including IEEE EDS Distinguished Lectures, an Electronic Devices seminar series and an ED Matlab workshop. The chapter has also been well represented in worldwide and regional IEEE competitions including IEEE Xtreme 6.0 and the 2013 IEEE Region 8 Student Paper Contest.

In appreciation of the enthusiastic participation of their student members, the UoM ED Student Chapter held a well-attended ED Social



University of Manchester Student Chapter Counsellor, Professor Ali Rezazadeh, awarding a Certificate of Appreciation to one of the chapter's student members

Gathering on February 25, 2013. At the event, prizes, IEEE certificates and IEEE t-shirts were awarded to students and speakers in recognition of their contributions to the success of the Student Chapter.

Following on from these early successes, the chapter plans to organize bigger events in the future, such as an IEEE ED Mini Colloquium entitled *Engineering beyond Lecture Rooms* to be held in June 2013, as part of the chapter's mission to support the learning process not only in a traditional classroom setting, but also through high quality ED seminars and distinguished lectures.

~ **Jonathan Terry, Editor**

2013 ESSDERC

~by **Stefan Rusu**

The 43rd European Solid-State Device Research Conference (ESSDERC) will take place on September 16–20, 2013 at the J.W. Marriott Grand Hotel in Bucharest, Romania. The conference provides an annual European forum for the presentation and discussion of recent advances in solid-state devices and is co-located with the European Solid-State Circuits Conference (ESSCIRC). While keeping separate Technical Program Committees, the two conferences share plenary keynote presentations and joint sessions bridging both communities. Attendees registered for either conference are encouraged to attend any of the scheduled parallel sessions.

Plenary speakers include Infineon CEO, Reinhard Ploss, speaking about "Automotive electronics and energy efficiency" and Wilfried Haensch (IBM) discussing carbon electronics for 2020.

The technical program includes papers on advanced CMOS devices, process & integration, microwave and power solid state devices, modeling and simulation, characterization, reliability and yield, advanced and emerging memories, MEMS, bio-sensors and display technologies, optoelectronic and photonic devices, emerging non-CMOS devices and technologies, carbon-based devices.

Three tutorials will be organized on Monday, September 16, 2013:

- "RF MEMS: technology and applications" (Organizer: Adrian Ionescu, EPFL, Switzerland);
- "High Voltage Devices" (Organizer: Florin Udrea, University of Cambridge, UK);
- "Graphene" (Organizers: Adrian Ionescu, EPFL & Florin Udrea, University of Cambridge).

Several workshops will take place on Friday, September 20, 2013, including MOS-AK Compact Modeling, Eastern European Research in Nanotechnologies, Cognitive Radios, Variability and Reliability, Guardian Angels Project and Reliable Chip Designs. The social program includes an opening reception and a gala dinner event.

The city of Bucharest is the capital of Romania and its most important cultural, business and financial center. It is easily accessible from all major European cities and with only one-stop connections from Asia and the Americas. The city benefits from a modern international airport and an extensive public transport system. Romania is the largest country in south-eastern Europe and a member of the European Union since January 2007.

Full details about the conference can be found on the ESSDERC web site at www.essderc.org.

~ **Tomislav Suligoj, Editor**

2013 CDE

~by **Helena Castán**

An IEEE EDS Mini-Colloquium was held in Valladolid, Spain, February 12–14, 2013, as a core part of the 9th Spanish Conference on Electron Devices (CDE'2013). The CDE'2013 was organized by the University of Valladolid (UVA, Valladolid, Spain). UVA also organized the IEEE EDS Mini-Colloquium that was integrated into the CDE'2013. The Chairwoman of CDE'2013 was Prof. Helena Castán, from UVA, and the chairman of the IEEE EDS Mini-Colloquium was Prof. Benjamin Íñiguez, from University

of Rovira I Virgili (URV, Tarragona, Spain). The venue of the conference was the "Palacio de Congresos Conde Ansúrez" (Valladolid).

The goals of the conference and the IEEE EDS Mini-Colloquium were to present and discuss recent advances in all topics related to electron devices, with topics ranging from materials to circuits and systems, including devices, fabrication methodologies, and also modeling techniques. Both the Symposium and the Mini-Colloquium were supported by: University of Valladolid, Campus de Excelencia Internacional E³-"Los Horizontes del Hombre," Government of Castilla y León, City of Valladolid, Diputación de Valladolid, IEEE Spanish Section, IEEE Electron Devices Society, Banco Santander, Instrumentos de Medida S.L., Agilent Technologies, SicenTec, and American Elements.

The program of the IEEE EDS Mini-Colloquium was as follows: *Recent Development in Electrostatic Discharge Protection of RF Integrated Circuits* (Prof. Juin J. Liou, University of Central Florida, USA); *Trends in Technology, Reliability and Qualification of Leading Edge MOS Technologies* (Prof. Fernando Guarín, SRDC, IBM, Fishkill, New York); *Radiation Sensors* (Prof. Eugeni García Moreno, UIB, Spain); *Thin Film Transistor Modeling: Specific features and requirements* (Prof. Magali Estrada, CINVESTAV, Mexico); *Ultra-Thin Chips: A new paradigm in silicon technology?* (Prof. Joachim Burghartz, IMSCHIPS, Stuttgart, Germany); and *Nanostructured polymers for ordered bulk heterojunction solar cells* (Prof. Luís F. Marsal, URV, Spain).

The CDE'2013 and the IEEE EDS Mini-Colloquium were attended by 137 people, from both academia and industry. The social program included a welcome reception chaired by the University Chancellor, Prof. Marcos Sacristán, a visit to the University Historical Library and to the Jiménez Arellano Foundation Museum, a classical music performance, a jazz concert, a tourist visit of the historical



downtown of Valladolid, a visit to the National Sculpture Museum, a gala dinner, and a "tapas tour."

Attendees considered the conference very successful in terms of organization, technical quality of the contributions and opportunities for discussions. As a result of this positive impression, it is planned to organize again the CDE and the related IEEE EDS Mini-Colloquium in 2015, this time in the Spanish city of Aranjuez.

~Jan Vobecky, Editor

ASIA & PACIFIC (REGION 10)

Technophil 2013

~by Atanu Kundu

Technophil 2013, "a Workshop on CMOS & Beyond CMOS Circuits and System Design," was organized by the Special Manpower Development Project (SMDP-II) in association with the IEEE EDS Chapter, Kolkata Section and Synopsys (India) EDA Software



Pvt. Ltd., at Jadavpur University, Kolkata, from March 18–21, 2013.

The program was inaugurated at Amitava Dey Memorial Hall, Jadavpur University, by Atanu Kundu and Prof. Chandan Kumar Sarkar, Chair, IEEE EDS Chapter, Kolkata Section. The other dignitaries present in the inauguration, were Prof. Salil Kumar Sanyal, Dept. of ETCE, Jadavpur University, Prof. Sudhabindu Ray, Dept. of ETCE, Jadavpur University, and Prof. Sayan Chatterjee, Dept. of ETCE, Jadavpur University.

Throughout the workshop several lectures on emerging topics were delivered by renowned academicians, namely, Prof. M. S. Baghini from Indian Institute of Technology, Bombay,

Prof. Santanu Mahapatra from Indian Institute of Science, Bangalore and Prof. Debaprasad Das from Meghnad Saha Institute of Technology, Kolkata. In addition, the workshop curriculum also included hands-on training on IC Compiler using the Synopsys EDA tool. All the Lab Sessions were conducted by Mr. Gurmeet Singh, Physical Design Engineer from Synopsys (India) EDA Software Pvt. Ltd., Bangalore.

The workshop was extremely successful in bringing together students from different domains of Electronics and Communication Engineering, providing them an opportunity to interact with experts in their respective field. The program was coordinated by Dipankar Saha from SMDP-II Lab. It was really a collaborative training program initiated by IEEE EDS Kolkata between software industry Synopsys (India) and Jadavpur University, fulfilling the objectives of the IEEE Electron Devices Society.

ED Delhi

~by Manoj Saxena & Mridula Gupta

The ED Delhi Chapter organized one national conference, one workshop, one Distinguished Lecture (DL) and technical talks during the first quarter of 2013.

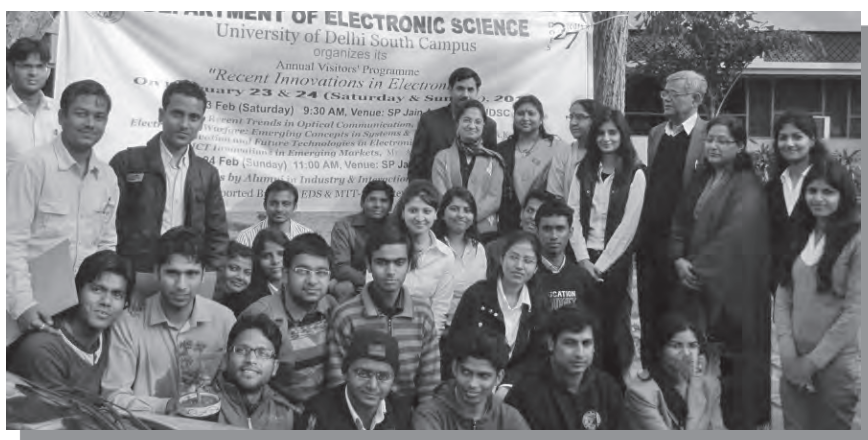
The chapter organized an IEEE EDS Distinguished Lecture by Rajendra Singh, Department of Electrical and Computer Engineering and Center for Silicon Nanoelectronics, Clemson University, USA, entitled, "Semiconductor Manufacturing in Sub 20 nm Era: Challenges and Opportunities." The lecture was held on January 7, 2013, at University of Delhi South Campus, New Delhi.

The First National Conference on Recent Developments in Electronics (NCRDE 2013), was held at the University of Delhi South Campus, New Delhi, January 18–20, 2013. The Conference received about 81 contributory papers, out of which 51 were accepted for oral presentations. There were in total 10 technical sessions along with 14 keynote/





Dr. Rajendra Singh and attendees of the DL



Group of participants of Recent Innovations in Electronics

invited/plenary talks addressed by very eminent speakers. The conference was held in conjunction with the *Third National Workshop on Recent Trends in Semiconductor Devices and Technology*, sponsored by the Defense Research and Development Organization, Government of India. There were two tutorials conducted on diverse topics like *"ESD Challenges in Sub-micron Devices: Design, Testing and Application,"* by Prof. M.K. Radhakrishnan (NanoRel Bangalore) and *"Extending Microwave Measurements beyond the Horizon"* by Mr. Adesh Kumar Jain (Agilent Technologies), for the benefit of the students.

On February 1–2, 2013, the ED Delhi Chapter and Deen Dayal Upadhyaya College, University of Delhi, jointly organized the *Lecture Workshop on Transdisciplinary Areas of Research and Teaching*, which was

sponsored by the Council of Scientific and Industrial Research (CSIR), Government of India. *Shanti Swarup Bhatnagar Awardees* delivered invited talks during the workshop, which was attended by 227 students and faculty members from more than 21 institutions.

The Annual Visitors' Program of the Department of Electronic Science University of Delhi, South Campus, was held February 23–24, 2013, on the theme "Recent Innovations in Electronics" which was sponsored by the ED Delhi Chapter. This program, attended by 100 students, had four technical talks given by experts from the Defense Laboratory, Government of India.

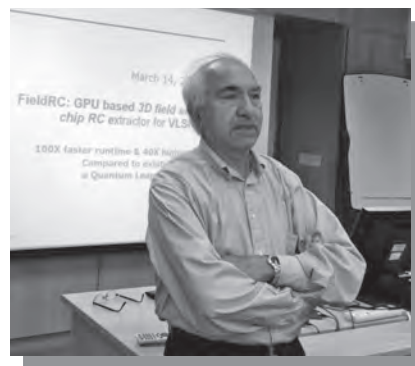
A Technical Talk by Mr. Ramesh Kaza, Senior Vice President, Bank of America, on *"Life After University"* was organized by the Chapter on March 1, 2013.

ED/REL/CPMT/Singapore

—by Xing Zhou and Yeow Kheng Lim

The chapter organized three technical talks at the beginning of the year, beginning on February 15th with Dr. Leo Lorenz of Infineon Technologies, Germany, who gave a Distinguished Lecture (DL) on *"Power Semiconductor Devices—Technology Trends and Challenges in the Application"* at the National University of Singapore. This DL event was co-hosted with the Singapore IA/PEL Chapter.

On March 14th, Dr. Narain Arora gave a DL entitled, *"FieldRC: GPU based 3D field solver on chip RC extractor for VLSI design."* The talk was co-hosted with the School of EEE of Nanyang Technological University



Dr. Narain Arora at the DL talk on March 14, 2013

(NTU). Dr. Arora also gave two related seminars on *"Modeling and Characterization of VLSI Interconnects"* to the students at EEE on March 1st and 7th, while he was a visiting senior research scientist at the School.

On March 22, 2013, Dr. Philippe Perdu of CNES, France, gave a talk at NTU entitled, *"3D Devices Failure Analysis—From Diagnosis to Defect Localization, What can we do?"*

~ M.K. Radhakrishnan, Editor

Report on the IEEE EDS Mini-Colloquium, (WIMNACT-37), Held in Tokyo, Japan

—by Akira Toriumi

Eight world-class researchers on nanoelectronics were invited to speak at the 37th Workshop and IEEE EDS



Mini-colloquium (MQ) on Nanometer CMOS Technology (WIMNACT), which was co-sponsored by the ED Japan Chapter and Tokyo Institute of Technology (TIT). The event was held on February 18th, at Tokyo Tech Front, Tokyo, Japan.

The speakers were as follows:

- "Carbon Nanotubes for Electronic Applications?" by Prof. W. I. Milne, Cambridge University,
- "Heterogeneous Micro/Nano-Electronics: Towards the Maturity Learning into the Zero Variability Era," a lecture on the future of nano-electronics, by Dr. S. Deleonibus, CEA-LETI,
- "Graphene and Beyond-Graphene Nanomaterials for Green Electronics," Prof. K. Banerjee, UC Santa Barbara,
- "When Lanthana Meets Silicon," Prof. H. Wong, Hong Kong City University

After a break for lunch, the program continued with lectures from Prof. A. Toriumi, the University of Tokyo, and ED Japan Chapter Chair, speaking on graphene-metal contacts; Prof. K. Shiraishi on a theoretical study of SiC-MOSFETs; Dr. T. Mogami, PETRA, also the ED Japan Chapter Vice-Chair, on emerging analysis technologies for nano-electronics, and finally Prof. K. Tsutsui, Tokyo Institute of Technology, on the photoelectron spectroscopic analysis of scaled devices.

The attendees really enjoyed the lectures from these top professors in the field of nanoelectronics. After the lectures, a poster session was held for young researchers and students.

ED Kansai

—by Michinori Nishihara

The ED Kansai Chapter held a feedback meeting from the 2012 IEDM with more than 20 students and members from academia and industries. The meeting was held at the Josho Gakuen Osaka Center, in Osaka, Japan, January 31, 2013.

The following three researchers reported: Dr. Hidetoshi Ishida of Panasonic, on compound semiconductor sessions and Prof. Takuji Hosoi of Osaka University, on Silicon and SiC related

sessions. Prof. Yoshinari Kamakura of Osaka University summarized the Modeling and Reliability sessions.

According to the reports, we felt a clear change in technology trends toward post-silicon materials and compound semiconductor FETs. During the Luncheon Presentation of the 2012 IEDM, Ajit Manocha indicated there will be only four groups engaged in SoC technology such as Intel, Samsung, TSMC and Global Foundry. It will be quite a change from those days when there were many papers from Japanese semiconductor companies. Instead there were a growing number of papers from Japanese semiconductor companies in Imaging and Power Semiconductors sessions.

While GaN power devices show steady performance improvement in the Power Semiconductors session, papers on SiC based power devices are now shifting to reliability and manufacturability topics.

After the IEDM feedback meeting, we held the annual general meeting to review activities of ED Kansai in 2012 and to discuss plans for 2013. We elected Prof. Yukiharu Uraoka of Nara Institute of Science and Technology as our new Chair and Dr. Takashi Nakamura of ROHM Co., Ltd. as the new Vice Chair. We also elected Prof. Toshihiko Maemoto as Secretary and Dr. Ken Nakahara of ROHM as Treasurer. Also discussed were plans for the upcoming 2013 IMFEDK international conference, which is to be co-sponsored with the Solid-State Circuits Society Kansai Chapter on June 5–6 in Osaka, Japan.

~ Kuniyuki Kakushima, Editor



Dr. Hidetoshi Ishida (Panasonic) at the IEDM feedback meeting



Prof. Takuji Hosoi (Osaka University) at the IEDM feedback meeting

EDS MEETINGS CALENDAR

(As of 4 June 2013)

THE COMPLETE EDS CALENDAR CAN BE FOUND AT OUR WEB SITE:

[HTTP://EDS.IEEE.ORG](http://eds.ieee.org). PLEASE VISIT.

02 Jul - 03 Jul 2013

2013 International Conference on Optical Imaging Sensor and Security (ICOSS)

Conf Record :31921
Location: Coimbatore , India
Contact : MUNIRAJ N J R
Tel : +919344707218
Fax : +914212333175
E-mail: njrmuniraj@yahoo.com
Deadline : 30 Jun 2013
www : <http://www.tejaashakthi.org/icoss2013/>

22 Sep - 25 Sep 2013

2013 IEEE Custom Integrated Circuits Conference - CICC 2013

Conf Record :18692
Location: San Jose CA , USA
Contact : Melissa Widerkehr
Tel : +1 301 527 0900
Fax : +1 301 527 0994
E-mail: melissaw@widerkehr.com
Deadline :
www : <http://www.ieee-cicc.org>

09 Dec - 11 Dec 2013

2013 IEEE International Electron Devices Meeting (IEDM)

Conf Record :11125
Location: Washington DC ,
Contact : Ms. Phyllis W. Mahoney
Tel : +1 301 527 0900 (Ext. 2)
Fax : +1 301 527 0994
E-mail: phyllism@widerkehr.com
Deadline :
www : <http://www.ieee-iedm.org>

02 Jul - 05 Jul 2013

2013 Twentieth International Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD)

Conf Record :30622
Location: Kyoto , Japan
Contact : Yukiharu Uraoka
Tel : +81-743-72-6060
Fax : +81-743-72-6060
E-mail: uraoka@ms.naist.jp
Deadline : 12 Mar 2013
www : <http://www.amfpd.jp>

23 Sep - 26 Sep 2013

2013 XVIIIth International Seminar/Workshop on Direct and Inverse Problems of Electromagnetic and Acoustic Wave Theory (DIPED)

Conf Record :31680
Location: Lviv , Ukraine
Contact : Mykhaylo Andriychuk
Tel : +38 032 2585144
Fax :
E-mail: andr@iapmm.lviv.ua
Deadline : 10 Aug 2013
www : <http://ewh.ieee.org/soc/cpmt/ukraine/>

22 Apr - 24 Apr 2014

2014 IEEE International Vacuum Electronics Conference (IVEC)

Conf Record :20241
Location: Monterey CA , USA
Contact : Glenys Natera
Tel : +1 212 460 8090
Fax :
E-mail: gnatera@pcm411.com
Deadline :
www : <http://>

09 Jul - 12 Jul 2013

2013 26th International Vacuum Nanoelectronics Conference (IVNC)

Conf Record :31038
Location: Roanoke VA , USA
Contact : Jonathan Shaw
Tel : 2027679205
Fax : 2027679205
E-mail: jon.shaw@nrl.navy.mil
Deadline : 03 Jun 2013
www : <http://www.ivnc2013.org/>

30 Sep - 04 Oct 2013

ESREF 2013 24th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis

Conf Record :31739
Location: Arcachon , France
Contact : Nathalie LABAT
Tel : +33540006551
Fax : +33556371545
E-mail: nathalie.labat@ims-bordeaux.fr
Deadline : 24 May 2013
www : <http://http://www.esref.org>

31 May - 05 Jun 2014

2014 IEEE International Reliability Physics Symposium (IRPS)

Conf Record :20379
Location: Waikoloa HI , USA
Contact : David Barber
Tel : +1 828 898 7001
Fax : +1 828 898 6375
E-mail: dbarbsta@aol.com
Deadline :
www : <http://www.irps.org>

15 Jul - 19 Jul 2013

2013 20th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)

Conf Record :31912
Location: Suzhou , China
Contact : Jasmine Leong
Tel : +65 6743 2523
Fax :
E-mail: mingxiang_wang@suda.edu.cn
Deadline : 10 Jun 2013
www : <http://http://ieee-ipfa.org/>

30 Sep - 03 Oct 2013

2013 IEEE Bipolar/BiCMOS Circuits and Technology Meeting - BCTM

Conf Record :30279
Location: Bordeaux , France
Contact : Bruce Hecht
Tel : +1 781-937-1535
Fax : +1 781-937-1702
E-mail: Bruce.Hecht@analog.com
Deadline : 19 Jul 2013
www : <http://ieee-bctm.org/>

08 Jun - 13 Jun 2014

2014 IEEE 40th Photovoltaic Specialists Conference (PVSC)

Conf Record :21196
Location: Denver CO , USA
Contact : Richard R. King
Tel : +1 805 558 4576
Fax : +1 818 838 7474
E-mail: rking@spectrolab.com
Deadline : 26 May 2014
www : <http://www.ieee-pvsc.org/PVSC40>

12 Aug - 14 Aug 2013

13th Non-Volatile Memory Technology Symposium

Conf Record :31643
Location: Minneapolis MN , USA
Contact : Marie Rahne
Tel : + 1 612-626-0375
Fax : + 1 612-625-4583
E-mail: lars1789@umn.edu
Deadline : 05 Aug 2013
www : <http://http://nvmts.org>

06 Oct - 09 Oct 2013

2013 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)

Conf Record :30122
Location: Monterey CA , USA
Contact : Francois Colomb
Tel : +1 978-684-5435
Fax :
E-mail: francois_y_colomb@raytheon.com
Deadline :
www : <http://www.csics.org>

10 Jun - 12 Jun 2014

2014 IEEE Symposium on VLSI Technology

Conf Record :18214
Location: Honolulu HI , USA
Contact : Phyllis Mahoney
Tel : +1 301 527 0900
Fax : +1 301 527 0994
E-mail: phyllism@widerkehr.com
Deadline :
www : <http://www.vlsisymposium.org>

02 Sep - 06 Sep 2013

2013 Symposium on Microelectronics Technology and Devices (SBMicro)

Conf Record :31025
Location: Curitiba , Brazil
Contact : Jacobus Swart
Tel : +55-19-35213707
Fax :
E-mail: jacobus@fee.unicamp.br
Deadline : 01 Jun 2013
www : <http://cobre.eletrica.ufpr.br/chipin/sbmicro.html>

06 Oct - 08 Oct 2013

2013 European Microwave Integrated Circuit Conference (EuMIC)

Conf Record :30843
Location: Nuremberg , Germany
Contact : Wolfgang Heinrich
Tel : +49 30 6392 2620
Fax :
E-mail: w.heinrich@eumwa.org
Deadline : 14 Jun 2013
www : <http://www.eumweek.com>

15 Jun - 19 Jun 2014

2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD)

Conf Record :20170
Location: Waikoloa HI , USA
Contact : Don Disney
Tel : +1 408 684 5223
Fax :
E-mail: ispsd.disney@gmail.com
Deadline : 08 Mar 2014
www : <http://www.ispsd2014.com>

03 Sep - 05 Sep 2013

2013 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)

Conf Record :31141
Location: Glasgow , United Kingdom
Contact : Salvatore Amoroso
Tel :
Fax :
E-mail: salvatore.amoroso@glasgow.ac.uk
Deadline :
www : <http://www.sispad2013.org/>

07 Oct - 10 Oct 2013

2013 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S) (Formerly known as SOI Conference)

Conf Record :30572
Location: Monterey CA , USA
Contact : Joyce Hooper
Tel : 818-795-3768
Fax : 818-855-8392
E-mail: joyce@imf.la
Deadline :
www : <http://s3sconference.org/>

28 Jul - 31 Jul 2014

IEEE International Nanoelectronics Conference 2014

Conf Record :31843
Location: Sapporo , Japan
Contact : Kazuhiko Endo
Tel : +81-29-861-3857
Fax :
E-mail: endo.k@aist.go.jp
Deadline :
www : <http://>

04 Sep - 06 Sep 2013

2013 IEEE International Symposium on Low Power Electronics and Design (ISLPED)

Conf Record :31512
Location: Beijing , China
Contact : Pai Chou
Tel : +1 949 824 3229
Fax :
E-mail: phchou@uci.edu
Deadline : 25 Jun 2013
www : <http://www.islped.org/>

13 Oct - 17 Oct 2013

2013 IEEE International Integrated Reliability Workshop (IIRW)

Conf Record :31681
Location: South Lake Tahoe CA , USA
Contact : Jason Campbell
Tel : +1 301 975 8308
Fax :
E-mail: jason.campbell@nist.gov
Deadline : 13 Oct 2013
www : <http://www.iirw.org>

14 Sep - 17 Sep 2014

2014 IEEE Custom Integrated Circuits Conference - CICC 2014

Conf Record :18693
Location: San Jose CA , USA
Contact : Melissa Widerkehr
Tel : +1 301 527 0900
Fax : +1 301 527 0994
E-mail: melissaw@widerkehr.com
Deadline :
www : <http://www.ieee-cicc.org>

06 Sep - 06 Sep 2013

2013 e-Manufacturing & Design Collaboration Symposium (eMDC)

Conf Record :31329
Location: Hsinchu , Taiwan
Contact : Celia Shih

14 Oct - 16 Oct 2013

2013 International Semiconductor Conference (CAS 2013)

Conf Record :31015
Location: Sinaia , Romania
Contact : Cristina Buiculescu

06 Oct - 08 Oct 2014

2014 IEEE Bipolar/BiCMOS Circuits and Technology Meeting - BCTM

Conf Record :31342
Location: Chicago IL , USA
Contact :

Tel : +886 3 5917092
Fax : +886-3-5820056
E-mail: celia@tsia.org.tw
Deadline : 31 Jul 2013
www : <http://www.tsia.org.tw/seminar/eManufacturing2013/>

Tel : +40 21 269 0775
Fax :
E-mail: cas@imt.ro
Deadline : 01 Jun 2013
www : <http://www.imt.ro/cas>

Tel :
Fax :
E-mail:
Deadline : 18 Jul 2014
www : <http://http://iee-bctm.org/>

08 Sep - 13 Sep 2013
2013 23rd International Crimean Conference "Microwave & Telecommunication Technology" (CriMiCo)

Conf Record :31299
Location: Sevastopol , Ukraine
Contact : Yelena Red'kina
Tel : +380992858311
Fax :
E-mail: ElenaRedkina@gmail.com
Deadline : 10 May 2013
www : <http://www.crimico.org/en/>

21 Oct - 23 Oct 2013
2013 IEEE International Conference on Microwaves, Communications, Antennas and Electronic Systems (COMCAS)

Conf Record :30834
Location: Tel Aviv , Israel
Contact : Shmuel Auster
Tel : +972 8 857-5982
Fax :
E-mail: auster@ieee.org
Deadline : 01 Aug 2013
www : <http://www.comcas.org>

13 Oct - 14 Oct 2014
INTERNATIONAL CONFERENCE ON COMMUNICATION & NANO TECHNOLOGY

Conf Record :31570
Location: CHENNAI , India
Contact : Arun prasad
Tel : +919865413635
Fax :
E-mail: pgsrtswj@gmail.com
Deadline : 06 Sep 2013
www : <http://WWW.ICCNT-ECE.ORG>

08 Sep - 13 Sep 2013
2013 35th Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD)

Conf Record :31180
Location: Las Vegas NV , USA
Contact : Lisa Pimpinella
Tel : +1-315-339-6937
Fax :
E-mail: lpimpinella@esda.org
Deadline : 11 Jun 2013
www : <http://www.esda.org>

07 Nov - 09 Nov 2013
2013 International Workshop on Dielectric Thin Films for Future Electron Devices : Science and Technology (IWDTF)

Conf Record :30932
Location: Tokyo , Japan
Contact : Koji Kita
Tel : +81-3-5841-7164
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E-mail: kita@scio.t.u-tokyo.ac.jp
Deadline :
www : <http://home.hiroshima-u.ac.jp/iwdtf>

19 Oct - 22 Oct 2014
2014 IEEE Compound Semiconductor Integrated Circuit Symposium

Conf Record :31991
Location: San Diego CA , USA
Contact : Douglas McPherson
Tel : +1 613-670-3371
Fax :
E-mail: dmcphers@ciena.com
Deadline : 25 Jul 2014
www : <http://www.csics.org>

12 Sep - 13 Sep 2013
2013 International Siberian Conference on Control and Communications (SIBCON 2013)

Conf Record :30855
Location: Tomsk , Russia
Contact : Oleg Stukach
Tel : +73822260299
Fax : +73822260299
E-mail: tomsk@ieee.org
Deadline : 30 Jul 2013
www : <http://sibcon.sfu-kras.ru>

04 Dec - 07 Dec 2013
2013 IEEE 44th Semiconductor Interface Specialists Conference (SISC)

Conf Record :20912
Location: Arlington VA , USA
Contact : Alexander Demkov
Tel : +1 512 471 8560
Fax :
E-mail: demkov@physics.utexas.edu
Deadline :
www : <http://www.ieeesisc.org/>

10 Dec - 13 Dec 2014
2014 IEEE 45th Semiconductor Interface Specialists Conference (SISC)

Conf Record :31578
Location: San Diego CA , USA
Contact : Alex Demkov
Tel : +1 512 471 8560
Fax :
E-mail: demkov@physics.utexas.edu
Deadline : 20 Aug 2014
www : <http://www.ieeesisc.org/>

16 Sep - 20 Sep 2013
ESSDERC 2013 - 43rd European Solid State Device Research Conference

Conf Record :31895
Location: Bucharest , Romania
Contact : Stefan Rusu
Tel : +1-408-765-5739
Fax :
E-mail: stefan.rusu@intel.com
Deadline :
www : <http://essderc2013.imt.ro/>

09 Dec - 11 Dec 2013
2013 International Conference on Field-Programmable Technology (FPT)

Conf Record :30984
Location: Kyoto , Japan
Contact : Tomonori Izumi
Tel :
Fax :
E-mail: t-izumi@se.ritsumei.ac.jp
Deadline : 20 Sep 2013
www : <http://www.icfpt.org>

11 Dec - 19 Dec 2014
2014 IEEE International Electron Devices Meeting (IEDM)

Conf Record :11149
Location: San Francisco CA , USA
Contact : Ms. Phyllis W. Mahoney
Tel : +1 301 527 0900 (Ext.103)
Fax : +1 301 527 0994
E-mail: phyllism@widerkehr.com
Deadline :
www : <http://>

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*Samar Saha
EDS Vice-President
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Semiconductor Physics

Question 058-13

While simulating superlattice (e.g. QCL) structures, should we consider band bending at junctions?

*Samar Saha
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