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Technical Briefs

Reliability Trends of Nano-scaled CMOS Devices

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With the continuous downscaling of CMOS technologies, reliability is more and more becoming a major bottleneck and this for several reasons. First of all the electric fields and current and power densities have increased continuously and are now reaching the maximum values that can be allowed for reliable operation. At the same time an impressive effort is taking place introducing new materials and novel device architectures to maintain the effective performance scaling. New materials like high k dielectrics and metal gates for both logic and memory technologies and novel device concepts such as Multiple gate FET's have already been introduced, while Ge or III-V materials for high mobility devices are under investigation. These new materials and devices often have unknown reliability behavior and/or introduce new failure mechanisms, whereas their speed of introduction exceeds the capabilities to explore their reliability performance in great detail. Finally, the market is continuously demanding higher reliability levels, with single digit failure rates in FIT units (1 FIT = 1 failure per 10^9 operating device hours) for present technologies. In the past, the technological reliability margins that were available to achieve the required failure rate levels were always sufficiently high, but in some of the technologies under development this becomes more and more cumbersome. In this technical note we review the evolution of reliability for nanoscaled technologies, and we show that for some failure mechanisms the lifetime can no longer be guaranteed. As a result alternative ways of reliability assurance will become necessary.

As an example of the trends in the electric fields existing in the transistors under operating conditions, Fig. 1 shows the evolution over the past 40 years of the oxide and silicon fields as a function of the gate length [1].

(continued on page 3)

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Reliability Trends of Nano-scaled CMOS Devices

(continued from page 1)

Clearly 3 periods can be distinguished: a first constant voltage scaling period in the seventies and eighties, in which the power supply voltage was not reduced when scaling the geometries, and consequently the fields increased continuously with scaling. This was followed by a more or less constant field scaling period, in which the power supply voltages were reduced with every new technology node, so that the fields saturated at a certain plateau. Since the 65 nm node, however, the power supply voltages are saturating at a level around 1 V, and can no further be reduced because of the non-scaling sub-threshold slopes of the MOSFET's. As a result we observe again a further increase in the electric fields, which starts to put new constraints on the reliability of the devices. Moreover, the power density has also continuously increased, which leads to higher chip temperatures, and consequently even a stronger acceleration of the degradation mechanisms. All of this leads to a strong reduction of the reliability margins for most failure mechanisms.

Until now, reliability assessment and assurance was mainly carried out at the technology level, through accelerated testing for each major failure mechanism. Accelerated test methodologies and models have been developed and are available for most failure mechanisms such as hot carrier degradation, Time-Dependent Dielectric Breakdown, Bias-Temperature Instability (BTI)], electromigration, stress voiding, interconnect dielectric instability and breakdown.

Due to the trends discussed above, however, reliability margins of these failure mechanisms are reduced, in some cases even to zero. As an example, Figure 2 shows the 10 year over-drive voltage to be decreasing with reducing EOT [2].

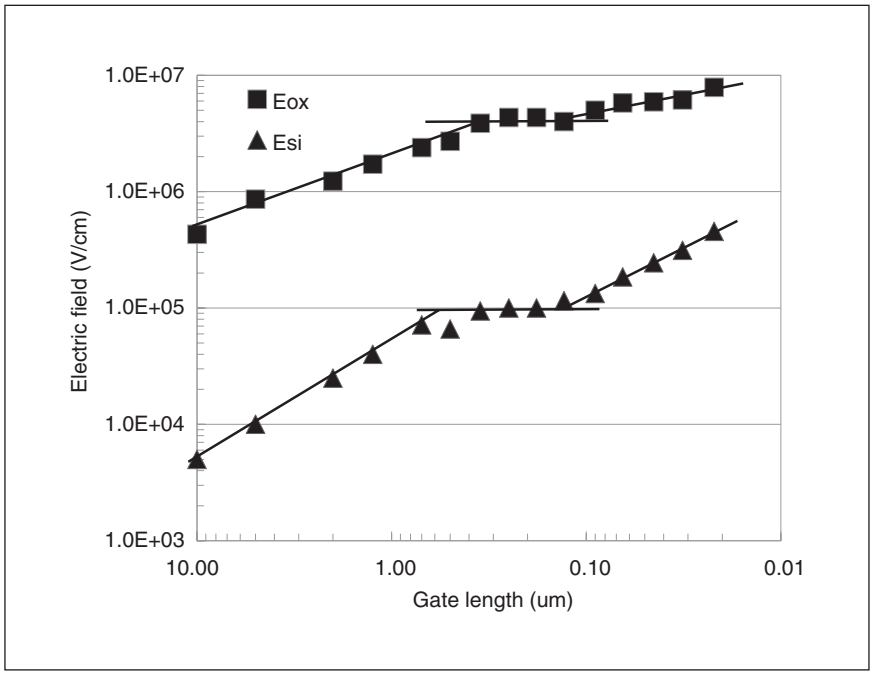

Fig. 1. Evolution of oxide and silicon electric fields showing 3 different scaling scenario periods [1]

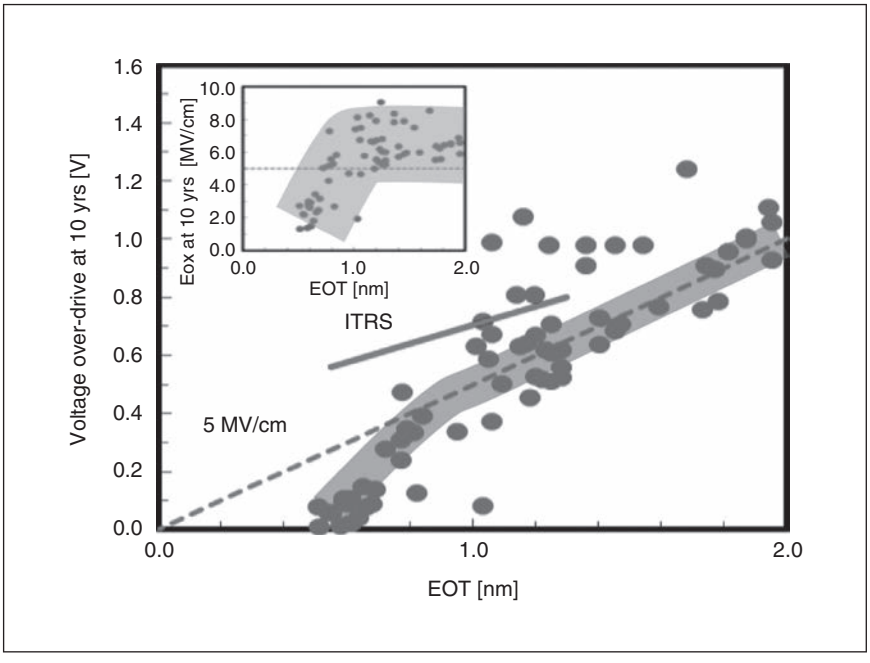

Fig. 2. Evolution of p-MOSFET NBTI over-drive voltage at 10 years. ITRS roadmap data is also added. [2]

This figure shows that the extrapolated gate overdrive at 10 year is linearly dependent on EOT. The expected NBTI overdrive versus EOT is shown by the dotted iso-electric field line of 5 MV/cm. However, it

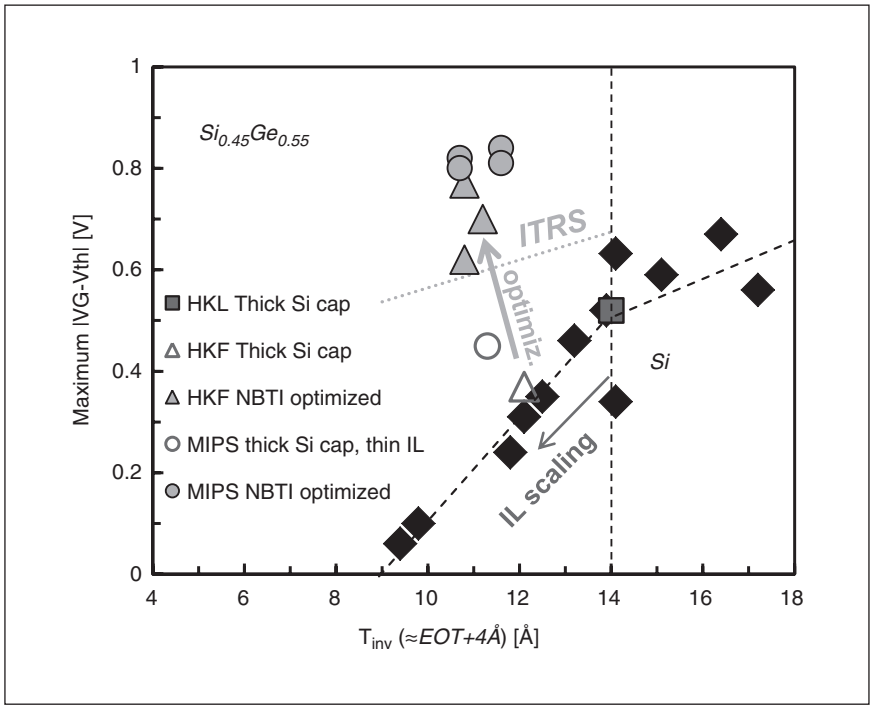

Fig. 3. Optimized SiGe devices boost the maximum operating overdrive to meet the target V_{DD} at ultra-thin EOT.

is clearly observed that below 1 nm EOT the NBTI degradation is faster than expected. The extrapolated operating field at 10 year lifetime is plotted versus the EOT in the inset in Figure 2. Conversely to ITRS specifications, the devices below 1 nm EOT show a rapid decrease in the maximum operating field. The strong electric field dependence change below 1 nm suggests a different or additional NBTI degradation mechanism in the sub 1-nanometer EOT regime. We have found the additional mechanism for this severe degradation in sub-nanometer EOT devices to be the increased bulk charge trapping effect enhanced by the reduced interfacial layer [2]. This means that it will become more and more difficult to guarantee the lifetime of the transistors as it was done before using the classical accelerated testing approaches.

There are some technology solutions available for the dramatic reduction in BTI lifetime. One of them is the use of SiGe-based devices, which are not only investigated to boost the performance by their higher mobility, but also promise a significantly improved NBTI robustness, as is illustrated on Fig. 3. To benefit from this property, the SiGe quantum well devices were optimized for enhanced reliability, including a high Ge fraction in the channel, a sufficiently thick quantum well and a Si passivation layer of reduced thickness [3, 4]. By means of such optimization, sufficiently reliable ultra-thin EOT SiGe pMOSFETs with a 10 year lifetime at operating conditions in both gate-first and gate-last process flows were demonstrated, as shown on Fig. 3 [5].

Nevertheless because of such reduced reliability margins in the future we will have to learn to design reliable circuits with unreliable components. Interaction with the design community to fine-tune the lifetime assessment and using realistic circuit-based failure criteria becomes mandatory [6].

On top of this trend another one is observed in reliability assessment, namely the impact of increasing statistical variability of the degradation effects, comparable to the well-known increasing variability of the initial parameters. Until now, the large, micrometer-sized FET devices of the past CMOS technologies were considered identical in terms of electrical performance. Similarly, the application of a given stress resulted in an identical parameter shift in all devices. With the gradual downscaling of the FET devices the oxide dielectric was the first to reach nanometer dimensions, thus introducing the first stochastically distributed reliability mechanism—the Time Dependent Dielectric Breakdown. With the shrinking of lateral device dimensions to sub-22 nm levels, variations between devices start to appear due to effects such as random dopant fluctuations and line edge roughness [7, 8]. Similarly, application of a fixed stress in such devices results in a distribution of the parameter shifts [9, 10]. Understanding these distributions is crucial for correctly predicting the reliability of future deeply downscaled technologies [11].

In such deeply downscaled CMOS technologies only a handful of defects is present in each device, while their relative impact on the device characteristics is significant. The behavior of these defects is stochastic, voltage and temperature dependent, and widely distributed in time, resulting in each device behaving very differently during operation. Fig. 4 shows a typical result of a Measure-Stress-Measure (MSM) measurement of a relaxation transient following NBTI (Negative-Bias-Temperature Instability) stress. Clear steps caused by single discharge events are visible in the NBTI relaxation transients. For larger device sizes these relaxation transients are continuous and spread over several decades in time. In this case, however, the average step height is significantly larger than reported earlier. It is important to note here that the steps corresponding to a single discharging event in some devices

exceed 30 mV, the BTI lifetime criterion presently used by most groups, which means that 1 single charge can cause threshold voltage shifts as high as the failure criterion. The histogram of the step heights is shown on Fig. 4b.

This trend leads to a shift in our perception of reliability: the "top-down" approach (deducing the microscopic mechanisms of average degradation in large devices) is being replaced in deeply-scaled devices by the "bottom-up" approach, in which the time-dependent variability of several degradation mechanisms, such as RTN and BTI, is understood in terms of charging and discharging of individual defects.

Values of ΔV_{th} caused by individual defects appear to be approximately exponentially distributed in our devices (Fig. 4b) [12,13] The average ΔV_{th} value of the distribution η scales inversely with device area but is expected to improve with lower channel doping concentrations. The knowledge of single defect impact distribution, combined with the assumption of Poisson-distributed number of defects per device, allows predicting the distribution of the total degradation per device [12,13] and projecting the fraction of failing devices at 10 years, as is shown on Fig. 5 [11]. This figure clearly shows the trend: for large area devices, like in the past, all devices behave identical and have one single predicted maximum overdrive voltage. But for nanoscaled devices, although the median of the devices has the same maximum overdrive as the large area devices, there is a huge tail towards lower maximum overdrives. This poses new challenges on the reliability assessment and assurance of such nanoscaled technologies.

In conclusion, it is generally accepted that reliability margins assessed using the classical method are rapidly vanishing. This becomes more critical when in the near future the use of high-mobility channels will be considered for further device performance enhancement in future CMOS technology nodes. (Si)Ge and III-V based quantum well devices are the first candidates for p- and n-type

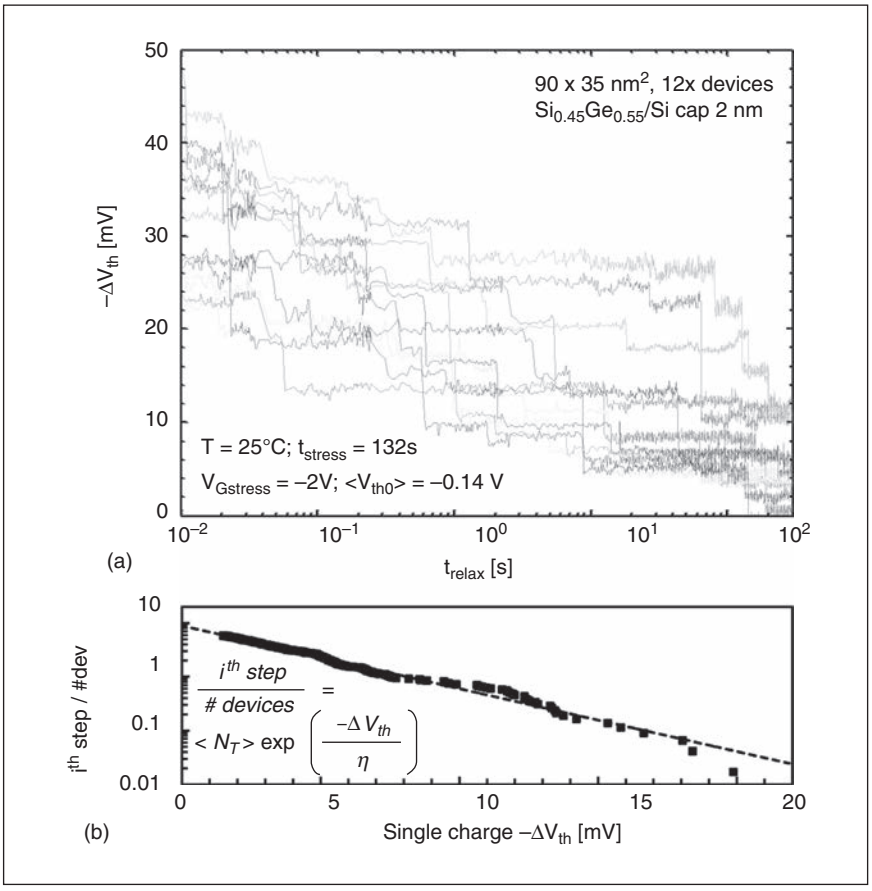

Fig. 4. (a) NBTI relaxation transients recorded on nanoscaled SiGe devices. (b) Weighted complementary Cumulative Distribution Function (CCDF) plot of the individual ΔV_{TH} step heights observed on multiple devices. The average number of defects per device, $\langle N_T \rangle$, can be easily read in this plot as the intersection of the distribution with the y-axis [11].

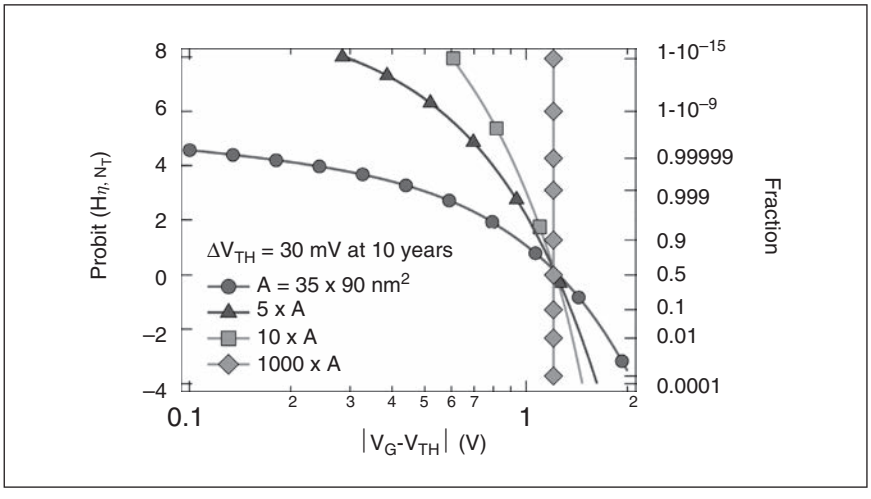

Fig. 5. Predicted 10 years maximum overdrive cumulative distributions of the pFET for ΔV_{th} = 30 mV at t_{relax} = 1 ms for various device area. The median overdrive is independent of device area, but a significant fraction exceeds failure criteria at lower overdrives as the device area decreases [11].

channels, respectively. Although promising drive current performance has been reported for these devices by several groups, much less information on their reliability is available. Nevertheless, it is mandatory that, besides good performance and mobility, also sufficient reliability can be guaranteed before these Beyond-Silicon devices can be considered for production.

Next to this, the increasing systematic and statistical variability caused by the stochastic nature of the failure mechanisms will have to be considered in the design of future ULSI circuits. To that end, the time dependence of the parameter distributions during circuit operation, after being thoroughly understood, will need to be inserted into circuit simulators. Recent work has shown very strong workload-dependent characteristics in the aging of scaled devices and wires. As a result a need has emerged for mixed statistical-deterministic modeling approaches [6] as opposed to the early worst-case modeling or more recent statistical modeling options.

Reliability assessment of future applications can thus be seen as time-dependent variability analysis. All this will ultimately lead to a paradigm shift in the reliability assessment and assurance of future technologies, circuits and systems, which will have to be guaranteed at the system design level rather than at the device and technology level. Research is underway to develop such reliability-aware design methodologies [15] which will change the operation conditions of the critical transistors during runtime.

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Guido Groeseneken is an IMEC Fellow and Professor at the KU in Leuven, Belgium, where he is Program Director of European Erasmus Mundus Master program in Nanoscience and nanotechnology. He is responsible for research in reliability physics for deep submicron CMOS technologies at IMEC and has made contributions to the fields of non-volatile semiconductor memory devices and technology, reliability physics of VLSI-technology, hot carrier effects in MOSFET's, time-dependent dielectric breakdown of oxides, Negative-Bias-Temperature Instability effects, ESD-protection and—testing, plasma processing induced damage, electrical characterization of semiconductors and characterization and reliability of high k dielectrics. Recently he has also interest in nanotechnology for post-CMOS applications, such as carbon nanotubes for interconnect and sensor applications, tunnel FET's for alternative ultra-low power devices. He has served as a technical program committee member of several international scientific conferences, IEDM, IRPS, IEEE SISC, European Solid State Device Research Conference (ESSDERC) and the EOS/ESD Symposium. From 2000 until 2002 he also acted as European Arrangements Chair of IEDM. He was the General Chair of the Insulating Films on Semiconductor (INFOS) conference in 2005. From 1999 until 2006 he was an editor of IEEE Transactions on Electron Devices. Since January 2005 he is elected to the grade of IEEE Fellow.

Report on 2015 IEEE International Reliability Physics Symposium

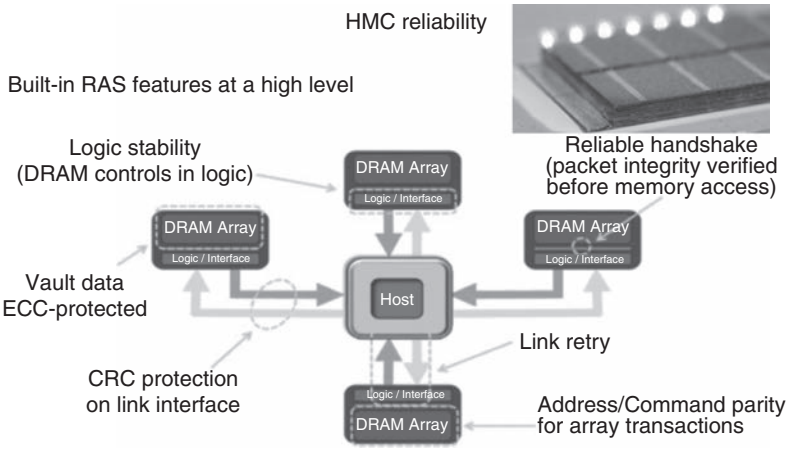
The IRPS15 held from April 19–23, 2015, at the Hyatt Regency Monterey Resort and Spa, Monterey, California, USA, serendipitously kicked off exactly on the 50th anniversary of Moore's Law on April 19th which was recognized in IEEE Spectrum's April publication. The key question with respect to reliability—can Moore's Law continue and not be limited by reliability? IRPS15 technical program kicked off with keynotes by Kaizad Mistry of Intel and Brent Keeth of Micron respectively addressing these topics.

Kaizad Mistry illustrated Dennard's classical scaling which was applicable through the late 1990's and how a "golden age of innovation" was occurring with advent of strained silicon, high-K metal gate, and tri-gate (fin-fet) introduction in the 21st century. Improvements in reliability mode data of time dependent dielectric breakdown (TDDB), bias temperature instability (BTI), and soft error were reviewed.

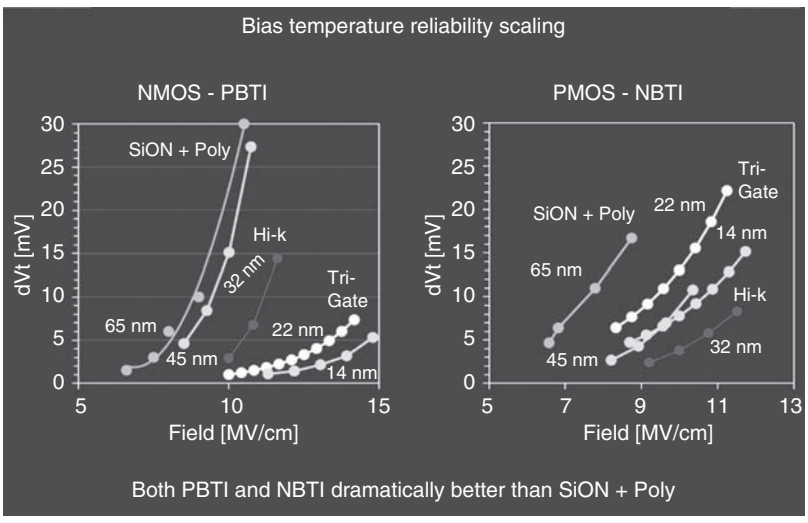
Brent Keeth presented dynamic random access memory (DRAM) performance and scaling, citing the need for a dramatic performance changes to ready 1 TB/s bandwidth, reduced energy consumption of 5mW/GB/s, and x-scale computing of 1018 Flops/s. A radical rethinking of DRAM design to utilize tightly stacked memory in through silicon vias (TSV) coupled with a logic layer to manage the memory and communications with the host which included reliability, availability, and serviceability (RAS) features. These keynotes provided excellent introduction to the technical program and substantial motivation towards continual enabling of reliability aspects of Moore's Law!

IRPS15 technical program featured reliability topics focusing on the continued advancement of Moore's Law with several 14 nm and many FIN- FET papers from industry leaders. The technical program kicked off with a first-ever combined gate dielectrics and back-end-of-line (BEOL) breakdown session which was highly attended. As dimensions have been scaled continuously, new considerations for interconnect dielectric breakdown must be made in addition to traditional electromigration reliability. Wednesday's evening poster session, in the Monterey Grand Ballroom, featured over seventy-five poster presentations accompanied by delicious dinner selections. Conference proceedings

Kaizad Mistry, VP Intel, delivering keynote "Transistors and Reliability in the Innovation Era."



Brent Keeth, Senior Fellow Micron, delivering keynote "Hybrid Memory Cube (HMC): Achieving High Performance and High Reliability" and Hybrid Memory Cube built in reliability, availability, and serviceability (RAS) features (courtesy Brent Keeth, Micron).



BTI reliability scaling by process generation showing effectiveness of innovation in making improvements in reliability with scaling (courtesy Kaizad Mistry, Intel).

are available in the *IEEE Xplore Digital Library*. The "best of IRPS15" will be announced on Twitter.

The next IRPS will be held in Pasadena, California, April 17–21, 2016. Call For Papers have been issued with an abstract deadline of October 12, 2015, and late news submissions due January 11, 2016. Please follow on Facebook, Linked-IN, Twitter @IEEEIRPS, and visit http://IRPS.org for latest information. The Device Reliability team looks forward to seeing you in Pasadena for IRPS16!

Chris Connor, Yuan Chen and Giuseppe LaRosa
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Wide Bandgap Semiconductors, They're Special

Recent advances in wide band gap semiconductors (typically compound, like Gallium Nitride (GaN) and Silicon Carbide (SiC), but also elementary, like Diamond) for power applications were a big hit during the IEDM 2014 conference. The IEDM invited plenary speech by J.W. Palmour of Cree, showed impressive data on the yield and performances of SiC devices on 15 cm substrates—micro-pipes still are a threat but their density has decreased so much that yield is almost unaffected. The presentation included an unusual testimonial for widegap semiconductors. US President Barack Obama himself in a speech held at NCSU on January 15, 2014, supporting a $140 million proposal to bring a manufacturing innovation hub to Raleigh, with

Jayant Baliga as a principal investigator. "Wide bandgap semiconductors, they're special because they use up to 90 percent less power; they can operate at higher temperatures than normal semiconductors. So that means they can make everything from cell phones to industrial motors to electric cars smaller, faster, cheaper. There are still going to be applications for traditional semiconductors, but these can be focused on certain areas that will vastly improve energy efficiency, vastly improve the quality of our lives." See the transcript of Barack Obama's speech, http://www.bizjournals.com/triangle/transcript-of-president-obamas-speech.html?page=all .

As pointed out by Prof. Baliga in the invited paper *Social Impact of Power Semiconductor Devices,* those play a fundamental role in a sustainable society and involve an impressive range of applications, from transportation to air conditioning and refrigeration to lighting. Two-digit improvements in efficiency have led, during the last 20 years, to staggering results in terms of energy consumption and decrease in carbon dioxide emissions.

Cars are one of the major sources of carbon dioxide emission and 93.5% of the energy used for transportation is based on fossil fuels. This could be improved in the future with a more widespread use of Hybrid Electrical Vehicles (HEV) and EVs. Researchers from Toyota Central R&D Labs presented a novel SiC vertical JFET for automotive applications, allowing for a 50% reduction of switching losses vs. conventional MOSFETs. Despite their impressive performances, widegap semiconductor power devices based on SiC or GaN should be targeted towards specific applications where they bring real advantages in terms of performance but also cost vs. Si. A complex SWAT analysis of different technologies for power switching is discussed, by researchers from Infineon. In a nutshell, Si still dominates for low price applications, SiC for high-end, high voltage applications, GaN (but only in the GaN-on-Si variety) for high-end and medium voltage applications.

Widegap power semiconductor devices will also play a fundamental role in smart power grids. SiC devices with ultrahigh breakdown voltage (>10 kV) for UHV applications in power grids (researchers from Kyoto University, AIST and Kansai Electric Power). An optimized PiN SiC process is described with high temperature performances up to 250 C and 70% expected power reduction expected vs. Si converters operating at a switching frequency of 2 kHz.

GaN has become widespread in our homes thanks to the introduction of GaN-based LED high-efficiency lighting (as recognized by the recent Nobel prize in physics to Isamu Akasaki, Hiroshi Amano and Shuji Nakamura), but very soon domestic appliances exploiting GaN power devices will become widespread, at least in Japan. PV conditioners using 600 V GaN-on-Si devices will be sold on the Japanese market starting January 2015. The PV conditioner exploits a JEDEC-qualified GaN-on-Si process using a cascode configuration with a normally-off Si MOSFET. The 1500 V breakdown voltages ensures reliability in the targeted 600 V application, with a 40% loss reduction and size reduction when compared to a Si implementation; the switching frequency is 27 MHz and careful packaging alleviates EMI problems. In the future, 900 V e-mode devices will be on the market.

Bulk GaN substrates could be the ultimate solution for GaN electronics, in particular for vertical devices. Researchers from the Advanced Research Projects Agency show an overview of available widegap power solution, having in mind a target price of 0.1 $/A at 40 KHz switching frequency. Contrary to common belief, the SiC solution is not necessarily more expensive than the Si one—the cost is higher but also the power density is larger. For GaN-on-GaN vertical devices, the current solutions are monothermal GaN boules or GaN transferred substrates obtained by epitaxial lift-off.

A last area of interest is diamond power electronics, for which the main challenge remains n-type doping in bipolar diodes and transistors. A possible solution for power diamond devices avoiding the issues related to doping is the surface H-termination (already proposed about 20 years back), that induces a surface 2D hole gas, allowing for the development of diamond-based MESFETs and MOSFETs. Very good results in terms of stability and high-voltage operation were presented by Waseda University researchers. The technology exploited here is a MOSFET with an Al2O3 layer. The proposed process also has good properties in terms of high-temperature behavior up to 400 C.

IEDM 2014 had sessions where many technological developments were reported, and the contribution of the session invited speakers well summarized the contents of the sessions: Dr. Tetsu Ueda, from Panasonic reported on the potential of the GaN HEMTs in the power switching applications. Prof. Gaudenzio Meneghesso, from the University of Padova, provided an important overview of the most critical parasitic effects today present in these devices that need to be taken care of, to allow for a large market penetration.

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Gaudenzio Meneghesso
University of Padova

Upcoming Technical Meetings

2015 IEEE International Integrated Reliability Workshop (IIRW)

The 2015 IEEE International Integrated Reliability Workshop (IIRW), sponsored by the IEEE Reliability Society and the IEEE Electron Devices Society, will be held at the Stanford Sierra Conference Center on the shores of Fallen Leaf Lake near South Lake Tahoe, California, October 11–15, 2015. This workshop provides a unique forum for open and frank discussions of all areas of reliability research and technology for present and future semiconductor applications.

Some of the highlights of this year's technical program will include:

- A **keynote** speech on Product Reliability given by Prasad Chaparala, Director, Hardware Reliability Engineering, Amazon Lab 126
- A strong collection of **invited** speakers including (but not limited to): John Conley Jr. (Oregon State University)—Dielectric Stack Engineering; Christian Shweta Deora (Sematech)—RRAM Reliability; JH Lee (TSMC)—FEOL Reliability; Sang-Woo Pae (Samsung)—FEOL Reliability; Pieter Wechx (IMEC)—RTN and BTI time-dependent reliability, John Robertson (Cambridge University)—Reliability of III-V MOSFETs
- A strong **tutorial** program will cover many hot reliability topics including (and not limited to) radiation effects on devices including non-volatile memories, 14 nm node FinFET reliability, LDMOS reliability & modeling, reliability of power GaN devices, physical analysis of device degradation (TEM, STM, CAFM etc.).
- On Sunday (first) night "tech lite" presentation: Brian Schratz, Lead Engineer, Entry Descent and Landing Telecommunications Team, **Mars Curiosity Rover**, JPL-NASA

View of Fallen Leaf Lake from the ski dock at the Stanford Sierra Conference Center. The Stanford Sierra Conference Center provides lodging, meals and meeting facilities as well as excellent recreation including hiking in the Desolation Wilderness and boating on Fallen Leaf Lake

The IIRW is also an excellent forum to present new and original technical works. Reliability topics for the workshop include: SiGe and strained Si, III-V, SOI, high-k and nitrided SiO2 gate dielectrics, reliability assessment of novel devices, organic electronics, emerging memory technologies (RRAM etc.) and future "nano"-technologies, NEMS/MEMS, photovoltaic's, transistor reliability including hot carriers and NBTI/PBTI, Cu interconnects and low-k dielectrics, product reliability and burn-in strategy, impact of transistor degradation on circuit reliability, reliability modeling and simulation, optoelectronics, single event upsets, as well as the traditional topics of wafer level reliability (WLR) and built-in reliability (BIR). The Call for Papers can be found at the web address (www.iirw.org). The abstract submission deadline is July 12, 2015. Contact the Technical Program Chair, Richard Southwick (southwick@us.ibm.com) for further details. Also, visit www.iirw.org for continued updates about the conference. Also note that all attendees have the opportunity to present a "walk-in" poster of their latest work. This is a great way to share that new project you are working on and to get world-class feedback.

IIRW is fairly different from a typical technical conference. Located 6000 ft. high in the Sierra Nevada Mountains, the Stanford Sierra Conference Center provides an ideal atmosphere for a relaxing yet informative workshop. Nestled throughout the pines and cedars along the shoreline of Fallen Leaf Lake, attendees stay in cabins furnished in the

rustic style of an alpine resort. All cabins have decks with magnificent views of Fallen Leaf Lake and the surrounding Sierra peaks. Comfortable, informal dress is encouraged, affiliations are downplayed, and meals are provided family-style in the lodge dining room.

All aspects of the workshop, including the physical isolation of the venue, the absence of distractions such as in-room phone and televisions, and the format of the technical program encourage extensive interaction among the workshop attendees. Such opportunity is seldom available at most other conferences. Participants spend their evenings at poster sessions, discussion groups, and special interest groups, all complemented with refreshments and snacks. The evening moderated discussion groups provide a forum with unparalleled access to world experts to discuss a wide array of relevant reliability issues. Often these discussions lead to the formation of a smaller special interest group, whose discussions extend long after the conclusion of the workshop.

The technical program is purposely kept open for Wednesday afternoon to allow attendees to enjoy a variety of the outdoor activities which the Stanford Sierra Conference Center location has to offer. These include hiking, sailing or kayaking, walking, or simply continuing that intriguing conversation from the night before. This free afternoon is a great way to not only network, but also to build long-lasting friendships.

Additional information about the workshop is available on the IIRW website at www.iirw.org, or by contacting Jason Ryan, NIST, 2015 IIRW General Chair, (Jason.ryan@nist.gov) Note: If you want to take part in this event, please register early as space at the Stanford Sierra Conference Center is limited to roughly 120 attendees and the workshop has sold out in the past.

On behalf of the 2015 IIRW Committee, I look forward to meeting you in Lake Tahoe!

Barry O'Connell
2015 IIRW Communications Chair
Fairchild Semiconductor
San Jose, CA, USA

2015 IEEE Compound Semiconductor IC Symposium (CSICS)

October 11th–14th in New Orleans, Louisiana

The 2015 IEEE CSICS will be held on October 11th–14th at the Sheraton Hotel located in New Orleans, Louisiana, USA.

The Compound Semiconductor IC Symposium (CSICS) covers GaN, GaAs, InP, SiGe, and nanoscale CMOS technologies and their application to microwave/mm-wave, THz, analog mixed signal, power conversion, and optoelectronic IC design. Now in its 38th year, CSICS has become the premier symposium at which to present state-of-the-art results in the areas of circuit switching speed, RF frequency of operation, RF output power, PA efficiency, and noise performance. The symposium also showcases the latest advances in emerging semiconductor device technology, modeling and manufacturing.

The symposium includes a three day dual track technical program, two short courses, a primer course, and a technology exhibition. Also, for the 2nd year, CSICS will offer a student paper competition. The technical program includes 60–70 high quality papers and 4 topical panel sessions. This year, CSICS is proud to announce 20 internationally renowned invited speakers, notably: Pascal Chavalier (ST), Jesus del Alamo (MIT), Eric Lind (Lund Univ.), Akira Nakajima (AIST), Masataka Higashiwaki (NICT), Thomas Zimmer (University of Bordeaux), Bruce Wallace (DARPA), Zoya Popovic (University of Colorado, Boulder), Ian Betty (Ciena), John Volakis (Ohio State University), Ken Brown (Raytheon),

Patrick Courtney (Qorvo), Bill Deal (Northrop Grumman), Kazuhiko Honjo (The University of Electro-communications, Japan), Shogo Yamanaka (NEC), Takayuki Shibasaki (Fujitsu), Sam Palermo (Texas A&M), Nomand Wolf (HHI), Michel Poulin (TeraXion), and Efthymios Rouvalis (Finisar). These distinguished speakers will present the latest advances in SiGe BiCMOS, InGaAs MOSFET's, nanowire FET devices, E-mode GaN HEMT's, device modelling, mm-wave/THz PA's and systems, spatially combined PA's, envelope tracking PA's, and low power RX and TX circuits and DSP's, as well as Si and InP modulators and drivers.

CSICS offers two in-depth short courses on Sunday, October 11th. The first course, Transmit and Receive IC Design for Fiber Optic Links, will be presented by leading experts: Linh Nguyen (Finisair), Kumar Lakshmikumar (Cisco), and Mark Webster (Cisco). This course details high-speed analog IC design basics for electronic and optoelectronic applications. The course will prove invaluable for anyone involved in high speed electronic or optoelectronic devices, circuit design, or systems.

The second course, Microwave Package Design Fundamentals, will be taught by leading high speed packaging experts. This course will cover the basics of microwave packaging for high speed and high power microwave applications. It will cover the packaging materials and technologies, assembly techniques, and design considerations for packaging high frequency microwave and mm-wave devices. It will be useful for device, circuit, and system designers.

On Sunday evening, Waleed Khalil (Ohio State), will teach an expanded Primer Course on Si RFIC design. This 3.5 hour lecture is intended for participants of all technical backgrounds who wish to learn or refresh their understanding of the fundamentals of designing the principal circuit building blocks in radio and radar SoCs. Among the blocks covered are PAs, LNAs, Mixers, VCOs, as well as integrated passives, with examples drawn from both CMOS and SiGe technology. The primer is an excellent way to start the symposium and is guaranteed to enhance attendee appreciation of the technical program.

In recognition of the exceptional contributions made by students, CSICS is proud to hold its second Student Paper Competition. To participate in the competition, an eligible student must submit a regular contributed paper naming, at a minimum, themselves and their principal supervisor as authors. The Student Paper Finalists must present their own papers at their assigned symposium session.

For registration and up-to-date information, please visit the CSICS website at www.csics.org. Further questions may be addressed to the Symposium Chair: Dr. Charles F. Campbell, Phone: +1 972 994-3644, e-mail: Charles.Campbell@qorvo.com.

We hope you can attend, 2015 IEEE CSICS Organizing Committee

Bruce Green
CSICS 2015 Publicity Chair

2015 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)

Boston Hyatt, Boston, MA, USA

www.ieee-bctm.org

Short Course: Monday, Oct. 26, 2015,
Conference: Tuesday–Wednesday, Oct. 27–28, 2015

Jean-Baptiste Begueret

Doug Weiser

Invitation to IEEE BCTM 2015

On behalf of the IEEE BCTM'15 Executive Committee, we are honored and delighted to invite you to the 2015 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) at the Boston Hyatt, Boston, Massachusetts, October 26–28, 2015. We invite you to participate at the 2015 BCTM where the highlights include:

- Keynote addresses "**5G Systems**" by Dr. Yukihiko Okumura of NTT DOCOMO
- Day-long short-course on **How to Make Great RF Products Using BiCMOS Technologies**
- Guofo Niu (Auburn University): Device Physics and Optimization for RF Applications
- Colin McAndrew (Freescale): Models for RF Circuit Simulation: Capabilities and Shortcomings
- Lawrence Larson (Brown University): Design fundamentals for RF Transmitters and Receivers
- Freek van Straaten/Henk Thoonen (NXP): Packaging Challenges for RF

- Forward-looking **Emerging Technologies Session** with invited speakers: Dieter Knoll (IHP) on "Photonic BiCMOS technology" and Pascal Chevalier (STMicroelectronics) on "14 nm FDSOI and HBT integration feasibility"
- Invited papers exploring advances in process technology, device physics, wireless design, analog/mixed-signal, and modeling
- Technical papers covering the latest advances in physics, design, performance, fabrication, characterization, modeling, and application of Si/SiGe/SiC bipolar, BiCMOS, and GaN ICs
- Evening dinner banquet

The IEEE BCTM is a forum for technical communication focused on the needs and interests of the bipolar and BiCMOS community. Papers covering the design, performance, fabrication, testing and application of bipolar and BiCMOS integrated circuits, bipolar phenomena, and discrete bipolar devices are solicited. A Special Issue of the *IEEE Journal of Solid-State Circuits* will include selected papers from BCTM 2015.

General Contact Information
Visit the conference website www.ieee-bctm.org or contact Catherine Shaw, Conference Manager: Phone: 1-732-501-3334, e-mail: cshaw.cmpevents@gmail.com

The IEEE BCTM is the world's premier forum focused on the needs and interests of the bipolar and BiCMOS community. If you are interested in leading edge bipolar/BiCMOS devices and technology, circuits, and applications, as well as networking with experts in these areas, please kindly join us this year in the beautiful city of Boston, MA, USA.

Jean-Baptiste Begueret
2015 BCTM General Chair
University of Bordeaux

Doug Weiser
2015 BCTM Technical Program Chair
Texas Instruments

Society News

EDS Vision and Mission Statements

Vision Statement
Promoting excellence in the field of electron devices for the benefit of humanity.

Mission Statement
To foster professional growth of its members by satisfying their needs for easy access to and exchange of technical information, publishing, education, and technical recognition and enhancing public visibility in the field of Electron Devices.

EDS President's Message

Albert Wang
EDS President

Dear Fellow EDS Members,

I am writing this Message in the air, which reminds me of two things: time does fly at a speed certainly not slower in an airplane and our volunteers are busy with their day jobs. Therefore, this Message should be informative, yet short.

Our last year-end Board of Governors (BoG) meeting series was held December 13–14, 2014, in San Francisco. As usual, several group working meetings were held on Saturday, December 13th, including all Standing Committee meetings and some Technical Committee meetings, i.e., the Power Devices and ICs Committee meeting and the Optoelectronic Devices Committee meeting. The BoG general meeting was held on Sunday, December 14th. Following a new format, the BoG meeting had a one-hour Open Forum session for all attending volunteers to discuss general issues of interests to EDS. The December BoG meeting was very fruitful and covered many critical issues.

One topic that attracted lots of attention was on developing new Editor-in-Chief (EIC) Selection and Evaluation Procedures for the EDS journals including *IEEE Transactions on Electron Devices (T-ED)*, *IEEE Electron Device Letters (EDL),* and the *IEEE Journal of the Electron Devices Society (J-EDS).* As a brief background, this new EIC selection proposal development task is part of the effort that I have been pushing for, aiming to ensure transparency of EDS operations in response to EDS members' voices recently. Believe or not, EDS does not have a formal written policy for its journal EIC evaluation and selection. A task force, led by Samar Saha (past VP for Publications) and Bin Zhao (VP for Publications and Products), was formed to investigate the details and to develop new formal EIC Selection and Evaluation Procedures.

There were extensive discussions among volunteers on this EIC selection matter during the Publications and Products Committee (PPC) meeting and BoG general meeting in San Francisco. Various comments and opinions on the EIC selection matter have been expressed during the meetings in San Francisco and after that, which clearly indicated that the EIC selection issue is a critical matter to our members and the existing EIC selection practices have room for improvement. As a result, two resolutions were recently approved by the PPC committee and the EDS Forum: first, the new "working" EIC Selection Proposal will be used for the immediate task of EIC selection for T-ED and EDL; second, a parallel process will continue for the PPC committee to develop and finalize the final written EIC Selection and Evaluation Procedures for future use, which will be submitted to the Forum and BoG for approval before the end of 2015. I want to remind all EDS members that the goal of this EIC selection proposal task is about transparency of EDS operations, fair opportunities for members, spirits of rotation for volunteer services, and avoiding potential conflict of interests. At this time, all EDS members should have received several email notices about nominations for the current TED and EDL EIC Search. I appreciate your active participation in this critical business.

Operations transparency is also a heated topic at IEEE level. It has drawn lots of attention recently, with the main focus on IEEE finance transparency. Largely initiated by a presentation on EDS incomes and the growing IEEE TAB support fees by then EDS President, Paul Yu, at the IEEE Technical Activity Board (TAB) meeting in February 2013, a group of five IEEE society presidents, including EDS, started to work together to lead the effort to push for IEEE finance transparency. An Ad Hoc IEEE Fin-Trans task group was formed in early 2014 to focus on this major task, and presented its analysis and motions at each IEEE TAB meeting since February 2014. We are seeing progresses now, though slowly. The IEEE finance team has been cooperating with the Fin-Trans Ad Hoc by providing IEEE financial data to selected societies for analysis on a trial basis. As volunteers who dedicate our time and effort to IEEE professional activities, we certainly deserve a transparent picture of IEEE finances. Considering the volunteer and rotating nature of member services, this Fin-Trans effort is deemed to be a challenging task. I will continuously update you on this matter.

The EDS mid-year Governance meeting series was held May 30–June 1, 2015 in Singapore. To encourage more active participation from EDS members, a two-hour Open Forum session was arranged for volunteers to discuss any EDS related issues. For a summary of the Governance meeting, see pages 16 and 17. To conclude this Message, I encourage you to write to me for any of your concerns and comments on EDS business.

Sincerely,
Albert Wang from Southern California

Albert Wang *is a Professor of Electrical and Computer Engineering at the University of California, Riverside. He is President for IEEE Electron Devices Society (2014-2015) and an IEEE Fellow. His research interests center on RF and mixed-signal IC designs, integrated design-for-reliability, device and circuit integration, emerging devices and circuits, and IC CAD.*

Message from VP Regions and Chapters

"Joe" Xing Zhou
EDS Vice President-Regions/Chapters

This is the third year I have been serving as VP-Regions/Chapters (R/C), and I would like to take this opportunity to share with EDS members and volunteers some of my observations and thoughts related to EDS regions and chapters. A year ago, I wrote *Message from VP-Regions/Chapters* [Newsletter, p. 11, July 2014], in which I outlined some major activities and programs under R/C, such as chapter subsidy, chapter of the year (CoY) award, sub-committee for regions/chapters (SRC), distinguished lecturer (DL) and mini-colloquia (MQ) programs, and some ideas for improvements. Many of the topics we discussed over the years in R/C committee meetings "were centered on how to serve members and reward volunteers at the society/region/chapter levels" [Newsletter, p. 11, Oct. 2013], and many of the ideas I proposed were detailed at the December 2012 AdCom meeting in my role as SRC-R10 chair, when I was appointed as the incoming VP-R/C.

Members and chapters are the grass-roots of a society, without them there will be no society and no meaning for such a volunteer-driven organization. Among the society (or IEEE) members, they can be largely categorized into two groups: active members (or "volunteers") and inactive members (who just pay dues without participating in any society activities). Among the volunteers, they can be active members at two different levels: chapter and society (the SRC within EDS is an "intermediate" regional level that is actually belonging to society level). Among the chapters, there is a large variety of different needs and practices: some are financially strong with large member base and well-established renewal process, and others are in short of funds or relying on institutional resources and struggle to maintain membership. The linkage between chapters and the society has been various programs under R/C, such as the biennial regional chapter meetings as well as the subsidy, CoY, DL/MQ programs. These programs have been designed to better "serve members and reward volunteers" with different levels of success over the years, and it has been a major challenge on how to improve these programs to serve the variety of different needs of chapters and members. With the limited total funds, ideally it would be better to have non-uniform fund allocation and targeted fund utilization for the diversity in different needs. However, it has always been a difficult task for making changes over established practices.

The DL and MQ programs have been very popular and successful among our chapters. Unlike some other societies, our DLs are not designed for the "prestige" but for serving our chapters. The limited funds are meant for assisting DLs and chapters in organizing technical events for members. We have been encouraging coordinated MQ organization and leveraging various resources. One good example was the joint MQs (WIMNACT-42, 43, 44) in November 2014, coordinated by Prof, Steve Chung as SRC-R10 chair, in which a group of DLs visited the Shanghai, Nanjing, and Hangzhou chapters in a combined trip with funds from the MQ and SRC budgets as well as chapters' support. However, we do still have a situation in which DL participation and chapters hosting MQs are very non-uniform. We need to assist those less-active DLs to participate and especially to serve those less-active chapters. SRC chairs/vice-chairs and R/C committee members can also serve the roles in linking DLs to chapters. Besides "top-down" assistance from EDS and SRC, "bottom-up" pro-active initiatives from all DLs as well as local chapters are also the key to engaging more DLs and chapters in these programs. I'd like to call for all DLs to check the EDS chapters' map (http://eds.ieee.org/global-chapters-map.html), and contact EDS/SRC for assistance if needed, to link with local chapters for a DL talk when traveling to various places. For MQ initiators, we also encourage coordination for joint events with nearby chapters and in conjunction with regional conferences. It is important to note that we would like to leverage various resources and DLs being on a side-trip, rather than supporting DLs to attend paid conferences from DL/MQ budgets. Together, let us work towards better service for our members and reward our volunteers.

"Joe" Xing Zhou
EDS Vice President-Regions/Chapters
Nanyang Technological University
Singapore

***"Joe" Xing Zhou**, Vice President of Regions/Chapters of IEEE EDS, is a professor at Nanyang Technological University, Singapore. His group has been developing a core compact model for silicon bulk-CMOS, SOI, FinFET and nanowire, as well as III-V HEMT devices. He was a guest-EiC for the Feb'2014 special issue of IEEE Transactions on Electron Devices on compact modeling for emerging devices, and is currently an editor for IEEE Electron Device Letters.*

Message from Editor-in Chief

M K Radhakrishnan
Editor-in-Chief,
EDS Newsletter

Dear Readers,

Greetings from the EDS Newsletter team. We have initiated a new column "Reflections from Young Professionals" in the Newsletter starting from this issue. An interview with a vivid EDS YP is published in this column. This column is intended to reflect the person's perception about the profession, IEEE as well as EDS and how the association with EDS helps in nurturing the professional career. We are planning to have such interviews with EDS young professionals in different career paths and from all geographic regions in future.

In the Technical Briefs section the major article is on Reliability Trends in nanoscale CMOS Devices. This will be the first one of its kind on the device reliability trends. The technical summary and links of major conferences in devices area are also featured.

Summary of the deliberations at the EDS Board of Governors meeting held on 31 May 2015 at Singapore is included in this issue. Our idea is to communicate to all our members in a speedy manner. Newsletter is now available in mobile compatible Flipbook version also, apart from the print and pdf format. Also it is accessible to all through EDS website. However, we are not receiving sufficient feedback from our readers. We would like hear the readers' views, and I encourage everyone to write to me or to edsnewsletter@ieee.org

M K Radhakrishnan
Editor-in-Chief, EDS Newsletter
e-mail: radhakrishnan@ieee.org

EDS Governance Meeting Summary

Singapore Fling!

Fernando Guarin
EDS Secretary

May 30–June 1, 2015: The EDS Mid-year Governance Meeting returned to Region 10 this year in grand style, bringing together the Society's senior leadership with over 20 EDS Chapter Chairs from across Asia and the Pacific in beautiful Singapore. The meeting was a phenomenal success, combining vital society business with some truly special social events to create an enriching and energizing event for all attendees. The weekend began on Saturday morning, with a series of important Standing Committee meetings.

Fellows Evaluations

Despite long travel, and heavy jet-lag, the Fellows Evaluation Committee began their work bright and early Saturday morning, with the difficult task of reviewing and evaluating 47 IEEE Fellow nominations. Led by Guido Groeseneken, the committee deliberated for over 9 hours, proving once again that the work of this committee is among the most challenging and important to the Society and the IEEE.

Publications and Newsletter Joint Meeting

Fernando Guarin and MK Radhakrishnan presented the status and recent improvements to the newsletter. The increased emphasis on technical content as well as the transition to web format received positive reviews.

ED Malaysia Chapter was selected as the 2014 recipient of the IEEE Electron Devices Society Region 10 Chapter of the Year Award. 'Joe' Xing Zhou, EDS VP Regions/Chapters (right), presenting award to Dr. Burhanuddin Yeop Majlis (Chapter Advisor) and Assoc. Dr. Badariah Bais (Chapter Chair)

> *"My goal is to keep EDS a happy volunteer family with transparency and efficiency."*
>
> *Albert Wang*
> *EDS President*

Bin Zhao, EDS VP of Publications and Products, chaired the critical Publications committee meeting. In addition to reviewing the status of the ongoing in-depth and detailed searches for the T-ED and EDL Editors-in-Chief, the committee launched plans to improve the health and vitality of some of the smaller, cosponsored publications.

Technical Committees and Meetings

Led by EDS's VP of Technical Committees and Meetings, Leda Lunardi, 2014 was a banner year for EDS's robust roster of technical meetings and conferences. To build on that success, the committee held a strategic planning

Attendees of the 2015 EDS Region 10 Chapters Meeting held at the Marina Mandarin Hotel, Singapore

Attendees of the EDS Board of Governors Dinner enjoyed the panoramic views of the Singapore skyline at the Pan Pacific Singapore Hotel (Marina Bay)

session to ensure not only the health of our conferences, but also define way to engage our 14 technical committees in all aspects of the society's affairs, such as publication, webinars, and defining new technical areas for the society to explore.

Education, Membership, and Chapters

Combining three committee discussions into a single afternoon meeting, Vice Presidents Mikael Östling (Membership) and Joe Zhou (Regions and Chapters) and EDS Secretary and Education Chair, Fernando Guarín, convened an outstanding forum to address these critical areas of the society's life. In addition to providing an important strategic planning session, the highlight of the meeting was the open dialogue and frank discussion with over 20 EDS chapter chairs from across Region 10. Chapters are the life-blood of the society and this meeting provided an excellent opportunity for staff and volunteer leadership to learn more about the chapters' perspectives, needs, and successes and to gain valuable insight into how EDS needs to continually evolve to meet the needs of its key constituents throughout the globe particularly through the webinar and EDS-ETC programs.

EDS Governance Meeting

The EDS Forum and Board of Governors met on Sunday, May 31st, for the Mid-Year Governance meeting. The meeting's discussions covered nearly every aspect of the society's operations, ending with an extended Open-Forum to provide a free exchange of ideas and debate over how we can continue to improve the Society to ensure its preeminence as the world's leading organization devoted to device engineering. Here are some of the highlights:

- Ravi Todi, EDS Treasurer, reporting remotely, reviewed the financial state of EDS and the news is good! We have well over a year's expenses in reserve. In addition he received approval for key 2016 budget inputs and additional spending in 2015 of roughly $100K.
- Past Vice President of the IEEE Technical Activities Board (TAB), Jacek Zurada, joined us to present information on the TAB's strategic direction and some new initiatives to support it.
- Paul Yu, EDS Junior Past President and Awards Chair, successfully presented a proposal from the Photovoltaics Specialists Conference (PVSC) to elevate the conference's William Cherry Award to be an official EDS Society-level award. Now that EDS has approved, the next step is to seek TAB's approval, which will happen at the TAB meeting series in November.

(continued on back cover)

Call For Nominations
EDS Board of Governors—BoG (formerly AdCom) Members-at-Large Election

Paul Yu
EDS Chair of Nominations & Elections

The IEEE Electron Devices Society invites nominations for election to its Board of Governors – BoG (formerly AdCom). The next election will be held after the BoG meeting on Sunday, December 6, 2015. This year, seven out of the twenty-two members will be elected for a 3-year term, with a maximum of two consecutive terms.

This year EDS will again be running the pilot program for one of the seven BoG Member-at-Large seats to be elected via the entire EDS membership. All nominees must choose to participate in either the election by EDS membership or the election by the BoG. There must be a minimum of two nominees for the seat elected by membership. If there are less than two nominees for the seat, an election by EDS membership will not be held and the candidate will be moved to the election by the BoG. All electees begin their term in office on January 1, 2016. The nominees need not be present to run for the election. Self-nominations are allowed.

Any EDS member who has served for a minimum of one year as an EDS Officer, Vice-President, Standing & Technical Committee Chair/Member, Publication Editor, and Chapter Chair is eligible to be nominated. The electees are expected to attend both BoG Meetings every year. While the December meeting is organized in connection with the IEEE International Electron Devices Meeting, the mid-year meeting is frequently held outside the US. Partial travel support is available to attend both of these meetings.

All nominees must be endorsed by one BoG member, i.e., one of the four officers (President, President-Elect, Treasurer or Secretary), the Jr. or Sr. Past President or one of the 22 current BoG Members-at-Large. It is the responsibility of the endorser to make sure that, if elected, the nominee is willing to actively serve in the position as a BoG member. In the unlikely event that a nominee must withdraw their name from the election ballot, they must do so by November 1, 2015.

Please submit your EDS BoG nomination by August 1, 2015, using the online nomination form (http://eds.ieee.org/bog-call-for-nominations.html).

Also, all endorsement letters should be sent to Laura J. Riello, EDS Executive Office, via e-mail: l.riello@ieee.org by August 1, 2015. If you have any questions, please feel free to contact Laura Riello (l.riello@ieee.org) with a copy to me at p.yu@ieee.org.

Paul Yu
EDS Chair of Nominations & Elections
University of California at San Diego
San Diego, CA, USA

EDS Board of Governors Members-at-Large Election Process

Paul Yu
EDS Nominations and Elections Chair

The Members-at-Large (MAL) of the EDS Board of Governors are elected for staggered 3-year terms, with a maximum of two consecutive terms. The 1993 Constitution and Bylaws changes mandated increasing the number of elected MAL from 18 to 22, and required that there be at least two members from each of the following geographic areas: Regions 1–7 and 9; Region 8; Region 10. In 2003, EDS made changes to its Constitution and Bylaws to require that at least one elected BoG member is a Young Professional (YP – formerly Gold member). A Young Professional member is defined by IEEE as a member who graduated with his/her first professional degree within the last fifteen years. It is also required that there are at least 1.5 candidates for each opening.

This year EDS will again be running the pilot program for one of the BoG Member-at-Large seats to be elected via the entire EDS membership. All nominees must choose to participate in either the election by EDS membership or the election by the BoG. There must be a minimum of two nominees for the seat elected by membership. If there are less than two nominees for the seat, an election by EDS membership will not be held and the candidate will be moved to the election by the BoG. All electees begin their term in office on January 1, 2016. The nominees need not be present to run for the election. In 2015, seven positions will be filled.

The election procedure begins with the announcement and Call for Nominations in the *EDS Newsletter*. The slate of nominees is developed by the EDS Nominations Committee and includes the non-Committee and self-nominations received. Nominees are asked to submit a two-page biographical resume and an optional 50 word personal statement in a standard format. The election for the one BoG seat voted on by the EDS membership will be done using Vote Net. Vote Net is a web based tool that allows members the opportunity to cast their ballots electronically. An e-announcement will be sent to those EDS members who have email addresses in the IEEE database prior to the election launch date. It will give the members an opportunity to indicate their preference to receive an electronic or paper ballot. By default, paper ballots are automatically printed and mailed to EDS members without email on file as well as to those that have indicated they prefer not to receive election material electronically (based upon the communication preference in their member profile).

Any EDS member who has served for a minimum of one year as an EDS Officer, Vice-President, Standing & Technical Committee Chair/Member, Publication Editor & Chapter Chair is eligible to be nominated, unless otherwise precluded from doing so in the EDS Bylaws. All nominees must be endorsed by one BoG member, i.e., one of the four officers (President, President-Elect, Treasurer or Secretary), the Jr. or Sr. Past President or one of the 22 current BoG Members-at-Large. Self-nomination is allowed. Endorsers should send a brief email to Laura Riello stating that they would like to endorse the candidate. Please note that there is no limit to the number of candidates that a full voting BoG member can endorse.

Nominations are closed after August 1, 2015, and the biographical resumes and endorsement letters are distributed to the BoG prior to the December BoG meeting. The election is then held after the conclusion of the meeting.

Paul Yu
EDS Chair of Nominations & Elections
University of California at San Diego
San Diego, CA, USA

IEEE Annual Election—Did You Vote Yet?

This is a reminder for EDS members to vote in the 2015 IEEE Annual Election for the following positions and candidates.

Listed below are the positions and candidates that will appear on the 2015 IEEE Annual Election ballot.

Position	Candidate
IEEE President-Elect, 2016	• Karen Bartleson (Nominated by IEEE Board of Directors) • Frederick (Fred) C. Mintzer (Nominated by IEEE Board of Directors)
IEEE Region 1 (Northeastern USA) Delegate-Elect/Director-Elect, 2016–2017	• Babak Dastgheib-Beheshti (Nominated by IEEE Region 1) • Gim Soon Wan (Nominated by IEEE Region 1)
IEEE Region 3 (Southern USA) Delegate-Elect/Director-Elect, 2016–2017	• John E. Montague (Nominated by IEEE Region 3) • Gregg L. Vaughn (Nominated by IEEE Region 3)
IEEE Region 5 (Southwestern USA) Delegate-Elect/Director-Elect, 2016–2017	• T. Scott Atkinson (Nominated by IEEE Region 5) • Robert C. Shapiro (Nominated by IEEE Region 5)
IEEE Region 7 (Canada) Delegate-Elect/Director-Elect, 2016–2017	• Xavier N. Fernando (Nominated by IEEE Region 7) • Maike Luiken (Nominated by IEEE Region 7)
IEEE Region 9 (Latin America) Delegate-Elect/Director-Elect, 2016–2017	• Jose-Ignacio Castillo-Velazquez (Nominated by IEEE Region 9) • Teofilo J. Ramos (Nominated by Petition) • Enrique A. Tejera M. (Nominated by IEEE Region 9)
IEEE Standards Association President-Elect, 2016	• Robert S. Fish (Nominated by IEEE Standards Association) • Forrest D. (Don) Wright (Nominated by IEEE Standards Assoc.)
IEEE Standards Association Board of Governors Member-at-Large, 2016–2017	• W. C. (Chuck) Adams (Nominated by IEEE Standards Association) • Philip B. Winston (Nominated by IEEE Standards Association)
IEEE Standards Association Board of Governors Member-at-Large, 2016–2017	• Stanley J. Krolikoski (Nominated by IEEE Standards Association) • Paul Nikolich (Nominated by IEEE Standards Association)
IEEE Technical Activities Vice President-Elect, 2016	• Marina Ruggieri (Nominated by IEEE Technical Activities) • Douglas N. Zuckerman (Nominated by IEEE Technical Activities)
IEEE-USA President-Elect, 2016	• Keith D. Grzelak (Nominated by IEEE-USA) • Karen S. Pedersen (Nominated by IEEE-USA)
IEEE-USA Member-at-Large, 2016–2017	• Wole Akpose (Nominated by IEEE-USA) • Daniel N. Donahoe (Nominated by IEEE-USA)
Constitutional Amendment	http://www.ieee.org/about/corporate/election/2015_constitutional_amendment.html

Balloting period starts on 17 August and ends at 12:00 noon, Central Time USA (17:00 UTC) on 1 October 2015. All eligible voting members should look for their ballot to arrive via postal mail or access their electronically at www.ieee.org/elections. Forward election questions to election@ieee.org

EDS Compound Semiconductor Devices and Circuits Technical Committee Report

Research on compound semiconductor (CS) electronics is showing continuous advances in traditional areas and new fields. Microwave and mm-wave applications are benefiting from further developments in well-established technologies (e.g. III-V HEMTs and HBTs), while research in III-V MOSFETs and FINFETs as a possible alternative to Si-based digital devices has reached interesting milestones. Progress in widegap (SiC and GaN) electronics continues and a steady improvement is seen in the related reliability issues. Further major advancements are found for the application of III-N concepts to power electronics for fast switching in energy conversion. At the same time, the quest for graphene-like 2D semiconductors has also found an interesting CS line in the 2D transition metal chalcogenides.

The main driver of the development of III-V MOSFETs lies in the superior electron transport properties of III-V materials with respect to Si, enabling an attractive route to downscaling at sub 10 nm nodes. Different architectures have been considered for aggressively scaled III-V devices; examples are the FINFET, the Nanowire FET (also called Gate All Around, GAA FET), the Extremely Thin Body Quantum Well (ETB-QW) FET. ETB-QW FETs exploit a metal gate, high-κ insulator, and an InGaAs/InAs/InGaAs composite channel. ETB-QW InAs MOSFETs with improved electrostatics, 50 nm gate length and subthreshold swing (SS) in excess of 100 mV/dec, DIBL of 73 mV/V, off-state current of 0.5 nA/μm and maximum g_m > 1.5 mS/μm at V_{DS} = 0.5 V were presented in 2012 at IEDM by researchers from SEMATECH, Globalfoundries, MIT, UT-Austin, CNSE, TEL and HKUST, see the IEDM 2012 Proc., p. 32.3.1. Researchers from Purdue and Harvard Universities presented (see IEDM 2012 Proc., p. 27.6.1) 20 nm–80 nm channel length strained InGaAs GAA nanowire FETs with record high on-state and off-state performance by equivalent oxide thickness (EOT; the insulator exploits Al_2O_3 and $LaAlO_3$ layers) and nanowire width scaling down to 1.2 nm and 20 nm, respectively; performances included a SS = 63 mV/dec, DIBL as low as 7 mV/V, I_{ON} = 0.63 mA/μm and g_m = 1.74 mS/μm at V_{DS} = 0.5 V, demonstrating the promise of InGaAs GAA FETs for 10 nm and beyond high-speed low-power digital applications. The same research groups (see the IEDM 2012 Proc., p. 23.7.1) proposed a vertically stacked nanowire array GAA InGaAs FET (imaginatively called 4D GAA FETs) achieving a 4x increase of the driving current and gm versus the 3D (non-stacked array) version. The device exhibits a record high I_{ON} = 9 mA/μm and g_m = 6.2 mS/μm. The III-V 4D transistor structure appears promising also in the RF and microwave analog field.

During the last few years, the development of widegap semiconductor devices, in particular GaN-based, has undergone a steady progress. For an overview of recent advances the reader can refer to the October 2013 (vol. 60, no. 10) Special Issue of the IEEE ED Trans. on GaN electronics. As mentioned, developments have concerned not only the traditional RF and microwave power, but also power switching applications with lower-cost GaN on Si devices.

The progress of RF, microwave and millimeter wave GaN HEMTs has led to cutoff frequencies exceeding 450 GHz and oscillation frequencies close to 600 GHz in devices with optimized asymmetric layout and nanometer-scale gate lengths, see the paper from HRL Laboratories (IEEE ED Trans., vol.60, no.10, p. 2982). TrQuint reports both E-mode and D-mode InAlN/AlN/GaN HEMTs with gate lengths in the 30 to 50 nm range with frequency performance well in excess of 200 GHz and a noise figure of 0.25 dB at 10 GHz, see IEEE ED Trans., vol. 60, no. 10, p. 3099. Also in high-frequency applications, properly optimized AlGaN/GaN HEMTs grown on Si substrates have shown a power density of 1.5 W/mm at 40 GHz, see IEEE ED Trans., vol. 60, no. 10, p. 3105.

Concerning power switching applications, wide-bandgap semiconductors such as SiC and GaN are witnessing rapid increase in R&D as well as capital investment for next-generation power conversion & management systems with higher efficiency. With SiC MOSFETs being exploited in vertical structures for its high current density, the development of GaN-based power transistors focuses on the lateral heterojunctions (e.g. AlGaN/GaN) for the material maturity. Major efforts being made to tackle key technology challenges include: (i) finding the suitable gate dielectrics with a low interface trap density for improved threshold voltage stability; (ii) optimizing buffer structures for high breakdown and low dynamic ON-resistance on large-area silicon substrates; and (iii) optimizing passivation techniques and field-plate structures for improved device reliability/stability. We are also witnessing a significant increase in product announcements of GaN power devices covering a wide range of voltage rating (30 V ~ 600 V) during the last year.

Significant advances have also been made in the development of GaN-based MOSFETs. With respect to SiC, the GaN MOSFET has higher mobility for higher speed application and lower power consumption during turn-on. Compared with AlGaN/GaN HEMTs, the GaN MOSFET has the advantages of positive threshold

voltage, lower leakage current and superior reliability for power electronics. To lower the cost, the GaN should be grown on Si substrate that has a large wafer size up to 12 inch. Nevertheless, the high tensile strain of GaN can create crack in the Si substrate. One solution is to add the compressive strained AlSiC layer before the epitaxial AlN buffer layer and the GaN/AlGaN layer (IEEE EDL 34, p. 975, Aug. 2013). Besides, good device performance of normally-off, gate-recessed GaN MOSFET was reached with a 600 V breakdown voltage, in addition to the crack-free surface. This technology may lead to grow GaN/AlGaN on large size Si wafers.

Recently, the new area of graphene-like 2D compound semiconductors opened up with the family of transition metal dichalcogenides. Similar to graphite, these can be exfoliated into single mono- or multilayers and deposed onto Si substrates. Molybdenum disulfide (MoS_2) probably is the most important material nowadays; although its mobility is of the order of 100 $cm^2/V.s$ only, MoS_2 mono- and multilayers, contrarily to graphene, have a bandgap, direct (2 eV) and indirect (1.8 eV), respectively. This allows the fabrication of thin-film transistors with excellent switch-off with E-mode D-mode operation, but also of sensors and photodetectors, as potential substitutes of Si in conventional electronics and of organic and amorphous Si in systems and display applications. The first MoS_2 TFT was presented by Kis et al. of EPFL in 2011 (see Nature Nanotech., vol. 6, no. 3, pp. 147–150, 2011) but many research groups are engaged in the development of this technology, see e.g. the multilayer MoS_2 transistor presented at IEDM in 2012 (pp. 5.5.1-5.5.4) and the bilayer MoS_2 integrated circuits (implementing logical functions and ring oscillators) in Nano Letters, 2012, 12 (9), pp. 4674–4680.

The 2013 EDS CSDC Committee member list can be found at: http://eds.ieee.org/technical-committees/eds-compound-semiconductor-devices-and-circuits-technical-committee.html. Some of the CSDC committee members have been guest editors of the October 2013 ED Trans. SI on GaN electron devices and in the chapter *RF and microwave semiconductor technologies* of the EDS anniversary book *Guide to state-of-the-art electron devices*, J. Burghartz, ed., Wiley-IEEE, 2013. Among future activities the EDS CSDC Committee would continue proposing special issues in the EDS periodicals focused on recent developments in the area.

Giovanni Ghione
EDS CSDC Technical Committee Chair
Politecnico di Torino, Italy

Kevin Chen
Hong Kong University of Science & Technology

Albert Chin
National Chiao Tung University
Taiwan

Ruediger Quay
Fraunhofer Institute
Freiburg, Germany

2015 William R. Cherry Award Winner—Dr. Christiana Honsberg

The Photovoltaic Specialist Conference Cherry Committee is proud to announce Prof. Christiana B. Honsberg as the winner of the 2015 William R. Cherry Award. This award is named in honor of William R. Cherry, a founder of the photovoltaic community. In the 1950's, he was instrumental in establishing solar cells as the ideal power source for space satellites and for recognizing, advocating, and nurturing the use of photovoltaic systems for terrestrial applications. The William R. Cherry award was instituted in 1980, shortly after his death. The purpose of the award is to recognize an individual engineer or scientist who devoted a part of their professional life to the advancement of the science and technology of photovoltaic energy conversion. The award winner must have made significant contributions to the science and/or technology of PV energy conversion, with dissemination by substantial publications and presentations.

Christiana B. Honsberg is a Professor at the School of Electrical, Computer and Energy Engineering and Senior Sustainability Scientist at the Julie Ann Wrigley Global Institute of Sustainability at Arizona State University in Tempe, Arizona. She is the Director of QESST: the NSF Engineering Research Center for Quantum Energy and Sustainable Solar Technologies and Director of the Solar Power Laboratories at Arizona State University. Dr. Honsberg received her PhD in Electrical Engineering from the University of Delaware in 1992, following a B.S. and M.S. in 1986 and 1989, respectively, both from the University of Delaware, as well. She has been a pioneer in the advanced concept photovoltaic area including: developing generalized thermodynamic theory for efficiency limits in solar cells allowing identification of common underpinning physical mechanisms in advanced concept approaches; proposal of combined

Auger/multiple quasi-Fermi level approaches; identification of quasi-Fermi levels as central requirement in interband and quantum well approaches; formulation and analyses of fundamental loss mechanisms in intermediate band approaches; and development of methods to identify existence of multiple quasi- Fermi levels in experimental devices.

Prof. Honsberg's leadership of QESST has brought together the photovoltaic research community representing multiple universities and world-renowned energy companies in a strategic partnership to generate innovative solutions to sustainable electricity generation. This Engineering Research Center is funded jointly ($29 million over 10 years) by the U.S. National Science Foundation and the U.S. Department of Energy to solve challenges to harnessing solar power in economically viable and sustainable ways.

Prof. Honsberg also was the Principal Investigator for the "Very High Efficiency Solar Cells" program, reaching a sum-of-the-efficiencies of 42.8%, and she led the first experimental demonstration of GaN and InGaN high-voltage solar cells. Her research has also identified and implemented the GaAsSb/InAsP barrier/quantum dot system for exploration of intermediate band solar cells and developed new commercial high-efficiency silicon solar cells, including invention and licensing of high-performance solar cell technology, technology transfer of buried contact technology and development of a new passivation technique which was used in the demonstration of the highest open-circuit voltage on a silicon solar cell at that time.

2015 PVSC Cherry Award Committee

42nd Photovoltaic Specialists Conference (PVSC) Young Professional Award Winner

Henry Snaith – Recipient of the 2015 PVSC Young Professional Award

The IEEE Photovoltaics Specialists Conference (PVSC) continued this year in recognizing an outstanding young professional in the photovoltaics (PV) community. The PVSC Young Professional Award recognizes individuals who have made significant contributions to the science and technology of PV energy conversion, including work on PV materials, devices, modules, and/or systems. The award recipient must also show significant promise as a leader in the field.

On behalf of the organizing and program committees of the 42nd IEEE PVSC, I am delighted to announce the recipient of this year's award—**Professor Henry Snaith** (University of Oxford). He is recognized for pioneering breakthroughs with hybrid perovskite-based materials that have spawned a revolution in thinking about thin film PV technologies.

Henry Snaith undertook his PhD at the University of Cambridge, working on organic photovoltaics under Prof. Sir. Richard Friend. Then, he spent two years at the EPFL, in Switzerland, as a post doc working on dye-sensitized solar cells under Prof Michael Grätzel. He returned to the Cambridge to take up a Fellowship for Clare College in 2006, and moved to the Clarendon Laboratory of Oxford Physics in 2007, where he now holds a professorship and directs a group researching in optoelectronics, specifically organic, hybrid and perovskite devices. His research is focused on developing new materials and structures for hybrid solar cells and understanding and controlling the physical processes occurring at interfaces. He has made a number of significant advances for emerging PV, including the first demonstration of "gyroid" structured titania for dye solar cells, the first demonstration of a mesoporous single crystal of TiO2, and the recent discovery of high efficiency organic-inorganic metal halide perovskite based solar cells. His recent work with perovskite solar cells has transformed the PV research community, and scientists from every sector are turning their hands to explore the intriguing properties of perovskites. He has risen over £9M in research funding from the UK research councils, European Commission and Industry over the last 8 years, which supports his research team. In December 2010 he founded Oxford Photovoltaics Ltd., which is rapidly commercializing the perovskite solar technology transferred from his University Laboratory.

Congratulations, Professor Snaith!

Kyle Montgomery
2015 PVSC Awards Chair
University of California, Davis

Congratulations to the 23 EDS Members Recently Elected to IEEE Senior Member Grade!

Hideaki Aochi
Laurent Blanquart
Jose Casallas
Salih Celik
Ho-Young Cha
Alan Delahoy
Yi Gu
James Henry
Tetsuya Hirose
M Saiful Islam
Hang-Ting Lue
Dheena Moongilan
Giacinta Parish
Tirthajyoti Sarkar
Shinji Sato
Suhaidi Shafie
Aaron Thean
Han Wui Then
Dimitris Tsoukalas
Jan Voves
Yih Wang
Alma Wickenden
Jiangeng Xue

If you have been in professional practice for 10 years, you may be eligible for Senior Membership, the highest grade of membership for which an individual can apply. New senior members receive a wood and bronze plaque and a credit certificate for up to US$25 for a new IEEE society membership. Upon request a letter will be sent to employers, recognizing this new status.

For more information on senior member status, visit: http://www.ieee.org/membership_services/membership/senior/index.html

To apply for senior member status, fill out the on-line application: https://www.ieee.org/membership_services/membership/senior/application/index.html.

You will need to Sign-in with your IEEE account.

Please remember to designate the Electron Devices Society as your nominating entity!

Enhance Your Career with IEEE Senior Membership

Mikael Östling
EDS Vice-President of Membership & Services

The Electron Devices Society established the EDS Senior Member Program to both complement and enhance the IEEE's Nominate-a-Senior-Member Initiative and make IEEE/EDS members aware of the opportunity and encourage them to elevate their IEEE membership grade to Senior Member. This is the highest IEEE grade for which an individual can apply and is the first step to becoming a Fellow of IEEE. If you have been in professional practice of 10 years, you may be eligible for Senior Membership.

Benefits of Senior Membership[1]

- **Recognition:** The professional recognition of your peers for technical and professional excellence.
- **Senior member plaque:** Since January 1999, all newly elevated Senior members have received an engraved Senior Member plaque to be proudly displayed for colleagues, clients and employers to see. The plaque, an attractive fine wood with bronze engraving, is sent within six to eight weeks after elevation.
- **US$25 coupon:** IEEE will recognize all newly elevated Senior members with a coupon worth up to US$25. This coupon can be used to join one new IEEE society. The coupon expires on 31 December of the year in which it is received.
- **Letter of commendation:** A letter of commendation will be sent to your employer on the achievement of Senior member grade (upon the request of the newly elected Senior member).
- **Announcements:** Announcement of elevation can be made in section/society and/or local newsletters, newspapers and notices.
- **Leadership Eligibility:** Senior members are eligible to hold executive IEEE volunteer positions.
- **Ability to refer other candidates:** Senior members can serve as a reference for other applicants for senior membership.
- **Review panel:** Senior members are invited to be on the panel to review senior member applications.
- **US$25 referral coupon:** Newly elevated Senior members are encouraged to find the next innovators of tomorrow and invite them to join IEEE. Invite them to join and the new IEEE member will receive $25 off their first year of membership.

As part of the IEEE's Nominate-a-Senior-Member Initiative, the nominating entity designated on the member's application form will receive US$10 from IEEE for each application approved for Senior Member grade when there are at least five approved applications. As an EDS member, we would appreciate it if you could indicate on your Senior Member application form that **EDS** is your nominating entity.

Please be aware that even if you decide to list EDS as your nominating entity, you still need to have an IEEE

member nominate you along with two other references. Your nominator and your references all must be active IEEE members holding Senior Member, Fellow or Honorary Member grade.

For more information on the criteria for elevation to Senior Member, please visit the Senior Membership Portal: http://www.ieee.org/membership_services/membership/senior/index.html .

We strongly encourage you to apply for IEEE Senior Membership to enhance your career. At the same time, you'll be helping EDS. Thank you for supporting IEEE and EDS.

[1]IEEE.org, http://www.ieee.org/membership_services/membership/senior/index.html

Mikael Östling
EDS Vice-President of Membership & Services
KTH, Royal Institute of Technology
Sweden

EDS Distinguished Lecturer and Mini-Colloquia Programs

The EDS Distinguished Lecturer (DL) Program exists for the purpose of providing EDS Chapters with a list of quality lecturers who can potentially give talks at local chapter meetings.

To arrange for a lecture, EDS chapters should visit the EDS website to view the listing of EDS DLs and contact the EDS DL directly. A general guideline for the visit, but not the absolute rule, is that the lecturer should be able to include the meeting site with an already planned travel schedule at a small incremental cost to the travel plan. Although the concept of the program is to have the lecturers minimize travel costs by combining their visits with planned business trips, EDS will help subsidize lecturer travel in cases where few/no lecturers will be visiting an area and/or a chapter cannot pay for all the expenses for a lecturer trip.

To request DL travel funding, the EDS DL would need to submit an EDS DL Activity Log & Funding Request Form (http://eds.ieee.org/lectures/procedures-for-requesting-eds-distinguished-lecturers-and-funding.html).

EDS is also encouraging chapters to hold mini-colloquia (MQ) in remote areas. This concept generally involves the sending of about 3 or more DLs to travel to a region/chapter and present the latest developments in a particular field. The chapters/regions would be responsible for handling all the arrangements of the event and only minimal financial support would be required of EDS and could be covered by the MQ Program budget upon request. Please visit the EDS website for more information (http://eds.ieee.org/lectures.html).

We ask all chapters that are holding EDS Mini-Colloquia to utilize the free EDS registration tool that we have developed to keep track of attendance at our MQ and DL events. EDS will provide possible membership discounts to non-IEEE/EDS members when they register for your MQ, so please include your personalized registration link in your MQ announcements.

For more information on the DL or MQ Programs, please visit the EDS website or contact Laura Riello of the EDS Executive Office.

EDS Chapter Subsidies for 2016

The deadline for EDS chapters to request a subsidy for 2016 is September 1, 2015. For 2015, the EDS BoG awarded funding to 67 chapters, with most amounts primarily ranging from US$250 to US$750. In June, Chapter Chairs were sent an e-mail notifying them of the current funding cycle and providing them with a list of guidelines. In general, activities which are considered fundable include, but are not limited to, membership promotion, travel allowances for invited speakers to chapter events, and support for student activities at local institutions.

Chapter Subsidy requests can be requested by completing the chapter activity report, which can be found at http://eds.ieee.org/chapter-subsidy-program.html. **Please note that the report needs to be submitted by September 1, 2015**.

Final decisions concerning subsidies will be made in December. Subsidy checks will be issued by early January of the following year. Please visit the EDS website (www.ieee.org/eds) for more information.

The EDS-ETC Program a Big Hit with our IEEE Families at Take Your Daughters and Sons to Work Day

The Electron Devices Society was a major contributor to this year's Take Your Daughters and Sons to Work Day at the IEEE Operations Center. On April 23rd, more than 100 visitors between the ages of 8 and 14 came to the IEEE Operations Center for a full schedule of educational and fun activities that helped to demonstrate the connection between their family's contributions on an every-day basis to the world-wide initiatives supported by the IEEE.

We were very fortunate to have two invaluable and dedicated EDS volunteers, Fernando Guarin (EDS Secretary and Chair of EDS Educational Activities Committee) and Nagi Naganathan (Secretary IEEE Princeton Section), to lead the children through various Snap Circuits® activities, which included electric light switch, DC motor, and light-emitting diode experiments. With the assistance of EDS staff Joyce Lombardini , Kellie Gilbert and Chris Jannuzzi, our volunteers organized and presented the first-ever and highly successful EDS-ETC workshop at IEEE.

A special surprise was Fernando's demonstration of the Raspberry pi, a single-board computer that stimulates the teaching of basic computer science. Adding a miniature monitor and keyboard, he demonstrated some of the Raspberry pi's many uses, like a looping animation program written with Scratch (one of the entry-level programming languages standard with the unit), an LED light show, and how to add photo/video capability with a simple camera attachment. With that last camera demo, the Raspberry 'selfie' was launched, with children clamoring to be the next in line.

One of the popular demos, the raspberry 'selfie'

The positive feedback received from parents and children proves once again the value of this program. We want all our volunteers to know how much their work is appreciated and we encourage each and every EDS-ETC program organizer to submit reports and articles to this newsletter to promote their good works and successes.

"What a great day!" said EDS Executive Director Chris Jannuzzi. *"As an EDS member and staffer, it was wonderful to see the EDS-ETC program in action at IEEE. And just as gratifying was being the parent of two of the children fortunate enough to attend this outstanding event. We're very grateful to Fernando and Nagi for their time and service to EDS and the IEEE."*

The following photos are just some of the dozens taken at the event:

Teamwork, building a sound-activated light

Pictured with EDS's Kellie Gilbert (right), IEEE Society volunteers Fernando Guarin (left) and Nagi Naganathan

Fernando (from left), secretary of the IEEE Electron Devices Society, shares a trick with Michael and Raymond Jannuzzi , and Anthony Riello

2015 EDS Award Winners and 2016 Call For Nominations

Call for Nominations
2015 EDS Chapter of the Year Award

The EDS Chapter of the Year Award is given each year based on the quantity and quality of the activities and programs implemented by the chapters during the prior July 1st–June 30th period.

At the June 2012 EDS BoG (AdCom) Meeting, the BoG (AdCom) approved to increase the number of awards we give out in a given year, starting with the 2013 Award. We will award one Chapter from each of the following Regions:

- Regions 1-7
- Region 8
- Region 9
- Region 10

Nominations for the awards can only be made by SRC Chairs/Vice-Chairs, or self-nominated by Chapter Chairs. Please visit the EDS website to submit your nomination form (http://eds.ieee.org/chapter-of-the-year-award.html).

Each winning chapter will receive a plaque and check for $500 to be presented at an EDS Conference or Chapter Meeting of their choice. Travel reimbursement will not be provided.

The schedule for the award process is as follows:

Action	Date
Call for Nominations E-Mailed to Chapter Chairs, SRC Chairs & SRC Vice-Chairs	June 1st
Deadline for Nominations	September 15th
Regions/Chapters Committee Selects Winners	Early-October
Award given to Chapter Representative at requested conference	Open

Call for Nominations
2014–2015 IEEE Electron Devices Society
Region 9 Biennial Outstanding Student Paper Award

Description: Awarded to promote, recognize, and support meritorious research achievement on the part of Region 9 (Latin America and the Caribbean) students, and their advisors, through the public recognition of their published work, within the Electron Devices Society's field of interest: All aspects of the physics, engineering, theory and phenomena of electron and ion devices such as elemental and compound semiconductor devices, organic and other emerging materials based devices, quantum effect devices, optical devices, displays and imaging devices, photovoltaics, solid-state sensors and actuators, solid-state power devices, high frequency devices, micromechanics, tubes and other vacuum devices. The society is concerned with research, development, design, and manufacture related to the materials, processing, technology, and applications of such devices, and the scientific, technical and other activities that contribute to the advancement of this field.

Prize: A distinction will be conferred in the form of an Award certificate bestowed upon the most outstanding Student Paper nominated for the two-year period. The prize will be presented at either the International Caribbean Conference on Devices, Circuits and Systems (ICCDCS) or the Symposium on Microelectronics Technology and Devices (SBMicro). In addition to the recognition certificate, the recipient will receive a subsidy of up to $1,500 to attend the conference, where the award is to be presented. There will be a formal announcement of the winner in a future issue of the EDS Newsletter. The winner will also receive up to three years of complimentary IEEE and EDS student membership, as long as winner remains eligible for student membership.

Eligibility: Nominee must be enrolled at a higher education institution located in Region 9. In the case of a co-authored paper, only eligible co-authors may be nominated. Papers should be written in English on an electron devices related topic. Papers should have been published, in full-feature form, during 2014-2015 in an internationally recognized IEEE sponsored journal or conference in the field of electron devices related topics. Statements by the student and by the faculty advisor should accompany the nomination. Nominator must be an IEEE EDS member. Previous winners of this award are ineligible. There must be a minimum of five nominations submitted in order for the award to be administered for that year.

Basis for Judging: Demonstration of Nominee's significant ability to perform outstanding research and report its results in the field of electron devices. Papers will be judged on: technical content merit, originality, structure, clarity of composition, writing skills, overall presentation. These criteria will be weighted by the assessment of the nominee's personal contribution and the linkage of the nominated work to the nominee's career plans.

Nomination Package:
- Nominating letter by an EDS member (it may be the faculty advisor)
- A brief one-page (maximum) biographical sketch of the student
- 1000 words (maximum) statement by the nominated student describing the significance and repercussion of the nominated work within the wider scope of the nominee's career plans
- 400 words (maximum) statement by the faculty advisor under whose guidance the nominated work was carried out. It should unmistakably state the faculty advisor's support of the nomination, and clearly explain the extent of the nominated student's contribution, as well as its relevance for the overall success of the reported work.
- A copy of the published paper

Timetable:
- Nomination packages are due at the EDS Executive Office no later than **15 February 2016.**
- Nomination packages can be submitted by mail, fax or e-mail, but a hard copy must be received at the EDS Office
- Winners will be notified by 15 March 2016.
- Recipients may choose to have the formal presentation of the award at either one of the conferences: ICCDCS 2016 or SBMicro 2016

Send completed package to:
IEEE Operations Center
EDS Executive Office
EDS R9 Outstanding Student Paper Award
445 Hoes Lane, Piscataway, NJ 08854 USA

For more information contact:
Laura Riello, EDS Executive Office
l.riello@ieee.org or 732-562-3927

Young Professionals

Reflections from EDS Young Professionals

We are initiating a new series in the EDS Newsletter called "Reflections from Young Professionals". The Newsletter Editor will be interviewing Young EDS Professionals to get their opinion and feedback on our society as well as how our professional body helps and supports them in developing their career.

The first part of this series is an interview with an outstanding Young EDS Professional, Dr. Nagarajan Raghavan, currently a post-doctoral fellow at MIT who will be joining Singapore University of Technology and Design (SUTD) soon as a faculty member. He was a recipient of the EDS PhD Student Fellowship in 2011.

M K Radhakrishnan, Editor-in Chief of EDS Newsletter has interviewed Nagarajan. Excerpts of the interview are given here in a question and answer format.

Editor: **As a young professional in the early age of your professional career, why do you consider the membership in IEEE and especially in EDS is important?**

Nagarajan Raghavan

Nagarajan: IEEE is a big organization with a reputed history and extensive membership networks all around the world. As a young professional, I was interested to get myself associated to this network as it gave me pride in being a part of a reputed organization. With the events and seminars organized by the EDS society in Singapore where I was pursuing my undergraduate studies and given its relevance to my interest in semiconductor physics, I very much wanted to be a part of the EDS community as well. EDS has played an active role in organizing seminars and invited talks by distinguished lecturers which provide a great opportunity for young people like me to learn, understand and interact with the big minds of the field. I drew a lot of inspiration from many of these seminars, which gave me the drive to pursue academic research as a career. I am now close to becoming a Senior Member of IEEE as this is my tenth year of membership and I very much look forward to working hard to receive the "Fellow" title in the future many years down the road. The EDS society has been very active in Singapore not just in organizing seminars, but also in promoting research, funding symposiums, recognizing young research talents through the Masters / PhD student fellowship awards and serving as a forum for active relevant job hunt in this area. What I like most about EDS is its sincere intention to reach out to many educational institutions even in the less known regions of large countries such as India and China. In short, I have cherished being an IEEE member and I look forward to playing a more active role and in contributing to the best of my abilities in serving the organization in the future.

Editor: **What was the specific temptation, if any, which made you to join this largest professional organization in the globe, at first?**

Nagarajan: I have heard a lot about the prestige and reputation associated with IEEE from my own father, who is in the technical line of electronics and communications. I remember his sharing of experiences on how being a part of IEEE is itself a recognition wherever you go. I could sense the vibrant nature of the IEEE society during my undergrad studies from the various events they organized throughout the year at Nanyang Technological University (NTU). There were several seminars not just on topical areas, but also on general interest themes such as resume writing, tips for succeeding in interviews, good approaches to write scientific journals etc… The happiest moment I had was when I was invited to be a reviewer for the first time by the IEEE Transactions on Device and Materials Reliability (TDMR) during my undergrad days. All these events got me really excited to be a full-fledged member of this organization.

Editor: **As a Professional, how do you position your interest in your own field with the activities and services you perform as an EDS member/volunteer?**

Nagarajan: My field of work can be summarized as "reliability modeling and physics of failure of semiconductor logic and memory devices". As a young professional, I have been an active reviewer for several IEEE journals such EDL, TED and TDMR over the past 5-6 years. I was also part of the technical program review committee for the IPFA, ESREF and IRPS symposiums. I have been invited to serve as the Technical Co-Chair for the IPFA 2016 symposium to be held in Singapore next July. My activities in IEEE and role as a reviewer and conference organizer are very much related to my field of work on reliability and failure analysis. I have gained a lot through these activities as it has given me a big network of collaborators both in the academia and the industry.

Editor: **What are your thoughts about the EDS membership and its paybacks? Whether the EDS membership benefited you at any time in your career growth?. If so, how?**

Nagarajan: The EDS membership has been very rewarding to me over the years. Other than the access to EDS based journals, the EDS newsletter itself is a rich resource to keep track of the various EDS seminars and events that are being held in the Asia-Pacific region (Region 10). The newsletter provides additional information on upcoming symposiums as well. I have attended several distinguished lecturer (DL) talks on a variety of topics and they have been very insightful and enriching as the topics dealt with are the latest relevant ones to the semiconductor industry. The EDS membership also helps me stay connected with other fellow community members in other parts of the globe and it has been an effective medium for me to find active collaborators to complement my statistical research work with the right experiments and atomistic simulations.

Editor: **As an YP, how do you consider the ED Society as a whole and what are the changes or developments you would like to see in evolving this professional body as a group devoted to the humanity and its causes?**

Nagarajan: I think the EDS society has been progressing very well over the last few years like never before and it is getting increasingly vibrant and spreading its wings to reach out to more young professionals and semiconductor enthusiasts in all geographical regions. The website of the EDS has also been very informative and resourceful. I would like to see the EDS society encourage the community and provide several avenues for young researchers to work on new topics that are very much needed for the future such as low cost technology for the under-developed or developing countries. Rather than purely focusing on theoretical advances and Moore's law based scaling progression, the EDS society should introduce more awards and call for proposals for young professionals who can make use of their device and process knowledge to come up with technology solutions for the underdeveloped world, aged people, physically challenged people etc. This could be in the form of new low cost sensors, actuators, that people can afford as well as design for low-cost solar panels that can be self-cleaning etc… Given that the interests of EDS span across materials, process, devices and circuits, people affiliated to this society are in the best position to leverage on each other's expertise to realize new technology innovations that are reliable, low cost and of good performance. Perhaps, the IEEE EDS society should launch its own research grant calls for different geographical regions for young researchers (post-docs and junior faculty) to pursue their dreams and prototype, validate and implement new ideas. Also, I would like to see the EDS society having greater interaction in the form of joint symposiums, interdisciplinary seminars and workshops with other relevant societies such as the Reliability Society, Circuits and Systems Society, Signal Processing Society as well as the Solid-State Circuits Society.

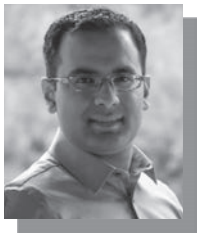
Editor: **What are your suggestions and recommendations for those young professionals who may aspire to join EDS?**

Nagarajan: The EDS society provides a good platform for young professionals to learn more, interact with the community, establish networks, be informed of the latest developments, realize their potential talents and implement their ideas. On the whole, it plays a key role in bringing together a large group of people with diverse backgrounds to work for the advancement of semiconductor devices. Given its vibrant nature and active involvement and support for technical activities, I see no reason why anyone should be reluctant to join the EDS. There is much more to EDS than the affordable membership fee and conference discounts as an IEEE member. If the EDS membership privileges are well utilized, it could play a big role in the advancement of one's career in the field of semiconductors and nanotechnology.

Nagarajan Raghavan *is currently pursuing his joint post-doctoral fellowship at the Singapore University of Technology and Design (SUTD) and Massachusetts Institute of Technology (MIT). He will soon be joining SUTD as an Assistant Professor in the Engineering Product Development (EPD) pillar starting AUG 2015. Prior to this, he was a post-doc at the Interuniversity Microelectronics Center (IMEC) in joint association with the Katholieke Universiteit Leuven (KUL), Belgium. He obtained his Ph.D. (Microelectronics, 2012) at the Division of Microelectronics, Nanyang Technological University (NTU), Singapore and S.M. (Advanced Materials for Micro & Nano Systems, 2008) and M.Eng (Materials Science and Engineering, 2008) from National University of Singapore (NUS) and Massachusetts Institute of Technology (MIT), Boston respectively. His work focuses on statistical characterization and reliability modeling of dielectric breakdown and resistance switching in novel high-κ dielectric material based logic and memory device stacks. His other research interests include random telegraph noise, prognostics for nanodevices, design for reliability and reliability statistics. He is the Asia-Pacific recipient for the IEEE EDS PhD Student Fellowship in 2011 and the IEEE Reliability Society Graduate Scholarship Award in 2008. To date, he has authored / co-authored close to 100 international peer-reviewed publications and four invited book chapters as well. He also holds a US patent as a co-inventor for using CMOS platform to fabricate RRAM devices. He has served on the review committee for various IEEE journals and conferences including IRPS, IIRW, IPFA, ISDRS and ESREF. He is currently a Member of IEEE (2005-present) and was an invited member of the IEEE GOLD committee (2012–2014).*

IEEE Young Professionals—An Exciting New Rebranded Outlook

By Ishan Sharma (sharmai@ieee.org)



What is IEEE Young Professionals? *IEEE Young Professionals Program* (YPP) is the rebranded successor of *IEEE GOLD* (Graduates Of the Last Decade). If you graduated with your first degree within the last 15 years, then you are automatically part of YPP with the option of participating beyond this timeframe. With these changes and a 77,000-strong membership, there is renewed energy in the young professionals' community to continue to transform IEEE into an intellectual and social hub that fosters collaboration and networking at a global scale to achieve IEEE's mission.

I got my first glimpse into these exciting initiatives at the IEEE YPP Committee Meeting in Panama in early May 2015. During this meeting, the focus was on globally organized efforts for a local impact. In 2015, the YPP committee is focusing on four work-streams: (1) Collabratec™, (2) Global Entrepreneurship Program (GEP), (3) Leadership and Volunteer Portal, and (4) Industrial Relations and Sponsorships. Each attendee of this meeting was assigned to one of these work-streams. Let's dig deeper into each of these initiatives.

Collabratec™ is an online global collaboration environment that offers networking, vibrant communities, world class publishing, and unique features including Q&A forums and private research spaces! This allows the perspective to move beyond the organizational unit to the *individual*. Better yet, Collabratec™ will be available to the IEEE membership in the summer of this year!

The goal of the Global Entrepreneurship Program is to provide resources to budding entrepreneurs within the IEEE, mentorship with experienced entrepreneurs and incubation opportunities. The first offering of the GEP will be an online portal with resources to get started with entrepreneurship. So if you are just starting out or already a seasoned entrepreneur, look for communications from the GEP!

The Leadership and Volunteer Portal will feature a new re-designed website to enable the local volunteers to reach out to young professionals at events in their IEEE Region. The goal is to use major events and conferences to create or revitalize local young professional affinity groups. Branding and multi-purpose event kits will be available through the MGA or YPP committee.

The Corporate Sponsorships initiative aims to get companies to sponsor conferences and meetup events giving the attendees chances to network with local, multinational, small and large businesses, while providing the companies with advertising and recruiting opportunities. Since pathways for large businesses are already established, the focus of this team is on smaller companies and startups.

We, at EDS, can be an integral part of each of these IEEE Young Professional initiatives – by contributing articles to the EDS community on Collabratec™, volunteering as entrepreneurship mentors, participating in the GEP, setting up YP events, booths and talks at the EDS conferences, and contributing to the corporate sponsorship program.

My experience at the IEEE Young Professionals Program Committee Meeting showed me the energy and commitment we, the young professionals, are investing as a team to make both a global and local impact through the IEEE organization. If you would like to be a part of this exciting effort, please email me at sharmai@ieee.org.

Attendees of the 2015 IEEE Young Professionals Committee Meeting

Register Now for Upcoming EDS Webinars!

Terahertz Electronics for Sensing Applications
Presented by: **Dr. Michael S. Shur**, Rensselaer Polytechnic Institute

JULY 27 MONDAY
Monday, July 27, 2015
11:00 am–12:00 pm EDT

Abstract: Terahertz sensing is enabling technology for detection of biological and chemical hazardous agents, cancer detection, detection of mines and explosives, providing security in buildings, airports, and other public space, short-range covert communications (in THz and sub-THz windows), and applications in radioastronomy and space research. I will review the-state-of-the-art of existing THz sources, detectors, and sensing systems and prospects for novel emerging devices enabling terahertz electronics for sensing applications. Two-terminal semiconductor devices are capable of operating at the low bound of the THz range, with the frequencies up to a few terahertz achieved using Schottky diode frequency multipliers. High-speed three terminal electronic devices (FETs and HBTs) are approaching the THz range (with cutoff frequencies and maximum frequencies of operation above 1 THz and close to 0.5 GHz for InGaAs and Si technologies, respectively). A new approach called plasma wave electronics recently demonstrated terahertz emission and detection in GaAs-based and GaN-based HEMTs and in Si MOS and SOI, including the resonant THz detection. Graphene and 2D materials "beyond graphene" have also emerged as candidates for plasmonic THz detectors, modulators, and emitters. Emerging THz electronic devices have potential to revolutionize THz sensing technology.

For more information and to register, please visit the EDS website: http://eds.ieee.org/webinars.html

Engineering a Sustainable Society with Power Semiconductor Devices
Presented by: **Dr. Jayant Baliga**, North Carolina State University

AUGUST 26 WEDNESDAY
Wednesday, August 26
11:00 am–12:00 pm EDT

Abstract: Power semiconductor devices are an embedded technology hidden from the eyes of society. Silicon IGBTs are now used in all the major sectors of our economy including transportation, consumer, lighting, industrial, medical, and renewable energy generation. The improved efficiency derived from IGBT-based automotive electronic ignition systems has reduced gasoline consumption by 1.5 Trillion gallons over the last 25 years. During this time span, adjustable speed motor drives and compact fluorescent lamps have reduced electricity consumption by 73,000 TWhrs, which is equivalent to eliminating construction of 1366 one-GW coal fired power plants. The social impact includes consumer cost savings of more than $ 23 Trillion and carbon dioxide emission reduction by over 100 Trillion pounds.

This talk will review the evolution of the IGBT concept and provide examples of its applications in various sectors of the economy. The energy savings and carbon emission reduction enabled by the IGBT will be quantified. In addition, the talk will describe enhancing the performance of silicon power MOSFET products using the charge coupling concept and achieving a quantum leap in power device performance with emerging wide band gap semiconductor based power devices.

For more information and to register, please visit the EDS website: http://eds.ieee.org/webinars.html

New Webinars Available in the Archive

As part of our commitment to enhancing the value of membership in EDS, we are pleased to invite you to view a special webinar hosted by our friends in the IEEE Solid-State Circuits Society (SSCS) entitled, Physics is tough, but girls are tougher, presented by Wanda Gass.

Another important topic, Plagiarism Detection and Prevention: Crosscheck Overview was covered by Bill Hagen, IEEE Senior Manager Intellectual Property Rights, and Anthony Ven Graitis, IEEE Intellectual Property Rights Specialist.

To view these and any past events, please visit the EDS Webinar Archive at, http://eds.ieee.org/webinar-archive.html

Physics is tough, but girls are tougher
Presented by: **Wanda Gass**, IEEE Fellow

Abstract: In this talk, Wanda Gass examines the business case for why we need more women in Science, Technology, Engineering and Math (STEM) and she covers the things about the camp that spark an interest in physics. The data shows that the summer program translates into the participants having more self-confidence, better grades and a higher percentage of young women receiving a STEM degree in college.

Speaker Biography: Wanda Gass graduated from Rice University with a BS in Electrical Engineering in 1978 and received an MS in

Biomedical Engineering from Duke University in 1980. She worked at Texas Instruments for 32 years before retiring in 2012. Wanda is an IEEE Fellow for her pioneering work in the development of TI's first Digital Signal Processor (DSP). In 2014 she founded Design Connect Create, a nonprofit focused on expanding the reach of a successful program in Dallas to other schools districts across the country.

Plagiarism Detection and Prevention: CrossCheck Overview
Presented by: **Bill Hagen & Anthony VenGraitis**

Abstract: Publishing and authorship in the digital age is a dynamic, ever-changing proposition. With all the benefits these technological advancements offer, they create some new challenges as well. Chief among these is the ease with which original work can now be copied (either legitimately or otherwise).

In this webinar, plagiarism is examined in the era of electronic publishing and demonstrates tools the IEEE provides volunteers to help them identify similarities that exist between recently submitted manuscripts and other previously published papers. One such tool is CrossCheck.

Bill Hagen, Senior Manager, IEEE Intellectual Property Rights (IPR), presents an overview of CrossCheck, what it is, and why we use it. He explains how volunteers can access CrossCheck, either through a vendor system that has the tool integrated, or through the IEEE CrossCheck Portal, which is available to all publication volunteers. In addition, Hagen provides a demo on how to use the CrossCheck Similarity Reports that are issued for all manuscripts submitted through the system, explaining how to interpret the Similarity Report results and how to determine if CrossCheck detected a problem.

Background Info: IEEE began offering CrossCheck as an optional tool for publication volunteers to use in early 2009. As it became clear that CrossCheck could be a valuable quality check for content going into Xplore, the Publication Services and Products Board (PSPB) and Board of Directors approved policy in November 2012 that mandated the use of CrossCheck in all publications. Because most IEEE periodicals are handled through ScholarOne Manuscripts, CrossCheck was integrated in their submission system, and in February 2013 they began automatically uploading all manuscripts to CrossCheck at submission. This saved time and effort for the editors, who previously had to initiate the upload manually. In April 2013, the IPR Office launched the CrossCheck Portal. This allowed all publication volunteers to access CrossCheck and helped connect staff support to volunteers' use of the tool/service.

Report from the IEEE ED Coimbatore Chapter Program

EDS-ETC
Engineers Demonstrating Science: an Engineer Teacher Connection

On March 25th, the IEEE ED Coimbatore Chapter and the IETE Student Forum KARUNYA University, jointly organized a hands-on training session for Elenco Snap Circuits® kits as part of the Engineers Demonstrating Science: an Engineer Teacher Connection (EDS-ETC) program.

The goal of the program is to enable IETE chapter members to visit local schools or host events designed to engage young students in the field of electrical engineering. By utilizing the easy-to-use Elenco Snap Circuits® kits, students learn about electronic circuits using a "hands-on" approach to experience the exciting and creative field of electronics.

The Students were given a chance to get comfortable with the Elenco kit and later would be given a chance to demonstrate the same to kids in various schools nearby, thereby encourage them to consider electrical and electronic engineering as a career.

Students who took part in the training were so excited about the program and are looking forward for further development in the same. A few photos of student members working with the kits are included in this report.

Chapter News

IEEE EDS Mini-Colloquium, WIMNACT 45—Yokohama

The IEEE EDS Mini-Colloquium, WIMNACT-45, was held at Tokyo Institute of Technology, Yokohama, Japan, on February 19, 2015. After the greetings of T. Mogami, ED Japan Chapter Chair, S. Deleonibus, Leti and H. Iwai, TIT, there were five lecturers who gave the following talks: S. Deleonibus, "Future Heterogeneous Device and System Process Technology;" T. Ernst, Leti, "Nanoelectromechanical systems, paths for co-integration with CMOS;" M. Casse, Leti, "Advanced devices: Toward ultimate scaled Nanowire Transistors;" H. Iwai, TIT, "Future of Electron Devices technologies;" H. Wakabayashi, TIT, "Two dimensional material device technologies."

After lunch, there were 6 lectures: K. Tsutsui, TIT, "Ohmic contacts formation on AlGaN/GaN HEMTs by introducing uneven AlGaN layer structures;" K. Kakushima, TIT, "Resistive switching of CeO_x/SiO_2 stacked film based on anodic oxidation and breakdown;" T. Mogami, PETRA, "Positive for Silicon;" Z. Tang, Dalian University of Technology, "Some Researches of Thermal Problem in 3D ICs;" H. Wong, City University of Hong Kong, "Thermal Annealing and Interface Reaction of Lanthanum-based Subnanometer EOT Gate Dielectrics;" S. Dong, Zhejiang University, "ESD protection of nanometer CMOS process." All the above lectures are regarding the frontier of the electron device technologies, and the participants were satisfied the high level of the talks.

After the lectures, there were 31 poster presentations by students and young researches, followed by a reception, providing opportunities for them to interact top-level scientists in the world.

T. Mogami
ED Japan Chapter Chair

H. Iwai
EDS Region Chapter Committee Member

Attendees of WIMNACT-45 held at Tokyo Institute of Technology

Report on the IEEE EDS Mini-Colloquium on Nanometer CMOS Technology, Shenzhen

The 46th Workshop & IEEE EDS Mini-Colloquium (MQ) on Nanometer CMOS Technology (WIMNACT-46) was organized by IEEE ED/SSC Beijing Section Shenzhen Chapter at the PKU Graduate School Shenzhen Campus on April 18, 2015.

The event started with a welcome by Prof. Xinnan Lin, the Chapter Chair of the IEEE ED/SSC Beijing Section Shenzhen chapter. It is then followed by technical presentations are given by four EDS Distinguished Lecturers. The title of their presentations are given below:

- "Carbon Nanotube Interconnect Vias," by Prof. Cary Yang, Santa Clara University
- "Compact Modeling for High-Power Circuit Design and Its Application," by Prof. Mitiko Miura-Mattausch, Hiroshima University
- "A Unified Compact Model for Generic HEMTs," by Prof. Xing Zhou, Nanyang Technological University

- "Microelectrode Array for Communication Between Silicon Chips and Living Cells," by Prof. Mansun Chan, Hong Kong University of Science & Technology

Over 50 local students and professors attended the MQ and there are lively interaction between the speakers and the audiences.

A student poster competition is also co-organized with the MQ. Seventeen student posters were put on display. One Best Student Poster Award and three Outstanding Student Awards were given out at the event.

Attendees of WIMNACT-46 held at PKU Graduate School Shenzhen Campus

ED NIST Student Chapter organizes the 4th IEEE EDS Mini-Colloquium

The IEEE ED NIST Student Chapter organized the 4th IEEE EDS Mini-Colloquium on February 20, 2015. Prof. Subir Kumar Sarkar, Jadavpur University, Prof. G N Dash, Sambalpur University, Prof. C K Sarkar, Jadavpur University, and Prof. M K Radhakrishnan from Nanorel, Bangalore, were the speakers of the MQ, which was attended by nearly 236 students, faculty and research scholars from various institutions.

Ajit K Panda
ED NIST Student Chapter Chair

Attendees of the ED NIST Student Chapter's 4th IEEE EDS Mini-Colloquium

ED Delhi Chapter Organizes Mini-Colloquia on Compact Modeling Techniques

–by Mridula Gupta and Manoj Saxena

The ED Delhi Chapter organized a Mini Colloquia on "Compact Modelling Techniques for Nanoscale Devices and Circuit Analysis" on January 13, 2015, which was attended by over 100 students and faculty members. Professor Anisul Haque of the Department of Electrical and Electronic Engineering, East West University, Dhaka, Bangladesh, gave his talk on "Quantum mechanical effects in surface potential based MOS compact models;" Dr. M.K. Radhakrishnan, NanoRel, Bangalore, India, discussed the Analysis, Challenges and Reliability in Si Nano Devices; Professor Souvik Mahapatra, Department of Electrical Engineering, Indian Institute of Technology Bombay, Mumbai, India, discussed Macroscopic and Stochastic Aspects of Negative Bias Temperature Instability in CMOS Devices and Circuits, and the last talk was delivered by Professor Gana Nath Dash, School of Physics, Sambalpur University, Odisha, India on the topic "Modeling Issues with Graphene FETs".

Attendees of the ED Delhi Chapter Mini-Colloquia

Regional News

USA, Canada & Latin America (Regions 1-6, 7 & 9)

ED/MTT Orange County

–by Héctor J. De Los Santos

The Orange County, California's EDS/MTT Joint Chapter was honored on January 29, 2015 with the visit of Prof. Dr. Hermann Schumacher, Director of the Institute of Electron Devices and Circuits, University of Ulm, Germany. Prof. Dr. Schumacher presented the talk *"Si/SiGe BiCMOS Transceiver ICs for a Ka-band Actively Steered Reflect Array Antenna."*

Hermann Schumacher received his doctorate in engineering (Dr.-Ing.) degree from RWTH Aachen, Aachen, Germany, in 1986. From 1986 to 1990, he was a member of technical staff at Bellcore, Red Bank, New Jersey, working on long-wavelength fiberoptic receivers and on early InP-based heterojunction bipolar transistors. In 1990, he joined Ulm University, Ulm, Germany as professor in the Institute of Electron Devices and Circuits. His research interests cover heterostructure devices (at present, most Si/SiGe HBTs and AlGaN/GaN HFETs) and their application in microwave and millimeter-wave circuits. Prof. Schumacher was the founder of one of the first English taught Master programs in electrical engineering in Germany and, for 17 years until June 2014, its director. He served as Vice President for Research for Ulm University from 2000–2003, and is now, in addition to his institute appointment, also the director of Ulm University's School of Advanced Professional studies, which develops continuing education Master programs, a new strategic direction for Ulm University.

Dr. Hermann Schumacher

The talk presented a proposed solution to the serious problem of unit cell size minimization, encountered as phased arrays applications move into the millimeter-wave range. In particular, a solution where four vector modulators are placed on a single Si/SiGe BiCMOS chip, which also contains mixed-signal electronics to control phase and magnitude via a common I2C serial interface, was discussed. In this approach, the signal path through the vector modulators can be reversed to allow transmit and receive operation, and reconfiguration is achieved using MOS switches and, in one version, also with an RF MEMS SPDT switch, which is tightly integrated into the backend of line (BEOL) of the underlying BiCMOS technology.

For additional information contact Dr. Héctor J. De Los Santos at hector.delossantos@ieee.org.

2015 IEEE 7th International Memory Workshop (IMW) Summary

–by Agostino Pirovano

The seventh IEEE International Memory Workshop (IMW) was held at the Hyatt Regency, Monterey, California from Sunday May 17th through Wednesday May 20th, 2015. Although it is the seventh IMW meeting to be held this year, it has a long history of Non-Volatile Semiconductor Memory Workshops (NVSMW) dating back to 1976. In 2008, NVSMW and the International Conference on Memory Technology and Design (ICMTD) merged to incorporate both the volatile and non-volatile memory aspects in one forum while maintaining the workshop experience. And the scope was extended from non-volatile memory technology and design, which had been successfully discussed in more than 30 years of NVSMW, to the other memory technologies, which were the focus of ICMTD. The IMW is a unique forum for specialists in all aspects of memory (non-volatile & volatile) microelectronics and people with different backgrounds who wish to gain a better understanding of the field. Attended by more than 200 people every year, the morning and afternoon technical sessions are organized in a manner that provides ample time for informal exchanges amongst presenters and attendees.

This year's program included a one-day short course chaired by Pei-Ying Du from Macronix, with lectures on the reliability of Flash based Solid-State-Drives, database technologies for Non-Volatile RAM, 3D-DRAM, ReRAM and 3D Vertical NAND Flash. The IMW program also included an interesting panel discussion addressing the remarkable question—Future of Memory: Application-driven or Technology-driven, which will dominate in the new era of computing?—followed by a poster session with a reception banquet sponsored by Applied Materials.

The single-track conference spanned three days, including a half-day invited talks session given by experts in the memory field—Sung-Kye Park (SK-Hynix), Will Akin (Micron), Dale Juenemann and Prasad Alluri (Intel), Barbara DeSalvo (CEA-LETI), Thomas Jew (Freescale), and Shinobu Fujita (Toshiba) - providing an exciting overview of the main trends for memory technologies and applications. The IMW is also an excellent forum to present new and original technical works and this year technical program comprised 32 excellent papers selected by the

technical committee among more than 65 papers submitted and covering the major categories of memory technologies (RRAM, NAND DRAM, emerging technologies) and applications (SSD, eNVM, e-MMC). Among the most exciting news presented at the conference, a selector for high density resistive RAM applications, a procedure to reduce cell variation in PCM multi-level applications, a machine learning prediction for enhancing the endurance in ReRAM SSD System, and a triple protection structured COB FRAM capable of 10^{17} endurance.

IMW was also selected for hosting the presentation of the 2015 IEEE Reynold B. Johnson Information Storage Systems Award, an IEEE Technical Field Award presented to individuals for outstanding contributions to information storage systems, with emphasis on computer storage systems. During the IMW social dinner, the 2015 IEEE Division Director for Region 6, Tom Coughlin, awarded D. Moran, A. Ban and S. Litsyn "for pioneering contributions to storage systems based on Flash memory."

The next IMW will be held in May 2016 in Europe. For more details on the IMW conference please visit the IMW website http://www.ewh.ieee.org/soc/eds/imw/. IMW technical proceedings are available on the IEEE Xplore database.

~Adam Conway, Editor

ED Mexican Chapters

–by Arturo Escobosa

On February 20–21, 2015, an EDS Mexican Chapters' Meeting was held at the facilities of INAOE in Tonantzintla, a small village near Puebla in México. INAOE is a renowned research center focusing in Astrophysics, Optics, Electronics and Computer Science, which was founded in 1971.

Participants from Veracruz, Morelia, México City, and Puebla, took advantage of the visit to INAOE by Jacobus Swart (SRC Region 9 Chair), and Fernando Guarin (EDS Secretary), to hold a meeting of the Mexican EDS chapters, exchanging opinions and defining future actions to boost EDS activities in the country.

Participants of EDS Mexican Chapters Meeting

After a warm welcome by Roberto Murphy and a general presentation of Region 9 activities by Jacobus Swart, several issues related to EDS activities were discussed, such as: how to increase the interaction between different EDS chapters and members increasing our presence and activities in EDS.

The most important agreements on concrete actions were:

- The creation of a short course on Electronic Devices using the facilities of INAOE. Part of the funds assigned to Region 9 SRC can be used to support participant´s travel expenses. Brazil has a successful program in this line.
- Increase the participation in the EDS-ETC program. To start, an induction workshop is to be hosted by the *Instituto Tecnológico de Morelia* Student Branch Chapter. The intention is to involve all Mexican EDS chapters in the program.
- To organize the Workshop of Advanced Devices and Materials as a special session of the ROPEC 2015 (International Autumn Meeting on Power, Computing and Electronics). This is intended to be a forum for experts in the field.
- To continue organizing the ICCDCS (International Caribbean Conference on Circuits, Devices and Systems); the 2016 edition is going to be held in Cancún, México.

~Joao A. Martino, Editor

Europe, Middle East & Africa (Region 8)

ED IRE NASU-Kharkiv Student Branch Chapter

In accordance with the website http://ewh.ieee.org/sb/ukraine/ire-kharkiv/chapters/eds/index.php the Chapter is going to make in June, 2015, a trip to the Experimental Center of Institute of Ionosphere of Ministry of Education and Sciences & National Academy of Sciences of Ukraine. The Institute houses one of the world largest incoherent radar experimental facilities.

MTT/ED/AP/CPMT/SSC West Ukraine Chapter

–by Mykhaylo I. Andriychuk

The IEEE MTT/ED/AP/CPMT/SSC West Ukraine Chapter was a co-organizer of the 13th International Conference "The Experience of Designing and Application of CAD Systems in Microelectronics" (CADSM 2015). The Technical Co-Sponsorship from the IEEE Ukraine Section and from the Chapter was provided for the event. The Conference was held on February 24–27, 2015, in the beautiful resort village Polyana Svalyava, Zakarpattya, Ukraine.

More than 160 papers were submitted for presentation at the Conference. Following a review, 136 papers from Iraq, Kazakhstan, Mexico, Poland, Russia, and Ukraine were included in the Conference Program.

This year the following topics were discussed: Modeling and Optimization for Integrated Circuit Manufacturing, Models and Methods for Microelectronic Device and System Design in Radio Electronics, Models and Methods for Microelectromechanical Systems, Design of Specialized Systems and Devices, Optimal Design Problems, Testing and Reliability Issues, Modern Information Technology for CAD.

The most interesting works were reported at the plenary sessions. Prof. Alexander Zemliak, University of Puebla, Mexico, presented a general strategy for development and optimization of ICs and electronic devices. Based on this approach the design problem is reduced to analog network design with a minimum computer time and is formulated in terms of functional minimization problem of the control theory. A concept of the Lyapunov function was proposed to analyze the behavior of the design process.

The active discussion was stimulated also by Prof. Jan Dziuban, Wroclaw University of Technology, Poland. His talk was devoted to silicon MEMS pressure sensors in medical, automotive, industrial, military equipment and in consumer devices, e.g. smartphones. The most commonly used piezoresistive and capacitive pressure sensors cannot be used at harsh environment conditions: high temperature, strong electromagnetic fields, ionizing radiation. In this case a new pressure sensor design is required including optical measurement techniques which are non-contact, non-destructive, temperature insensitive and adaptive in harsh environment.

Many young scientists, engineers, students, and PhD students participated in the Conference. They received the opportunity to present the results of their research, as well as to receive knowledge from their experienced colleagues. The wonderful scenery of the Carpathian Mountains contributed to the fruitful Conference.

ED/AES/AP/MTT/GRS/NPS East Ukraine Chapter

In accordance with the website http://www.rocket.kharkov.ua/~euachapter/ the Chapter co-organized in the second half of 2014 two events. The 15th International Conference on Mathematical Methods in Electromagnetic Theory was held on August 26–28, 2014 in Dnipropetrovsk, Ukraine IEEE. It was organized by AP/MTT/ED/AES/GRS/NPS/EMB East Ukraine Joint Chapter in cooperation with IEEE APS, MTTS and EDS. The 4th Microwaves, Radar and Remote Sensing Symposium (MRRS-2014) was held on September 23–25, 2014 in Kiev, Ukraine. These symposia integrate researchers, experts and students who work in the aread of electromagnetic theory and applications; microwaves; radar technology, systems and signal processing; remote sensing methods and data processing. The MRRS-2014 symposium was organized by IEEE SP/AES Ukraine (Kiev) Joint Chapter in collaboration with National Aviation University, Kiev, Ukraine.

CADSM-2015 Conference opening ceremony attendees

IEEE ED/AES/AP/MTT/GRS/ NPS East Ukraine Chapter

–by Nikolay Cherpak, Mikhail Balaban, and Ganna Veselovska

In 2015 the Chapter is a co-organizer and co-sponsor of IEEE annual conferences, namely:

- The 35th International Conference on Electronics and Nanotechnology, ELNANO 2015, at National Technical University of Ukraine "Kyiv Polytechnic Institute", April 21–24, 2015, Kyiv, Ukraine; this event is intended to bring together researchers from leading universities, research laboratories and industry working in the areas of nanotechnology, biomedical electronics, signal processing, power electronics, smart grid and electronic systems.
- International Young Scientists Forum on Applied Physics, YSF 2015, at Oles Honchar Dnipropetrovsk National University September 29–October 2, 2015, Dnipropetrovsk, Ukraine; the Forum is designed as a means stimulating interactions and collaboration (projects) and motivating to move forward in science.

Additionally, several times a year the Chapter committee holds technical meetings at O.Ya. Usikov Institute for Radiophysics and Electronics of National Academy of Science of Ukraine (IRE NASU). At the meetings numerous engineering problems are considered, e.g. theory of semiconductors, metals, and plasma as well as experiments and simulations related to electron devices. The committee plans to have at least 5 such meetings in 2015.

ED/AP/MTT/COM/ EMC Tomsk Chapter

In accordance with the website http://chapters.comsoc.org/tomsk/en/events.html, the Chapter has the following events planned:

- Student Paper Contest and Conference on the Information Security (SIBINFO), April 14–15, Tomsk, Russia;
- International Siberian Conference on Control and Communications (SIBCON), May 21–23, Omsk, Russia with a technical sponsorship of IEEE ED and MTT Societies;

A technical sponsorship of Tomsk IEEE Chapter & Student Branch for both events is also acknowledged.

ED/MTT Republic of Georgia Chapter

–by Tamar Gogua and Mykhaylo I. Andriychuk

The XIXth Edition of the International Seminar/Workshop "Direct and Inverse Problems of Electromagnetic and Acoustic Wave Theory" DIPED-2014 was held at the Tbilisi State University, Georgia, on September 22–25, 2014. It was organized by IEEE MTT/ED/AP/CPMT/SSC West Ukraine and MTT/ED/AP Georgia Chapters in cooperation with Tbilisi State University (TSU) and Institute of Applied Problems in Mechanics and Mathematics, NASU, Ukraine. IEEE APS, EDS, MTT-S, SSCS and IEEE Section Ukraine provided the technical co-sponsorship. Thanks to TSU financial support the number of attendees from outside of Georgia were increased (Figure 1). Locally the Workshop was organized by Prof. Revaz S. Zaridze, Chairman of the Organizing Committee, Dr. Tamar Gogua and Dr. Giorgi Ghvedashvili, IEEE MTT/ED/AP Georgian Chapter.

The program consisted of 44 papers, including 5 invited talks. Scientists from Georgia, Germany, Israel, Pakistan, Poland, Russia, South Korea, USA, and Ukraine presented their papers arranged in sections: Theoretical Aspects of Electrodynamics, Diffraction and Scattering, Antenna Synthesis and Inverse Problems, Novel Methods in Electrodynamics, Antenna Design, Analytical and Numerical Methods, Acoustics and Remote Sensing.

Prof. Alexander G. Ramm (Kansas State University, USA), gave a talk on theory of wave scattering by small bodies (particles). In his presentation,

DIPED-2014 participants at the opening ceremony

the mathematical foundations of electromagnetic wave scattering theory for small impedance particles of an arbitrary shape were given. The report stimulated the active discussion. Other presentations can be mentioned: "Base Station Antenna's EM Field Distribution in the Room with a Human Model Inside" by Ms. Veriko Jeladze, "Comparing Different Approaches to Linear Antenna Synthesis Problems according to Power Radiation Pattern" by Dr. Olena Bulatsyk, and a talk on the electromagnetic analysis of a complex structure cylindrical antenna by Prof. Guram Kevanishvili.

Many young scientists attended the Seminar. The following researchers received the Best Young Speaker Award: Ms. Veriko Jeladze, Dr. Olena Bulatsyk, Mr. Victor Lysechko, Mr. Giga Gabriadze, Mr. Giorgi Jambazishvili, and Mr. Kaka Lomia.

After the Workshop its participants took part in an excursion in Tbilisi. In our opinion, DIPED-2014 was a good opportunity to intensify cooperation between scientific groups involved in the diffraction theory and its application, and to expand existing contacts. The next, 20th Edition of DIPED will be held at the Institute of Applied Problems in Mechanics and Mathematics, Lviv, Ukraine, on September 21–24, 2015.

IEEE ED Romania Section Chapter

–by Cristian Ravariu

The ED Romanian Chapter has been recently revitalized and celebrates in May 2015 the first year of the activity. The activity was restored with the aim of few enthusiastic ED members, supported by our colleagues from the local Solid State Circuits Society Chapter, encouraged by EDS community and by the IEEE-Romania Section. The members of the young ED Chapter wish to express their gratitude to all the contributors of this initiative. The Electron Device Chapter becomes a joint Chapter to SSCS and is looking forward to a good collaboration.

Since 2014 the main activities of the Chapter have been focused on a few technical meetings devoted to gated diodes in breakdown regime, which demonstrate faster switching operation than the MOSFETs (invited speaker—Al. Rusu, EPFL), to pinFET optimization for the telecommunication applications, to integrated biosensors using active electronic devices, to SOI devices, to new challenges for Nano-Electronics. These issues were partly presented during the ED tour across Romania, including Bucharest, Iasi, Brasov, Timisoara and Sinaia.

At the end of 2014 a new officer board of the Chapter was elected. More than 7 colleagues became student members. Three papers presented at the International Semiconductor Conference CAS 2014, Sinaia, October 13–15, 2014, received the Best Paper Awards in a form of a free IEEE EDS membership in 2015. The plans for 2015 include: stimulation of new members joining, student awards at the CAS 2015 IEEE Conference and at the Student ETTI 2015 competition, organization of the EDS conferences and technical meeting, assisting potential members in publishing their works in ED Journals and at the related conferences, finding new partners involved in the electron device research for preparation of research project proposals and for other forms of collaboration with the Chapter.

~Daniel Tomaszewski, Editor

Asia & Pacific (Region 10)

ED UCAS Student Chapter

–by Yang Li

ED University of Chinese Academy of Sciences (UCAS) - Beijing Student Branch Chapter, held a visiting tour to BOE in Beijing on April 16th. BOE Technology Group Co., Ltd., founded in April 1993, is the world's leading supplier of semiconductor display technologies, products and services. It is among the top five companies within the global display industry.

During the visit, engineers from BOE introduced TFT-LCD (Thin Film Transistor—Light Emitting Diode) and showed the Gen 8.5 TFT-LCD processing line. Many innovations and developments of display industry are also shown and introduced to the students, like OLED (Organic Light-Emitting Diode), transparent display panel, eye- controlled operation and so on. After the visit, academic exchange is held. Manager of technology development department introduced their pioneer work and answered questions from students.

The visit to BOE aimed at enhancing the students' understanding

ED University of Chinese Academy of Sciences (UCAS) – Beijing Student Branch Chapter, visiting BOE in Beijing

of industry companies and the development of the microelectronics industry. It may help to inspire students to think about how to better combine scientific research work with the real industry applications and their future career planning.

~Mansun Chan, Editor

ED Kansai

–by Michinori Nishihara

The ED Kansai Chapter held a feedback meeting from the 2014 IEDM with 20 students and members from both academia and industries. The meeting was held at the Osaka Institute of Technology Umekita Knowledge Center, in Osaka, Japan, February 3, 2015. The following two researchers reported: Dr. Tatsuya Kunikiyo of Renesas Electronics, on Power Devices and Image Sensors and Dr. Shingo Sato of Kansai University, on Advanced FET sessions.

Dr. Kunikiyo reported that SiC and GaN based power devices show clearly better performance than the one with Silicon. The better efficience of those new devices will have a large impact to our society. Advancement of power semicondutor technology will contribute to the growth of Hibrid Electric Vehicles and Electric Vehicles market.

Dr. Tatsuya Kunikiyo, speaker

Dr. Shingo Sato, speaker

Dr. Sato reported on the aspects of reliability and modeling of nanoscale FETs which indicate steady progress in the most advanced semiconductor technology front.

After the IEDM2014 feedback meeting, we held the annual general meeting to review activities of ED Kansai in 2014 and to discuss plans for 2015.

Also discussed was a plan for the upcoming 2015 IMFEDK international conference, which is to be co-sponsored with the Microwave Theory and Techniques Society Kansai Chapter on June 4–5, 2015 in Kyoto, Japan. Please check www.imfedk.org for more information.

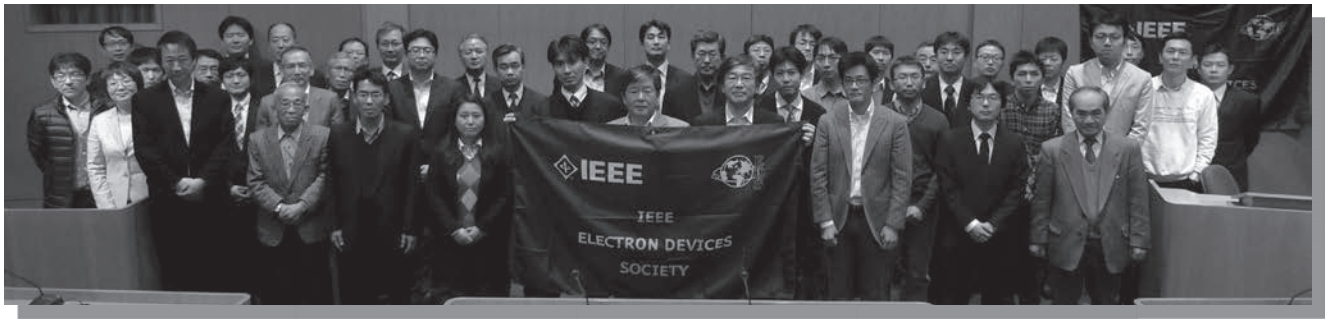
ED Japan

–by Tohru Mogami

On February 12, 2015, the annual meeting of the ED Japan Chapter was held at the University of Tokyo. Dr. Tohru Mogami, Japan Chapter Chair and Prof. Masaaki Niwa, Vice Chair, reported 2014 activities and 2015 plans of the Chapter. At the meeting, the 2014 EDS Japan Chapter Student Award (VLSI & IEDM) was presented to 6 students, who made excellent presentations at the Symposium on VLSI Technology 2014 and IEDM 2014. The award winners are posted on the Japan Chapter's webpage: (http://www.ieee-jp.org/japancouncil/chapter/ED-15/ed15_award.htm).

After the annual meeting, the IEDM 2014 Report Session was held. Nine Japanese members of the

Participants of the 2014 IEDM feedback meeting



Attendees and presenters of the IEDM 2014 Report Session

2015 ED Japan Chapter executive committee meeting attendees

IEDM program committee reported on summary, topics and research trends of their sub-committees, for more than sixty attendees. This session provided a good opportunity for the attendees to understand the research trends of various areas, especially for those who were not able to attend the IEDM.

The executive committee meeting of the EDS Japan Chapter was also held on the same day and the plans for 2015 of the Chapter were approved. The EDS Japan Chapter Executives: Dr. Tohru Mogami; Chair, Prof. Masaaki Niwa; Vice Chair, Dr. Meishoku Masahara; Secretary, and Prof. Takahiro Shinada; Treasurer invited the guests (the 9 guest speakers of the IEDM Report Session), as well as Prof. Hiroshi Iwai, EDS Jr. Past President, Prof. Kuniyuki Kakushima, EDS Newsletter Regional Editor, and Dr. Naoki Yokoyama, Past EDS Japan Chapter Chair, Prof. Akira Toriumi, Past EDS Japan Chapter Chair, Koji Kita, Past EDS Japan Chapter Treasurer.

IEEE EDS Distinguished Lecture at Tokyo Institute of Technology

–by Hiroshi Iwai

Prof. Arun Chandorkar of Indiana Institute of Bombay was invited by Tokyo Institute of Technology to deliver an IEEE EDS Distinguished Lecture, entitled by "Co-Design of RF Power Amplifier with consideration of issues of Device, Circuit and Technology," at Suzukakedai campus of Tokyo Institute, Yokohama, Japan, on March 4, 2015. The talk highlights some of these RF systems and discusses Design of a RF Power Amplifier on a Nano CMOS technology platform. DeMOS device has been proposed to realize Power Amplifier. The key design parameters of a Shallow Trench Isolation based drain-extended MOS device are experimentally discussed for high power RF applications in advanced CMOS technologies. Active discussion was conducted after his talk.

~Kuniyuki Kakushima, Editor

Prof. Arun Chandorkar of Indian Institute of Bombay (third from left), with organizers and attendees of EDS DL

ED Kuala Lumpur, Malaysia

–by Badariah Bais & Zubaida Yusoff

2015 EDS Malaysia AGM

On the of January, 16, 2015, the ED Malaysia Chapter held its Annual General Meeting at the Palm Garden Hotel, IOI Resort, Putrajaya. Assoc. Prof. Dr. Badariah Bais from Universiti Kebangsaan Malaysia (UKM) was elected to be the Chapter Chair while Assoc. Prof. Dr. Norhayati Soin from Universiti Malaya (UM) was elected to be the Vice-Chair. Assoc. Prof. Dr. P. Susthitha Menon from the Institute of Microengineering and Nanoelectronics (IMEN), Universiti Kebangsaan Malaysia (UKM), Dr. Zubaida Yusoff from Multimedia University and Assoc. Prof. Dr Roslina Sidek from Universiti Putra Malaysia (UPM) were also elected to be the Secretary, Assistant Secretary and Treasurer respectively. Several members from various universities and industries in Malaysia were also elected to be part of the committee. EDS Malaysia's main activity for 2015 is to organize the 10th IEEE Regional Symposium of Micro and Nanoelectronics (IEEE-RSM2015) which will be held on August 19–21, 2015, at Primula Hotel, Kuala Terengganu. Other activities include IEEE Distinguished Lecture (DL) talks, technical workshops, membership drive projects, final year project awards and social activities.

10th IEEE Regional Symposium on Micro and Nanoelectronics (IEEE-RSM2015)

From August 19 to 21, 2015, the ED Malaysia Chapter will organize the 10th IEEE Regional Symposium on Micro and Nanoelectronics (IEEE-RSM2015) at Primula Hotel, Kuala Terengganu. This is the tenth RSM organized by the Electron Devices Chapter of the IEEE Malaysia Section and is chaired by Assoc. Prof. Dr Mohd. Nizar Hamidon from the Institute of Advanced Technology, Universiti Putra Malaysia with Universiti Sultan Zainal Abidin (UNISZA) as a co-organizer. Over the last 18 years, RSM has become the prominent international forum on micro and nano electronics embracing all aspects of the semiconductor technology from application of microelectronics in product development, device modeling & simulation, VLSI design & test, device packaging & testing, device physics and characterization, material and new fabrication facilities technologies, micromachining, microsensors and MEMS,mocrowave device and MMIC, opto-electronics and photonics technology,process technology (CMOS, bipolar, BiCMOS, GaAs), realibility and failure analysis, training and human resource development in microelectronics industry, nano technology and nano electronics.

This conference offers two keynote lectures by distinguished persons in their own fields with an expected participation of more than 100 participants from more than 10 countries from around the world including India, Thailand, Australia, Taiwan, China, Bangladesh, Japan and Indonesia. The keynote speakers and their keynote titles are Dr. Meyya Meyyapan from NASA Ames Research Center, USA , who will be giving a talk on "*Nanotechnology: Development of Practical Systems and Nano-Micro-Macro Integration"* and Prof. Dr. Hirofumi Tanaka from Kyushu Institute of Technology, Japan, who will talk on "*Brain-like signal generating electric devices made of single-walled carbon nanotube and nanoparticle complex*." More info about the conference can be obtained at the conference website http://ieeemalaysia-eds.org/rsm2015/home.html

Technical Talk and Membership Drive at UNISZA

On March, 1, 2015, representatives of the ED Malaysia Chapter visited Universiti Sultan Zainal Abidin (UNISZA) to deliver a technical talk as well as to introduce and promote IEEE EDS membership to UNISZA students and staff. This event was conducted at UNISZA library auditorium and was attended by 80 people. Assoc. Prof. Dr. Roslina Sidek delivered a talk on "Semiconductor Revolution" while Assoc. Prof. Dr Norhayati Soin delivered a talk about chapter.

Technical Talk at IMEN

On March, 18, 2015, the chapter co-organized a technical talk on "*I Have Never Registered Even Though I Have Worked as an Engineer for Years—Is It Really Necessary?*" which was delivered by Mr. Cheang Kok Meng, who is a Senior Member of the IEEE and who is also the Former Executive Director of the Institution of Engineers, Malaysia. The talk was held at the Institute of Microengineering

Members who attended the IEEE ED Malaysia AGM 2015

Participants of the technical talk/membership drive at UNISZA

Participants of the technical talk at IMEN with Mr Cheang

Prof. Shantanu Mahapatra delivering technical talk at IIEST Shibpur

and Nanoelectronics (IMEN), Universiti Kebangsaan Malaysia (UKM) and attended by both students and staff. Mr Cheang explained about the importance of being registered with professional societies in an attempt to gain experience and enhance networking.

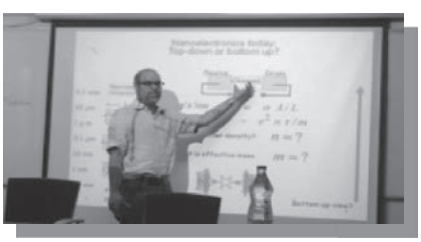
~P Susthitha Menon, Editor

ED Calcutta Chapter

–by Swapnadip De and Soumya Pandit

The ED Calcutta Chapter, in association with IIEST Shibpur, organized a technical talk on "Nanoscale Quantum Transport-Beyond Charge based Nanoelectronics," on February 12, 2015, by Prof. Bhaskaran Muralidharan, Department of Electrical Engineering, Indian Institute of Technology Bombay. The talk was attended by faculty members from IIEST Shibpur and 40 post graduate students and research scholars from IIEST, University of Calcutta and Jadavpur University.

The ED Calcutta Chapter in association with IIEST Shibpur, also organized a one-day workshop on "The Art of Compact Modeling", on February 19, 2015, by Prof. Santanu Mahapatra, Department of Electronic Systems Engineering, Indian Institute of Science, Bangalore. The workshop was extremely successful in bringing together students from diverse domains of Electronics Engineering and VLSI Technology and provided them an opportunity for hands-on experience on Semiconductor device modeling. The workshop was attended by 45 post graduate students and research scholars from IIEST, University of Calcutta and Jadavpur University. The Department of Electronics & Communication Engineering, HITK and IEEE EDS Calcutta Chapter jointly organized a technical talk by Dr. Shubhajit Roy Chowdhury, Assistant Professor, Centre for VLSI and Embedded Systems Technology, IIIT Hyderabad, India at Heritage Institute of Technology on February 6, 2015. The talk was attended by over 50 students and faculty members of Heritage Institute of Technology.



Prof. Bhaskaran Muralidharan delivering technical talk at IIEST Shibpur

Dr. Shubhajit Roy Chowdhury delivering his talk at Heritage Institute of Technology

ED NIST Student Chapter

–by Ajit Kumar Panda

The ED NIST Student Chapter organized a one day seminar on "Strain Engineering in Silicon Nanoelectronics," on March, 30, 2015. Prof. C K Maiti, formerly professor at Department of ECE, IIT-Kharagpur, talked about the recent trend in technology and the strain engineering like bidirectional strain, unidirectional strain, process induced strain and effect of scalability. 33 participants including IEEE member and non-members had attended the seminar to enhance their knowledge as well as to focus on the new areas of research activity in devices and fabrication.

The chapter also organized its first National Conference on Devices and Circuits on February, 21, 2015. Dr. Sudeb Dasgupta, IIT-Roorkee, and Dr. Sanjeev Manhas, IIT-Roorkee, were the main speakers of the conference which was attended by over 120 delegates from IIT-Kharagpur, NIT-Silchar, VSSUT-Burla, SUIIT-Sambalpur, KIIT-Bhubaneswar, ITER-Bhubaneswar, Berhampur University and NIST-Berhampur.

ED Coimbatore Chapter

–by D. Nirmal

On February 13, 2015, the ED Coimbatore Chapter in association with Department of Electronics and Communication Engineering, Karunya University, organized a DL talk on "Trends and Challenges of Silicon-Nano devices," by Dr. M. K. Radhakrishan, wherein he initially gave an overview of the IEEE Electron Devices Society and Quest EDS program. During his talk, he discussed reliability concerns during fabrication process of silicon-nanodevice structure, applications of Dual–Channel Nanowire Transistors.

Distinguished Lecture attendees at the formal inauguration of ED Coimbatore Chapter

AP/ED Bombay Chapter

–by V. Ramgopal Rao

The AP/ED Bombay Chapter, IIT Bombay, organized around fifteen talks in diverse areas such as MEMS fabrication, organic semiconductors, photovoltaics, semiconductor devices, CMOS technology, embedded system design, reliability and device characterization. Prof. Hiroshi Iwai from Tokyo Institute of Technology, Japan, former-President, IEEE EDS and a recipient of the IEEE J.J. Ebers Award and IEEE Paul Rappaport Award, delivered an EDS Distinguished Lecture on "Future of Logic Nano CMOS Technology." In his lecture, he discussed the importance of CMOS devices and stressed that there are no other promising candidates which could replace CMOS with better performance for high-density integration with low cost for the moment.

Prof. Subodh Mhaisalkar from NTU Singapore in his lecture addressed the various challenges and opportunities in perovskite solar cells beyond methyl ammonium lead-iodide with particular emphasis on their optoelectronic properties. Prof. Chris McNeil from Monash University delivered a talk on "Characterizing organic semiconductors with soft x-rays." In his talk, he provided an overview of the range of microscopy, reflectivity and scattering techniques based on soft x-rays that have been developed in recent years and their utility for providing new insight into the complex structure of organic semiconductor thin films. Dr. Jai Verma from Intel Corporation in his talk titled, "Band gap and polarization engineered III-nitrides UV LEDs", discussed about the potential applications of light-weight and robust ultraviolet (UV) light emitting sources in water purification, bio sensors, solid state lighting and lithography. Prof. Ulf Schlichtmann's talk, "Reliability and Robustness Challenges in IC and Embedded System Design—How can EDA help?" gave an overview about the current situation of IC and Embedded System Design. It addressed reliability and robustness challenges and reported on research activities and results on Electronic Design Automation (EDA)

One-day seminar organized by ED NIST Student Chapter

Prof. Subodh Mhaisalkar delivering his lecture

(From left Mr. Nagesh Ch, Dr. A K Sunaniya, Mr. G. P. Keshri, Dr. Taimoor Khan, Dr. R. H. Laskar, Prof. F. A. Talukdar (Branch Counselor), Dr. T. R. Lenka (Chair), Mr. Koushik Guha (Coordinator), Mr. Gaurav Saxena and attendees of the Workshop). Organized by the ED National Institute of Technology Silchar Student Branch Chapter

techniques at TUM which address these challenges.

ED National Institute of Technology Silchar Student Chapter

–by Trupti Ranjan Lenka

The EDS Student Branch Chapter—National Institute of Technology Silchar, Assam, India, organized a one-day Workshop on "MEMS" on Februate 7, 2015, at Department of Electronics and Communication Engineering, NIT Silchar. Mr. Gaurav Saxena, IIT Guwahati and Mr. Nagesh Ch., IIT Guwahati, delivered technical talks on MEMS which was attended by engineering students and research scholars of Department of ECE, NIT Silchar.

EDS Delhi Chapter

–by Mridula Gupta and Manoj Saxena

During January 30-31, 2015, the chapter jointly organized the Second Lecture Workshop on Trans-disciplinary Areas of Research and Teaching by Shanti Swaroop Bhatnagar Awardee with Department of Electronics, Deen Dayal Upadhyaya College, University of Delhi. The inaugural talk was delivered by Professor Asis Datta, FTWAS, Former Vice Chancellor, Jawaharlal Nehru University, New Delhi, Dr. Indira Nath, FTWAS, Former, Head, Dept. Of Biotechnology, AIIMS, Delhi Former, Raja Ramanna Fellow highlighted the importance of Health and Well being in the Changing Urban Environment, Professor Surendra Prasad, Former Director-IIT Delhi addressed some fundamental breakthroughs in Communication Theory, Professor S. K. Joshi, Distinguished Emeritus Scientist CSIR & Honorary Vikram Sarabhai Professor, JNCASR, NPL covered 100 Years of X-ray Crystallography and Professor Sankar K. Pal, FTWAS, FIEEE, Distinguished Scientist and former Director, Indian Statistical Institute, Kolkata covered advance topics like generalized Rough Sets, uncertainty Analysis and Granular Image Mining.

On March, 11, 2015, the chapter in association with Motilal Nehru College, organized a lecture on "Semiconductor Technology and MMIC development in India" by Dr. Meena Mishra, Scientist-'F' at the Solid State Physics lab., Defense Research and Development Organization (DRDO), Govt. of India. She enumerated various advancements that India has achieved in developing GaN based discrete devices.

On March 27, 2015, the chapter jointly organized the Annual Visitor's programme of Department of Electronics Science, University of Delhi. Dr. A. K. Tripathi, Scientist-'F', Ministry of New and Renewable Energy, Government of India, New Delhi gave a talk on "Renewable Energy Development in India", Dr. P. K. Chaudhary, Scientist-'H' Solid State Physical Laboratory, Delhi discussed the growth and applications of Carbon Nano Tube based Devices, Prof. Viresh Dutta, Professor and Head, Center For Energy Studies, IITD discussed gave an overview of Photovoltaic Material and Devices and Dr. Suraj P. Khanna, Principal Scientist, National Physical Laboratory, New Delhi, enlightened the audience about the Nobel Prize in Physics 2014-Blue Light Emitting Diodes.

~Manoj Saxena, Editor

Attendees of the ED Delhi Chapter event

EDS MEETINGS CALENDAR

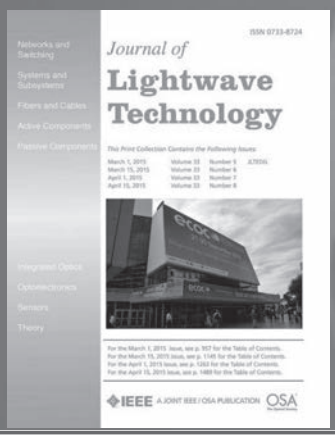
THE COMPLETE EDS CALENDAR CAN BE FOUND AT OUR WEB SITE: HTTP://EDS.IEEE.ORG. PLEASE VISIT.

2015 IEEE 22nd International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)	29 Jun - 02 Jul 2015	Lakeshore hotel No. 773, Ming Hu Road Hsinchu, Taiwan
2015 22nd International Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD)	01 Jul - 03 Jul 2015	Ryukoku University Avanti Kyoto Hall 31 Nishi Sanno-cho Higashi Kujo Minami-Ku Kyoto, Japan
2015 28th International Vacuum Nanoelectronics Conference (IVNC)	13 Jul - 17 Jul 2015	Kaifeng Hotel Sun Yat-sen University north gate, No.135, Xingang Xi Road, Haizhu District, Guangzhou, 510275, P. R. China
2015 6th Asia Symposium on Quality Electronic Design (ASQED)	03 Aug - 05 Aug 2015	Hotel Equatorial Penang Jalan Bukit Jambul 11900 Pulau Pinang Penang, Malaysia
2015 30th Symposium on Microelectronics Technology and Devices (SBMicro)	31 Aug - 04 Sep 2015	Universidade Federal da Bahia UFBA Escola Politécnica da UFBA Rua Aristides Novis 2 Federação Salvador, Brazil
2015 Joint e-Manufacturing and Design Collaboration Symposium (eMDC) & 2015 International Symposium on Semiconductor Manufacturing (ISSM)	02 Sep - 03 Sep 2015	Taipei World Trade Center Nangang Exhibition Hall Taipei, Taiwan
2015 International Workshop on Computational Electronics (IWCE)	02 Sep - 04 Sep 2015	Purdue University 610 Purdue Mall West Lafayette, IN, USA
ESSDERC 2015 - 45th European Solid-State Device Research Conference	14 Sep - 18 Sep 2015	Messe Congress Graz Betriebsgesellschaft m.b.H. Messeturm, Messeplatz 1 Graz, Austria

2015 XXth IEEE International Seminar/Workshop on Direct and Inverse Problems of Electromagnetic and Acoustic Wave Theory (DIPED) Full Paper Submission deadline: 01 Aug 2015 Final submission deadline: 20 Aug 2015 Notification of acceptance date: 15 Aug 2015	21 Sep - 24 Sep 2015	Pidstryhach Institute for Applied Problems of Mechanics and Mathematics Naukova St., 3"B" Lviv, Ukraine
2015 37th Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD)	27 Sep - 02 Oct 2015	Peppermill Resort Hotel 2707 South Virginia Street Reno, NV, USA
2015 26th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF)	05 Oct - 09 Oct 2015	Centre de Congrès Pierre Baudis 11, esplanade Compans Cafarelli Toulouse, France
2015 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)	05 Oct - 08 Oct 2015	DoubleTree by Hilton Sonoma Wine Country One DoubleTree Drive Rohnert Park, CA, USA
2015 IEEE International Integrated Reliability Workshop (IIRW) Abstract submission deadline: 12 Jul 2015 Final submission deadline: 11 Oct 2015 Notification of acceptance date: 14 Aug 2015	11 Oct - 15 Oct 2015	Stanford Sierra Conference Center 130 Fallen Leaf Road South Lake Tahoe, CA, USA
2015 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)	11 Oct - 14 Oct 2015	Sheraton New Orleans Hotel 500 Canal Street New Orleans, LA, USA
2015 International Semiconductor Conference (CAS)	12 Oct - 14 Oct 2015	Hotel Rina Sinaia Bd. Carol I, Nr 8, Sinaia, Romania
2015 15th Non-Volatile Memory Technology Symposium (NVMTS)	12 Oct - 14 Oct 2015	Tsinghua University Haidian District Beijing, China
2015 IEEE Bipolar/BiCMOS Circuits and Technology Meeting - BCTM	26 Oct - 28 Oct 2015	Hyatt Boston Harbor 101 Harborside Drive Boston, MA, USA

2015 12th International Conference on Electrical Engineering, Computing Science and Automatic Control (CCE) Full Paper Submission deadline: 20 Jul 2015 Final submission deadline: 18 Sep 2015 Notification of acceptance date: 24 Aug 2015	28 Oct - 30 Oct 2015	Centro de investigación y de Estudios Avanzados del IPN (Cinvestav) Av. Instituto Politécnico Nacional 2508 Col San Pedro Zacatenco Del. Gustavo A. Madero Mexico City, Mexico
2015 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)	09 Nov - 12 Nov 2015	CA, USA
2015 IEEE 46th Semiconductor Interface Specialists Conference (SISC)	02 Dec - 05 Dec 2015	The Key Bridge Marriott 1401 Lee Highway Arlington, VA, USA
2015 IEEE International Electron Devices Meeting (IEDM) Final submission deadline: 22 Sep 2015 Notification of acceptance date: 14 Aug 2015	07 Dec - 09 Dec 2015	Hilton Washington Washington, DC, USA
2016 IEEE International Reliability Physics Symposium (IRPS)	17 Apr - 21 Apr 2016	CA, USA
2016 IEEE International Vacuum Electronics Conference (IVEC)	26 Apr - 28 Apr 2016	Monterey Marriott 350 Calle Principal Monterey, CA, USA
2016 IEEE 43rd Photovoltaic Specialists Conference (PVSC)	05 Jun - 10 Jun 2016	Oregon Convention Center 77 NE Martin Luther King Jr. Blvd. Portland, OR, USA
2016 28th International Symposium on Power Semiconductor Devices and IC's (ISPSD)	12 Jun - 16 Jun 2016	Zofin Palace Slovanský ostrov 226 Prague, Czech Republic
2016 IEEE Symposium on VLSI Technology	14 Jun - 16 Jun 2016	Hilton Hawaiian Village 2005 Kalia Road Honolulu, HI, USA
2016 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS) Abstract submission deadline: 01 May 2016 Final submission deadline: 15 Jul 2016 Notification of acceptance date: 30 May 2016	23 Oct - 26 Oct 2016	Doubletree by Hilton Austin 6505 N IH 35 Austin, TX, USA
2016 IEEE International Electron Devices Meeting (IEDM)	01 Dec - 09 Dec 2016	Hilton San Francisco San Francisco, CA, USA

We are excited to announce the launch of the new website of the IEEE/OSA Journal of Lightwave Technology, www.ieee-jlt.org



Among other interesting information, our new website contains:

- Highly cited and frequently downloaded JLT papers
- Featured JLT Special Issues (right now featuring ECOC 2014)
- Winners of the JLT Award with free open access to the winning papers
- Recent noteworthy JLT papers
- JLT Special Issues-Browse by year or by topic area
- Call for Papers for upcoming JLT Special Issues
- Answers to frequently asked questions on such topics as JLT review times, open access publication options, and ArXiv posting
- Who is who on JLT's Editorial Board, Staff, and Steering/ Coordinating Committee

Happy Browsing!

EDS Governance Meeting Summary

(continued from page 17)

We offer our sincere thanks to Joe Zhou (EDS VP of Regions and Chapter) and Singapore chapter administrator Jasmine Leong, for their invaluable help in planning this meeting. Without their diligence, patience, and dedication, this meeting simply would not have happened. Thank you both for all of your efforts!

Lastly, we must acknowledge the generous support by the ED/CPMT/Rel Singapore Chapter, led by chair Prof. Chee Lip Gan. To all members of the Singapore chapter we extend our deepest thanks and gratitude. The Singapore chapter is a vibrant, engaged community of members and volunteers. You do the society proud!

Fernando Guarin
EDS Secretary