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Table of Contents

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Technical Briefs

Tunnel Field Effect Transistors: Past, Present and Future

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Why Tunnel FETs?

The answer to this question is linked with breakdown of Moore's law and Dennard's scaling theory. In the last two decades, MOS technology has seen a significant progress in terms of scaling down from sub-micron feature sizes to sub-10 nm dimensions. To give a quantitative feel, the gate length, gate dielectric thickness and junction depth have been reduced by about three orders of magnitude in the past 20 years, which has significantly improved the power-performance metrics. However, in recent times, the scaling pace has slowed down – for example, a 11 nm technology node doesn't have 11 nm gate length devices anymore. The minimum gate lengths are still around 20–24 nm. This is attributed to an increased S/D leakage, weak gate control and higher power consumption at very short gate lengths. To address this, power supply (V_{DD}) scaling is desired; however, to meet the ON current requirements, i.e. performance targets, the threshold voltage needs to be scaled along with VDD. However, leakage current increases exponentially as threshold voltage is reduced. Hence, threshold voltage has become a non-scalable parameter, as any decrease of threshold voltage exponentially increases the leakage current, which is mainly because of MOSFET's fundamental limit of subthreshold swing (60 mV/dec at room temperature). In reality, owing to the short channel effects, subthreshold swing (SS) is far worse than the ideal value of 60 mV/decade.

Around the same time when Dennard's scaling theory practically became difficult to implement (late 90's), a significant increase in requirement for low power technologies for wireless and handheld applications was seen. The surge in handheld consumer electronic devices like smart phones, smart watches and tablet PCs requires

(continued on page 3)

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Tunnel Field Effect Transistors

(continued from page 1)

minimization of active as well as static power dissipation by scaling down the supply voltage below 0.5 V, while maintaining acceptable performance targets. It was therefore well accepted that, in order to reduce the leakage current and scale supply voltage, it is important to explore new device structures, which can offer subthreshold swing values below 60 mV/decade. MOSFET devices, which work on the principle of thermionic injection of carriers from source to channel, do not offer enough design space and therefore limit the supply voltage scaling. To account for the future roadmap, several CMOS like devices such as the Nanowire Gate All Around (GAA) MOSFETs, FinFETs, carbon nanotube field effect transistor (CNTFET), Impact ionization FETs (I-MOSFET), and TFETs were demonstrated by various groups, in order to minimize the short channel effects (SCE) and to lower the source-drain leakage current. Among these devices, only TFET and I-MOSFET promise a SS less than 60 mV/dec and improved short channel performance, which is attributed to fundamentally a different mechanism used for carrier injection from source to channel. However, given the fact that I-MOSFET requires very high voltage operation, TFET is the only promising solution available beyond FinFET and Nanowire FETs. Tunnel FET fundamentally offers a very steep sub-threshold slope, thereby allowing threshold voltage and V_{DD} scaling beyond CMOS limits without affecting the static leakage and ON currents.

Quick Review

In last 15 years there have been extensive investigations on Tunnel FET devices for ultra-low power and high performance operation. Tunnelling phenomena allows sub-60 mV subthreshold operation thereby has a potential to scale leakage and improve ON current at lower supply voltages. The very early TFET concept of gated P-i-N diode configuration, despite several advancements like SiGe source, Low-k drain spacer, high-k source spacer, low drain doping, highly doped source, abrupt source junction profiles, post silicidation implant, band gap engineering and double gate architectures, suffered from extremely low ON currents. This was primarily attributed to limited tunnelling cross-section/area available in gated P-i-N diodes (also known as point tunnelling FETs) [1]–[9]. To overcome this problem, vertical tunnelling [10], [11]/area scaled tunnelling [12], [13] / line tunnelling [14]–[16] devices were proposed, which theoretically show significantly improved ON current, reduced leakage and subthreshold swing which can be attributed to an increased tunnelling cross section and gate-field aligned binary tunnelling mechanism [17], [18]. However, there are still open concerns related to TFET design in terms of dealing with trap assisted tunnelling (TAT) [19] and diffused junction profiles [20], which adversely affect the ON current and cause an increased leakage and SS of area scaled tunnelling or vertical tunnelling devices.

Circuit Advantages

As mentioned above, higher SS limits the supply voltage scaling, which further increases the power dissipation ($\alpha I_{OFF} \cdot V_{DD}^3$). Higher power dissipation at shorter channel lengths necessitates supply reduction, which however is limited by higher SS. To reduce the SS and thereby allow supply voltage scaling, one requires relying on carrier injection methods other than thermionic injection. A sub-thermionic injection device is expected to offer better energy performance compared to MOSFETs, as depicted in Fig. 1 [21].

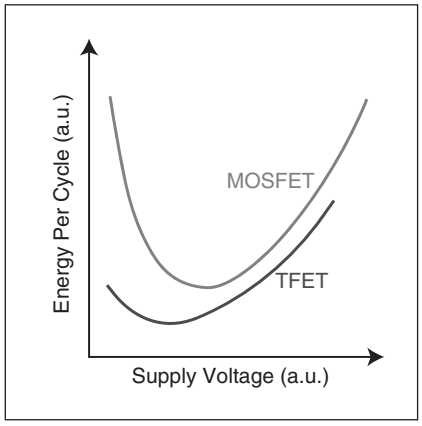

Fig. 1. Energy consumption per cycle as a function of supply voltage for MOSFET and TFET devices [21].

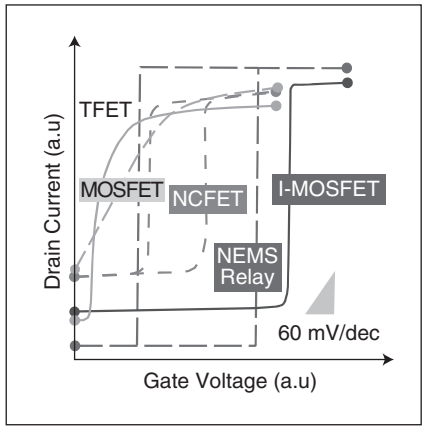

Fig. 2. Input characteristics of various switching devices [28].

Figure 2 compares the input characteristics of some of the potential candidates for sub-thermionic operation. These are NEMS switches [22], Negative capacitance FET (NCFET), Impact Ionization FET (I-MOSFET) [24] and Tunnel FET. NCFETs and I-MOSFET require a certain minimum voltage for their adequate operation and thereby do not allow supply voltage scaling beyond a certain point. Tunnel FET so far is the most promising alternative for supply voltage reduction while maintaining steep sub-threshold slope. It has potential

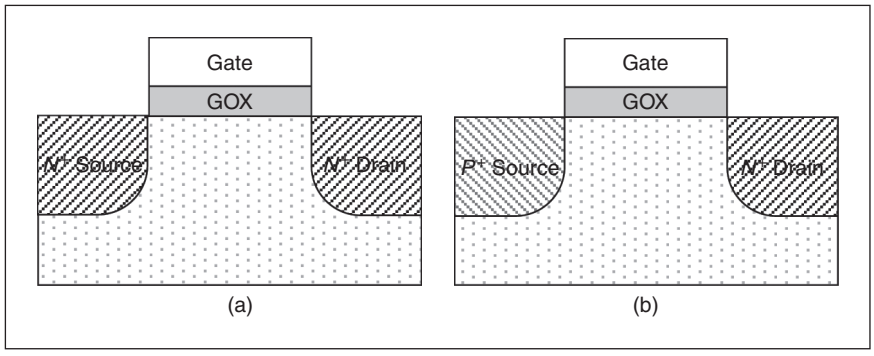

Fig. 3. Schematic view of (a) MOSFET and (b) TFET devices.

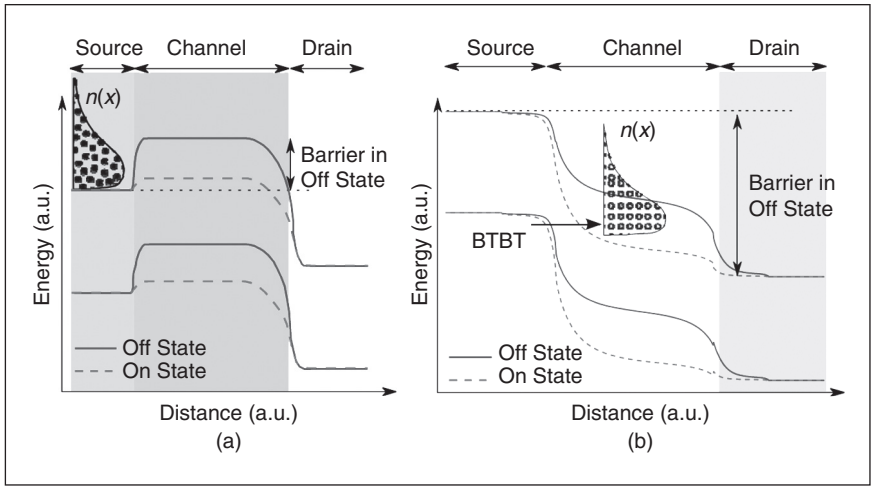

Fig. 4. Energy band diagram of (a) MOSFET and (b) TFET in ON and OFF states, depicting fundamental difference between thermionic injection mechanism and band to band tunnelling.

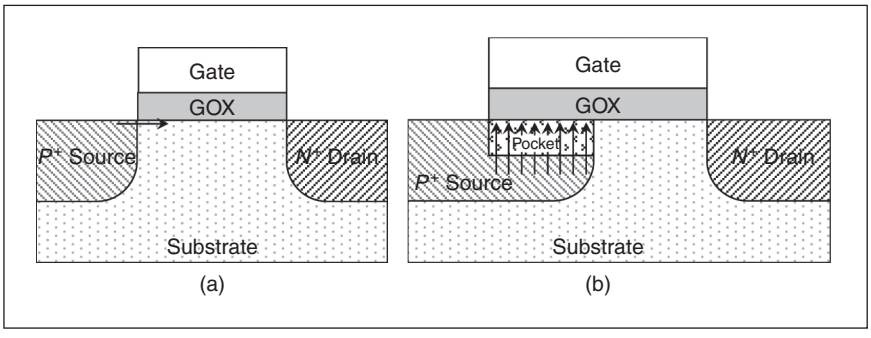

Fig. 5. Functional and structural difference (a) Line TFET and (b) Line TFET. The arrows and their density depict the tunnelling path and tunnel cross sectional area, respectively.

to offer low static leakage and adequate ON current even at lower supply voltages, which minimises power dissipation without sacrificing the performance. It also combats various short channel effects such as DIBL [30], hot carrier effects [34] even at shorter channel lengths, which makes it a potential candidate for future technology nodes.

How Tunnel FET Works?

A. Fundamental Principle: Figure 3 compares cross sectional view of a MOSFET and TFET. The only difference is in the way the source region is engineered, which in fact defines the carrier injection from source to channel. In principle a TFET is a gated p-i-n diode which behaves like a tunnel diode in ON state and like a reverse bias P-i-N diode under OFF state. Asymmetry in the structure and tunnel injection of carriers allows very high I_{ON}/I_{OFF}; however, it restricts the source-drain exchange, which works well in case of MOSFET.

Figure 4 compares the operational difference between Tunnel FET and MOSFET. In case of MOSFET, carriers are injected thermionically over the barrier, whereas in case of TFET they are injected from source to channel due to gate field induced band to band tunnelling (BTBT). In the OFF state, alignment between the conduction band of the channel and the valence band of the source is missing, which avoids carrier tunnelling and maintains a very low leakage current. However, in the ON state, when the gate field is present, the channel region's conduction band is pulled down, which allows it to align with the source region's valance band. This alignment reduces the tunnelling barrier width and height, which allows carrier injection/tunnelling from source to channel region. This enables a sharp turn-on when the bands are aligned, and therefore allows TFET devices to operate well below the sub-thermionic limits with sub-threshold swing values below 60 mV/dec. Under OFF state condition, TFET has comparatively higher barrier for the minority carriers, which leads to negligible leakage current due to minority carrier injection. In fact whatever leakage current exists in TFET is mostly dominated by SRH recombination and trap assisted tunnelling (TAT) [25] at the source-channel junction, which however, are well below leakage in MOSFET devices at shorter channel lengths.

B. Point TFET versus Area Scaled TFET: Despite its ability to combat short channel effects, enable voltage scaling and minimise leakage, the conventional/gated P-i-N TFET architectures suffer from their low ON current. In recent literature, this device is frequently referred as point TFET (Fig. 5a). ON current of TFET is directly proportional to the tunnelling

probability (T_{BTBT}) and tunnelling cross-section. The expression for the tunnelling probability obtained by approximating the tunnel barrier by a triangular barrier, as shown in Figure 6, and using WKB approximation is given by [35]:

$$T_{BTBT} = \exp\left(-\frac{4\lambda\sqrt{2m^* E_g^3}}{3qh\left(E_g + \Delta\Phi\right)}\right)$$
$$\approx \exp\left(-\frac{4\sqrt{2m^* E_g^3}}{3qhF}\right)$$

Where m^* is the effective tunnelling mass, E_g is the bandgap of the material, F is the electric field and λ is the tunnelling distance. For point TFET, the only parameter which one can engineer is to use the low bandgap material with low tunnelling effective mass. This improves the tunnelling probability and improves the ON current; which however is at the cost of increased SRH leakage. To keep the SRH leakage under control, use of low bandgap material only at the tunnel junction is a technique which is implemented widely. Except at the tunnelling junction (low bandgap source region for N-type device and low bandgap channel region for P-type device), rest of the device uses a relatively higher bandgap material, which is also known as hetero-junction TFET. Other methods which were proposed to improve point TFET's performance were use of Low-k drain spacer, high-k source spacer, low drain doping, highly doped source, abrupt source junction profiles, post silicidation implant, and double gate architectures. However, they all suffer from extremely low ON currents, which is attributed to limited tunnel area available. This issue was addressed by increasing tunnelling cross section area, by introducing vertical tunnelling [10], [11] in the direction of gate field [17], [18] by incorporating a N-type pocket sandwiched between gate stack and P+ source (Fig. 5b). This concept is also known as area scaled tunnelling [12], [13] or line tunnelling [14]–[16], which significantly improves the ON current, subthreshold slope and gate control over the tunnelling junction.

Pocket layer design and source engineering plays a very important role in line TFET's performance. The design parameters are source and pocket layer's doping and bandgap, as well as pocket region's thickness [12]. One can say that the pocket engineering leverages additional control to design device for a range of applications. It is worth mentioning that line TFET architecture is CMOS compatible and easy to integrate using standard CMOS unit process steps [13].

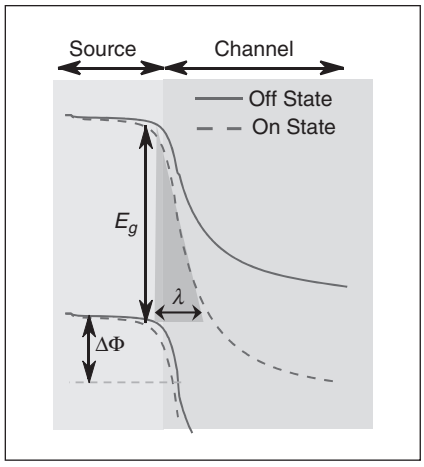

Fig. 6. Energy band bending, tunnelling barrier height and tunnelling distance at the source-channel junction under ON and OFF states of the device.

TFET Future Beyond FinFET: Fin Enabled Area Scaled TFET

It took almost 20 years for FinFET technology to mature and become a reality for semiconductor products by replacing planar devices. However, as technology evolution doesn't allow abrupt changes, FinFETs too enjoy advancements from planar nodes like High-k metal gate, raised/epi source-drain, strained silicon and gate last process. It is widely accepted that Si or SiGe FinFET can be replaced by TFETs, but what was not so clear was whether there will be a serious change in technological evolution while scaling below 7 nm nodes. In other words how to take TFET concept to Fin-based technologies, allowing smooth transition from FinFET technology to Fin-based vertical Tunnel FETs, while enjoying benefits of FinFET architecture.

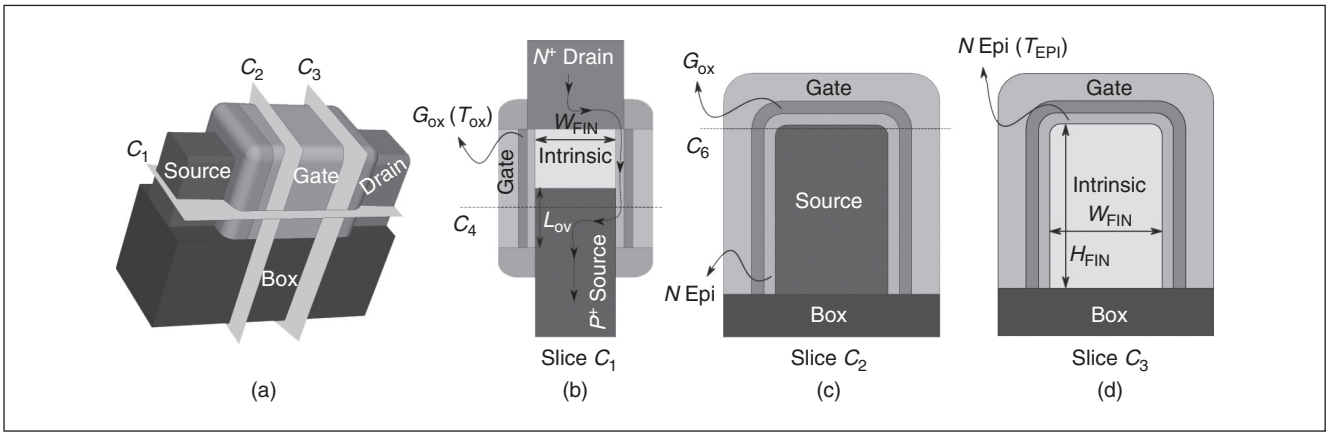

Fig. 7. Fin Enabled Area Scaled Tunnel FET along with different slices and the operation of the device. (a) 3D view of the device; (b) 2D slice along C_1 depicting paths followed by the carrier from source to drain; (c) & (d) 2D views along the slices C_2 and C_3.

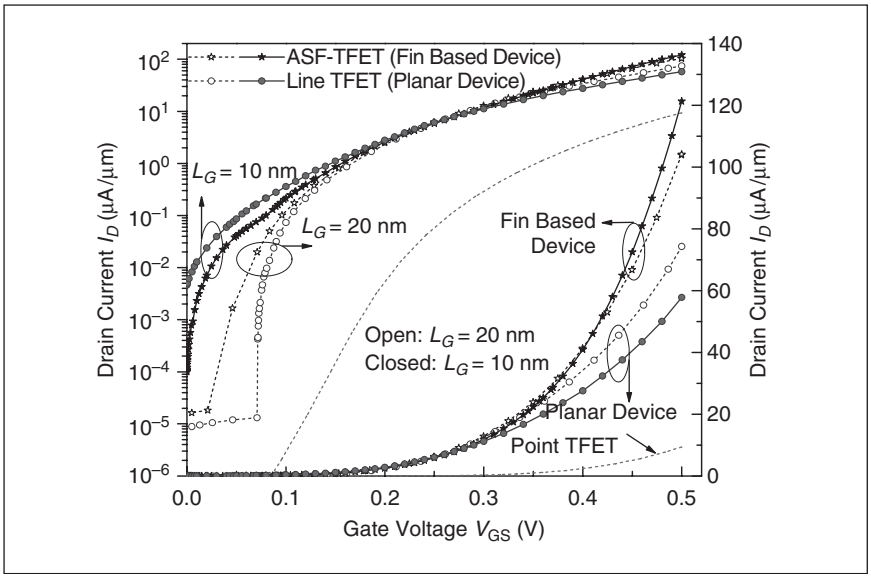

Fig. 8. Input characteristics Point TFET, Line TFET and ASF-TFET [25].

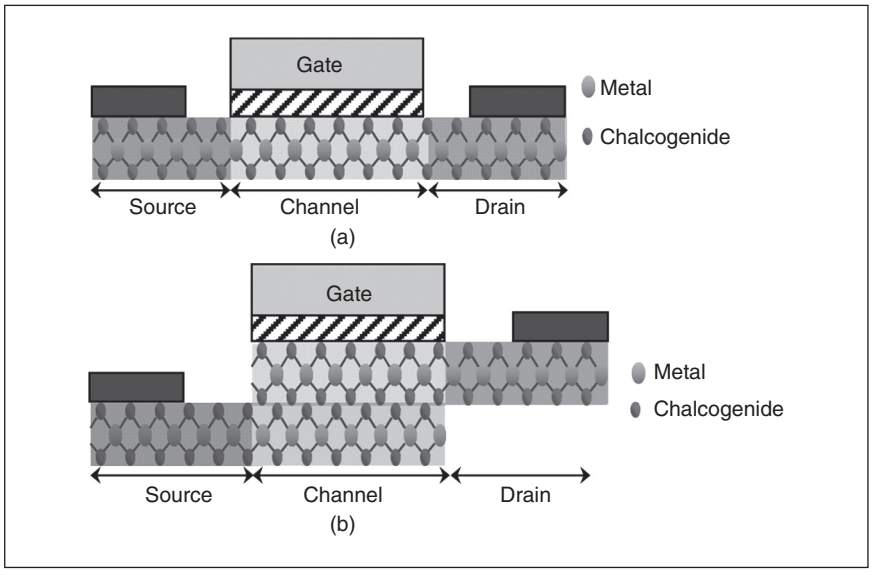

Fig. 9. Schematic of TMDC based (a) point TFET and (b) Line TFET.

To address this, a Fin Enable Area Scaled Tunnel FET namely ASF-TFET was recently proposed [25], as depicted in Fig. 7. The working principle of this device is same as line TFETs, however the device enjoys excellent gate control over the channel as well as the tunnel junction, which improves the performance significantly [36], as depicted in Fig. 8. According to simulated results, ASF-TFET at 10 nm gate length, when compared to the conventional vertical tunnelling FET or planar area scaled device, offers 100% improvement in ON current, 15× reduction in OFF current, 3× increase in the transconductance, 30% improvement in output resistance, 55% improvement in the unity gain frequency and more importantly 6× reduction in the footprint area for a given drive capability. Furthermore, the proposed device brings the average and minimum sub-threshold swing (SS) down to 40 mV/dec and 11 mV/dec at 10 nm gate length. This gives a path for beyond FinFET System on Chip (SoC) applications while enjoying analog, digital and RF performance improvements [25].

TFET Beyond Conventional Semiconductors: 2D Material Based Hetero-Structure TFET

In recent years 2D materials like Graphene, Hexagonal Boron Nitride (h-BN) and Transition metal dichalcogenides (TMDC) have seen extensive investigations for electronics applications. These investigations revealed greater potential of 2D materials for low power SoC products, which is attributed to (i) their extraordinary channel properties, (ii) atomically thin channel, which allows excellent gate control and hence scalability beyond Si limits and (iii) flexible nature of 2D materials which allows integration over flexible substrates [26]–[29]. Moreover, the 2D material surfaces are extremely flat and free of defects, which potentially offer improved device reliability [19]–[20]. Like conventional semiconductors, various groups have been exploring TFET possibilities using 2D materials as well (Fig. 9) [30]–[33]. Initial results depict a great potential of TMDC based tunnel FET, which is attributed to excellent gate control over the tunnel junction, scalability, broken gap TFET architecture and absence of TAT leakage; however, the technology still has a long road ahead, as far as meeting the semiconductor industry roadmap targets is concerned.

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Prof. Shrivastava had held short term visiting positions in Infineon Technologies, Munich, Germany from April 2008 to October 2008 and again in May 2010 to July 2010. He worked for Infineon Technologies, East Fishkill, NY; Intel Mobile Communications, Hopewell Junction, NY; and Intel Corp., Mobile and Communications Group, Munich, Germany between 2010 and 2013. He joined Indian Institute of Science as an Assistant professor in year 2013 where he has established *Advance Nanoelectronic Device and Circuit Research Group*.

To get more information about Prof. Shrivastava's current research interests, publications and patents visit: http://www.dese.iisc.ernet.in/people/mayank/.

V. Ramgopal Rao was a P. K. Kelkar Chair Professor for Nanotechnology in the Department of Electrical Engineering and the Chief Investigator for the Centre of Excellence in Nanoelectronics project at IIT Bombay. He is currently on lien from IIT Bombay to serve as a Director at IIT Delhi. Dr. Rao has over 400 publications in the area of Electron Devices &Nanoelectronics in refereed international journals and conference proceedings and is an inventor on 32 patents (including 13 issued US patents) and patent applications, with many of his patents licensed to industries for commercialization. He is also a co-founder of the company NanoSniff Technologies Pvt. Ltd. at IIT Bombay which is developing products in the area of Nanotechnology.

Prof. Rao's work is recognized with many awards and honors in the country and abroad. He is a recipient of the Shanti Swarup Bhatnagar Prize in Engineering Sciences in 2005 and the Infosys Prize in 2013. Dr. Rao also received the Swarnajayanti Fellowship award from the Department of Science & Technology, IBM Faculty award, Best Research award from the Intel Asia Academic Forum, Techno-Mentor award from the Indian Semiconductor Association, DAE-SRC Outstanding Research Investigator award, NASI-Reliance Platinum Jubilee award, J.C.Bose National Fellowship, Prof. C.N.R.Rao National Nanoscience award and the Excellence in Research Award from IIT Bombay. Prof. Rao was an Editor for the IEEE Transactions on Electron Devices during 2003–2012 for the CMOS Devices and Technology area and currently serves on the Editorial boards of various other international journals. Dr. Rao is a Fellow of the Indian National Academy of Engineering, Indian Academy of Sciences, National Academy of Sciences, and the Indian National Science Academy. He is a Distinguished Lecturer, IEEE Electron Devices Society and interacts closely with many semiconductor industries including Intel, IBM, Infineon, Applied Materials, Maxim and Texas Instruments.

Dr. Rao served as a Chairman, IEEE AP/ED Bombay Chapter and is currently the Vice-President, Materials Research Society of India. He also served as a Vice-Chairman, IEEE Asia Pacific Regions/Chapters sub-committee during 2007–2013 and was the first elected Chairman for the India section, American Nano Society during 2013–2015.

For more information about Prof. Rao's current research interests and a list of publications visit: http://www.ee.iitb.ac.in/~rrao/

Upcoming Technical Meetings

2016 IEEE International Integrated Reliability Workshop (IIRW)

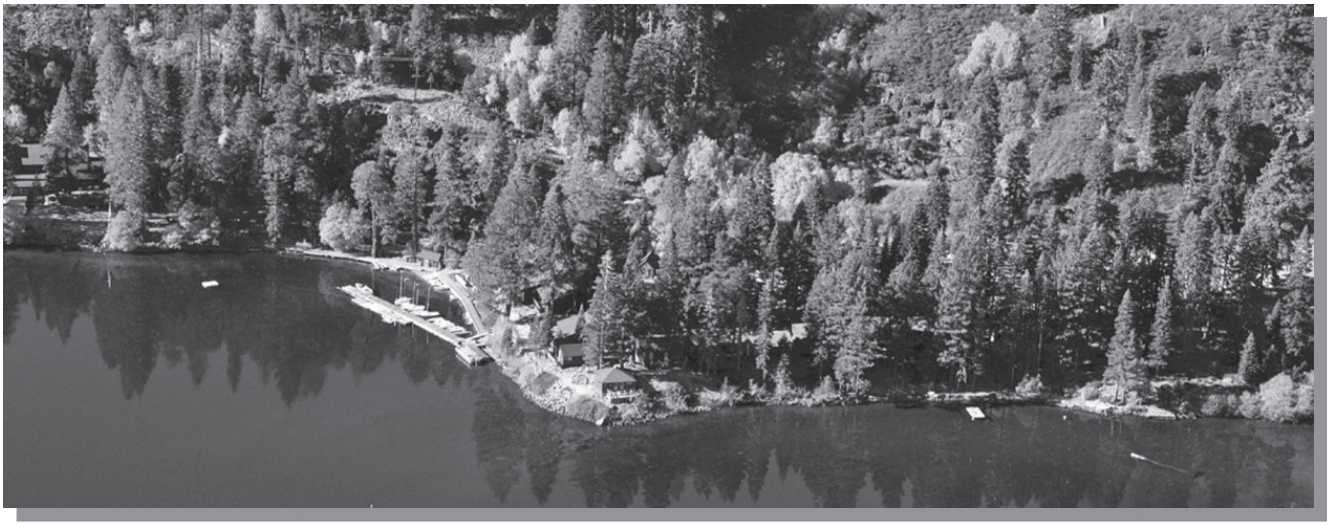
The 2016 IEEE International Integrated Reliability Workshop (IIRW), sponsored by the IEEE Reliability Society and the IEEE Electron Devices Society, will be held at the Stanford Sierra Conference Center on the shores of Fallen Leaf Lake near South Lake Tahoe, California, October 9–13, 2016. This workshop provides a unique forum for open, lively discussions of all areas of reliability research and technology for present and future semiconductor applications.

Reliability topics for the workshop include: SiGe and strained Si, III–V, SOI, high-k and nitrided SiO_2 gate dielectrics, reliability assessment of novel devices, Power devices reliability (SiC, GaN), organic electronics, emerging memory technologies (RRAM etc.) and future "nano"-technologies, NEMS/MEMS, photovoltaics, transistor reliability including hot carriers and NBTI/PBTI, Cu interconnects and low-k dielectrics, product reliability and burn-in strategy, impact of transistor degradation on circuit reliability, reliability modeling and simulation, optoelectronics, single event upsets, array testing as well as the traditional topics of wafer level reliability (WLR) and building-in reliability (BIR). Special focus this year will be on MEMS and other sensor reliability, atomic and molecular scale modeling for reliability, and advanced characterization techniques for reliability studies.

The Call for Papers can be found at www.iirw.org. Please submit abstracts though www.iirw.org. The submission deadline is July 11, 2016. Contact the Technical Program Chair, Tom Kopley (tpc.iirw2016@gmail.com) for any further questions or visit www.iirw.org for continued updates about the conference.

IIRW is quite different from a typical technical conference. Located 6400 feet above sea level in the California Sierra Nevada, the Stanford Sierra Conference Center provides an ideal atmosphere for a relaxing yet informative workshop. All aspects of the workshop, including the physical isolation of the location, the absence of distractions such as in-room phone/television, and the format of the technical program, encourages extensive interaction among the workshop attendees. You feel yourself drawn into technical discussions from the start.

Attendees lodge in cabins nestled throughout the pines and cedars along the shoreline of Fallen Leaf Lake. All rooms have decks with magnificent views of Fallen Leaf Lake and the surrounding Sierra peaks. Comfortable, informal dress is encouraged, affiliations are downplayed, and meals are provided family-style in the lodge dining room. This peaceful setting presents a terrific opportunity to get to know your colleagues, including internationally renowned experts. Such opportunity is seldom available at larger conferences. Participants spend their evenings at poster sessions, discussion groups, and special interest groups, all complemented with refreshments and snacks. At the end of the day, attendees are free to relax in front of a roaring fireplace in the rustic Old Lodge.



Aerial view of the Stanford Sierra Conference Center – The Center provides lodging, meals and meeting facilities as well as excellent recreational opportunities, including hiking in the Desolation Wilderness and boating on Fallen Leaf Lake

The conference traditionally begins Sunday evening after the majority of attendees arrive. The single Sunday night talk includes refreshments, and is designed for the weary traveler, being a technically toned-down presentation on an interesting topic either peripherally related to reliability, or simply an interesting hobby or business from one of the attendees. This year we are delighted to announce this Sunday night talk will be on the applications of sensor fusion for motion tracking by Per Slyke, VP of Fairchild's Motion Tracking product line.

Invited speakers at this year's IIRW will include Roya Maboudian (UC Berkeley) on MEMS reliability, Stuart Friedman (PrimeNano) on scanning microwave impedance microscopy, Ashraf Alam (Purdue U.) on polymer dielectric reliability, Don Gajewski (Wolfspeed, CREE) on SiC reliability, Gaudenzio Meneghesso (U. Padova) on GaN reliability, and Kevin Huang (TSMC) on AC stress for standard cell aging characterization, among several others.

Another advantage of attending IIRW is the extensive collection of tutorials, presented by leading experts and included at no additional cost. This year the tutorials cover diverse reliability topics such as BEOL reliability (Patrick Justison, Globalfoundries), SiC power device reliability (Kevin Matocha, Monolith Semi), MEMS reliability (Allyson Hartzell, |Veryst), and DFT defect modeling in SiO_2 and HfO_2 dielectrics (Al-Moatasem El-Sayed, UCL). Please check the IIRW website for updates on tutorial presenters.

One other advantage of IIRW is the moderated discussion groups that are held in the evenings. Following up on the discussion groups are the Special Interest Groups, which are composed of small groups of attendees who want to continue their discussions on a particular topic of interest, which often continue even after the workshop.

One unique aspect of the workshop is the opportunity for any attendee to present a walk-in poster of their latest work. Finally, attendees have Wednesday afternoon off to enjoy a variety of outdoor activities such as hiking, volleyball, sailing or kayaking, biking, walking, or simply continuing that intriguing conversation from the night before. This free afternoon is a great way to not only network, but also to build long-lasting friendships.

Additional information about the workshop is available on the IIRW website at www.iirw.org, or by contacting Richard G. Southwick, III, 2016 IIRW General Chair, (southwick@us.ibm.com). Information on the Stanford Camp is available at stanfordsierra.com. Note: If you want to take part in this event, please register early as space at the Stanford Sierra Conference Center is limited to roughly 120 attendees and the workshop has sold out in the past.

On behalf of the 2016 IIRW Management Committee, I look forward to meeting you in Lake Tahoe!

Zakariae Chbili
2016 IIRW Communications Chair
GLOBALFOUNDRIES, Inc.
Malta, NY, USA

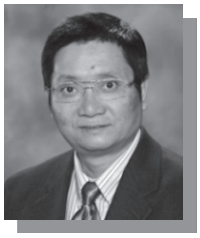
2016 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)

Short Course: September 25, 2016; Conference: September 26–27, 2016

On behalf of the IEEE BCTM'16 Executive Committee, we are honored and delighted to invite you to the 2016 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) at the beautiful Hyatt Regency, New Brunswick, New Jersey, USA, from September 25th–27th. We invite you to participate at the 2016 BCTM where the highlights include:

- Day-long short-course on **Advances in Design Enablement for RF and High Performance Analog Circuit Design**
  - Dr. Sharad Kapur (Integrand Software): Advanced EM Simulation
  - Art Schaldenbrand (Cadence): Developments in EDA tools for analog design
  - Dr. Ali Niknejad (UC Berkeley): Modeling of Passives at High Frequencies
  - Dr. Shahriar Shahramian (Bell Labs): Circuit design point of view on EM Simulation, EDA tools, and modeling
- Invited papers exploring advances in analog/mixed-signal design, device physics, modeling and simulation, process technology, and wireless design
- Technical papers covering the latest advances in physics, design, performance, fabrication, characterization, modeling, and application of Si/SiGe/SiC bipolar, BiCMOS, and GaN ICs
- Evening dinner banquet

Doug Weiser



Foster Dai

The IEEE BCTM is a forum for technical communication focused on the needs and interests of the bipolar and BiCMOS community. Papers covering the design, modeling, performance, fabrication, testing and application of bipolar and BiCMOS integrated circuits and devices as well as high-performance circuits using other competitive technologies such as CMOS, SiC, GaN, GaAs, and InP are solicited. Best Paper Awards will be given to the top regular and student papers. A Special Section of the IEEE Journal of Solid-State Circuits will include selected papers from BCTM 2016.

General Contact Information

Visit the conference website: www.ieee-bctm.org or contact: Catherine Shaw, Conference Manager, Phone 1-732-501-3334, E-mail: cshaw.cmpevents@gmail.com

The IEEE BCTM is the world's premier forum focused on the needs and interests of the bipolar and BiCMOS community. If you are interested in leading edge bipolar/BiCMOS devices and technology, circuits, and applications, as well as networking with experts in these areas, please kindly join us this year at the beautiful Hyatt Regency, New Brunswick, New Jersey, USA!

Foster Dai
2016 BCTM Technical Program Chair
University of Auburn

Doug Weiser
2016 BCTM General Chair
Texas Instruments

Society News

Message from EDS President

Samar K. Saha
EDS President
2016–2017

Dear Fellow EDS Members:

At the onset of assuming the duties as 2016–2017 President of IEEE Electron Devices Society (EDS), in my first message in January, I stated to *continue building* EDS *on the excellent foundation of the past to meet the challenges of the future*. Accordingly, the plans to continue ongoing activities and executions and define the future directions of our Society along with suitable outreach programs were outlined. A gist of the progress made so far in the initiated programs is in this message.

However, before summarizing the initiated EDS programs, I am happy to inform all our members that James Skowrenski joined the EDS office as the Operations Director. Jim is highly experienced and knowledgeable in working with membership-based organizations. His experience with the American Diabetes and American Medical Associations will bring new perspective in our society's day-to-day operations. In addition, he has a strong background in institutional publishing including executive roles with Nature Publishing and Macmillan Magazines Ltd. Jim, also managed a consulting business focusing on both association marketing and membership. Please join me in welcoming Jim to the EDS staff.

In an effort to grow and retain EDS membership, we have started implementing different strategies through EDS Membership Fee Subsidy Program and various activities of Regions and Chapters Committees. About 600 new members have joined the EDS during the first 4 months of this year through these efforts. The details of these strategies as well as the number growth process of EDS membership will be reported in the Board-of-Governors (BoG) meetings and later in issues of this Newsletter.

Our flagship publications, the *IEEE Transactions on Electron Devices* (T-ED) and *IEEE Electron Device Letters* (EDL) are of world class by themselves and are in good shape under the new Editor-in-Chiefs (EiC) of each journal. In order to establish our worldwide leading position in Open Access (OA) publications through the *IEEE Journal of Electron Devices Society* (J-EDS), we are in the process of implementing several initiatives to increase the number of manuscript submission. I am also happy to inform that we have successfully completed the J-EDS Editor-in Chief (EiC) search process by the (EiC) search committee ensuing the (EiC) *Selection Procedure.* Professor Mikael Östling of KTH Royal Institute of Technology Sweden has been selected and appointed as the second (EiC) of the three-year old infant, J-EDS. For the healthy growth of J-EDS to maturity, we are in the process of initiating plans to integrate J-EDS in the publication loop of EDS's flagship conferences for publishing selected high-impact extended conference papers.

Besides sustaining our existing flagship conferences, we need to *expand our worldwide leading position* with respect to device and technology conferences to the geographical regions with major activities on device and technology. In this endeavour, the inaugural conference of the newly proposed EDS's Electron Devices Technology and Manufacturing (EDTM) is scheduled at Toyama International Conference Center, Toyama, Japan on February 28 to March 2, 2017. EDTM is the resultant of a concerted effort by a dedicated team of volunteers led by Shu Ikeda as the Chair of EDTM Executive Committee. EDTM is structured to be a unique EDS's flagship conference in Asia that is intimately integrated to EDS Executive and Technical Committees along with publication process tied to the J-EDS.

With more than 190 EDS Chapters around the globe distributed in all the 10 Regions serving the members and constantly engaging with academia and industry, our target is to penetrate the young, especially students, through more active EDS student Chapters. It is extremely critical to plan the growth and development of EDS *Student Chapters* in academic institutions with existing IEEE chapters only. We are also pursuing the service to the community through joining in the IEEE *Special Interest Group in Humanitarian Technology (SIGHT)* program and promoting it through our EDS Chapters.

We are continuing our stellar educational programs including Masters Student and PhD Student Fellowships, Distinguished Lectures (DLs), Mini-Colloquia (MQ), Webinars, and so on. I am pleased to report that through April 2016, we organized two EDS Webinars of total six planned in 2016.

We have initiated reaching out to other IEEE Organizational Units (OUs) with common interest for bilateral collaboration of mutually beneficial programs as well as to outreach youth. In continuing effort

to outreach to youth, EDS hosted a student event at the 43rd Photovoltaic Specialists Conference (PVSC), June 5–10, 2016, in Portland.

The first open session to discuss EDS's strategy on *Future Direction* program is slated in 2016 mid-year BoG meeting at Grenoble, France.

In summary, some of the programs initiated and outlined in my earlier message in the January 2016 issue of the Newsletter is shaping its results. Details will be informed through future issues of this Newsletter.

Samar K. Saha
EDS President
Prospicient Devices
Milpitas, CA, USA

Message from EDS Vice President of Membership and Services

Tian-Ling Ren
EDS Vice President of Membership and Services

I am extremely honored and pleased to work as the new EDS Vice President of Membership and Services. EDS is one of the best societies of IEEE and members' benefits are always our primary concerns. EDS has a steady member count of over 10,000 members. The member count was kept constant while some other societies had an obvious decline in membership. Although the result is encouraging, we still need to do better to attract more members.

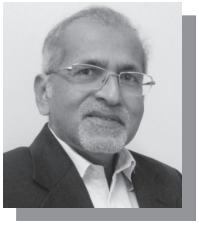
During the EDS Board of Governors Meeting (BoG) in 2015, we had an interesting discussion about how to increase the member benefits. Some of the conclusions were to continue to focus on young professionals and affiliate members, focus on on-line membership and improve the way we promote the Society at events such as EDS Distinguished Lectures (DLs) and Mini-Colloquium (MQ). We will also continue the focus on webinar offerings, which deliver live lectures with luminaries from the field of electron device engineering.

Most importantly, the success of EDS depends on you, our valuable members. Please get in touch and tell us your ideas on what you expect and want to see. You are all invited to share your ideas. You can preferably do this by e-mail to Joyce Lombardini, who is the EDS Membership Administrator, e-mail: j.lombardini@ieee.org

Sincerely yours,

Tian-Ling Ren
EDS Vice President of Membership and Services
Tsinghua University
Beijing, China

Message from Editor-in-Chief



M. K. Radhakrishnan
Editor-in-Chief

Dear EDS Members and Readers,

I hope you enjoy reading the information featured in this issue of the newsletter, such as the technical article discussing the research studies and the development which led to Tunnel FET (TFET) devices. TFETs could provide solutions for one of the greatest challenges in device technology through ultra-low power consumption during transistor switching. After a series of articles on reliability trends in devices, now we are moving towards new developments in device technology. Such technical articles by experts which are so digestible to any reader is published for the benefit of all the members and readers of this Newsletter and we welcome your views and comments about them.

A summary of the deliberations at the mid-year meeting of the EDS Board of Governors held at Grenoble, France on May 29, 2016, is included in the Society News Section. Also, the announcement of various EDS awards is given in the section.

Our Regional Editors Adam Convey (Regions 5 & 6) and Mansun Chan (Region 10 – East Asia) served their terms very successfully, engaging the Chapters and activities in their respective Regions. On behalf of all our readers and the EDS Newsletter team, I would like to express our sincere gratitude to both of them. Thank you, Adam and Mansun.

Two new members have joined our Editorial team. Kyle Montgomery from Air Force Research Laboratory, Albuquerque, as the Regional Editor for Regions 5 & 6 and Ming Liu from Institute of Microelectronics, Chinese Academy of Science as Regional Editor for East Asia of Region

10. It is my pleasure to welcome both of them to our team as New Editors.

Kyle Montgomery is a Research Engineer with the Air Force Research Laboratory (AFRL) in Albuquerque, New Mexico, USA. In addition, he holds a Research Assistant Professor title at the University of New Mexico in the Electrical & Computer Engineering department, where he teaches a graduate course on solar cells. Dr. Montgomery's research interests (PhD, Purdue University, 2012) focus on high efficiency solar cells and power systems for space applications. He serves on the EDS Young Professionals Committee and the planning committee of the IEEE Photovoltaic Specialists Conference (PVSC).

Ming Liu is a Professor at the Institute of Microelectronics, Chinese Academy of Sciences and Director of the Key Laboratory of Microelectronics Devices & Integrated Technology. She received her Ph.D. in Material Engineering from Beijing University of Aeronautics and Astronauts, China in 1998 and later joined the Institute of Microelectronics, Chinese Academy of Sciences and became professor in 2000. Her current research areas include micro/nanofabrication, new structure NVM device and circuit, modeling and simulation, reliability and organic electronic devices.

M. K. Radhakrishnan
Editor-in-Chief, EDS Newsletter
e-mail: radhakrishnan@ieee.org

EDS Board of Governors Meeting Highlights

Simon Deleonibus
EDS Secretary

May 28–29, 2016: The EDS Mid-Year Governance Meeting returned to Region 8 this year in grand style, bringing together the Society's senior leadership and several EDS Chapter Chairs from across Region 8 to beautiful Grenoble, France. The meeting was a phenomenal success, combining vital society business with some truly special social events to create an enriching and energizing event for all attendees. The weekend began on Saturday morning, with a series of important Standing Committees meetings.

EDS Forum members during dinner at Restaurant du Teleferique in Grenoble (450m above sea level) – May 29, 2016

The EDS BoG meetings started with the introduction of new EDS Operations Director, James Skowrenski, who joined the EDS team with extensive experience in association management. The first day's meetings included Fellows Evaluations, Publications and Newsletter Joint meeting, Technical Committees meeting and Education, Membership and Chapters meeting.

The Fellows Evaluation Committee began their work bright and early Saturday morning, with the difficult task of reviewing and evaluating 42 IEEE Fellow nominations. Led by Paul Yu, the committee did the evaluations of all nominations and endorsements for many hours, proving once again that the work of this committee is among the most challenging and important to the Society and the IEEE.

As the EiC of Newsletter, M. K. Radhakrishnan presented the status and the improvements made in the newsletter during the last 3 years. The increased emphasis on technical content, introduction of columns for YPs and introduction of Messages from Presidents in each issue were highlighted. The transition to web format and open access for Newsletter received positive reviews.

Hisayo Momose, EDS VP of Publications and Products, chaired the critical Publications committee meeting. The new editor for J-EDS was

announced as Mikael Ostling and the strategy for the management of the EDS publication portfolio was shared.

Led by EDS's VP of Technical Committees and Meetings, Ravi Todi reviewed our many technical meetings and conferences. The discussions also included the newly approved Electron Devices Technology and Manufacturing Conference, which will be held on February 28 to March 2, 2017 in Japan.

Combining the Membership, Chapters and Education meetings has proved very effective. Vice Presidents Tian-Ling Ren (Membership), M. K. Radhakrishnan (Regions and Chapters) and Mansun Chan (Education Chair), convened an outstanding forum to address these important areas of the society's life. In addition to providing an important strategic planning session, the highlight of the meeting was the open dialogue with all present. This meeting was followed by Region 8 Chapters meeting chaired by Region 8 SRC Chair Simon Deleonibus in which several EDS chapter chairs from across Region 8 participated. The meeting provided an excellent opportunity for staff and volunteer leadership to learn more about the chapters' perspectives, needs, and successes. This meeting continued with the Region 8 Chapters meeting

The EDS Forum and Board of Governors met on Sunday, May 30th for the Mid-Year Governance meeting chaired by the President Samar Saha. The meeting's discussions covered nearly every aspect of the society's operations, ending with an extended Open-Forum to provide a free exchange of ideas and debate over how we can continue to improve the Society to ensure its preeminence as the world's leading organization devoted to device engineering. Here are some of the highlights:

- EDS Treasurer, Subramanian Iyer, reviewed the financial state of EDS and the news is good! Publication page counts and prices for 2017 have been approved. Also, EDS membership dues will remain the same at $18 for 2017.
- EDS has endorsed the collaboration with the CMPT society and SEMI in sponsoring the heterogeneous integration roadmap with the goal of collaboration with other IEEE societies and other organizations.
- An updated EDS field of interest has been approved and will be sent to IEEE for formal approval.
- It has been noted that EDS member strength is almost stagnant and the student member strength is very low compared to the student Chapters.
- A good number of Chapters are found to be shy in communicating activities and reports. Regions and Chapters committee is empowered to revitalize weak Chapters. A concerted effort to improve and monitor student Chapters is planned.
- For the EDS Region 9 Outstanding Student Paper Award a minor modification to the eligibility requirements is made by allowing a nominee to be enrolled at a higher education institution located in Region 9 at the time of the paper publication date.
- A motion was made and passed to create an EDS Documents Review Ad Hoc Committee to review the inconsistencies of the EDS Constitution and Bylaws, along with other documents.

We offer our sincere thanks to Mireille Mouis and Marco Pala for their invaluable help in planning this meeting. Without their diligence, patience, and dedication, this meeting simply would not have happened.

Simon Deleonibus
EDS Secretary

EDS Region 8 Meeting

The EDS Region 8 Meeting was held during the BoG/Forum meetings series in Grenoble on the afternoon of May 29th. The meeting gathered 30+ attendees from all regions and mainly Region 8 Chapters Chairs and Representatives (11). For the meeting preparation, all Region 8 Chapters Chairs were requested by Region 8 SRC Chair, Simon Deleonibus, to send 3 highlights from their Chapter's recent activities. After introductory remarks and data presentations by both M. K. Radhakrishnan, EDS Vice President of Regions and Chapters and Simon Deleonibus, the Chapters Chairs and Representatives were invited to comment directly on their highlights tables.

An intensive debate occured during the discussion on the following points:

- Region 8 is the widest region for IEEE and includes 1,619 members, 52 chapters, among which 13 are 100% EDS, 31 are Joint Chapters and 8 Students Chapters. It has the largest proportion of Joint Chapters among all regions, mainly due to the fact that diversification is widely spread in the industry activities.
- The formal reporting of our Chapters to the IEEE EDS headquarters was analyzed and commented through the use of a common metrics. The available data include L31 forms, MQ and DL deliveries, and EDS Newsletter reporting. As a matter of fact, the number of L31 forms generated by the Chapters is not a direct measure of Chapters' activities because these forms are used for

different purposes by different Chapters. The number of these forms ranges from 0 to 132 in a year (2015) in different Chapters! For no reason, these forms have to be used for internal reporting! Region 8 has at least 6 «dormants/shy Chapters» (3 Chapters are 100% EDS), which for unknown reasons have not reported for the last 3 years. This number has to be corrected and we should know why.

- The activity of Region 8 SRC (Chair Simon Deleonibus; Vice-Chairs Tomislav Suligoj, Arokia Nathan and Andrzej Napieralski) was reported. Region 8 SRC has prioritized since 2015 to revitalize «dormant/ shy» chapters (2 were reactivated last year and 6 are in revitalization process in 2016), increase the number of chapters (2 were created in 2015 and 2 are in process), strengthen the network by visits to the Chapters (2 in 2015). New opportunities for chapters creation (at least 3) are analyzed and being considered.
- A discussion was carried out on the opportunity to create new chapters from larger ones. This is not a simple question, because local conditions in each country need to be considered. For example, in some countries, maintaining or defining one/several chapters could be critical because members may be spread all over the country or concentrated in a specific area. Finally, do we need more chapters or more members? Which is the optimal number to set up a Chapter? All these questions have to be addressed properly on a case-by-case basis.
- The detailed highlights tables of different chapters and their slides presented at the meeting have been disseminated to all Chapters Chairs.

Society officers and chapter chairs who attended the EDS Region 8 Meeting in Grenoble, France

Simon Deleonibus
Region 8 SRC Chair
CEA/LETI, MINATEC
Grenoble, France

Awards and Recognitions

2016 William R. Cherry Award Winner


Dr. Pierre Verlinden

Dr. Pierre Verlinden, Chief Scientist and Vice-President of Trina Solar, has received the IEEE William R. Cherry Award in recognition of his long and distinguished career at the forefront of PV technology and commercialization, for leading technology advances including the interdigitated back contact (IBC) cell, mono- and multicrystalline PERC silicon solar cells and multijunction III–V dense array technology for CPV application, and for his overall leadership of key R&D organizations throughout his career. Dr. Verlinden is currently Vice-Chair of the State Key Laboratory of PV Science and Technology, Changzhou, China, as well as adjunct Professor at Sun Yat-sen University, Guangzhou, China.

He has been involved with high-efficiency PV technologies for more than 35 years, first as an early developer of IBC silicon solar cells from 1979, at the University of Louvain, Belgium, and Stanford University, California. He continued his pioneer work on IBC solar cell development for CPV and one-sun applications as Director of R&D at SunPower until 2001. After a short stay at Origin Energy Solar, Australia, to build a pilot line for the Sliver cell, he founded AMROCK and helped many other companies and research centers to develop advanced PV technologies, including multijunction III–V dense arrays for reflective CPV systems at Solar Systems, Australia. In early 2012, Dr. Verlinden joined Trina Solar in Changzhou, China, where, marrying western-style and Chinese-style R&D, he transformed the State Key Laboratory of PV Science and Technology into one of the most advanced research centers in photovoltaics. He has been associated with several efficiency world records during his long career dedicated to photovoltaics.

Dr. Verlinden delivered his Cherry Award acceptance speech on Monday, June 6th in the Oregon Ballroom, during the 2016 PVSC Opening Keynote Session.

43rd Photovoltaic Specialists Conference (PVSC) Young Professional Award Winner

Dr. Bram Hoex, Recipient of the 43rd PVSC Young Professional Award

The IEEE Photovoltaic Specialists Conference (PVSC) continued this year in recognizing an outstanding young professional in the photovoltaics (PV) community. The PVSC Young Professional Award recognizes individuals who have made significant contributions to the science and technology of PV energy conversion, including work on PV materials, devices, modules, and/or systems. The award recipient must also show significant promise as a leader in the field.

On behalf of the organizing and program committees of the 43rd IEEE PVSC, I am delighted to announce the recipient of this year's award—**Dr. Bram Hoex** (The University of New South Wales). He is recognized for pioneering work on rear-surface passivation of Si solar cells, which enabled an industry transition to higher efficiency, passivated emitter rear contact (PERC) cell technology.

Bram Hoex completed a MSc degree and PhD degree in Applied Physics from the Eindhoven University of Technology (TU/e) in the Netherlands. His PhD work on functional thin films for high-efficiency solar cells was recognized by both the SolarWorld "Junior Einstein" and Leverhulme "Technology Transfer" awards. After completing his PhD degree in 2008 he joined the Solar Energy Research Institute of Singapore (SERIS) at the National University of Singapore (NUS) as head of the Photovoltaic Characterization group. From 2012 to the end of 2014 he was Director of the Silicon Materials and Solar Cells Cluster as well as group leader Monocrystalline Silicon Wafer Solar Cells. In 2015 he joined the School of Photovoltaic and Renewable Energy Engineering (SPREE) at the University of New South Wales (UNSW) in Australia as an academic in a convertible tenure track position. His research focusses on the development and characterization of high-efficiency silicon wafer solar cells, typically working in close collaboration with equipment and solar cell manufacturers to ensure rapid transfer to the PV industry. His current research focuses on development and commercialization of high-efficiency device architectures that capitalize on the UNSW advanced hydrogenation technique. He is best known for his ground breaking work on aluminum oxide for crystalline silicon surface passivation which is now the de facto standard for industrial PERC solar cells. He also pioneered the application of atomic layer deposition for silicon wafer solar cell manufacturing. During his career he has raised over US$ 15M in competitive research funding of which US$ 11M as lead Principal Investigator. He has published over 100 journal and conference papers which have been cited over 3100 times to date.

Congratulations, Dr. Hoex!

Kyle Montgomery
Awards Chair, PVSC-43
Air Force Research Laboratory

Editorial 2015 IEEE T-SM Best Paper Award

High quality scholarship requires technical excellence but also connects the work to the primary references in the field. In this way the reader advances their knowledge and gains perspective. The *Transactions on Semiconductor Manufacturing* supports these goals by recognizing the best paper chosen by the Associate Editors and reviewers. The winning paper was selected from 140 papers published by T-SM in 2015. The winner is "*An Algorithm of Multi-subpopulation Parameters with Hybrid Estimation of Distribution for Semiconductor Scheduling with Constrained Waiting Time*" by Hung-Kai Wang, Chen-Fu Chien, and Mitsuo Gen published in the August 2015 issue of *IEEE Transactions on Semiconductor Manufacturing* (10.1109/TSM.2015.2439054). I congratulate the authors on their selection.

Anthony J. Muscat,
Editor-in-Chief, T-SM
Department of Chemical
& Environmental Engineering
University of Arizona

2014–2015 EDS Region 9 Outstanding Student Paper Award

The Electron Devices Society confers its prestigious Region 9 Outstanding Student Paper Award to the best Region 9 student paper published in an internationally recognized IEEE sponsored journal or conference in the field of electron devices related topics. The winning paper is entitled, "*Modeling the Impact of Multi-Fingering Microwave MOSFETs on the Source and Drain Resistances*". This paper was published in the *IEEE Transactions on Microwave Theory and Techniques*, and was authored by Fabián Zárate-Rincón, Roberto S. Murphy-Arteaga, Reydezel Torres-Torres, Adelmo Ortiz-Conde and Francisco J. García-Sánchez. The award will be presented at Symposium on Microelectronics Technology and Devices (SBMicro), which will be held August 30 to September 2, 2016 in Belo Horizonte, Brazil. The Award consists of a certificate and reimbursement of up to US $1,500 to cover one author's travel and accommodations to attend the conference. On behalf of the Electron Devices Society, I would like to congratulate Fabián Zárate Rincón and the remaining authors for this achievement. Brief biographies of all the authors of the paper are given below.

Fabián Zárate Rincón received the B.S. degree in Electronic Engineering from University of Quindio, Armenia, Colombia, in 2006 and the M.S. degree in Electronics from the National Institute for Astrophysics, Optics and Electronics (INAOE), Puebla, Mexico, in 2012. He is currently pursuing the Ph.D. degree in Electronics at INAOE and working as an International Scholar at IMEC in Belgium. From 2006 to 2010, he was a Research Assistant with the University of Quindio. His research interest includes the study of semiconductor devices operating at microwave frequencies.

Roberto S. Murphy-Arteaga (SM'02) studied Physics at St. John's University, Minnesota, and got his M.Sc. and Ph.D. degrees from the National Institute for Research on Astrophysics, Optics and Electronics (INAOE), in Tonantzintla, Puebla, México. He has taught graduate courses at the INAOE since 1988, totaling over 100 taught undergrad and graduate courses. He has given over 80 talks at scientific conferences and directed seven Ph.D. theses, 13 M.Sc. and 2 B.Sc. theses. He has published more than 120 articles in scientific journals, conference proceedings and newspapers, and is the author of a text book on Electromagnetic Theory. He is currently a senior researcher with the Microelectronics Laboratory of the INAOE.

Reydezel Torres-Torres (S'01–M'06) is a senior researcher in the Microwave Research Group of INAOE in Mexico. He has authored more than 60 journal and conference papers and directed 5 Ph.D. and 14 M.S. theses, all in experimental high-frequency characterization and modeling of materials, interconnects, and devices for microwave applications. He received his Ph.D. from INAOE and has worked for Intel Laboratories in Mexico and IMEC in Belgium.

Francisco. J. García Sánchez (M'76–SM'97) received B.E.E., M.E.E. and Ph.D. degrees in Electrical Engineering from the Catholic University of America, Washington, DC, USA, in 1970, 1972 and 1976, respectively. In 1977 he joined the faculty of the Electronics Department at Universidad Simón Bolívar (USB), Caracas, Venezuela, and founded in 1979 USB's Solid State Electronics Laboratory (LEES). He presently holds a Research Professorship at USB. Since 2003 he has been an EDS Distinguished Lecturer. In 2007 he was bestowed the honorary title of "Professor Emeritus" of USB.

Adelmo Ortiz-Conde (S'82-M'85-SM'97) received the professional Electronics Engineer degree from Universidad Simón Bolívar (USB), Caracas, Venezuela, in 1979 and the M.E. and Ph.D. from the University of Florida, Gainesville, in 1982 and 1985, respectively. In 1985, he joined the technical Staff of Bell Laboratories, Reading, PA, where he was engaged in the development of high voltage integrated circuits. Since 1987 he returned to the USB where he was promoted to Full Professor in 1995. He is an EDS Distinguished Lecturer and the Chair of IEEE's CAS/ED Venezuelan Chapter. He is editor of IEEE Electron Device Letters.

Jacobus Swart
EDS Region 9 Outstanding Student Paper Award Chair
FEEC/UNICAMP—State University of Campinas
Brazil

EDS Members Recently Elected to IEEE Senior Member Grade

Kunihiro Asada
Mustafa Badaroglu
Adrijan Baric
Ivan Boshnakov
James Cale
Saurabh Chaudhury
Rishu Chaujar
Zhihong Chen
Kuan Yew Cheong
Woo Young Choi
Alan Cook
Chao-Hai Du
A. D. D. Dwivedi
Gabriele Formicone
Tong Ge
Andrea Ghetti
Mohd Nizar Hamidon
Pouya Hashemi
Bram Hoex
Mark Hollis
Heng-Ming Hsu
Bommanna Raja K.
Sivasankaran K.
Jinfeng Kang
Ya-Chin King
Maxim Klebanov
Nagarajan Krishnan Kothalam
Trupti Lenka
Hai Li
Lain-Jong Li
Len Mizrah
Mohammad Nasser
Mohsin Nawaz
Sung-Kun Park
Richard Poore
Siavash Pourkamali
Ionut Radu
Kartik Raol
Angus Rockett
Stephen Sampayan
Thomas Simacek
Soegija Soegijoko
Anthony Suto
Wing-Shan Tam
Ramesh Vaddi
Xiaohong Wang
Harry Wiederspahn
Mark Wistey
Purakh Verma
Yee Yeo
Jeffrey Yue
Brian Zahnstecher

If you have been in professional practice for 10 years, you may be eligible for Senior Membership, the highest grade of membership for which an individual can apply. New senior members receive a wood and bronze plaque and a credit certificate for up to US $25 for a new IEEE society membership. Upon request a letter will be sent to employers, recognizing this new status. For more information on senior member status, visit: http://www.ieee.org/membership_services/membership/senior/index.html

To apply for senior member status, fill out the on-line application after signing in with your IEEE account: https://www.ieee.org/membership_services/membership/senior/application/index.html.

Please remember to designate the Electron Devices Society as your nominating entity!

Call for Nominations and Election

Call For Nominations EDS Board of Governors—BoG Members-at-Large Election

Albert Wang
EDS Chair of Nominations & Elections

The IEEE Electron Devices Society invites nominations for election to its Board of Governors – BoG *(formerly AdCom)*. The next election will be held after the BoG meeting on Sunday, December 4, 2016. This year, seven out of the twenty-two members will be elected for a 3-year term, with a maximum of two consecutive terms.

This year EDS will again be running the pilot program for one of the seven BoG Member-at-Large seats to be elected via the entire EDS membership. All nominees must choose to participate in either the election by EDS membership or the election by the BoG. There must be a minimum of two nominees for the seat elected by membership. If there are less than two nominees for the seat, an election by EDS membership will not be held and the candidate will be moved to the election by the BoG. All electees begin their term in office on January 1, 2017. The nominees need not be present to run for the election. Self-nominations are allowed. In the unlikely event that a nominee must withdraw their name from the

election ballot they must do so by September 1, 2016, with an email to Laura Riello (l.riello@ieee.org).

Any EDS member who has served for a minimum of one year as an EDS Officer, Vice-President, Standing & Technical Committee Chair/Member, Publication Editor and Chapter Chair is eligible to be nominated, unless otherwise precluded from doing so in the EDS Bylaws. The electees are expected to attend both BoG Meetings every year. While the December meeting is organized in connection with the IEEE International Electron Devices Meeting, the mid-year meeting is frequently held outside the US. Partial travel support is available to attend both of these meetings.

All nominees must be endorsed by one BoG member, i.e., one of the four officers (President, President-Elect, Treasurer or Secretary), the Jr. or Sr. Past President or one of the 22 current BoG Members-at-Large. It is the responsibility of the endorser to make sure that, if elected, the nominee is willing to actively serve in the position as a BoG member.

Please submit your EDS BoG nomination by August 1, 2016, using the online nomination form (https://ieeeforms.wufoo.com/forms/k4vny-ad0ys3o4z/).

Also, all endorsement letters should be sent to Laura Riello, EDS Executive Office, via e-mail: l.riello@ieee.org by August 1, 2016. If you have any questions, please feel free to contact Laura Riello (l.riello@ieee.org) with a copy to me at aw@ece.ucr.edu.

Albert Wang
EDS Chair of Nominations & Elections
University of California, Riverside
Riverside, CA, USA

EDS Board of Governors Members-at-Large Election Process

Albert Wang
EDS Chair of Nominations & Elections

The Members-at-Large (MAL) of the EDS Board of Governors are elected for staggered 3-year terms, with a maximum of two consecutive terms. The 1993 Constitution and Bylaws changes mandated increasing the number of elected MAL from 18 to 22, and required that there be at least two members from each of the following geographic areas: Regions 1–7 and 9; Region 8; Region 10. In 2003, EDS made changes to its Constitution and Bylaws to require that at least one elected BoG member is a Young Professional (YP–formerly Gold member). A Young Professional member is defined by IEEE as a member who graduated with his/her first professional degree within the last fifteen years. It is also required that there are at least 1.5 candidates for each opening.

This year EDS will again be running the pilot program for one of the BoG Member-at-Large seats to be elected via the entire EDS membership. All nominees must choose to participate in either the election by EDS membership or the election by the BoG. There must be a minimum of two nominees for the seat elected by membership. If there are less than two nominees for the seat, an election by EDS membership will not be held and the candidate will be moved to the election by the BoG. All electees begin their term in office on January 1, 2017. The nominees need not be present to run for the election. In 2016, seven positions will be filled.

The election procedure begins with the announcement and Call for Nominations in the *EDS Newsletter*. The slate of nominees is developed by the EDS Nominations Committee and includes the non-Committee and self-nominations received. Nominees are asked to submit a two-page biographical resume and an optional 50 word personal statement in a standard format. The election for the one BoG seat voted on by the EDS membership will be done using Vote Net. Vote Net is a web based tool that allows members the opportunity to cast their ballots electronically. An e-announcement will be sent to those EDS members who have email addresses in the IEEE database prior to the election launch date. It will give the members an opportunity to indicate their preference to receive an electronic or paper ballot. By default, paper ballots are automatically printed and mailed to EDS members without email on file as well as to those that have indicated they prefer not to receive election material electronically (based upon the communication preference in their member profile).

Any EDS member who has served for a minimum of one year as an EDS Officer, Vice-President, Standing & Technical Committee Chair/Member, Publication Editor & Chapter Chair is eligible to be nominated, unless otherwise precluded from doing so in the EDS Bylaws. All nominees must be endorsed by one BoG member, i.e., one of the four officers (President, President-Elect, Treasurer or Secretary), the Jr. or Sr. Past President or one of the 22 current BoG Members-at-Large. Self-nomination is allowed. Endorsers should send a brief email to Laura Riello, stating that they would like to endorse the candidate. Please note

that there is no limit to the number of candidates that a full voting BoG member can endorse.

Nominations are closed after August 1, 2016, and the biographical resumes and endorsement letters are distributed to the BoG prior to the December BoG meeting. The election is then held after the conclusion of the meeting.

Albert Wang
EDS Chair of Nominations & Elections
University of California, Riverside
Riverside, CA, USA

IEEE Annual Election – Don't Forget to Vote!

This is a reminder for EDS members to vote in the 2016 IEEE Annual Election for the following positions and candidates. In addition to the election of officers, this year members will be asked to vote on an amendment to the IEEE Constitution. Listed below are the positions and candidates that will appear on the 2016 IEEE Annual Election ballot.

Position	Candidate
IEEE President-Elect, 2017	• James A. Jefferies (nominated by IEEE Board of Directors) • Wanda K. Reder (nominated by IEEE Board of Directors)
IEEE Division I Delegate-Elect/Director-Elect, 2017	• Renuka P. Jindal (nominated by IEEE Division I) • Rakesh Kumar (nominated by IEEE Division I)
IEEE Region 2 Delegate-Elect/ Director-Elect, 2017-2018	• Wolfram Bettermann (nominated by IEEE Region 2) • Murty S. Polavarapu (nominated by IEEE Region 2)
IEEE Region 4 Delegate-Elect/ Director-Elect, 2017-2018	• David Alan Koehler (nominated by IEEE Region 4) • Hamid Vakilzadian (nominated by IEEE Region 4)
IEEE Region 6 Delegate-Elect/ Director-Elect, 2017-2018	• Tariq S. Durrani (nominated by IEEE Region 8) • Elya B. Joffe (nominated by IEEE Region 8) • Magdalena Salazar-Palma (nominated by IEEE Region 8)
IEEE Region 8 Delegate-Elect/ Director-Elect, 2017-2018	• Stefan G. Mozar (nominated by IEEE Region 10) • Akinori Nishihara (nominated by IEEE Region 10)
IEEE Region 10 Delegate-Elect/Director-Elect, 2017-2018	• W.C. "Chuck" Adams Jr. (nominated by IEEE Standards Association) • Mark Epstein (nominated by IEEE Standards Association) • Robert S. Fish (nominated by IEEE Standards Association)
IEEE Standards Association Board of Governors Member-at-Large, 2017-2018	• W.C. "Chuck" Adams Jr. (nominated by IEEE Standards Association) • Mark Epstein (nominated by IEEE Standards Association) • Robert S. Fish (nominated by IEEE Standards Association)
IEEE Technical Activities Vice President-Elect, 2017	• Sergio Benedetto (nominated by IEEE Technical Activities) • Susan "Kathy" Land (nominated by IEEE Technical Activities)
IEEE-USA President-Elect, 2017	• Edward G. Perkins (nominated by IEEE-USA) • Sandra L. "Candy" Robinson (nominated by IEEE-USA) • Charles P. Rubenstein (nominated by IEEE-USA)
IEEE-USA Member-at-Large, 2017-2018	• Wole Akpose (Nominated by IEEE-USA) • Peter S. Winokur (Nominated by IEEE-USA)
Constitutional Amendment	• http://www.ieee.org/about/corporate/election/2016_constitutional_amendment.html

Balloting period starts on 15 August and ends at 12:00 noon, Central Time USA (17:00 UTC) on 3 October 2016. All eligible voting members should look for their ballot package to arrive via postal mail or access it electronically at www.ieee.org/elections. For more information on the election and candidates, visit the IEEE Annual Election Web page at www.ieee.org/elections, or email election@ieee.org.

Apply Now – 2017 EDS Chapter Subsidies

The deadline for EDS chapters to request a subsidy for 2017 is September 1, 2016. For 2016, the EDS BoG awarded funding to 78 chapters, with most amounts primarily ranging from US$250 to US$750. In June, Chapter Chairs were sent an e-mail notifying them of the current funding cycle and providing them with a list of guidelines. In general, activities which are considered fundable include, but are not limited to, membership promotion,

travel allowances for invited speakers to chapter events, and support for student activities at local institutions.

Chapter Subsidy requests can be submitted by completing the EDS Chapter Subsidy Request Form. Please note that the request needs to be submitted by September 1st.

Final decisions concerning subsidies will be made in December. Subsidy checks will be issued by early January of the following year. Please visit the EDS website for more information, http://eds.ieee.org/chapter-subsidy-program.html.

Enhance Your Career with IEEE Senior Membership!

Tian-Ling Ren
EDS Vice-President of Membership & Services

The Electron Devices Society established the EDS Senior Member Program to both complement and enhance the IEEE's Nominate-a-Senior-Member Initiative and make IEEE/EDS members aware of the opportunity and encourage them to elevate their IEEE membership grade to Senior Member. This is the highest IEEE grade for which an individual can apply and is the first step to becoming a Fellow of IEEE. If you have been in professional practice of 10 years, you may be eligible for Senior Membership.

Benefits of Senior Membership[1]

- **Recognition:** The professional recognition of your peers for technical and professional excellence.
- **Senior member plaque:** Since January 1999, all newly elevated Senior members have received an engraved Senior Member plaque to be proudly displayed for colleagues, clients and employers to see. The plaque, an attractive fine wood with bronze engraving, is sent within six to eight weeks after elevation.
- **US$25 coupon:** IEEE will recognize all newly elevated Senior members with a coupon worth up to US$25. This coupon can be used to join one new IEEE society. The coupon expires on 31 December of the year in which it is received.
- **Letter of commendation:** A letter of commendation will be sent to your employer on the achievement of Senior member grade (upon the request of the newly elected Senior member).
- **Announcements:** Announcement of elevation can be made in section/society and/or local newsletters, newspapers and notices.
- **Leadership Eligibility:** Senior members are eligible to hold executive IEEE volunteer positions.
- **Ability to refer other candidates:** Senior members can serve as a reference for other applicants for senior membership.
- **Review panel:** Senior members are invited to be on the panel to review senior member applications.
- **US$25 referral coupon:** Newly elevated Senior members are encouraged to find the next innovators of tomorrow and invite them to join IEEE. Invite them to join and the new IEEE member will receive $25 off their first year of membership.

As part of the IEEE's Nominate-a-Senior-Member Initiative, the nominating entity designated on the member's application form will receive US$10 from IEEE for each application approved for Senior Member grade when there are at least five approved applications. As an EDS member, we would appreciate it if you could indicate on your Senior Member application form that **EDS** is your nominating entity.

Please be aware that even if you decide to list EDS as your nominating entity, you still need to have an IEEE member nominate you along with two other references. Your nominator and your references all must be active IEEE members holding Senior Member, Fellow or Honorary Member grade.

For more information on the criteria for elevation to Senior Member, please visit the Senior Membership Portal: http://www.ieee.org/membership_services/membership/senior/index.html .

We strongly encourage you to apply for IEEE Senior Membership to enhance your career. At the same time, you'll be helping EDS. Thank you for supporting IEEE and EDS.

[1]IEEE.org, http://www.ieee.org/membership_services/membership/senior/index.html

Tian-Ling Ren
EDS Vice-President of Membership and Services
Tsinghua University
Beijing, China

2016 EDS Chapter of the Year Award
Call for Nominations

The EDS Chapter of the Year Award is given each year based on the quantity and quality of the activities and programs implemented by the chapters during the prior July 1st–June 30th period.

Each year EDS will award one Chapter from each of the following Regions:

- Regions 1–7
- Region 8
- Region 9
- Region 10

Nominations for the awards can only be made by SRC Chairs/Vice-Chairs, Regions/Chapters Committee Members or self-nominated by Chapter Chairs. Please visit the EDS website to submit your nomination form (http://eds.ieee.org/chapter-of-the-year-award.html).

Each winning chapter will receive a plaque and check for $500 to be presented at an EDS conference or chapter meeting of their choice. Travel reimbursement will not be provided.

The schedule for the award process is as follows:

Action	Date
Call for nominations e-mailed to chapter chairs, SRC Chairs, SRC Vice-Chairs and Regions/ Chapters Committee	June 1st
Deadline for nominations	September 15th
Regions/Chapters Committee & SRC Chairs & Vice Chairs selects winners	Early-October
Award given to chapter representative at requested chapter meeting	Open

ATTENTION!

Your Chapter Could Be Missing Important Notices and Funding Opportunities!

Please remember, whenever there is a change to Chapter Officers, both IEEE and EDS must be notified.

Please follow these two steps:

1. Report officer changes to IEEE via the vTools Officer Reporting form: https://officers.vtools.ieee.org/ (access to vTools requires use of an IEEE account).
2. Report officer changes to EDS by completing the Chapter Chair Update Form: https://ieeeforms.wufoo.com/forms/pgu6n1i1ixepnu/

Thank you in advance for your assistance.

EDS WEBINARS—RECENT EVENTS

EDS serves as a scientific publisher, technical conference organizer and sponsor and a networking resource to its members' learning process.

From undergraduate students to tenured professors and renowned researchers, EDS is a family providing knowledge and opportunities in the domain of electronic devices.

As part of our commitment to enhancing the value of membership in EDS, we are pleased to present the EDS Webinar Archive. The online collection provides our members with on-demand access to streaming video of past events. Recently held webinars listed below can be accessed at, http://eds.ieee.org/webinar-archive.html.

Metal Halide Perovskite Solar Cells Abstract

Presented by: Henry J. Snaith, University of Oxford

Within the last few years metal halide perovskites have risen to become a very promising PV material, captivating the research community. In the most efficient devices, which now exceed 22% solar to electrical power conversion efficiency, the perovskite is present as a solid absorber layer sandwiched between n and p-type charge collection contacts. Increasing importance of improving solar cell operation is reliant upon understanding and controlling thin-film crystallisation and controlling the nature of the p and n-type contacts. In addition, understanding and enhancing long term stability of the materials and devices if a key driver. Here I will present a brief overview of the perovskite field and the emergence of this technology. I will then present some of our recent work on developing thin film perovskite solar cells, and specifically highlight recent advances in understanding the thin film crystallisation and the mechanism driving hysteresis, which is often observed in the current voltage curves. I will further present our recent work on all inorganic perovskites, which may offer vastly enhanced stability at elevated temperatures, and on narrow band gap Sn based perovskites. Finally I will discuss the opportunity to combine perovskite with silicon in tandem junction solar cells, and the further challenges to overcome before this technology is ready for production.

Memory—the N3XT Frontier

Presented by: H.-S. Philip Wong, Stanford University

Computer architecture is going to change in the coming decade because today's architecture has severe limitations in energy efficiency and latency for memory access.

At the same time, new types of non-volatile memory have emerged that can easily be integrated on-chip with the microprocessor cores. Some of them can be programmed and read quickly; others can have very high data storage density. Importantly, all of these memories are free from the limitations of Flash — that is, low endurance, need for high voltage supply, slow write speed and cumbersome erase procedure. Fine-grain, monolithic 3D integration of massive memory with logic will be the next frontier that will provide more than 1,000× improvement in energy efficiency of computing systems [1].

I will give an overview [2] of the "new" memory technologies that are being explored currently in industry and in academia: magnetic memory, resistive switching metal oxide memory [3], conductive bridge memory, phase change memory [4]. I will go over the fabrication process, essential device characteristics, and potential applications. To facilitate a connection with circuit designers, a compact model for RRAM has been developed and made available to the public [5]. I will describe our efforts to explore device size scaling below 10 nm as well as 3D stacking of RRAM and the use of nanomaterials such as graphene in RRAM and PCM devices.

Work supported in part by STARnet SONIC, IARPA, SRC/GRC, NSF, and member companies of the Stanford Non-Volatile Memory Technology Research Initiative (NMTRI) and Stanford SystemX Alliance.

Power Semiconductor Device Basics

Presented by: Ichiro Omura, Kyushu Institute of Technology

Power semiconductor device has been the key technology for controlling various kinds of electric equipment, energy flow management for power grid and power transmission such as HVDC and energy saving systems control including PVs, HEVs, wind turbines and batteries. Specially, recent increase in electric energy demand highlights power semiconductor device as the solution technology to meet the requirement for energy saving.

Power MOSFETs and insulated gate bipolar transistors (IGBT) have been the major power semiconductor devices in the today's market and these silicon devices show technology progress by breaking the limit with

the superjunction structure, trench MOS gate, thin-wafer / field stop technologies. Emerging new material (SiC, GaN) devices have recently penetrates in some application segment by the extreme performance. Power IC technology, packaging and protection technology have become more important than ever with the high density integration of the power electronics system and devices.

Power Electronics as an enabler for a Smart Energy Future

Power Electronics circuitry is a key enabler to implement a smart energy future. It is almost unthinkable to implement a sustainable electricity system without controlled conversion in, for instance, high-power transmission in AC as well as DC at high and low voltages, renewable energy grid integration of wind and photovoltaic power, energy storage interfacing, electric vehicle charging, microgrids and efficient high-dynamic industrial drives.

Presented by: Johan Driesen, KU Leuven/ EnergyVille

In this webinar we will discuss the current role of power electronic circuits in the smart energy systems, including intelligent grids and buildings, using implementation examples or demonstrators. Starting from selected challenging applications, the evolution of the circuits is linked to the evolution in components such as new wide-bandgap semiconductors and passives.

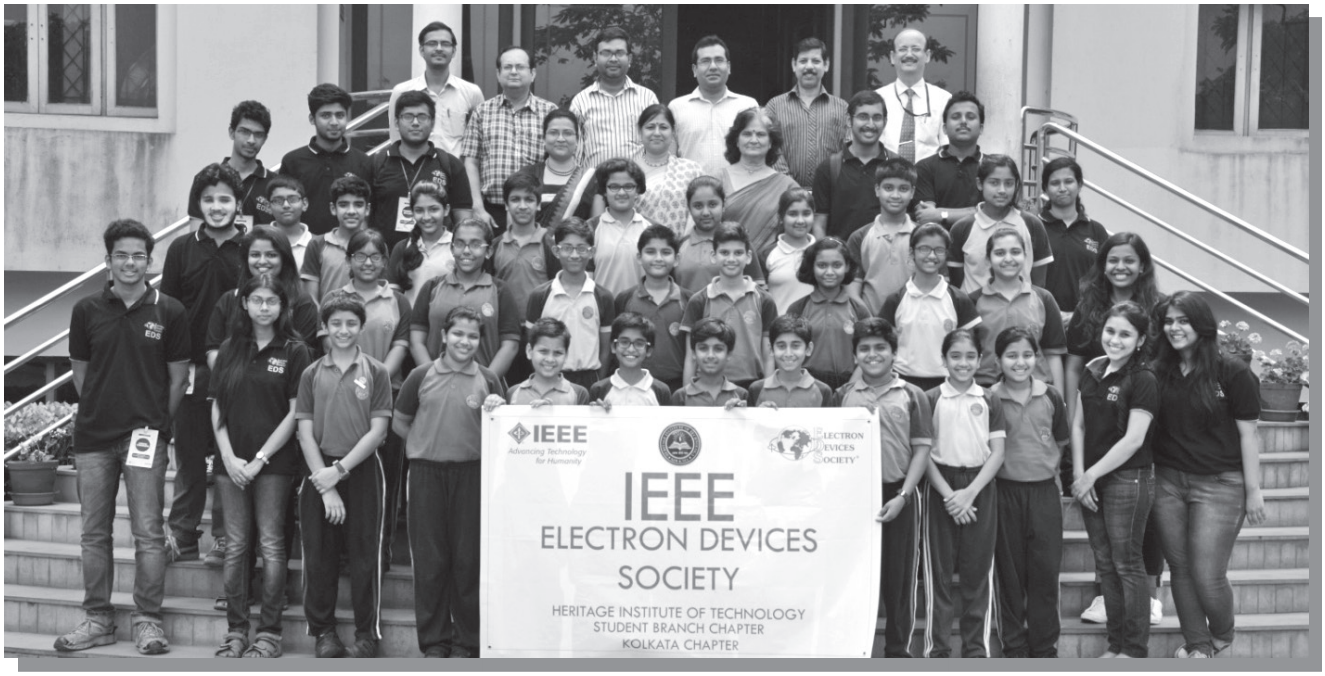
This tutorial is intended for the Power Electronics/Power Devices professional who is interested in the (bidirectional) interaction between trends on circuit/component level and applications in system-wide electrical energy conversion.

M.K. Radhakrishnan
EDS Newsletter Editor-in-Chief

EDS-ETC Programs

EDS-ETC by ED Coimbatore Chapter

A "Science to Engineering – Electronics Kit Demo" program was organized by the IEEE Student Branch (08171), Cape Institute of Technology, Levengipuram, in association with the Electron Devices Society Coimbatore Chapter. Events were held February 10, 2016 at Govt. Middle School, Kathadithattu and February 15, 2016, at St. Mary's Higher Secondary School, Kaliyal. Five student volunteers from the chapter participated and organized the training program. Around 38 students from Middle class and 30 students from 8th Standard attended the programs respectively. The training to the students was given with the kits provided by the ED Coimbatore Chapter. Some basic electronic component presentations were made with the volunteers explaining the importance of electronics and its impact. The participants were divided into 5 teams and the session started with hands-on training to the students. The post-lunch session began with some innovative video presentations



Instructors and student attendees of the 'MINDSPARK' workshop

about electronics. To make the day more interesting, some contests like Quiz, Colour Coder and the circuit combo contests were conducted for the students.

An EDS-ETC program named 'MINDSPARK' was organized at The Heritage School, Kolkata, India, March 10, 2016, with participation of the IEEE EDS Heritage Institute of Technology Student Branch Chapter and IEEE EDS Kolkata Chapter. The workshop had 26 children from standard VI, actively working hand-in-hand with 13 student volunteers from IEEE EDS HIT SBC.

With the help of student volunteers the children completed several projects of their choice using 'Elenco Snap Circuits®' kits. Having experienced the exciting and creative field of electronics, the children were overwhelmed with joy. The organizers had to leave promising to return with more such exciting projects.

Participants of the EDS Kolkata EDS-ETC Program

EDS-ETC by HITK and Kolkata Chapters

—Dwaipayan Chakraborty and Atanu Kundu

EDS HITK Student Branch Chapter jointly with the EDS Kolkata Chapter and Cognizant Technology Solutions Outreach team organized an EDS-ETC Program on March 26, 2016, at Bangur School. The program was part of a weekly Science/Computer/English class.

A few projects were demonstrated to the students with the help of the Elenco Snap Circuits® kits. There were 98 participants who attended the program. The experiments demonstrated the basic concept of electronic devices and circuits.

At Kasba Social Development

The EDS HITK Student Branch Chapter, jointly with IEEE EDS Kolkata Chapter and Cognizant Technology Solutions Outreach team, organized an EDS-ETC Program on March 26, 2016, at Kasba Social Development Society. The program was part of a weekly Science/Computer/English class. There were 28 participants who attended this program.

Participants at the EDS-ETC Program held for the Kasba Social Development Society

EDS-ETC Program participant at Lighthouse for the Blind

At Lighthouse Kolkata for the Blind

The EDS HITK Student Branch Chapter, jointly with IEEE EDS Kolkata Chapter and Cognizant Technology Solutions Outreach team, organized an EDS-ETC Program on March 26, 2016, at Lighthouse for the Blind. The program was a part of a weekly Science/Computer/English class.

A few projects were demonstrated to the sole student attendee of the class given at Lighthouse for the Blind. Experiments demonstrating the basic concept of electronic devices and circuits were given.

At AIWC Buniyadi School, Kolkata

The EDS HITK Student Branch Chapter, jointly with IEEE EDS Kolkata

Chapter and Cognizant Technology Solutions Outreach team, organized an EDS-ETC Program on March 26, 2016, at AIWC Buniyadi School. The program was a part of a weekly Science/Computer/English class.

A few Snap Circuits projects were demonstrated to the 25 students who attended the program. The experiments demonstrated the basic concept of electronic devices and circuits.

~ Manoj Saxena, Editor

Demonstration of the projects with the help of the Elenco Snap Circuits® kits

QuestEDS

Interested in knowing why it's not possible to measure the built-in voltage of a PN junction using a voltmeter? Do you need to understand the best way to derive an expression for the average thermal velocity of an electron? Or are you curious about what quantum dots and wires are? The answers to these questions and more are available through the QuestEDS Question and Answer page.

To ask a question not already addressed on the Q&A page, visit www.ieee.org/go/questeds. Technical experts answering the questions posed represent academic, government and industry sectors. Questions are grouped into five technical categories and two general ones. Technical categories cover subject areas like semiconductor and device physics, process technology, device characterization and quantum electronics. Subject areas addressed are anticipated to expand in the future. Two other categories address questions pertaining to educational activities and general inquiries about society membership. Within a two week time frame from when the question is asked, an answer is posted online. Incoming questions are handled by an editor-in-chief who ensures that they fall within the technical scope of EDS and that they are adequately answered.

Question 062-16:
What is the mechanism that causes the drain current to increase for devices on GaAs with WSi gates under high temperature conditions, i.e. reliability testing, where the typical profile is a decrease in the drain current over time for other gate alloys?

Answer 062-16:

WSi gates are generally more stable than conventional Ti/Pt/Au metallization schemes: they are exempt from major interdiffusion and hydrogen poisoning problems at the expense of a slightly higher gate resistivity.

If the drain current is measured in DC and the gate contact is responsible for drain current changes (in this case drain current increase) one should measure a change in the threshold voltage towards negative values, possibly corresponding to a decrease in the Schottky barrier height. The later may be due to several reasons: changes in the interface, piezoelectric effects due to different thermal expansion coefficient of materials, chemical reaction at interface (difficult with WSi). One should also look at forward and reverse I-V characteristics of the gate Schottky diode.

If nothing occurs at the gate (no change in threshold voltage, no barrier height change, no change at all in the gate characteristics), maybe the current drain is improving because of the improvement in the ohmic contacts, reducing the drain and source series resistance, and the gate contact is simply stable (which is not in the case for Ti/Pt/Au) gates.

Hypothetically, thermal treatments may improve the electron mobility under WSi contact, which could be again a piezoelectric effect.

It is of interest to the expert providing the answer of the question as well as to the readers to know if the drain current increase noticed in reliability test is permanent.

For an archive of past questions and answers, visit http://eds.ieee.org/questeds/question-and-answer-page.html .

This issue's QuestEDS Question and Answer is from the category of **Compound Semiconductor Devices.**

Chapter News

Reflections from EDS Malaysia Chapter

By Badariah Bais

The IEEE Electron Devices Society (EDS) Malaysia Chapter was established in 1991 by a team lead by the late Prof. Dr. Zahari Mohd Darus from the Department of Electrical, Electronic and Systems Engineering, Universiti Kebangsaan Malaysia (UKM). The leadership of EDS was continued by Prof. Dato' Dr. Burhanuddin Yeop Majlis, currently the Director of the Institute of Microengineering and Nanoelectronics (IMEN), UKM from 1994–2006, followed by Prof. Dr. Sahbudin Shaari, UKM from 2007-2008, Prof. Dr. Zaliman Sauli, Universiti Malaysia Perlis (UniMAP) from 2009–2010, Prof. Dr. Ibrahim Ahmad, Universiti Tenaga Nasional (Uniten) from 2011-2012 and Assoc. Prof. Dr. Mohd Nizar Hamidon, Universiti Putra Malaysia (UPM) from 2013–2014. Assoc. Prof. Dr Badariah Bais from the Faculty of Engineering & Built Environment, UKM is the current chair.

ICSE 1992 organizing team with S. M. Sze

Since the establishment, EDS Malaysia has been actively organizing conferences, short courses, technical talks and workshops related to semiconductor electronics devices. Two flagship conferences i.e. International Conference on Semiconductor Electronics (ICSE) started in 1992 and Regional Symposium on Micro and Nanoelectronics (RSM), previously known as National Symposium on Microelectronics (NSM), are the main activities of the chapter. ICSE'92, held in Kuala Lumpur was the first experience for EDS in organizing an international conference. Even though the conference only attracted 27 papers,

A picture of ICSE 2012 participants

the majority of the participants were international. Invited speakers included Prof. S.M. Sze, Prof. Cary Yang, Prof. Jong Duk Lee. Not many papers were from Malaysia at the first ICSE, but it paved a way for improving research in the country. In the second international conference ICSE organized by the EDS Chapter in 1996 which was held in Penang and research papers from Malaysia was limited, however overall papers and participation improved. In 1997, EDS organized its first national symposium National Symposium on Microelectronics (NSM'97). The vision of the symposium was to provide a suitable platform to encourage and train local researchers and lecturers to participate in the next ICSE and at the same time to cultivate research cultures in Malaysia. NSM97 was held in UKM with only 33 papers from all over Malaysia.

EDS kept on organizing its international conference and national symposium year after year. The number of papers and participants kept increasing and in 2002, ICSE2002 had attracted a total of 121 papers, a sharp rise from its previous conferences and had started to attract sponsorship as well. ICSE2006 was the peak time for EDS where a total of 225 papers were presented with 69 of them related to MEMS and Nanoelectronics. The national symposium has also started gaining its momentum with more papers and regional participation from many Asian countries by NSM2005. So, NSM was renamed to be IEEE Regional Symposium on Micro and Nanoelectronics in 2007.

ICSE is now a known conference in Asia, and is technically co-sponsored by EDS. The 12th ICSE will be held in Kuala Lumpur from August 17-19, 2016. These flagship conferences of EDS Malaysia have been recognized worldwide, and have attracted participants from all over the world. Through these conferences, EDS Malaysia has the opportunity to invite well respected individuals in their field as keynote speakers.

Beginning 2015, the Chapter started to participate in community engagement related projects. The Chapter introduced the EDS-ETC kits in their Educational Program to elementary and high school students. The main objective of the program is to increase awareness and stimulate interest in the field of Electrical and Electronics Engineering among the elementary and high school students.

Throughout the years, EDS has grown and flourished with the hard work and dedication from all members. This hard work and dedication paid off when the Electron Devices Malaysia Chapter won the 2014 EDS Region 10 Chapter of the Year Award. One of the EDS ExCom members, Dr. P. Susthitha Menon from UKM, won the best volunteer award from the IEEE Malaysia Section in 2015.

With the involvement of EDS in Malaysia, research activities in the field of semiconductor electronics has had a significant increase and ICSE and RSM continue to provide the platform for meetings among researchers and academia. In fact, through all these activities, the EDS Malaysia Chapter provided a lead to Malaysia's growth in electronics technology incorporating research along with fabrication facilities in the country.

2016 IEEE EDS South Asia Chapter Chair Meeting

By Manoj Saxena, Region 10 SRC Vice Chair

The 12th meeting of the EDS Chapter Chairs in the South Asia region of Region 10 was held at the ED NIST Student Chapter at Berhampur, India, on February, 2, 2016. EDS Vice President of Regions and Chapters, M. K. Radhakrishnan chaired the meeting. EDS President Samar Saha, Regions & Chapters Committee member and BoG member Durga Misra, R/C committee member Soumya Pandit and SRC Vice Chair Manoj Saxena, attended the meeting along with Chapter Chairs, representatives and Student Chapter advisors.

Attendees of the 2016 IEEE EDS South Asia Chapter Chair meeting

Out of the 24 ED Chapters in the South Asia region, 22 Chapters reported their activities. The major deliberations include the plans to revive the Highly Valued Volunteer recognition from the region from this year. Also, there will be research paper citation recognition for papers published in EDS journals and IEDM. The ICEE 2016 will be held at IIT Bombay

in December, which is the brain child of all the Chapters in the region.

During the year, one ED Chapter and three ED Student Chapters were formed in the region. Now there are plans for two more Chapters and one student Chapter in Bangladesh. The communication between Chapters will be streamlined through a Google Group. The next Chapter Chairs meeting will be held in conjunction with ICEE in December 2016.

MQs, DLs and Conference Reports

EDS Mini-Colloquium Held in Grenoble, France

Lecturers and attendees of EDS Mini-Colloquium on May 30, 2016

The French chapter of the Electron Devices Society organized a Mini-Colloquium held in Grenoble, France, at the Phelma Minatec Campus, May 30, 2016. The MQ gathered nine EDS Distinguished Lecturers from around the world presenting state of the art of various nano-electronics branches.

First, Dr. Simon Deleonibus gave an overview of the IEEE-Electron Devices Society and its benefits. Then the program continued with the oral presentations, each of about 25 minutes, on the following topics:

- *State of the art Power Switching Devices in SiC,* Mikael Ostling, KTH, Royal Institute of Technology, Sweden
- *Ultra-thin Chips – a New Paradigm in Silicon Technology,* Joachim Burghartz, Institute for Microelectronics Stuttgart, Germany
- *GaN-HEMT Compact Model for Future Hybrid III-V/CMOS Technology,* Xing Zhou, Nanyang Technological University, Singapore
- *Recent Advances of Si/SiGe Tunneling FET for Low Voltage/Power Applications,* Steve Chung, National Chiao Tung University, Taiwan
- *Silicon device technology for intelligent communications,* Shunri Oda, Tokyo Institute of Technology, Tokyo, Japan
- *Transparent Large Area Flexible Electronics,* Arokia Nathan, Cambridge University Centre for Advanced Photonics and Electronics, UK
- *Flexible, Bendable Self Packaged MEMS Sensors,* Zeynep Celik Butler, University of Texas at Arlington
- *Three Dimensional Integration Technology,* Mukta Farooq, IBM, Hopewell Junction, USA
- *SiGe Heterojunction Bipolar Transistor "HBT" Reliability Overview with a comparison to III-V HBT's,* Fernando Guarin, Global Foundries, USA

The MQ was attended by about 60 participants.

Simon Deleonibus
Region 8 SRC Chair

Mireille Mouis
ED France Chapter Chair
IMEP-LaHC

Marco Pala
IEEE Member
IMEP-LaHC

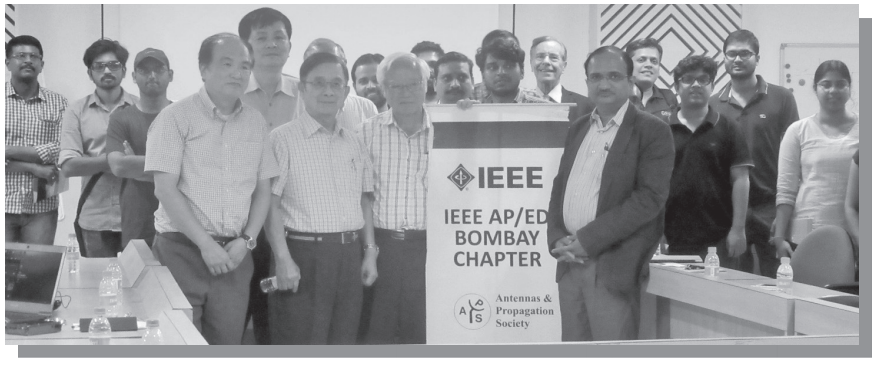
IEEE EDS Mini-Colloquium on Electron Devices QNERC International Symposium on Nano Devices at Tokyo Institute of Technology

By Masaaki Niwa, Japan Chapter Chair, Shunri Oda and Hiroshi Iwai

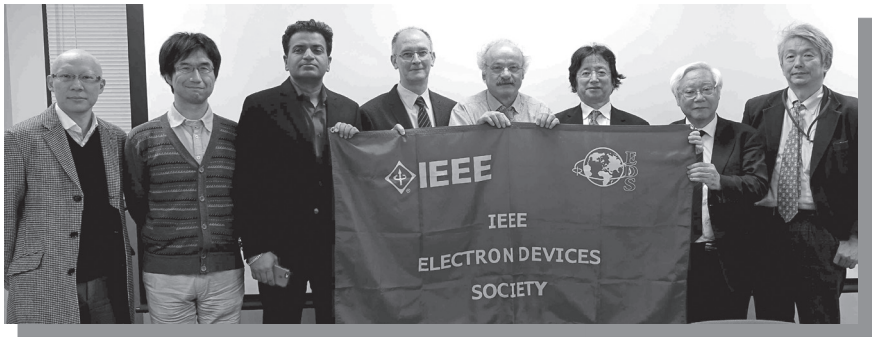
The IEEE EDS Mini-Colloquium on Electron Devices QNERC International Symposium on Nano Devices was held at Tokyo Institute of Technology, Tokyo, Japan, March 14, 2016. After the introduction by Professor Shunri Oda, Tokyo Institute of Technology (TIT) the following lectures were presented:

- Dr. Simon Deleonibus, Leti, France, on "Towards the Energy Efficient, Heterogeneous Process Technology, Zero Intrinsic Variability Devices and Zero Power Era"
- Professors Takayuki Iwasaki and Yukio Kawano of TIT, with "Diamond Electronics" and "Graphene and Carbon Nanotube Devices for Nanoscale Terahertz Imaging and Spectroscopy"
- Prof. Adrian Ionescu, EPFL, Switzerland, on "Steep-slope devices for energy efficient computing, analog/RF and sensing for Internet-of-Everything"
- Professors Yasuyuki Miyamoto and Safumi Suzuki of TIT, on "Steep Slope Devices with InGaAs Channel" and "Terahertz electron devices for various applications"
- Prof. Kaustav Banerjee on, "2D Crystals for Smart Life"
- Takamasa Kawanago, and Hiroshi Iwai of TIT spoke on "Self-assembled monolayer-based gate dielectrics for MoS_2 field-effect transistors" and "End of scaling and Moore's law"

This was a very exiting MQ, with severe and hot discussions exchanged between the audience and speakers about the future possibilities of nano devices.



Edward Yi Chang, C. Y. Chang and Hiroshi Iwai (front row, left to right), with some of the AP/ED Bombay Chapter mini-colloquium attendees



Speakers of the symposium on nano devices, at TIT, Tokyo

AP/ED Bombay Chapter Mini-Colloquium

—by V. Ramgopal Rao

The AP/ED Bombay Chapter organized a mini-colloquium on **"Nano-scale Electron Devices"** on January 12, 2016, at IIT Bombay. Professors C. Y. Chang, National Chiao Tung University, Taiwan; Hiroshi Iwai, Tokyo Institute of Technology, Japan; and Edward Yi Chang, National Chiao Tung University, Taiwan, delivered talks during this event. Chun-Yen Chang is considered to be the father of the Taiwan semiconductor manufacturing industry and is credited for the semiconductor manufacturing revolution that Taiwan underwent in the early 1980's.

Hiroshi Iwai and Edward Yi Chang are leading researchers in their respective fields, and have made significant contributions to the CMOS and compound semiconductor areas. The colloquium saw a huge attendance of students and faculty with over 100 participants.

ED NIST Student Chapter Mini-Colloquium

—by Ajit Kumar Panda

The chapter organized the **6th IEEE ED Mini-Colloquium on "Device and Reliability,"** February 20, 2016, at National Institute of Science & Technology, Palur Hill, Berhampur. Four Distinguished Lecturers were invited to address the mixed audience of students, researchers and faculties from various universities and institutes of the Odisha area and beyond. Ninety-six participants from faculties and M.Tech students made this mini-colloquium a grand success.

The Invited Distinguished Lecturers were Dr. Samar Saha, President,

Attendees and invited speakers at the National Institute of Science & Technology (NIST)

IEEE ED Society, USA; Dr. M. K. Radhakrishnan, EDS Vice President-of Regions and Chapters; Dr. Durga Madhava Misra, Member IEEE, EDS BoG and professor at NJIT; and Dr. Ravi M. Todi, EDS Vice President of Technical Committees and Meetings, ED and Director Global Technologies, USA.

Ravi Todi spoke to the students about Global Foundries and its Advanced Technology Solutions. He focused on "Technology Portfolio and Global Market", RFCMOS in Cell Phone, Power Performance Area Cost (PPAC), Reliability of 14 nm technology, Back-Bias and much more. Samar Saha discussed the various student activities of the IEEE ED Society and its benefits. He explored the research scopes in devices: Statistical Dopant Fluctuations in Semiconductor Devices, Modeling Threshold Voltage Variance due to Stochastic Dopant fluctuations in MOSFETs and JFETs, Modeling Threshold Voltage Variance in Tunnel FETs. M. K. Radhakrishnan discussed the topic of, "Circa: Device Research-from Last Century," which included the history and evolution of Devices for the last 100 years to present day semiconductor, 5 nm gate length MOS, Research activity in India (Paper publication, Patents) and its need. Dr. Durga Madhab Misra covered the topics of Acceleration in Technology Innovation, Next generation Enabling Materials, Devices and Systems, High density Logic and Storage, System on Pocket, Low power devices with high K, Nanotechnology based innovation, etc.

ED Bhubaneswar-Kolkata Chapter Mini-Colloquium

—by Sanjit Kumar Swain and Atanu Kundu

During February 20-22, 2016, a two-day mini-colloquium on **"Advanced CMOS based Nano Devices"** (MCACND-2016), was organized by the Department of ECE & Applied Electronics and Instrumentation Engineering, Silicon Institute of Technology, Bhubaneswar, in association with the EDS Bhubaneswar-Kolkata Chapter and ISTE Student Chapter, Silicon. The goal of MCACND-2016 was to introduce some of the advanced topics and cutting edge problems in the area of advanced Nano CMOS Devices. It also aimed to foster quality technical education and research to meet global challenges. The program was subdivided into three hand-on sessions: 1) TCAD Simulator; 2) Mini-Colloquium, and 3) Poster Presentation by research scholars and final year Silicon students.

- The inaugural talk was delivered by Prof. (Dr.) N V L N Murthy, Professor, Electrical Department, IIT Bhubaneswar, on the topic "4H-SIC MIS Interfaces for

MQ Speakers:((from left) Prof. (Dr.) G. N. Dash, Prof. (Dr.) Samar K. Saha, Prof. (Dr.) Durga Madhava Misra, (Dr.) Ajit Kumar Panda (extreme right)

Inaugural talk delivered by Prof. (Dr.) N V L N Murthy, Professor, Electrical Department, IIT Bhubaneswar

better passivation to SIC FETS". Mr. D. Godwinraj, Sr. Research Fellow, Jadavpur University and Mr. Arka Dutta, Sr. Research Fellow, Jadavpur University, conducted a hands-on practice session on "T-CAD Simulator." On February 22nd the following talks were given:

- Prof. (Dr.) G. N. Dash, Professor & Head of Sambalpur University's School of Physics, delivered a talk on "CMOS Scaling issues and Tunneling Graphene FET"
- Prof. (Dr.) Chandan Kumar Sarkar, Professor, ECE Dept., Jadavpur University, Kolkata, enlighted the audience through is talk on "GaN based Heterostructure Nano Transistor"
- Prof. (Dr.) Samar K. Saha, President , IEEE EDS, San Francisco, USA, delivered his talk on "Planar MOSFET Devices for Nanoscale CMOS Technology"
- Prof. (Dr.) Ajit Kumar Panda, ECE Dept., NIST, Berhampur, gave his talk entitled, "Beyond CMOS, HEMT is a Prospective Device"
- Prof. (Dr.) Durga Madhava Misra, Professor, Department of Electrical & Computer Engineering, New Jersey Institute of Technology, New Jersey, USA, lectured on "Advantages High-K Material".

The total number of participants for this lecture series was 70, with thirty-two attendees from outside organizations like KIIT University, IIIT Bhubaneswar, BJB College, CET, ITER, Trident & GIFT Engg colleges.

Distinguished Lecture at ED IIT Roorkee Student Chapter

—by Om Prakash and Arvind Sharma

The IEEE Electron Devices Society (EDS) Student Chapter, IIT Roorkee, organized an EDS Distinguished Lecture on "Technology Circuit Co-Design for Low Power Design," January, 22, 2016. The event was successfully held in the Electronics & Communication Engineering Department of IIT Roorkee. Around 60 participants, including faculty, research scholars and graduate students from IIT Roorkee attended this event. There was good technical interaction between the invited speaker and participants. In addition to the talk, there was one break session which provided a venue for fruitful discussions and exchanges of ideas and thoughts. The lecture duration was around 3 hours and was co-sponsored by IIT-Roorkee Circuits and Systems Student Branch Chapter.

Dr. Rajiv V. Joshi, Research Staff Member, T. J. Watson Research Center, focused on "Technology Circuit Co-Design for Low Power Design". In the talk, he discussed the pros and cons analysis on technology from the power perspective and various techniques to exploit lower power. He also talked about the reliability and different power optimization techniques for logic and memory cells. He summarized his talk with the key challenges in achieving low power.

Scenes of recognitions presented to Dr. Joshi and audience participation at IIT Roorkee DL event

Speaker and attendees at the IEEE Distinguished Lecture held at IIT Roorkee

The IIT Roorkee Microelectronics and VLSI group research scholars also presented their work to Dr. Joshi and received valuable feedback.

Distinguished Lecture at ED Taipei (Hsinchu) Chapter and ED NCTU Student Chapter

—by Steve Chung

The ED Taipei (Hsinchu) Chapter along with the ED NCTU Student Chapter held an invited talk on March 3rd. The speaker was Dr. Ravi Todi of GlobalFoundries, California. Dr. Todi is currently the EDS Vice President of Technical Committees and Meetings and combined his business trip to the Science Park in Taiwan, with his visit to give a EDS DL. His talk, entitled, *"Trends in Global Semiconductor Industry and Advanced Technology Solutions,"* began by reviewing the current trends in the semiconductor industry, the key growth areas, and how the foundry industry is growing. He then presented on how Finfet technology is addressing challenges the broad spectrum application needs, from super high-performance/high power server application space to high end and mid-range mobile application processors, including consumer applications, down to ultra-low power application ranges. Finally, he discussed PPA (power, performance, area) metric for 10/7 nm and advanced R&D challenges for future technology nodes. This talk was attended by around 40 students, professors, and post-doc researchers.

EDS Distinguished Lecture at ED Peking University Student Chapter

—by Xiaobo Jiang

The ED Peking University (PKU) Student Chapter held two invited talks recently.

On March 21st, Dr. Carlo Reita from CEA-LETI talked about *"Recent Advances on Nanowires for Sub-10 nm Technologies,"* where he showed the audience that a Si-SiGe CMOS platform based on nanowires would be a good candidate for continuing the scaling of devices for the 7 nm, 5 nm and possibly below.

On March 23rd, a Distinguished Lecture entitled *"Memristors: From Devices to Neuromorphic and Arithmetic Computing Applications"* was delivered by Prof. Wei Lu from University of Michigan, which attracted more than 50 students and teachers. After Prof. Lu's talk, there was a discussion on efficient neuromorphic computing with the students.

Report on China Semiconductor Technology International Conference (CSTIC 2016)

The *China Semiconductor Technology International Conference 2016 (CSTIC 2016)* was held March 13–14, 2016, in Shanghai, China. CSTIC is the largest

Prof. T. H. Hou (seated), Dr. Ravi Todi, and Prof. A. Chin. (Far right photo) Dr. Ravi Todi (right)

CSTIC 2016 Conference Committee and Keynote speakers, including CSTIC Conference Chair Dr. Hanming Wu (8th from left) and IEEE EDS members Prof. Cor Claeys (6th from left), Prof. Hiroshi Iwai (7th from left) and Prof. Ru Huang (1st from right)

Prof. Cor Claeys (right) receiving from SEMI China President Allen Lu (left) the Outstanding CSTIC Contributions Award

and the most comprehensive annual industrial semiconductor technology conference in China, aiming to provide a platform for executives, managers, engineers and researchers from around the world to exchange the latest developments in semiconductor technology and manufacturing and related fields.

CSTIC 2016 was organized by Semiconductor Equipment and Material International (SEMI), the Electrochemical Society, and The Integrated Circuit Materials Industry Technology Innovation Alliance (ICMTIA), with technical co-sponsorship by the IEEE Electron Devices Society. The conference relies on a long-time tradition, which began in 2001 and consists of 12 Symposia.

- Device Engineering and Technology
- Lithography and Patterning
- Dry & Wet Etch and Cleaning
- Thin Film Technology
- Chemical-Mechanical Polishing (CMP) and Post-CMP Cleaning
- Materials and Process Integration for Devices and Interconnections
- Packaging and Assembly
- Metrology, Reliability and Testing
- Emerging Semiconductor Technologies
- Advances in MEMS and Sensor Technologies
- Circuit Design, System Integration and Applications
- Si Materials and Photovoltaic Technology

The Symposium on Packaging and Assembly is organized jointly with the IEEE Components, Packaging and Manufacturing Technology Society (CPMTS).

For CSTIC 2016 the papers came from 19 major semiconductor manufacturing regions in the world, including Austria, Belgium, Brazil, Canada, China, France, Germany, Hong Kong, Italy, Japan, Korea, Malaysia, Mexico, Singapore, Sweden, Taiwan, The Netherlands, United Kingdom and the United States of America. About 337 papers have been selected for oral presentations and approximate 100 papers for poster presentations after careful reviews by the conference organizing committee. Approximately 60% of the papers came from industry. The EDS Student Chapter of Peking University took special action to facilitate students to participate in the conference.

During the Opening Session of CSTIC 2016 there were three conference plenary speakers, i.e. Andrea Onetti, Executive Group Vice-President and General Manager Volume MEMS & Analog Division at ST-Microelectronics, Italy; Chia-Hong Jan, Intel Fellow and Director of the System-on-Chips (SOC) Technology Integration for the Technology and Manufacturing group, Intel, USA and Qing Chu, Vice-President, Huawei Technologies, China. There were more than 1,000 attendees at the conference.

Almost 200 peer-reviewed papers were submitted for publication in *IEEE Xplore*. They represent a snapshot of the recent developments in semiconductor technology and manufacturing in the world and offer a glimpse into the

state-of-the-art of semiconductor technology and manufacturing in China.

Dr. David Huang will be the General Chair of CSTIC 2017, which will take place on March 12–13, 2017, in Shanghai.

Hanming Wu
2016 CSTIC General Chair, SMIC
Shanghai, China

Cor Claeys
2016 CSTIC Co-Chair, Imec
Leuven, Belgium

Report on 22nd IPFA
—by Dave Tan

The 22nd International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA) 2015 was successfully held June 29–2 July 2, 2015, at the scenic Lakeshore Hotel in Hsinchu, Taiwan. IPFA 2015 was organized by the IEEE ED Taipei Chapter and the IEEE Reliability/CPMT/ED Singapore Chapter. The Symposium is technically co-sponsored by the IEEE Electron Devices Society and the IEEE Reliability Society.

IPFA is devoted to the fundamental understanding of the physical mechanisms of semiconductor device failures and issues related to semiconductor device reliability, yield and performance, especially those related to advanced process technologies. Keynote Talk was given by Dr. Antony S. Oates, TSMC, Taiwan, on Reliability and Technology Challenges Beyond 10 nm node who gave an excellent overview of the upcoming challenges as process technology scales unabatedly and generated plenty of interest. Another Keynote Talk by Dr. Xin Wu, Xilinx, USA on 3D-IC was very well received as Xilinx is the first company to commercialize 3D FPGA technology and everyone was eager to learn from leaders.

A one-day Tutorial involving short courses was held with 4 topical topics covering Dynamic Fault Isolation Techniques, Scaling and Reliability Challenges, ESD Protection and FA Techniques. There were 15 Invited Talks spread throughout 3 days of intense technical sessions running in parallel Failure Analysis and Reliability tracks. The high audience interest was evident in the number of questions and comments which followed till tea break!

Hsinchu, known as "Taiwan's Silicon Valley" proved to be a very popular venue with more than 25 Exhibitors showcasing their technologies and state-of-the-art tools. The conference concluded with announcement of IPFA 2016 planned to be held July 4–8 at home turf Singapore.

Dear EDS Chapters:

When planning your upcoming chapter meetings, workshops, etc., please remember to visit the EDS website for a recent list of EDS Distinguished Lecturers and lecture topics.

Checklist

- Chapter contacts EDS DL to check availability, confirms date/location of lecture, discusses DL funding needs and determines chapter funding.
- EDS DL completes EDS DL Activity Log and Funding Request Form.
- If applicable, obtain EDS funding approval.
- Chapter publicizes lecture via web, email, etc. Obtain a chapter member list via SAMIEEE (http://www.ieee.org/about/volunteers/samieee/index).
- If applicable, DL submits an IEEE expense report to Laura Riello, to receive reimbursement.
- Chapter Chair/DL Coordinator submits an EDS DL/MQ Feedback Form.

If you have any questions and/or need more information, please do not hesitate to contact Laura Riello, EDS Executive Office.

PLEASE NOTE: A Distinguished Lecture activity completion report from the Chapter is a must for future DL approvals. Thank you for your continued support of the Society.

Europe, Middle East & Africa (Region 8)

ED Scotland

—by Anthony Walton

Earlier in the year, the Scottish Chapter of the Electron Devices Society held its second *Evening's Exploration of Past, Present and Future Electronics*. At the event, Jed Hurwitz of Analog Devices gave a fascinating talk entitled *An Insider's Outside View of CMOS Image Sensor Development: Past, Present and Future* to an audience of over 150 engineers, academics and members of the public. Drawing on experience gained from a career with companies including Matra MHS, Vision Group Ltd, ST Microelectronics and Metroic, Jed entertained the audience with a talk that took them from the beginning of CMOS imaging, through the progress of the glory years and on to his perspective of the future of digital imaging.

The talks were followed by a drinks reception in the University of Edinburgh's Eng Inn Café at which guests were able to enjoy an exhibition that included table-top displays from the Imaging Division of ST Microelectronics, the University of Edinburgh CMOS Sensors and Systems Group (http://css.eng.ed.ac.uk/), and the Museum of Communication (www.mocft.co.uk). Feedback for the event from the large audience was universally positive with many interesting discussions initiated at the reception. The evening was organized by Dr. Jonathan Terry and due to the overwhelmingly positive response to the event, plans are already in place for the third evening in the series scheduled for 2017.

~ Jonathan Terry, Editor

The Evening's Speaker Jed Hurwitz with ED Scotland Chair Professor Anthony Walton (top left); Jed joins in the lively discussions at the drinks reception (bottom) and exhibition (top right)

AP/MTT/ED/AES/GRS/NPS East Ukraine Chapter

—by Nikolay Cherpak, Mikhail Balaban and Ganna Veselovska

In 2015, our Chapter co-sponsored the Young Scientists Forum on Applied Physics (YSF-2015) held in Dnipropetrovsk, Ukraine.

This Forum brought together many PhD students and young scientists and engineers from 6 cities across Ukraine. More than 150 scientific papers were accepted for presentation. Scientific program of the conference included oral presentations on the following topics: optics and photonics, biophysics, microwave and terahertz electronics, geoscience and remote sensing, solid-state radiophysics, radio astronomy and astrophysics, nano- and metamaterials, magnetism and magnetic materials, mathematical physics, high-energy physics, high-energy astrophysics and cosmology, condensed matter physics, physical materials science and nondestructive testing, power & energy conversion and control systems, nuclear and plasma physics.

The YSF-2015 was opened by Prof. Maksym Strikha, the Deputy Minister of Education and Science of Ukraine. The Forum was held in four days, each one starting with a plenary session which was followed by three parallel scientific sessions. Among plenary lecturers there were Prof. Maksym Strikha, Prof. Gregory Quarles (EdgeLight Incorporated, Tucson, Arizona, USA), and professors representing different Ukrainian scientific institutions.

A Workshop of Opportunities (www.ysc.org.ua/workshops.php) was also held during the Forum. It was a two-day event.The main aim was to demonstrate different ways to succeed in science, technology, self-development and career building, to provide inspiring examples of Ukrainian people who have

Participants of the Young Scientists Forum on Applied Physics (YSF-2015) Dnipropetrovsk, Ukraine

succeeded in different domains, and to show the grant opportunities of different scientific organizations to each and every participant of the Forum. The program included presentations on Humboldt foundation, Fulbright program, IEEE grant opportunities, and OSA benefits for student chapters. We had also presentations of several Ukrainian projects: first Ukrainian mass open online courses "Prometheus", a Science park "Kyivska Polytechnika", a summer school AACIMP, a forum "Science. Business. Innovations-2015", a POLYTAN-1 project (development and launch of the first Ukrainian satellite), a "Science Slam" movement in Ukraine, and others. During the Workshop there were also talks on modern technologies like 3D-printing and the opportunities they bring. The attendees were able to see how 3D-printing works with their own eyes. The Workshop was held in two different locations, a conference hall in a Dnipropetrovsk restaurant and an anti-cafe, both being very comfortable, creating a very friendly atmosphere for the event.

~ Daniel Tomaszewski, Editor

Asia & Pacific (Region 10)

ED Kansai

—by Michinori Nishihara

The ED Kansai Chapter held a feedback meeting from the 2015 IEDM with students and members from both academia and industries. The meeting was held at the Osaka Institute of Technology Umekita Knowledge Center, in Osaka, Japan, January 20, 2016. The following two researchers reported: Dr. Yoshiharu Yoshii of Murata Manufacturing Co., Ltd., on sensor and neuromorphic devices and Prof. Yoshinari Kamakura of Osaka Iuniversity on modeling and silicon devices as well as overall paper statistics.

Lecturer Dr. Yoshiharu Yoshii

Lecturer Prof. Yoshinari Kamakura

Dr. Yoshii presented a quick review on Sensor Technology and Neuromorphic Devices. There were two sessions devoted to Neuromorphic technology and received strong interest as there are many new applications taking advantage of Deep Learning. Several relatively new memory technologies such as phase change memory or RAM were reported as an element of Neuromorphic devices.

Prof. Kamakura reported on modeling and mainstream silicon technology. There seemed to be more attention on energy efficient device technologies aiming at IoT applications. Sub 60 mV swing FinFET from Taiwan was one example of those papers.

After the IEDM2015 feedback meeting, we held the annual general meeting to review activities of ED Kansai in 2015 and to discuss plans for 2016.

Also discussed was a plan for the upcoming 2016 IMFEDK international conference, which is to be cosponsored with the Microwave Theory and Techniques Society Kansai Chapter on June 23–24, 2016 in Kyoto, Japan. Please check www.imfedk.org for more information.

~Kuniyuki Kakushima, Editor

ED Dalian Chapter

—by Zhengxing Huang

The ED Dalian Chapter organized a seminar about semiconductor gas sensors, January 23-29, 2016. Professor Alexander Gaskov, the director of the semiconductor devices chemical and physical laboratory at Moscow

Prof. Gaskov (left), Prof. Rumyntseva (right)

State University, and Professor Rumyntseva Marina, the recipient of the Young Scholar Award of Moscow State University, were the key speakers. Prof. Gaskov introduced the basic situation of the semiconductor devices chemical and physical laboratory including the equipment and the scientific research project, which is on-going. Then he provided detailed descriptions of achievements in the field of semiconductor gas sensors; more than 20 years of research. Prof. Gaskov's *"Semiconductor Metal Oxide Hetero junction Gas Sensor"* and *"Enrichment Technology for the Detection of Volatile Compounds of Trace Toxic Chemicals,"* were the theme of the lectures. He also put forward the basic ideas and methods of the design of sensitive materials for semiconductor oxide sensors. Prof. Rumyntseva presented a report on the theme *"Promoting Effect of Noble Metal Catalysts on Gas Sensing Properties of Semiconductor Metal Oxide"* and *"In the light of auxiliary, the sensing properties of semiconductor oxide surface-modified by the quantum dots under room temperature."* Prof. Rumyntseva focused on the basic sensing process and mechanism, and deeply revealed the role of noble metal catalysts and quantum dots in the realization of low power semiconductor oxide gas sensors at room temperature.

The seminar was supported by the State Administration of Foreign Experts Affairs (SAFEA) of PRC. About thirty attendees, including most of the IEEE members from our chapter, took part in this seminar.

ED Beijing Chapter

—by Kangwei Zhang

The ED Beijing Chapter has finished the changeover of Chapter Officers, including the Chapter Chair, Vice Chair and Secretary. Replacing Prof. Jinjun Feng, as Chair of the ED Beijing Chapter, a new, qualified and competent Chapter Chair, Prof. Ming Liu from Institute of Microelectronics of the Chinese Academy of Sciences, was elected. Two young professionals, Prof. Qi Liu and Yinfu Hu were also elected as new Chapter Vice-Chairs. Many young engineers and researchers in the Beijing area are joining and helping to make it a better and more youthful chapter. The ED Beijing Chapter is planning to hold the "7th International Conference on Computer Aided Design for Thin-Film Transistors" in Beijing in 2016, and also several local ED technical and social activities with universities and institutes.

ED Guangzhou Chapter

—by Yunfei En

The ED Guangzhou Chapter finished the change of Chapter Officers, including the Chapter Chair and Secretary. Due to the retirement of Prof. Xuedong Kong, former Chair of ED Guangzhou Chapter, a new Chapter Chair, Prof. Yunfei En from China CEPREI Lab., was elected, as well as a new Chapter Secretary, Dr. Zhangang Zhang. Younger engineers and researchers in the Southern China area are joining our chapter and revitalizing it. Activities planned for the remainder of 2016, are two mini-colloquium and co-hosting of several local ED technical and social activities with universities and institutes in Southern China.

ED Taipei (Hsinchu) Chapter

—by Steve Chung

One major event the chapter is involved with is the regional conference, called 2016 IEEE ISNE (International Symposium on Next-Generation Electronics), held May 3–6 at Tsing Hua University, Hsinchu, Taiwan. EDS is a co-sponsor and key members of the local chapter are involved, with paper submissions now completed. The conference program can be accessed via: http://www.isne2016.tw/index.asp.

A historical and important event is the WIMNACT-50, which marked the 50th in its series since its kick-off in early 2000. The event will be held in the afternoon of May 3rd, with 4 invited Distinguished Lecturers and free to all registered participants of ISNE.

ED Xi'an Chapter

—by Yuming Zhang

The "First Chinese Microelectronics Youth Science and Technology Forum" was held at Xidian University in Xi'an, Shaanxi, November 3–5, 2015. There were more than 20 young participants from all over the nation. This forum was co-hosted by the ED Xi'an Chapter and the School of Microelectronics, Xidian University.

On November 3rd, Prof. Genquan Han gave a presentation on how to improve during researches. Later on, participants had a discussion with young teachers of Xidian University.

On the second day, the meeting was opened with welcoming remarks by Prof. Yue Hao, Vice President of Xidian University and Member of Chinese Academy of Science, followed by an overview presented by Prof. Yuming Zhang, Dean of the School of Microelectronics of Xidian University. Prof. Xiaochen Dong of Nanjing Technology

University gave a talk entitled *"Nanoelectronic Biosensor and Photodynamic Therapy,"* which was followed by another talk on *"Nonvolatile Memory Based on Few-Layer Materials,"* by Prof. Peng Zhou of Fudan University, Shanghai. Prof. Fengqiu Wang from Nanjing University spoke on *"Hish-performance Photodetectors Based on Planar SWNT/graphene Hybrid Film. "*The final talk was given by Prof. Chunfu Zhang of Xidian University on *"the Organic Solar Cell Electrodes and Interface Engineering."*

~ Ming Liu, Editor

Activities by SUTD Student Branch: Makerfaire 2016 and Open House 2016

ED Singapore University of Technology and Design (SUTD) Student Branch Chapter

—by Navnidh Bhalla

The Singapore University of Technology and Design (SUTD) IEEE Student Branch participated in Makerfaire 2016, where the student branch worked with other specialist clubs and showcased our illuminating conductive paint mural. Thereafter, in early March, we setup an IEEE publicity booth at our university's Open House. Through this endeavor, we managed to publicize IEEE to approximately 100+ members of the public. In mid-March, we also attended the Singapore IEEE GenCo event held at Marina Bay Sands. In May, we carried out a membership recruitment drive, hosting our signature Arduino workshop and sending representatives from our student branch to be May Day Rally Flag Bearers for IEEE. We look forward to welcoming the second quarter of 2016 and championing the cause of IEEE even further.

Singapore Reliability/CPMT/ED Chapter

—by Dave Tan

The chapter hosted the EDS Governance Meeting Series from May 29–June 1, 2015, at Marina Mandarin Hotel, where local hospitality was provided for the delegates. We also hosted and co-sponsored the ExCom dinner at the Sky on 57 of Marina Bay Sands. This was followed by the 2015 IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC'2015) held in Singapore for the first time at NTU, June 1–4 2015. The week was rounded off when the 47th Workshop and IEEE EDS Mini-colloquium on NAnometer CMOS Technology (WIMNACT-47) was held on June 5th with 11 distinguished lecturers (DLs) giving their talks at 3 local universities (NUS, NTU, SUTD) simultaneously.

The chapter also organized two technical talks, one by Prof. Mahesh Patil of IIT-Bombay on June 12, 2015, titled *"Applications of Particle Swarm Optimization for Device Modeling and Circuit Design,"* and the other by Prof. Cary Yang of Santa Clara University on July 2, 2015, with a topic on *"Metal-CNT Contacts."* Both seminars were co-hosted by the NOVITAS, Nanoelectronics Centre of Excellence, at the School of EEE, NTU.

The chapter then organized a social and humanity event with the movie screening of "Minions" on June 20, 2015. A total of 165 participants attended the event, with 80 children and their guardians coming from Chen Su Lan Methodist Children¹s Home and Gracehaven. The rest of the attendees are from our committee and society members with their families. Before the movie, we arranged dinner for everyone at the Pepper Steakhouse & Bistro.

ED Malaysia Kuala Lumpur Chapter

—by Badariah Bais & Siti Noorjannah Ibrahim

The first EDS Chapter meeting was held on the 4th of March 2016 in UKM and was attended by 10 committee members and volunteers. Many items were discussed at the meeting, including portfolios for the committee members, ICSE2016 conference, Professional Skills Workshop, DL/

Chapter members before the movie screening

Speakers of ICDCS'16

Technical programs, Student Awards, EDS-ETC Educational outreach, Senior Member Elevation Workshop, formation of ED student branch and community engagement projects. The chapter would like to continue their achievements for 2016.

The ED Malaysia Final Year Project (FYP) Poster Competition 2016 was held on the 26th January 2016 at the Kulliyyah of Engineering, IIUM. A total of 52 posters were presented and the winner for the award was Mr. Muhammad Jabrullah Johari with his poster entitled: "Design and Simulation of MEMS HEMHOLTZ Resonator with Piezoelectric Cantilever for Acoustic Energy Harvesting". He was supervised by Dr. Rosminazuin Abdul Rahim.

On the 12th of March 2016, the 2016 IEEE Malaysia Section Leadership Camp was held at the Grand Blue Wave Hotel, Shah Alam. The chapter was represented by the chapter chair, secretary and treasurer. The leadership camp was organized to provide training to the chapter volunteers in managing and organizing activities.

~P. Susthitha Menon, Editor

ED Coimbatore

—by D. Nirmal

The chapter organized the 3rd International Conference on Devices, Circuits and Systems, March 3–5, 2016, in the Department of ECE, Karunya University, Coimbatore. The Inaugural function was followed by the key note talk by Dr. Christian Teichert on, *"Exploring the potential of graphene as transparent electrode material for organic semiconductor devices."* Dr. Rajendra Singh gave a key note talk on *"Photovoltaics, Battery and Internet of Things Manufacturing for Transformation Of Global Electricity and Transport Sectors."*

The afternoon session began with paper presentations by eminent people from National Applied Research Laboratories, Taiwan, Saudi Arabia, University of Western Australia, Kirkuk University, Iraq, and various Indian government research agencies, with participants from 14 different Indian states. The second conference day combined sessions for ICDCS and the National Workshop on Recent Research Trends in Nano Scale Devices, Circuits and Systems. Dr. N. Mohan Kumar, Professor, SKP Engineering College, Tiruvannamalai and IEEE EDS Madras Chair, gave a guest lecture on *"GaN, InAs and GaSb based Tera-Hertz Electronics for Biomedical Sensing and Imaging applications,"* followed by a guest lecture on *"GCGS-DGMOSFETs is a prospective device for Nanoscale CMOS Technology"* by Prof. Chandan K. Sarkar, Jadavpur University, Kolkatta and EDS Distinguished Lecturer, which was attended by more than 80 people. Dr. Christian Teichert, Associate Professor, Institute of Physics, Montan Universitaet, Leoben delivered a guest lecture on *"Atomic Force Microscopy."* Dr. D. Nirmal gave a lecture on *"Applications of high power and low power devices"* followed by a visit to the NEMS/MEMS lab and other research facilities.

ED Nepal Chapter

—by Bhadrapokharel

On January, 11, 2016, Dr. Moritz-Caspar Schlegel, Research Scientist, Federal Institute for Materials Research & Testing, Berlin, Germany, gave an invited talk on *"In-Situ Structure Analysis of Nano-Porus materials Molecules Trapped in Crystal Cages,"* at Pulchowk Campus, Institute of Engineering Pulchowk, Lalitpur, Nepal. Around thirty-three physicists, chemists, engineers and students attended. Dr. Moritz stressed the importance of nano-porous materials for device fabrication and the role of structure in their properties. The program was supported by the Department of Engineering Science and Humanities, Pulchowk, with dinner hosted by Golden Gate International College, Kathmandu.

Dr. Moritz-Caspar Schlegel at Institute of Engineering Pulchowk

ED National Institute of Technology Calicut Student Branch

—by Akshay K.

The chapter organized a Distinguished Lecture technical talk on *"Engineering Evolution in Electronics and 50 years of Moore,"* by Dr. M. K. Radhakrishnan, January 19, 2016 at the ECE department of NIT Calicut. An audience of 60 students and faculty members listened to Dr. Radhakrishnan discuss the evolution of the field of electronics engineering, beginning with vacuum tubes to present day ICs. He explained the growth of the electronics industry and the need for miniaturization of semiconductor devices. His talk was followed by the chapter's ExCom meeting, which Dr. Radhakrishnan also attended.

On February 25, 2016, the first session of the "Talk of the Month" series was given by Akshay K., EDS Student Branch Chair of NIT Calicut, in the ECE department seminar hall on the topic *"Transparent electronics."* The talk covered various aspects of the emerging field of transparent electronics from its atomic scale development to research possibilities. This talk garnered a large audience of about 80 undergraduates, post graduates, PhD scholars and faculty of various departments of the institute.

The second installment of the "Talk of the Month" series was conducted on March 10, 2016 on *"Electronics and genetic engineering"* by Reshma V. R., a 4th year ECE student of NIT Calicut. Through her one-hour talk she gave information on how electronic circuits can be used in the genetic engineering field for modelling gene activities (protein synthesis) in living cells, by using circuits designed to work analogous to protein synthesizing mechanisms of genes.

ED IIT Roorkee Student Chapter

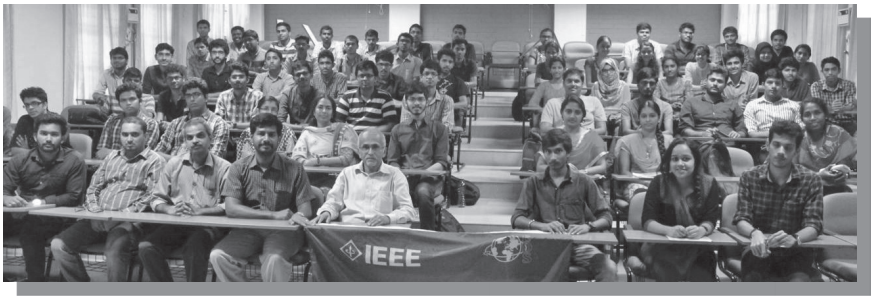
—by Om Prakash and Arvind Sharma

The chapter and IIT-Roorkee Circuits and Systems Student Branch Chapter jointly organized a Distinguished Lecture on *"Technology Circuit Co-Design for Low Power Design"* by Dr. Rajiv V. Joshi, Research Staff Member, T. J. Watson Research Center, January, 22, 2016. The event was successfully held in the Department of ECE, IIT Roorkee. Dr. Joshi discussed the pros and cons analysis on technology from power perspective and various techniques to exploit lower power. Further, he talked about the reliability and different power optimization techniques for logic and memory cells. Around 60 participants including Faculty, Research Scholars and graduate students from IIT Roorkee, attended this lecture.

AP/ED Bombay Chapter

—by V. Ramgopal Rao

The IEEE AP/ED Bombay Chapter, IIT Bombay, organized several technical talks by speakers belonging to both academia and industry. Prof. Yong Chen from Purdue University; Dr. Arul Kumar, IMEC, Belgium; Prof. C. Y. Chang, National Chiao Tung University, Taiwan; Prof. Hiroshi Iwai, Tokyo Institute of Technology, Japan; Prof. Edward Yi Chang, National Chiao Tung University, Taiwan; Prof. Dirch Hjorth Petersen, Technical University of Denmark; Prof. Subodh Mhaisalkar, Nanyang Technological University, Singapore; Prof. Srinivas Tadigadapa, The Pennsylvania State University, USA and Prof. Durga



Dr. Radhakrishnan (first row, fifth from left) with audience

Dr. Rajiv V. Joshi (1st left, behind banner), and attendees at the joint EDS and CAS DL held at IIT Roorkee

Misra, New Jersey Institute of Technology, Newark, USA, were some of the speakers who through their talks, shared their perspectives on various research topics.

Some of the talks given were:

- Prof. Yong Chen, *"What are topological insulators good for?"* Prof. Chen reviewed the key electronic properties and device potentials of Tis and presented his recent experimental demonstration of the most intrinsic TI so far.
- Prof. Dirch Hjorth Petersen, in his talk titled, *"Microprobe based metrology for magnetic tunnel junctions – monitoring MRAM production,"* discussed recent innovations in the CIPT method, including advanced data analysis to boost precision on blanket films, adaptation to small test pads and vibration tolerant microelectrodes.
- Prof. Srinivas Tadigdapa emphasized that micromachining quartz offers various new configurations and advantages for gravimetric, thermal, viscoelastic, and magnetic sensing in his talk titled, *"Quartz MEMS - Only a matter of Time!"*
- Prof. Durga Misra delivered a talk on *"Dielectric-Semiconductor Interface with High-k Gate Dielectrics."* He outlined some of the recent developments of EOT scaling of high-k gate dielectrics on silicon and germanium and how it impacts the interface; and the challenges of obtaining an acceptable interface for high-k on high mobility substrates.

ED VIT Chennai Student Branch

—by B. Lakshmi

The chapter organized a one-day *workshop on "Characterization, Modeling and Reliability Issues on Nano Materials and Devices,"* March 2, 2016. The workshop was attended by 19 external participants and 60 internal participants, who enjoyed four expert talks. Dr. Kaustab Ghosh discussed the Fundamental concepts on quantum mechanics for nanoelectronic device modeling; Prof. Cher Ming Tan enlightened the audience on the frontier areas of Statistical Analysis of Reliability Test Data; Dr. Gargi Raina's talk focused on Nanolithography Techniques for Novel Nanomaterials & related Issues; concluding with Dr. Karmalkar S. speaking on the topic of *"Modeling and simulation of the effects of ambient field in nanoscale junctions and FETs."*

Prof. Cher Ming Tan giving a talk on "Statistical Analysis of Reliability Test Data"

ED NIST Student Chapter

—by Ajit Kumar Panda

The chapter organized a one-day seminar on *"Devices for Internet of Things,"* February, 17, 2016, at National Institute of Science & Technology, Palur Hill, Berhampur, for the young faculties/researchers to enhance the research activity. Professor Ganapati Panda, School of Electrical Sciences, IIT-Bhubaneswar, discussed different methods for solving the real-life problems like providing correct information regarding the plants to the farmers at proper time to improve the grain quality, preparing intelligent sensors for biomedical applications and signal processing, cyber security and many more. Thirty participants, including faculties and M.Tech students, attended the seminar from their parent institutes.

The chapter also organized the *"Second National Conference on Devices and Circuits,"* February, 19, 2016, at National Institute of Science & Tech-

Professor Ganapati Panda with participants

Audience of Second National Conference on Devices and Circuits

nology, Palur Hill, Berhampur. Thirty-three research papers were presented by university/institute scholars from the Institute of Radio Physics, Calcutta University, VSSUT-Burla, Sambalpur University, KIIT University, SOA University, Berhampur University, Indira Institute of Management-Pune. Two papers selected as the best paper presentation were entitled *"Mobility Modulation in Delta Doped Coupled Double Quantum Well-Field Effect Transistor,"* by Narayan Sahoo, Berhampur University and *"A Comparison of Three State-of-Art Heterojunction Bipolar Transistor (BJT); The AlGaAs/ GaAs HBT, the InGaAs/InP HBT and InP/InGaAs/InP Double HBT,"* by M. R. Jena and S. Mohapatra, VSSUT-Burla.

Participants of STTP at NIT Silchar with (from left) Dr. K. L. Baishnab, Prof. S. Dhar, Prof. S. Baishya, Dr. T. R. Lenka (Faculty Advisor ED NIT Silchar SBC) and Rupam Goswami (Student Chair)

ED Hyderabad Chapter

—by Mohammed Arifuddin Sohel

The chapter organized a Distinguished Lecture by Prof. Vijay K. Arora, Wilkes University, USA, on the topic *"Quantum Nano engineering -Non equilibrium High-Electric-Field Transport for Signal Propagation,"* at Osmania University, December 19, 2015, which was attended by 25 participants. The Chapter also organized a one-day workshop on "*Carbon the soul of Future Nano electronics,"* by Prof. Vijay K. Arora, at Hotel Karat Longspur, Begumpet, December 20, December 2015. It was attended by 15 participants.

ED National Institute of Technology Silchar Student Branch

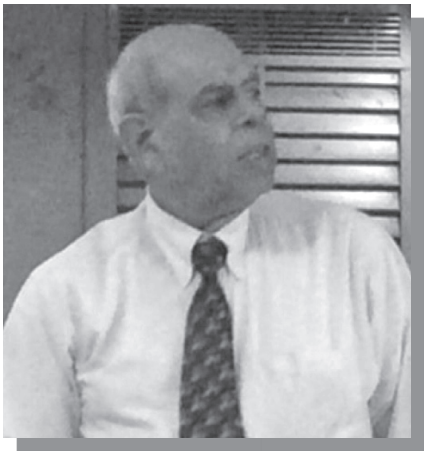
—by Trupti Ranjan Lenka

The IEEE ED NIT Silchar Student Branch Chapter in association with Department of Electronics and Communication Engineering, NIT Silchar, organized the *One Week Self-Financed Short Term Training Program on "Microelectronics and VLSI Design,"* March 21–26, 2016. A total of 37 participants, including IEEE members and non-members, comprising of B.Tech/M.Tech/PhD scholars of NIT Silchar and Assam University, Silchar, attended the program. The course coverage was Semiconductor device physics, VLSI Design, IC Fabrication Technology and Hands on Laboratory on EDA tools, Silvaco/Synopsys TCAD tool etc. Professor S. Baishya, Dr. T. R. Lenka, Prof. S. Dhar, Dr. K. L. Baishnab and Dr. Brinda Bhowmick were the resource persons for the program.

ED HITK Student Branch

—by Anindya Sen, Mousiki Kar and Atanu Kundu

On February 15, 2016, the chapter organized a technical talk by Dr. Nabarun



Dr. Vijay Arora delivering his Distinguished Lecture for the ED Hyderabad Chapter

Dr. Nabarun Bhattacharyya (from left) of CDAC and Prabir Bannerjee, HOD, ECE, HITK

Bhattacharyya, Associate Director at the Centre for Development of Advanced Computing (C-DAC), Kolkata, India, on the topic *"Artificial Olfaction–The Emerging Frontier of Electronic Perception,"* at the ECE Department, Heritage Institute of Technology. This was in joint sponsorship by the TEQIP II program for Industry and Institute interaction and the IEEE ED Kolkata Section. The talk was attended by over 175 attendees, which included third and final year ECE students and faculties.

Participants along with Prof. Durga Misra (fourth from right) at A. K. Choudhury Auditorium

ED Calcutta Chapter

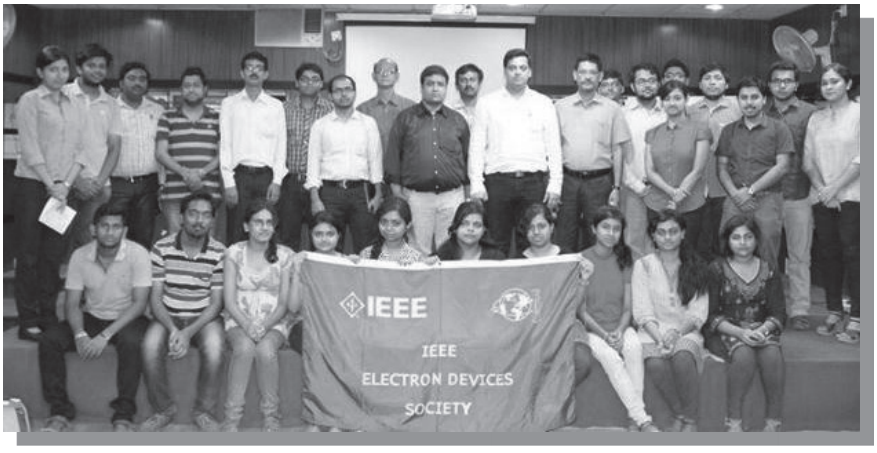
—by Atanu Kundu and Swapnadip De

and

ED Meghnad Saha Institute of Technology Student Branch Chapter

—by Manash Chanda and Swapnadip De

A one-day workshop on "VLSI Design and Microelectronics" was organized by the IEEE Meghnad Saha Institute of Technology Student Branch, and the IEEE Meghnad Saha Institute of Technology EDS Student Branch Chapter, in association with the IEEE EDS Calcutta Chapter, the IEEE HITK EDS Student Branch Chapter and the Department of ECE, Meghnad Saha Institute of Technology, March 21, 2016, at Meghnad Saha Institute of Technology. Dr. Writam Banerjee, Assistant Professor of the Institute of Microelectronics, Chinese Academy of Science, P. R. China, delivered a technical talk in the workshop. The program was attended by 51 participants.



Dr. Writam Banerjee with the participants of the VLSI Design and Microelectronics workshop

ED University of Calcutta Student Branch Chapter

—by Sarmista Sengupta and Soumya Pandit

On January 11, 2016, the chapter organized a Distinguished Lecture on *"Dielectric-Semiconductor Interface with High-k Gate Dielectrics for Nanoscale CMOS Technology,"* by Prof. Durga Misra, Electrical and Computer Engineering, New Jersey Institute of Technology, Newark, USA, at A. K. Choudhury Auditorium, Institute of Radio Physics and Electronics, University of Calcutta. The lecture contained details of the Low power requirements for semiconductors of high-k metal gates and FinFETs in CMOS technologies and device scaling for sub-14 nm CMOS technology (More Moore) and EOT scaling of gate dielectric beyond 0.7 nm. Various atomic layer deposition (ALD) methods of HfO2-based high-k gate dielectrics (e.g., cyclic deposition) and how it impacts the interface; and the challenges of obtaining an acceptable interface for high-k on high mobility substrates were discussed. About 55 students, several Ph.D. research scholars and 10 faculty members attended the seminar.

ED Delhi Chapter

—by Manoj Saxena and Rakhi Narang

On January 8, 2016, the chapter organized a short course on "*Quantum Transport in Carbon-Based Devices,"* by Prof. Vijay K. Arora, Wilkes University, USA, Universiti Teknologi Malaysia at University of Delhi South Campus, New Delhi, which was attended by 100 students and faculty members.

On January 13, 2016, a distinguished lecture on *"Creating a Perfect Dielectric-Semiconductor Interface with High-k Gate Dielectrics for sub-14 nm CMOS Technology"* by Prof. Durga Misra, Electrical and Computer Engineering Department, New Jersey Institute of Technology (NJIT), Newark, USA, was organized at the University of Delhi South Campus, New Delhi, and attended by 70 students and faculty members.

On January 15, 2016, Prof. Mridula Gupta, Chairperson IEEE EDS Delhi Chapter delivered a technical talk on *"Advancements in Semiconductor Device Technology: Modeling and Simulation,"* at Jammu University,

Speakers and participants of DL at University of Delhi South Campus

Jammu, which was attended by over 30 participants.

On January 15, 2016, a technical talk on "Asynchronous Circuit Design and CAD Tool Design for Asynchronous Circuits" was delivered by Ms. Tannu Sharma, Graduate Research Assistant at University of Utah, Vice Chair-IEEE Student Chapter University of Utah and Formerly Senior Application Engineer, Cadence Design Systems. The talk was organized at Deen Dayal Upadhyaya College and attended by over 50 undergraduate students.

On March 12, 2016, the chapter jointly organized the Department of Electronic Science, University of Delhi South Campus Annual Visitors' Program, which was attended by 100 students and a few faculty members. There were four technical talks: Next Generation Optical Transport Networks by Sh. Vikas Jain, General Manager, Huawei Telecommunications (India) co. Pvt. Ltd; Gurgaon. Prof. Subhasis Ghosh, School of Physical sciences, JNU, New Delhi, delivered his talk on Nano science and Nanotechnology; Sh. Shashi Bhushan Taneja, Director, Institute for Systems Studies and Analyses, New Delhi, gave a talk on Constructive Simulation: Overview and design considerations; and Digital broadcasting-Emerging technologies by Sh. I. L George, Addl. Director General (Training), National Academy of Broadcasting and Multimedia, Delhi.

The chapter jointly organized the annual Techfest 'URJASVA'16' of Department of Electronics, Deen Dayal Upadhyaya College, University of Delhi, January 22–23, 2016, in which over 200 students participated from different colleges of the University of Delhi.

During March 13–14, 2016, the chapter jointly organized Third Workshop On "Quantum Mechanics: Theory and Application" with Silizium-Electronics Society-Department of Electronics-Deen Dayal Upadhyaya College (University of Delhi), and The National Academy of Sciences, India (NASI) – Delhi Chapter. The lectures covered Evolution of quantum theory; Heuristic derivation of the Schrödinger equation; free particle solution of the Schrödinger equation and applications of quantum mechanics in Nanoscale Electronics. The workshop was attended by over 140 undergraduate students.

The Department of Applied Physics, Delhi Technological University (DTU), in association with the ED Delhi Chapter, organized the One Day National Seminar on Frontier in Applied Science and Technology (FAST) on March 22, 2016. Professor Yogesh Singh, Vice-Chancellor, DTU and Professor K. L. Chopra gave the Inaugural Address and Keynote address respectively. Other speakers were Professor Ajoy Ghatak, Formerly with Department of Physics, IIT Delhi; Professor M. P. Shrivastava, Formerly with Department of Physics and Astrophysics, University of Delhi; Dr. Seema Vinayak, Associate Director, SSPL, DRDO, New Delhi; Professor Avinash Khare, Department of Physics and Astrophysics, University of Delhi; Professor Suresh C Sharma, Head, Department of Applied Physics, DTU; Professor V. D. Vanker, Department of Physics, IIT Delhi and Professor Sudhir Chandra, Centre for Applied Research in Electronics (CARE), IIT Delhi.

IEEE SJCE Student Branch—Sri Jayachamarajendra College of Engineering, Mysuru

—by Akshay Kumar C.

The Robotics 7.1 workshop was hosted by the EDS chapter of IEEE SJCE Student Branch. The focus of the workshop was on using low

Robotics 7.1 Participants and Volunteers

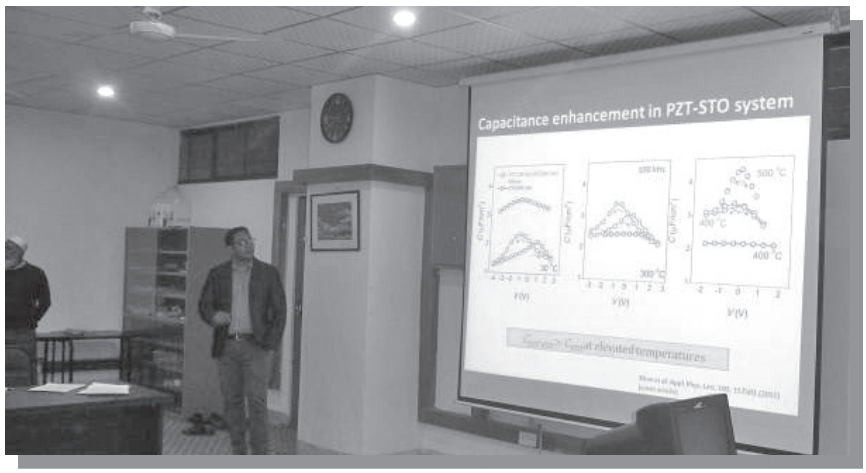
power board and introducing the advanced embedded systems to the participants. Forty-two teams (maximum 4 members to a team) registered, with 165 participants and 20 volunteers attending the workshop. Sample codes, hardware (development boards, IR sensors) debugging, software installation, teaching of basic concepts, debugging the user code were all carried out by the volunteers themselves. The show stealer was a voice-controlled robot session, in which students were introduced to Jarvis (speech recognition software) and used it to set their custom commands and corresponding response from it. A demo of using Jarvis to control a robot was jaw dropping.

The Chapter also organized an EDS Distinguished Lecture by Dr. Durga Misra on "CMOS High-k Gate Stacks to Nanotechnology" on March 8, 2016, in the E & C Department, which was attended by 80 IEEE members.

ED/SSCS Bangladesh Chapter

—by Md. Ziaur Rahman Khan

The ED/SSC Bangladesh Chapter and Department of EEE, BUET, jointly organized a technical talk on *"Beyond-CMOS Nanoelectronics with Ferroelectrics, Complex Oxides and Negative Capacitors,"* January 11, 2016, at the Department of EEE, BUET. The talk was given by Dr. Asif Islam Khan, Post-doctoral Research Associate, UC Berkeley, with a total 28 participants (12 of whom were IEEE members).



Dr. Asif giving his talk at BUET

The chapter and Department of EEE, BUET, jointly organized a technical talk on *"Electronic Application of van der Waals Heterostructure Devices,"* January 18, 2016, at the Department of EEE, BUET. The talk was given by Ahmad Zubair, PhD Student, Department of EECS, Massachusetts Institute of Technology. Total 18 participants, including 9 IEEE members attended the talk.

The chapter and Department of EEE, BUET, also jointly organized a technical talk on *"Spintronic Logic Circuit and Device Prototypes Utilizing Domain Walls,"* January 18, 2016, at the Department of EEE, BUET. The talk was given by, Saima Afroz Siddiqui, PhD Student, Department of EECS, Massachusetts Institute of Technology. A total of 18 participants with 10 IEEE members were present.

~Manoj Saxena, Editor

EDS MEETINGS CALENDAR

THE COMPLETE EDS CALENDAR CAN BE FOUND AT OUR WEB SITE: HTTP://EDS.IEEE.ORG. PLEASE VISIT.

2016 23rd International Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD)	6-8 Jul 2016	Ryukoku University Avanti Kyoto Hall 31 Nishi Sanno-cho Higashi Kujo, Minami-Ku Kyoto, Japan
2016 29th International Vacuum Nanoelectronics Conference (IVNC)	11-15 Jul 2016	University of British Columbia Earth Sciences Building 2207 Main Mall Vancouver, BC, Canada
2016 Lester Eastman Conference (LEC)	2-4 Aug 2016	Lehigh University Dept. of ECE 19 Memorial Drive West Bethlehem , PA, USA
2016 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)	3-5 Aug 2016	The University of Hong Kong Hong Kong
2016 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)	6-8 Sep 2016	Le Meridien Grand Hotel Bahnhofstrasse 1 Nuremberg, Germany
2016 e-Manufacturing and Design Collaboration Symposium (eMDC)	9 Sep 2016	The Ambassador Hotel Hsinchu Hsinchu, Taiwan
2016 38th Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD)	11-16 Sep 2016	Hyatt Regency Garden Grove, CA, USA
ESSDERC 2016 - 46th European Solid-State Device Research Conference	12-14 Sep 2016	SwissTech Convention Center Ecole Polytechnique Fédérale Lausanne, Switzerland
2016 IEEE Bipolar/BiCMOS Circuits and Technology Meeting - BCTM	25-27 Sep 2016	Hyatt Regency New Brunswick 2 Albany Street New Brunswick, NJ, USA
2016 European Conference on Silicon Carbide & Related Materials (ECSCRM) Full Paper Submission deadline: 16 Sep 2016 Final submission deadline: 02 Dec 2016 Notification of acceptance date: 28 Oct 2016	25-29 Sep 2016	PORTO CARRAS Sithonia Halkidiki Neos Marmaras, Greece

2016 11th European Microwave Integrated Circuits Conference (EuMIC)	3-5 Oct 2016	ExCeL London One Western Gateway Royal Victoria Dock London, United Kingdom
2016 IEEE International Integrated Reliability Workshop (IIRW) Abstract submission deadline: 11 Jul 2016 Final submission deadline: 09 Oct 2016 Notification of acceptance date: 14 Aug 2016	9-13 Oct 2016	Stanford Sierra Conference Center 130 Fallen Leaf Road South Lake Tahoe, CA, USA
2016 International Semiconductor Conference (CAS) Full Paper Submission deadline: 28 May 2016 Notification of acceptance date: 19 Jul 2016	10-12 Oct 2016	Rina Sinaia hotel 8, Carol I str Sinaia, Romania
2016 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)	10-13 Oct 2016	Hyatt Regency San Francisco Airport 1333 Bayshore Highway Burlingame, CA, USA
2016 16th Non-Volatile Memory Technology Symposium (NVMTS)	17-19 Oct 2016	Carnegie Mellon University 5000 Forbes Ave Pittsburgh, PA, USA
2016 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)	23-26 Oct 2016	Doubletree by Hilton Austin 6505 N IH 35 Austin, TX, USA
2016 7th International Conference on Computer Aided Design for Thin-Film Transistor Technologies (CAD-TFT)	26-28 Oct 2016	To be determined Beijing, China
2016 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)	7-10 Nov 2016	Doubletree by Hilton Hotel Austin 6505 N. Interstate 35 Austin, TX, USA
2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA) Abstract submission deadline: 10 Jul 2016 Full Paper Submission deadline: 25 Sep 2016 Final submission deadline: 25 Sep 2016 Notification of acceptance date: 21 Aug 2016	7-9 Nov 2016	Hilton Garden Inn 1325 North Palak Drive Fayetteville, AR, USA
2016 11th International Conference on Advanced Semiconductor Devices & Microsystems (ASDAM) Final submission deadline: 15 Oct 2016 Notification of acceptance date: 15 Jul 2016	13-16 Nov 2016	Smolenice Castle Zámocká Smolenice, Slovakia
2016 IEEE International Electron Devices Meeting (IEDM) Abstract submission deadline: 10 Aug 2016	3-7 Dec 2016	Hilton San Francisco Union Square 333 O'Farrell St. San Francisco, CA, USA

2016 IEEE 47th Semiconductor Interface Specialists Conference (SISC) Abstract submission deadline: 14 Aug 2016 Notification of acceptance date: 18 Sep 2016	7-10 Dec 2016	Catamaran Resort Hotel 3999 Mission Blvd. San Diego, CA, USA
2016 International Symposium on Semiconductor Manufacturing (ISSM) Abstract submission deadline: 31 Aug 2016 Full Paper Submission deadline: 11 Nov 2016 Final submission deadline: 11 Nov 2016 Notification of acceptance date: 23 Sep 2016	12-13 Dec 2016	KFC Hall 1-6-1 Yokoami Sumida-ku Tokyo, Japan
2016 3rd International Conference on Emerging Electronics (ICEE)	27-30 Dec 2016	Indian Institute of Technology Bombay, Powai Mumbai, India
2017 IEEE International Reliability Physics Symposium (IRPS) Abstract submission deadline: 30 Sep 2016 Final submission deadline: 01 Feb 2017 Notification of acceptance date: 21 Dec 2016	2-6 Apr 2017	Hyatt Regency Monterey One Old Golf Course Road Monterey, CA, USA
2017 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD)	28 May - 1 Jun 2017	Royton Sapporo Kita 1 jyou nishi 11-1 Chuo-ku Sapporo, Japan
2017 IEEE 44th Photovoltaic Specialists Conference (PVSC)	25-30 Jun 2017	Marriott Washington Wardman Park 2660 Woodley Road NW Washington, DC, USA
2017 International Siberian Conference on Control and Communications (SIBCON) Abstract submission deadline: 28 Feb 2017 Final submission deadline: 28 Apr 2017 Notification of acceptance date: 28 Mar 2017	29-30 Jun 2017	Sultanbek S. Isenov KATU Pobedy Ave., 62 Astana, Kazakhstan
2017 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS) Abstract submission deadline: 21 Apr 2017 Final submission deadline: 21 Jul 2017 Notification of acceptance date: 14 Jul 2017	22-25 Oct 2017	Miami Marriott Biscayne Bay 1633 N. Bayshore Drive Miami, FL, USA
2017 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)	12-16 Nov 2017	Irvine Marriott 18000 Von Karman Ave. Irvine, CA, USA
2017 IEEE International Electron Devices Meeting (IEDM)	4-6 Dec 2017	Hilton San Francisco Union Square 333 O'Farrell St. San Francisco, CA, USA

2018 IEEE International Reliability Physics Symposium (IRPS) Abstract submission deadline: 10 Oct 2017 Full Paper Submission deadline: 01 Jan 2018 Final submission deadline: 10 Jan 2018 Notification of acceptance date: 15 Dec 2017	11-15 Mar 2018	Hyatt Regency San Francisco Airport 1333 Bayshore Highway Burlingame, CA, USA
2018 IEEE 30th International Symposium on Power Semiconductor Devices and IC's (ISPSD) Abstract submission deadline: 31 Oct 2017 Full Paper Submission deadline: 31 Mar 2018 Final submission deadline: 31 Mar 2018 Notification of acceptance date: 31 Dec 2017	13-17 May 2018	Palmer House Hilton 17 East Monroe Street Chicago, IL, USA
2018 IEEE Symposium on VLSI Technology	12-14 Jun 2018	Hilton Hawaiian Village Beach Resort & Spa 2005 Kalia Rd. Honolulu, HI, USA
2018 IEEE International Electron Devices Meeting (IEDM)	29 Nov - 7 Dec 2018	Hilton San Francisco Union Square 333 O'Farrell St. San Francisco, CA, USA

EDS Vision and Mission Statements

Vision Statement
Promoting excellence in the field of electron devices for the benefit of humanity

Mission Statement
To foster professional growth of its members by satisfying their needs for easy access to and exchange of technical information, publishing, education, and technical recognition and enhancing public visibility in the field of Electron Devices.

Field of Interest
The field of interest for EDS is all aspects of engineering, physics, theory, experiment and simulation of electron and ion devices involving insulators, metals, organic materials, plasmas, semiconductors, quantum-effect materials, vacuum, and emerging materials. Specific applications of these devices include bioelectronics, biomedical, computation, communications, displays, electro and micro mechanics, imaging, micro actuators, optical, photovoltaics, power, sensors and signal processing.

The society is concerned with research, development, design and manufacture related to the materials, processing, technology, and applications of such devices, and scientific, technical, educational and other activities that contribute to the advancement of this field.